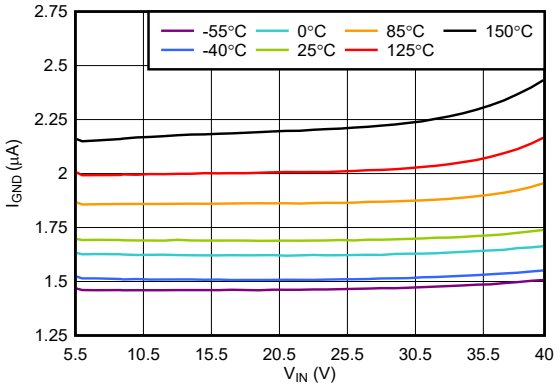
TPS7B92 300mA, 40V, 1.8µA I_Q, Low-Dropout Linear Regulator

1 Features

- Input voltage range: 2.5V to 40V
- Output voltage range: 1.2V to 12V
- Output current: 300mA
- Ultra-low I_Q: 1.8µA at I_{OUT} = 0mA
- Stable with output capacitors ≥ 1.0µF
- High PSRR:
  - 70dB at 1kHz
  - 43dB at 100kHz
- Fold-back current limiting
- Overtemperature protection
- Package:
  - 5-pin SOT-23 (DBV)
- Operating junction temperature: –40°C to +125°C

2 Applications

- Appliances
- Home and building automation
- Retail automation and payment
- Grid infrastructure
- Medical applications
- Lighting applications



I_{GND} vs V_{IN} (V_{OUT} = 5.0V, I_{OUT} = 0mA)

3 Description

The TPS7B92 low-dropout (LDO) linear voltage regulator is a low quiescent current device. The TPS7B92 offers a wide input voltage range (up to 40V), wide output range, and low-power operation in miniaturized packaging. The wide output range is from 1.2V to 12V.

The TPS7B92 is optimized to power microcontrollers and other low power loads for battery-powered applications. The TPS7B92 is stable with a output capacitor range of 1.0µF to 47µF.

The TPS7B92 low quiescent current (1.8µA typically) makes this device designed for battery-powered or always-on systems that require very little idle-state power dissipation.

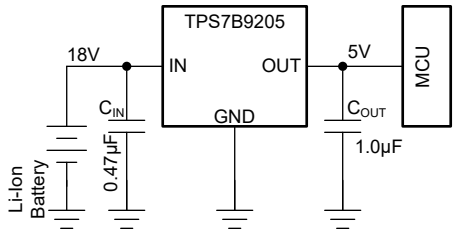
The TPS7B92 LDO supports a low dropout of typically 900mV at 150mA of load current. The TPS7B92 also features an internal soft-start to lower the inrush current during start-up. The built-in foldback overcurrent limit protection and thermal shutdown help protect the regulator in the event of a load short or fault condition.

The TPS7B92 is available in a 2.9mm × 2.8mm, 5-pin SOT-23 (DBV) package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7B92	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

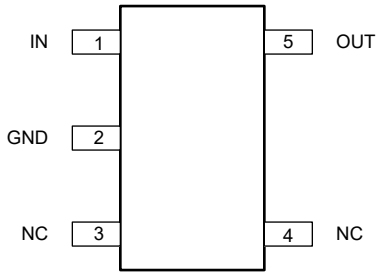


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DBV		
GND	2	—	Ground pin.
IN	1	I	Input supply pin. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section for more information.
OUT	5	O	Output of the regulator. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section for more information.
NC	3, 4	—	Not internally connected. Leave this pin open or connected to any potential. Tie this pin to ground for improved thermal performance.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage (2)	V_{IN}		–0.3	42	V
	V_{OUT}		–0.3	$2 \times V_{OUT(typ)}$ or V_{IN} + 0.3 or 15 (whichever is lower)(2)	V
Power dissipation (3) (4)	SOT-23 (DBV)	T_A = –55°C		1.775	W
		T_A = +25°C		1.375	
		T_A = +125°C		0.875	
Current	V_{OUT}		Internally limited		A
Temperature	Operating junction, T_J		–55	125	°C
	Storage, T_{stg}		–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminal.
(3) The power dissipation rating is defined as the continuous peak power that is dissipated across a voltage regulator over a 24-hour period. This rating represents the maximum amount of heat energy that the voltage regulator handles without exceeding safe operating limits during continuous operation.
(4) The power dissipation values mentioned in *Absolute Maximum Ratings* are PCB mounted and is for reference only. The PCB configuration is based on JEDEC standard of 2s2p configuration (EIA/JESD51-x).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		40	V
V_{OUT}	Output voltage(1)	1.2		12	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor (2)		0.47		µF
C_{OUT}	Output capacitor (3)	1		47	µF
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitance with an effective value of 0.1 µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of systemlevel instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values listed are the nominal value and the effective capacitance is assumed to derate to 50% of the nominal capacitor value.

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5.4 Thermal Information

THERMAL METRIC[1]		TPS7B92 DBV (SOT-23) [2] 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	40.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	73.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters are further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application note.

5.5 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted); typical values are at T_J = 25°C [1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			2.5		40	V
I_{OUT} [2] [3]	Maximum output current				300		mA
V_{OUT}	Output voltage	V_{OUT} = 1.8V	V_{IN} = V_{OUT} + 3.8V, 100µA ≤ I_{OUT} ≤ 300mA, T_J = 25°C	–3.0		4.5	%
		V_{OUT} = 3.3V		–2.75		4.25	
		V_{OUT} = 5.0V		–3.75		4.25	
		V_{OUT} = 12V		–5.25		5.25	
		V_{OUT} = 1.8V	V_{IN} = V_{OUT} + 3.8V, 100µA ≤ I_{OUT} ≤ 300mA, –40°C ≤ T_J ≤ 125°C	–3.75		5.0	
		V_{OUT} = 3.3V		–3.5		5.0	
		V_{OUT} = 5.0V		–4.25		4.75	
		V_{OUT} = 12V		–5.75		5.75	
$\Delta V_{OUT}/V_{IN}$	Line regulation	I_{OUT} = 1mA, V_{OUT} + 1V ≤ V_{IN} ≤ 40V			0.00005	0.007	%/V
$\Delta V_{OUT}/I_{OUT}$	Load regulation	V_{IN} = V_{OUT} + 2V, 100µA ≤ I_{OUT} ≤ 150mA			0.1		%/A
$\Delta V_{OUT}/I_{OUT}$	Load regulation	V_{IN} = V_{OUT} + 3.8V, 100µA ≤ I_{OUT} ≤ 300mA			0.3		%/A
V_{DO}	Dropout voltage	I_{OUT} = 50mA			440	700	mV
V_{DO}	Dropout voltage	I_{OUT} = 150mA			1100	1800	mV
V_{DO}	Dropout voltage	I_{OUT} = 300mA			2175	3700	mV
I_{LIM}	Output current limit	V_{OUT} = 0.90*$V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 9V		320	530	740	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0V, V_{IN} = $V_{OUT(nom)}$ + 6V		75	175	290	mA
I_{GND}	GND pin current	V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 0mA, T_J = 25°C			1.7	2.65	µA
		V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 0mA, T_J = –40°C to 85°C				2.9	
		V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 0mA, T_J = –40°C to 125°C				3	
		V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 100µA			2.8		
I_{GND}	GND pin current	V_{IN} = $V_{OUT(nom)}$ + 3.8V, I_{OUT} = 300 mA			250		µA
PSRR	Power-supply ripple rejection	V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 50mA, C_{OUT} = 0.47µF , f = 10kHz			55		dB
		V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 50mA, C_{OUT} = 0.47µF , f = 100kHz			43		

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5.5 Electrical Characteristics (continued)

over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted); typical values are at T_J = 25°C (1)

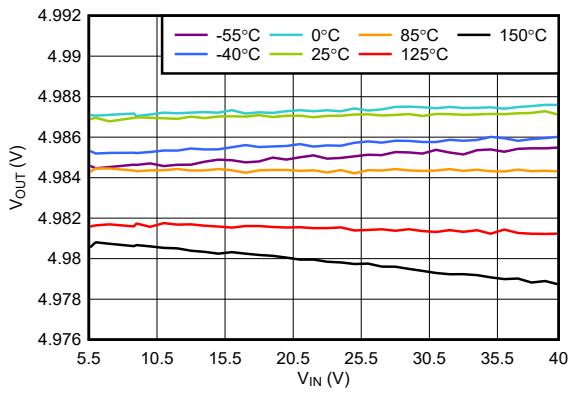
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_n	Output noise voltage	Bandwidth = 10Hz to 100kHz, V_{IN} = $V_{OUT(nom)}$ + 3.8V, I_{OUT} = 300mA, C_{OUT} = 1µF	Bandwidth = 10Hz to 100kHz, V_{IN} = $V_{OUT(nom)}$ + 3.8V, I_{OUT} = 300mA, C_{OUT} = 1µF		525		μV_{RMS}
T_{sd+}	Thermal shutdown temperature increasing	Shutdown, temperature increasing			160		°C
T_{sd-}	Thermal shutdown temperature decreasing	Reset, temperature decreasing			140		°C
t_{sup} (4)	Start-up time				400		µs

(1) Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; take thermal effects into account separately.
(2) Higher power dissipation across the voltage regulator leads to activation of thermal shutdown circuit, preventing attainment of maximum output current.
(3) Maximum supported power dissipation ratings are listed in *Absolute Maximum Rating* table. Exceeding these ratings leads to permanent SOA damage to the voltage regulator.
(4) Start-up time is measured as difference between t = 0 when V_{IN} is ramped at slew rate more than 1V/µs and the time when V_{OUT} reaches 95% of $V_{OUT(nom)}$ value.

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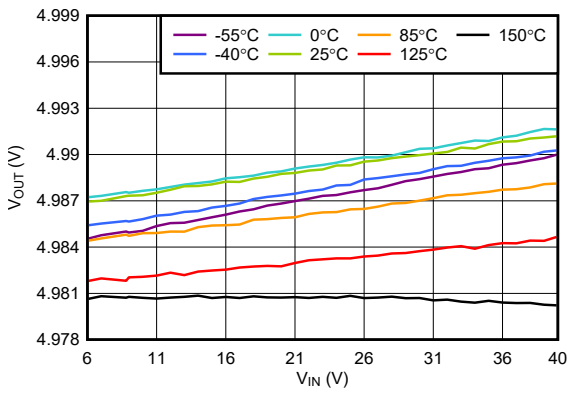
5.6 Typical Characteristics

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



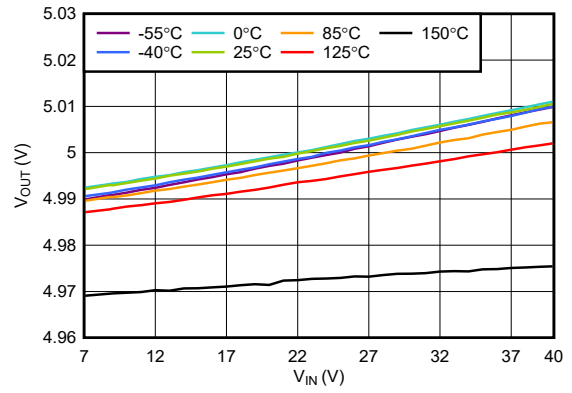
V_{OUT} = 5.0V, I_{OUT} = 10mA

Figure 5-1. V_{OUT} vs V_{IN}



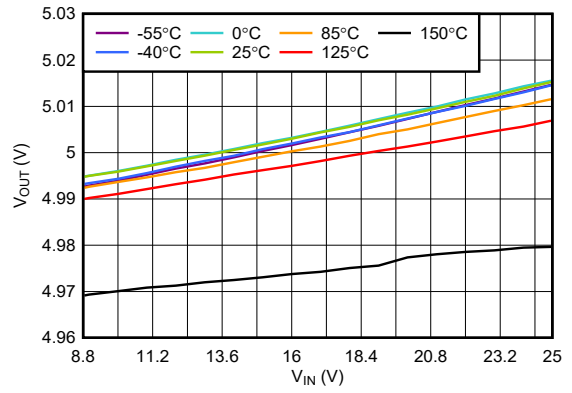
V_{OUT} = 5.0V, I_{OUT} = 50mA

Figure 5-2. V_{OUT} vs V_{IN}



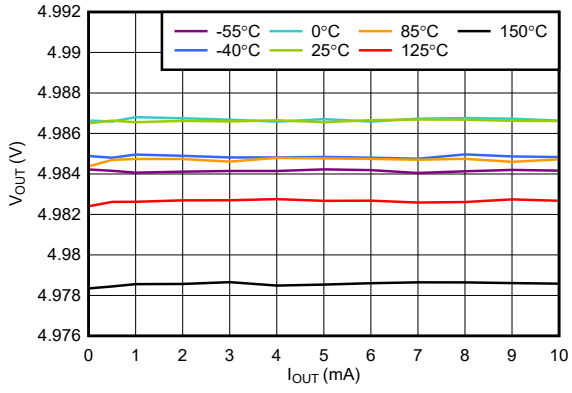
V_{OUT} = 5.0V, I_{OUT} = 150mA

Figure 5-3. V_{OUT} vs V_{IN}



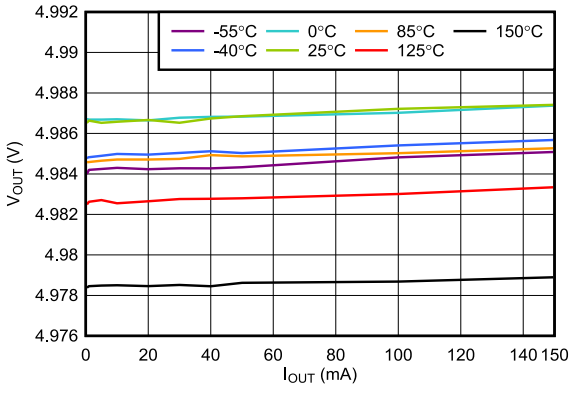
V_{OUT} = 5.0V, I_{OUT} = 300mA

Figure 5-4. V_{OUT} vs V_{IN}



V_{IN} = 5.5V, V_{OUT} = 5.0V

Figure 5-5. V_{OUT} vs I_{OUT}



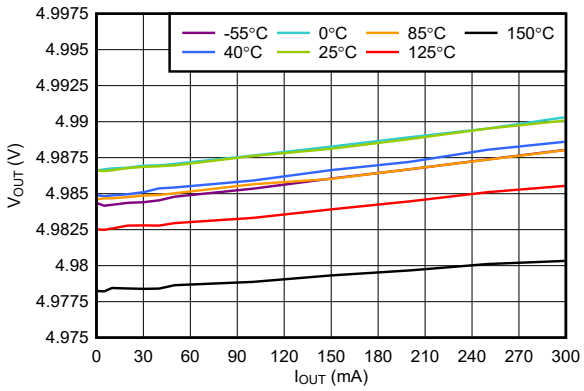
V_{IN} = 7.0V, V_{OUT} = 5.0V

Figure 5-6. V_{OUT} vs I_{OUT}

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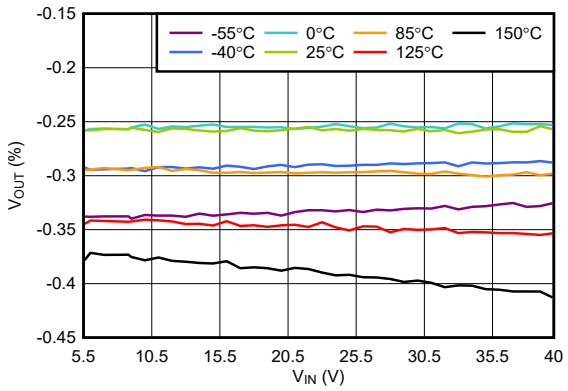
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



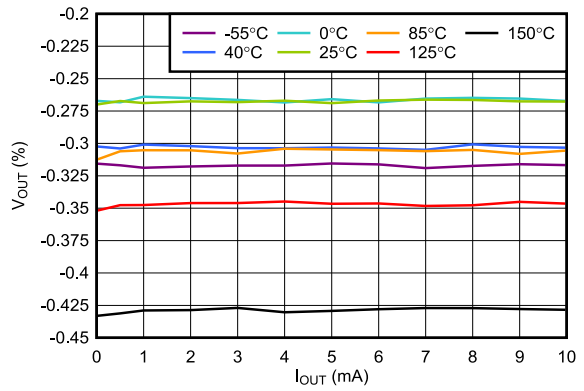
V_{IN} = 8.8V, V_{OUT} = 5.0V

Figure 5-7. V_{OUT} vs I_{OUT}



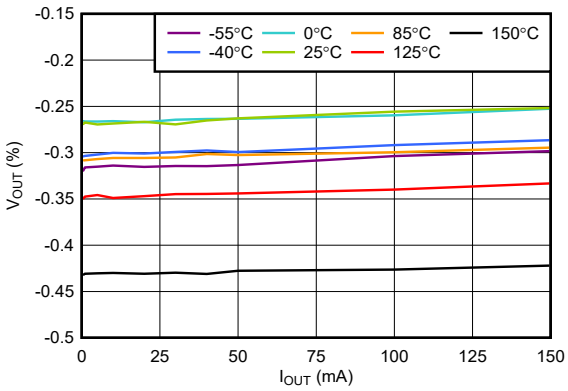
V_{OUT} = 5.0V, I_{OUT} = 1.0mA

Figure 5-8. V_{OUT} Accuracy vs V_{IN}



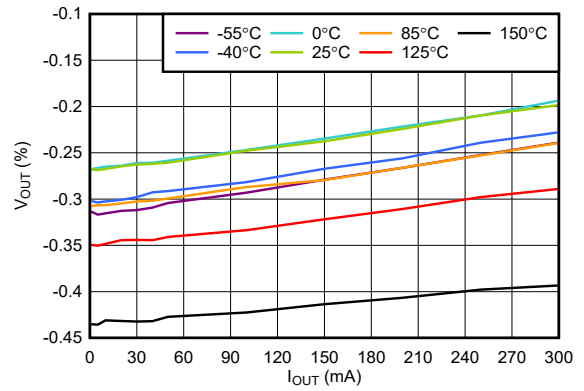
V_{IN} = 5.5V, V_{OUT} = 5.0V

Figure 5-9. V_{OUT} Accuracy vs I_{OUT}



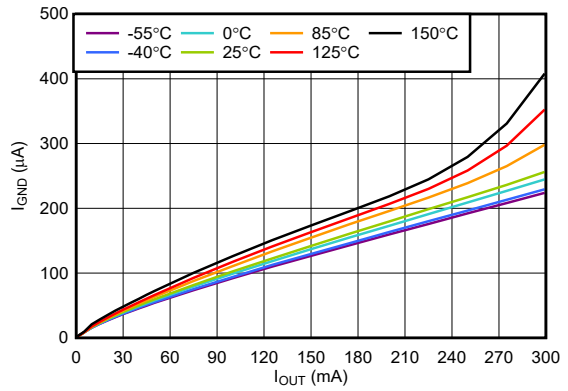
V_{IN} = 7.0V, V_{OUT} = 5.0V

Figure 5-10. V_{OUT} Accuracy vs I_{OUT}



V_{IN} = 8.8V, V_{OUT} = 5.0V

Figure 5-11. V_{OUT} Accuracy vs I_{OUT}



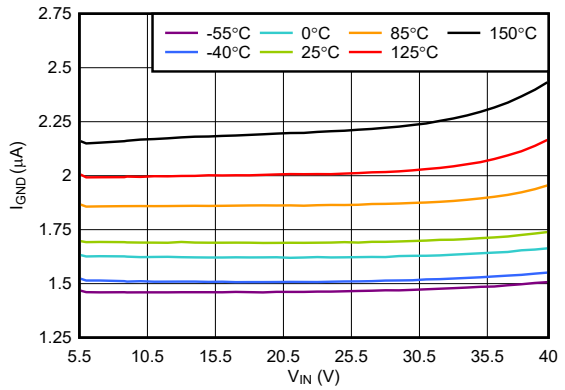
V_{IN} = 8.8V, V_{OUT} = 5.0V

Figure 5-12. I_{GND} vs I_{OUT}

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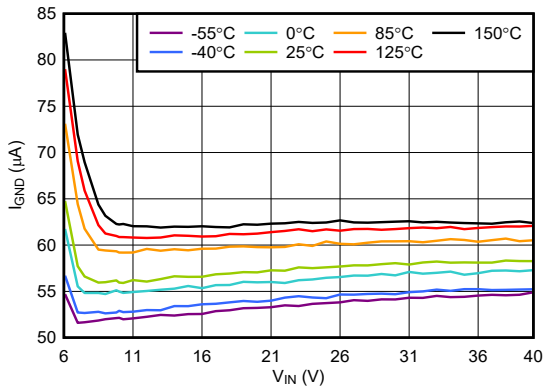
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



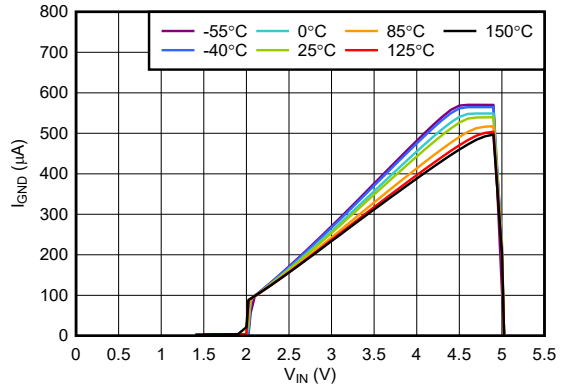
V_{OUT} = 5.0V, I_{OUT} = 0mA

Figure 5-13. I_{GND} vs V_{IN}



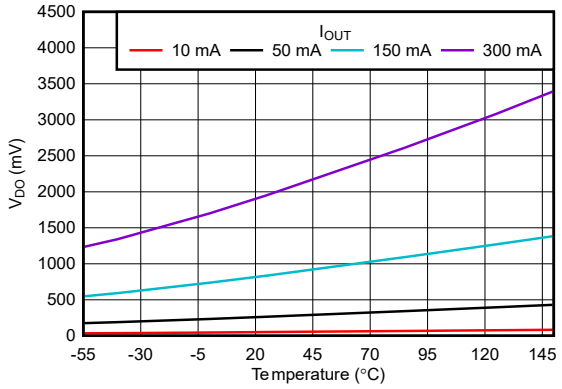
V_{OUT} = 5.0V, I_{OUT} = 50mA

Figure 5-14. I_{GND} vs V_{IN}



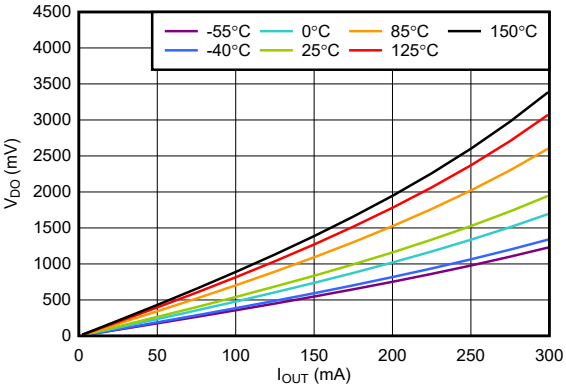
V_{OUT} = 5.0V, I_{OUT} = 0mA

Figure 5-15. I_{GND} vs V_{IN} (Dropout Operation)



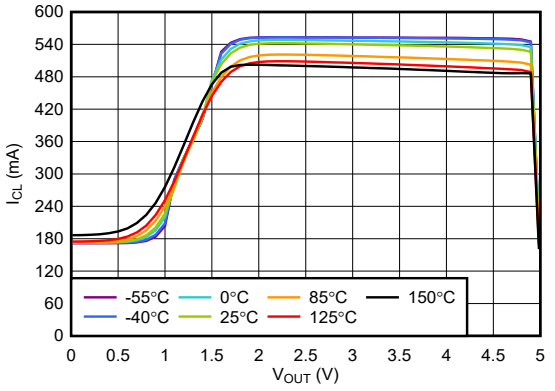
V_{OUT} = 5.0V

Figure 5-16. Dropout vs Temperature



V_{OUT} = 5.0V

Figure 5-17. Dropout vs I_{OUT}



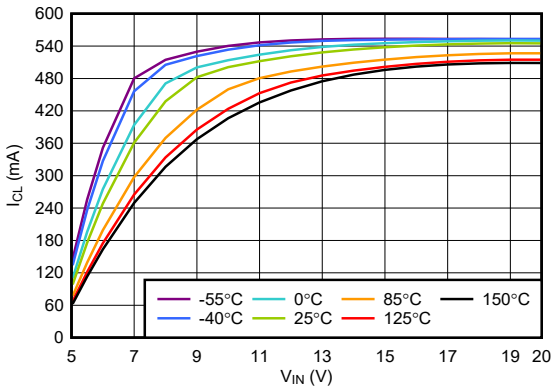
V_{IN} = 14V

Figure 5-18. Current Limit vs V_{OUT}

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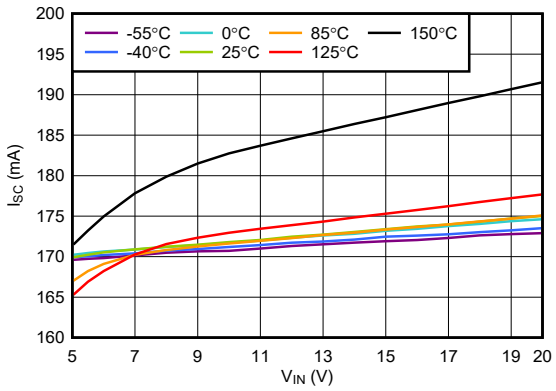
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



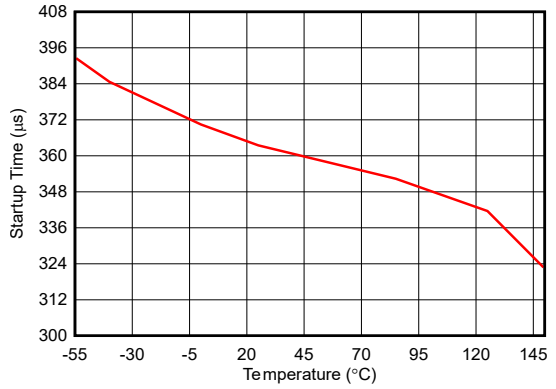
V_{OUT} = 5.0V

Figure 5-19. Current Limit vs V_{IN}



V_{OUT} = 5.0V

Figure 5-20. Short-Current Limit vs V_{IN}



V_{IN} = 5.5V, V_{OUT} = 5.0V

Figure 5-21. Start-Up Time vs Temperature

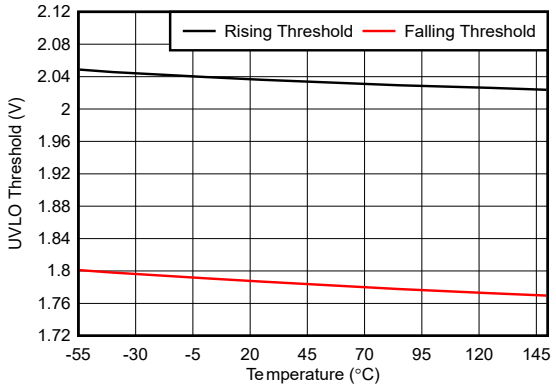
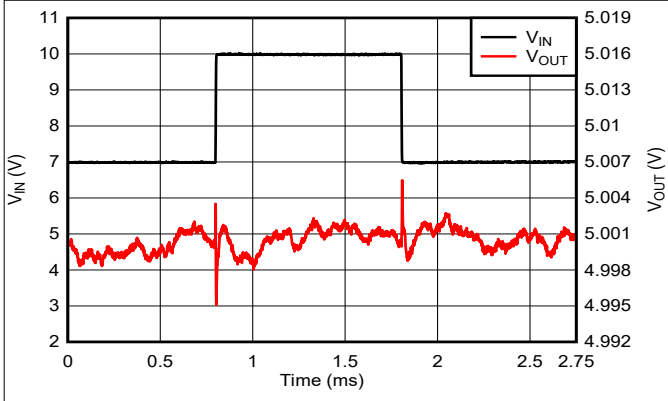
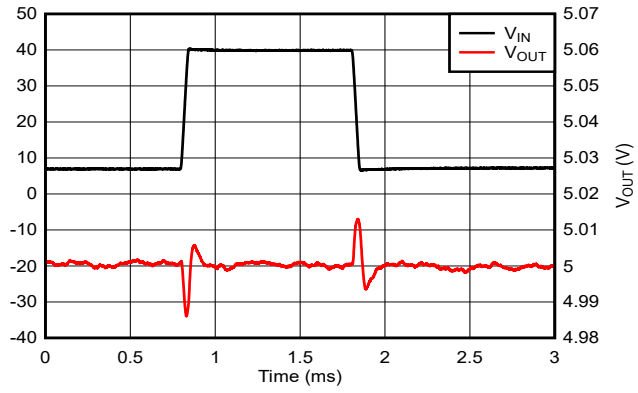


Figure 5-22. UVLO Thresholds vs Temperature



V_{OUT} = 5.0V, I_{OUT} = 150mA, dV_{IN}/dt = 1V/µs

Figure 5-23. V_{IN} Line Transient (7V to 10V)



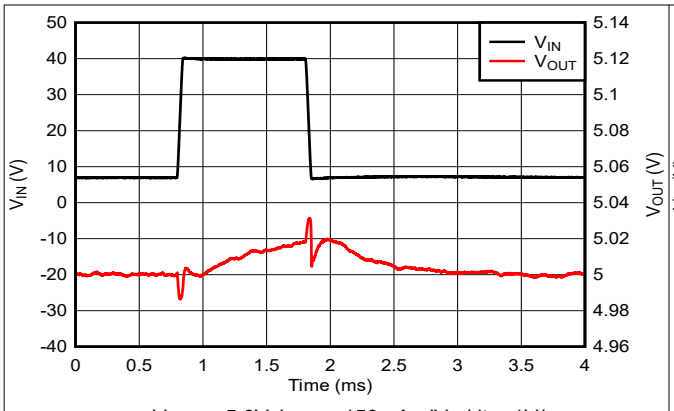
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 5-24. V_{IN} Line Transient (7V to 40V)

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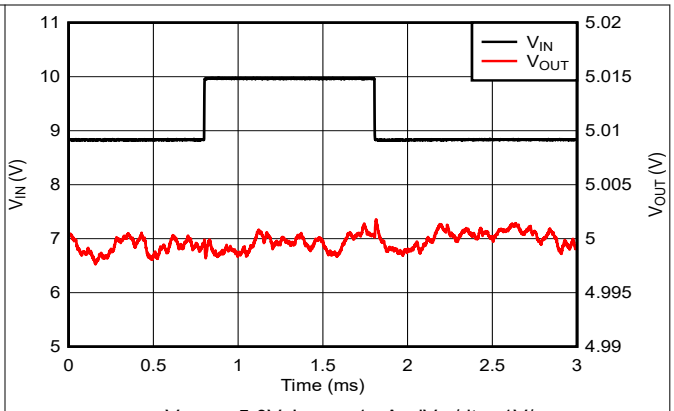
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



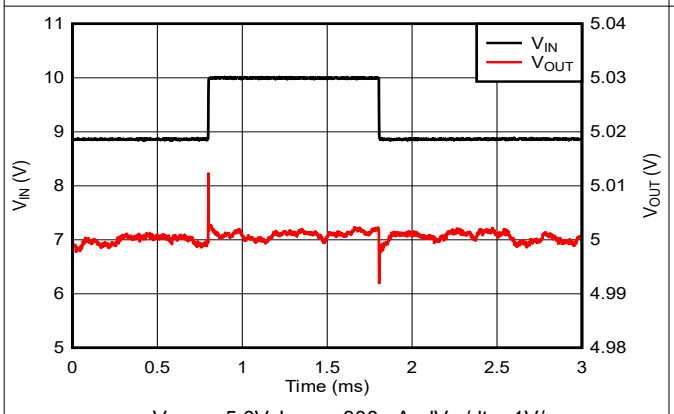
V_{OUT} = 5.0V, I_{OUT} = 150mA, dV_{IN}/dt = 1V/µs

Figure 5-25. V_{IN} Line Transient (7V to 40V)



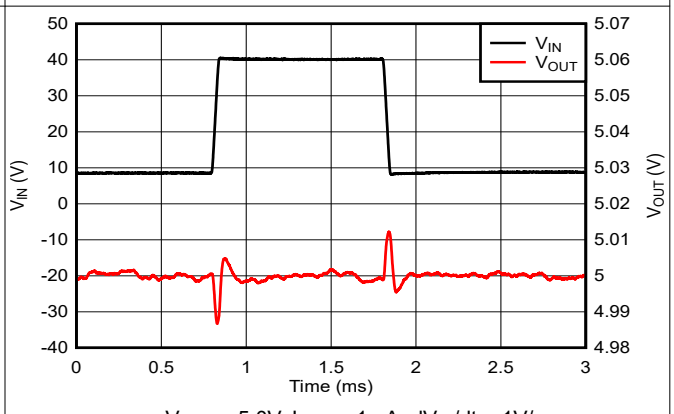
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 5-26. V_{IN} Line Transient (8.8V to 10V)



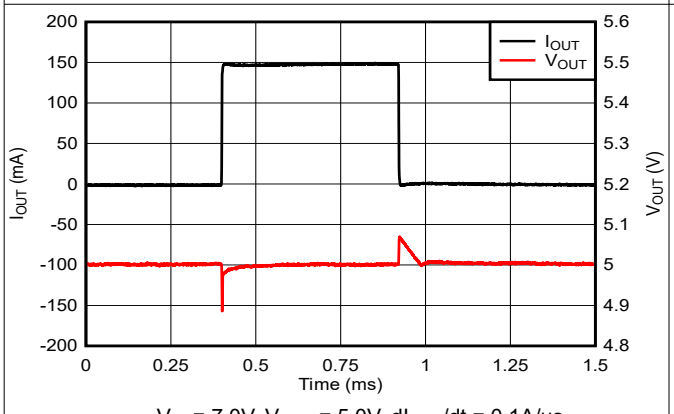
V_{OUT} = 5.0V, I_{OUT} = 300mA, dV_{IN}/dt = 1V/µs

Figure 5-27. V_{IN} Line Transient (8.8V to 10V)



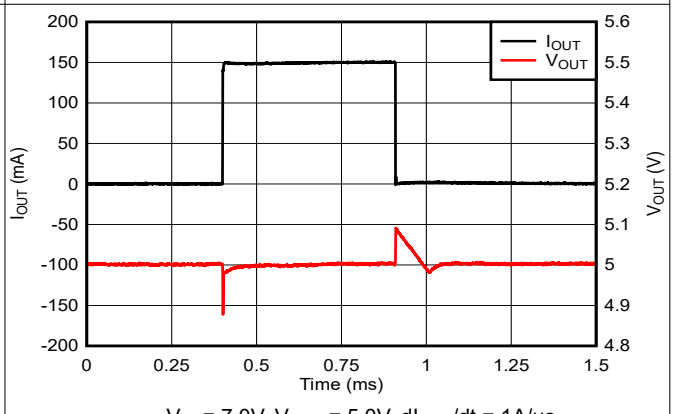
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 5-28. V_{IN} Line Transient (8.8V to 40V)



V_{IN} = 7.0V, V_{OUT} = 5.0V, dI_{OUT}/dt = 0.1A/µs

Figure 5-29. Load Transient (1mA to 150mA)



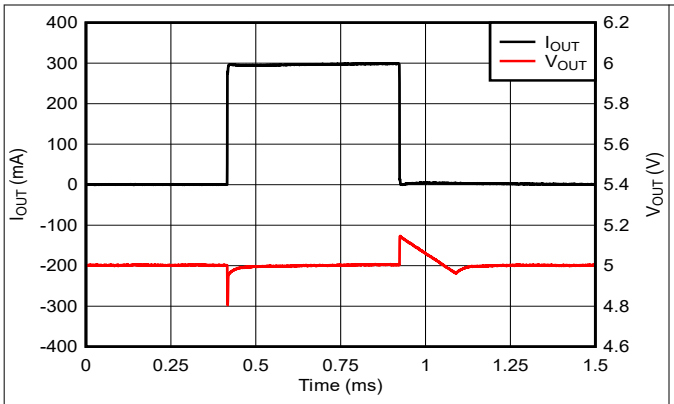
V_{IN} = 7.0V, V_{OUT} = 5.0V, dI_{OUT}/dt = 1A/µs

Figure 5-30. Load Transient (1mA to 150mA)

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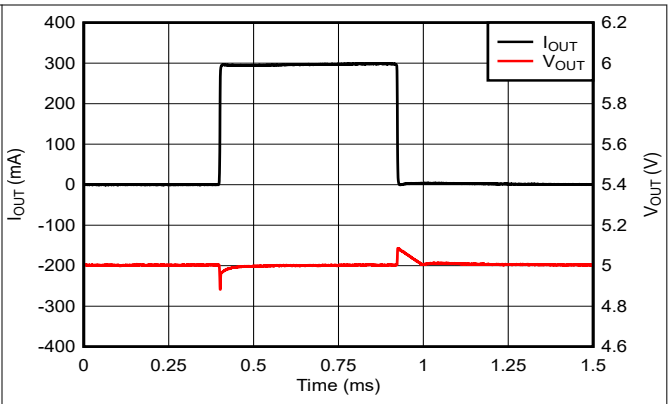
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



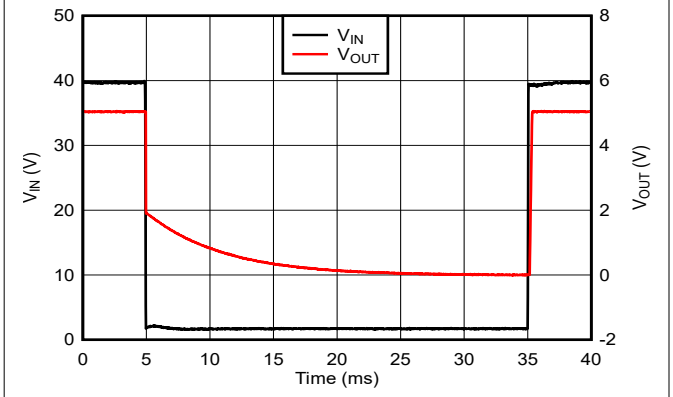
V_{IN} = 8.8V, V_{OUT} = 5.0V, dI_{OUT}/dt = 1A/µs

Figure 5-31. Load Transient (1mA to 300mA)



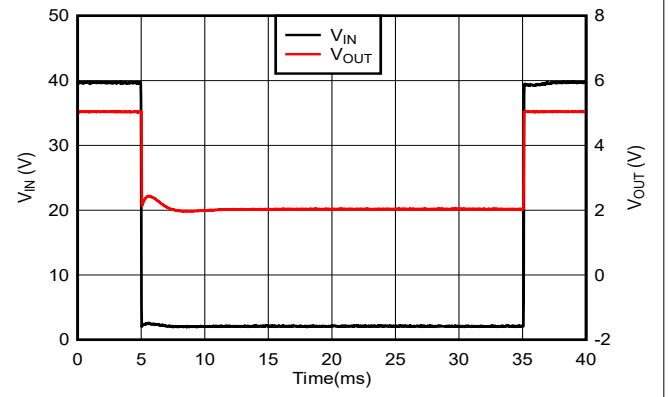
V_{IN} = 8.8V, V_{OUT} = 5.0V, dI_{OUT}/dt = 0.1A/µs

Figure 5-32. Load Transient (1mA to 300mA)



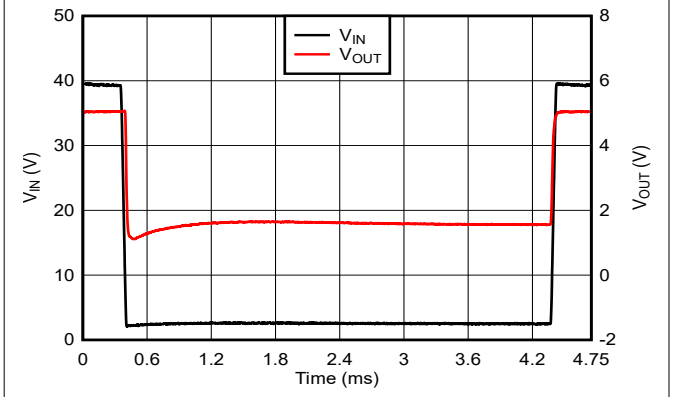
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 5-33. Brownout Transient (40V to 1.7V)



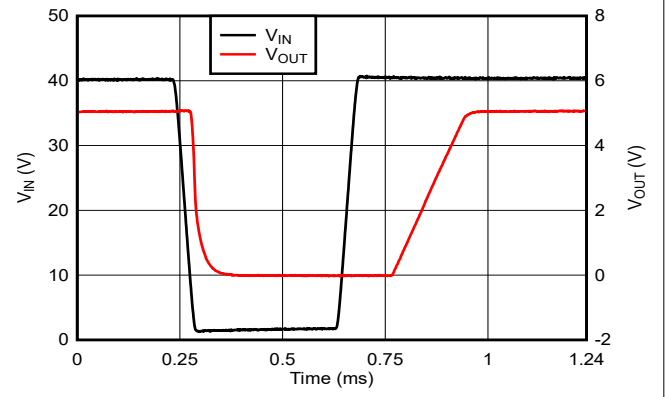
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 5-34. Brownout Transient (40V to 2.1V)



V_{OUT} = 5.0V, I_{OUT} = 300mA, dV_{IN}/dt = 1V/µs

Figure 5-35. Brownout Transient (40V to 2.5V)



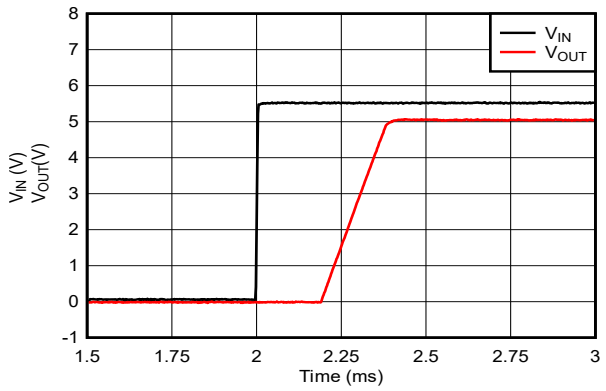
V_{OUT} = 5.0V, I_{OUT} = 300mA, dV_{IN}/dt = 1V/µs

Figure 5-36. Brownout Transient (40V to 1.7V)

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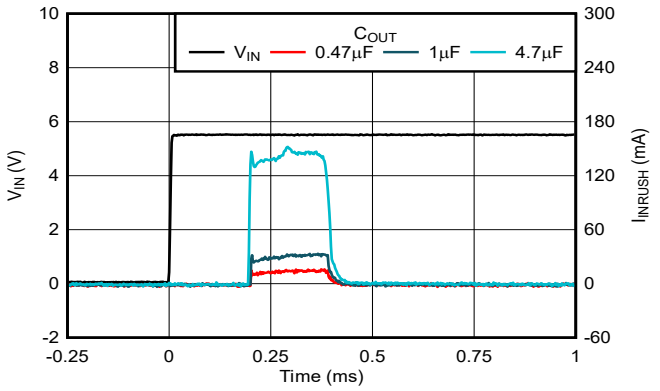
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



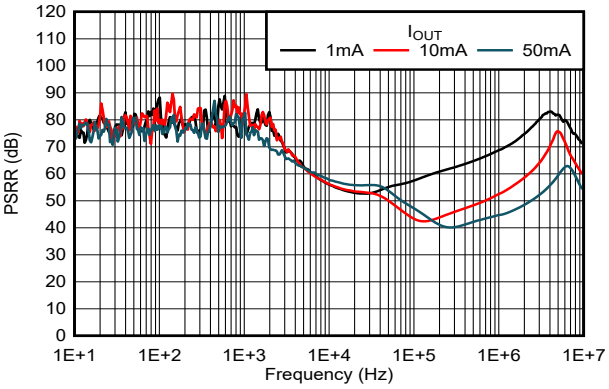
V_{IN} = 5.5V, V_{OUT} = 5.0V, R_{OUT} = 5kΩ

Figure 5-37. Start-Up



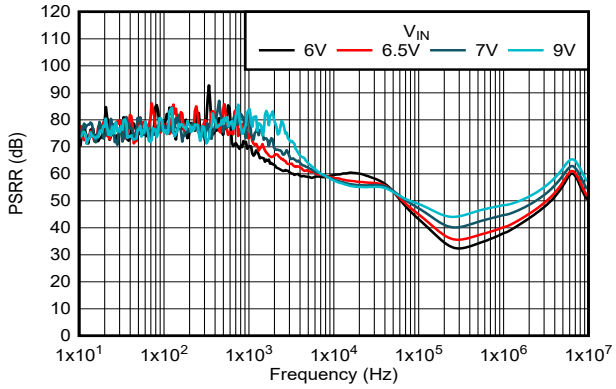
V_{IN} = 5.5V, V_{OUT} = 5.0V

Figure 5-38. Inrush Current vs Output Capacitor



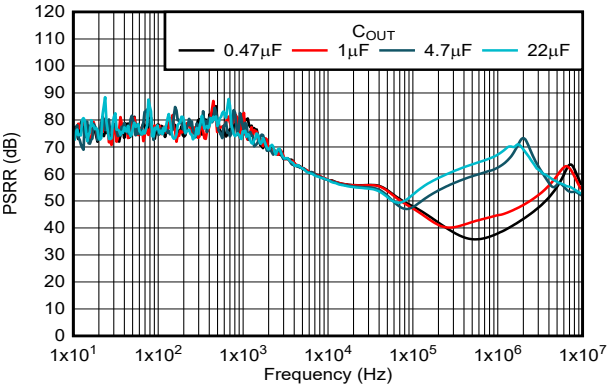
V_{OUT} = 5.0V, C_{OUT} = 1µF, V_{IN} = 7V

Figure 5-39. PSRR vs Load Current



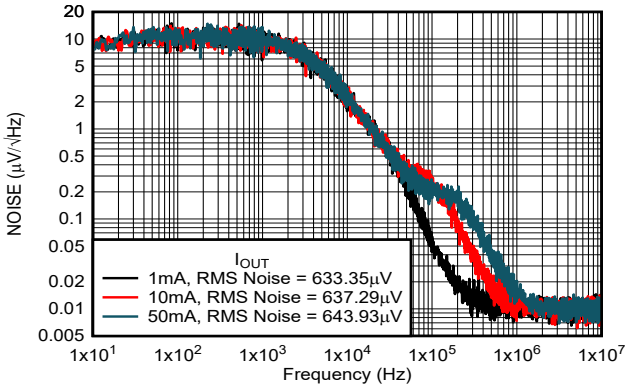
V_{OUT} = 5.0V, C_{OUT} = 1µF, I_{OUT} = 50mA

Figure 5-40. PSRR vs Input Supply



V_{IN} = 7.0V, V_{OUT} = 5.0V, I_{OUT} = 50mA

Figure 5-41. PSRR vs Output Capacitor



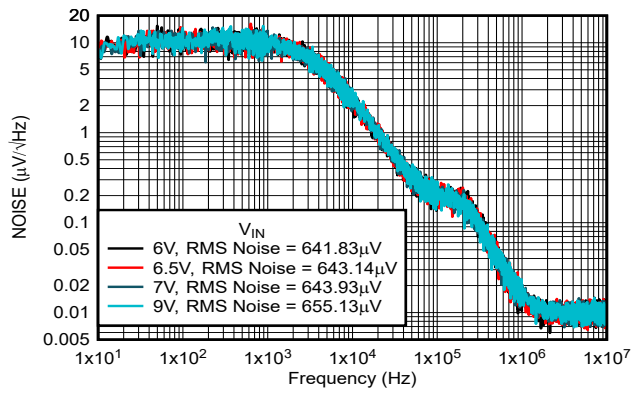
V_{IN} = 7.0V, V_{OUT} = 5.0V, C_{OUT} = 1µF

Figure 5-42. Noise vs Load Current

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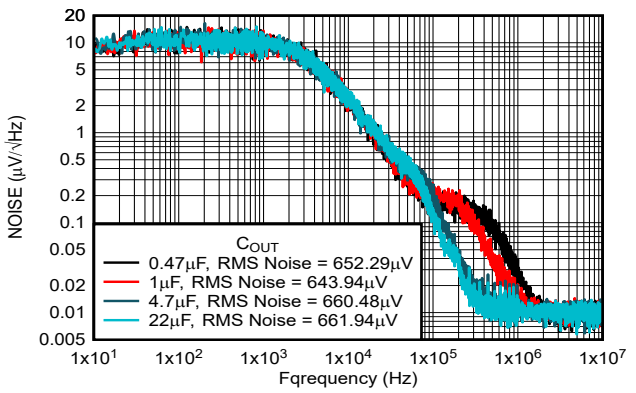
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 2.5V or V_{IN} = V_{OUT}(nom) + 0.5V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 1µF, and I_{OUT} = 1mA (unless otherwise noted)



V_{OUT} = 5.0V, I_{OUT} = 50mA, C_{OUT} = 1µF

Figure 5-43. Noise vs Input Supply



V_{IN} = 7.0V, V_{OUT} = 5.0V, I_{OUT} = 50mA

Figure 5-44. Noise vs Output Capacitor

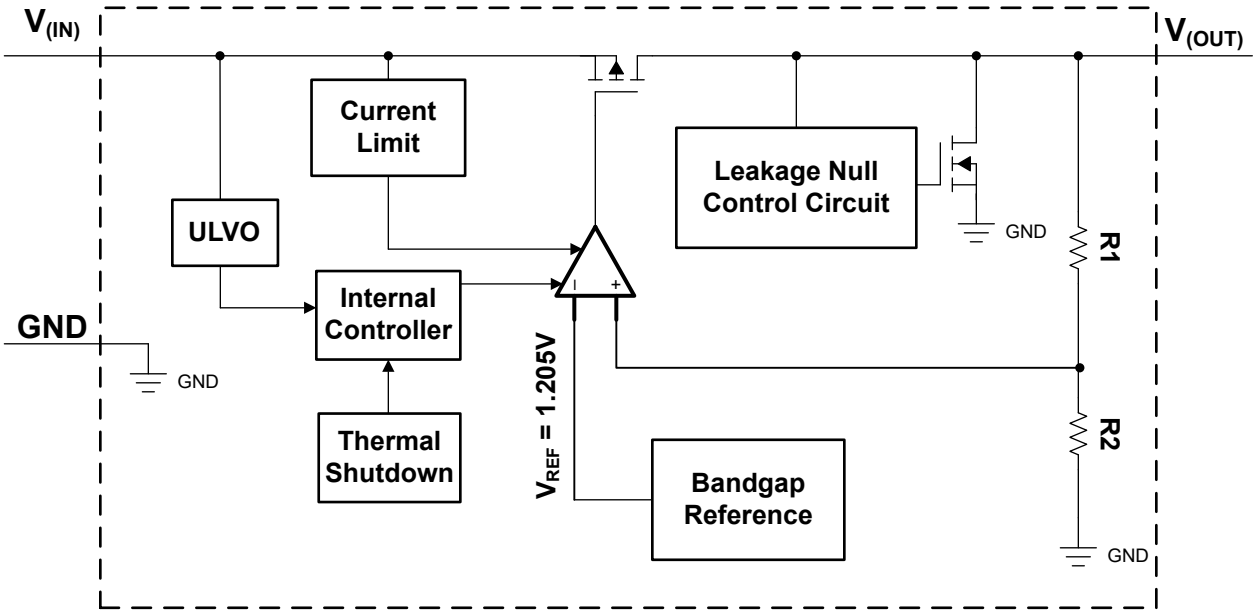
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6 Detailed Description

6.1 Overview

The TPS7B92 low-dropout regulator (LDO) consumes only 1.8µA (typ) of quiescent current at no-load current. The device offers a wide input voltage range (2.5V to 40V) and wide output range in small packaging. The wide output range is from 1.2V to 12V. The device is stable with the output capacitor range of 1µF to 47µF. The low quiescent current across the complete load current range makes the TPS7B92 designed for powering battery-operated applications. The TPS7B92 has an internal soft-start mechanism that provides a uniform start-up with controlled inrush current. This LDO also has foldback overcurrent and thermal protection during a load-short or fault condition on the output.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Wide Supply Range

This device has an operational input supply range of 2.5V to 40V, allowing for a wide range of applications. This wide supply range is designed for applications that have either large transients or high DC voltage supplies.

6.3.2 Low Quiescent Current

This device only requires 1.8µA (typical) of quiescent current at no load. The LDO consumes less than 0.1% of the full load current capacity (300mA) at room temperature. For load currents higher than 1mA, the TPS7B92 manages the I_Q consumption to be less than 0.5% of the load current to maintain high efficiency. In this manner, the device maintains good transient performance.

6.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. $V_{IN} – V_{OUT}$ is input voltage minus the output voltage. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

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For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Equation 1 calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 50% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

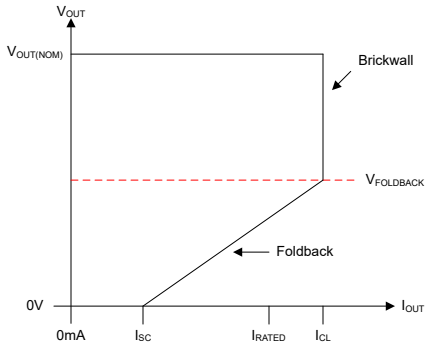


Figure 6-1. Foldback Current Limit

6.3.5 Leakage Null Control Circuit

This device has a built-in, leakage-null control circuit. At high temperatures, pass-transistor leakage increases and starts impacting the V_{OUT} accuracy at low-load conditions. This leakage becomes more aggravated with higher headroom across the LDO (V_{IN} – V_{OUT}). The TPS7B92 has a built-in, leakage-null control circuit that detects pass-transistor leakage and provides a ground discharge path for the leakage. This circuitry helps the TPS7B92 maintain much tighter V_{OUT} accuracy across wide V_{IN} and temperature (–40°C to +125°C) ranges.

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6.4 Device Functional Modes

Table 6-1 provides a quick comparison between the normal and dropout modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

6.4.2 Dropout Operation

The device operates in dropout mode when the input voltage is lower than the nominal output voltage plus the specified dropout voltage. However, make sure all other conditions are met for normal operation. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. Because of this operation, the transient performance of the device becomes significantly degraded. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven into the ohmic or triode region. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start up. During dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the input voltage returns to a value ≥ $V_{OUT(NOM)} + V_{DO}$, the output voltage overshoots for a short period of time. During this time, the device pulls the pass transistor back into the linear region. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS7B92 LDO regulator is a good choice for battery-powered applications. The device is a good supply for low-power microcontrollers, such as the MSP430, because of the device low I_Q performance across load current range. The ultra-low-supply current of the TPS7B92 maximizes efficiency at light loads. The device features flexibility in the output voltage selection. These features and the high input voltage range makes the device excellent as a supply in building automation and power tools.

7.2 Typical Application

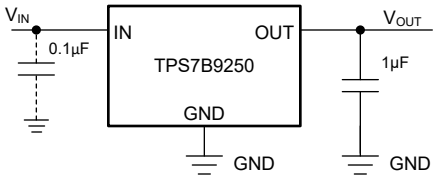


Figure 7-1. Typical Application Circuit

7.2.1 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-1.

Table 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	12V
Output voltage	5.0V
Output current	100mA

7.2.2 Detailed Design Procedure

7.2.2.1 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.2.2.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. A higher value capacitor is necessary if large, fast rise-time load or line transients are anticipated. A higher value capacitor is also required if the device is located several inches from the input power source.

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Dynamic performance of the device is improved by using a larger output capacitor. The TPS7B92 requires an output capacitor of 1µF or larger (0.47µF or larger capacitance) for stability. An equivalent series resistance (ESR) between 0.001Ω and 1Ω is also required. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.2.2.3 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Figure 7-2 shows one approach for protecting the device.

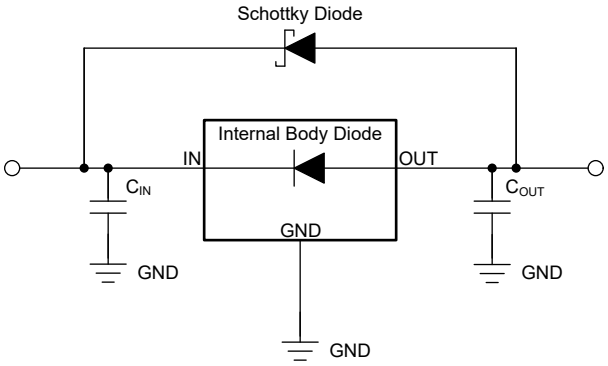


Figure 7-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, circuit location on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Note

Power dissipation is minimized, and therefore greater efficiency achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$). The $R_{\theta JA}$ component is the combined PCB, device package, and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

The maximum peak power dissipation supported for the TPS7B92 is defined in the *Absolute Maximum Ratings*. The power dissipation ratings are recorded for the PCB configurations and are based on a JEDEC standard of 2s2p configuration (EIA/JESD51-x). The maximum supported power provides reliable operation for the TPS7B92. Exceeding the power limits leads to extreme junction temperatures (related to junction-to-ambient thermal resistance $R_{\theta JA}$, Equation 3). Extreme temperatures risk damage to the device, and potentially reduces the expected device lifetime. Based on the safe operating limits, Figure 7-3 shows the supported load current (I_{OUT}) for a headroom ($V_{IN} - V_{OUT}$).

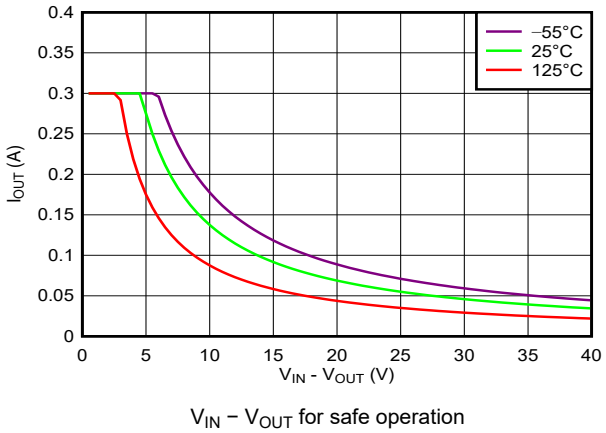


Figure 7-3. I_{OUT} vs Headroom ($V_{IN} - V_{OUT}$)

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance. $R_{\theta JA}$ is improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimized. See the *An empirical analysis of the impact of board layout on LDO thermal performance* application note.

7.2.2.5 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

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$$T_J = T_T + \psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (5)$$

where:

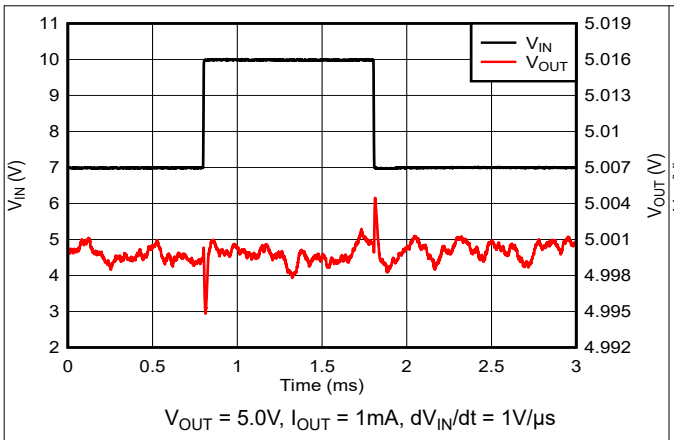
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see *Semiconductor and IC Package Thermal Metrics* application note.

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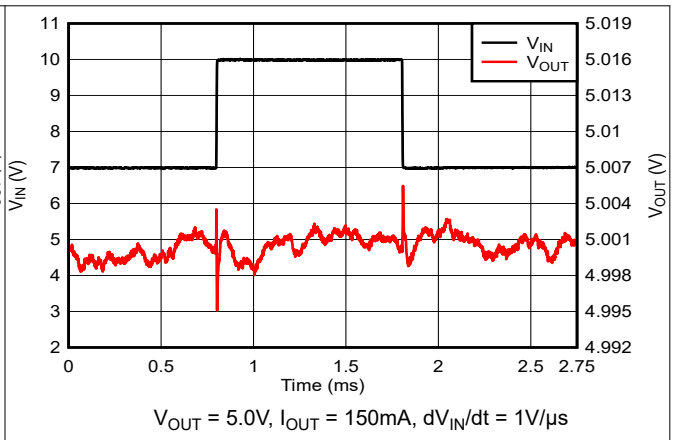
7.2.3 Application Curves

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2.5V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)



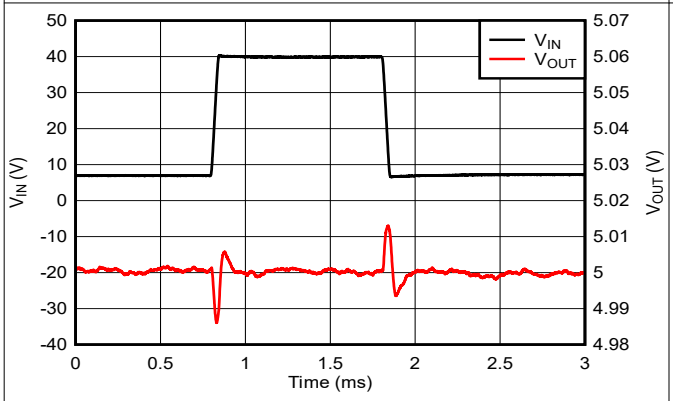
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 7-4. V_{IN} Line Transient (7V to 10V)



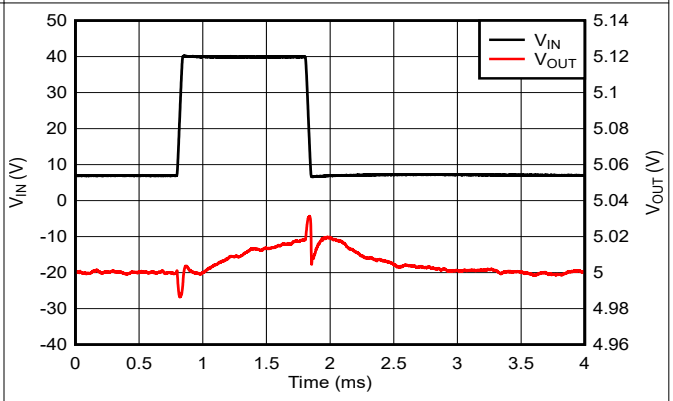
V_{OUT} = 5.0V, I_{OUT} = 150mA, dV_{IN}/dt = 1V/µs

Figure 7-5. V_{IN} Line Transient (7V to 10V)



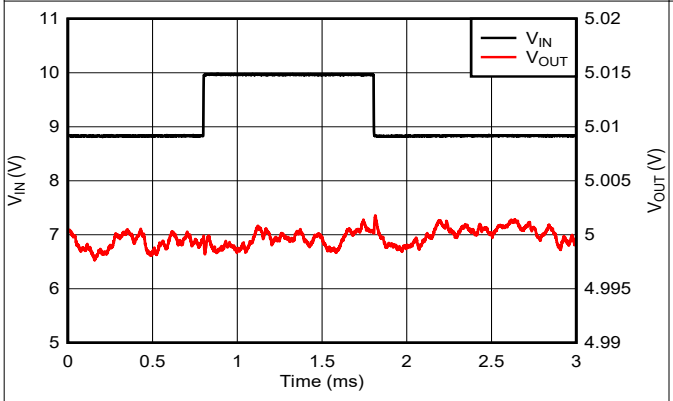
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 7-6. V_{IN} Line Transient (7V to 40V)



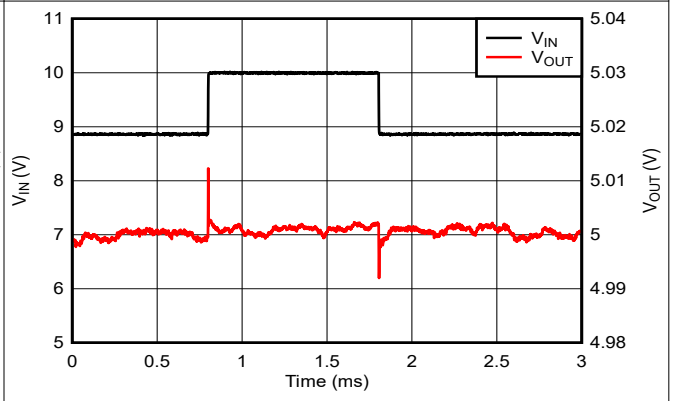
V_{OUT} = 5.0V, I_{OUT} = 150mA, dV_{IN}/dt = 1V/µs

Figure 7-7. V_{IN} Line Transient (7V to 40V)



V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 7-8. V_{IN} Line Transient (8.8V to 10V)



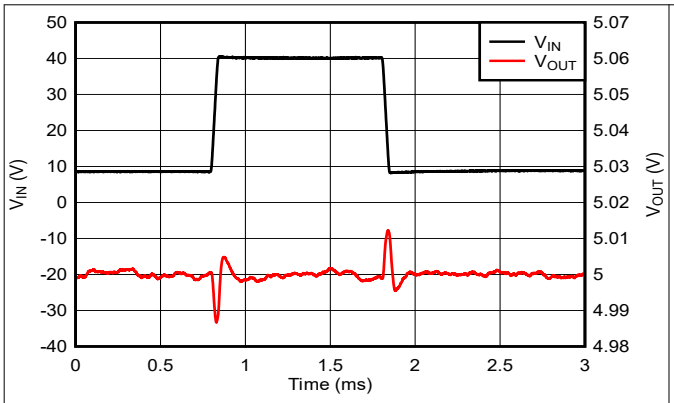
V_{OUT} = 5.0V, I_{OUT} = 300mA, dV_{IN}/dt = 1V/µs

Figure 7-9. V_{IN} Line Transient (8.8V to 10V)

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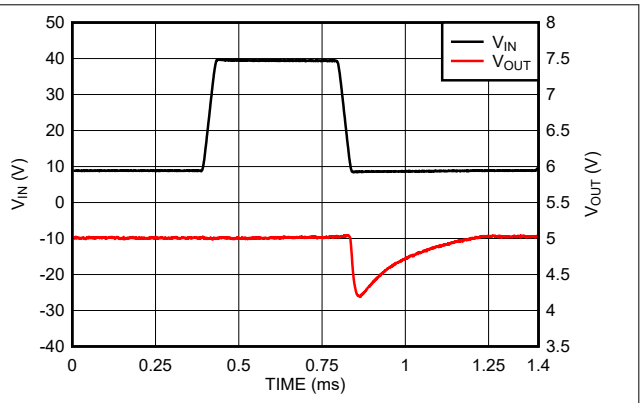
7.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2.5V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)



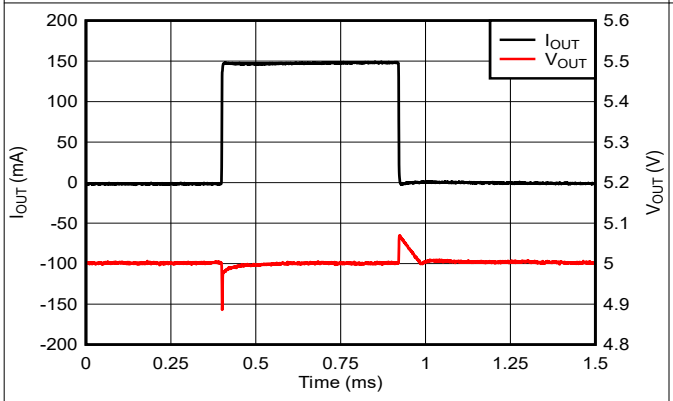
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 7-10. V_{IN} Line Transient (8.8V to 40V)



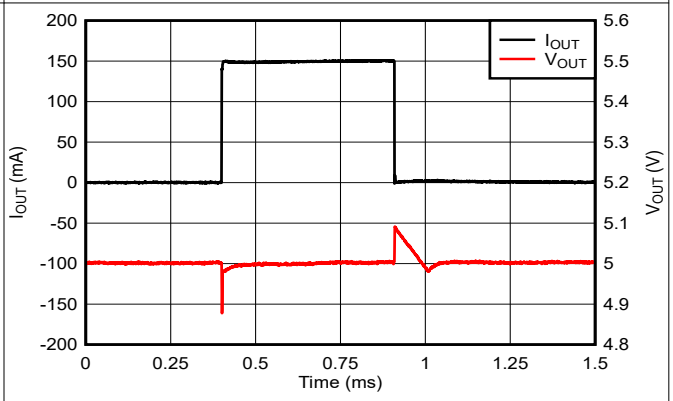
V_{OUT} = 5.0V, I_{OUT} = 300mA, dV_{IN}/dt = 1V/µs

Figure 7-11. V_{IN} Line Transient (8.8V to 40V)



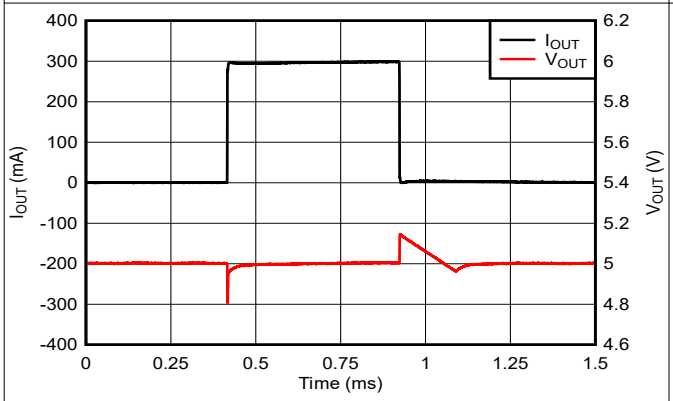
V_{IN} = 7.0V, V_{OUT} = 5.0V, dI_{OUT}/dt = 0.1A/µs

Figure 7-12. Load Transient (1mA to 150mA)



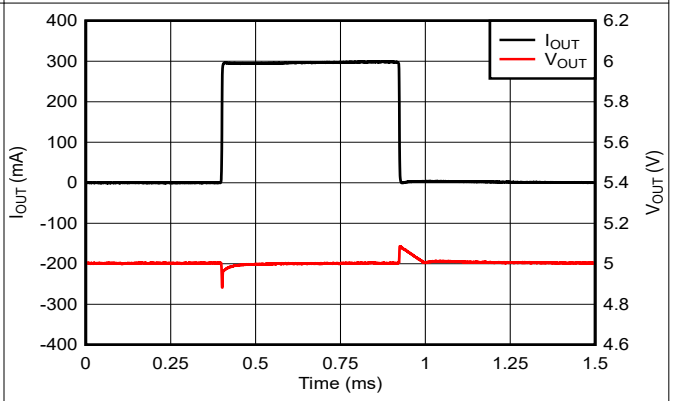
V_{IN} = 7.0V, V_{OUT} = 5.0V, dI_{OUT}/dt = 1A/µs

Figure 7-13. Load Transient (1mA to 150mA)



V_{IN} = 8.8V, V_{OUT} = 5.0V, dI_{OUT}/dt = 1A/µs

Figure 7-14. Load Transient (1mA to 300mA)



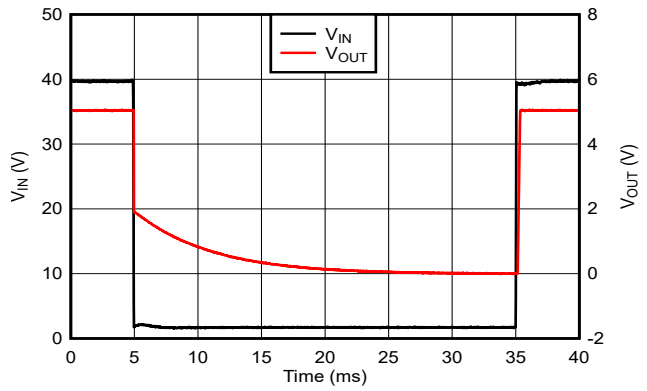
V_{IN} = 8.8V, V_{OUT} = 5.0V, dI_{OUT}/dt = 0.1A/µs

Figure 7-15. Load Transient (1mA to 300mA)

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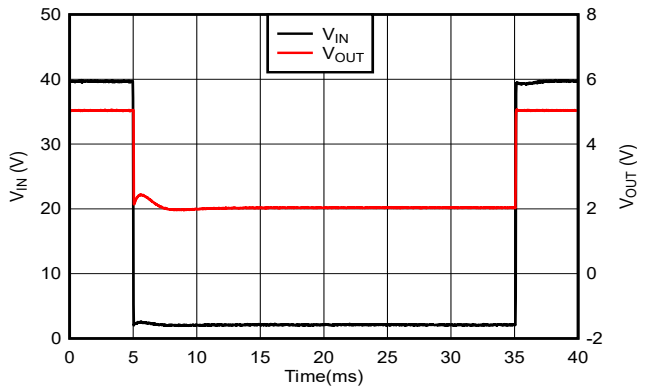
7.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2.5V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted)



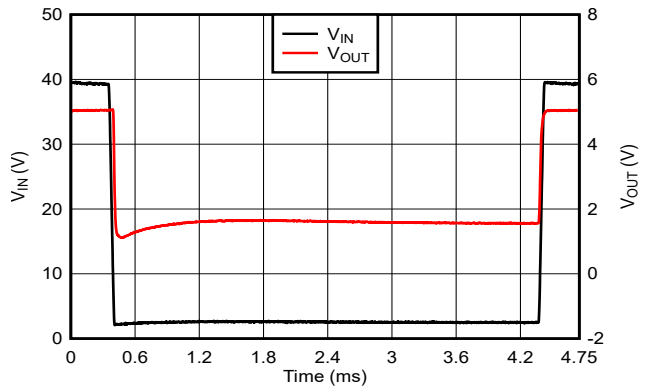
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 7-16. Brownout Transient (40V to 1.7V)



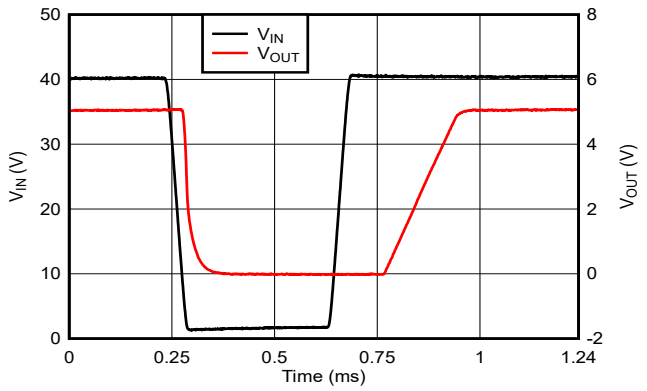
V_{OUT} = 5.0V, I_{OUT} = 1mA, dV_{IN}/dt = 1V/µs

Figure 7-17. Brownout Transient (40V to 2.1V)



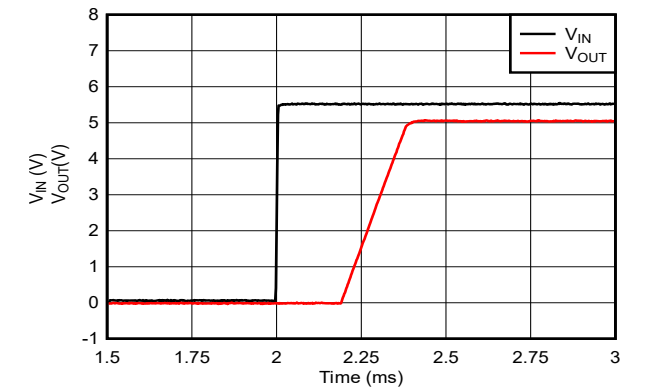
V_{OUT} = 5.0V, I_{OUT} = 300mA, dV_{IN}/dt = 1V/µs

Figure 7-18. Brownout Transient (40V to 2.5V)



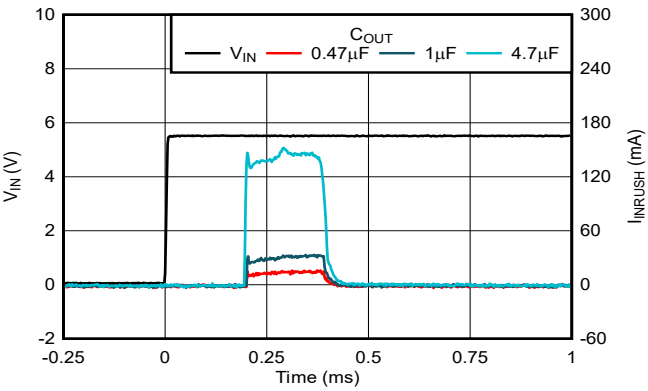
V_{OUT} = 5.0V, I_{OUT} = 300mA, dV_{IN}/dt = 1V/µs

Figure 7-19. Brownout Transient (40V to 1.7V)



V_{IN} = 5.5V, V_{OUT} = 5.0V, I_{OUT} = 1mA, R_{OUT} = 5kΩ

Figure 7-20. Start-Up



V_{IN} = 5.5V, V_{OUT} = 5.0V

Figure 7-21. Inrush Current vs Output Capacitor

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7.3 Best Design Practices

Place at least one 1.0µF capacitor as close as possible to the OUT and GND pins of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor as close as possible to the IN and GND pins of the regulator for best performance.

Do not exceed the absolute maximum ratings.

7.4 Power Supply Recommendations

The TPS7B92 is designed to operate from an input voltage supply range between 2.5V and 40V. The input voltage range provides adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

For best overall performance, follow the guidelines in this section. Place all circuit components on the same side of the printed circuit board (PCB) and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or resistor divider. This practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage and shield the LDO from noise.

7.5.1.1 Power Dissipation

To provide reliable operation, make sure worst-case junction temperature does not exceed 125°C. This restriction limits the power dissipation the regulator handles in any given application. To make sure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation ($P_{D(max)}$). Also calculate the actual dissipation (P_D) to be less than or equal to $P_{D(max)}$.

Equation 6 determines the maximum-power-dissipation limit:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \tag{6}$$

where:

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

Equation 7 calculates the regulator dissipation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{7}$$

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7.5.2 Layout Example

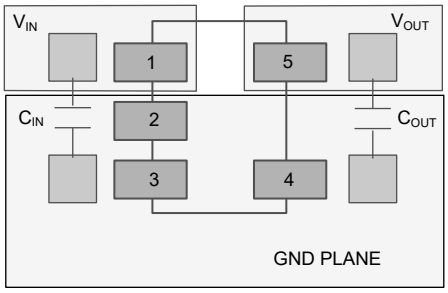


Figure 7-22. Example Layout

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7B92. The Universal EVM (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7B92 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS7B92 **xx**DBV**z**	In the SOT-23 (DBV) package: **XX** is the nominal output voltage (for example, 33 = 3.3V, 50 = 5.0V). **Z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Universal Low-Dropout Linear Voltage Regulator (LDO) Evaluation Module* user guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2024) to Revision A (May 2025)	Page
• Deleted adjustable (ADJ) functionality from document	1
• Changed *Available output voltage options* to *Output voltage range* in *Features*	1
• Deleted reference to adjustable configuration and outputs in *Description* section	1
• Deleted adjustable DBV package information from *Pin Configuration and Functions*	3
• Deleted adjustable configuration curves from *Typical Characteristics*	7
• Changed *Overview* section	15
• Deleted adjustable version block diagram	15
• Deleted output voltage flexibility for the adjustable configuration discussion from *Application Information*	18
• Deleted *Adjustable LDO Regulator Programming* figure and *Adjustable Output Voltage for Resistors R_1 and R_2* from *Typical Application* section	18
• Deleted *Setting V_{OUT} for the TPS7B9201 Adjustable LDO* section	18
• Deleted *Feed-Forward Capacitor (C_{FF})* section	19
• Changed *Example Layout* figure	26
• Deleted adjustable information from *Device Nomenclature*	27

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B92018DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37EH
TPS7B92018DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37EH
TPS7B92033DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37FH
TPS7B92033DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37FH
TPS7B92050DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37GH
TPS7B92050DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37GH
TPS7B92120DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37HH
TPS7B92120DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37HH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

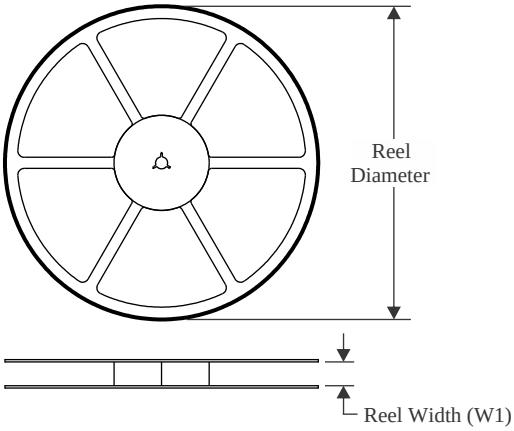
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

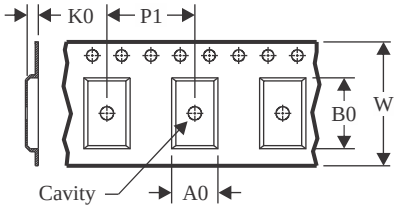
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

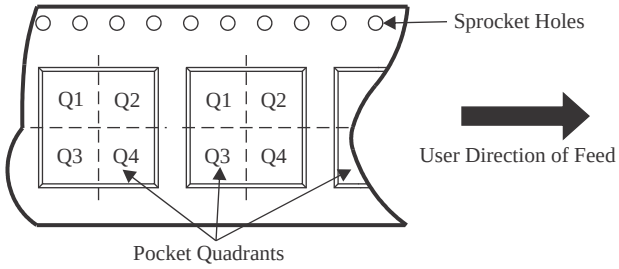


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

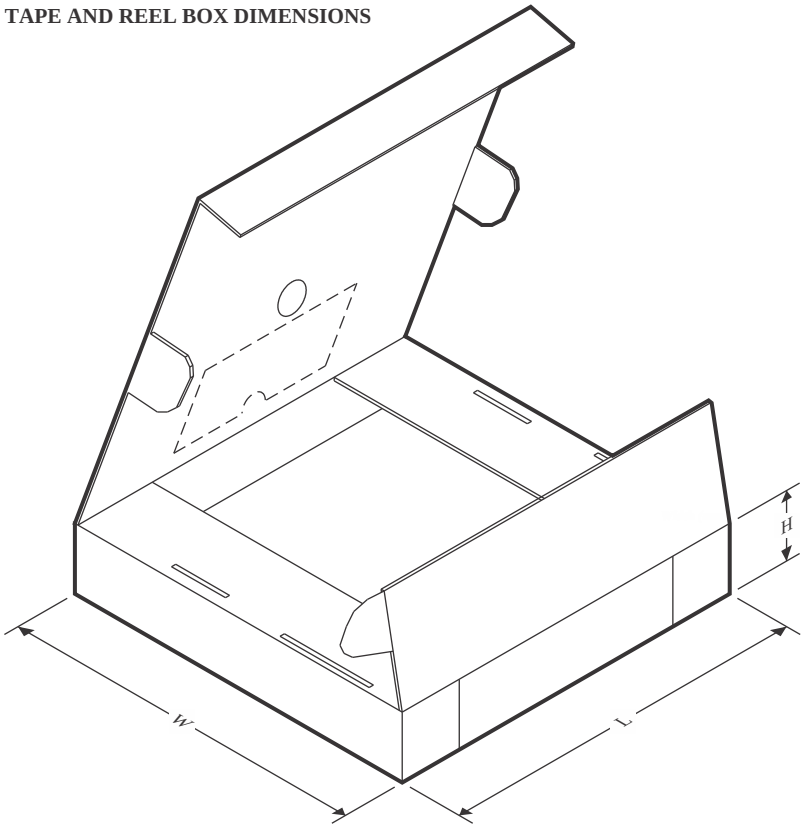
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B92018DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7B92033DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7B92050DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7B92120DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

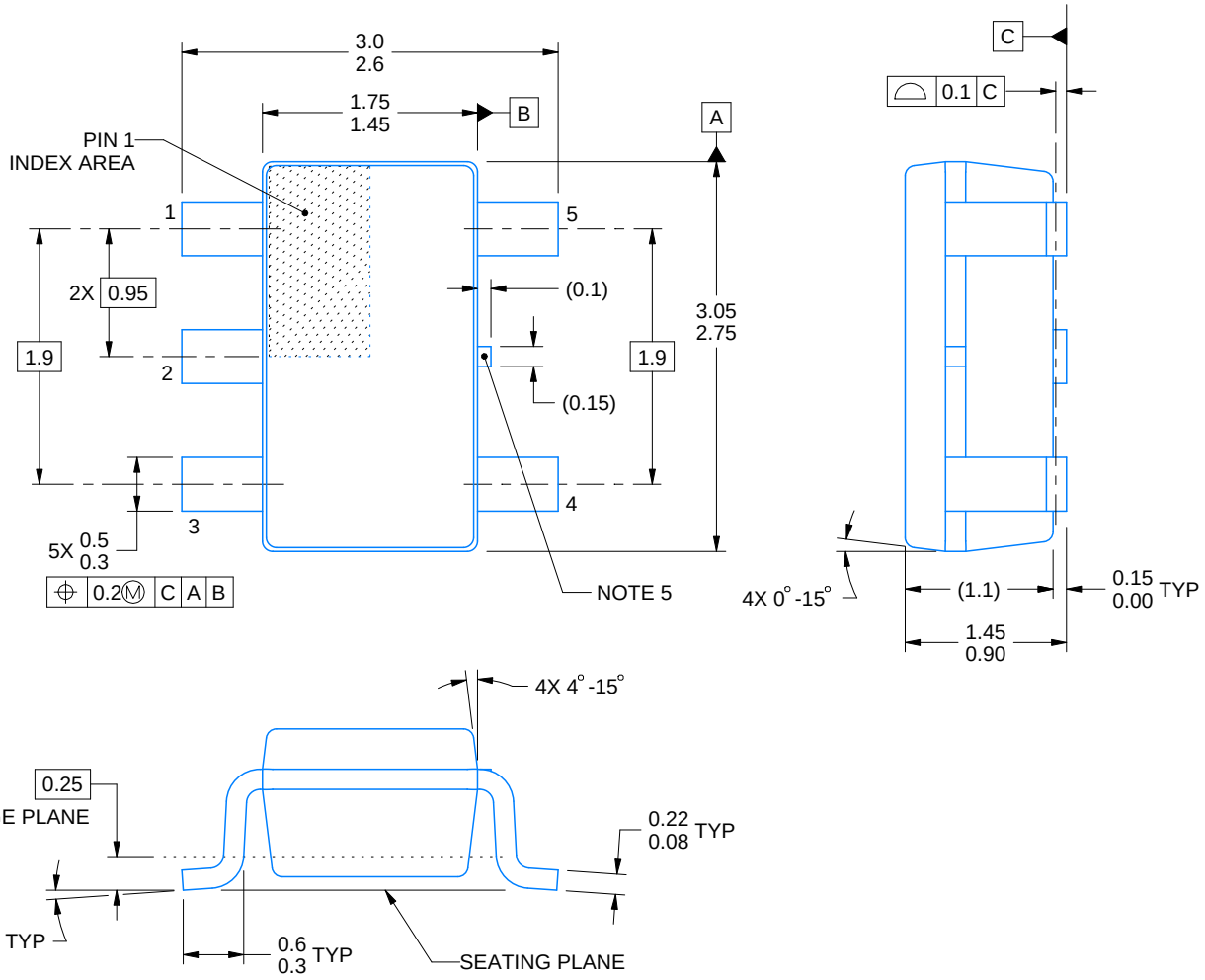
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B92018DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7B92033DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7B92050DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7B92120DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

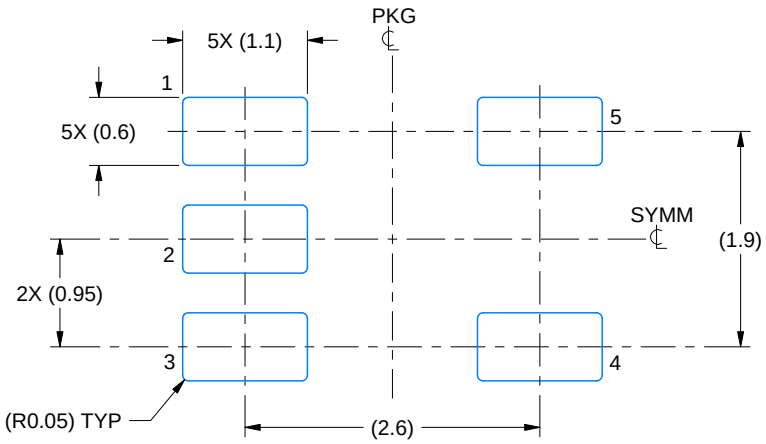
SMALL OUTLINE TRANSISTOR



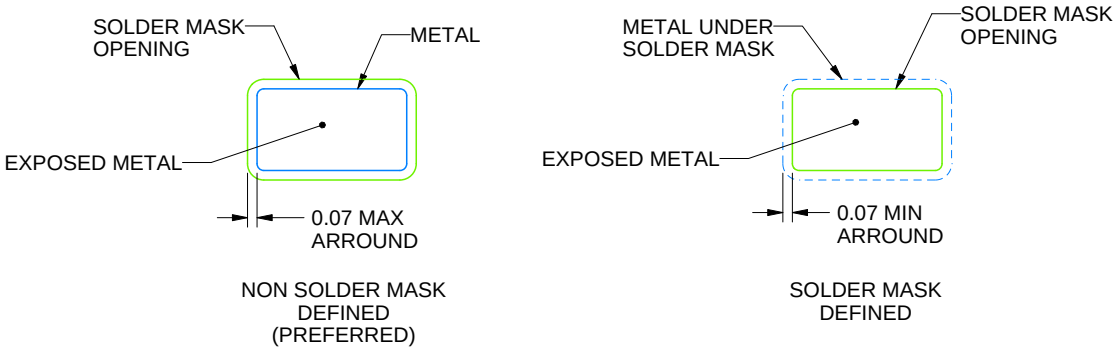
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

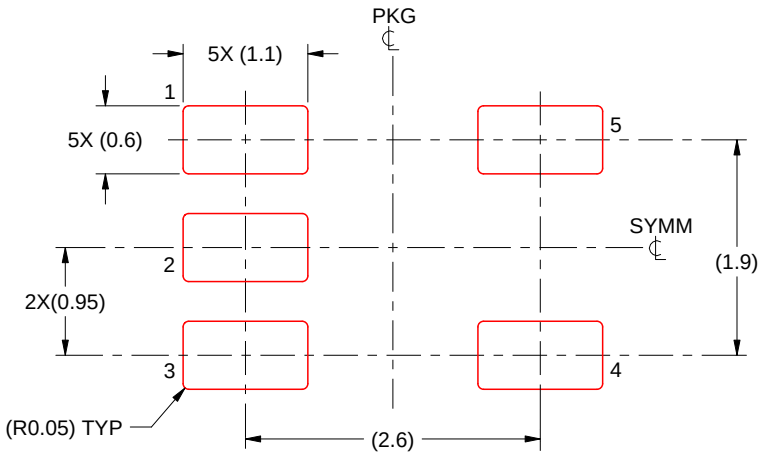


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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