TPS7A74 1.5-A, Low-Dropout Linear Regulator With Programmable Soft-Start

1 Features

- V_{OUT} range: 0.65 V to 3.6 V
- Ultra-low V_{IN} range: 0.65 V to 6 V
- V_{BIAS} range: 1.7 V to 6 V
- Low dropout: 150 mV typical at 1.5 A, V_{BIAS} = 5 V
- Noise: 7.1 μV_{RMS}
- PSRR:
  - 70 dB at 1 kHz
  - 60 dB at 10 kHz
  - 55 dB at 100 kHz
  - 50 dB at 1 MHz
- 1.5% accuracy over line, load, and temperature
- Programmable soft-start provides linear voltage start-up
- V_{BIAS} permits low V_{IN} operation with good transient response
- UVLO on both IN and BIAS
- Stable with any output capacitor ≥ 10 µF
- Package: Small, 3-mm × 3-mm × 0.8-mm WSON-8

2 Applications

- High-performance computing
- Microservers
- Desktop and PC motherboards
- Data concentrators
- Rugged PC laptops

3 Description

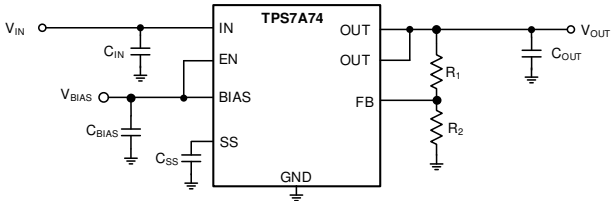
The TPS7A74 low-dropout (LDO) linear regulator provides an easy-to-use robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start up. The soft-start is monotonic and well-suited for powering many different types of processors and application-specific integrated circuits (ASICs). The enable input allows for easy sequencing with external regulators. This complete flexibility allows a solution to be configured that meets the sequencing requirements of field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and other applications with special start-up requirements.

A precision reference and error amplifier deliver 1.5% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 10 µF, and is fully specified for T_J = –40°C to +125°C. The TPS7A74 is offered in a small, 3-mm × 3-mm, WSON-8 package, yielding a highly compact, total solution size.

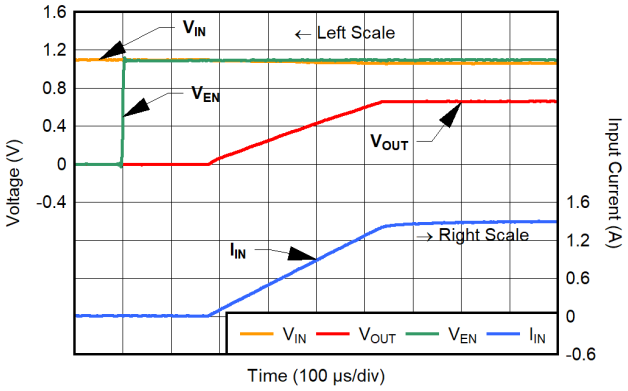
Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A74	WSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit (Adjustable)



Loaded Start-Up

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....3
6 Specifications....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....5
6.4 Thermal Information....5
6.5 Electrical Characteristics....5
6.6 Typical Characteristics....7
7 Detailed Description....17
7.1 Overview....17
7.2 Functional Block Diagram....17
7.3 Feature Description....18
7.4 Device Functional Modes....21
7.5 Programming....22
8 Application and Implementation....24
8.1 Application Information....24
8.2 Typical Application....28
8.3 Power Supply Recommendations....29
8.4 Layout....30
9 Device and Documentation Support....32
9.1 Device Support....32
9.2 Documentation Support....32
9.3 Receiving Notification of Documentation Updates....32
9.4 Support Resources....32
9.5 Trademarks....32
9.6 Electrostatic Discharge Caution....32
9.7 Glossary....32
10 Mechanical, Packaging, and Orderable Information....33

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2022) to Revision B (August 2022)	Page
• Changed Minimum startup time parameters limit values	5

Changes from Revision * (May 2022) to Revision A (July 2022)	Page
• Changed document status from *advance information* to *production data*	1

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5 Pin Configuration and Functions

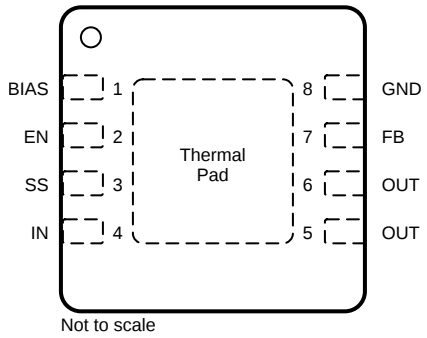


Figure 5-1. DSD Package, 8-Pin WSON With Thermal Pad (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	BIAS	I	Bias input voltage for error amplifier, reference, and internal control circuits. Use a 0.1 µF or larger input capacitor for optimal performance. If IN is connected to BIAS, a 4.7 µF or larger capacitor must be used.
2	EN	I	Enable pin.
3	SS	I	Soft-start pin. This pin must be connected to a capacitor to GND.
4	IN	I	Input to the device. Use a 1 µF or larger input capacitor for optimal performance.
5, 6	OUT	O	Regulated output voltage. A small capacitor (total typical capacitance of ≥ 10 µF, ceramic) is required from this pin to ground to assure stability.
7	FB	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
8	GND	—	Ground.
—	Thermal Pad	—	Ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	6.5	V
Bias voltage	BIAS	–0.3	6.5	V
Enable voltage	EN	–0.3	6.5	V
Soft-start voltage	SS	–0.3	6.5	V
Feedback voltage	FB	–0.3	2	V
Output voltage	OUT	–0.3	V_{IN} + 0.3	V
Maximum output current	I_{LIMIT}	Internally limited		
Output short-circuit duration	I_{SC}	Indefinite		
Continuous total power dissipation	P_{DISS}	See Thermal Information		
Junction Temperature	T_J	–40	150	°C
Storage Temperature	T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	0.65		V_{BIAS} – 0.1	V
V_{BIAS} (1)	BIAS supply voltage	1.7		6	V
V_{EN}	Enable voltage			6	V
V_{OUT}	Output voltage	0.65		3.6	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor	10			µF
C_{IN}	Input capacitor(2)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A74		UNIT
		DSD (WSON) (2)	DSD (WSON) (3)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.3	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.3	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.3	18.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) JEDEC standard. (2s2p, no vias to internal planes and bottom layer).
(3) TPS7A74 thermal characteristics on EVM.

6.5 Electrical Characteristics

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 10 nF, I_{OUT} = 10 mA, V_{BIAS} = 5.0 V (3), and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (adj.)		0.641	0.65	0.659	V
	Output accuracy (1) (4) (5)	2.97 V ≤ V_{BIAS} ≤ 6 V, 0 mA ≤ I_{OUT} ≤ 1.5 A	–1.5	±0.5	1.5	%
	Line regulation (V_{BIAS})	Max(2.7 V, V_{OUT} + 1.6 V) ≤ V_{BIAS} ≤ 6 V		0.2	0.32	%/V
	Line regulation (V_{IN})	$V_{OUT(nom)}$ + 0.15 V ≤ V_{IN} ≤ 6 V		0.01	0.05	%/V
	Load regulation	0 mA ≤ I_{OUT} ≤ 1.5 A		0.33		%/A
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 2.8 V		150	180	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS}		1.1	1.3	V
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	2	2.7	3.3	A
I_{BIAS}	BIAS pin current	I_{OUT} = 10 mA		0.25	0.33	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V, V_{IN} = 6 V, V_{BIAS} = 6 V		1	55	µA
I_{FB}	Feedback pin current		–1	0.15	1	µA
$V_{BIAS(UVLO)}$	Bias rail UVLO rising threshold		1.04	1.4	1.65	V
$V_{BIAS(UVLO),HYST}$	Bias rail UVLO hysteresis		0.02	0.06	0.07	V

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6.5 Electrical Characteristics (continued)

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 10 nF, I_{OUT} = 10 mA, V_{BIAS} = 5.0 V (3), and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

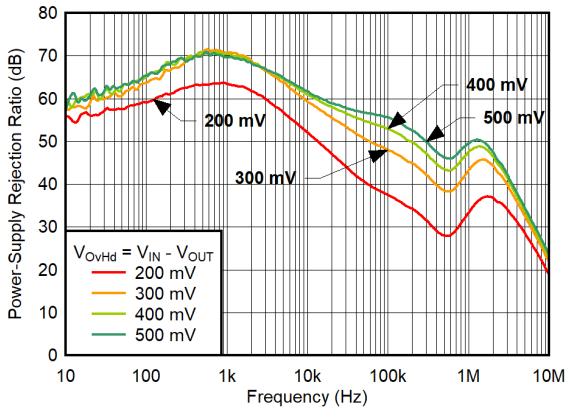
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(UVLO),\ rising}$	In rail UVLO rising threshold		0.39	0.455	0.5	V
$V_{IN(UVLO),\ falling}$	In rail UVLO falling threshold		0.21	0.26	0.3	V
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open	35		335	µs
I_{SS}	Soft-start charging current	V_{SS} = 0 V	8	17	31	µA
V_{SS}	Soft-start pin disable voltage	V_{EN} = 0 V		0	50	mV
PSRR	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, Iout = 1.5 A, Vin = 1.8 V, Vout = 1.5 V		57		dB
		300 kHz, Iout = 1.5 A, Vin = 1.8 V, Vout = 1.5 V		27		
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	BW = 10 Hz to 1 MHz, I_{OUT} = 1 A, V_{IN} = 2.05 V, V_{OUT} = 1.8 V		27		dB
Vn	Output voltage noise	BW = 10 Hz to 100 kHz, I_{OUT} = 1 A, V_{IN} = 0.95 V, V_{OUT} = 0.65 V		7.1		μV_{RMS}
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			55		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	0.2	µA
$R_{PULLDOWN(OUT)}$	V_{BIAS} = 5 V, V_{EN} = 0 V			0.6	1	kΩ
$R_{PULLDOWN(FB)}$	V_{BIAS} = 5 V, V_{EN} = 0 V			120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.65 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) V_{BIAS} = $V_{DO_MAX(BIAS)}$ + V_{OUT} for V_{OUT} ≥ 3.4 V
(4) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65 V and I_{OUT} = 1.5 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.
(5) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65 V and I_{OUT} = 1.5 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

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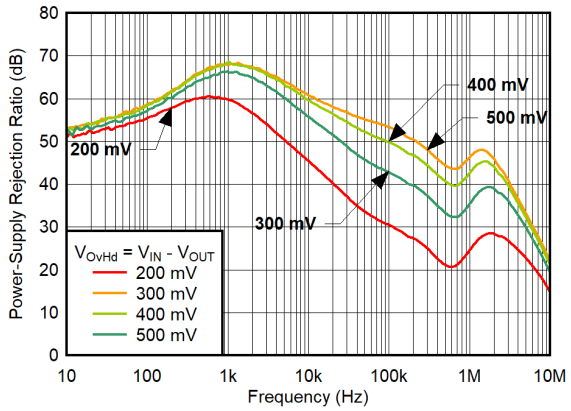
6.6 Typical Characteristics

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



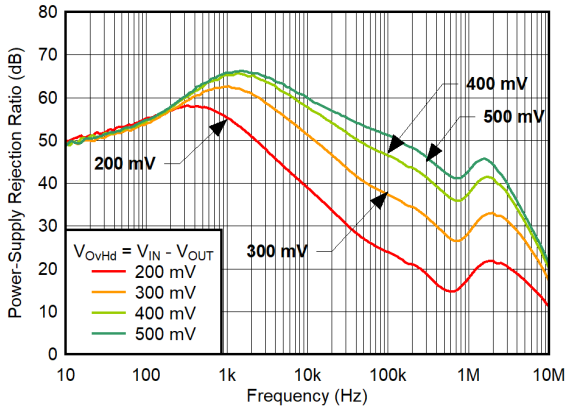
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-1. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 400 mA, V_{OUT} = 1.8 V



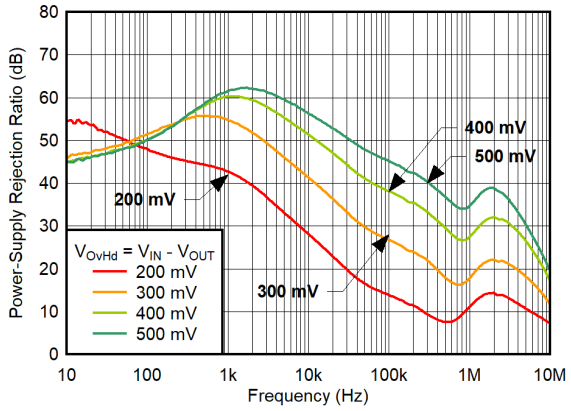
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-2. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 750 mA, V_{OUT} = 1.8 V



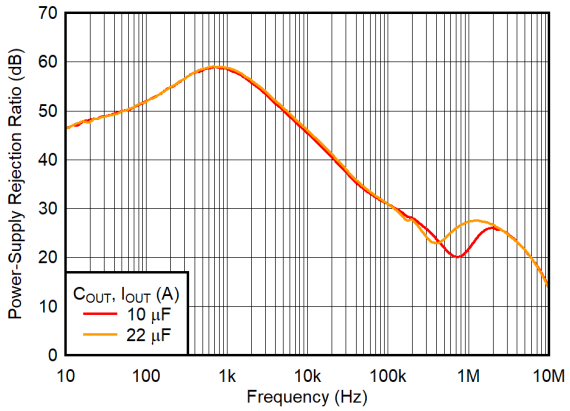
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-3. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 1.1 A, V_{OUT} = 1.8 V



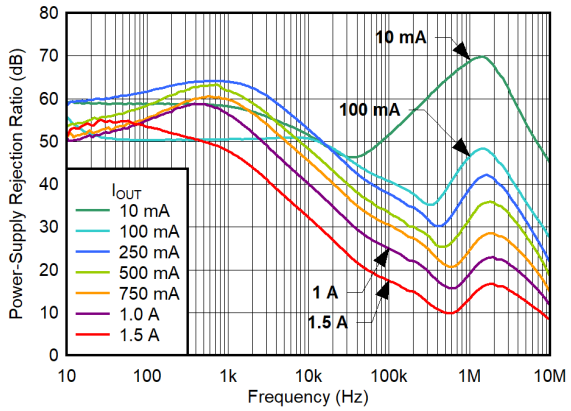
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-4. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 1.5 A, V_{OUT} = 1.8 V



C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A

Figure 6-5. PSRR vs Frequency and C_{OUT} for V_{OUT} = 1.8 V



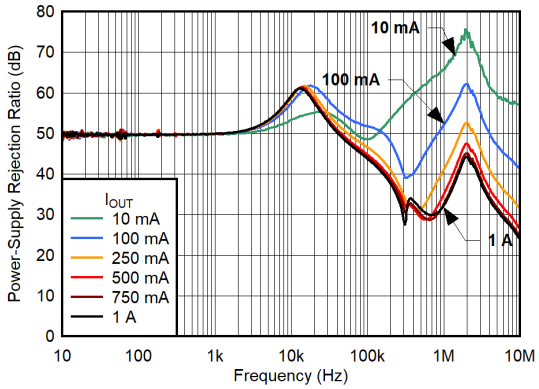
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-6. PSRR vs Frequency and I_{OUT} for V_{OvHd} = 200 mV

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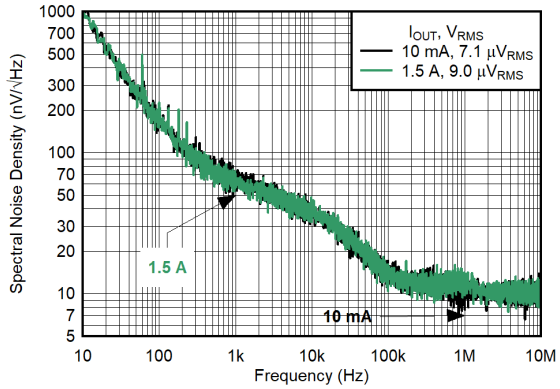
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



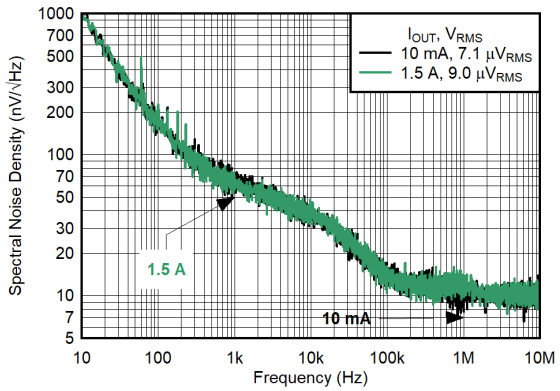
V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0 µF, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-7. Bias Rail PSRR vs Frequency and I_{OUT}



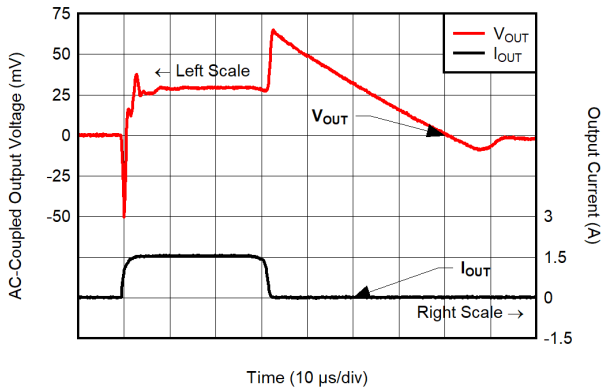
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-8. Noise vs Frequency and I_{OUT} for V_{OUT} = 0.65 V



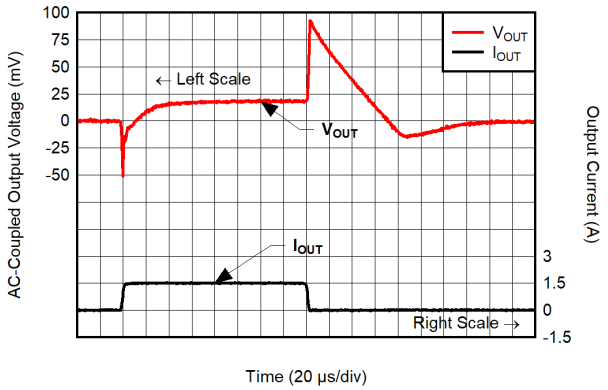
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-9. Noise vs Frequency and I_{OUT} for V_{OUT} = 3.3 V



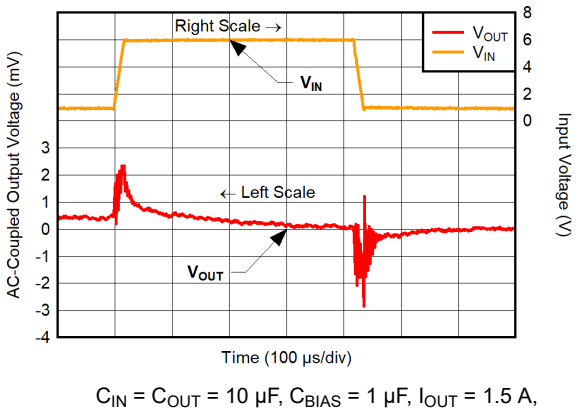
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 10 mA to 1.5 A to 10 mA at 1 A/µs

Figure 6-10. Load Transient for V_{OUT} = 0.65 V



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 10 mA to 1.5 A to 10 mA at 1 A/µs

Figure 6-11. Load Transient for V_{OUT} = 3.3 V



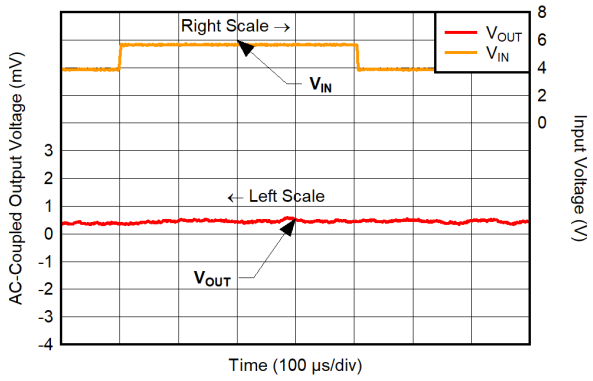
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 0.95 V to 6 V to 0.95 V at 1 V/µs

Figure 6-12. Line Transient for V_{OUT} = 0.65 V

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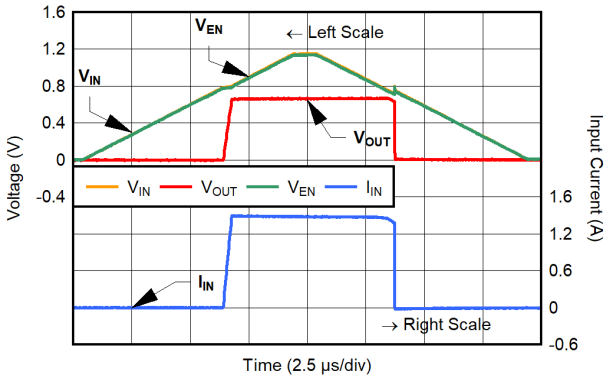
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



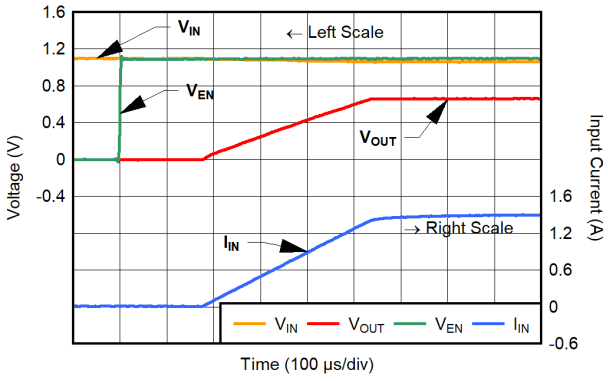
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 3.9 V to 5.8 V to 3.9 V at 1 V/µs

Figure 6-13. Line Transient for V_{OUT} = 3.3 V



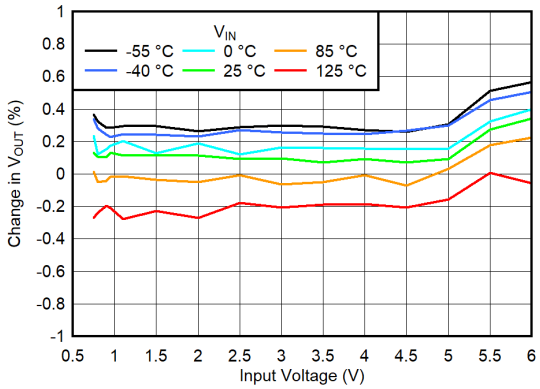
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{BIAS} = 5 V

Figure 6-14. Input Ramp-Up and Ramp-Down



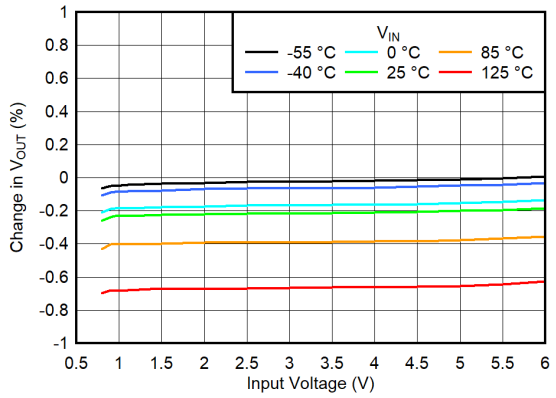
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 1.1 V, V_{BIAS} = 5 V

Figure 6-15. Input Ramp With Fast Soft-Start



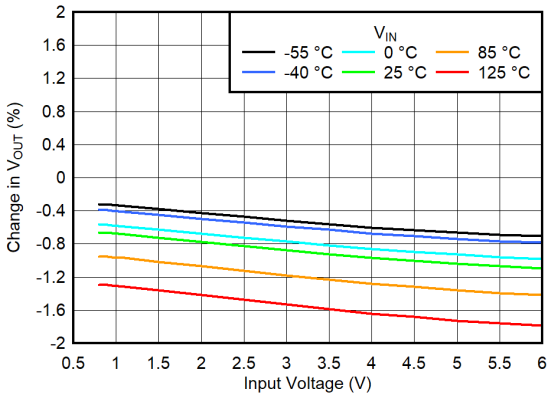
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-16. IN Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 0 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-17. IN Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 10 mA



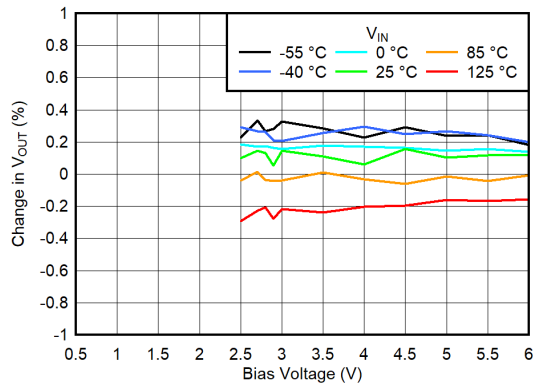
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-18. IN Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 1.5 A

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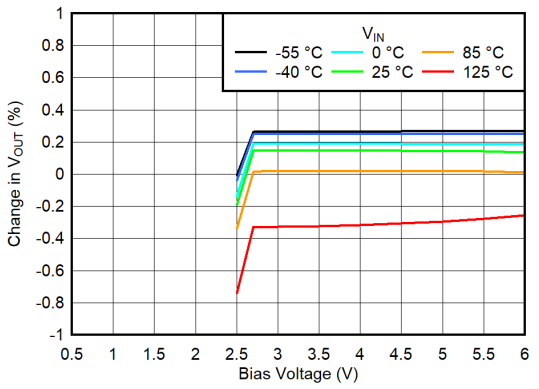
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



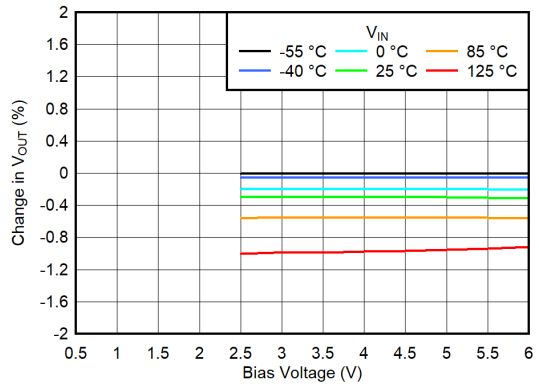
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-19. BIAS Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 0 A



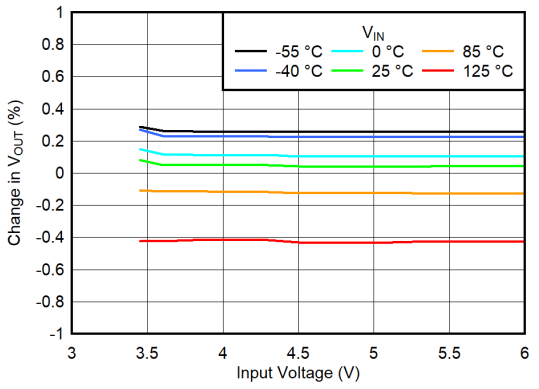
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-20. BIAS Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 10 mA



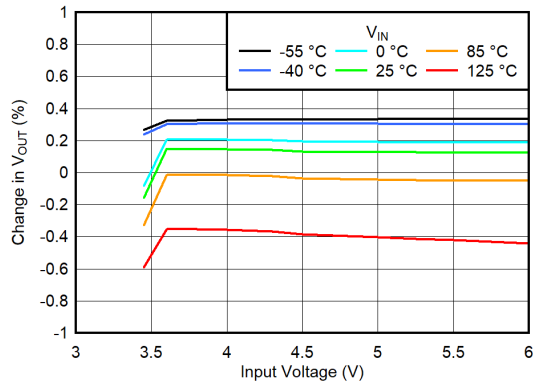
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-21. BIAS Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 1.5 A



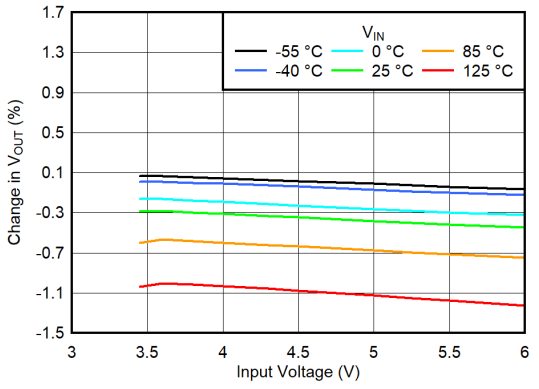
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-22. IN Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 0 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-23. IN Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 10 mA



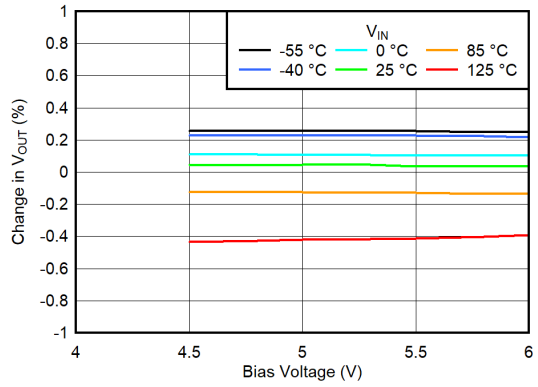
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-24. IN Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 1.5 A

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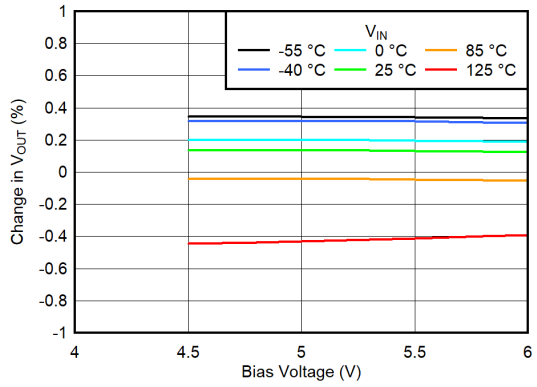
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



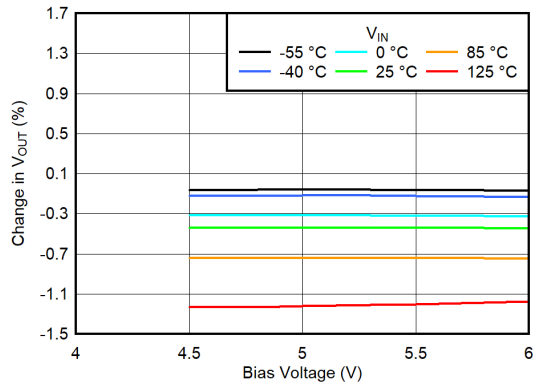
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 3.6 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.1 V

Figure 6-25. BIAS Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 0 A



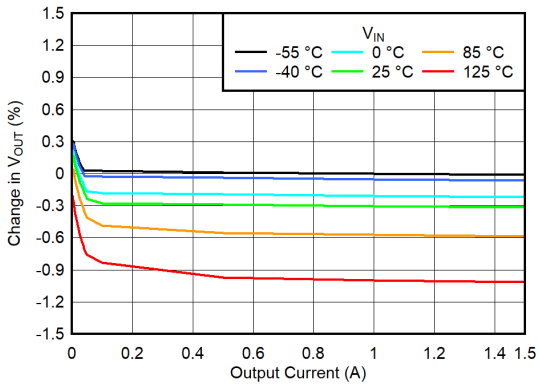
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 3.6 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.1 V

Figure 6-26. BIAS Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 10 mA



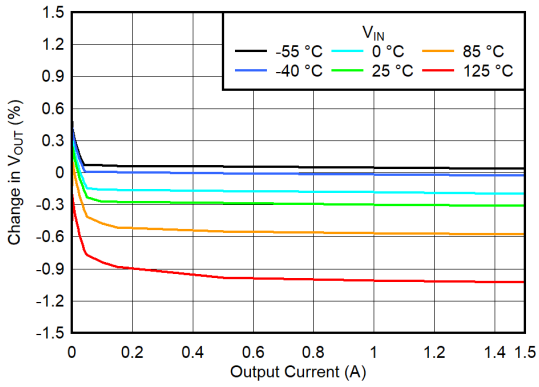
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 3.6 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.1 V

Figure 6-27. BIAS Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 1.5 A



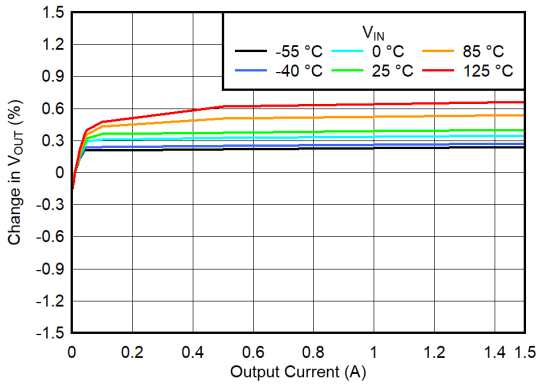
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, 2.3 V ≤ V_{BIAS} ≤ 5 V, V_{EN} = 1.1 V

Figure 6-28. Load Regulation for I_{OUT} = 0 A to Load, V_{OUT} = 0.65 V



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-29. Load Regulation for I_{OUT} = 0 A to Load, V_{OUT} = 3.3 V



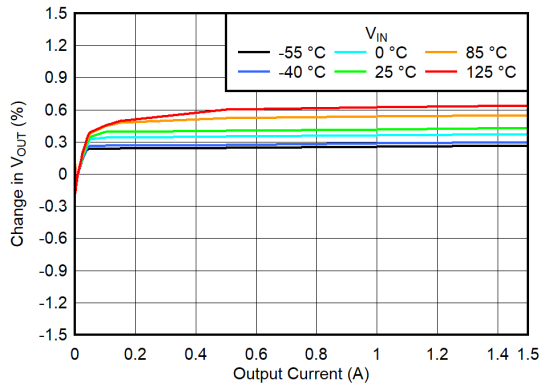
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, 2.3 V ≤ V_{BIAS} ≤ 5 V, V_{EN} = 1.1 V

Figure 6-30. Load Regulation for I_{OUT} = 10 mA to Load, V_{OUT} = 0.65 V

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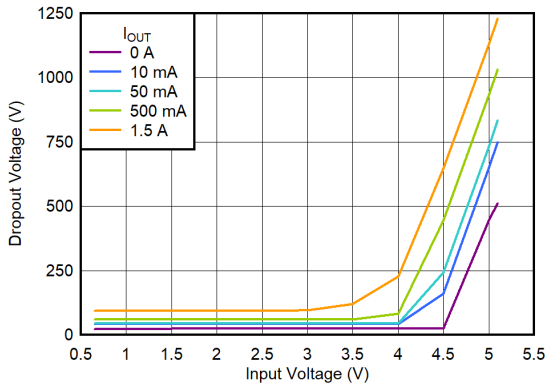
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



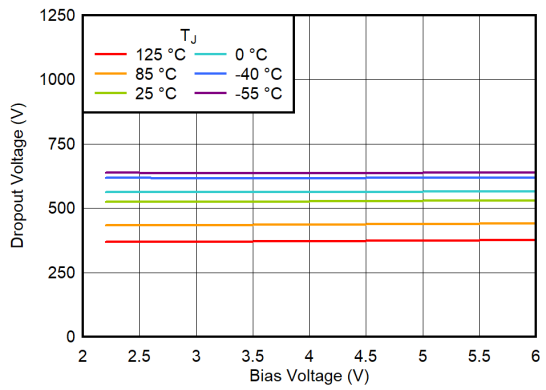
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-31. Load Regulation for I_{OUT} = 10 mA to Load, V_{OUT} = 3.3 V



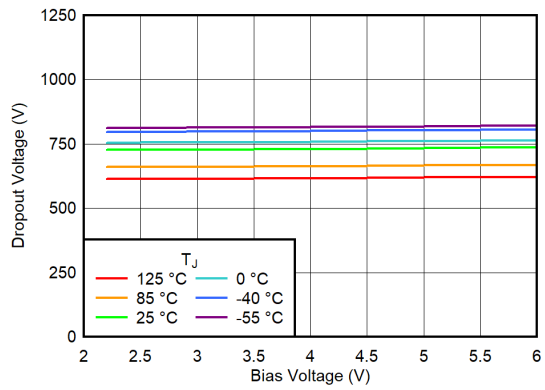
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-32. Dropout Voltage vs Input Voltage



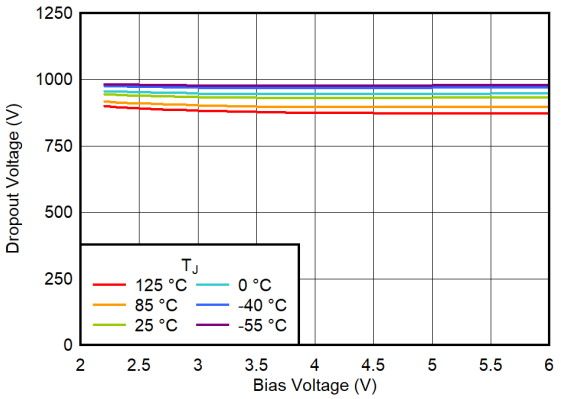
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-33. Dropout Voltage vs Bias Voltage for I_{OUT} = 0 A



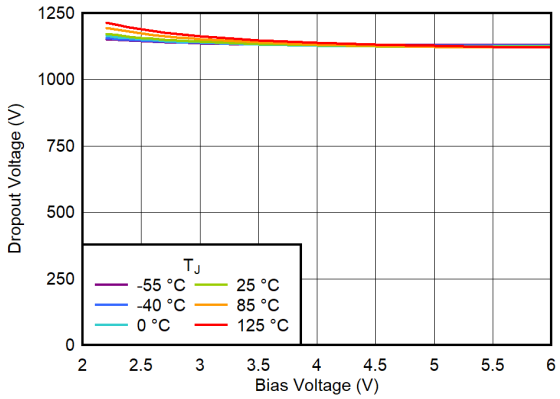
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-34. Dropout Voltage vs Bias Voltage for I_{OUT} = 50 mA



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-35. Dropout Voltage vs Bias Voltage for I_{OUT} = 500 mA



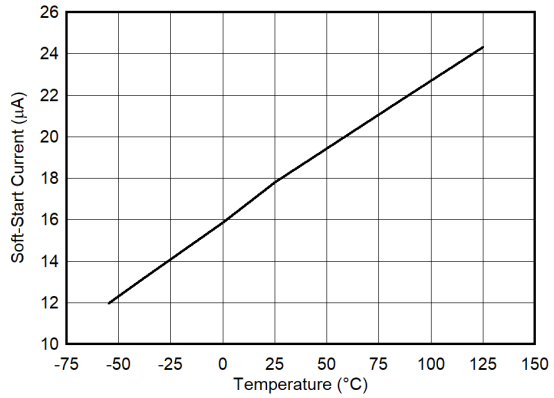
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-36. Dropout Voltage vs Bias Voltage for I_{OUT} = 1.5 A

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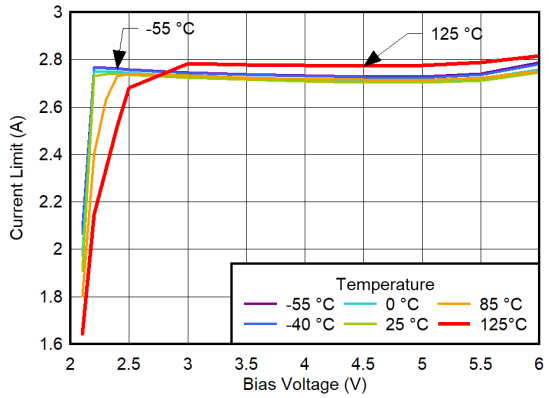
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



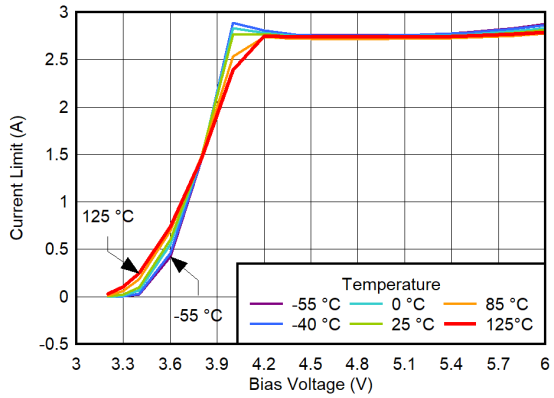
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN} = 6 V, V_{OUT} = 0.65 V, V_{EN} = 1.5 V, I_{OUT} = 0 A

Figure 6-37. Soft-Start Current vs Temperature



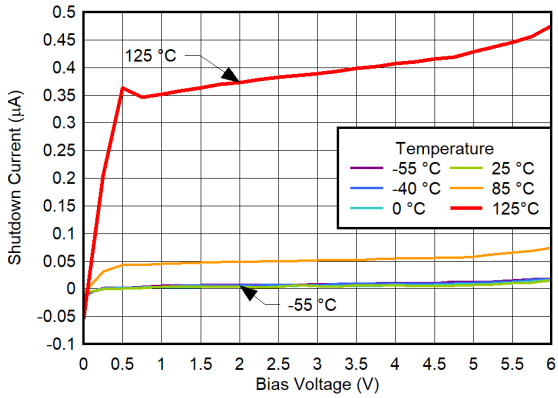
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-38. Current Limit vs Bias Voltage for V_{OUT} = 0.65 V



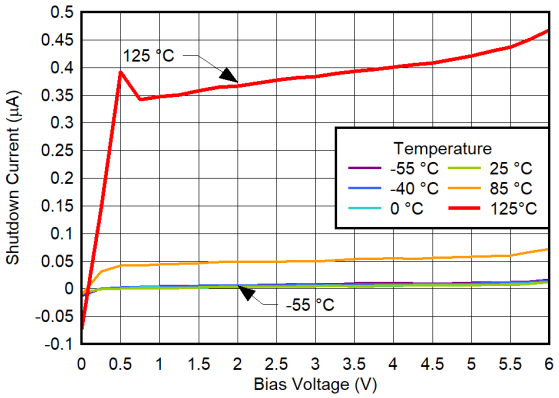
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{EN} = 1.1 V

Figure 6-39. Current Limit vs Bias Voltage for V_{OUT} = 3.3 V



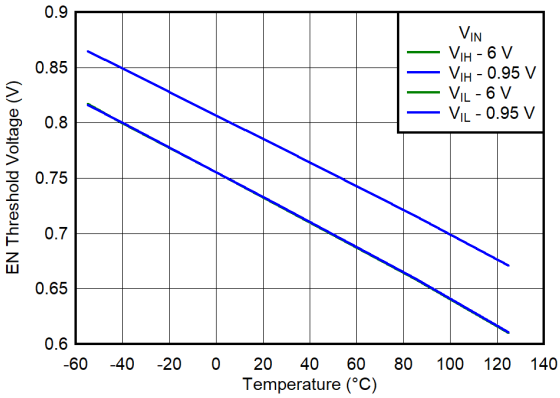
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{EN} = 0.4 V

Figure 6-40. Shutdown Current vs Bias Voltage for V_{IN} = 0.95 V



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{EN} = 0.4 V

Figure 6-41. Shutdown Current vs Bias Voltage for V_{IN} = 6 V



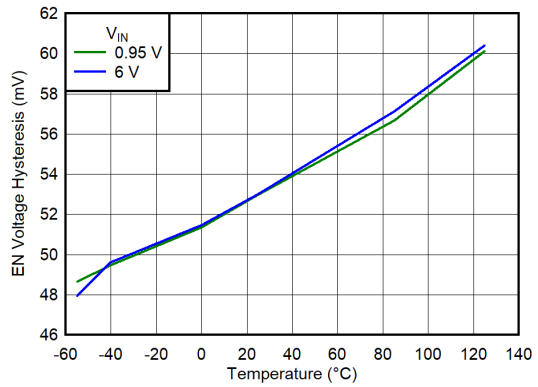
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 6 V

Figure 6-42. Enable Voltage Threshold vs Temperature

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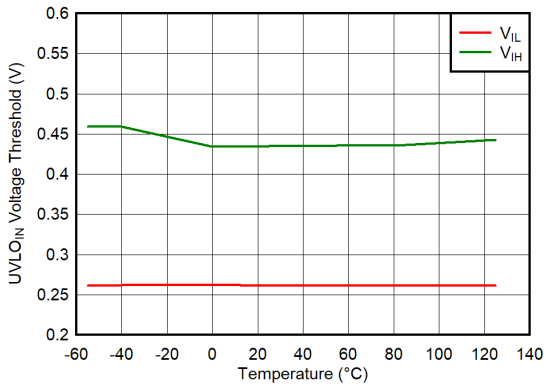
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



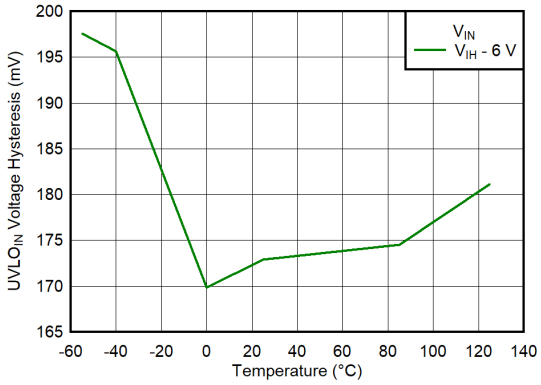
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 6 V

Figure 6-43. Enable Voltage Hysteresis vs Temperature



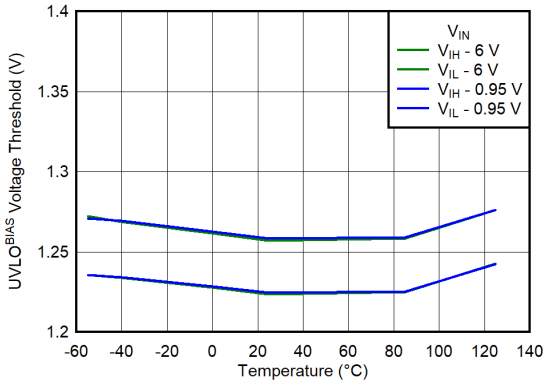
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-44. $UVLO_{IN}$ Voltage Threshold vs Temperature



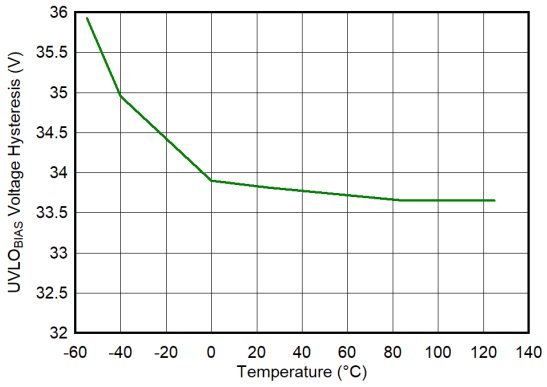
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-45. $UVLO_{IN}$ Voltage Hysteresis vs Temperature



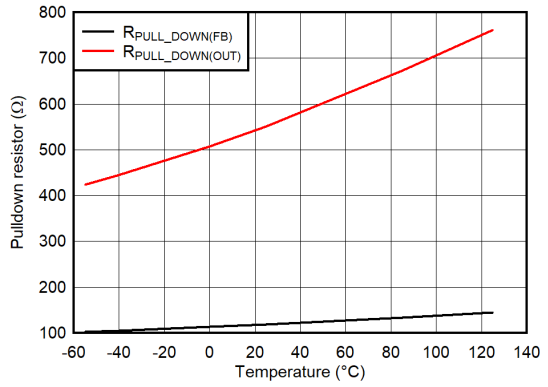
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-46. $UVLO_{BIAS}$ Voltage Threshold vs Temperature



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-47. $UVLO_{BIAS}$ Voltage Hysteresis vs Temperature



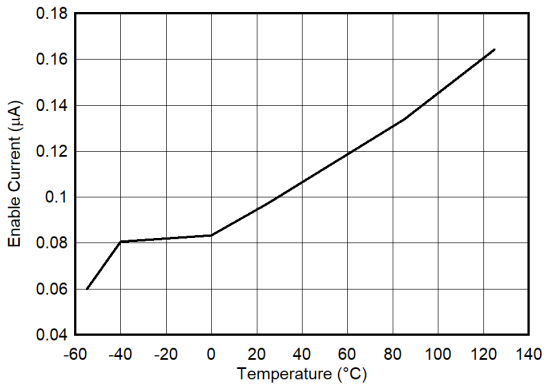
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 6 V, V_{EN} ≤ 0.4 V

Figure 6-48. Pulldown Resistors vs Temperature

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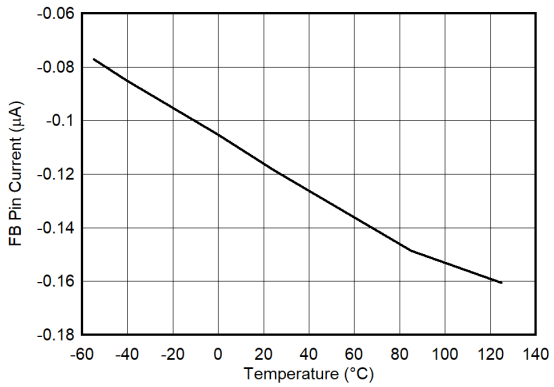
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



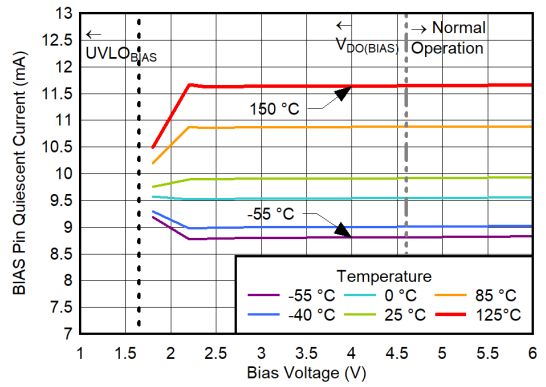
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 6 V, $V_{OUT(NOM)}$ = 0.65 V, V_{BIAS} = 6 V, I_{OUT} = 2 mA, V_{EN} = 6 V

Figure 6-49. EN Pin Current vs Temperature



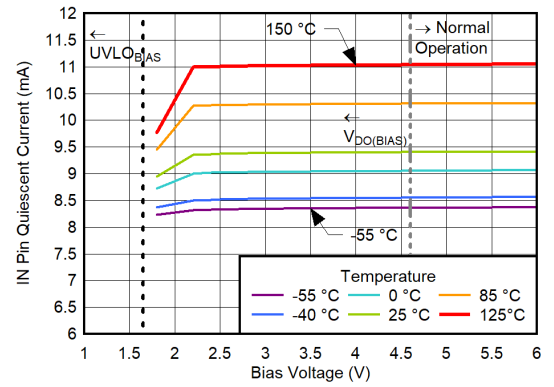
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 0.95 V ≤ V_{IN} ≤ 6 V, $V_{OUT(NOM)}$ = 0.65 V, V_{BIAS} = 6 V, I_{OUT} = 2 mA, V_{EN} = 6 V

Figure 6-50. FB Pin Current vs Temperature



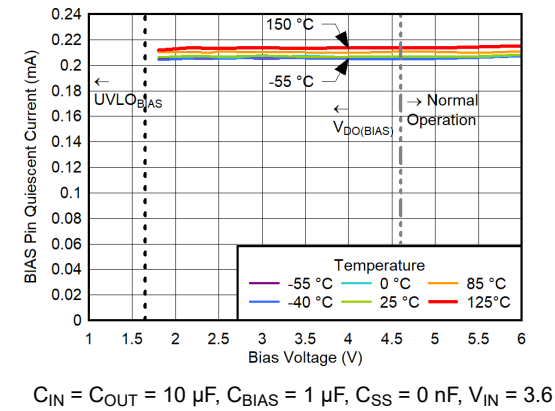
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-51. BIAS Pin Quiescent Current vs Bias Voltage for I_{OUT} = 1.5 A



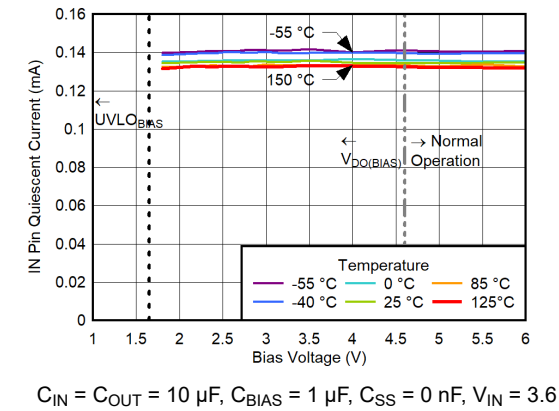
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-52. IN Pin Quiescent Current vs Bias Voltage for I_{OUT} = 1.5 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-53. BIAS Pin Quiescent Current vs Bias Voltage for I_{OUT} = 10 mA



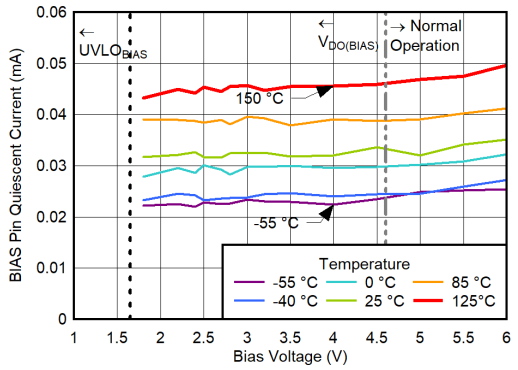
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-54. IN Pin Quiescent Current vs Bias Voltage for I_{OUT} = 10 mA

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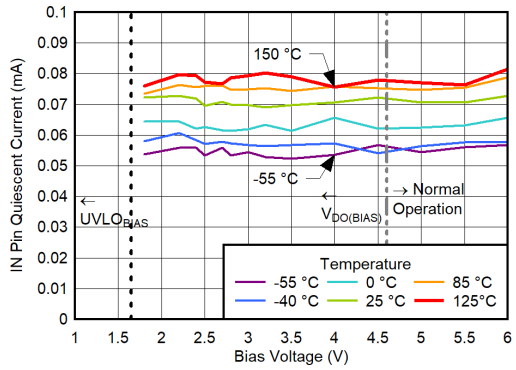
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



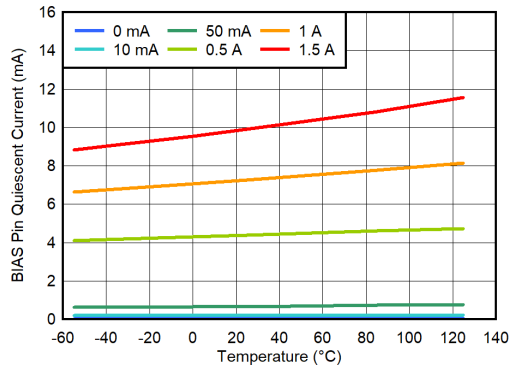
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-55. BIAS Pin Quiescent Current vs Bias Voltage for I_{OUT} = 0 A



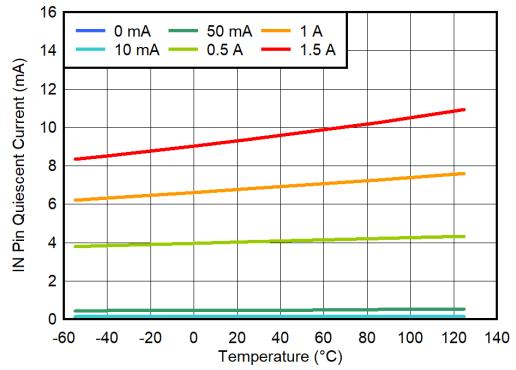
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-56. IN Pin Quiescent Current vs Bias Voltage for I_{OUT} = 0 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-57. BIAS Pin Quiescent Current vs Temperature



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-58. IN Pin Quiescent Current vs Temperature

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7 Detailed Description

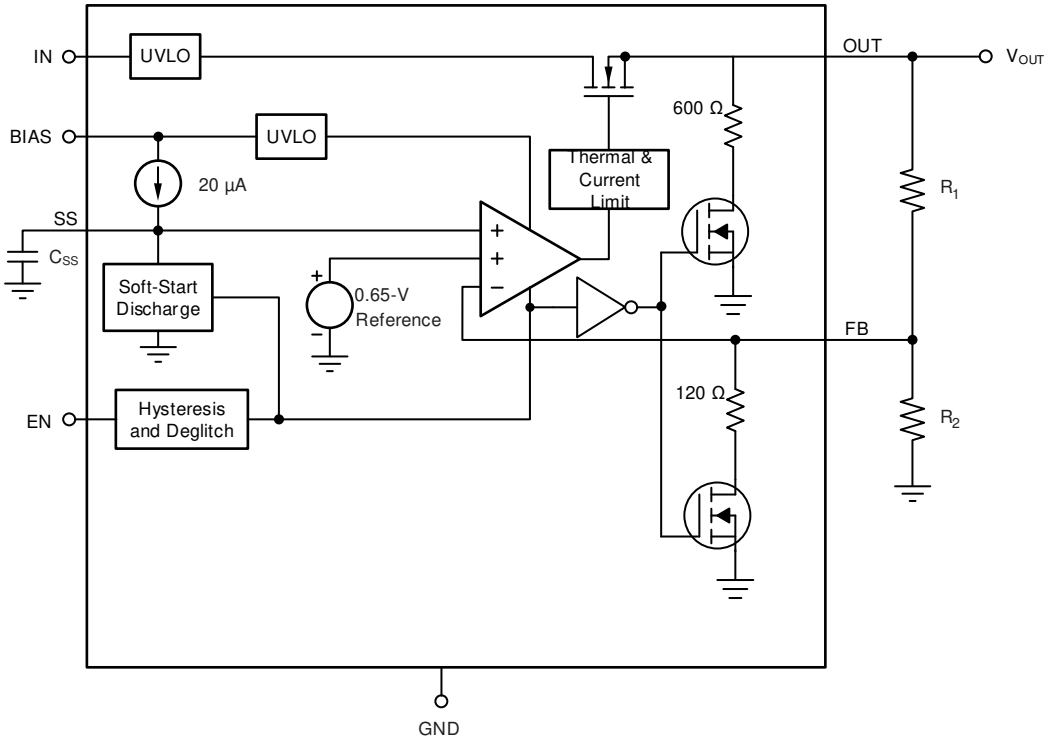
7.1 Overview

The TPS7A74 is a low-input, low-output, low-quiescent-current linear regulator optimized to support excellent transient performance. This regulator uses a low-current bias rail to power all internal control circuitry, allowing the n-type field effect transistor (NMOS) pass transistor to regulate very-low input and output voltages.

Using an NMOS-pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS7A74 to be stable with any ceramic capacitor 10 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS7A74 features a programmable voltage-controlled, soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Shutdown

The enable (EN) pin is active high and compatible with standard digital-signaling levels. Setting V_{EN} below 0.4 V turns the regulator off, and setting V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the device to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.75 V and varies with temperature and process variations, see Figure 6-42. Temperature variation is approximately –1.2 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used.

If not used, EN can be connected to BIAS. Place the connection as close as possible to the bias capacitor.

7.3.2 Active Discharge

The TPS7A74 has two internal active pulldown circuits: one on the FB pin and one on the OUT pin.

Each active discharge function uses an internal metal-oxide-semiconductor field-effect transistor (MOSFET) that connects a resistor ($R_{PULLDOWN}$) to ground when the low-dropout resistor (LDO) is disabled in order to actively discharge the output voltage. The active discharge circuit is activated when the device is disabled by driving EN to logic low, when the voltage at IN or BIAS is below the UVLO threshold, or when the regulator is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

The first active pulldown circuit connects the output to GND through a 600-Ω resistor when the device is disabled.

The second circuit connects FB to GND through a 120-Ω resistor when the device is disabled. This resistor discharges the FB pin. Equation 1 calculates the output capacitor discharge time constant when OUT is shorted to FB, or when the output voltage is set to 0.65 V.

$$\tau_{OUT} = (600 \,||\, 120 \times R_L / (600 \,||\, 120 + R_L) \times C_{OUT} \quad (1)$$

If the LDO is set to an output voltage greater than 0.65 V, a resistor divider network is in place and minimizes the FB pin pulldown. Equation 2 and Equation 3 calculate the time constants set by these discharge resistors.

$$R_{DISCHARGE} = (120 \,||\, R_2) + R_1 \quad (2)$$

$$\tau_{OUT} = R_{DISCHARGE} \times R_L / (R_{DISCHARGE} + R_L) \times C_{OUT} \quad (3)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input and can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

See Figure 6-48 for additional information.

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7.3.3 Global Undervoltage Lockout (UVLO) Circuit

Two undervoltage lockout (UVLO) circuits are present to prevent the TPS7A74 from turning on with an insufficient rail. One circuit is present on the BIAS pin and the other circuit is on the IN pin. The two UVLO signals are connected internally through an AND gate, as shown in Figure 7-1, that turns off the device when the voltage on either input is below their respective UVLO thresholds.

In other words, the output is disabled until the IN pin voltage reaches a value greater than $UVLO_{IN}$ and the BIAS pin voltage reaches a voltage greater than $UVLO_{BIAS}$.

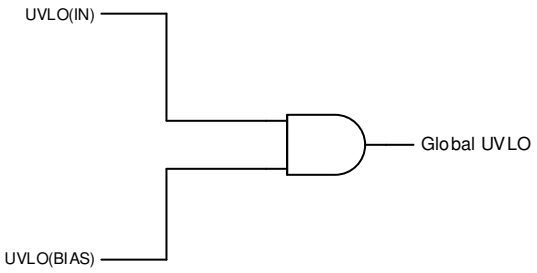


Figure 7-1. Global UVLO Circuit

7.3.4 Internal Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the *short-circuit current limit* (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ is approximately 60% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in a brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. When the device sufficiently cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note. Figure 7-2 illustrates a diagram of the foldback current limit.

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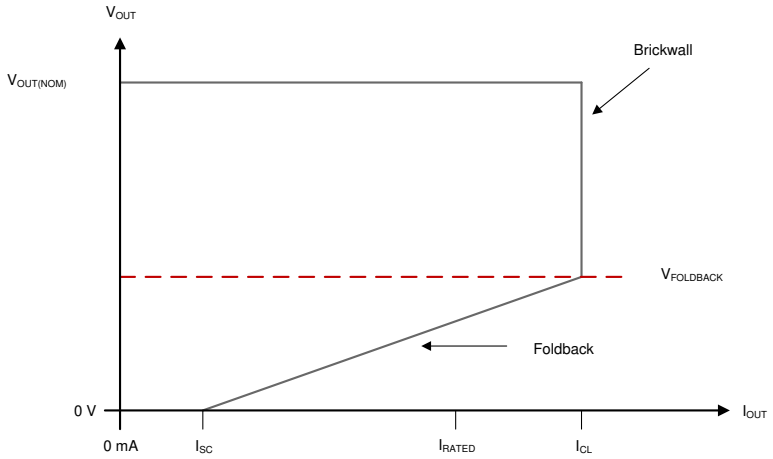


Figure 7-2. Foldback Current Limit

7.3.5 Thermal Shutdown Protection (T_{SD})

The internal thermal shutdown protection circuit disables the output when the thermal junction temperature (T_J) of the pass transistor rises to the thermal shutdown temperature threshold, $T_{SD(shutdown)\ (typical)}$. The thermal shutdown circuit hysteresis ensures that the LDO resets (turns on) when the temperature falls to $T_{SD(reset)\ (typical)}$.

The thermal time constant of the semiconductor die is fairly short; thus, the device may cycle on and off when thermal shutdown is reached until the power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the regulator into thermal shutdown, or above the maximum recommended junction temperature, reduces long-term reliability.

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7.4 Device Functional Modes

Table 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT\ (nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT\ (nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and functions as a switch. Line or load transients in dropout can result in large output voltage deviations.

When operating in dropout, the ground current may increase. For dropout operation and the effect on the IN and BIAS current, see Figure 6-51 to Figure 6-56.

When the device is in a steady dropout state, defined as when the device is in dropout, ($V_{IN} < V_{OUT} + V_{DO}$ or $V_{BIAS} < V_{OUT} + V_{DO}$ directly after being in normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

7.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than $V_{IL(EN)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

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7.5 Programming

7.5.1 Programmable Soft-Start

The TPS7A74 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because the soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}). Equation 4 calculates the soft-start ramp time.

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \tag{4}$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. The start-up time is given by Equation 5 in this case.

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \tag{5}$$

where:

- $V_{OUT(nom)}$ is the nominal output voltage
- C_{OUT} is the output capacitance
- $I_{CL(min)}$ is the minimum current limit for the device

In applications where monotonic start up is required, the soft-start time given by Equation 4 must be set greater than Equation 5.

The maximum recommended soft-start capacitor is 15 nF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 15 nF can be a problem in applications where the enable pin must be rapidly pulsed and the device must soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Table 7-2 lists suggested soft-start capacitor values.

Table 7-2. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1 ms
1 nF	0.032 ms
5.6 nF	0.182 ms
10 nF	0.325 ms

(1) $t_{SS}(s) = \frac{V_{REF} \cdot C_{SS}}{I_{SS}} = \frac{0.65V \cdot C_{SS}(F)}{20\mu A}$, where $t_{SS}(s)$ = soft-start time in seconds.

Another option to set the start-up rate is to use a feedforward capacitor; see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note for more information.

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7.5.2 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate.

There are several different start-up responses that are possible, but not typical:

- If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until reaching the set output voltage
- If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}
- If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}
- If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor

Figure 7-3 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

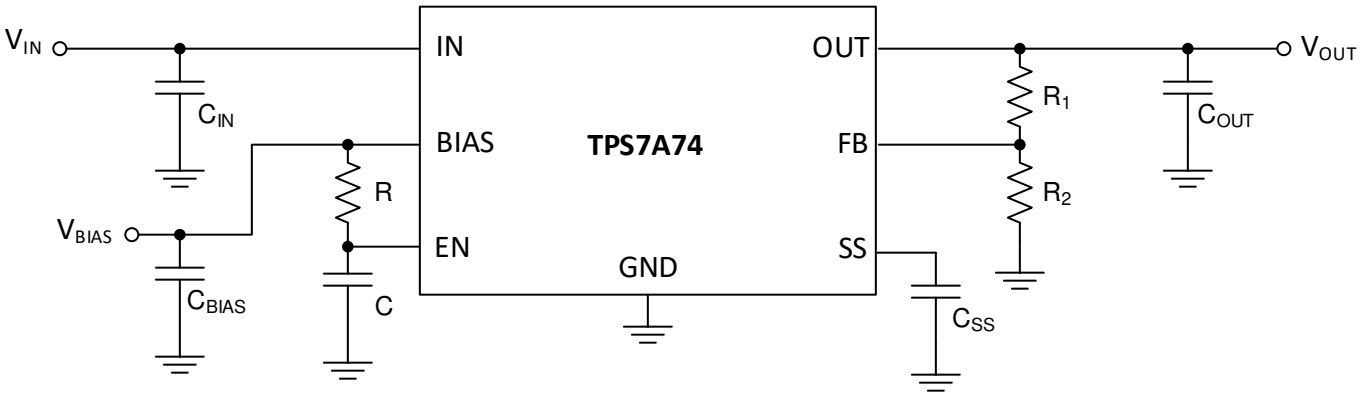


Figure 7-3. Soft-Start Delay Using an RC Circuit to Enable the Device

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A74 is a low-input, low-output (LILO) low-dropout regulator (LDO) that feature soft-start capability. This regulator uses a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows stability with ceramic capacitors of 10 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

A programmable voltage-controlled, soft-start circuit provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

8.1.1 Adjusting the Output Voltage

Figure 8-1 shows the typical application circuit for the adjustable output device.

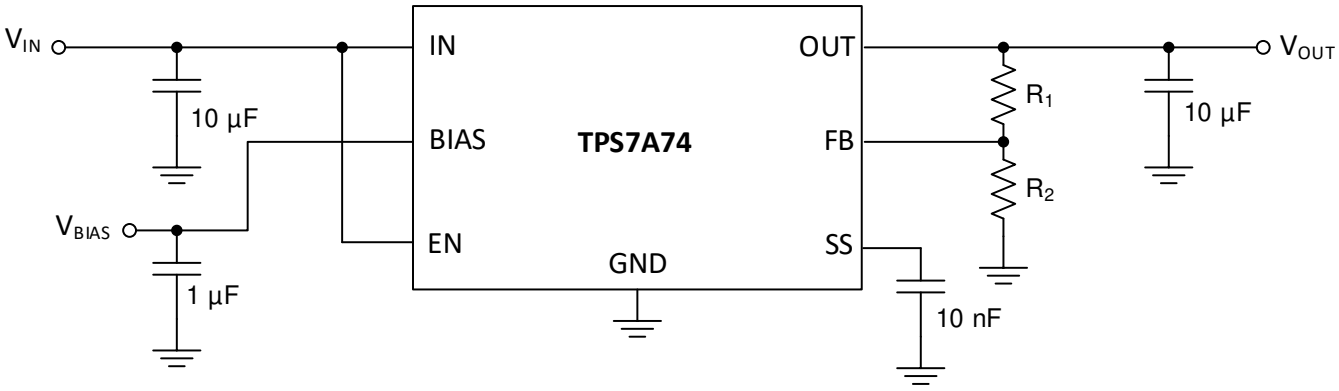


Figure 8-1. Typical Application Circuit for the TPS7A74 (Adjustable)

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 8-1. Table 8-1 lists sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 must be ≤ 4.99 kΩ.

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Table 8-1. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	Targeted V_{OUT} (V)
Short	Open	0.65
0.768	4.99	0.75
2.43	4.53	1.00
2.72	4.42	1.05
3.48	4.99	1.10
4.22	4.99	1.20
4.99	3.83	1.50
4.99	2.80	1.80
4.99	1.74	2.51
4.99	1.21	3.33

(1) $V_{OUT} = 0.65 \times (1 + R_1 / R_2)$.

Note

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

Because this LDO has a relatively low quiescent current of 50 µA, some applications may benefit from using larger R_1 and R_2 resistor values. In such cases where resistor values greater than 5 kΩ are considered, adding a C_{ff} capacitor across R_1 may help improve stability.

8.1.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for ceramic capacitor of values ≥ 10 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1 µF and the minimum recommended capacitor for V_{BIAS} is 0.1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Use good quality, low equivalent series resistance (ESR) and equivalent series inductance (ESL) capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close the pins as possible for optimum performance.

Low ESR and ESL capacitors improve high-frequency PSRR.

8.1.3 Transient Response

The TPS7A74 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see Figure 6-10 in the *Typical Characteristics* section. Because the TPS7A74 is stable with output capacitors as low as 10 µF, many applications may then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

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8.1.4 Dropout Voltage

The TPS7A74 offers very low dropout performance, making the device well-suited for high-current, low V_{IN} and low V_{OUT} applications. The low dropout allows the device to be used in place of a dc/dc converter and still achieve good efficiency. Equation 6 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \tag{6}$$

This efficiency provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solutions.

For this architecture, there are two different specifications for dropout voltage. The first specification (see Figure 8-2) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 2.8 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 5.0-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} + 2.8 V, the V_{IN} dropout is less than specified.

Note

2.8 V is a test condition of this device and can be adjusted by referring to the *Electrical Characteristics* table.

The second specification (illustrated in Figure 8-2) is referred to as *V_{BIAS} dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.3 V above V_{OUT}. Because of this usage, having IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the device package.

8.1.5 Output Noise

The TPS7A74 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 1-nF, soft-start capacitor, the output noise is reduced by half and is typically 7.1 μV_{RMS} for a 0.65-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. Equation 7 gives the RMS noise with a 1-nF, soft-start capacitor:

$$V_N(\mu V_{RMS}) = 7.1 \cdot \left(\frac{\mu V_{RMS}}{V}\right) \cdot V_{OUT}(V) \tag{7}$$

The low output noise makes this LDO a good choice for powering transceivers, phase-locked loops (PLLs), or other noise-sensitive circuitry.

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8.1.6 Estimating Junction Temperature

By using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 8). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{8}$$

Where P_D is the power dissipation shown by Equation 9, T_T is the temperature at the center-top of the package, and T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*.

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.

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8.2 Typical Application

8.2.1 FPGA I/O Supply at 1.8 V With a Bias Rail

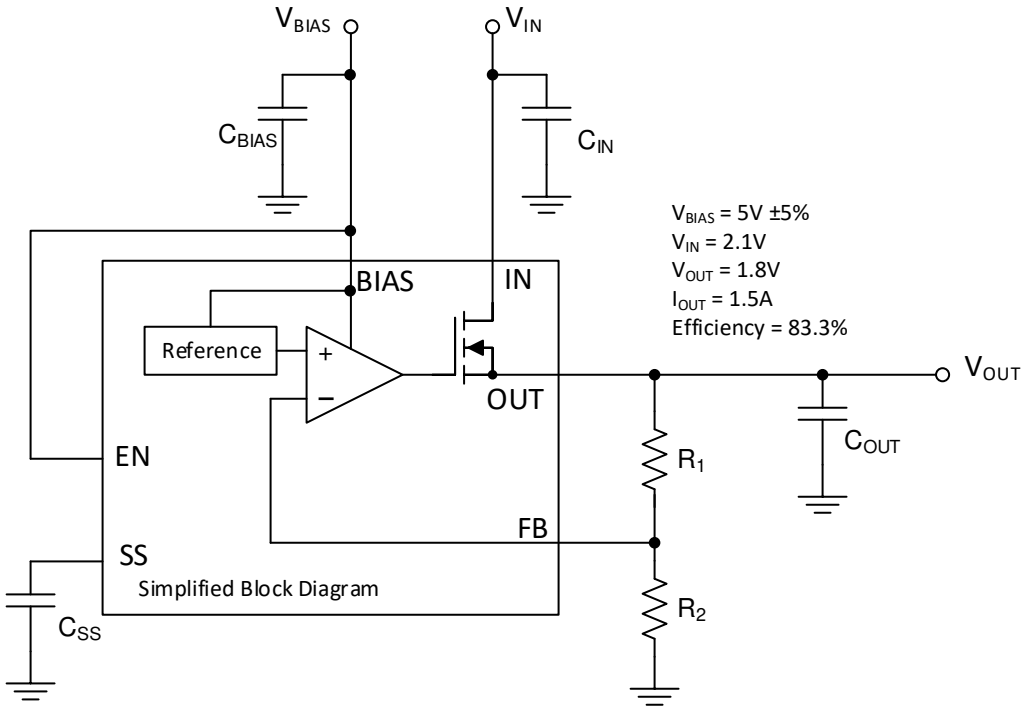


Figure 8-2. Typical Application Using an Auxiliary Bias Rail

8.2.1.1 Design Requirements

This application powers the I/O rails of an FPGA , at $V_{OUT(nom)}$ = 1.8 V and $I_{OUT(dc)}$ = 1.5 A. The available external supply voltages are 2.1 V, 3.3 V, and 5 V.

Table 8-2 lists the parameters for this design example.

Table 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	2.1 V
V_{BIAS}	2.4 V to 5.5 V
V_{OUT}	1.8 V
I_{OUT}	600 mA (typical), 900 mA (peak)

8.2.1.2 Detailed Design Procedure

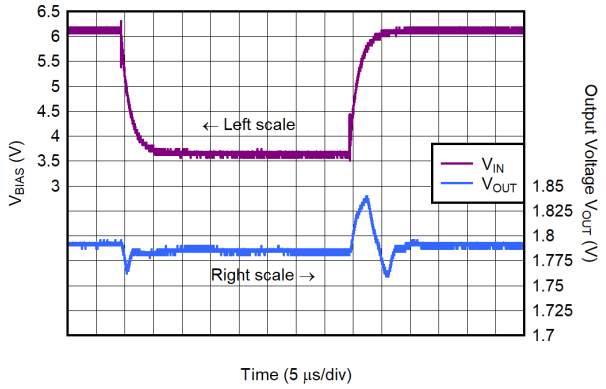
First, determine what supplies to use for the input and bias rails. A 2.1-V input can be stepped down to 1.5 V at 1.5 A if an external bias is provided, because the maximum dropout voltage is 180 mV if V_{BIAS} is at least 2.8 V higher than V_{OUT}. To achieve this voltage step, the bias rail is supplied by the 5-V supply. The approximation in Equation 6 estimates the efficiency at 83.3%.

The output voltage then must be set to 1.5 V. As Table 8-1 describes, set R_1 = 4.99 kΩ and R_2 = 3.82 kΩ to obtain the required output voltage. The minimum capacitor sizing requires the total solution size footprint to be reduced; see the *Input, Output, and Bias Capacitor Requirements* section for C_{IN} = 1 µF, C_{BIAS} = 1 µF, and C_{OUT} = 2.2 µF. Use C_{SS} = 1 nF for a typical 0.032-ms start-up time.

Figure 8-2 shows a simplified version of the final circuit.

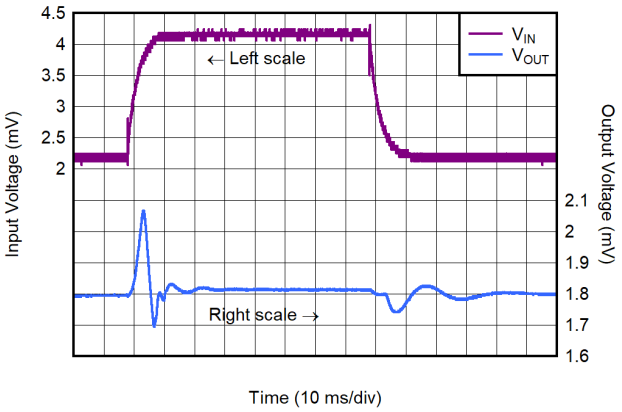
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8.2.1.3 Application Curves



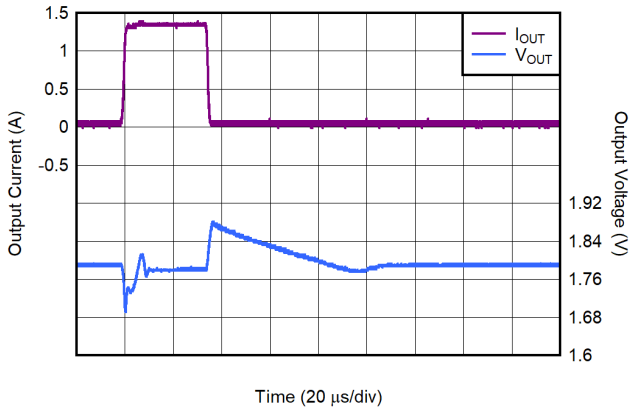
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{IN} = 2.1 V, V_{BIAS} = 6 V to 3.5 V to 6 V, I_{OUT} = 1.5 A

Figure 8-3. V_{BIAS} Line Transient



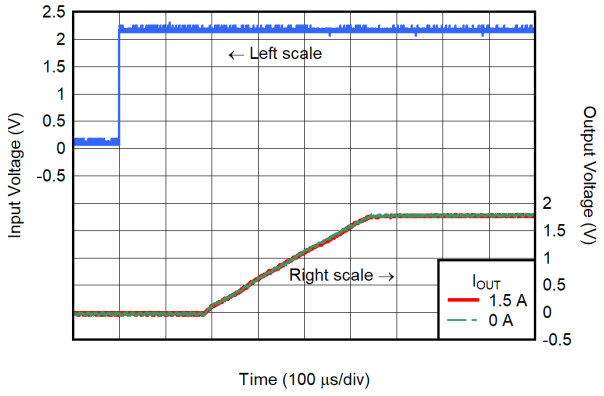
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{BIAS} = 5 V, V_{IN} = 2.1 V to 4.1 V to 2.1 V, I_{OUT} = 1.5 A

Figure 8-4. V_{IN} Line Transient



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{BIAS} = 5 V, V_{IN} = 2.1 V, I_{OUT} = 10 mA to 1.5 A to 10 mA

Figure 8-5. Output Load Transient Response



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{BIAS} = 5 V, V_{IN} = 2.1 V, I_{OUT} = 0 mA

Figure 8-6. Turn-On Response

8.3 Power Supply Recommendations

The TPS7A74 is designed to operate from an input voltage up to 6.0 V, provided the bias rail is at least 1.3 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin. This supply must have at least 1 µF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1 µF or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7-µF capacitor is required for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

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8.4 Layout

8.4.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 8-1 must be connected as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation (P_D) of the device depends on input voltage and load conditions. Equation 9 calculates P_D.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{9}$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the WSON (DSD) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, this pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. Equation 10 calculates the maximum junction-to-ambient thermal resistance.

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{10}$$

Note

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

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8.4.1.1 Estimating Junction Temperature

By using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 11). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{11}$$

Where P_D is the power dissipation shown by Equation 9, T_T is the temperature at the center-top of the package, and T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*.

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.

8.4.2 Layout Example

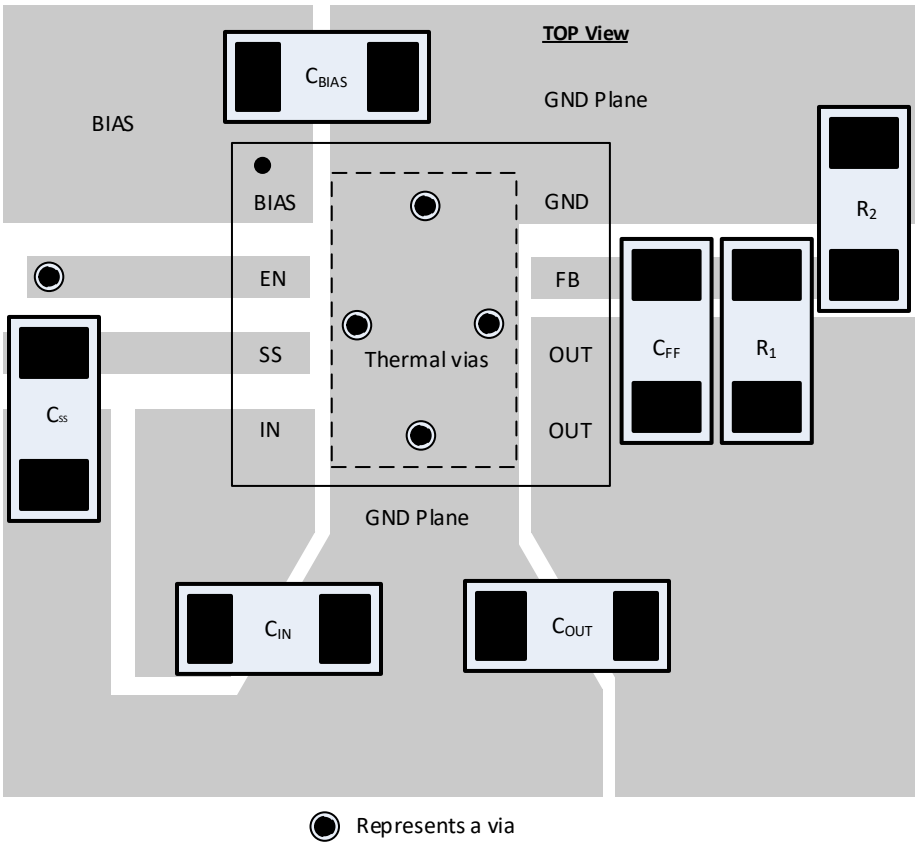


Figure 8-7. Example Layout (DSD Package)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A74. The evaluation module(and related user guide user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A74 is available through the product folders under *Tools & Software*.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Ultimate Regulation with Fixed Output Versions of TPS742xx, TPS743xx, and TPS744xx* application note
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note
- Texas Instruments, *TPS74701EVM-177 and TPS74801EVM-177* user's guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A7401DSDR	Active	Production	SON (DSD) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A7401
TPS7A7401DSDR.A	Active	Production	SON (DSD) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A7401

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

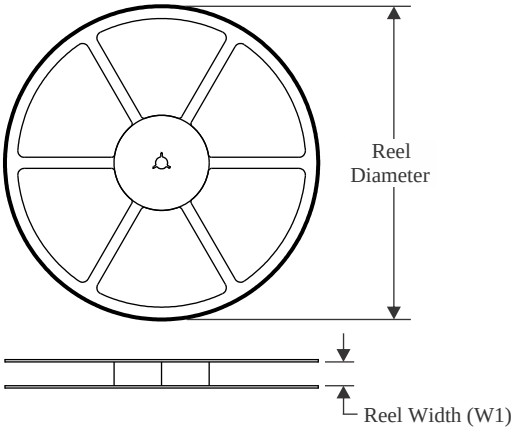
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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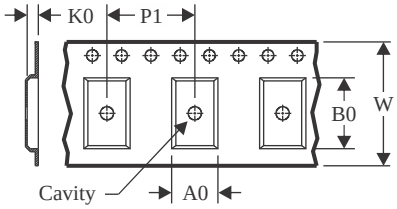
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

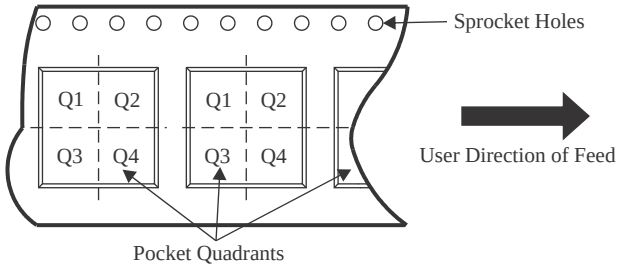


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

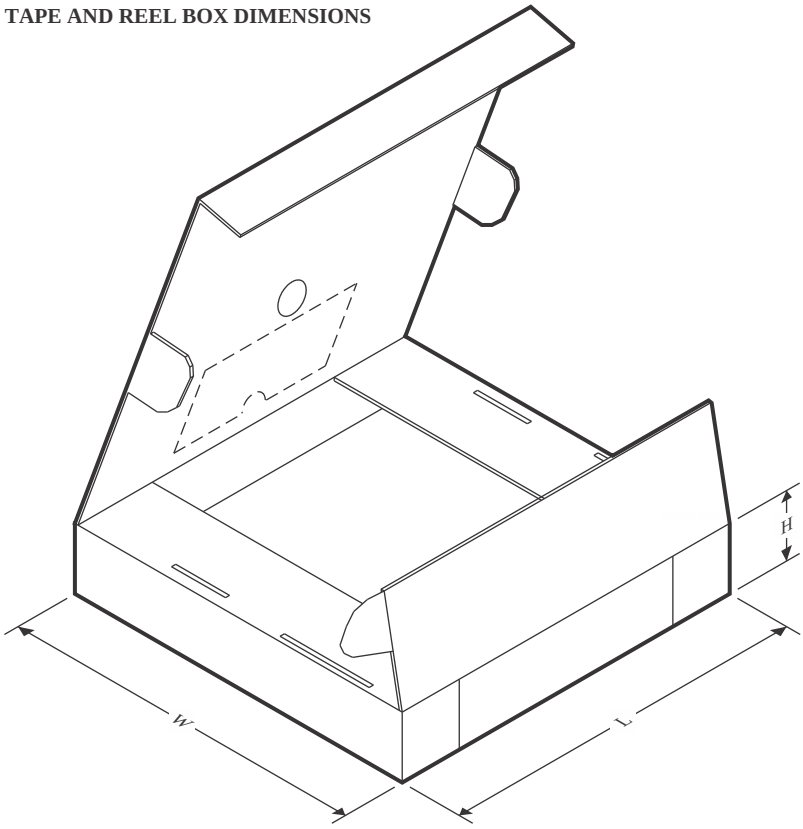
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7401DSDR	SON	DSD	8	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7401DSDR	SON	DSD	8	5000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

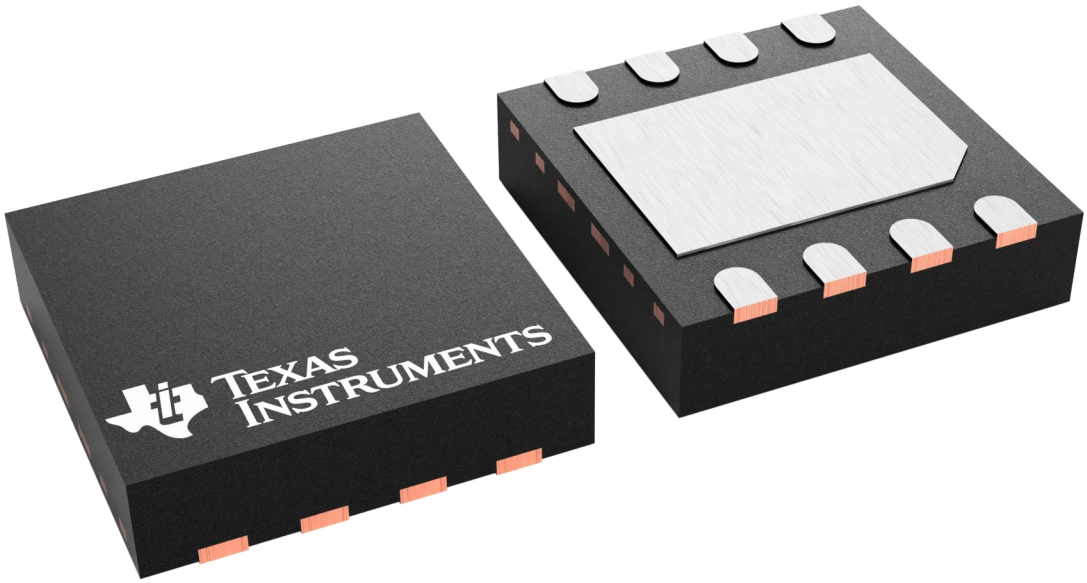
DSD 8

WSON - 0.8 mm max height

3 X 3, 0.8 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



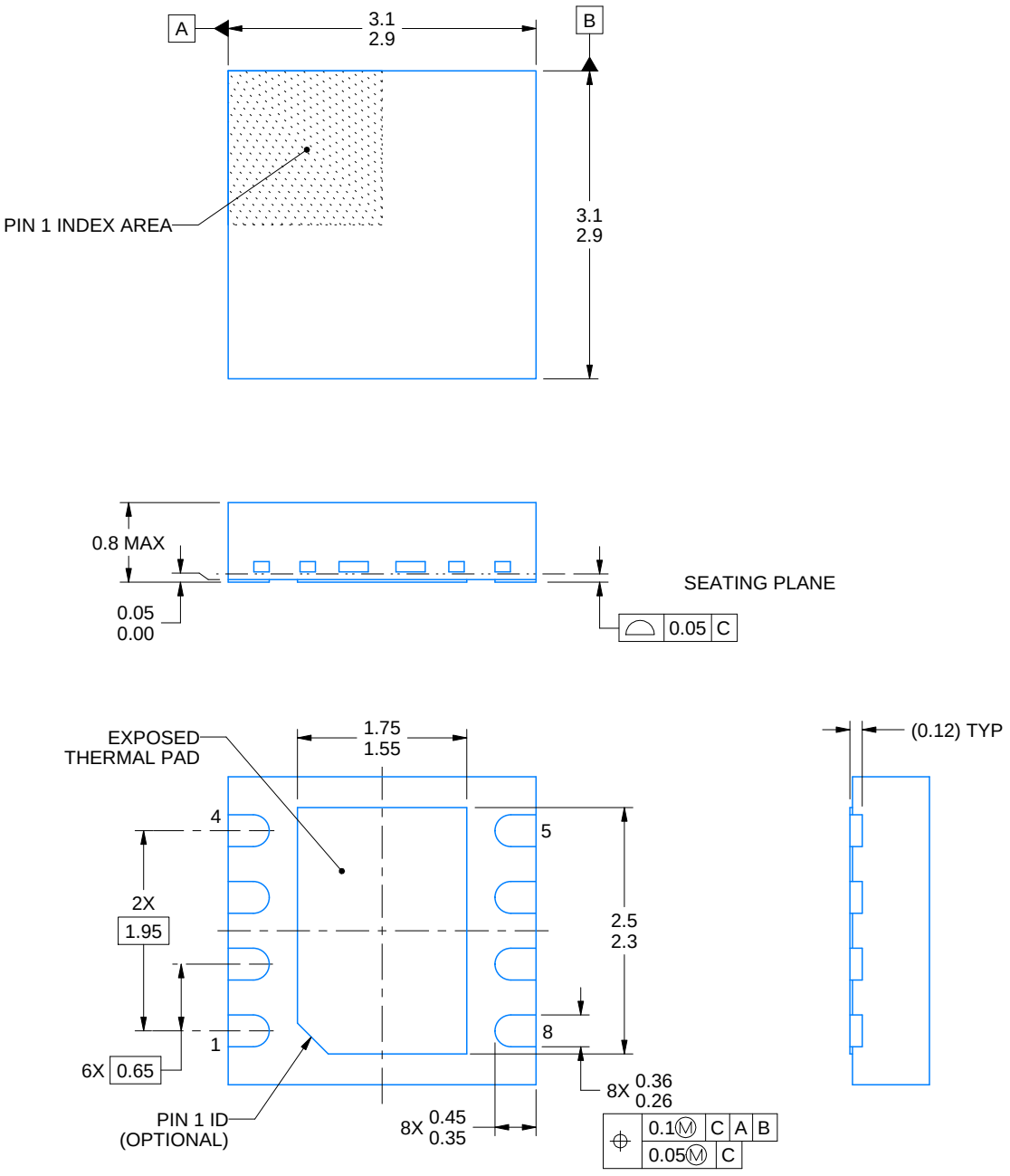
4227007/A

DSD0008B

PACKAGE OUTLINE

WSON - 0.8 mm max height

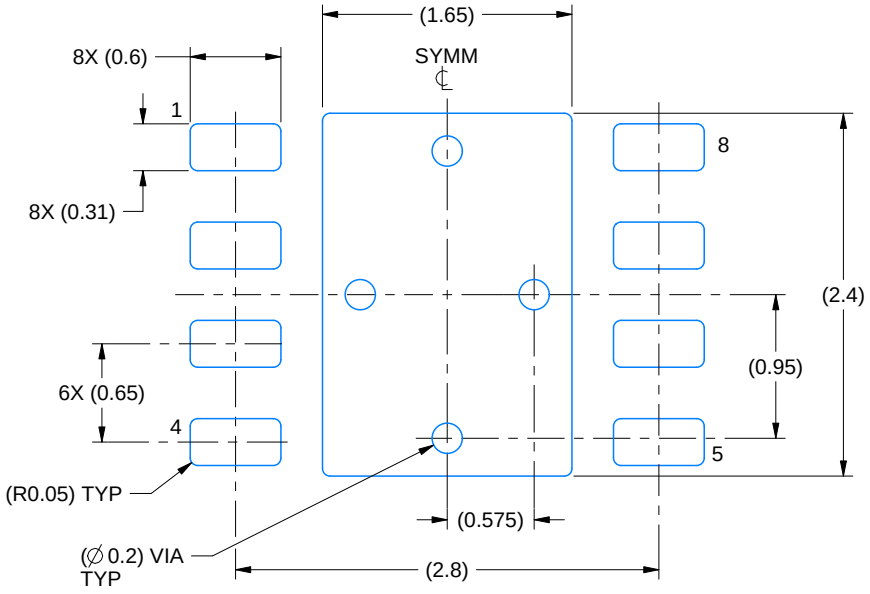
PLASTIC SMALL OUTLINE - NO LEAD



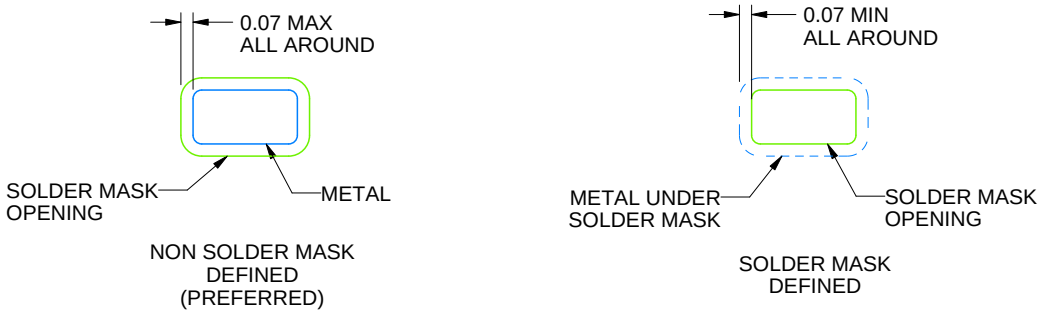
4226923/A 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4226923/A 06/2021

NOTES: (continued)

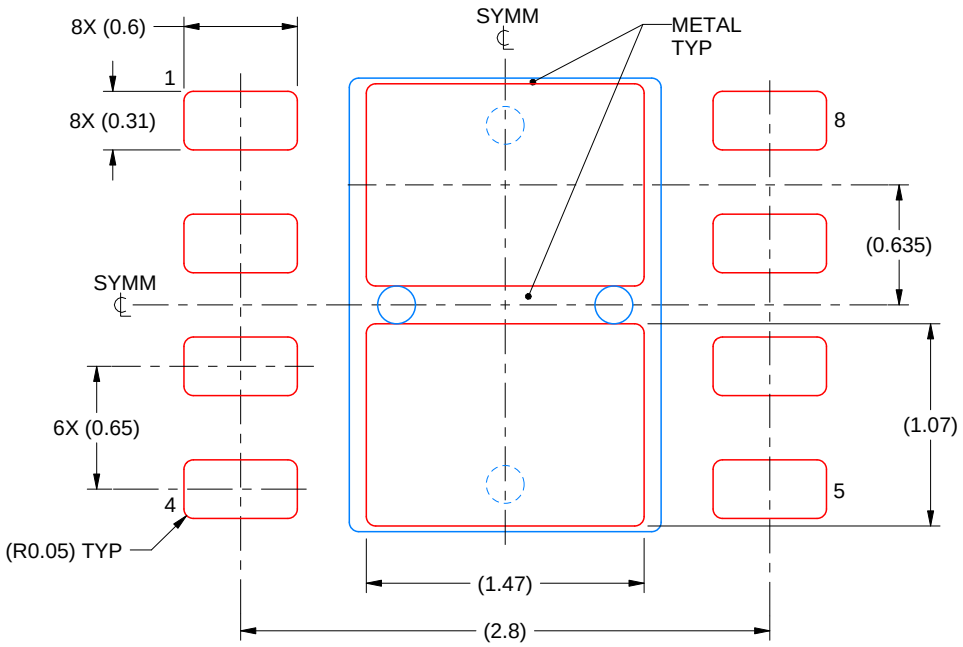
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSD0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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