TOP264-271
TOPSwitch-JX Family

Integrated Off-Line Switcher with EcoSmart™ Technology
for Highly Efficient Power Supplies

Product Highlights

EcoSmart – Energy Efficient
- Ideal for applications from 10 W to 245 W
- Energy efficient over entire load range
- No-load consumption below 100 mW at 265 VAC
- Up to 750 mW standby output power for 1 W input at 230 VAC

High Design Flexibility for Low System Cost
- Multi-mode PWM control maximizes efficiency at all loads
- 132 kHz operation reduces transformer and power supply size
  - 66 kHz option for highest efficiency requirements
- Accurate programmable current limit
- Optimized line feed-forward for line ripple rejection
- Frequency jittering reduces EMI filter cost
- Fully integrated soft-start for minimum start-up stress
- 725 V rated MOSFET
  - Simplifies meeting design derating requirements

Extensive Protection Features
- Auto-restart limits power delivery to <3% during overload faults
  - Output short-circuit protection (SCP)
  - Output over-current protection (OCP)
  - Output overload protection (OPP)
- Output overvoltage protection (OVP)
  - User programmable for hysteretic/latching shutdown
  - Simple fast AC reset
  - Primary or secondary sensed
- Line undervoltage (UV) detection prevents turn-off glitches
- Line overvoltage (OV) shutdown extends line surge withstand
- Accurate thermal shutdown with large hysteresis (OTP)

Advanced Package Options
- eDIP™-12 package:
  - 43 W / 117 W universal input power output capability with PCB / metal heat sink
  - Low profile horizontal orientation for ultra-slim designs
  - Heat transfer to both PCB and heat sink
  - Optional external heat sink provides thermal impedance equivalent to a TO-220
- eSIP™-7C package:
  - 177 W universal input output power capability
  - Vertical orientation for minimum PCB footprint
  - Simple heat sink mounting using clip provides thermal impedance equivalent to a TO-220
- eSOP™-12 package:
  - 66 W universal input output power capability
  - Low profile surface mounted for ultra-slim designs
  - Heat transfer to PCB via exposed pad and SOURCE pins
  - Supports wave or reflow soldering
- Extended creepage to DRAIN pin
- Heat sink is connected to SOURCE for low EMI

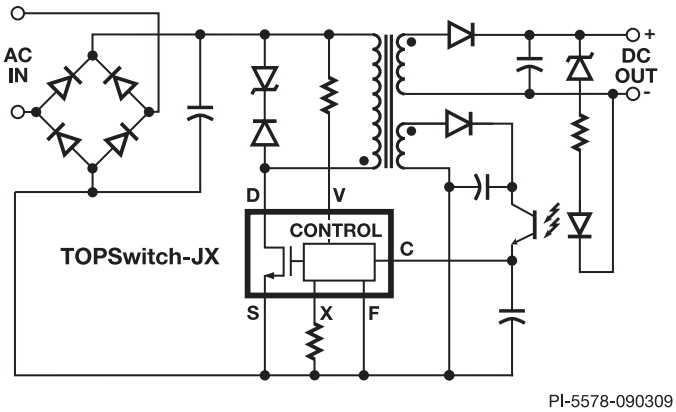
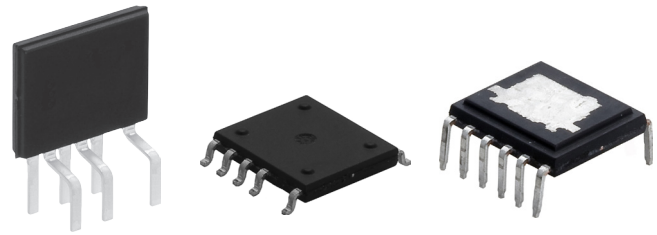


Figure 1. Typical Flyback Application.



eSIP-7C (E Package) eSOP-12B (K Package) eDIP-12B (V Package)

Figure 2. Package Options.

Description

TOPSwitch™-JX cost effectively incorporates a 725 V power MOSFET, high-voltage switched current source, multi-mode PWM control, oscillator, thermal shutdown circuit, fault protection and other control circuitry onto a monolithic device.

Typical Applications
- Notebook or laptop adapter
- Generic adapter
- Printer
- LCD monitor
- Set-top box
- PC or LCD TV standby
- Audio amplifier

Output Power Ratings
See next page.

This Product is Covered by Patents and/or Pending Patent Applications.

Output Power Table

Product[5]	PCB Copper Area[1]				Product[5]	Metal Heat Sink[1]			
	230 VAC ±15%[4]		85-265 VAC			230 VAC ±15% [4]		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]		Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
TOP264VG	21 W	34 W	12 W	22.5 W	**TOP264EG/VG**	30 W	62 W	20 W	43 W
TOP264KG	30 W	49 W	16 W	30 W					
TOP265VG	22.5 W	36 W	15 W	25 W	**TOP265EG/VG**	40 W	81 W	26 W	57 W
TOP265KG	33 W	53 W	20 W	34 W					
TOP266VG	24 W	39 W	17 W	28.5 W	**TOP266EG/VG**	60 W	119 W	40 W	86 W
TOP266KG	36 W	58 W	23 W	39 W					
TOP267VG	27.5 W	44 W	19 W	32 W	**TOP267EG/VG**	85 W	137 W	55 W	103 W
TOP267KG	40 W	65 W	26 W	45 W					
TOP268VG	30 W	48 W	21.5 W	36 W	**TOP268EG/VG**	105 W	148 W	70 W	112 W
TOP268KG	46 W	73 W	30 W	50 W					
TOP269VG	32 W	51 W	22.5 W	37.5 W	**TOP269EG/VG**	128 W	162 W	80 W	120 W
TOP269KG	50 W	81 W	33 W	55 W					
TOP270VG	34 W	55 W	24.5 W	41 W	**TOP270EG/VG**	147 W	190 W	93 W	140 W
TOP270KG	56 W	91 W	36 W	60 W					
TOP271VG	36 W	59 W	26 W	43 W	**TOP271EG/VG**	177 W	244 W	118 W	177 W
TOP271KG	63 W	102 W	40 W	66 W					

Table 1. Output Power Table.

Notes:
1. See Key Application Considerations section for more details.
2. Maximum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient temperature.
3. Maximum continuous power in an open frame design at +50 °C ambient temperature.
4. 230 VAC or 110/115 VAC with doubler.
5. Packages: E: eSIP-7C, V: eDIP-12, K: eSOP-12. See Part Ordering Information section.

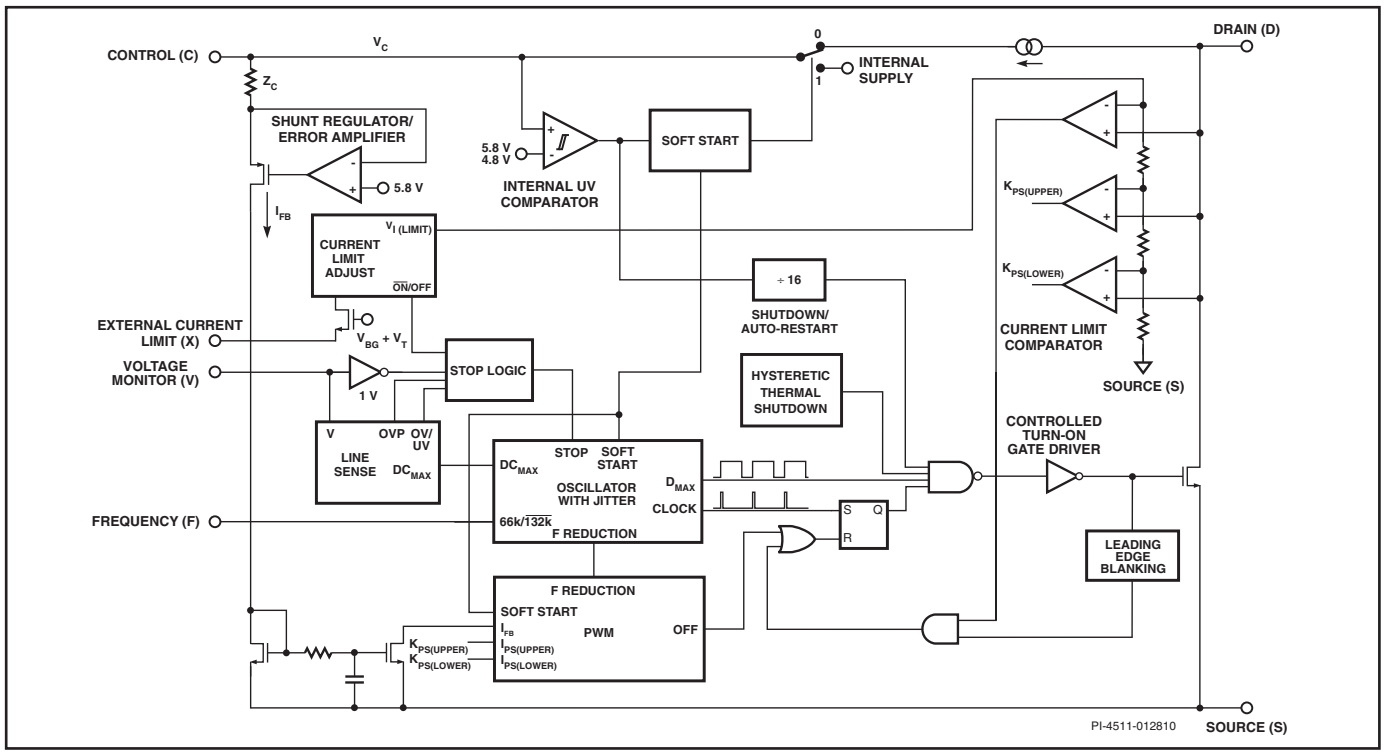


Figure 3. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
High-voltage power MOSFET DRAIN pin. The internal start-up bias current is drawn from this pin through a switched high-voltage current source. Internal current limit sense point for drain current.

CONTROL (C) Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the connection point for the supply bypass and auto-restart/ compensation capacitor.

EXTERNAL CURRENT LIMIT (X) Pin:
Input pin for external current limit adjustment remote-ON/OFF and device reset. A connection to SOURCE pin disables all functions on this pin. This pin should not be left floating.

VOLTAGE MONITOR (V) Pin:
Input for OV, UV, line feed-forward with DC_{MAX} reduction, output overvoltage protection (OVP), remote-ON/OFF. A connection to the SOURCE pin disables all functions on this pin. This pin should not be left floating.

FREQUENCY (F) Pin:
Input pin for selecting switching frequency 132 kHz if connected to SOURCE pin and 66 kHz if connected to CONTROL pin. This pin should not be left floating.

SOURCE (S) Pin:
Output MOSFET source connection for high-voltage power return. Primary-side control circuit common and reference point.

NO CONNECTION (NC) Pin:
Internally not connected, floating potential pin.

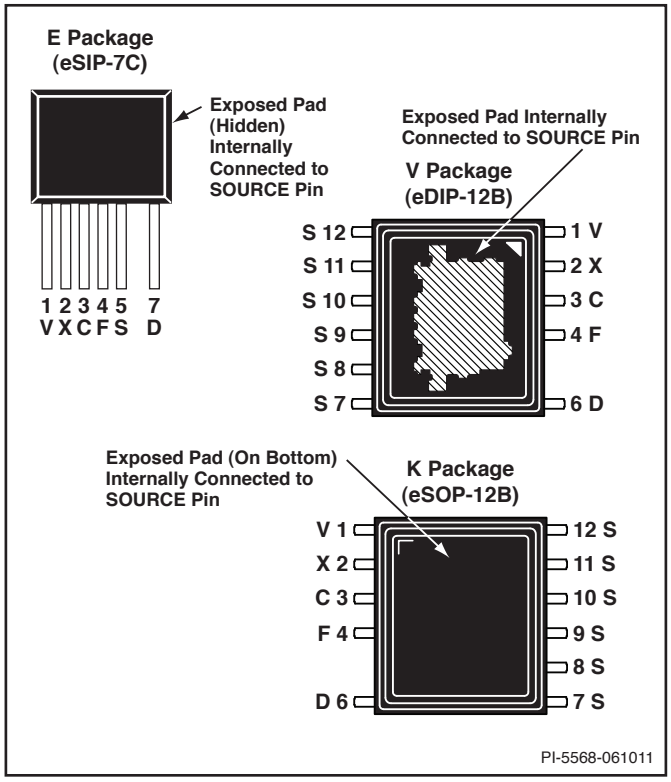


Figure 4. Pin Configuration (Top View).

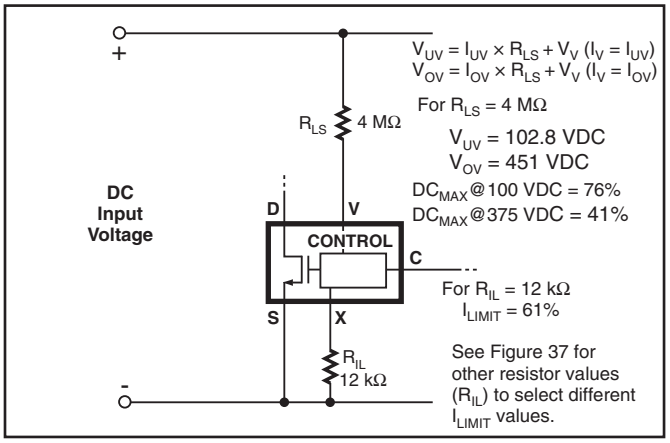


Figure 5. Package Line-Sense and Externally Set Current Limit.

TOP264-271 Functional Description

Like TOPSwitch-HX, TOP264-271 is an integrated switched mode power supply chip that converts a current at the control input to a duty cycle at the open drain output of a high-voltage power MOSFET. During normal operation the duty cycle of the power MOSFET decreases linearly with increasing CONTROL pin current as shown in Figure 6.

In addition to the three terminal TOPSwitch features, such as the high-voltage start-up, the cycle-by-cycle current limiting, loop compensation circuitry, auto-restart and thermal shut-down, the TOP264-271 incorporates many additional functions that reduce system cost, increase power supply performance and design flexibility. A patented high-voltage CMOS technology allows both the high-voltage power MOSFET and all the low voltage control circuitry to be cost effectively integrated onto a single monolithic chip.

Three terminals, FREQUENCY, VOLTAGE-MONITOR, and EXTERNAL CURRENT LIMIT have been used to implement some of the new functions. These terminals can be connected to the SOURCE pin to operate the TOP264-271 in a TOPSwitch-like three terminal mode. However, even in this three terminal mode, the TOP264-271 offers many transparent features that do not require any external components:

1. A fully integrated 17 ms soft-start significantly reduces or eliminates output overshoot in most applications by sweeping both current limit and frequency from low to high to limit the peak currents and voltages during start-up.
2. A maximum duty cycle (DC_{MAX}) of 78% allows smaller input storage capacitor, lower input voltage requirement and/or higher power capability.
3. Multi-mode operation optimizes and improves the power supply efficiency over the entire load range while maintaining good cross regulation in multi-output supplies.
4. Switching frequency of 132 kHz reduces the transformer size with no noticeable impact on EMI.
5. Frequency jittering reduces EMI in the full frequency mode at high-load condition.

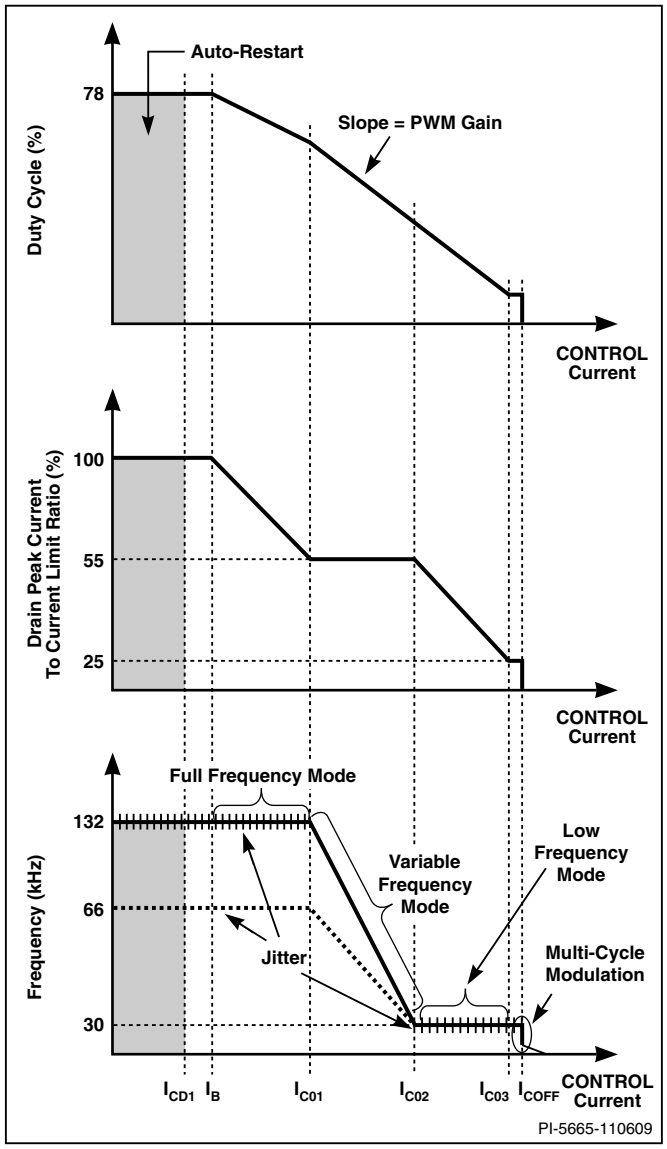


Figure 6. Control Pin Characteristics (Multi-Mode Operation).

6. Hysteretic over-temperature shutdown ensures thermal fault protection.
7. Packages with omitted pins and lead forming provide large drain creepage distance.
8. Reduction of the auto-restart duty cycle and frequency to improve the protection of the power supply and load during open-loop fault, short-circuit, or loss of regulation.
9. Tighter tolerances on I^2f power coefficient, current limit reduction, PWM gain and thermal shutdown threshold.

The VOLTAGE-MONITOR (V) pin is usually used for line sensing by connecting a 4 MΩ resistor from this pin to the rectified DC high-voltage bus to implement line overvoltage (OV), under-voltage (UV) and dual-slope line feed-forward with DC_{MAX} reduction. In this mode, the value of the resistor determines the OV/UV thresholds and the DC_{MAX} is reduced linearly with a dual slope to improve line ripple rejection. In addition, it also provides another threshold to implement the latched and

hysteretic output overvoltage protection (OVP). The pin can also be used as a remote-ON/OFF using the I_{UV} threshold.

The EXTERNAL CURRENT LIMIT (X) pin can be used to reduce the current limit externally to a value close to the operating peak current, by connecting the pin to SOURCE through a resistor. This pin can also be used as a remote-ON/OFF input.

The FREQUENCY (F) pin sets the switching frequency in the full frequency PWM mode to the default value of 132 kHz when connected to SOURCE pin. A half frequency option of 66 kHz can be chosen by connecting this pin to the CONTROL pin instead. Leaving this pin open is not recommended.

CONTROL (C) Pin Operation

The CONTROL pin is a low impedance node that is capable of receiving a combined supply and feedback current. During normal operation, a shunt regulator is used to separate the feedback signal from the supply current. CONTROL pin voltage V_C is the supply voltage for the control circuitry including the MOSFET gate driver. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the instantaneous gate drive current. The total amount of capacitance connected to this pin also sets the auto-restart timing as well as control loop compensation. When rectified DC high-voltage is applied to the DRAIN pin during start-up, the MOSFET is initially off, and the CONTROL pin capacitor is charged through a switched high-voltage current source connected internally between the DRAIN and CONTROL pins. When the CONTROL pin voltage V_C reaches approximately 5.8 V, the control circuitry is activated and the soft-start begins. The soft-start circuit gradually increases the drain peak current and switching frequency from a low starting value to the maximum drain peak current at the full frequency over approximately 17 ms. If no external feedback/supply current is fed into the CONTROL pin by the end of the soft-start, the high-voltage current source is turned off and the CONTROL pin will start discharging in response to the supply current drawn by the control circuitry. If the power supply is designed properly, and no fault condition such as open-loop or shorted output exists, the feedback loop will close, providing external CONTROL pin current, before the CONTROL pin voltage has had a chance to discharge to the lower threshold voltage of approximately 4.8 V (internal supply undervoltage lockout threshold). When the externally fed current charges the CONTROL pin to the shunt regulator voltage of 5.8 V, current in excess of the consumption of the chip is shunted to SOURCE through an NMOS current mirror as shown in Figure 3. The output current of that NMOS current mirror controls the duty cycle of the power MOSFET to provide closed loop regulation. The shunt regulator has a finite low output impedance Z_C that sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance Z_C of the CONTROL pin together with the external CONTROL pin capacitance sets the dominant pole for the control loop.

When a fault condition such as an open-loop or shorted output prevents the flow of an external current into the CONTROL pin, the capacitor on the CONTROL pin discharges towards 4.8 V. At 4.8 V, auto-restart is activated, which turns the output MOSFET off and puts the control circuitry in a low current standby mode. The high-voltage current source turns on and charges the external capacitance again. A hysteretic internal supply undervoltage comparator keeps V_C within a window of typically 4.8 V to 5.8 V by turning the high-voltage current source on and off as shown in Figure 8. The auto-restart circuit has a divide-by-sixteen counter, which prevents the output MOSFET from turning on again until sixteen discharge/charge cycles have elapsed. This is accomplished by enabling the output MOSFET only when the divide-by-sixteen counter reaches the full count (S15). The counter effectively limits TOP264-271 power dissipation by reducing the auto-restart duty cycle to typically 2%. Auto-restart mode continues until output voltage regulation is again achieved through closure of the feedback loop.

Oscillator and Switching Frequency

The internal oscillator linearly charges and discharges an internal capacitance between two voltage levels to create a triangular waveform for the timing of the pulse width modulator. This oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle.

The nominal full switching frequency of 132 kHz was chosen to minimize transformer size while keeping the fundamental EMI frequency below 150 kHz. The FREQUENCY pin, when shorted to the CONTROL pin, lowers the full switching frequency to 66 kHz (half frequency), which may be preferable in some cases such as noise sensitive video applications or a high efficiency standby mode. Otherwise, the FREQUENCY pin should be connected to the SOURCE pin for the default 132 kHz.

To further reduce the EMI level, the switching frequency in the full frequency PWM mode is jittered (frequency modulated) by approximately ±2.5 kHz for 66 kHz operation or ±5 kHz for 132 kHz operation at a 250 Hz (typical) rate as shown in Figure 7. The jitter is turned off gradually as the system is entering the variable frequency mode with a fixed peak drain current.

Pulse Width Modulator

The pulse width modulator implements multi-mode control by driving the output MOSFET with a duty cycle inversely proportional to the current into the CONTROL pin that is in excess of the internal supply current of the chip (see Figure 6). The feedback error signal, in the form of the excess current, is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise in the chip supply current generated by the MOSFET gate driver.

To optimize power supply efficiency, four different control modes are implemented. At maximum load, the modulator operates in full frequency PWM mode; as load decreases, the modulator automatically transitions, first to variable frequency PWM mode, then to low frequency PWM mode. At light load, the control operation switches from PWM control to multi-cycle-modulation control, and the modulator operates in multi-cycle-modulation mode. Although different modes operate differently to make transitions between modes smooth, the simple relationship between duty cycle and excess CONTROL pin current shown in Figure 6 is maintained through all three PWM

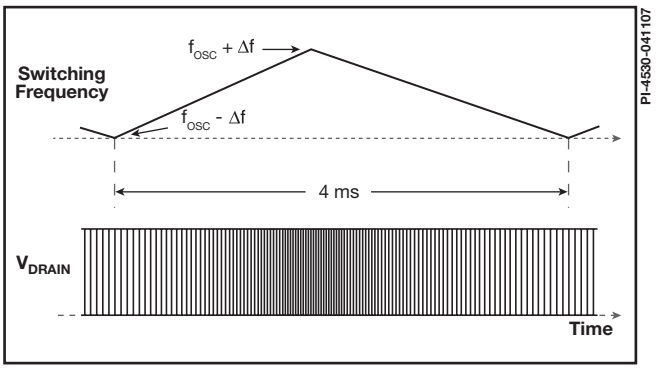


Figure 7. Switching Frequency Jitter (Idealized V_{DRAIN} Waveforms).

modes. Please see the following sections for the details of the operation of each mode and the transitions between modes.

Full Frequency PWM mode: The PWM modulator enters full frequency PWM mode when the CONTROL pin current (I_C) reaches I_B. In this mode, the average switching frequency is kept constant at f_{OSC} (pin selectable 132 kHz or 66 kHz). Duty cycle is reduced from DC_{MAX} through the reduction of the on-time when I_C is increased beyond I_B. This operation is identical to the PWM control of all other TOPSwitch families. TOP264-271 only operates in this mode if the cycle-by-cycle peak drain current stays above $k_{PS(UPPER)} \times I_{LIMIT}$(set), where $k_{PS(UPPER)}$ is 55% (typical) and I_{LIMIT}(set) is the current limit externally set via the EXTERNAL CURRENT LIMIT (X) pin.

Variable Frequency PWM mode: When peak drain current is lowered to $k_{PS(UPPER)} \times I_{LIMIT}$(set) as a result of power supply load reduction, the PWM modulator initiates the transition to variable frequency PWM mode, and gradually turns off frequency jitter. In this mode, peak drain current is held constant at $k_{PS(UPPER)} \times I_{LIMIT}$(set) while switching frequency drops from the initial full frequency of f_{OSC} (132 kHz or 66 kHz) towards the minimum frequency of $f_{MCM(MIN)}$ (30 kHz typical). Duty cycle reduction is accomplished by extending the off-time.

Low Frequency PWM mode: When switching frequency reaches $f_{MCM(MIN)}$ (30 kHz typical), the PWM modulator starts to transition to low frequency mode. In this mode, switching frequency is held constant at $f_{MCM(MIN)}$ and duty cycle is reduced, similar to the full frequency PWM mode, through the reduction of the on-time. Peak drain current decreases from the initial value of $k_{PS(UPPER)} \times I_{LIMIT}$(set) towards the minimum value of $k_{PS(LOWER)} \times I_{LIMIT}$(set), where $k_{PS(LOWER)}$ is 25% (typical) and I_{LIMIT}(set) is the current limit externally set via the X pin.

Multi-Cycle-Modulation mode: When peak drain current is lowered to $k_{PS(LOWER)} \times I_{LIMIT}$(set), the modulator transitions to multi-cycle-modulation mode. In this mode, at each turn-on, the modulator enables output switching for a period of $T_{MCM(MIN)}$ at the switching frequency of $f_{MCM(MIN)}$ (4 or 5 consecutive pulses at 30 kHz) with the peak drain current of $k_{PS(LOWER)} \times I_{LIMIT}$(set), and stays off until the CONTROL pin current falls below $I_{C(OFF)}$. This mode of operation not only keeps peak drain current low but also minimizes harmonic frequencies between 6 kHz and 30 kHz. By avoiding transformer resonant frequency this way, all potential transformer audible noises are greatly suppressed.

Maximum Duty Cycle

The maximum duty cycle, DC_{MAX}, is set at a default maximum value of 78% (typical). However, by connecting the VOLTAGE-MONITOR to the rectified DC high-voltage bus through a resistor with appropriate value (4 MΩ typical), the maximum duty cycle can be made to decrease from 78% to 40% (typical) when input line voltage increases from 88 V to 380 V, with dual gain slopes.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary-side feedback applications. The shunt regulator voltage is accurately derived from a temperature-compensated bandgap reference. The CONTROL pin dynamic impedance Z_C sets the gain of the error amplifier. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and becomes the feedback current I_{FB} for the pulse width modulator.

On-Chip Current Limit with External Programmability

The cycle-by-cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain to source voltage $V_{DS(ON)}$ with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize the variation of the current limit due to temperature related changes in $R_{DS(ON)}$ of the output MOSFET. The default current limit of TOP264-271 is preset internally. However, with a resistor connected between EXTERNAL CURRENT LIMIT (X) pin and SOURCE pin, current limit can be programmed externally to a lower level between 30% and 100% of the default current limit. By setting current limit low, a larger TOP264-271 than necessary for the power required can be used to take advantage of the lower $R_{DS(ON)}$ for higher efficiency/smaller heat sinking requirements. With a second resistor connected between the EXTERNAL CURRENT LIMIT (X) pin and the rectified DC high-voltage bus, the current limit is reduced with increasing line voltage, allowing a true power limiting operation against line variation to be implemented. When using an RCD clamp, this power limiting technique reduces maximum clamp voltage at high-line. This allows for higher reflected voltage designs as well as reducing clamp dissipation.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that, if a power supply is designed properly, current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time should not cause premature termination of the switching pulse. The current limit is lower for a short period after the leading edge blanking time. This is due to dynamic characteristics of the MOSFET. During start-up and fault conditions the controller prevents excessive drain currents by reducing the switching frequency.

Line Undervoltage Detection (UV)

At power-up, UV keeps TOP264-271 off until the input line voltage reaches the undervoltage threshold. At power-down,

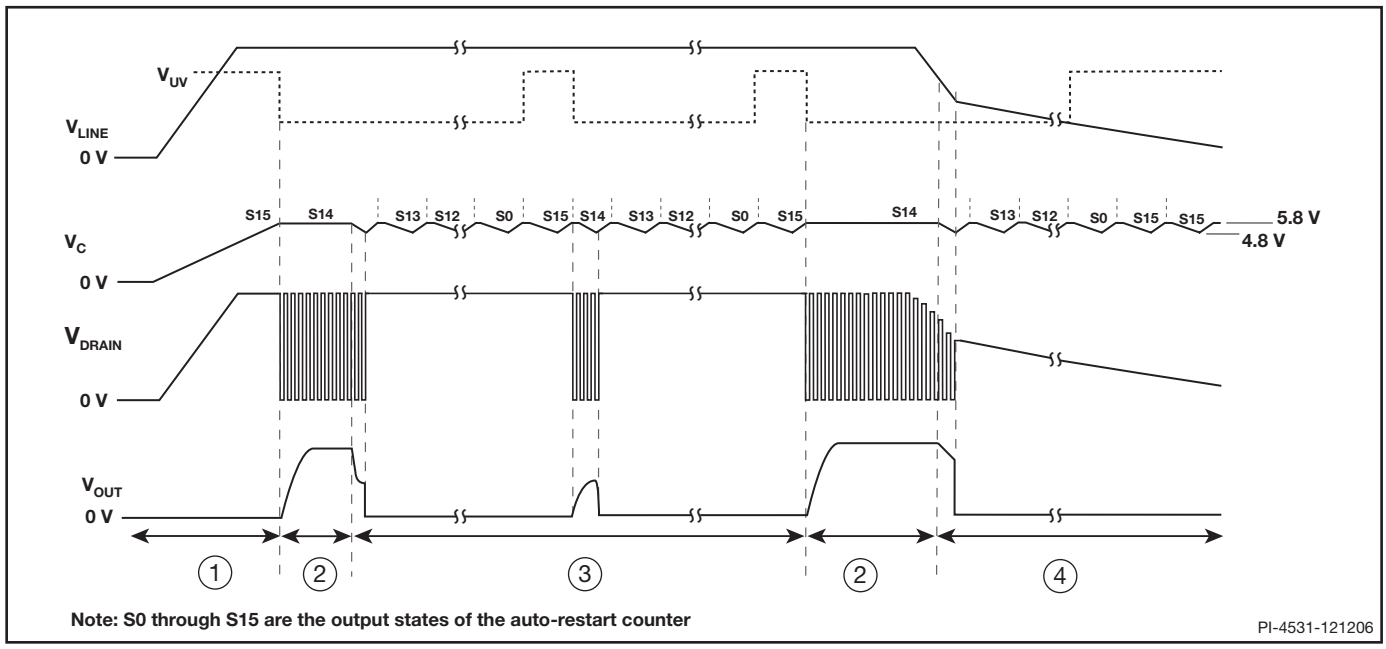


Figure 8. Typical Waveforms for (1) Power-Up (2) Normal Operation (3) Auto-Restart (4) Power-Down.

UV prevents auto-restart attempts after the output goes out of regulation. This eliminates power-down glitches caused by slow discharge of the large input storage capacitor present in applications such as standby supplies. A single resistor connected from the VOLTAGE-MONITOR pin to the rectified DC high-voltage bus sets UV threshold during power-up. Once the power supply is successfully turned on, the UV threshold is lowered to 44% of the initial UV threshold to allow extended input voltage operating range (UV low threshold). If the UV low threshold is reached during operation without the power supply losing regulation, the device will turn off and stay off until UV (high threshold) has been reached again. If the power supply loses regulation before reaching the UV low threshold, the device will enter auto-restart. At the end of each auto-restart cycle (S15), the UV comparator is enabled. If the UV high threshold is not exceeded, the MOSFET will be disabled during the next cycle (see Figure 8). The UV feature can be disabled independent of the OV feature.

Line Overvoltage Shutdown (OV)

The same resistor used for UV also sets an overvoltage threshold, which, once exceeded, will force TOP264-271 to stop switching instantaneously (after completion of the current switching cycle). If this condition lasts for at least 100 µs, the TOP264-271 output will be forced into off state. When the line voltage is back to normal with a small amount of hysteresis provided on the OV threshold to prevent noise triggering, the state machine sets to S13 and forces TOP264-271 to go through the entire auto-restart sequence before attempting to switch again. The ratio of OV and UV thresholds is preset at 4.5, as can be seen in Figure 9. When the MOSFET is off, the rectified DC high-voltage surge capability is increased to the voltage rating of the MOSFET (725 V), due to the absence of the reflected voltage and leakage spikes on the drain. The OV feature can be disabled independent of the UV feature.

In order to reduce the no-load input power of TOP264-271 designs, the V pin operates at very low currents. This requires careful layout considerations when designing the PCB to avoid noise coupling. Traces and components connected to the V pin should not be adjacent to any traces carrying switching currents. These include the drain, clamp network, bias winding return or power traces from other converters. If the line sensing features are used, then the sense resistors must be placed within 10 mm of the V pin to minimize the V pin node area. The DC bus should then be routed to the line-sense resistors. Note that external capacitance must not be connected to the V pin as this may cause misoperation of the V pin related functions.

Hysteretic or Latching Output Overvoltage Protection (OVP)

The detection of the hysteretic or latching output overvoltage protection (OVP) is through the trigger of the line overvoltage threshold. The V pin voltage will drop by 0.5 V, and the controller measures the external attached impedance immediately after this voltage drops. If I_V exceeds $I_{OV(LS)}$ (336 µA typical) longer than 100 µs, TOP264-271 will latch into a permanent off-state for the latching OVP. It only can be reset if I_X exceeds $I_{X(TH)}$ = -27 µA (typ) or V_C goes below the power-up reset threshold ($V_{C(RESET)}$) and then back to normal. If I_V does not exceed $I_{OV(LS)}$ or exceeds no longer than 100 µs, TOP264-271 will initiate the line overvoltage and the hysteretic OVP. Their behavior will be identical to the line overvoltage shutdown (OV) that has been described in detail in the previous section. During a fault condition resulting from loss of feedback, output voltage will rapidly rise above the nominal voltage. The increase in output voltage will also result in an increase in the voltage at the output of the bias winding. A voltage at the output of the bias winding that exceeds of the sum of the voltage rating of the Zener diode connected from the bias winding output to the V pin and V pin voltage, will cause a current in excess of I_V to be injected into the V pin, which will trigger the OVP feature.

If the power supply is operating under heavy load or low input line conditions when an open-loop occurs, the output voltage may not rise significantly. Under these conditions, a latching shutdown will not occur until load or line conditions change. Nevertheless, the operation provides the desired protection by preventing significant rise in the output voltage when the line or load conditions do change. Primary-side OVP protection with the TOP264-271 in a typical application will prevent a nominal 12 V output from rising above approximately 20 V under open-loop conditions. If greater accuracy is required, a secondary sensed OVP circuit is recommended.

Line Feed-Forward with DC_{MAX} Reduction

The same resistor used for UV and OV also implements line voltage feed-forward, which minimizes output line ripple and reduces power supply output sensitivity to line transients. Note that for the same CONTROL pin current, higher line voltage results in smaller operating duty cycle. As an added feature, the maximum duty cycle DC_{MAX} is also reduced from 78% (typical) at a voltage slightly lower than the UV threshold to 36% (typical) at the OV threshold. DC_{MAX} of 36% at high-line was chosen to ensure that the power capability of the TOP264-271 is not restricted by this feature under normal operation. TOP264-271 provides a better fit to the ideal feed-forward by using two reduction slopes: -1% per μA for all bus voltage less than 195 V (typical for 4 MΩ line impedance) and -0.25% per μA for all bus voltage more than 195 V.

Remote-ON/OFF

TOP264-271 can be turned on or off by controlling the current into the VOLTAGE-MONITOR pin or out from the EXTERNAL CURRENT LIMIT pin. In addition, the VOLTAGE-MONITOR pin has a 1 V threshold comparator connected at its input. This voltage threshold can also be used to perform remote-ON/OFF control.

When a signal is received at the VOLTAGE-MONITOR pin or the EXTERNAL CURRENT LIMIT pin to disable the output through any of the pin functions such as OV, UV and remote-ON/OFF, TOP264-271 always completes its current switching cycle before the output is forced off.

As seen above, the remote-ON/OFF feature can also be used as a standby or power switch to turn off the TOP264-271 and keep it in a very low power consumption state for indefinitely long periods. If the TOP264-271 is held in remote-off state for long enough time to allow the CONTROL pin to discharge to the internal supply undervoltage threshold of 4.8 V (approximately 32 ms for a 47 μF CONTROL pin capacitance), the CONTROL pin goes into the hysteretic mode of regulation. In this mode, the CONTROL pin goes through alternate charge and discharge cycles between 4.8 V and 5.8 V (see CONTROL pin operation section above) and runs entirely off the high-voltage DC input, but with very low power consumption (<100 mW typical at 230 VAC with X pin open). When the TOP264-271 is remotely

Voltage Monitor and External Current Limit Pin Table*

Figure Number	13	14	15	16	17	18	19	20	21	22	23	24
Three Terminal Operation	✓											
Line Undervoltage (UV)		✓	✓	✓						✓	✓	
Line Overvoltage (OV)		✓	✓		✓					✓	✓	
Line Feed-Forward (DC_{MAX})		✓	✓							✓	✓	
Output Overvoltage Protection (OVP)			✓									
Overload Power Limiting (OPP)							✓					
External Current Limit						✓	✓		✓	✓	✓	✓
Remote-ON/OFF								✓	✓	✓		
Device Reset								✓	✓	✓		
Fast AC Reset												✓
AC Brown-Out												✓

*This table is only a partial list of many VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT Pin Configurations that are possible.

Table 2. VOLTAGE MONITOR (V) Pin and EXTERNAL CURRENT LIMIT (X) Pin Configuration Options.

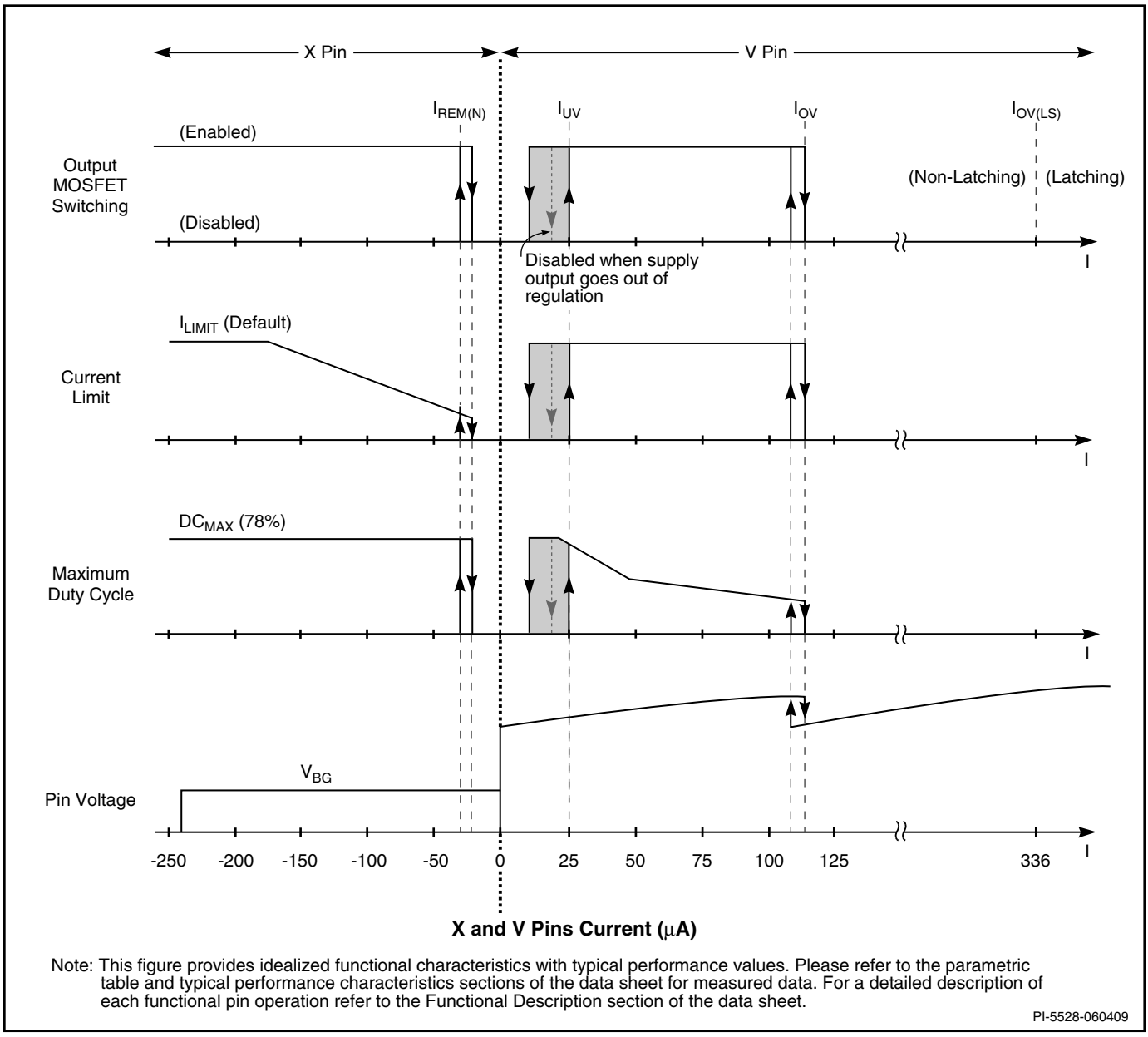


Figure 9. VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT Pin Characteristics.

turned on after entering this mode, it will initiate a normal start-up sequence with soft-start the next time the CONTROL pin reaches 5.8 V. In the worst-case, the delay from remote-on to start-up can be equal to the full discharge/charge cycle time of the CONTROL pin, which is approximately 125 ms for a 47 µF CONTROL pin capacitor. This reduced consumption remote-off mode can eliminate expensive and unreliable in-line mechanical switches. It also allows for microprocessor controlled turn-on and turn-off sequences that may be required in certain applications such as inkjet and laser printers.

Soft-Start

The 17 ms soft-start sweeps the peak drain current and switching frequency linearly from minimum to maximum value by operating through the low frequency PWM mode and the variable frequency mode before entering the full frequency mode. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after being in hysteretic regulation of CONTROL pin voltage (V_C), due to remote-off or thermal shutdown conditions. This effectively minimizes current and voltage stresses on the output MOSFET,

the clamp circuit and the output rectifier during start-up. This feature also helps minimize output overshoot and prevents saturation of the transformer during start-up.

Shutdown/Auto-Restart (for OCP, SCP, OPP)
To minimize TOP264-271 power dissipation under fault conditions such as over current (OC), short-circuit (SC) or over power (OP), the shutdown/auto-restart circuit turns the power supply on and off at an auto-restart duty cycle of typically 2% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode as described in CONTROL pin operation section. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Hysteretic Over-Temperature Protection (OTP)
Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (142 °C typical). When the junction temperature cools to below the lower hysteretic temperature point, normal operation resumes, thus providing automatic recovery. A large hysteresis of 75 °C (typical) is provided to prevent overheating of the PC board due to a continuous fault condition. V_C is regulated in hysteretic mode, and a 4.8 V to 5.8 V (typical) triangular waveform is present on the CONTROL pin while in thermal shutdown.

Bandgap Reference
All critical TOP264-271 internal voltages are derived from a temperature-compensated bandgap reference. This voltage reference is used to generate all other internal current references, which are trimmed to accurately set the switching frequency, MOSFET gate drive current, current limit, and the line OV/UV/OVP thresholds. TOP264-271 has improved circuitry to maintain all of the above critical parameters within very tight absolute and temperature tolerances.

High-Voltage Bias Current Source
This high-voltage current source biases TOP264-271 from the DRAIN pin and charges the CONTROL pin external capacitance during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart, remote-off and over-temperature shutdown. In this mode of operation, the current source is switched on and off, with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching. The effect of the current source switching will be seen on the DRAIN voltage waveform as small disturbances and is normal.

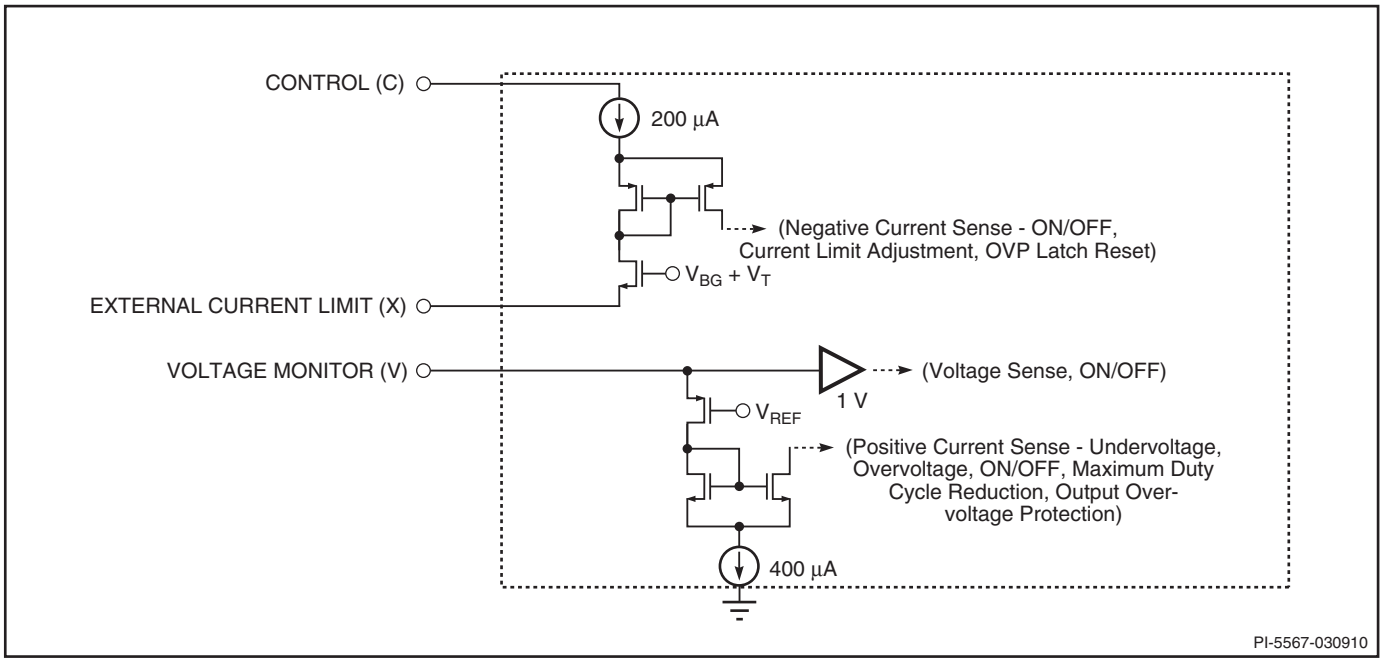


Figure 10. VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) Pin Input Simplified Schematic.

Typical Uses of FREQUENCY (F) Pin

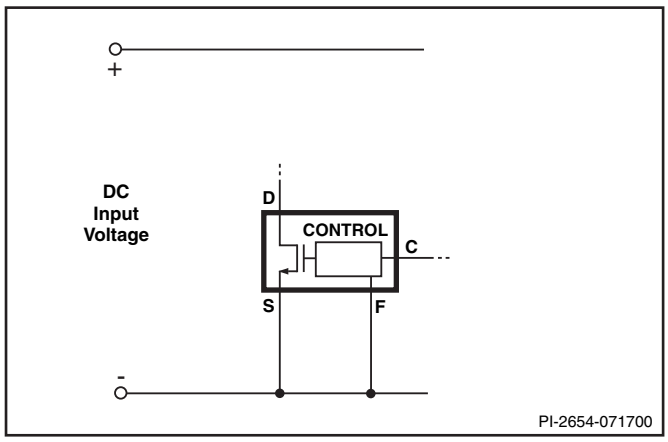


Figure 11. Full Frequency Operation (132 kHz).

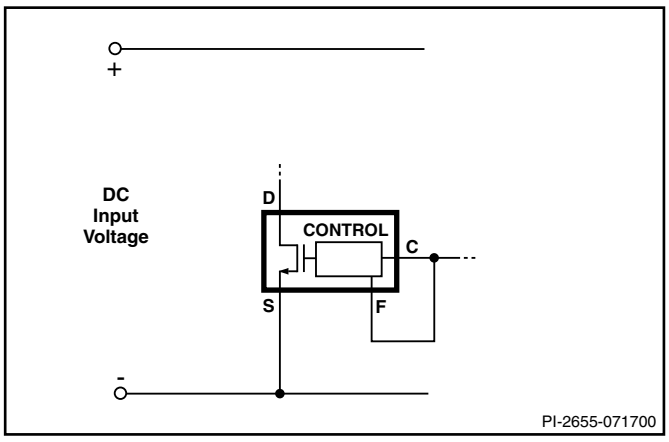


Figure 12. Half Frequency Operation (66 kHz).

Typical Uses of VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) Pins

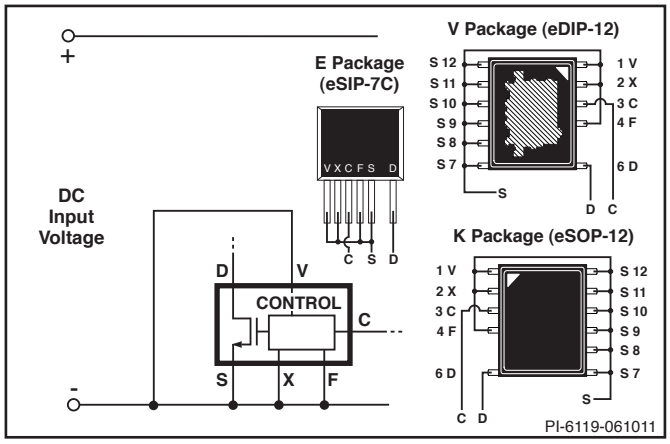


Figure 13. Three Terminal Operation (VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT Features Disabled. FREQUENCY Pin Tied to SOURCE or CONTROL Pin.)

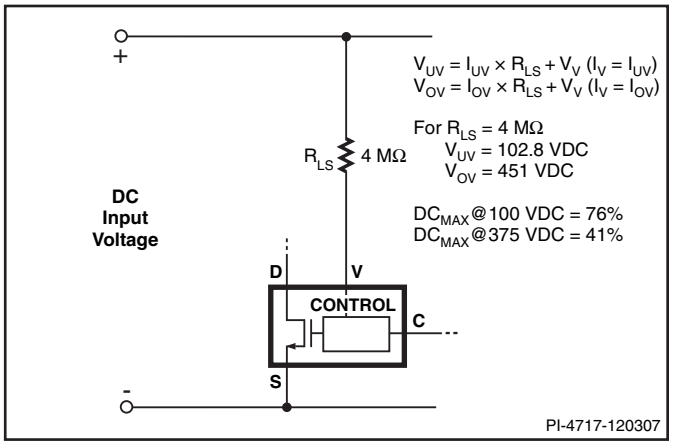


Figure 14. Line-Sensing for Undervoltage, Overvoltage and Line Feed-Forward.

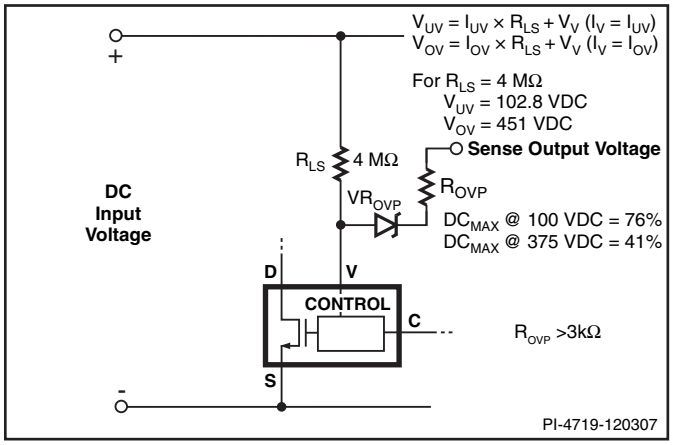


Figure 15. Line-Sensing for Undervoltage, Overvoltage, Line Feed-Forward and Hysteretic Output Overvoltage Protection.

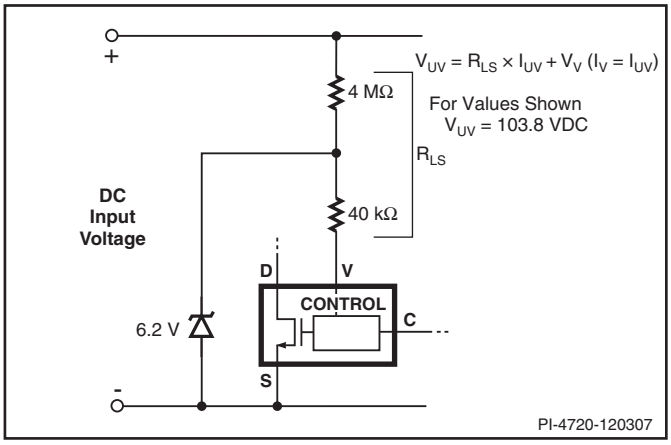


Figure 16. Line-Sensing for Undervoltage Only (Overvoltage Disabled).

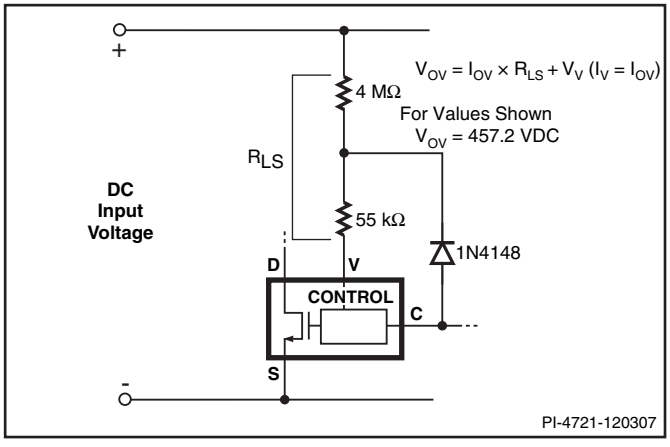


Figure 17. Line-Sensing for Overvoltage Only (Undervoltage Disabled). Maximum Duty Cycle Reduced at Low-Line and Further Reduction with Increasing Line Voltage.

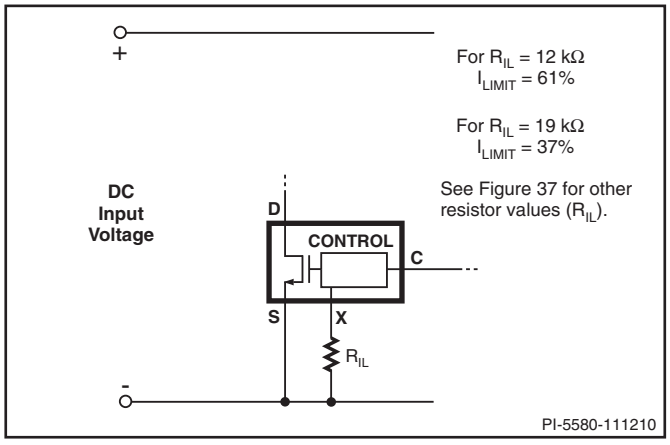


Figure 18. External Set Current Limit.

Typical Uses of VOLTAGE MONITOR (V) and EXTERNAL CURRENT LIMIT (X) Pins (cont.)

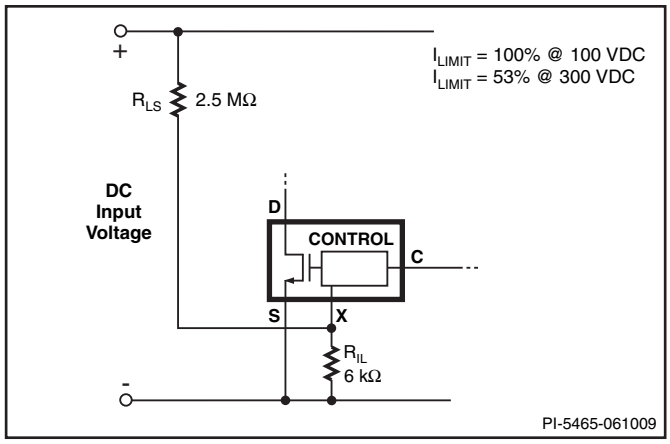


Figure 19. Current Limit Reduction with Line Voltage.

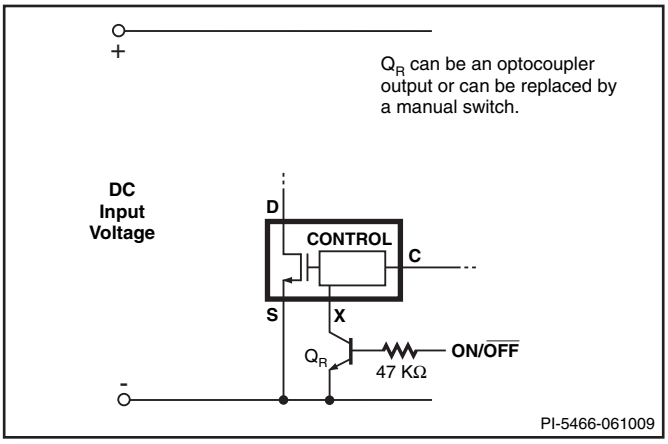


Figure 20. Active-On (Fail Safe) Remote-ON/OFF, and Latch Reset.

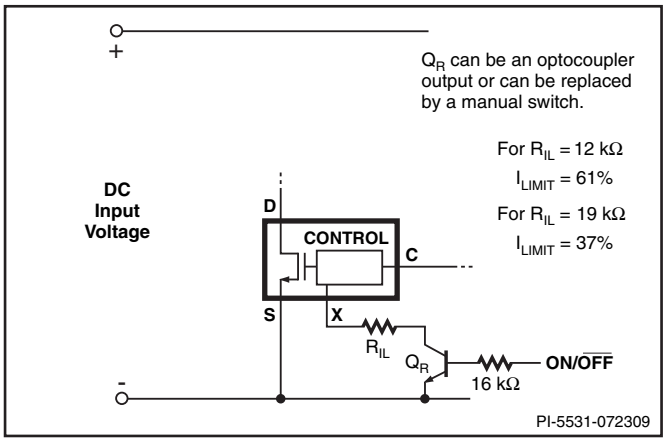


Figure 21. Active-On Remote-ON/OFF with Externally Set Current Limit, and Latch Reset

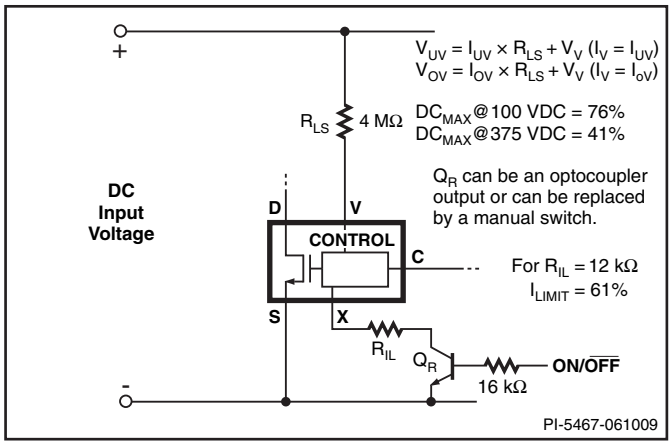


Figure 22. Active-On Remote-ON/OFF with Line-Sense and External Current Limit, and Latch Reset.

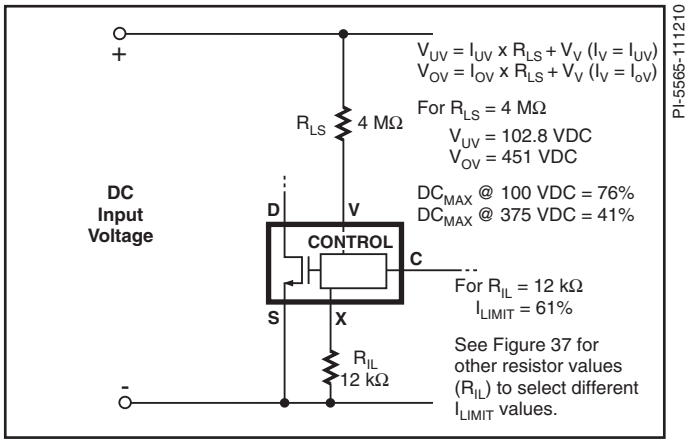


Figure 23. Line Sensing and Externally Set Current Limit.

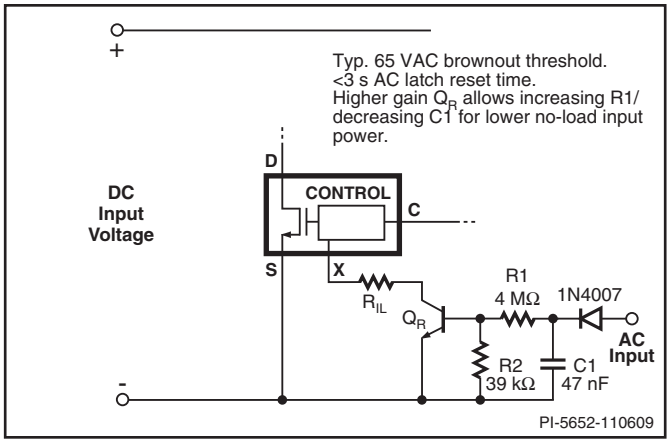


Figure 24. Externally Set Current Limit, Fast AC Latch Reset and Brown-Out.

Application Example

Low No-Load, High Efficiency, 65 W, Universal Input Adapter Power Supply

The circuit shown in Figure 25 shows a 90 VAC to 265 VAC input, 19 V, 3.42 A output power supply, designed for operation inside a sealed adapter case type. The goals of the design were highest full load efficiency, highest average efficiency (average of 25%, 50%, 75% and 100% load points), and very low no-load consumption. Additional requirements included latching output overvoltage shutdown and compliance to safety agency limited power source (LPS) limits. Measured efficiency and no-load performance is summarized in the table shown in the schematic which easily exceed current energy efficiency requirements.

In order to meet these design goals the following key design decisions were made.

PI Part Selection

- One device size larger selected than required for power delivery to increase efficiency

The current limit programming feature of TOPSwitch-JX allows the selection of a larger device than needed for power delivery. This gives higher full load, low-line efficiency by reducing the MOSFET conduction losses ($I_{RMS}^2 \times R_{DS(ON)}$) but maintains the overload power, transformer and other components size as if a smaller device had been used.

For this design one device size larger than required for power delivery (as recommended by the power table) was selected. This typically gives the highest efficiency. Further increases in device size often results in the same or lower efficiency due to the larger switching losses associated with a larger MOSFET.

Line-Sense Resistor Values

- Increasing line-sensing resistance from 4 MΩ to 10.2 MΩ to reduce no-load input power dissipation by 16 mW

Line-sensing is provided by resistors R3 and R4 and sets the line undervoltage and overvoltage thresholds. The combined value of these resistors was increased from the standard 4 MΩ to 10.2 MΩ. This reduced the resistor dissipation, and therefore contribution to no-load input power, from ~26 mW to ~10 mW. To compensate the resultant change in the UV (turn-on) threshold resistor R20 was added between the CONTROL and VOLTAGE-MONITOR pins. This adds a DC current equal to ~16 μA into the VOLTAGE MONITOR pin, requiring only 9 μA to be provided via R3 and R4 to reach the VOLTAGE MONITOR pin UV (turn-on) threshold current of 25 μA and setting the UV threshold to 95 VDC.

This technique does effectively disable the line OV feature as the resultant OV threshold is raised from ~450 VDC to ~980 VDC. However in this design there was no impact as the value of input capacitance (C2) was sufficient to allow the design to withstand differential line surges greater than 2 kV without the peak drain voltage reaching the BV_{DSS} rating of U1.

Specific guidelines and detailed calculations for the value of R20 may be found in the TOPSwitch-JX Application Note (AN-47).

Clamp Configuration – RZCD vs RCD

- An RZCD (Zener bleed) was selected over an RCD clamp to give higher light load efficiency and lower no-load consumption

The clamp network is formed by VR2, C4, R5, R6, R11, R28, R29 and D2. It limits the peak drain voltage spike caused by leakage inductance to below the BV_{DSS} rating of the internal

Input Voltage (VAC)	90	115	230
Full Power Efficiency (%)	86.6	88.4	89.1
Average Efficiency (%)		89.8	89.5
No-load Input Power (mW)	57.7	59.7	86.7

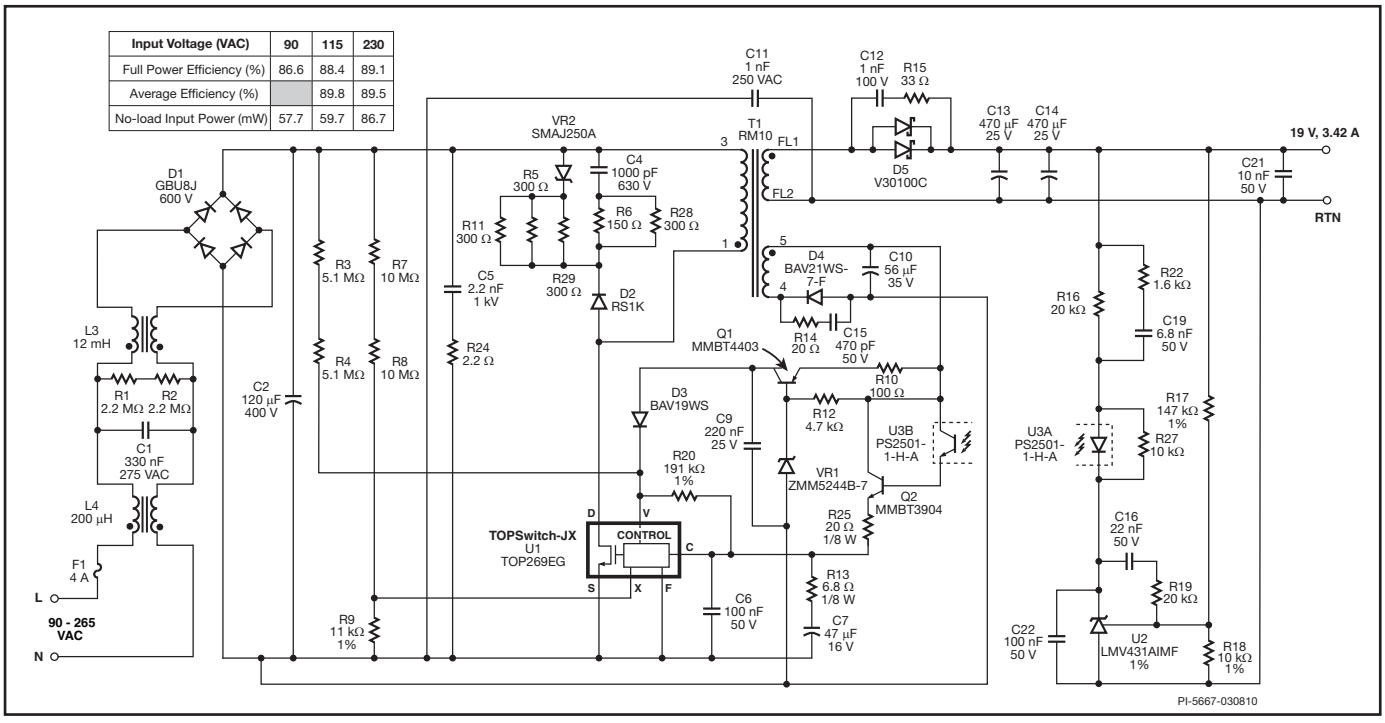


Figure 25. Schematic of High Efficiency 19 V, 65 W, Universal Input Flyback Supply with Low No-load.

TOPSwitch-JX MOSFET. This arrangement was selected over a standard RCD clamp to improve light load efficiency and no-load input power.

In a standard RCD clamp C4 would be discharged by a parallel resistor rather than a resistor and series Zener. In an RCD clamp the resistor value is selected to limit the peak drain voltage under full load and overload conditions. However under light or no-load conditions this resistor value now causes the capacitor voltage to discharge significantly as both the leakage inductance energy and switching frequency are lower. As the capacitor has to be recharged to above the reflected output voltage each switching cycle the lower capacitor voltage represents wasted energy. It has the effect of making the clamp dissipation appear as a significant load just as if it were connected to the output of the power supply.

The RZCD arrangement solves this problem by preventing the voltage across the capacitor discharging below a minimum value (defined by the voltage rating of VR2) and therefore minimizing clamp dissipation under light and no-load conditions.

Resistors R6 and R28 provide damping of high frequency ringing to reduce EMI. Due to the resistance in series with VR2, limiting the peak current, standard power Zeners vs a TVS type may be used for lower cost (although a TVS type was selected due to availability of a SMD version). Diode D2 was selected to have an 800 V vs the typical 600 V rating due to its longer reverse recovery time of 500 ns. This allows some recovery of the clamp energy during the reverse recovery time of the diode improving efficiency. Multiple resistors were used in parallel to share dissipation as SMD components were used.

Feedback Configuration

- A Darlington connection formed together with optocoupler transistor to reduce secondary-side feedback current and therefore no-load input power.
- Low voltage, low current voltage reference IC used on secondary-side to reduce secondary-side feedback current and therefore no-load input power.
- Bias winding voltage tuned to ~9 V at no-load, high-line to reduce no-load input power.

Typically the feedback current into the CONTROL pin at high-line is ~3 mA. This current is both sourced from the bias winding (voltage across C10) and directly from the output. Both of these represent a load on the output of the power supply.

To minimize the dissipation from the bias winding under no-load conditions the number of bias winding turns and value of C10 was adjusted to give a minimum voltage across C10 of ~9 V. This is the minimum required to keep the optocoupler biased. To minimize the dissipation of the secondary-side feedback circuit Q2 was added to form a Darlington connection with U3B. This reduced the feedback current on the secondary to ~1 mA. The increased loop gain (due to the h_{FE} of the transistor) was compensated by increasing the value of R16 and the addition of R25. A standard 2.5 V TL431 voltage reference was replaced with the 1.24 V LMV431 to reduce the supply current requirement from 1 mA to 100 μA.

Output Rectifier Choice

- Higher current rating, low V_F Schottky rectifier diode selected for output rectifier.

A dual 15 A, 100 V Schottky rectifier diode with a V_F of 0.455 V at 5 A was selected for D5. This is a higher current rating than required to reduce resistive and forward voltage losses to improve both full load and average efficiency. The use of a 100 V Schottky was possible due to the high transformer primary to secondary turns ratio (V_{OR} = 110 V) which was in turn possible due to the high-voltage rating of the TOPSwitch-JX internal MOSFET.

Increased Output Overvoltage Shutdown Sensitivity

- Transistor Q1 and VR1 added to improve the output over-voltage shutdown sensitivity.

During an open-loop condition the output and therefore bias winding voltage will rise. When this exceeds the voltage of VR1 plus a V_{BE} voltage drop Q1 turns on and current is fed into the VOLTAGE MONITOR pin. The addition of Q1 ensures that the current into the VOLTAGE MONITOR pin is sufficient to exceed the latching shutdown threshold even when the output is fully loaded while the supply is operating at low-line as under this condition the output voltage overshoot is relatively small

Output overload power limitation is provided via the current limit programming feature of the X pin and R7, R8 and R9. Resistors R8 and R9 reduce the device current limit as a function of increasing line voltage to provide a roughly flat overload power characteristic, below the 100 VA limited power source (LPS) requirement. In order to still meet this under a single fault condition (such as open circuit of R8) the rise in the bias voltage that occurs during an overload condition is also used to trigger a latching shutdown.

Very Low No-Load, High Efficiency, 30 W, Universal Input, Open Frame, Power Supply

The circuit shown in Figure 26 below shows an 85 VAC to 265 VAC input, 12 V, 2.5 A output power supply. The goals of the design were highest full load efficiency, average efficiency (average of 25%, 50%, 75% and 100% load points), very low no-load consumption. Additional requirements included latching output overvoltage shutdown and compliance to safety agency limited power source (LPS) limits. Actual efficiency and no-load performance is summarized in the table shown in the schematic which easily exceed current energy efficiency requirements.

In order to meet these design goals the following key design decisions were made.

PI Part Selection

- Ambient of 40 °C allowed one device size smaller than indicated by the power table

The device selected for this design was based on the 85-265 VAC, Open Frame, PCB heat sinking column of power table (Table 1). One device size smaller was selected (TOP266V vs TOP267V) due to the ambient specification of 40 °C (vs the 50°C assumed in the power table) and the optimum PCB area and layout for the device heat sink. The subsequent thermal and efficiency data confirmed this choice. The maximum device temperature was 107 °C at full load, 40 °C, 85 VAC, 47 Hz (worst-case conditions) and average efficiency exceeded 83% ENERGY STAR and EuP Tier 2 requirements.

Transformer Core Selection

- 132 kHz switching frequency allowed the selection of smaller core for lower cost.

The size of the magnetic core is a function of the switching frequency. The choice of the higher switching frequency of 132 kHz allowed for the use of a smaller core size. The higher switching frequency does not negatively impact the efficiency in TOPSwitch-JX designs due its small drain to source capacitance (C_{OSS}) as compared to that of discrete MOSFETs.

Line-Sense Resistor Values

- Increasing line-sensing resistance from 4 MΩ to 10.2 MΩ to reduce no-load input power dissipation by 16 mW.

Line-sensing is provided by resistors R1 and R2 and sets the line undervoltage and overvoltage thresholds. The combined value of these resistors was increased from the standard 4 MΩ to 10.2 MΩ. This reduces the current into the VOLTAGE MONITOR pin, and therefore contribution to no-load input power, from ~26 mW to ~10 mW. To compensate the resultant change in the UV threshold resistor R12 was added between the CONTROL and VOLTAGE-MONITOR pins. This adds a DC current equal to ~16 µA into the VOLTAGE MONITOR pin, requiring only 9 µA to be provided via R1 and R2 to reach the VOLTAGE MONITOR pin UV threshold current of 25 µA and setting the UV threshold to approximately 95 VDC.

This technique does effectively disable the line OV feature as the resultant OV threshold is raised from ~450 VDC to ~980 VDC. However in this design there was no impact as the value of input capacitance (C3) was sufficient to allow the design to withstand differential line surges greater than 1 kV without the peak drain voltage reaching the BV_{DSS} rating of U1.

Specific guidelines and detailed calculations for the value of R12 may be found in the TOPSwitch-JX Application Note.

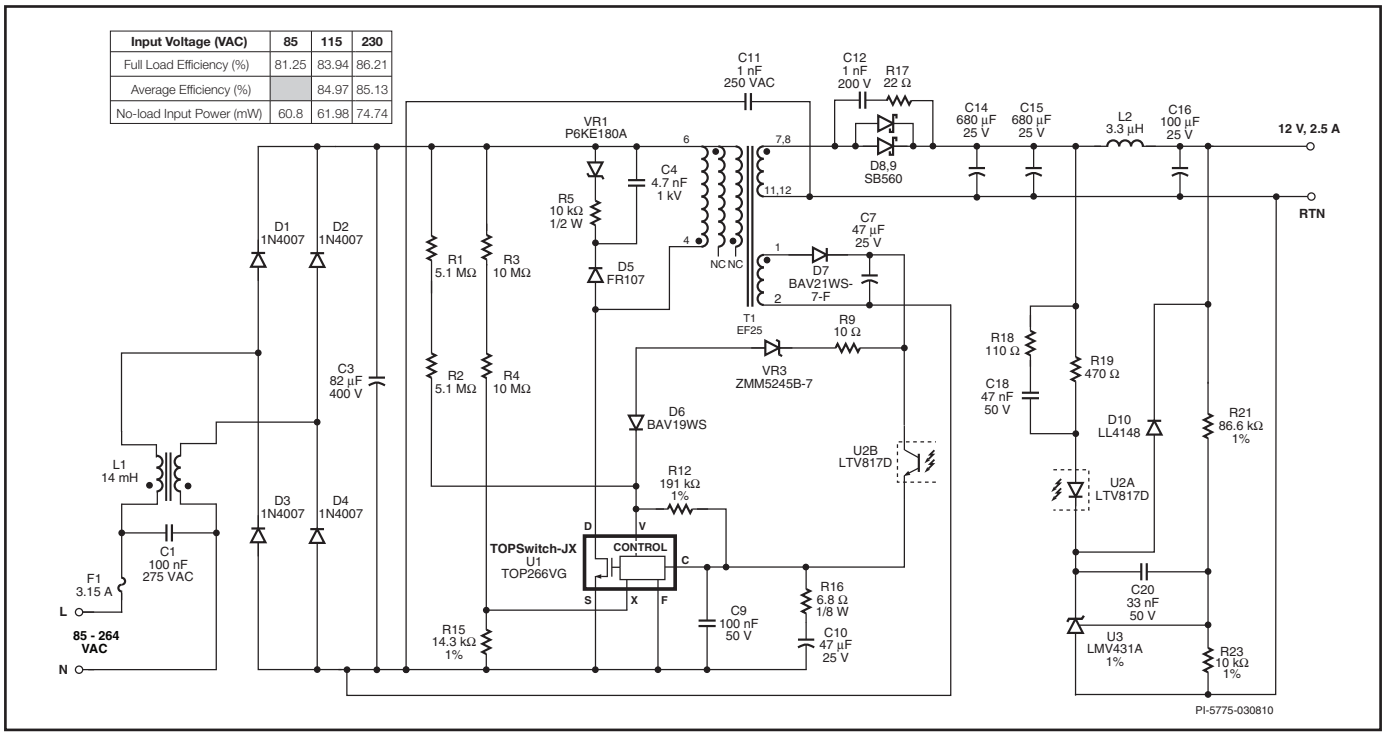


Figure 26. Schematic of High Efficiency 12 V, 30 W, Universal Input Flyback Supply with Very Low No-load.

Clamp Configuration – RZCD vs RCD

- An RZCD (Zener bleed) was selected over RCD to give higher light load efficiency and lower no-load consumption.

The clamp network is formed by VR1, C4, R5 and D5. It limits the peak drain voltage spike caused by leakage inductance to below the BV_{DSS} rating of the internal TOPSwitch-JX MOSFET. This arrangement was selected over a standard RCD clamp to improve light load efficiency and no-load input power.

In a standard RCD clamp C4 would be discharged by a parallel resistor rather than a resistor and series Zener. In an RCD clamp the resistor value of R5 is selected to limit the peak drain voltage under full load and overload conditions. However under light or no-load conditions this resistor value now causes the capacitor voltage to discharge significantly as both the leakage inductance energy and switching frequency are lower. As the capacitor has to be recharged to above the reflected output voltage each switching cycle the lower capacitor voltage represents wasted energy. It has the effect of making the clamp dissipation appear as a significant load just as if it were connected to the output of the power supply.

The RZCD arrangement solves this problem by preventing the voltage across the capacitor discharging below a minimum value (defined by the voltage rating of VR1) and therefore minimizing clamp dissipation under light and no-load conditions. Zener VR1 is shown as a high peak dissipation capable TVS however a standard lower cost Zener may also be used due to the low peak current that component experiences.

In many designs a resistor value of less than 50 Ω may be used in series with C4 to damp out high frequency ringing and improve EMI but this was not necessary in this case.

Feedback Configuration

- A high CTR optocoupler was used to reduce secondary bias currents and no-load input power.
- Low voltage, low current voltage reference IC used on secondary-side to reduce secondary-side feedback current and no-load input power.
- Bias winding voltage tuned to ~9 V at no-load, high-line to reduce no-load input power.

Typically the feedback current into the CONTROL pin at high-line is ~3 mA. This current is both sourced from the bias winding (voltage across C10) and directly from the output. Both of these represent a load on the output of the power supply.

To minimize the dissipation from the bias winding under no-load conditions the number of bias winding turns and value of C7 was adjusted to give a minimum voltage across C7 of ~9 V. This is the minimum required to keep the optocoupler biased and the output in regulation.

To minimize the dissipation of the secondary-side feedback circuit a high CTR (CTR of 300 – 600%) optocoupler type was used. This reduces the secondary-side opto-led current from ~3 mA to <~1 mA and therefore the effective load on the output. A standard 2.5 V TL431 voltage reference was replaced with the 1.24 V LMV431 to reduce the supply current requirement of this component from 1 mA to 100 μA.

Output Rectifier Choice

- Use of high V_{OR} allows the use of a 60 V Schottky diode for high efficiency and lower cost.

The higher BV_{DSS} rating of the TOPSwitch-JX of 725 V (compared to 600 V or 650 V rating of typical power MOSFETs) allowed a higher transformer primary to secondary turns ratio (reflected output voltage or V_{OR}). This reduced the output diode voltage stress and allowed the use of cheaper and more efficient 60 V (vs 80 V or 100 V) Schottky diodes. The efficiency improvement occurs due the lower forward voltage drop of the lower voltage diodes. Two parallel connected axial 5 A, 60 V Schottky rectifier diodes were selected for both low-cost and high efficiency. This allowed PCB heat sinking of the diode for low cost while maintaining efficiency compared to a single higher current TO-220 packaged diode mounted on a heat sink. For this configuration the recommendation is that each diode is rated at twice the output current and that the diodes share a common cathode PCB area for heat sinking so that their temperatures track. In practice the diodes current share quite effectively as can be demonstrated by monitoring their individual temperatures.

Output Inductor Post Filter Soft-Finish

- Inductor L2 used to provide an output soft-finish and eliminate a capacitor.

To prevent output overshoot during start-up the voltage appearing across L2 is used to provide a soft-finish function. When the voltage across L2 exceeds the forward drop of U2A and D10 current flows though the optocoupler LED and provides feedback to the primary. This arrangement acts to limit the rate of rise of the output voltage until it reaches regulation and eliminates the capacitor that is typically placed across U3 to provide the same function.

Key Application Considerations

TOPSwitch-JX vs. TOPSwitch-HX

Table 3 compares the features and performance differences between TOPSwitch-JX and TOPSwitch-HX. Many of the new features eliminate the need for additional discrete components. Other features increase the robustness of design, allowing cost savings in the transformer and other power components.

TOP264-271 Design Considerations

Power Table

The data sheet power table (Table 1) represents the maximum practical continuous output power based on the following conditions:

1. 12 V output.
2. Schottky or high efficiency output diode.
3. 135 V reflected voltage (V_{OR}) and efficiency estimates.
4. A 100 VDC minimum DC bus for 85-265 VAC and 250 VDC minimum for 230 VAC.
5. Sufficient heat sinking to keep device temperature ≤110 °C.

TOPSwitch-HX vs. TOPSwitch-JX

Function	TOPSwitch-HX	TOPSwitch-JX	TOPSwitch-JX Advantages
CONTROL current $I_{C(OFF)}$ at 0% duty cycle	$I_{C(OFF)} = I_B + 3.4$ mA (TOP256-258) I_B = External bias current	$I_{C(OFF)} = I_B + 1.6$ mA (TOP266-268)	• Reduced CONTROL current • Better no-load performance (<0.1 W) • Better standby performance
eDIP-12 / eSOP-12 packages	Not available	Available	• 66/132 kHz frequency option for DIP style heat sink less designs • Better thermal performance for increased power capability over DIP-8 / SMD-8 packages
Breakdown voltage BV_{DSS}	Min. 700 V at T_J = 25 °C	Min. 725 V at T_J = 25 °C	• Simplifies meeting customer derating requirements (e.g. 80%) • Extended line surge withstand
Fast AC reset	3 external transistor circuits using the V pin	1 external transistor circuit using the X pin	• Saves 5 components

Table 3. Comparison Between TOPSwitch-HX and TOPSwitch-JX.

6. Power levels shown in the power table for the V package device assume 6.45 cm^2 of 610 g/m^2 copper heat sink area in an enclosed adapter, or 19.4 cm^2 in an open frame.

The provided peak power depends on the current limit for the respective device.

TOP264-271 Selection

Selecting the optimum TOP264-271 depends upon required maximum output power, efficiency, heat sinking constraints, system requirements and cost goals. With the option to externally reduce current limit, TOP264-271 may be used for lower power applications where higher efficiency is needed or minimal heat sinking is available.

Input Capacitor

The input capacitor must be chosen to provide the minimum DC voltage required for the TOP264-271 converter to maintain regulation at the lowest specified input voltage and maximum output power. Since TOP264-271 has a high DC_{MAX} limit and an optimized dual slope line feed forward for ripple rejection, it is possible to use a smaller input capacitor. For TOP264-271, a capacitance of 2 µF per watt is possible for universal input with an appropriately designed transformer.

Primary Clamp and Output Reflected Voltage V_{OR}

A primary clamp is necessary to limit the peak TOP264-271 drain to source voltage. A Zener clamp requires few parts and takes up little board space. For good efficiency, the clamp Zener should be selected to be at least 1.5 times the output reflected voltage V_{OR}, as this keeps the leakage spike conduction time short. When using a Zener clamp in a universal input application, a V_{OR} of less than 135 V is recommended to allow for the absolute tolerances and temperature variations of the Zener. This will ensure efficient operation of the clamp circuit and will also keep the maximum drain voltage below the rated breakdown voltage of the TOP264-271 MOSFET. A high V_{OR} is required to take full advantage of the wider DC_{MAX} of TOP264-271. An RCD (or RCDZ) clamp provides tighter clamp voltage tolerance than a Zener clamp and allows a V_{OR} as high as 150 V. RCD clamp dissipation can be minimized by reducing the external current limit as a function of input line voltage (see Figure 19). The RCD clamp is more cost effective than the Zener clamp but requires more careful design (see Quick Design Checklist).

Output Diode

The output diode is selected for peak inverse voltage, output current, and thermal conditions in the application (including heat sinking, air circulation, etc.). The higher DC_{MAX} of TOP264-271, along with an appropriate transformer turns ratio, can allow the use of a 80 V Schottky diode for higher efficiency on output voltages as high as 15 V.

Bias Winding Capacitor

Due to the low frequency operation at no-load, a bias winding capacitance of 10 µF minimum is recommended. Ensure a minimum bias winding voltage of >9 V at zero load for correct operation and output voltage regulation.

Soft-Start

Generally, a power supply experiences maximum stress at start-up before the feedback loop achieves regulation. For a period of 17 ms, the on-chip soft-start linearly increases the drain peak current and switching frequency from their low starting values to their respective maximum values. This causes the output voltage to rise in an orderly manner, allowing time for the feedback loop to take control of the duty cycle. This reduces the stress on the TOP264-271 MOSFET, clamp circuit and output diode(s), and helps prevent transformer saturation during start-up. Also, soft-start limits the amount of output voltage overshoot and, in many applications, eliminates the need for a soft-finish capacitor. Note that as soon as the loop closes the soft-start function ceases even if this is prior to the end of the 17 ms soft-start period.

EMI

The frequency jitter feature modulates the switching frequency over a narrow band as a means to reduce conducted EMI peaks associated with the harmonics of the fundamental switching frequency. This is particularly beneficial for average detection

mode. As can be seen in Figures 27 and 28, the benefits of jitter increase with the order of the switching harmonic due to an increase in frequency deviation. The FREQUENCY pin offers a switching frequency option of 132 kHz or 66 kHz. In applications that require heavy snubber on the drain node for reducing high frequency radiated noise (for example, video noise sensitive applications such as VCRs, DVDs, monitors, TVs, etc.), operating at 66 kHz will reduce snubber loss, resulting in better efficiency. Also, in applications where transformer size is not a concern, use of the 66 kHz option will provide lower EMI and higher efficiency. Note that the second harmonic of 66 kHz is still below 150 kHz, above which the conducted EMI specifications get much tighter. For 10 W or below, it is possible to use a simple inductor in place of a more costly AC input common mode choke to meet worldwide conducted EMI limits.

Transformer Design

It is recommended that the transformer be designed for maximum operating flux density of 3000 Gauss and a peak flux density of 4200 Gauss at maximum current limit. The turns ratio should be chosen for a reflected voltage (V_{OR}) no greater than 135 V when using a Zener clamp or 150 V (max) when using an RCD clamp with current limit reduction with line voltage (overload protection). For designs where operating current is significantly lower than the default current limit, it is recommended to use an externally set current limit close to the operating peak current to reduce peak flux density and peak power (see Figure 18).

Standby Consumption

Frequency reduction can significantly reduce power loss at light or no-load, especially when a Zener clamp is used. For very low secondary power consumption, use a TL431 regulator for feedback control. A typical TOP264-271 circuit automatically enters MCM mode at no-load and the low frequency mode at light load, which results in extremely low losses under no-load or standby conditions.

High Power Designs

The TOP264-271 family contains parts that can deliver up to 162 W. High power designs need special considerations. Guidance for high power designs can be found in the Design Guide for TOP264-271 (AN-47).

TOP264-271 Layout Considerations

The TOP264-271 has multiple pins and may operate at high power levels. The following guidelines should be carefully followed.

Primary Side Connections

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor. The CONTROL pin bypass capacitor should be located as close as possible to the SOURCE and CONTROL pins, and its SOURCE connection trace should not be shared by the main MOSFET switching currents. All SOURCE pin referenced components connected to the VOLTAGE MONITOR (V) pin or EXTERNAL CURRENT LIMIT (X) pin should also be located closely between their respective pin and SOURCE. Once again, the SOURCE connection trace of these components should not be shared by the main MOSFET switching currents. It is very critical that SOURCE pin switching currents are returned to the input capacitor negative terminal through a separate trace that is not shared by the components connected to CONTROL, VOLTAGE MONITOR or EXTERNAL CURRENT LIMIT pins. This is because the SOURCE pin is also the controller ground reference pin. Any traces to the VOLTAGE MONITOR, EXTERNAL CURRENT LIMIT or CONTROL pins should be kept as short as possible and away from the DRAIN trace to prevent noise coupling. Voltage monitor resistors (R_{LS} in Figures 14, 15, 19, 22, 23, 26, 30) and primary-side OVP circuit components V_{ZOV}/R_{OV} in Figures (29, 30) should be located close to the VOLTAGE MONITOR pin to minimize the trace length on the VOLTAGE MONITOR pin side. Resistors connected to the VOLTAGE MONITOR or EXTERNAL CURRENT LIMIT pin should be connected as close to the bulk capacitor positive terminal as possible while routing these connections away from the power switching circuitry. In addition to the 47 µF CONTROL pin

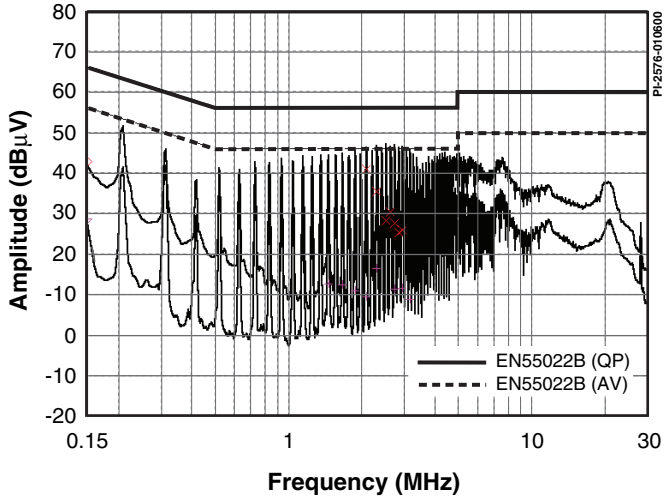


Figure 27. Fixed Frequency Operation without Jitter.

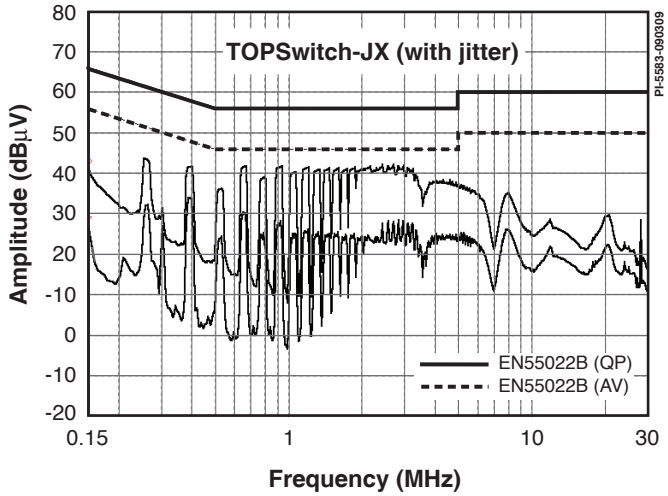


Figure 28. TOPSwitch-JX Full Range EMI Scan (132 kHz with Jitter) with Identical Circuitry and Conditions.

capacitor, a high frequency bypass capacitor (C_{BP}) in parallel should be used for better noise immunity. The feedback optocoupler output should also be located close to the CONTROL and SOURCE pins of TOP264-271 and away from the drain and clamp component traces. The primary-side clamp circuit should be positioned such that the loop area from the transformer end (shared with DRAIN) and the clamp capacitor is minimized. The bias winding return node should be connected via a dedicated trace directly to the bulk capacitor and not to the SOURCE pins. This ensures that surge currents are routed away from the SOURCE pins of the TOPSwitch-JX.

Y Capacitor

The Y capacitor should be connected close to the secondary output return pin(s) and the positive primary DC input pin of the transformer. If the Y capacitor is returned to the negative end of the input bulk capacitor (rather than the positive end) a dedicated trace must be used to make this connection. This is to "steer" leakage currents away from the SOURCE pins in case of a common-mode surge event.

Heat Sinking

The exposed pad of the E package (eSIP-7C), K package (eSOP-12) and the V package (eDIP-12) are internally electrically tied to the SOURCE pin. To avoid circulating currents, a heat sink attached to the exposed pad should not be electrically tied to any primary ground/source nodes on the PC board. On double sided boards, top side and bottom side areas connected with vias can be used to increase the effective heat sinking area. The K package exposed pad may be directly soldered to a copper area for optimum thermal transfer. In addition, sufficient copper area should be provided at the anode and cathode leads of the output diode(s) for heat sinking. In Figure 29, a narrow trace is shown between the output rectifier and output filter capacitor. This trace acts as a thermal relief between the rectifier and filter capacitor to prevent excessive heating of the capacitor.

Quick Design Checklist

In order to reduce the no-load input power of TOP264-271 designs, the VOLTAGE MONITOR pin operates at very low current. This requires careful layout considerations when designing the PCB to avoid noise coupling. Traces and components connected to the VOLTAGE MONITOR pin should not be adjacent to any traces carrying switching currents. These include the drain, clamp network, bias winding return or power traces from other converters. If the line-sensing features are used, then the sense resistors must be placed within 10 mm of the VOLTAGE MONITOR pin to minimize the VOLTAGE MONITOR pin node area. The DC bus should then be routed to the line-sense resistors. Note that external capacitance must not be connected to the VOLTAGE MONITOR pin as this may cause misoperation of the VOLTAGE MONITOR pin related functions. As with any power supply design, all TOP264-271 designs should be verified on the bench to make sure that components specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 675 V at highest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just before the power supply goes into auto-restart (loss of regulation).
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. TOP264-271 has a leading edge blanking time of 220 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit envelope (see Figure 34) for the drain current waveform at the end of the 220 ns blanking period.
3. Thermal check – At maximum output power, both minimum and maximum voltage and ambient temperature; verify that temperature specifications are not exceeded for TOP264-271, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of TOP264-271, as specified in the data sheet. The margin required can either be calculated from the values in the parameter table or it can be accounted for by connecting an external resistance in series with the DRAIN pin and attached to the same heat sink, having a resistance value that is equal to the difference between the measured $R_{DS(ON)}$ of the device under test and the worst-case maximum specification.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com

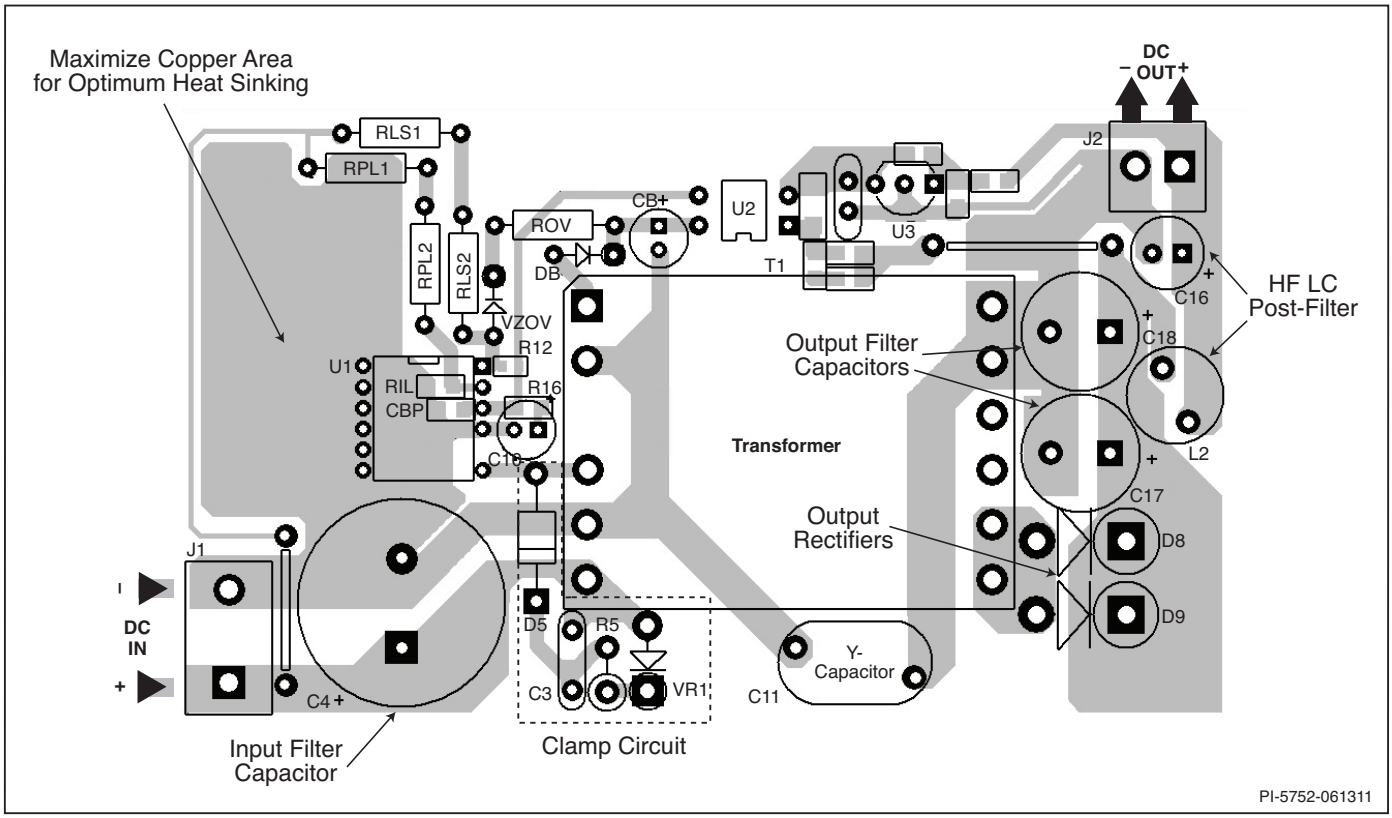


Figure 29. Layout Considerations for TOPSwitch-JX using V Package and Operating at 132 kHz.

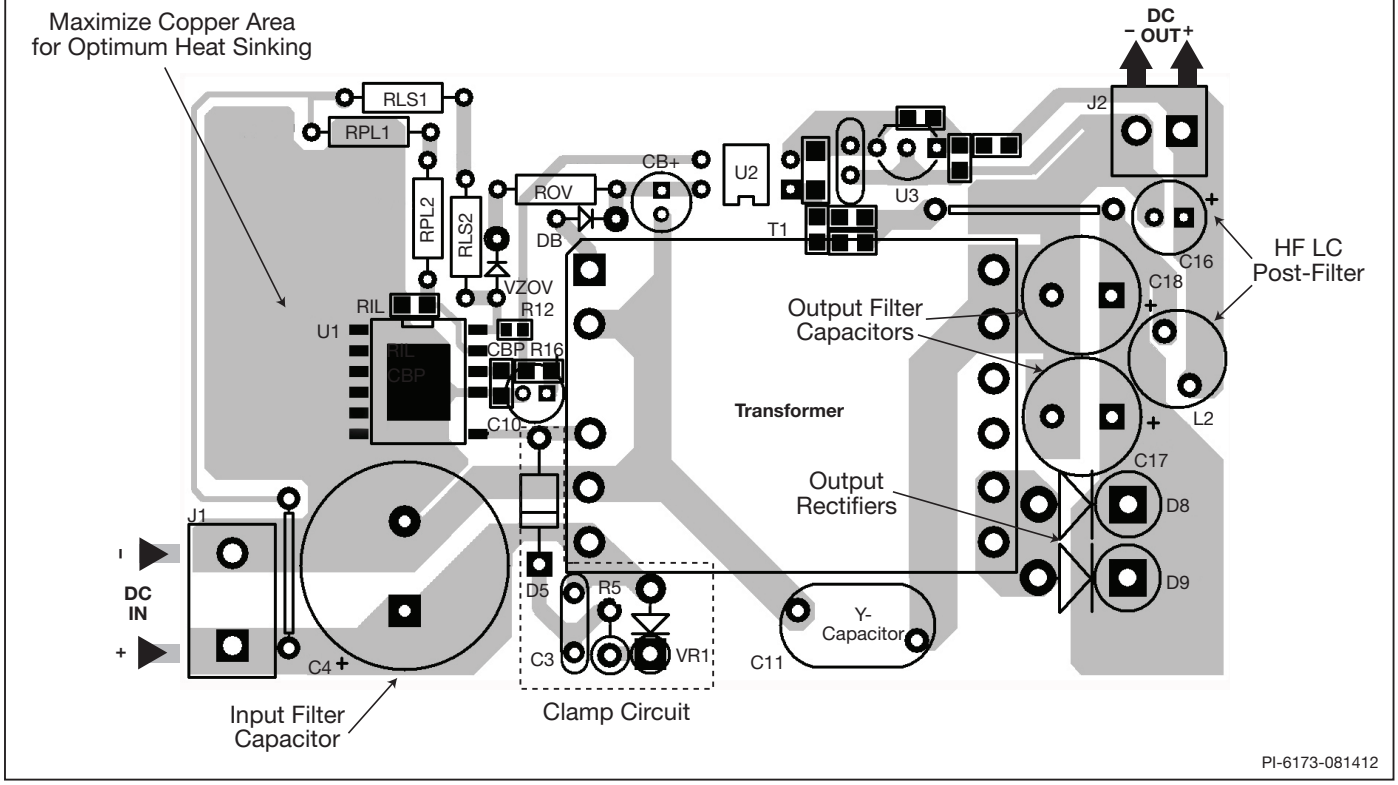


Figure 30. Layout Considerations for TOPSwitch-JX using K Package and Operating at 132 kHz.

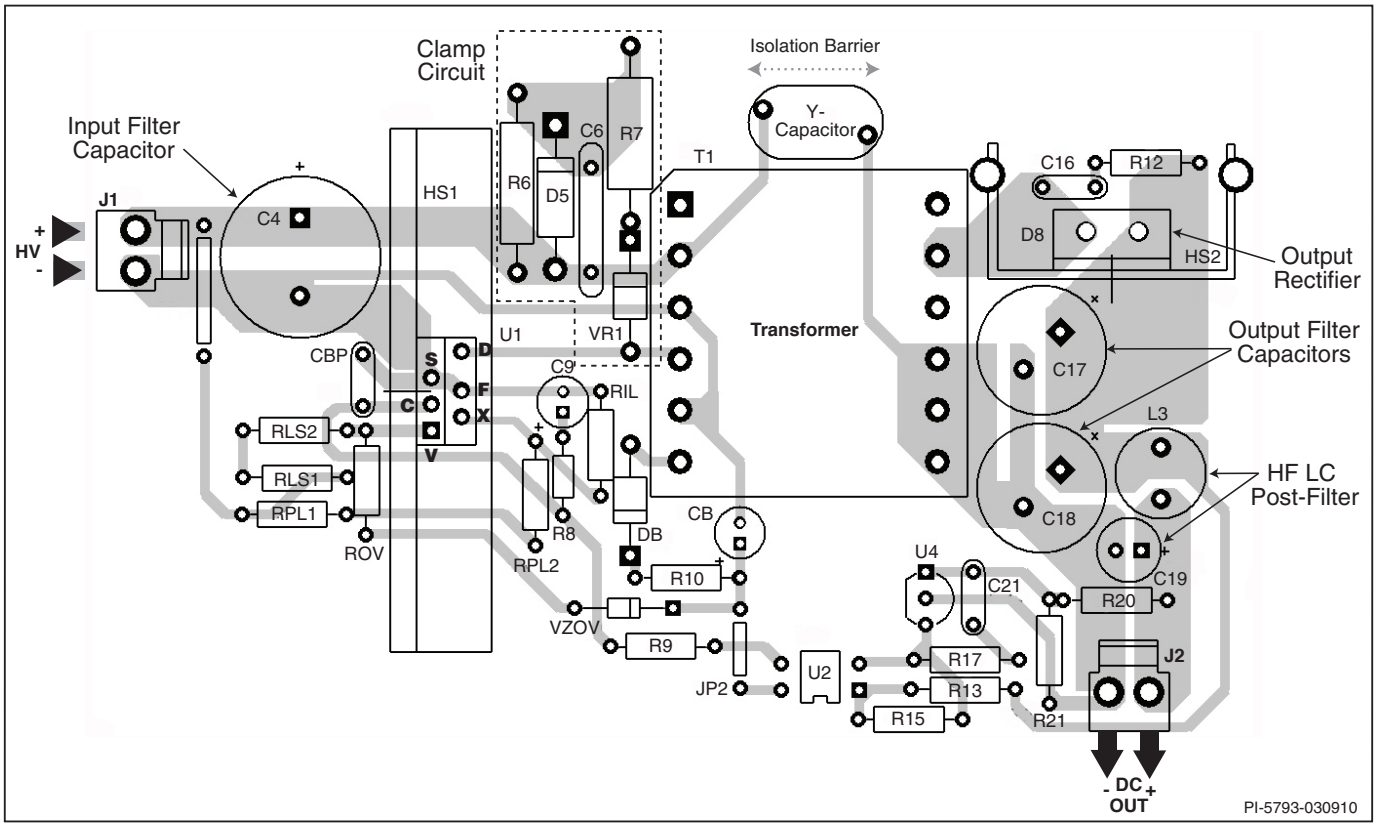


Figure 31. Layout Considerations for TOPSwitch-JX using E Package and Operating at 132 kHz.

Absolute Maximum Ratings[2]

DRAIN Pin Peak Voltage ..... -0.3 V to 725 V
DRAIN Pin Peak Current: TOP264 ..... 2.08 A
DRAIN Pin Peak Current: TOP265 ..... 2.72 A
DRAIN Pin Peak Current: TOP266 ..... 4.08 A
DRAIN Pin Peak Current: TOP267 ..... 5.44 A
DRAIN Pin Peak Current: TOP268 ..... 6.88 A
DRAIN Pin Peak Current: TOP269 ..... 7.73 A
DRAIN Pin Peak Current: TOP270 ..... 9.00 A
DRAIN Pin Peak Current: TOP271 ..... 11.10 A
CONTROL Pin Voltage..... -0.3 V to 9 V
CONTROL Pin Current ..... 100 mA
VOLTAGE MONITOR Pin Voltage ..... -0.3 V to 9 V
CURRENT LIMIT Pin Voltage ..... -0.3 V to 4.5 V
FREQUENCY Pin Voltage .....-0.3 V to 9 V
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature.....-40 °C to 150 °C
Lead Temperature[1] .....260 °C

Notes:
1. 1/16 in. from case for 5 seconds.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Expo sure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: E Package
(θ_{JA}) ..... 105 °C/W[1]
(θ_{JC}) ..... 2 °C/W[2]
V Package
(θ_{JA}) .....68 °C/W[3], 58 °C/W[4]
(θ_{JC}) ..... 2 °C/W[2]
K Package
(θ_{JA}) .....45 °C/W[3], 38 °C/W[4]
(θ_{JC}) ..... 2 °C/W[2]

Notes:
1. Free standing with no heat sink.
2. Measured at the back surface of tab.
3. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 0.36 sq. in. (232mm^2), 2 oz. (610 g/m^2) copper clad.
4. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 35 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Switching Frequency in Full Frequency Mode (average)	f_{OSC}	T_J = 25 °C	FREQUENCY Pin Connected to SOURCE	119	132	145	kHz
			FREQUENCY Pin Connected to CONTROL	59.4	66	72.6	
Frequency Jitter Deviation	Δf		132 kHz Operation		±5		kHz
			66 kHz Operation		±2.5		
Frequency Jitter Modulation Rate	f_M				250		Hz
Maximum Duty Cycle	DC_{MAX}	$I_C = I_{CD1}$	$I_V \le I_{V(DC)}$ V_V = 0 V	75	78	83	%
			I_V = 95 µA	30			
Soft-Start Time	t_{SOFT}	T_J = 25 °C			17		ms
PWM Gain	DC_{REG}	T_J = 25 °C $I_B < I_C < I_{C01}$ See Note C	TOP264-265	-62	-50	-40	%/mA
			TOP266-268	-54	-44	-34	
			TOP269-271	-50	-40	-30	
		T_J = 25 °C $I_C \ge I_{C01}$ See Note A	TOP264-265	-61	-51	-41	
			TOP266-268	-60	-50	-40	
			TOP269-271	-57	-48	-38	
PWM Gain Temperature Drift		See Note B			-0.01		%/mA/°C
External Bias Current	I_B	66 kHz Operation	TOP264-265	0.8	1.4	2.0	mA
			TOP266-268	0.9	1.5	2.1	
			TOP269-271	1.0	1.6	2.2	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
External Bias Current	I_B	132 kHz Operation	TOP264-265	0.9	1.5	2.1	mA
			TOP266-268	1.2	1.8	2.4	
			TOP269-271	1.5	2.1	2.8	
CONTROL Current at 0% Duty Cycle	$I_{C(OFF)}$	66 kHz Operation	TOP264-265		2.9	3.9	mA
			TOP266-268		3.1	4.1	
			TOP269-271		3.3	4.3	
		132 kHz Operation	TOP264-265		3.1	4.1	
			TOP266-268		3.4	4.4	
			TOP269-271		3.8	4.8	
Dynamic Impedance	Z_C	I_C = 2.5 mA; T_J = 25 °C, See Figure 33		13	21	25	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
CONTROL Pin Internal Filter Pole					7		kHz
Upper Peak Current to Set Current Limit Ratio	$k_{PS(UPPER)}$	T_J = 25 °C See Note C		50	55	60	%
Lower Peak Current to Set Current Limit Ratio	$k_{PS(LOWER)}$	T_J = 25 °C See Note C			25		%
Multi-Cycle-Modulation Switching Frequency	$f_{MCM(MIN)}$	T_J = 25 °C			30		kHz
Minimum Multi-Cycle-Modulation On Period	$T_{MCM(MIN)}$	T_J = 25 °C			135		µs
Shutdown/Auto-Restart							
CONTROL Pin Charging Current	$I_{C(CH)}$	T_J = 25 °C	V_C = 0 V	-5.0	-3.5	-1.0	mA
			V_C = 5 V	-3.0	-1.8	-0.6	
Charging Current Temperature Drift		See Note B			0.5		%/°C
Auto-Restart Upper Threshold Voltage	$V_{C(AR)U}$				5.8		V
Auto-Restart Lower Threshold Voltage	$V_{C(AR)L}$			4.5	4.8	5.1	V
Voltage Monitor (V) and External Current Limit (X) Inputs							
Auto-Restart Hysteresis Voltage	$V_{C(AR)HYST}$			0.8	1.0		V
Auto-Restart Duty Cycle	DC_{AR}				2	4	%
Auto-Restart Frequency	f_{AR}				0.5		Hz
Line Undervoltage Threshold Current and Hysteresis (V Pin)	I_{UV}	T_J = 25 °C	Threshold	22	25	27	µA
			Hysteresis		14		µA
Line Overvoltage Threshold Current and Hysteresis (V Pin)	I_{OV}	T_J = 25 °C	Threshold	107	112	117	µA
			Hysteresis		4		µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Voltage Monitor (V) and External Current Limit (X) Inputs (cont.)							
Output Overvoltage Latching Shutdown Threshold Current	$I_{OV(LS)}$	T_J = 25 °C		269	336	403	µA
V Pin Remote ON/OFF Voltage	$V_{V(TH)}$	T_J = 25 °C		0.8	1.0	1.6	V
X Pin Remote-ON/OFF and Latch Reset Negative Threshold Current and Hysteresis	$I_{REM(N)}$	T_J = 25 °C	Threshold	-35	-27	-20	µA
			Hysteresis		5		
V Pin Short-Circuit Current	$I_{V(SC)}$	T_J = 25 °C	$V_V = V_C$	300	400	500	µA
X Pin Short-Circuit Current	$I_{X(SC)}$	V_X = 0 V	Normal Mode	-260	-200	-140	µA
			Auto-Restart Mode	-95	-75	-55	
V Pin Voltage (Positive Current)	V_V	$I_V = I_{OV}$	TOP264-TOP271	2.83	3.0	3.25	V
V Pin Voltage Hysteresis (Positive Current)	$V_{V(HYST)}$		$I_V = I_{OV}$	0.2	0.5		V
X Pin Voltage (Negative Current)	V_X		I_X = -50 µA	1.23	1.30	1.37	V
			I_X = -150 µA	1.15	1.22	1.29	
Maximum Duty Cycle Reduction Onset Threshold Current	$I_{V(DC)}$	$I_C \geq I_B$, T_J = 25 °C		18.9	22.0	24.2	µA
Maximum Duty Cycle Reduction Slope		T_J = 25 °C	$I_{V(DC)} < I_V$ <48 µA		-1.0		%/µA
			$I_V \geq$48 µA		-0.25		
Remote-OFF DRAIN Supply Current	$I_{D(RMT)}$	V_{DRAIN} = 150 V	X or V Pin Floating		0.6	1.0	mA
			V Pin Shorted to CONTROL		1.0	1.6	
Remote-ON Delay	$t_{R(ON)}$	From Remote-ON to Drain Turn-On See Note C	66 kHz		3.0		µs
			132 kHz		1.5		
Remote-OFF Set-up Time	$t_{R(OFF)}$	Minimum Time Before Drain Turn-On to Disable Cycle See Note C	66 kHz		3.0		µs
			132 kHz		1.5		
Frequency Input							
FREQUENCY Pin Threshold Voltage	V_F	See Note B			2.9		V
FREQUENCY Pin Input Current	I_F	T_J = 25 °C	$V_F = V_C$	10	55	90	µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Self Protection Current Limit (See Note D)	I_{LIMIT}	TOP264 T_J = 25 °C	di/dt = 270 mA/µs	1.209	1.30	1.391	A
		TOP265 T_J = 25 °C	di/dt = 350 mA/µs	1.581	1.70	1.819	
		TOP266 T_J = 25 °C	di/dt = 530 mA/µs	2.371	2.55	2.728	
		TOP267 T_J = 25 °C	di/dt = 625 mA/µs	2.800	3.01	3.222	
		TOP268 T_J = 25 °C	di/dt = 675 mA/µs	3.023	3.25	3.478	
		TOP269 T_J = 25 °C	di/dt = 720 mA/µs	3.236	3.48	3.723	
		TOP270 T_J = 25 °C	di/dt = 870 mA/µs	3.906	4.20	4.494	
		TOP271 T_J = 25 °C	di/dt = 1065 mA/µs	4.808	5.17	5.532	
Initial Current Limit	I_{INIT}	See Note C		0.70 × $I_{LIMIT(MIN)}$			A
Power Coefficient	P_{COEFF}	T_J = 25 °C, See Note E	$I_X \leq$ - 165 µA	0.9 × I^2f	I^2f	1.2 × I^2f	A^2kHz
			$I_X \leq$ - 117 µA	0.9 × I^2f	I^2f	1.2 × I^2f	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C, See Figure 34			220		ns
Current Limit Delay	$t_{IL(D)}$				100		ns
Thermal Shutdown Temperature				135	142	150	°C
Thermal Shutdown Hysteresis					75		°C
Power-Up Reset Threshold Voltage	$V_{C(RESET)}$	Figure 35 (S1 Open Condition)		1.75	3.0	4.25	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)			Min	Typ	Max	Units
Output								
ON-State Resistance	$R_{DS(ON)}$	TOP264 I_D = 150 mA		T_J = 25 °C		5.4	6.25	Ω
				T_J = 100 °C		8.35	9.70	
		TOP265 I_D = 200 mA		T_J = 25 °C		4.1	4.70	
				T_J = 100 °C		6.3	7.30	
		TOP266 I_D = 300 mA		T_J = 25 °C		2.8	3.20	
				T_J = 100 °C		4.1	4.75	
		TOP267 I_D = 400 mA		T_J = 25 °C		2.0	2.30	
				T_J = 100 °C		3.1	3.60	
		TOP268 I_D = 500 mA		T_J = 25 °C		1.7	1.95	
				T_J = 100 °C		2.5	2.90	
		TOP269 I_D = 600 mA		T_J = 25 °C		1.45	1.70	
				T_J = 100 °C		2.25	2.60	
		TOP270 I_D = 700 mA		T_J = 25 °C		1.20	1.40	
				T_J = 100 °C		1.80	2.10	
		TOP271 I_D = 800 mA		T_J = 25 °C		1.05	1.20	
				T_J = 100 °C		1.55	1.80	
DRAIN Supply Voltage		T_J ≤ 85 °C, See Note F			18			V
					36			
OFF-State Drain Leakage Current	I_{DSS}	V_V = Floating, Device Not Switching, V_{DS} = 580 V, T_J = 125 °C					470	µA
Breakdown Voltage	BV_{DSS}	V_V = Floating, Device Not Switching, T_J = 25 °C, See Note G			725			V
Rise Time	t_R	Measured in a Typical Flyback Converter Application				100		ns
Fall Time	t_F					50		ns
Supply Voltage Characteristics								
Control Supply/ Discharge Current	I_{CD1}	Output MOSFET Enabled V_X, V_V = 0 V	66 kHz Operation	TOP264-265	0.6	1.2	2.0	mA
				TOP266-268	0.9	1.4	2.3	
				TOP269-271	1.1	1.6	2.5	
			132 kHz Operation	TOP264-265	0.8	1.4	2.1	
				TOP266-268	1.2	1.7	2.4	
				TOP269-271	1.5	2.1	2.9	
	I_{CD2}	Output MOSFET Disabled V_X, V_V = 0 V			0.3	0.5	1.2	

NOTES:

A. Derived during test from the parameters DC_{MAX}, I_B and $I_{C(OFF)}$ at 132 kHz.

B. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

C. Guaranteed by characterization. Not tested in production.

D. For externally adjusted current limit values, please refer to Figures 36 and 37 (Current Limit vs. External Current Limit Resistance) in the Typical Performance Characteristics section. The tolerance specified is only valid at full current limit.

E. I^2f calculation is based on typical values of I_{LIMIT} and $f_{OSC,}$ i.e. $I_{LIMIT(TYP)}{}^2 \times f_{OSC}$, where f_{OSC} = 66 kHz or 132 kHz depending on FREQUENCY pin connection. See f_{OSC} specification for detail.

F. The device will start up at 18 V_{DC} drain voltage. The capacitance of electrolytic capacitors drops significantly at temperatures below 0 °C. For reliable start-up at 18 V in sub-zero temperatures, designers must ensure that circuit capacitors meet recommended capacitance values.

G. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

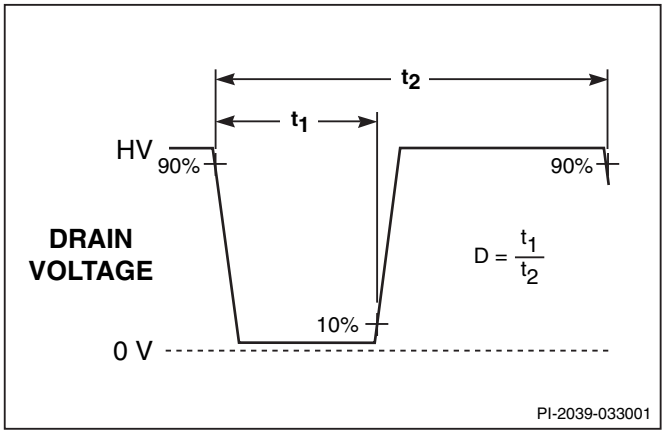


Figure 32. Duty Cycle Measurement.

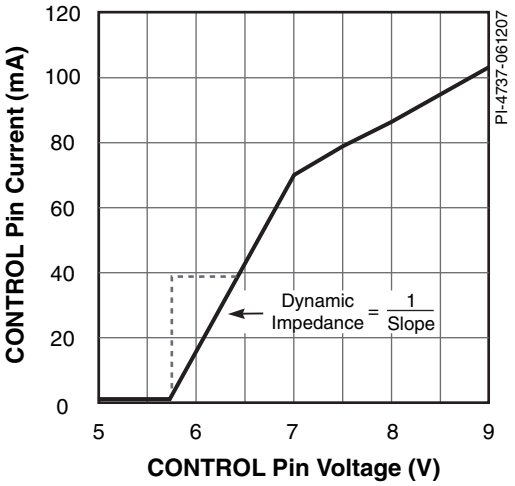


Figure 33. CONTROL Pin I-V Characteristic.

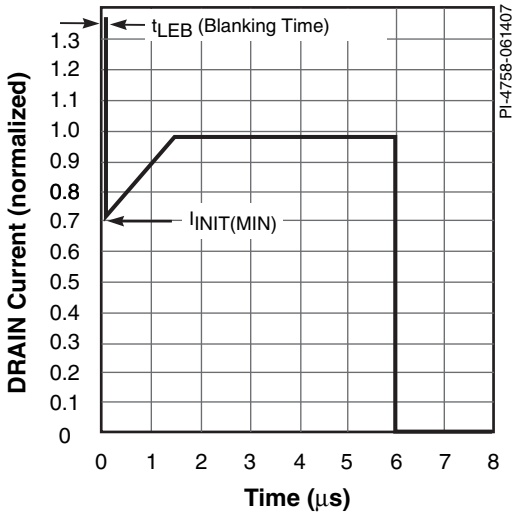
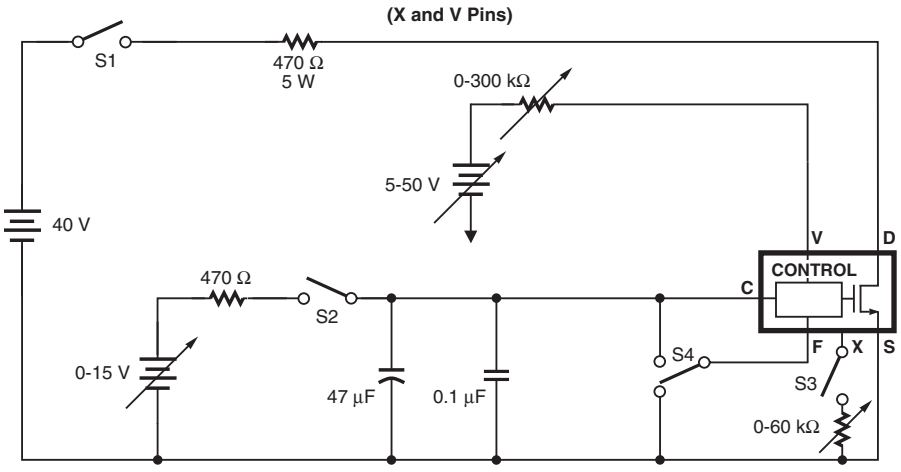


Figure 34. Drain Current Operating Envelope.



NOTES: 1. This test circuit is not applicable for current limit or output characteristic measurements.

Figure 35. TOPSwitch-JX General Test Circuit.

Typical Performance Characteristics

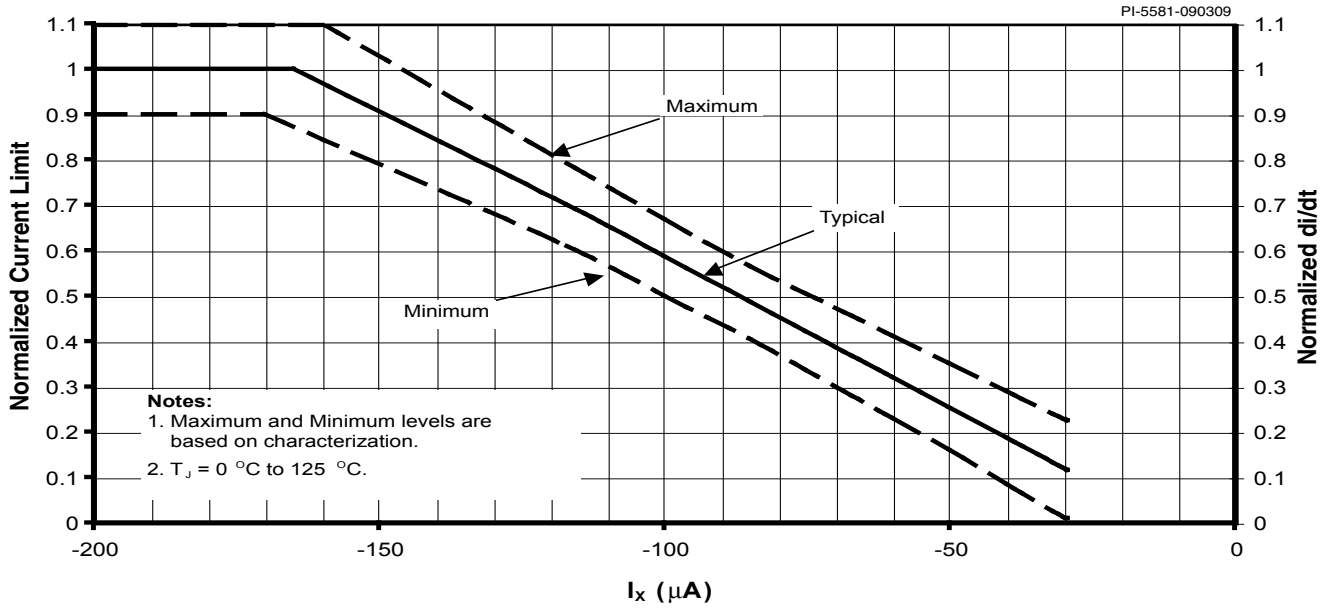


Figure 36. Normalized Current Limit vs. X Pin Current.

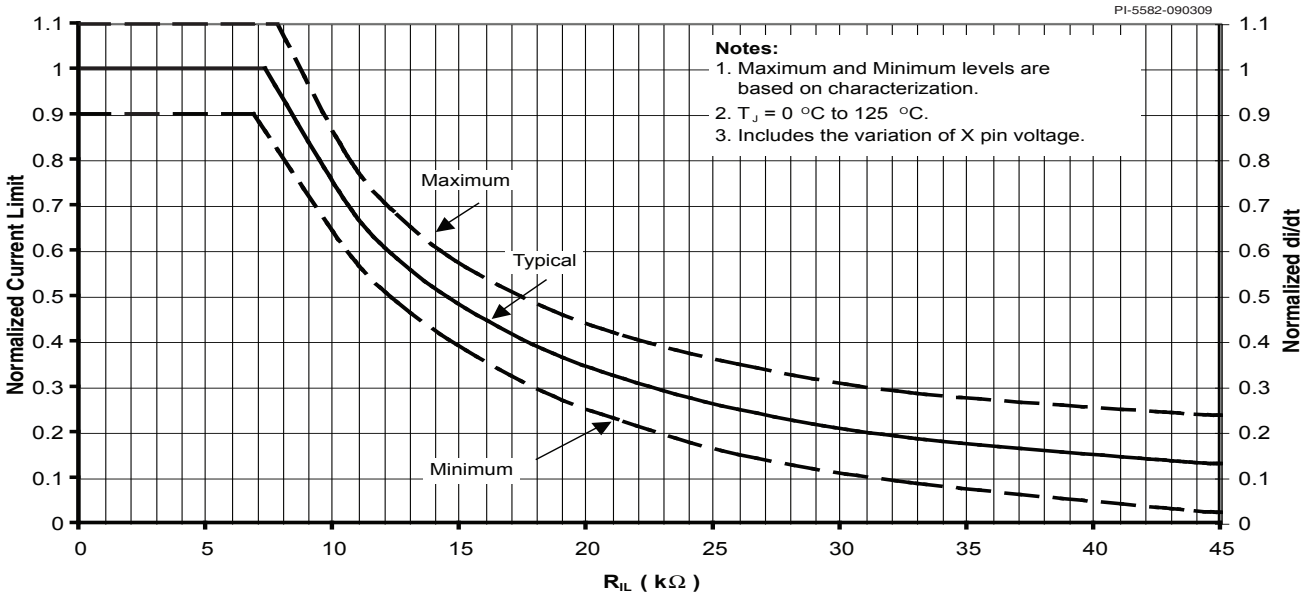


Figure 37. Normalized Current Limit vs. External Current Limit Resistance.

Typical Performance Characteristics (cont.)

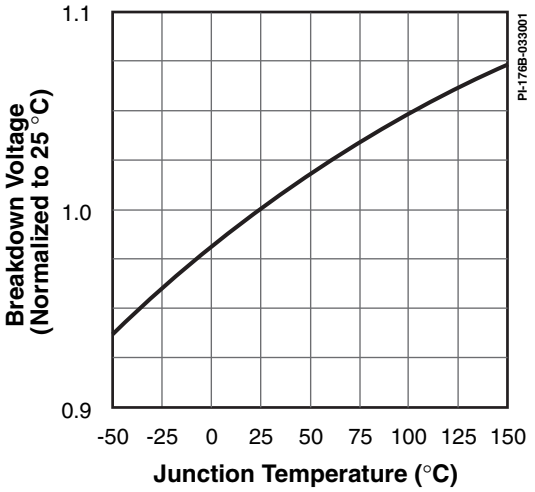


Figure 38. Breakdown Voltage vs. Temperature.

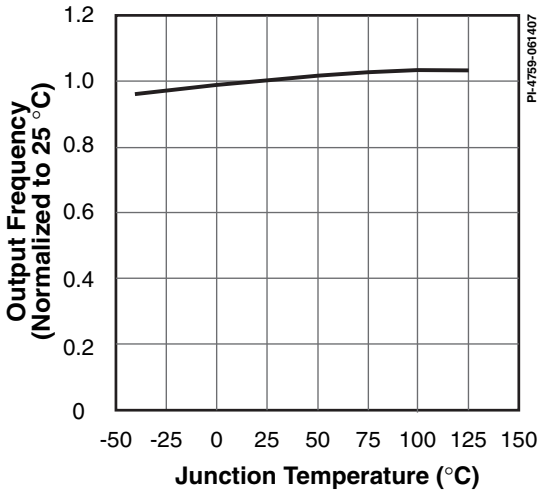


Figure 39. Frequency vs. Temperature.

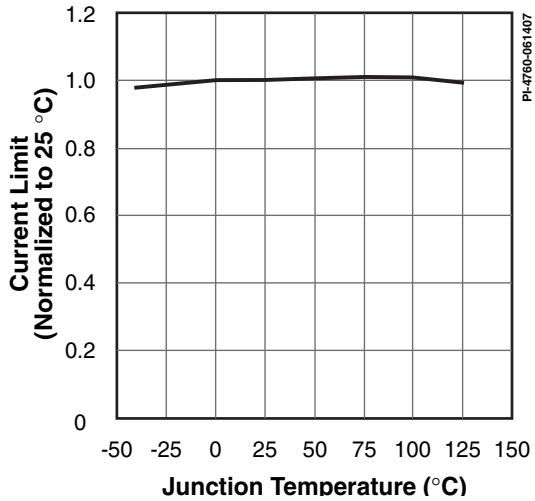


Figure 40. Internal Current Limit vs. Temperature.

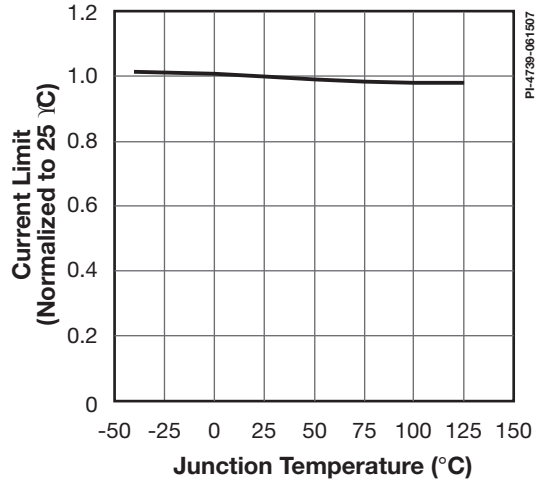


Figure 41. External Current Limit vs. Temperature with R_{IL} = 10.5 kΩ.

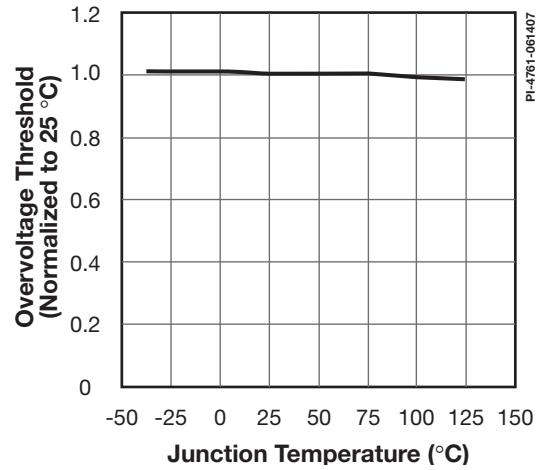


Figure 42. Overvoltage Threshold vs. Temperature.

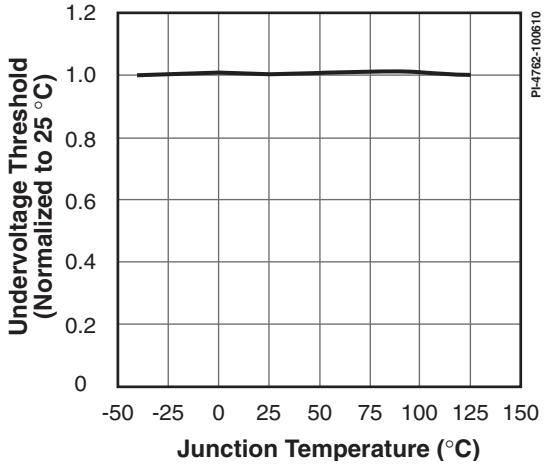


Figure 43. Undervoltage Threshold vs. Temperature.

Typical Performance Characteristics (cont.)

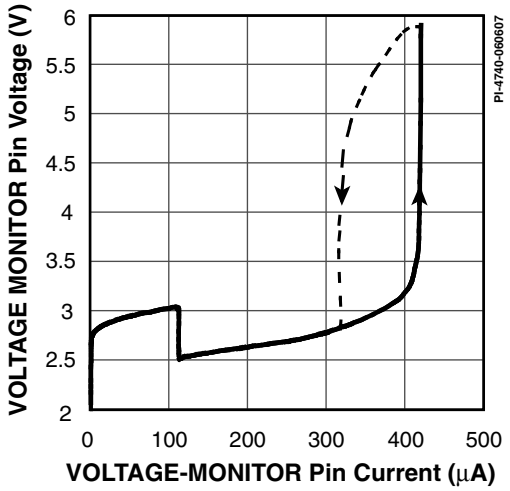


Figure 44. VOLTAGE-MONITOR Pin vs. Current.

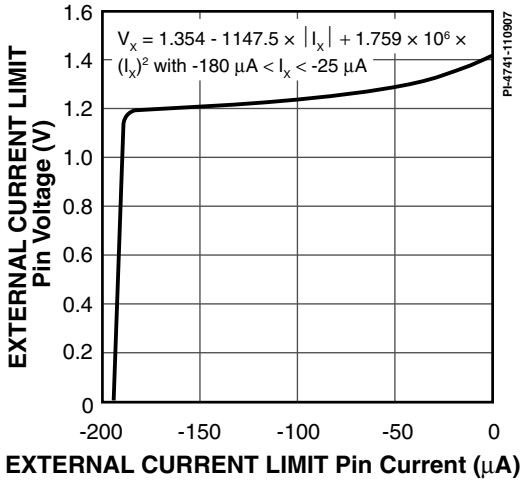


Figure 45. EXTERNAL CURRENT LIMIT Pin Voltage vs. Current.

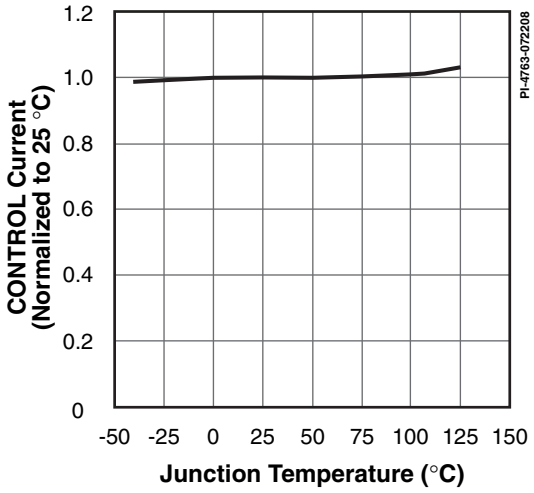


Figure 46. Control Current Out at 0% Duty Cycle vs. Temperature.

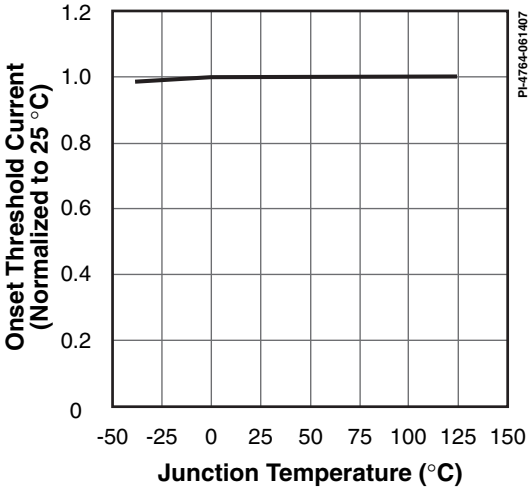


Figure 47. Maximum Duty Cycle Reduction Onset Threshold Current vs. Temperature.

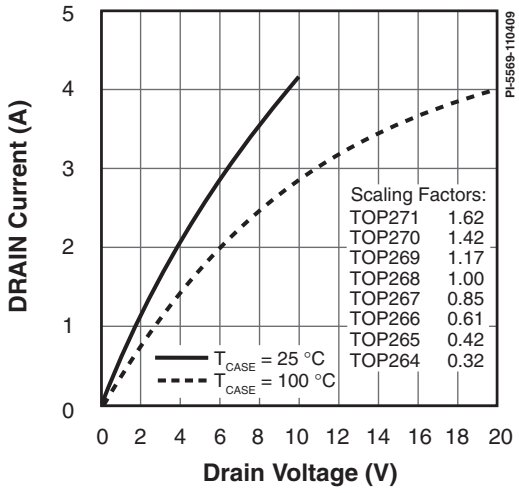


Figure 48. Output Characteristics.

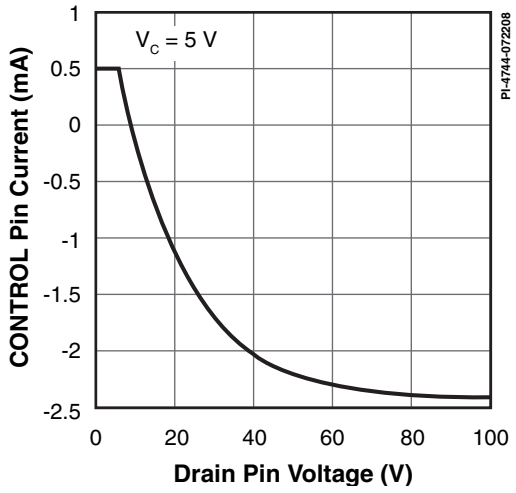


Figure 49. I_C vs. DRAIN Voltage.

Typical Performance Characteristics (cont.)

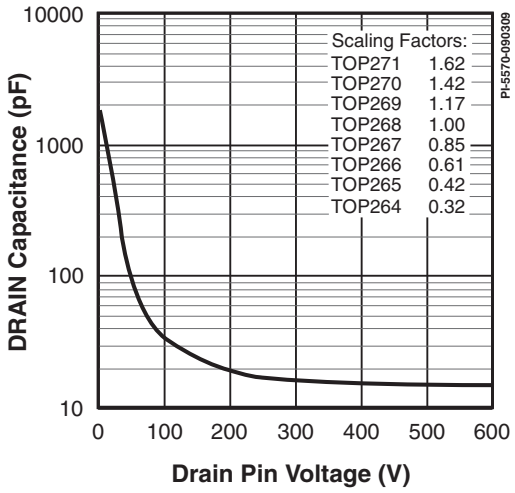


Figure 50. C_{OSS} vs. DRAIN Voltage.

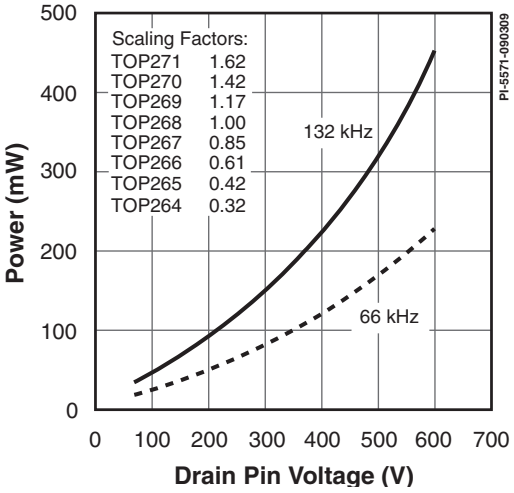


Figure 51. DRAIN Capacitance Power.

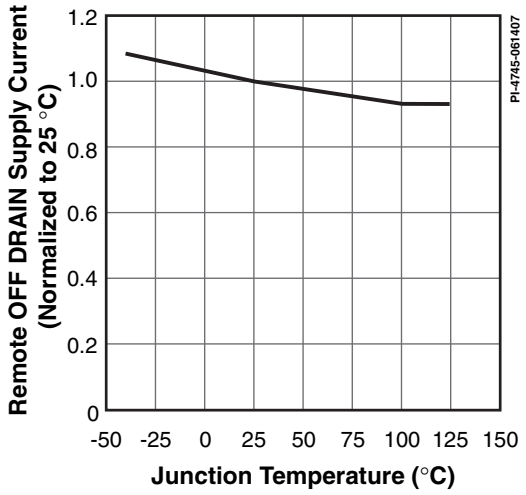
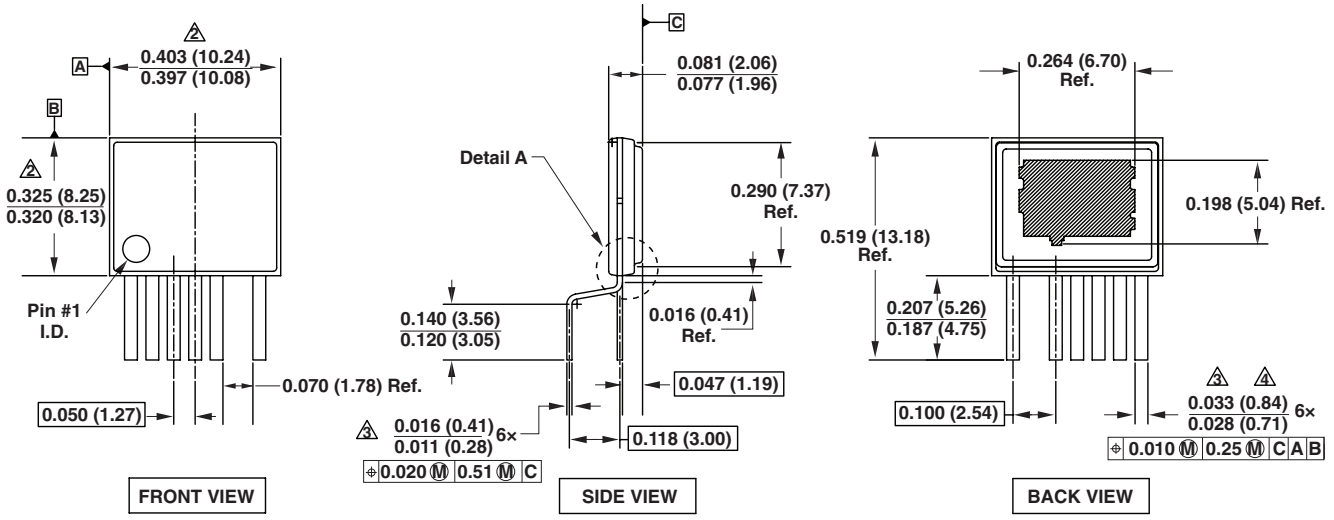
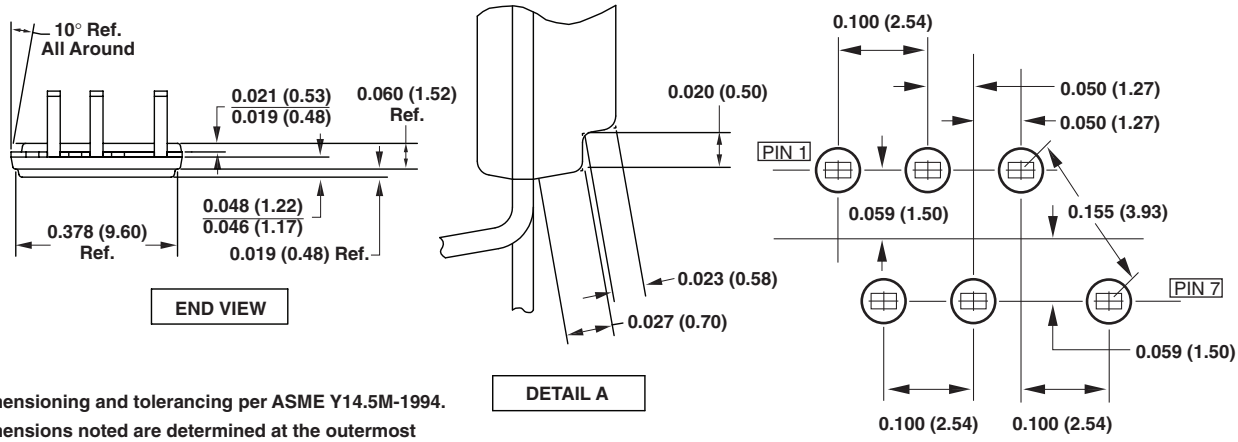


Figure 52. Remote-OFF DRAIN Supply Current vs. Temperature.

eSIP-7C (E Package)





Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

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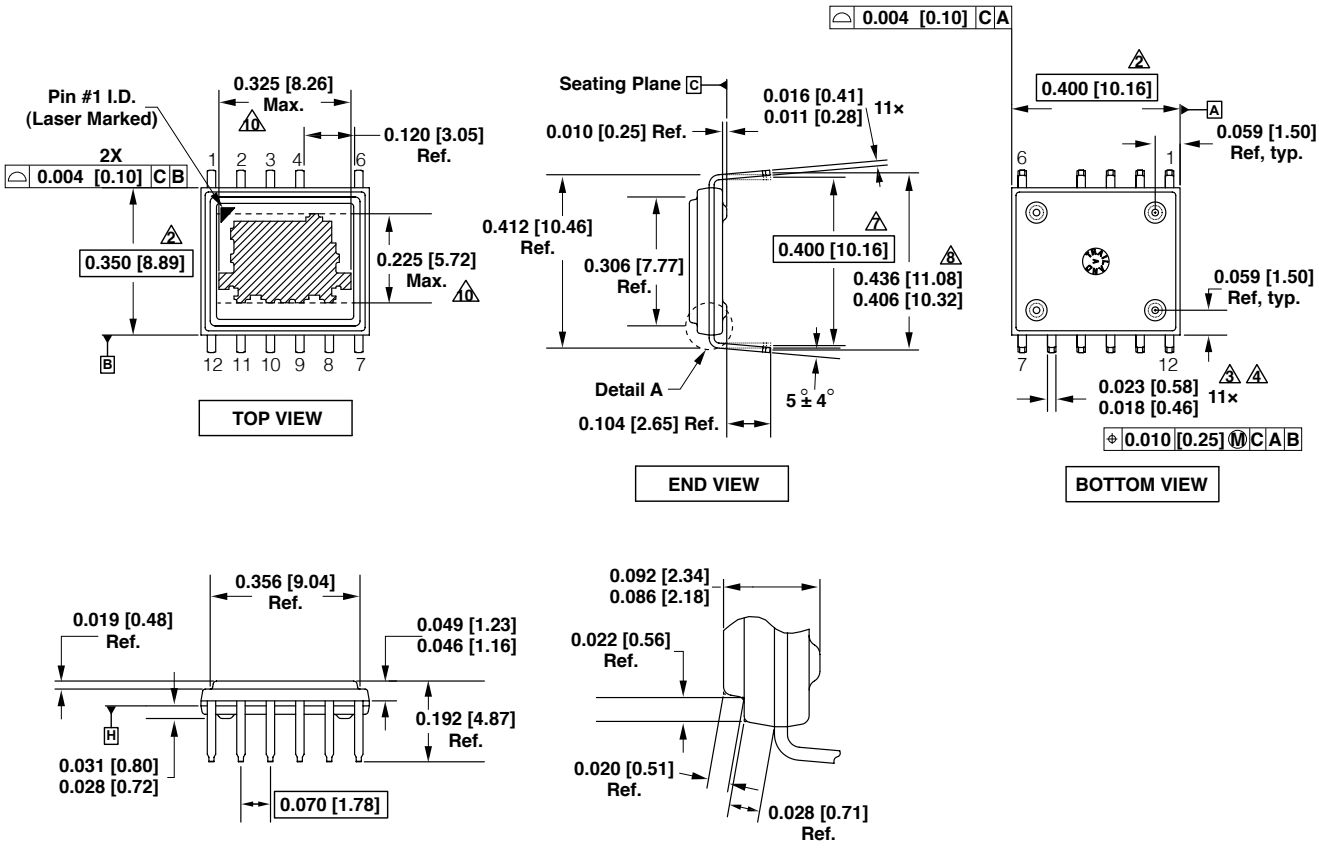
eDIP-12B (V Package)

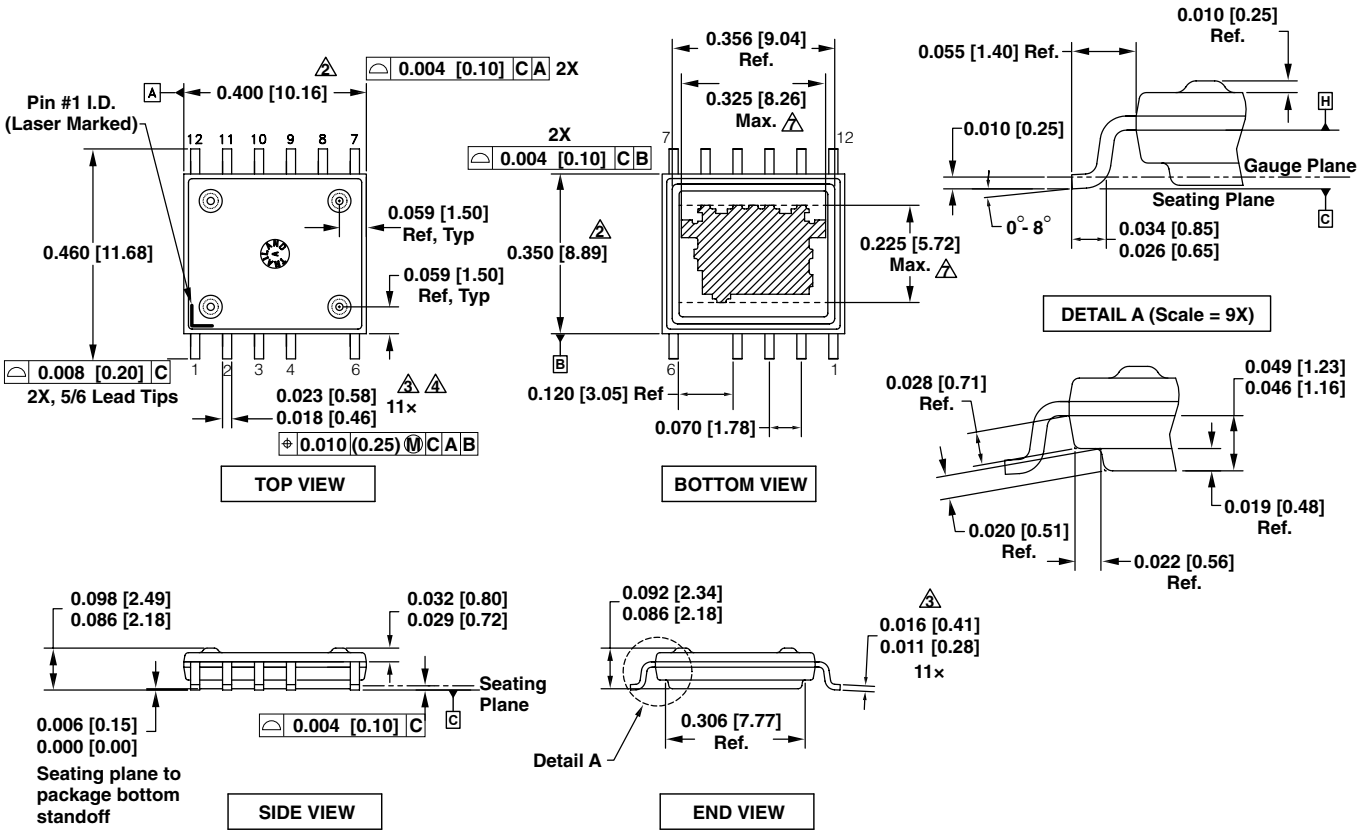


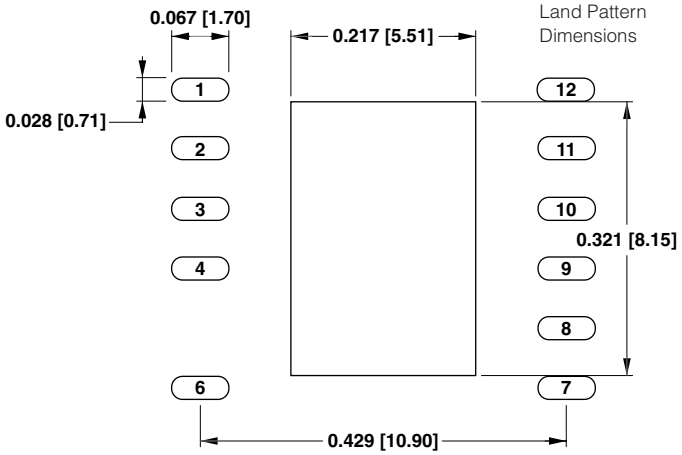
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Measured with the leads constrained to be perpendicular to Datum C.
8. Measured with the leads unconstrained.
9. Lead numbering per JEDEC SPP-012.
10. Exposed pad is nominally located at the centerline of Datums A and B. “Max” dimensions noted include both size and positional tolerances.

PI-5556a-100311

eSOP-12B (K Package)



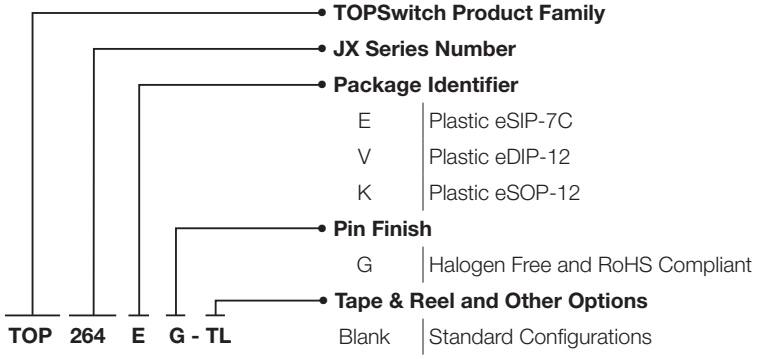


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Exposed pad is nominally located at the centerline of Datums A and B. "Max" dimensions noted include both size and positional tolerances.

PI-5748a-100311

Part Ordering Information



Revision	Notes	Date
A	Release data sheet.	01/10
B	Added eDIP parts.	01/10
B	Page 4 “latching” changed to “hysteretic”. Table 3 updated.	03/10
B	Sentence in ‘Line-Sense Resistor Values’ section updated.	07/10
C	Added K package parts.	11/10
D	Updated K and V package drawings.	06/11
E	Added eDIP-12B and eSOP-12B packages. Removed eDIP-12 and eSOP-12 packages.	10/11
E	Updated Figure 2 and K package layout.	08/12
F	Updated with new Brand Style.	05/15

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