For Non-Isolated
Off-Line PWM Controllers with Integrated Power MOSFET

# STR5A45xD Series

**Data Sheet**

## Description

The STR5A45xD Series is power ICs for switching power supplies, incorporating a MOSFET and a current mode PWM controller IC for non-isolated Buck converter and Inverting converter topologies.

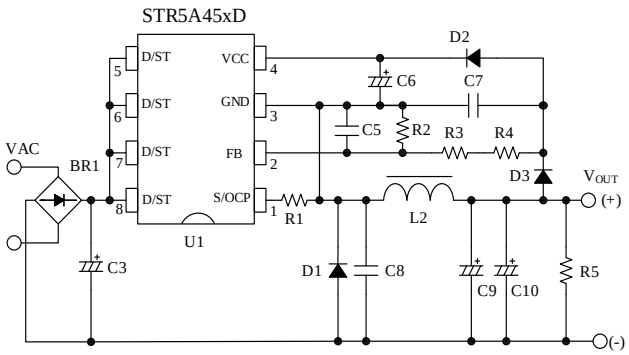
The operation mode is automatically changed, in response to load, to the fixed switching frequency, to the switching frequency control, and to the burst oscillation mode. Thus the power efficiency is improved.

The product achieves high cost-performance power supply systems with few external components.

## Features

- Pb-free (RoHS Compliant)
- Buck Converter
- Inverting Converter
- Current Mode PWM Control
- Automatically Switch the Operation Mode According to the Load
  Heavy Load: 60 kHz (typ.) Fixed Switching Frequency Mode
  Medium Load: Green Mode, 23 kHz (typ.) to 60 kHz (typ.)
  Light Load: Burst Oscillation Mode
- Built-in Startup Function
- Built-in Error Amplifier
- Random Switching Function
- Leading Edge Blanking Function
- Soft Start Function
- Protections
  Overcurrent Protection (OCP) with Input Compensation Function: Adjustabe OCP Operation Point by External Current Detection Resistor
  Overload Protection (OLP): Auto-restart
  Overvoltage Protection (OVP): Auto-restart
  Thermal Shutdown with Hysteresis (TSD): Auto-restart

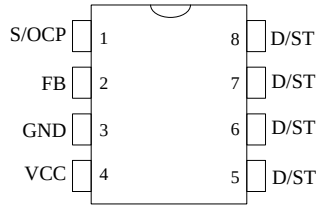
## Typical Application (Buck Convertor)




## Package

DIP8






Not to scale

## Selection Guide

- Electrical Characteristics
  $f_{OSC(AVG)}$ = 60 kHz (typ.)
  $V_{DSS}$ = 650 V (min.)

| Part Number | $R_{DS(ON)}$ (max.) | $I_{OUT(MAX)}$* (Universal, Open Frame, $V_{OUT}$ = 24 V) |
|---|---|---|
| STR5A451D | 4.0 Ω | 0.7 A |
| STR5A453D | 1.9 Ω | 0.9 A |

* The output power is actual continues current that is measured at 50 °C ambient. The peak output current can be 120 to 140 % of the value stated here. Thermal design affects the output current. It may be less than the value stated here.

## Recommended Operating Condition

| Parameter | Buck Converter | Inverting Converter |
|---|---|---|
| Input Voltage | AC 85 V to AC 265 V | |
| D/ST Input Voltage | ≥ 40 V | |
| Output Voltage Range* | > 11 V<br>< 27.5 V | > – 27.5 V<br>< – 11 V |

*Add a Zenner diode or a regulator to the VCC pin when the target output voltage is high.

## Applications

- White Goods
- Auxiliary Power Supply
  (lighting Equipment with Microcomputer, etc.)
- Power Supply for Motor Control (actuator, etc.)
- Telecommunication Equipment
  (Convertible from 48 VDC to 15 VDC)
- Other SMPS



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## 1. Absolute Maximum Ratings

The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
Unless otherwise specified, $T_A$ = 25 °C, all D/ST pins (5 pin to 8pin) are shorted.

| Parameter | Symbol | Test Conditions | Pins | Rating | Units | Remarks |
|---|---|---|---|---|---|---|
| Drain Peak Current | $I_{DPEAK}$ | Single pulse | 8 – 1 | 3.6 | A | STR5A451D |
| | | | | 5.2 | | STR5A453D |
| Avalanche Energy(1) | $E_{AS}$ | $I_{LPEAK}$ = 2.13 A | 8 – 1 | 53 | mJ | STR5A451D |
| | | $I_{LPEAK}$ = 2.46 A | | 72 | | STR5A453D |
| S/OCP Pin Voltage | $V_{S/OCP}$ | | 1 – 3 | −2 to 5 | V | |
| FB Pin Voltage | $V_{FB}$ | | 2 – 3 | −0.3 to 7 | V | |
| VCC Pin Voltage | $V_{CC}$ | | 4 – 3 | −0.3 to 32 | V | |
| D/ST Pin Voltage | $V_{D/ST}$ | | 4 – 5 | −0.3 to $V_{DSS}$ | V | |
| MOSFET Power Dissipation | $P_{D1}$ | (2) | 8 – 1 | 1.68 | W | STR5A451D |
| | | | | 1.76 | | STR5A453D |
| Control Part Power Dissipation | $P_{D2}$ | | 4 – 3 | 1.3 | W | |
| Operating Ambient Temperature | $T_{OP}$ | | — | −40 to 125 | °C | |
| Storage Temperature | $T_{STG}$ | | — | −40 to 125 | °C | |
| Junction Temperature | $T_J$ | | — | 150 | °C | |

## 2. Electrical Characteristics

The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
Unless otherwise specified, $T_A$ = 25 °C, all D/ST pins (5 pin to 8pin) are shorted.

| Parameter | Symbol | Test Conditions | Pins | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|---|---|
| **Power Supply Startup Operation** | | | | | | | | |
| Operation Start Voltage | $V_{CC(ON)}$ | | 4 – 3 | 13.6 | 15.0 | 16.6 | V | |
| Operation Stop Voltage | $V_{CC(OFF)}$ | | 4 – 3 | 7.3 | 8.0 | 8.7 | V | |
| Circuit Current in Operation | $I_{CC(ON)}$ | $V_{CC}$ = 12 V | 4 – 3 | — | — | 3.0 | mA | |
| Startup Circuit Operation Voltage | $V_{ST(ON)}$ | $V_{CC}$ = 13.5 V | 8 – 3 | 21 | 29 | 37 | V | |
| Startup Current | $I_{CC(ST)}$ | $V_{CC}$ = 13.5 V | 4 – 3 | –3.0 | −1.7 | –0.9 | mA | |
| **PWM Operation** | | | | | | | | |
| Average PWM Switching Frequency | $f_{OSC(AVG)}$ | $V_{FB}$ = $V_{FB(REF)}$ – 20 mV | 8 – 3 | 53 | 60 | 67 | kHz | |
| Switching Frequency Modulation Deviation | Δf | | 8 – 3 | — | 7.1 | — | kHz | |
| Feedback Reference Voltage | $V_{FB(REF)}$ | | 2 – 3 | 2.44 | 2.50 | 2.56 | V | |
| Feedback Current(1) | $I_{FB(OP)}$ | $V_{FB}$ = 2.3 V | 2 – 3 | −2.4 | −0.8 | — | µA | |

(1) Single pulse, $V_{DD}$ = 99 V, L = 20 mH
(2) When embedding this hybrid IC onto the printed circuit board (cupper area in a 15 mm×15 mm)
(1) Guaranteed by design.


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| Parameter | Symbol | Test Conditions | Pins | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|---|---|
| S/OCP Pin Standby Threshold voltage | $V_{OCP(STB)}$ | | 1 – 3 | — | 0.11 | — | V | |
| Maximum Duty Cycle | $D_{MAX}$ | | 8 – 3 | 56 | 62 | 69 | % | |
| **Protection** | | | | | | | | |
| Leading Edge Blanking Time(1) | $t_{BW}$ | | – | — | 280 | — | ns | |
| OCP Compensation Coefficient(1) | DPC | | – | — | 15.8 | — | mV/µs | |
| OCP Compensation Limit Duty(1) | $D_{DPC}$ | | – | — | 36 | — | % | |
| OCP Threshold Voltage at Zero Duty Cycle | $V_{OCP(L)}$ | | 1 – 3 | 0.640 | 0.735 | 0.830 | V | |
| OCP Threshold Voltage | $V_{OCP(H)}$ | | 1 – 3 | 0.74 | 0.83 | 0.92 | V | |
| OCP Threshold Voltage During LEB ($t_{BW}$) | $V_{OCP(LEB)}$ | | 1 – 3 | — | 1.61 | — | V | |
| OVP Threshold Voltage | $V_{CC(OVP)}$ | | 4 – 3 | 27.5 | 29.3 | 31.3 | V | |
| OLP Delay Time at Startup | $t_{OLP}$ | $V_{FB}$ = 0.41 V | 8 – 3 | 53 | 70 | 88 | ms | |
| Circuit Current in Overload Protection | $I_{OLP}$ | $V_{CC}$ = 9 V | 4 – 3 | — | 300 | — | | |
| Delay Time of FB Pin Short Protection at Startup | $t_{FBSH}$ | $V_{FB}$ = 0.2 V | 8 – 3 | 13.0 | 17.5 | 22.0 | | |
| Standby Blanking Time at Startup | $t_{STB(INH)}$ | $V_{FB}$ = 2.6 V | 8 – 3 | 2.0 | 3.0 | 4.0 | ms | |
| Thermal Shutdown Operating Temperature(1) | $T_{J(TSD)}$ | | – | 135 | — | — | °C | |
| Thermal Shutdown Hysteresis(1) | $T_{J(TSD)HYS}$ | | – | — | 80 | — | °C | |
| **Power MOSFET** | | | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{DSS}$ | $I_{DS}$ = 50 µA | 8 – 1 | 650 | — | — | V | |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = $V_{DSS}$ | 8 – 1 | — | — | 50 | µA | |
| On-resistance | $R_{DS(ON)}$ | $I_{DS}$ = 0.4 A | 8 – 1 | — | — | 4.0 | Ω | STR5A451D |
| | | | | — | — | 1.9 | | STR5A453D |
| Switching Time | $t_f$ | | 8 – 1 | — | — | 250 | ns | |
| **Thermal Characteristics** | | | | | | | | |
| Thermal Resistance Junction to Case (2) | $\theta_{J-C}$ | | — | — | — | 18 | °C/W | STR5A451D STR5A453D |

(2) Case temperature ($T_C$) measured at the center of the case top surface


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## 3. Mechanical Characteristics

| Parameter | Conditions | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Package Weight | | — | 0.51 | — | g | |

## 4. Performance Curves

### 4.1 Derating Curves

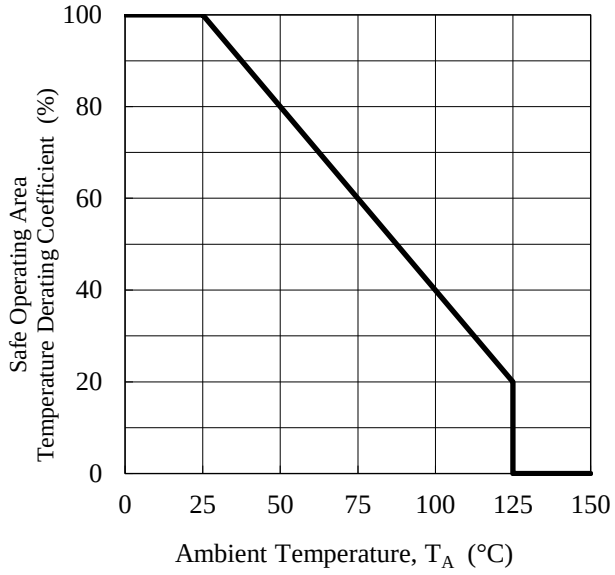


Figure 4-1. SOA Temperature Derating Coefficient Curve

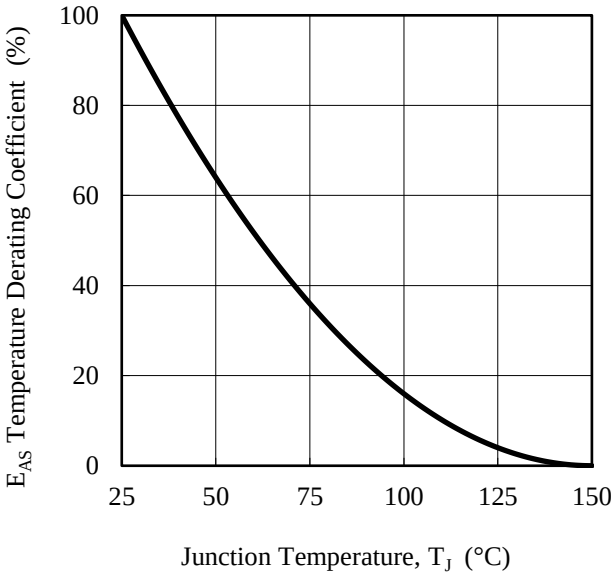


Figure 4-2. Avalanche Energy Derating Coefficient Curve


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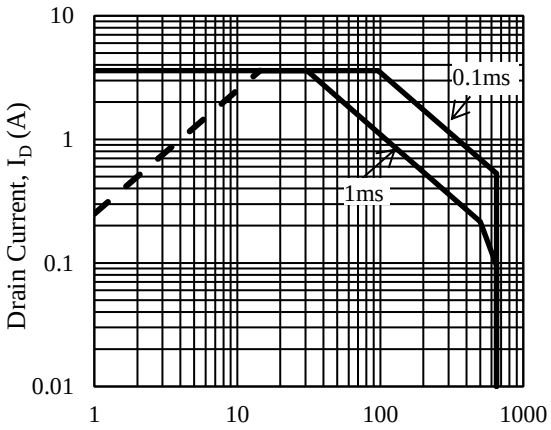
## 4.2 MOSFET Safe Operating Area Curves

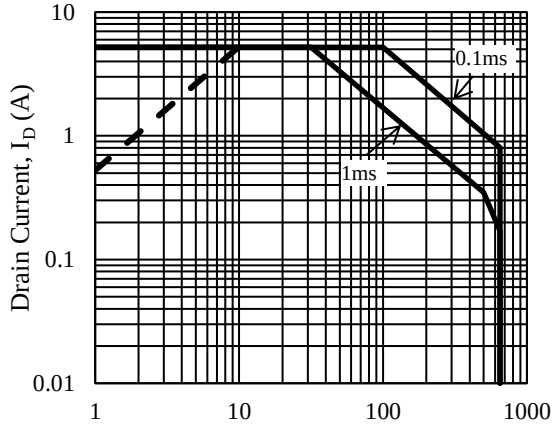
When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 4-1. The broken line in the safe operating area curve is the drain current curve limited by on-resistance.

Unless otherwise specified, $T_A$ = 25 °C, Single pulse.

● **STR5A451D**

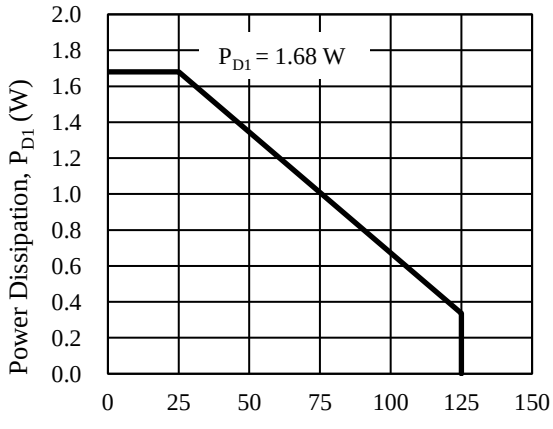



● **STR5A453D**

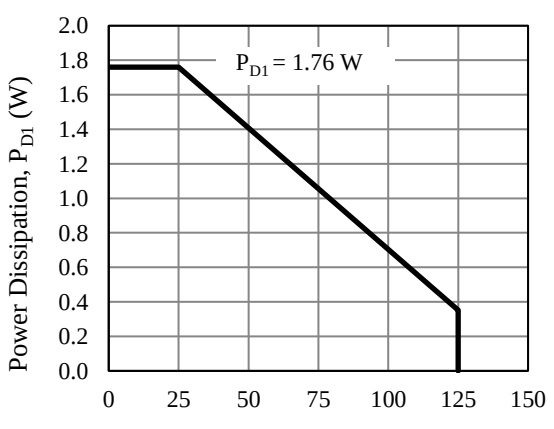



## 4.3 Ambient Temperature versus Power Dissipation Curves

● **STR5A451D**




● **STR5A453D**





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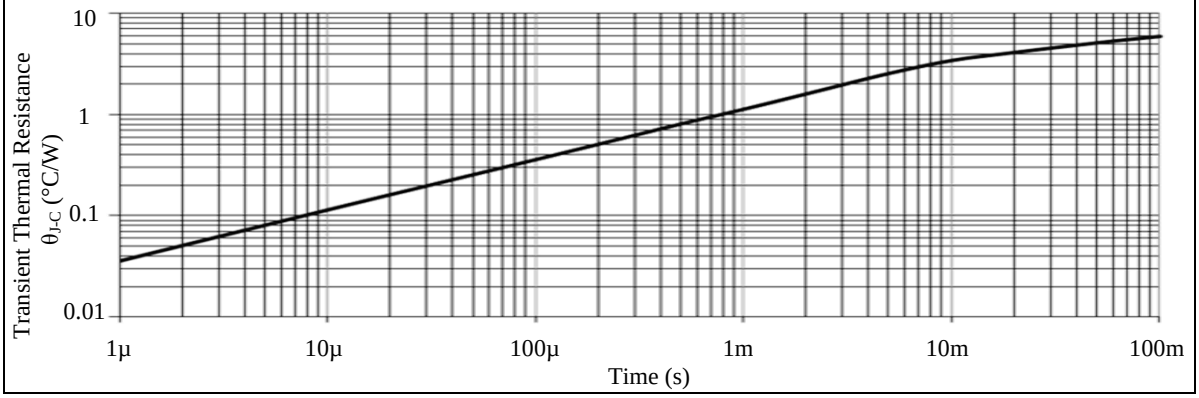
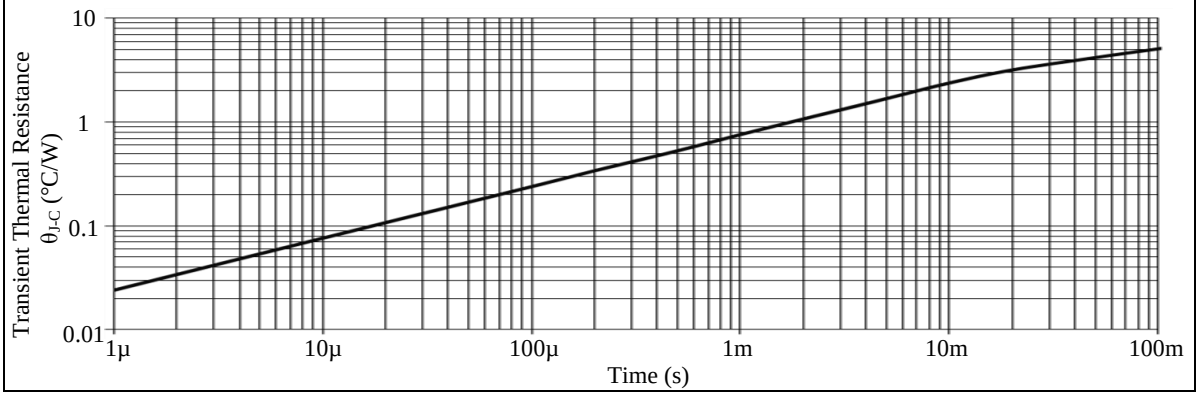
## 4.4 Transient Thermal Resistance Curves

● **STR5A451D**




● **STR5A453D**





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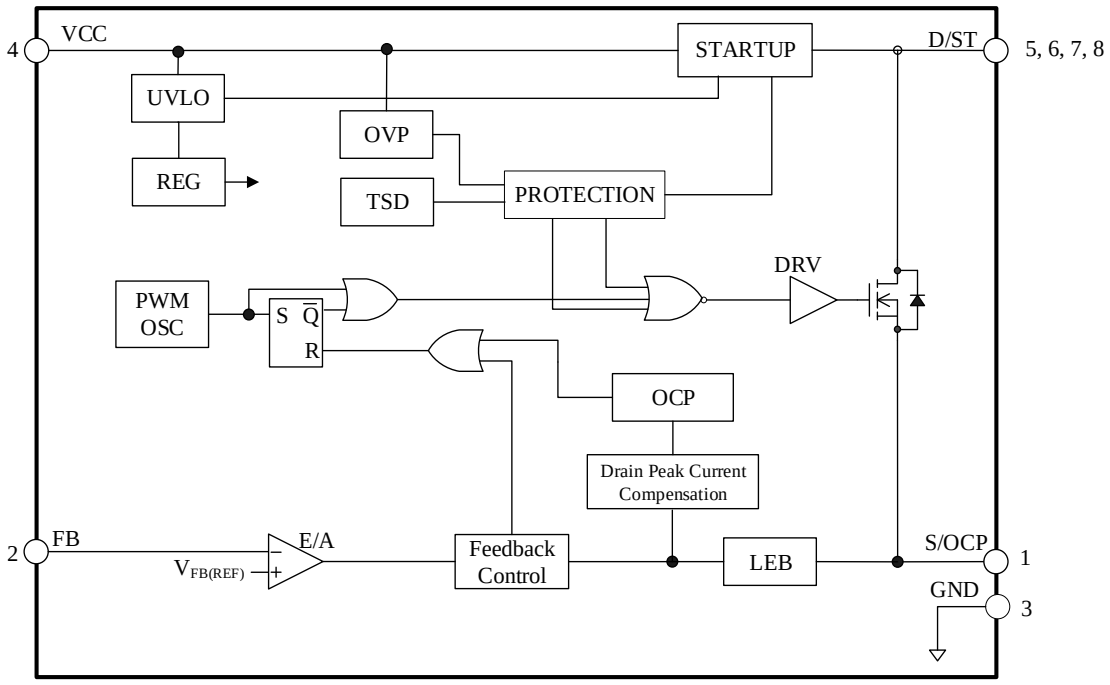
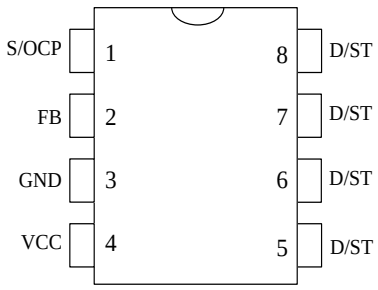
## 5. Block Diagram




## 6. Pin Configuration Definitions




| Pin | Name | Descriptions |
|---|---|---|
| 1 | S/OCP | Power MOSFET source and overcurrent protection (OCP) signal input |
| 2 | FB | Constant voltage control signal input and overload protection signal input |
| 3 | GND | Ground |
| 4 | VCC | Power supply voltage input for control part and overvoltage protection (OVP) signal input |
| 5 | D/ST | MOSFET drain and startup current input |
| 6 | | |
| 7 | | |
| 8 | | |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## 7. Typical Applications

Figure 7-1 and Figure 7-2 are the example circuits.

To enhance the heat dissipation, the wide pattern layout of the D/ST pin (5 through 8 pin) is recommended.

When the absolute value of the output voltage | $V_{OUT}$ | is 27.5 V or higher, add a Zenner diode DZ1 connected to D1 in serial as shown in Figure 7-3. Using the maximum duty cycle of 50 % in the steady state operation, the condition of $|V_{OUT}|$ is shown below:

$$| V_{OUT} | : \ 11V < |V_{OUT}| - V_{DZ1} < 27.5V$$

| $V_{OUT}$ | according to the input voltage:

For buck topology, | $V_{OUT}$ | ≤ 0.5 × input voltage

For inverting topology, | $V_{OUT}$ | ≤ input voltage

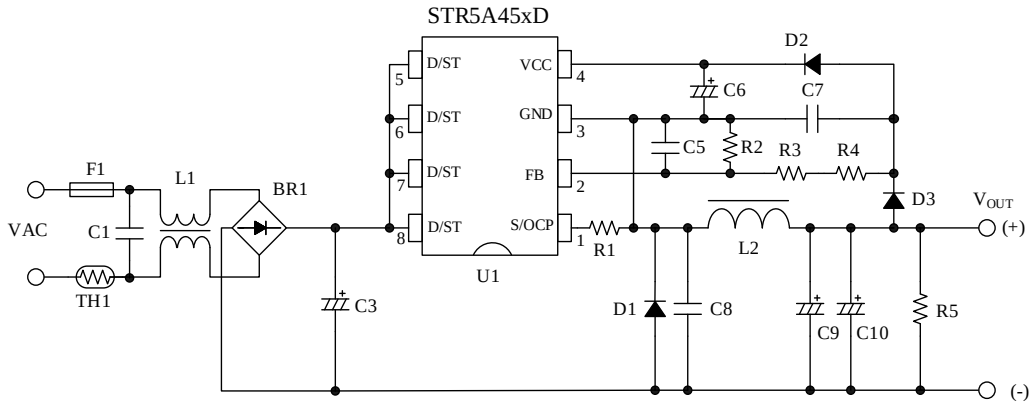


Figure 7-1. Buck Converter

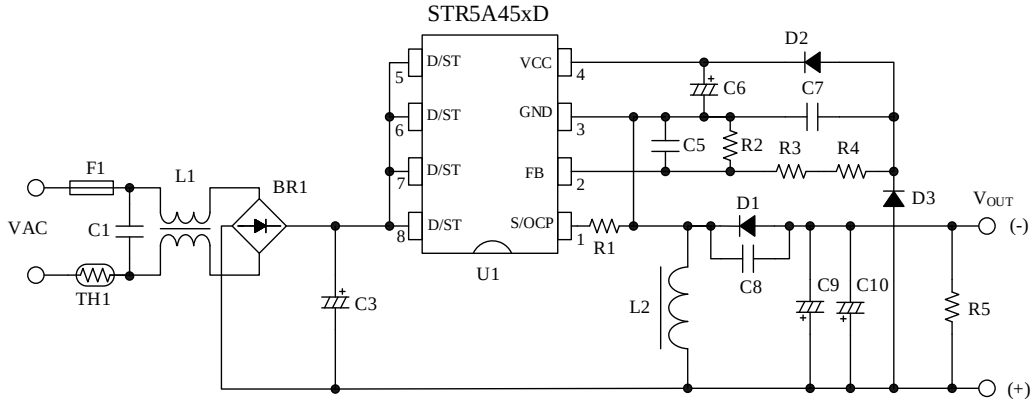


Figure 7-2. Inverting Converter

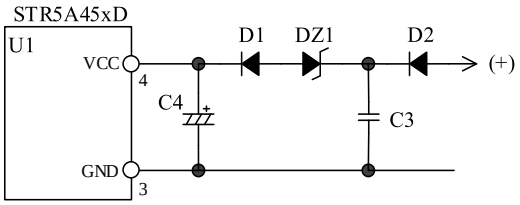


Figure 7-3. Increasing the Absolute Value of $|V_{OUT}|$


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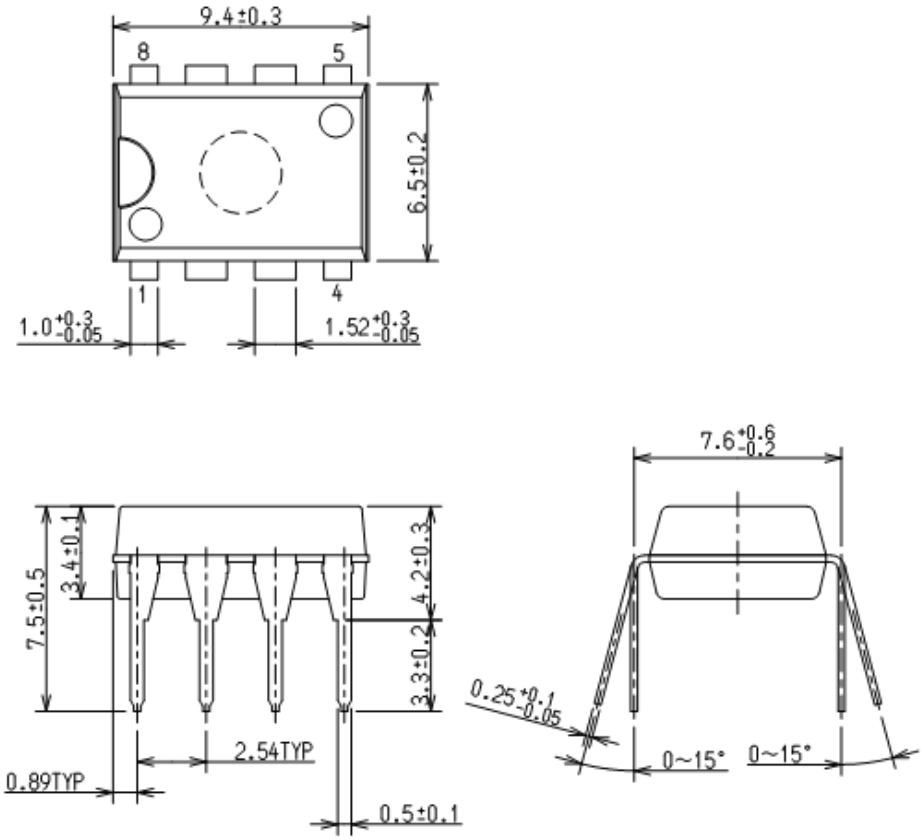
## 8. Physical Dimensions

● DIP8




**NOTES:**

- All dimensions in millimeters
- Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Soldering Iron: 350 °C / 3.5 s, 1 time
  Soldering should be at a distance of at least 1.5 mm from the body of the product.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## 9. Marking Diagram

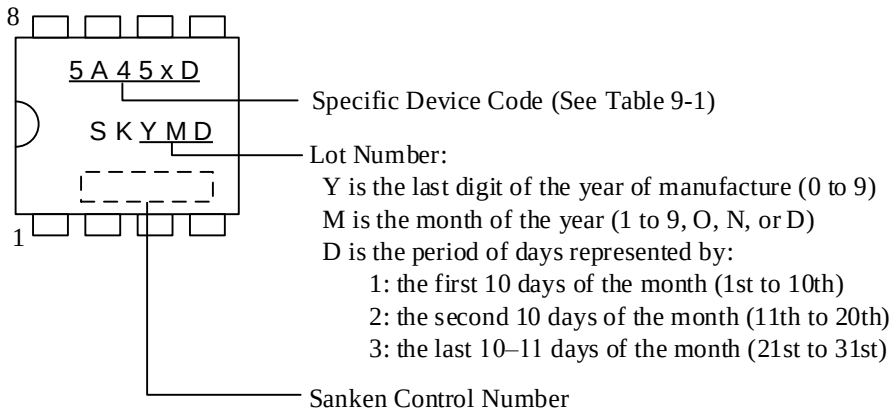


Table 9-1. Specific Device Code

| Specific Device Code | Part Number |
|---|---|
| 5A451D | STR5A451D |
| 5A453D | STR5A453D |


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## 10. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

The common items of Buck converter and Inverting are desribed by using Buck conveter.

### 10.1 Startup Operation of IC

Figure 10-1 shows the circuit around VCC pin.

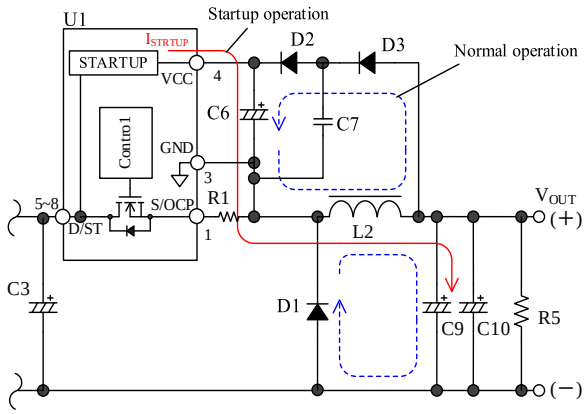


Figure 10-1. VCC Pin Peripheral Circuit in Buck Converter

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches the Startup Circuit Operation Voltage $V_{ST(ON)}$ = 29 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{CC(ST)}$ = −1.7 mA, charges C6 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation.

After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate startup time $t_{START}$ is calculated as follows:

$$t_{START} = C6 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{CC(ST)}|} \text{ (s)} \quad (1)$$

where,

$t_{START}$ is the startup time of IC (s),

$V_{CC(INT)}$ is the initial voltage on VCC pin (V).

When the internal power MOSFET turns off, the output voltage, $V_{OUT}$, charges C6 through D2 and D3 (see Figure 10-1).

The voltage between VCC pin and GND pin in the steady state operation is calculated as follows, where $V_{FD1}$, $V_{FD2}$ and $V_{FD3}$ are the forward voltage of D1, D2 and D3 respectively:

$$V_{CC} = V_{OUT} + V_{FD1} - (V_{FD2} + V_{FD3}) \text{ (V)} \quad (2)$$

### 10.2 Undervoltage Lockout (UVLO)

Figure 10-2 shows the relationship of VCC pin voltage and the circuit current, $I_{CC}$. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation and the circuit current, $I_{CC}$, increases. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.0 V, the control circuit stops its operation by the Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

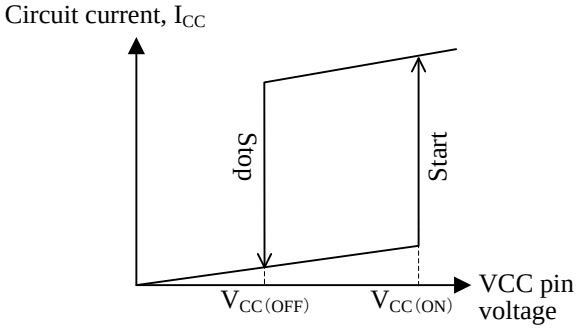


Figure 10-2. Relationship between VCC Pin Voltage and $I_{CC}$

### 10.3 Power Supply Startup and Soft Start Function

The soft start function reduces the voltage and the current stress of the internal power MOSFET and the freewheeling diode, D1.

Figure 10-3 shows the startup waveforms. After the IC starts, during the Standby Blanking Time at Startup, $t_{STB(INH)}$, the burst oscillation mode is disabled to operate the soft start.

The IC activates the soft start circuitry during the startup period. The soft start time is fixed to about 10.2 ms. During the soft start period, the overcurrent threshold is increased step-wisely (7 steps). The IC operates switching operation by the frequency responding to FB pin voltage until the output reaches the setting voltage.

Here, the $t_{LIM}$ is defined as the period until FB pin voltage reaches 1.6 V after the IC starts. When the $t_{LIM}$ reaches the OLP Delay Time at Startup, $t_{OLP}$, of 70 ms and


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more, the IC stops switching operation. Thus, it is necessary to adjust the value of output electrolytic capacitor, C9 and C10, so that the $t_{LIM}$ is less than $t_{OLP}$.

If VCC pin voltage reaches $V_{CC(OFF)}$ and a startup failure occurs as shown in Figure 10-4, increase C6 value or decrease C9 and C10 value. Since the larger capacitance causes the longer startup time of IC, it is necessary to check and adjust the startup process based on actual operation in the application.

Since the leading edge blanking function (See Section 10.5) is disabled during the soft start period, the on-time may be less than the Leading Edge Blanking Time ($t_{BW}$ = 280 ns).

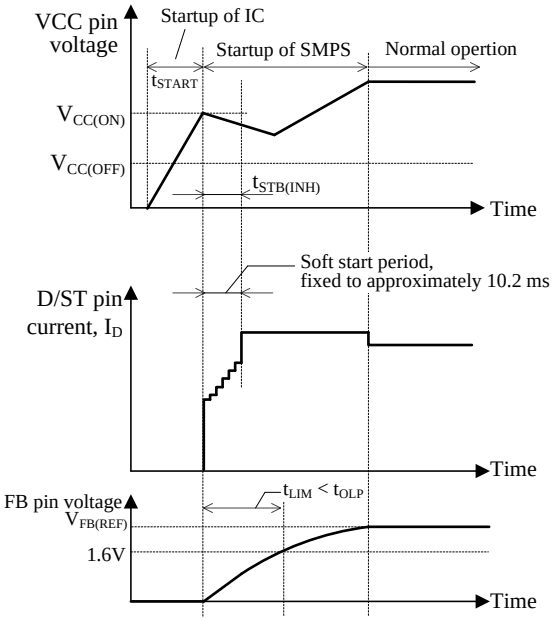


Figure 10-3. Startup Waveforms

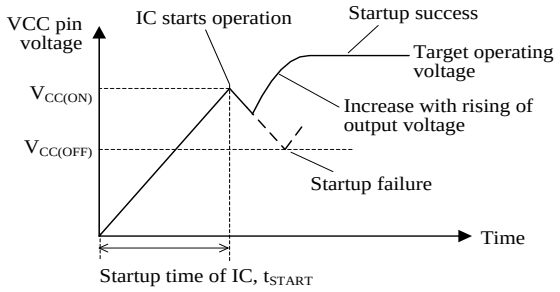


Figure 10-4. VCC Pin Voltage During Startup Period

## 10.4 Constant Voltage (CV) Control

The constant voltage (CV) control for power supply output adopts the peak-current-mode control method which enhances the response speed and the stable operation.

The IC controls the peak value of the voltage of a current detection resistor, R1, to be close to target voltage ($V_{SC}$), comparing $V_{ROCP}$ with $V_{SC}$ by internal FB comparator. Feedback Control circuit receives the target voltage, $V_{SC}$, reversed FB pin voltage by an error amplifier (see Figure 10-5 and Figure 10-6).

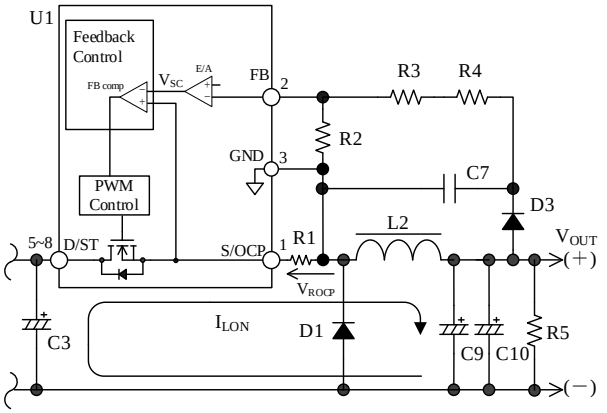


Figure 10-5. FB Pin Peripheral Circuit in Buck Converter

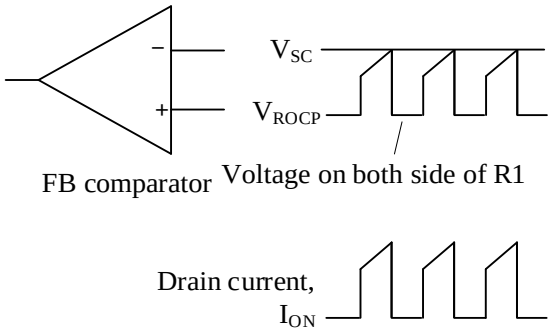


Figure 10-6. Drain Current $I_D$ and FB Comparator in Steady State Operation

- Decreasing Load
  When the output load decreases, the FB pin voltage increases in response to the increase of the output voltage. Since $V_{SC}$ which is the output voltage of internal error amplifier becomes low, the peak value of $V_{ROCP}$ is controlled to become low, and the peak of the drain current decreases. This control prevents the output voltage from increasing.

- Increasing Load
  When the output load increases, the control circuit operates the reverse of the former operations. Since $V_{SC}$ becomes high, the peak drain current increases. This control prevents the output voltage from decreasing.


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### 10.4.1 Buck Converter Operation

Figure 10-7 shows the output current path in the Buck converter. Figure 10-8 shows the operational waveforms.

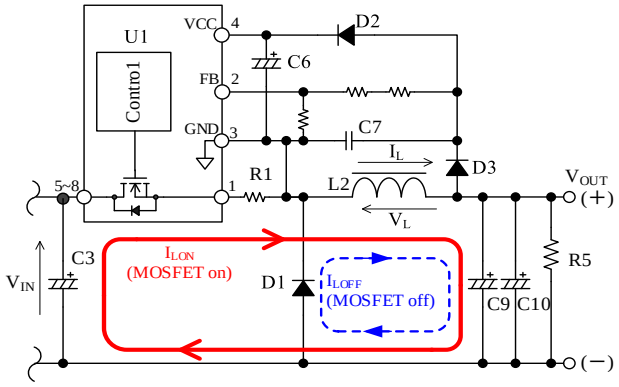


Figure 10-7. Output Current Path in Buck Converter

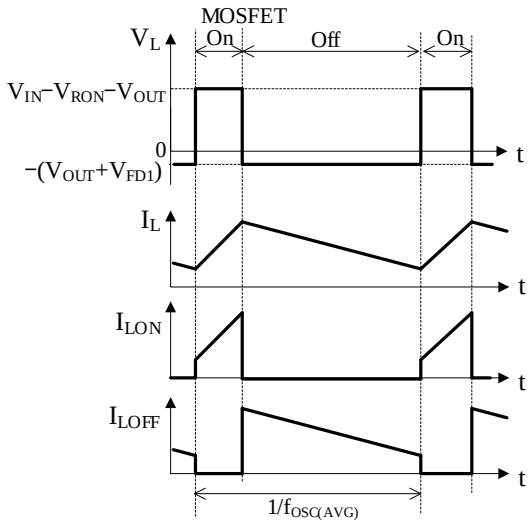


Figure 10-8. Operational Waveforms in Buck Converter

In the Buck converter, the PWM control is described in the following.

1) PWM On-time Period
When the internal power MOSFET turns on, the $I_{LON}$ current flows as shown in Figure 10-7, and the inductor, L2, stores some energy.
Since the $I_{LON}$ flows through the current detection resistor, R1, the voltage of R1 is detected as the current detection voltage, $V_{ROCP}$.
FB pin voltage is the voltage divided C7 voltage by voltage dividing resistors, and the target voltage, $V_{SC}$, is given by FB pin voltage.
When $V_{ROCP}$ reaches $V_{SC}$, the power MOSFET turns off.

2) PWM Off-time Period
When the internal power MOSFET turns off, the back electromotive force occurs in the inductor, L2, the freewheeling diode, D1, is forward biased and turns on. Thus, the $I_{LOFF}$ current flows as shown in Figure 10-7. As shown in Figure 10-8, after the average switching period, $1/f_{OSC(AVG)}$, the power MOSFET turns on again, and the event moves to the previous 1).

The output current is equal to the average inductor current of L2.

### 10.4.2 Inverting Converter Operation

Figure 10-9 shows the output current path in the Inverting converter. Figure 10-10 shows the operational waveforms.

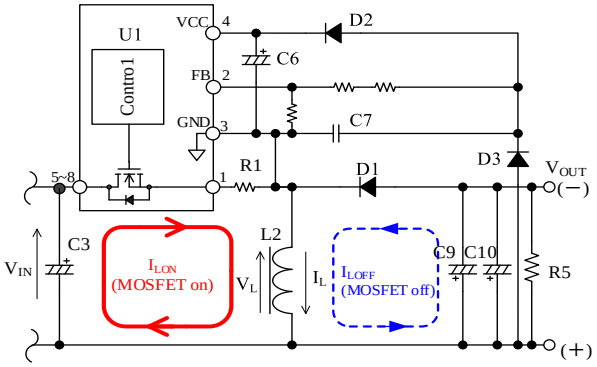


Figure 10-9. Output Current Path in Inverting Converter

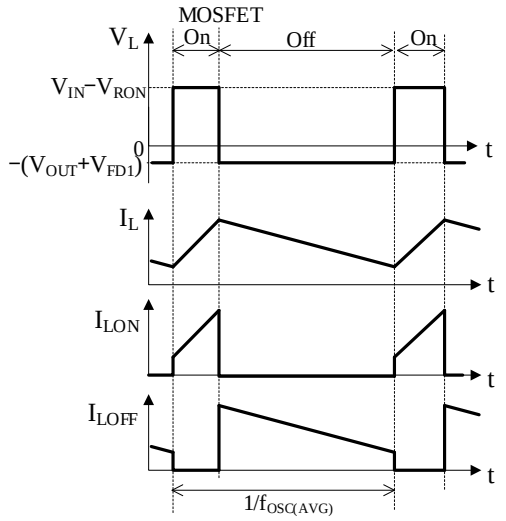


Figure 10-10. Operational Waveforms in Inverting Converter


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In the Inverting converter, the PWM control is described in the following.

1) PWM On-time Period
When the internal power MOSFET turns on, the $I_{LON}$ current flows as shown in Figure 10-9, and the inductor, L2, stores some energy.
Since the $I_{LON}$ flows through the current detection resistor, R1, the voltage of R1 is detected as the current detection voltage, $V_{ROCP}$.
FB pin voltage is the voltage divided C7 voltage by voltage dividing resistors, and the target voltage, $V_{SC}$, is given by FB pin voltage.
When $V_{ROCP}$ reaches $V_{SC}$, the power MOSFET turns off.

2) PWM Off-time Period
When the internal power MOSFET turns off, the back electromotive force occurs in the inductor, L2, the freewheeling diode, D1, is forward biased and turns on. Thus, the $I_{LOFF}$ current flows as shown in Figure 10-9
As shown in Figure 10-10, after the average switching period, $1/f_{OSC(AVG)}$, the power MOSFET turns on again, and the event moves to the previous 1).

The output current is equal to the average current of $I_{LOFF}$ of L2.

## 10.5 Leading Edge Blanking Function

The constant voltage control for power supply output adopts the peak-current-mode control method. The peak drain current is detected by the current detection resistor, R1. Just in turning on the internal power MOSFET, the steep surge current would occur.

If the overcurrent protection (OCP) responds to the voltage caused by that surge current, the power MOSFET may be turned off.

To prevent that response, the OCP threshold voltage increases during Leading Edge Blanking ($t_{BW}$ = 280 ns) just after the power MOSFET turns on, and this prevents the OCP detection from responding to the surge voltage in turning-on (see Section 10.8.1).

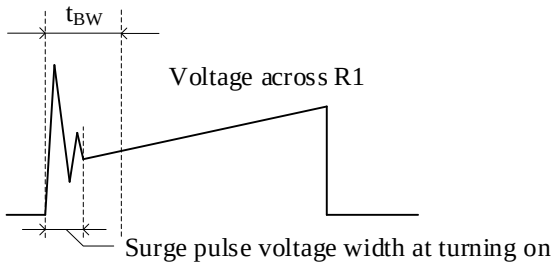


Figure 10-11. Leading Edge Blanking

## 10.6 Random Switching Function

The switching frequency is randomly modulated by superposing the modulating frequency on $f_{OSC(AVG)}$. This function reduces the conduction noise compared with other products without this function, and simplifies noise filtering of the input lines of power supply.

## 10.7 Operation Mode

As shown in Figure 10-12, when the output power is decreasing, together with the decrease of the drain current $I_D$ of the internal power MOSFET, the operation mode is automatically changed to the fixed switching frequency mode (60 kHz), to the green mode controlled the switching frequency (23 kHz to 60 kHz), and to the burst oscillation mode controlled by an internal oscillator. In the green mode, the number of switching is reduced. In the burst oscillation mode, the switching operation is stopped during a constant period. Thus, the switching loss is reduced, and the power efficiency is improved (see Figure 10-13).

When the output load becomes lower, FB pin voltage increases and S/OCP pin voltage decreases. The S/OCP pin voltage reaches to the S/OCP pin standby threshold voltage, $V_{OCP(STB)}$ = 0.11 V, the burst oscillation mode is activated.

As shown in Figure 10-13, the burst oscillation mode consists of the switching period and the non-switching period. The oscillation frequency during the switching period is the Minimum Frequency of about 23 kHz.

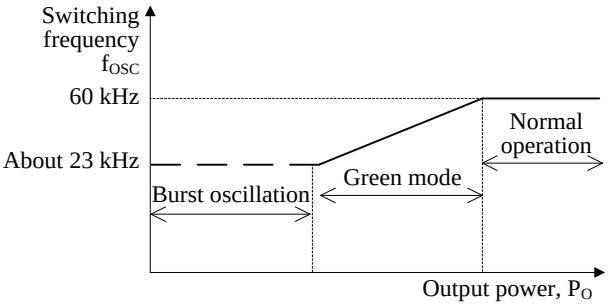


Figure 10-12. Switching Frequency in Response to $P_O$

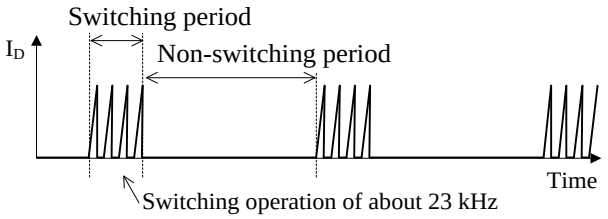


Figure 10-13. Switching Waveform at Burst Oscillation Mode


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## 10.8 Overcurrent Protection (OCP)

### 10.8.1 OCP Operation

The overcurrent protection (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the voltage on the current detection resistor, R1, reaches to OCP threshold voltage.

During Leading Edge Blanking Time shown in Figure 10-11, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.61 V which is higher than the normal OCP threshold voltage. Changing to this threshold voltage prevents the OCP detection from responding to the surge voltage in turning-on the power MOSFET. This function operates as protection at the condition including output shorted.

When the power MOSFET turns on, the surge voltage width of the S/OCP pin should be less than $t_{BW}$. To prevent surge voltage, pay extra attention to R1 trace layout (See Section 11.3).

### 10.8.2 OCP Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to $V_{OCP}$. Thus, the peak current has some variation depending on AC input voltage in OCP state. To reduce the variation of peak current in OCP state, the input compensation function is built-in.

This function compensates the OCP threshold voltage so that it depends on AC input voltage, as shown in Figure 10-14.

When AC input voltage is low, the OCP threshold voltage is controlled to become high. Thus this control reduces the difference of peak drain current between at low AC input voltage and at high.

When the on-time is 6 µs or more, the OCP threshold voltage is $V_{OCP(H)}$ of 0.83 V. When the on-time is less than 6 µs, that is $V_{OCP}$ shown in Equation (3).

$$V_{OCP} = V_{OCP(L)} + DPC \times 10^3 \times ONTime \quad (3)$$

Where,
$V_{OCP(L)}$: OCP Threshold Voltage at Zero Duty Cycle (V)
DPC: OCP Compensation Coefficient (mV/µs)
ONTime: On-time of power MOSFET (µs)

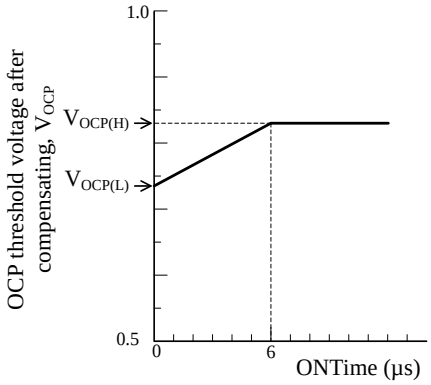


Figure 10-14. Relationship between ONTime and OCP Threshold Voltage after Compensating

## 10.9 Overload Protection (OLP)

When the voltage on the current detection resistor, R1, reaches the OCP threshold voltage, the internal power MOSFET turns off. Figure 10-15 shows the characteristic of output voltage and current.

The output voltage decreases in the overload state, and FB pin voltage also decreases. When the period keeping FB pin voltage less than 1.6 V continues for OLP Delay Time at Startup, $t_{OLP}$ = 70 ms, the overload protection (OLP) is activated, and the IC stops switching operation. Thus, VCC pin voltage decreases to $V_{CC(OFF)}$, and the control circuit stops operation. After that, the startup circuit is activated, VCC pin voltage increases to $V_{CC(ON)}$ by the startup current, and the control circuit operates again. Thus, the intermittent operation by UVLO is repeated in the OLP state (see Figure 10-16).

This intermittent operation reduces the stress of parts including the power MOSFET and the freewheeling diode. In addition, this operation reduces power consumption because the switching period in this intermittent operation is much shorter than the oscillation stop period.

When the abnormal condition is removed, the IC returns to normal operation automatically.

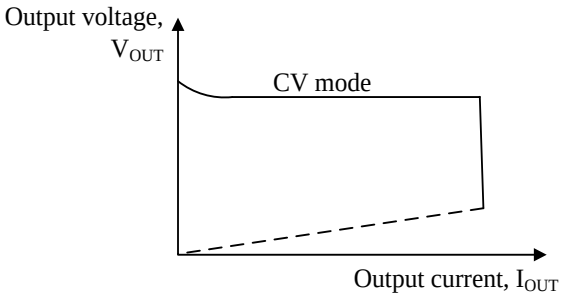


Figure 10-15. Overload Characteristics


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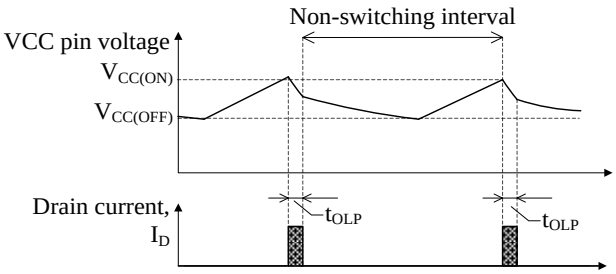


Figure 10-16. OLP Operational Waveform

## 10.10 Overvoltage Protection (OVP)

When the voltage between VCC pin and GND pin increases to $V_{CC(OVP)}$ = 29.3 V or more, the overvoltage Protection (OVP) is activated and the IC stops switching operation. The intermittent operation by UVLO is repeated in the OVP state. See Section 10.9 about the intermittent operation by UVLO.

When the abnormal condition is removed, the IC returns to normal operation automatically.

The approximate value of output voltage $V_{OUT(OVP)}$ in the OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = V_{CC(OVP)} + V_{FD2} + V_{FD3} - V_{FD1} \quad (4)$$

where,
$V_{OUT(OVP)}$ is voltage of between $V_{OUT}$(+) and $V_{OUT}$(−),
$V_{FD1}$ is the forward voltage of D1 in Figure 10-1,
$V_{FD2}$ is the forward voltage of D2, and
$V_{FD3}$ is the forward voltage of D3.

## 10.11 Thermal Shutdown (TSD)

Figure 10-17 shows the thermal shutdown (TSD) operational waveforms.

When the junction temperature of the IC control circuit increases to $T_{J(TSD)}$ = 135 °C (min.) or more, the TSD is activated, and the IC stops switching operation. The TSD has a temperature hysteresis. When VCC pin voltage decreases to about 9.4 V during the $T_J > (T_{J(TSD)}-T_{J(TSD)HYS})$, the startup circuit supplies startup current to VCC pin to keep the VCC pin voltage > $V_{CC(OFF)}$.

When the junction temperature is $T_{J(TSD)}-T_{J(TSD)HYS}$ or less, the startup circuit stops the startup current supply. Then, VCC pin voltage decreases to $V_{CC(OFF)}$ or less, and the control circuit stops operation. After that, the startup circuit is activated, VCC pin voltage increases to $V_{CC(ON)}$ by the startup current, and the control circuit operates again. The intermittent operation by TSD and UVLO is repeated in the TSD state.

After the fault condition is removed, the IC returns to normal operation automatically.

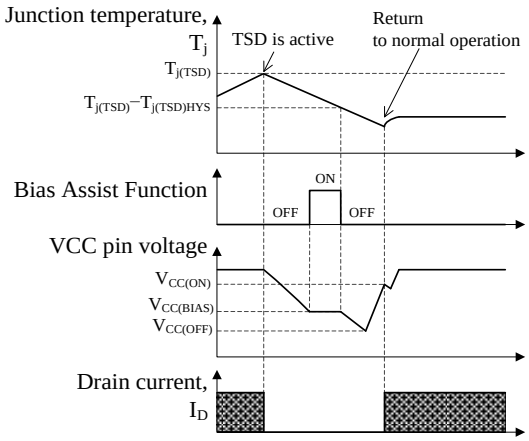


Figure 10-17. TSD Operational Waveforms

# 11. Design Notes

## 11.1 External Components

Take care to use properly rated, including derating as necessary, and proper type of components.

Figure 11-1 shows the peripheral circuit of IC in Buck converter.

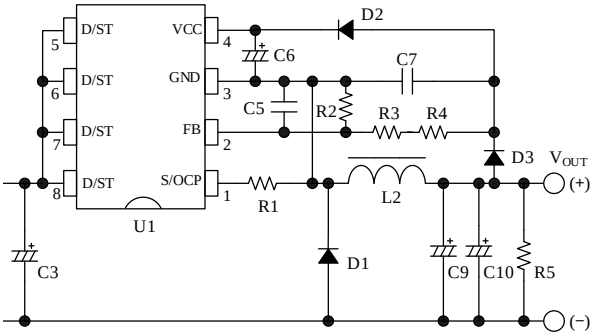


Figure 11-1. Peripheral Circuit of IC in Buck Converter


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### 11.1.1 Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise.

The value of output electrolytic capacitor, C9 and C10, should be fulfilled the following conditions:

- The specification of output ripple
- Enough shorter output voltage rising time in startup than the OLP Delay Time at Startup, $t_{OLP}$ = 70 ms.
- Low impedance types, designed for switch mode power supplies, is recommended.

The ESR of C9 and C10 should be set in the range of Equation (5).

$$Z_{CO} < \frac{\Delta V_{OR}}{I_{LRP}} \quad (5)$$

where,
$Z_{CO}$ is the ESR of electrolytic capacitor at the operation frequency (Since the ESR in general catalogs is mostly measured at 100 kHz, check the frequency characteristic.),
$\Delta V_{OR}$ is the output ripple voltage specification, and
$I_{LRP}$ is the ripple current of inductor.

### 11.1.2 Inductor

Apply proper design margin to core temperature rise by core loss and copper loss.

The inductor should be designed so that the inductor current does not saturate. The inductance should be the minimum considered a negative tolerance of inductance and a decline of DC superposition characteristics.

The on-time must be longer than the Leading Edge Blanking Time to control the output voltage constantly.

In the universal input voltage design, the on-time is easy to become short in the condition of maximum AC input voltage and light load. Be careful not to choose too small value for the inductance (The recommended value is 100 µH or more).

Refer to the following design example of how to the inductor setting of the buck converter.

- DEE0010 Design Example Using STR5A453D: 10.5 W (15 V, 0.7 A) Offline Buck Converter https://www.semicon.sanken-ele.co.jp/common/pdf/designexample/dee0010.pdf

### 11.1.3 VCC Pin Peripheral Circuit

The reference value of C6 in Figure 11-1 is generally 10 to 47 µF. See Section 10.1 about the startup time.

### 11.1.4 FB Pin Peripheral Circuit

As shown in Figure 11-1, FB pin is input the voltage divided the voltage between $V_{OUT}$(+) and GND pin by resistors.

C7 is the smoothing capacitor. The value of C7 depends on the value of output electrical capacitor, 9 and C10. Usually the value of C7 is 0.22 µF to 4.7 µF. When C7 value is set larger, the line regulation becomes better, however, the dynamic response of the output voltage becomes worse. Be careful of that value.

The voltage dividing resistor of R2, R3 and R4 is determined by the reference voltage, $V_{FB(REF)}$ = 2.50 V, the output voltage, $V_{OUT}$, and so on. The following Equation (6) shows the relationship of them.

The target value of R2 is about 10 kΩ to 22 kΩ. R3 and R4 should be adjusted in actual operation condition.

The $V_F$ of D1 and D3 affects the output voltage. Thus, the diodes of low $V_F$ should be selected.

$$|V_{OUT}| \cong V_{FB(REF)} \times \frac{R2 + R3 + R4}{R2} + V_{FD3} - V_{FD1}$$

$$\Rightarrow R3 + R4 = \left( \frac{|V_{OUT}| - V_{FD3} + V_{FD1}}{V_{FB(REF)}} - 1 \right) \times R2 \quad (6)$$

where,
$V_{FD1}$ is the forward voltage of D1, and
$V_{FD3}$ is the forward voltage of D3.

### 11.1.5 Freewheeling Diode

D1 in Figure 11-1 is the freewheeling diode.

When the internal power MOSFET turns on, the recovery current flows through D1. The current affects power loss and noise much. The $V_F$ affects the output voltage. Thus, the diode of fast recovery and low $V_F$ should be selected.

### 11.1.6 Bleeder Resistance

For light load application, the bleeder resistor, R5, in Figure 11-1 should be connected to both ends of output capacitor, C9 and C10, to prevent the increase of output voltage.

The value of R5 should be satisfied with Equation (7), and should be adjusted in actual operation condition.

$$R5 \leq \frac{|V_{OUT}|}{3mA} \quad (7)$$


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## 11.2 D/ST Pin

When the voltage or the current of the D/ST pins shown in
Figure 11-1 exceeds the Absolute Maximum Ratings, the internal power MOSFET connected to the D/ST pin would be permanently damaged.

## 11.3 PCB Trace Layout

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.
In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.
Figure 11-2 and Figure 11-3 show the circuit design example.

1) Main Circuit Trace Layout
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

2) Freewheeling Loop Layout
This is the trace for the current of freewheeling diode, D3, and thus it should be as wide trace and small loop as possible.

3) Control Ground Trace Layout
Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at single point grounding.

4) VCC Trace Layout
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C6 and the IC are distant from each other, placing a capacitor such as film capacitor $C_f$ (about 0.1 µF to 1.0 µF) close to the VCC pin and the GND pin is recommended.

5) FB Trace Layout
The divided voltage by R3+R4 and R2 of output voltage is input to the FB pin.
To increase the detection accuracy, R4 and R2 should be connected to the bottom of C7 and the GND pin, respectively. The trace between R2, R3 and the FB pin should be as short as possible.

6) Thermal Considerations
Since the internal power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
Since the copper area under the IC and the GND pin trace act as a heatsink, its traces should be as wide as possible.

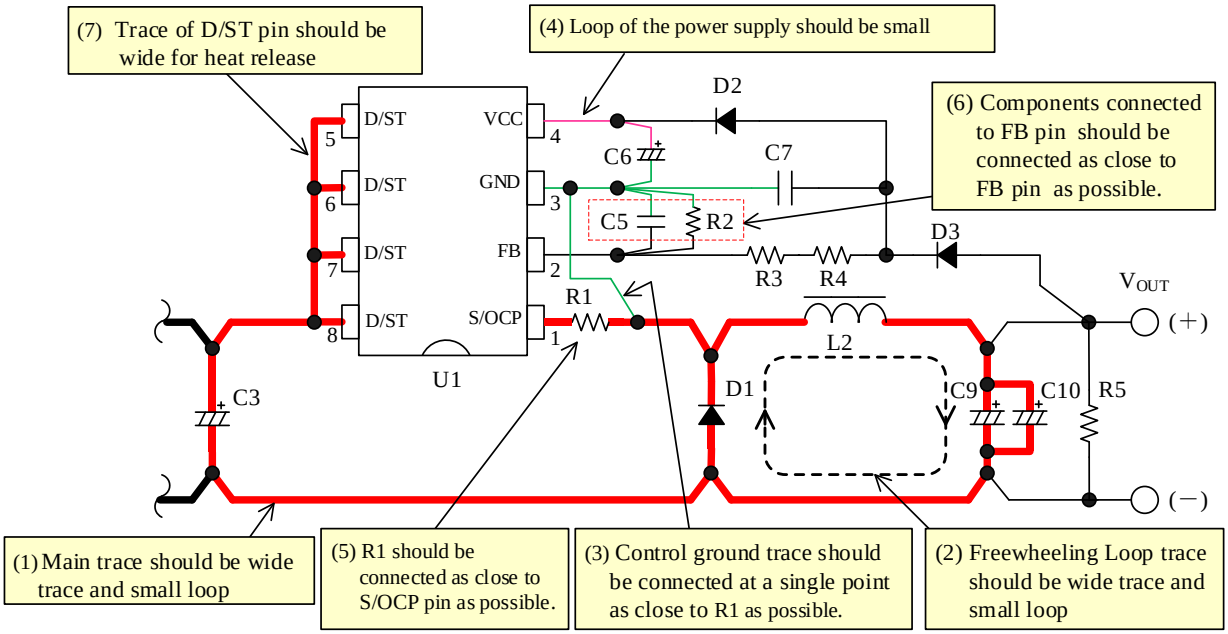


Figure 11-2 Peripheral Circuit Example Around IC for Buck Converter


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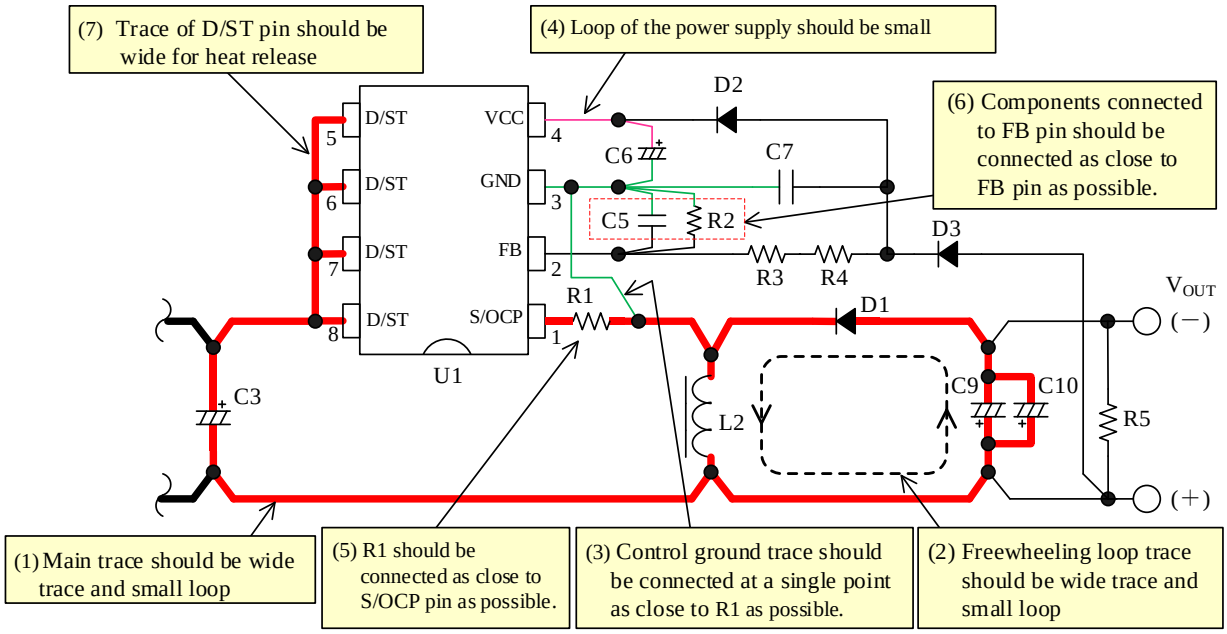


Figure 11-3 Peripheral Circuit Example Around IC for Inverting Converter


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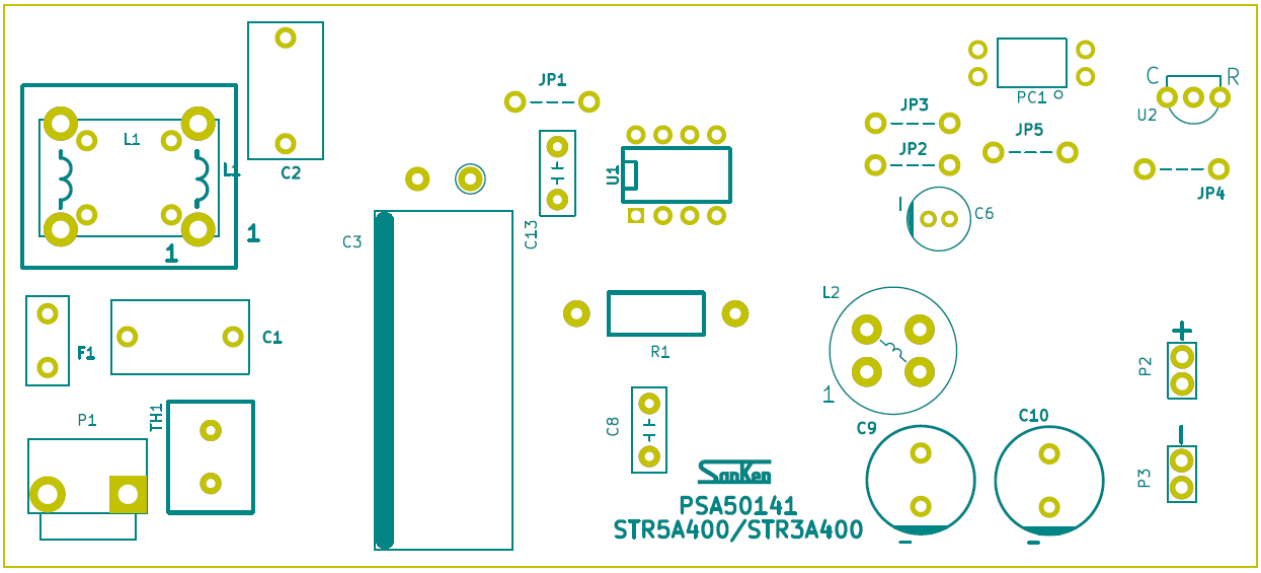
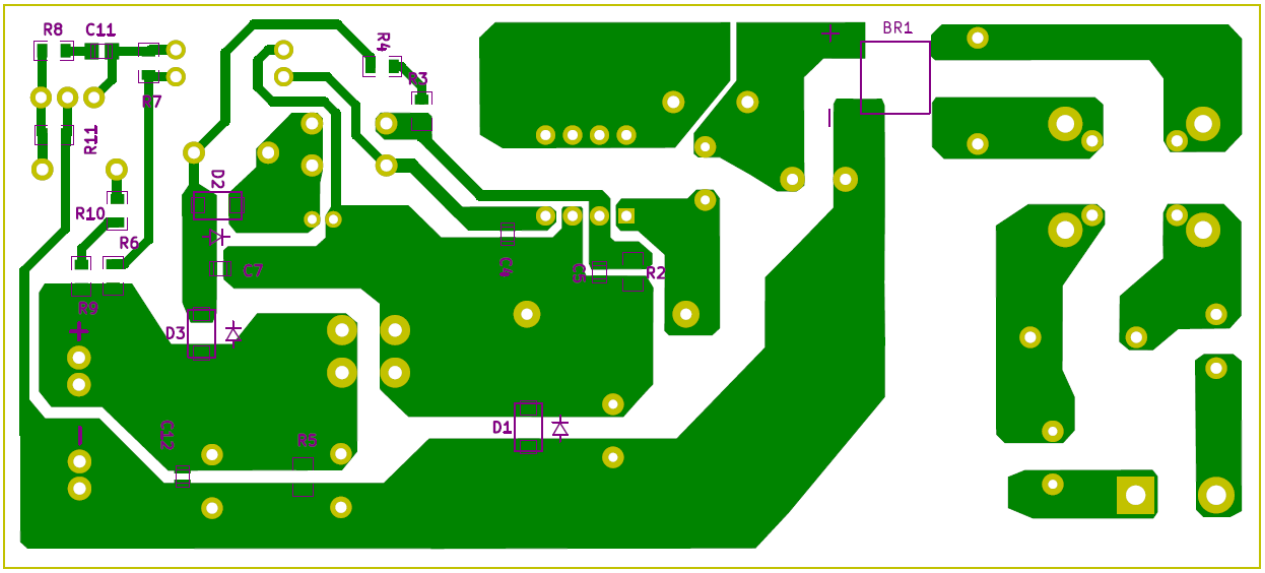
## 12. Pattern Layout Example (Buck Converter)

The following show the pattern layout example and the circuit schematic for the buck converter using STR5A45xD. The design example uses only the parts listed in the circuit diagram and the bill of materials.

PCB dimensions: 65 mm × 24 mm




(a) Top View




(b) Bottom View

Figure 12-1. Pattern Layout Example for Buck Converter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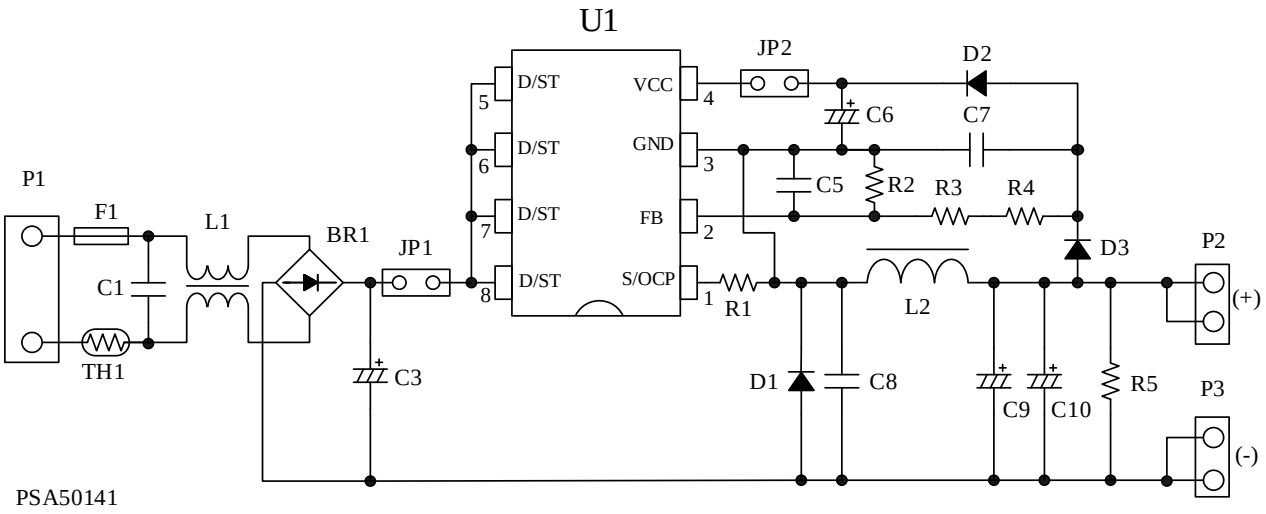


Figure 12-2. Circuit Diagram for Buck Converter


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## 13. Design Example

The following show the power supply specification, the circuit schematic, and the bill of materials of the buck converter reference design.

- Power Supply Specification

| | |
|---|---|
| IC | STR5A453D |
| Input voltage | AC 85 V to AC 265 V |
| Maximum output power | 10.5 W (max.) |
| Output voltage | 15 V |
| Output current | 0.7 A |

- Circuit Diagram

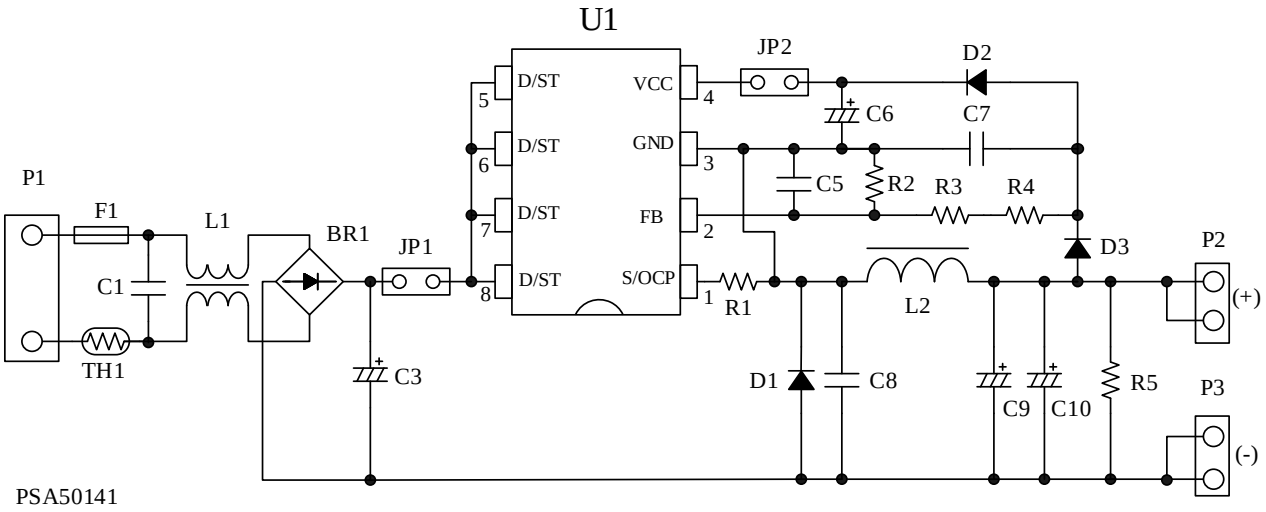


Figure 13-1. Circuit Diagram for Buck Converter


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● Bill of Materials

| Part Symbol | Part Type | Ratings | Recommended Sanken Parts |
|---|---|---|---|
| F1 | Hues | 250 V, 2 A | |
| TH1 | Power thermistor | 4.7 Ω, 3 A | |
| C1 | Film capacitor | 310 VAC, 0.1 µF | |
| C3 | Electrolytic capacitor | 105 °C, 400 V, 56 µF | |
| C5 | Chip ceramic capacitor | 50 V, 470 pF, 2012 | |
| C6 | Electrolytic capacitor | 105 °C, 50 V, 22 µF | |
| C7 | Chip ceramic capacitor | 50 V, 2.2 µF, 2012 | |
| C8 | Ceramic capacitor | 1 kV, 22 pF | |
| C9 | Electrolytic capacitor | 105 °C, 25 V, 470 µF | |
| C10 | Electrolytic capacitor | 105 °C, 25 V, 470 µF | |
| BR1 | Bridge rectifier diode | 1000 V, 1.5 A | |
| D1 | Fast recovery diode | 500 V, 3 A | SJPD-L5 |
| D2 | Schottky diode | 90 V, 1 A | SJPB-D9 |
| D3 | Fast recovery diode | 500 V, 1 A | SJPD-D5 |
| L1 | CM inductor | 18 mH, 0.3 A | |
| L2 | Inductor | 220 µH, 2.1 A | |
| R1 | Resistor | 1 W, 0.47 Ω | |
| R2 | Chip resistor | 10 kΩ, 1/8 W, 1608 | |
| R3 | Chip resistor | 47 kΩ, 1/8 W, 1608 | |
| R4 | Chip resistor | 4.7 kΩ, 1/8 W, 1608 | |
| R5 | Chip resistor | 6.8 kΩ, 1/8 W, 1608 | |
| U1 | PWM offline converter IC | 650 V, 1.9 Ω | STR5A453D |
| JP1 | Jumper wire | Plated wire, φ = 0.6, P = 7 mm | |
| JP2 | Jumper wire | Plated wire, φ = 0.6, P = 7 mm | |
| P1 | Connector | 250 V | |
| P2 | Connector | 50 V | |
| P3 | Connector | 50 V | |
| — | PCB | PSA50141 | |


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