Primary Side Regulation
Off-Line PWM Controllers with Integrated Power MOSFET

STR5A100D Series

General Descriptions

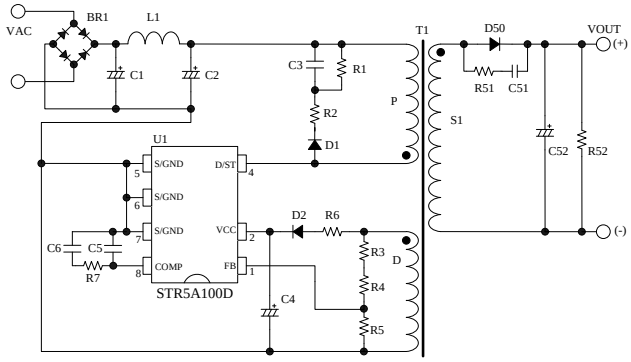
The STR5A100D series is power IC with primary side regulation for switching power supplies, incorporating a sense MOSFET and a current mode PWM controller IC.

Employing the Primary Side Regulation, the product achieves power supply systems with few external components. Including a startup circuit and a standby function in the controller, the product achieves the low standby power by the automatic switching between the PWM operation in normal operation and the burst-oscillation under light load conditions. The rich set of protection features helps to realize low component counts, and high performance-to-cost power supply.

Features

- Primary Side Regulation
- Constant Voltage (CV), Constant Current (CC) Control
- Auto Standby Function
  No Load Power Consumption < 30mW
- Operation Mode
  - Normal Operation ---------- PWM Mode
  - Light Load Operation ---------- Green-Mode
  - Standby ---------- Burst Oscillation Mode
- Build-in Startup Circuit
  (reducing power consumption at standby operation, shortening the startup time)
- Current Mode Type PWM Control
- Random Switching Function
- Leading Edge Blanking Function
- Soft Start Function (reducing the stress of power MOSFET and secondary side rectifier diode at startup)
- Protections
  Overcurrent Protection (OCP) ---------- Pulse-by-Pulse
  Overvoltage Protection (OVP) ---------- Auto-Restart
  Thermal Shutdown Protection (TSD) ----- Auto-Restart

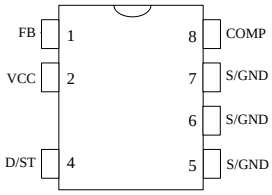
Typical Application Circuit



Package

DIP8





Not to scale

Lineup

- Electrical Characteristics
  $V_{D/ST}$(max.) = 730 V
  $f_{OSC(AVG)}$(typ.) = 65 kHz

Products	$R_{DS(ON)}$ (max.)	$I_{DLIM(H)}$
STR5A162D	24.6 Ω	0.285 A
STR5A164D	13 Ω	0.41 A

- Output Power, P_{OUT}*

Products	Adapter		Open frame	
	AC230V	AC85 ~265V	AC230V	AC85 ~265V
STR5A162D	4 W	3.5 W	5 W	4.5 W
STR5A164D	6.0 W	5.5 W	8.5 W	7 W

* The EI-16 core of transformer is assumed. The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, ON Duty, and thermal design affect the output power. It may be less than the value stated here.

Applications

- White Goods
- Other SMPS

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1. Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A is 25 °C, 5 pin = 6 pin = 7 pin

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Remarks
FB Pin Voltage	V_{FB}		1 – 5	7.0	V	
FB Pin Source Current	I_{FB}	Single pulse	1 – 5	− 10	mA	
VCC Pin Voltage	V_{CC}		2 – 5	− 0.3 to 32	V	
D/ST Pin Voltage	$V_{D/ST}$		4 – 5	− 0.3 to 730	V	
Drain Peak Current	I_{DP}	Positive: Single pulse Negative: Within 2µs of pulse width	4 – 5	− 0.2 to 0.69	A	5A162D
				− 0.2 to 0.97	A	5A164D
COMP Pin Voltage	V_{COMP}		8 – 5	− 0.3 to 7.0	V	
Power Dissipation(1)	P_D	(2)	–	1.53	W	
Operating Ambient Temperature	T_{OP}		–	− 40 to 125	°C	
Storage Temperature	T_{stg}		–	− 40 to 125	°C	
Junction Temperature	T_j		–	150	°C	

(1) Refer to MOSFET Temperature versus Power Dissipation Curve
(2) When embedding this hybrid IC onto the printed circuit board (cupper area in a 15mm×15mm)

2. Recommended Operating Conditions

Recommended operating conditions means the operation conditions maintained normal function shown in electrical characteristics.

Parameter	Symbol	Min.	Max.	Units	Remarks
D/ST Pin Voltage in Operation	$V_{D/ST(OP)}$	− 0.3	584	V	
VCC Pin Voltage in Operation	$V_{CC(OP)}$	11	27	V	

3. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A is 25 °C, $V_{D/ST}$ = 10 V, pin = 6 pin = 7 pin

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		2 – 5	13.6	15.0	16.6	V	
Operation Stop Voltage	$V_{CC(OFF)}$		2 – 5	7.3	8.1	8.9	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	2 – 5	–	–	2.5	mA	
Startup Circuit Operation Voltage	$V_{STARTUP}$	V_{CC} = 13.5 V	4 – 5	19	29	39	V	
Startup Current	$I_{STARTUP}$	V_{CC} = 13.5 V $V_{D/ST}$ = 100 V	2 – 5	− 3.7	− 2.1	− 0.9	mA	
PWM Operation								
Average Switching Frequency	$f_{OSC(AVG)}$	V_{COMP} = 5.5 V	4 – 5	57	65	73	kHz	
Frequency Modulation Deviation	Δf		4 – 5	–	2.8	–	kHz	

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Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
Feedback Reference Voltage	$V_{FB(REF)}$		1 – 5	2.45	2.50	2.55	V	
Feedback Current	$V_{FB(OP)}$	V_{FB} = 2.4 V	1 – 5	− 2.4	− 0.8	–	µA	
Minimum Sampling Time	t_{FBMS}		1 – 5	–	–	2.2	µs	
Standby Operation Threshold Voltage	V_{STBOP}		8 – 5	1.7	2.3	3.1	V	5A162D
				1.3	2.0	2.7	V	5A164D
Standby Operation Cycle	T_{STBOP}		4 – 5	–	1.3	–	ms	
Maximum ON Duty	D_{MAX}		4 – 5	50	57	64	%	
COMP Pin Sink Current	$I_{COMP(SI)}$	V_{COMP} = 5.5 V	8 – 5	–	4.5	–	µA	
COMP Pin Source Current	$I_{COMP(SO)}$	V_{COMP} = 2.5 V	8 – 5	–	– 4.5	–	µA	
Error Amplifier Conductance	gm	V_{FB} = 2.4V to 2.6V	–	–	16	–	µS	
Protection Function								
Leading Edge Blanking Time (1)	t_{BW}		–	–	250	–	ns	
Drain Current Limit Compensation ON Duty(1)	D_{DPC}		–	–	27	–	%	
Drain Current Limit (ON Duty ≥ 27 %)	$I_{DLIM(H)}$		4 – 5	0.250	0.285	0.320	A	5A162D
				0.36	0.41	0.46	A	5A164D
Drain Current Limit (ON Duty = 0 %)	$I_{DLIM(L)}$		4 – 5	0.210	0.242	0.280	A	5A162D
				0.29	0.34	0.39	A	5A164D
OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 5	27.5	29.3	31.3	V	
Constant Current Control Delay Time	t_{CCD}		4 – 5	–	90	–	ms	
Thermal Shutdown Operating Temperature(1)	$T_{j(TSD)}$		–	135	–	–	°C	
Thermal Shutdown Hysteresis(1)	$T_{j(TSDHYS)}$		–	–	70	–	°C	
Power MOSFET								
Drain Leakage Current	I_{DSS}	T_j = 125 °C $V_{D/ST}$ = 584 V	4 – 5	–	–	50	µA	
On Resistance	$R_{DS(ON)}$	I_D = 28.5 mA	4 – 5	–	21.0	24.6	Ω	5A162D
		I_D = 41 mA	4 – 5	–	11	13	Ω	5A164D
Switching Time	t_f		4 – 5	–	–	250	ns	
Thermal Characteristics								
Thermal Resistance Junction to Frame (1)(2)	θ_{j-F}		–	–	–	20	°C/W	
Thermal Resistance Junction to Case(1)(3)	θ_{j-C}		–	–	–	24	°C/W	

(1) Design assurance
(2) Frame temperature (T_F) measured at the root of the 6 pin (S/GND)
(3) Case temperature (T_C) measured at the center of the case top surface

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4. Performance Curves

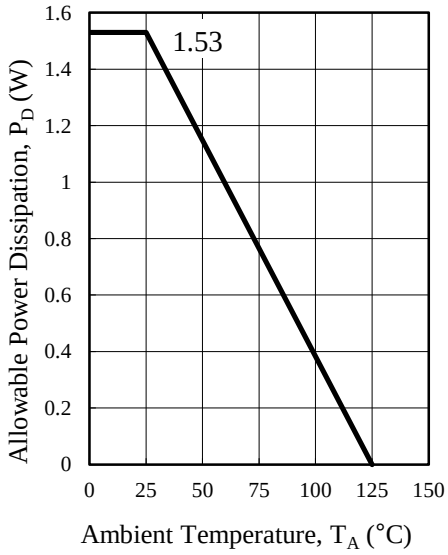

Figure 4-3 Ambient Temperature versus Power Dissipation Curve

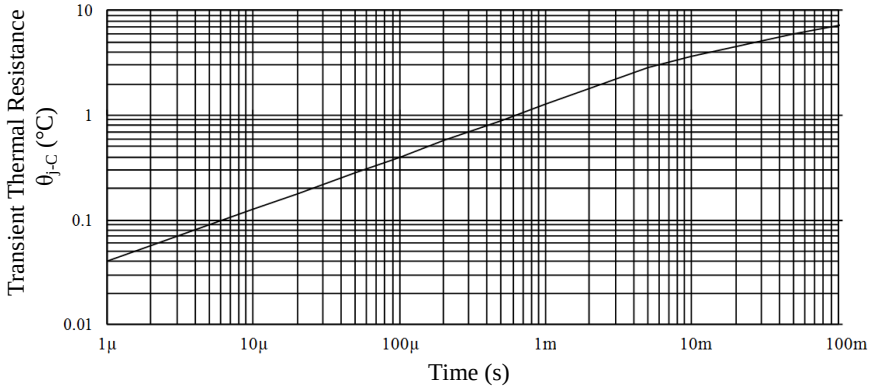

Figure 4-2 STR5A162D Transient Thermal Resistance Curve

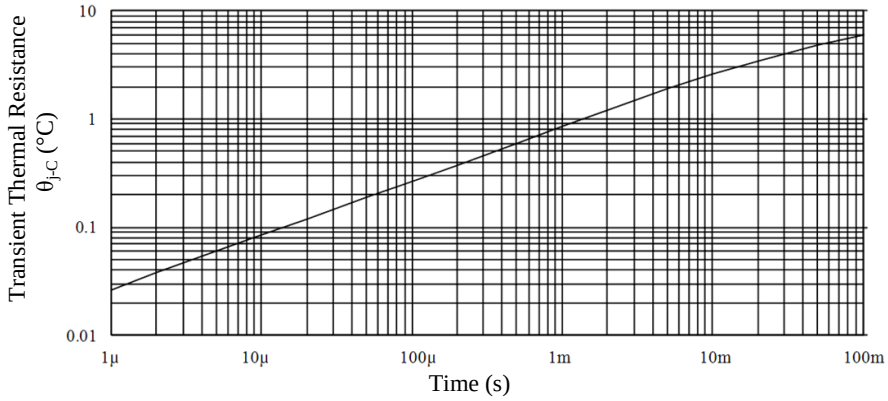

Figure 4-2 STR5A164D Transient Thermal Resistance Curve

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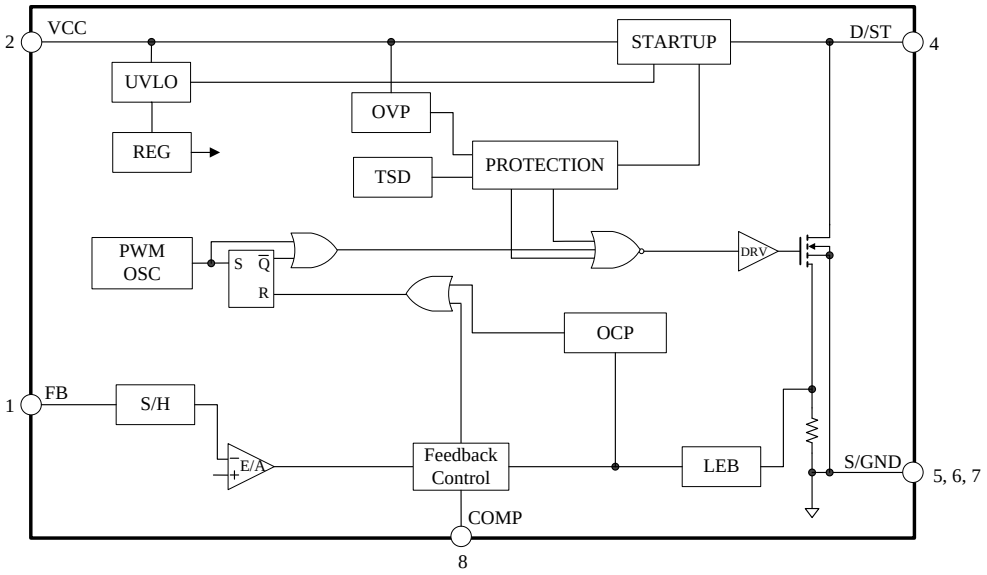
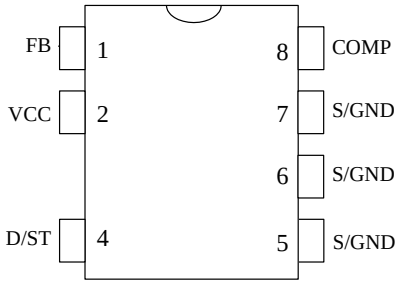
5. Functional Block Diagram

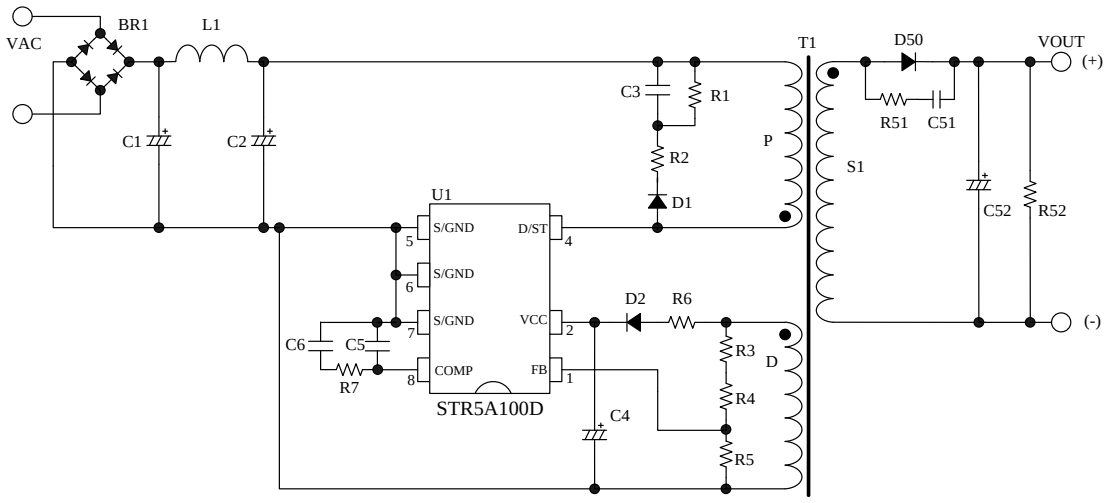


6. Pin Configuration Definitions



Pin	Name	Descriptions
1	FB	Input of constant voltage control signal
2	VCC	Power supply voltage input for Control Part and input of Overvoltage Protection (OVP) signal
3	–	(Pin removed)
4	D/ST	MOSFET Drain and input of startup current
5	S/GND	MOSFET Source and ground
6		
7		
8	COMP	Input of phase compensation

7. Typical Application Circuit



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8. Physical Dimensions

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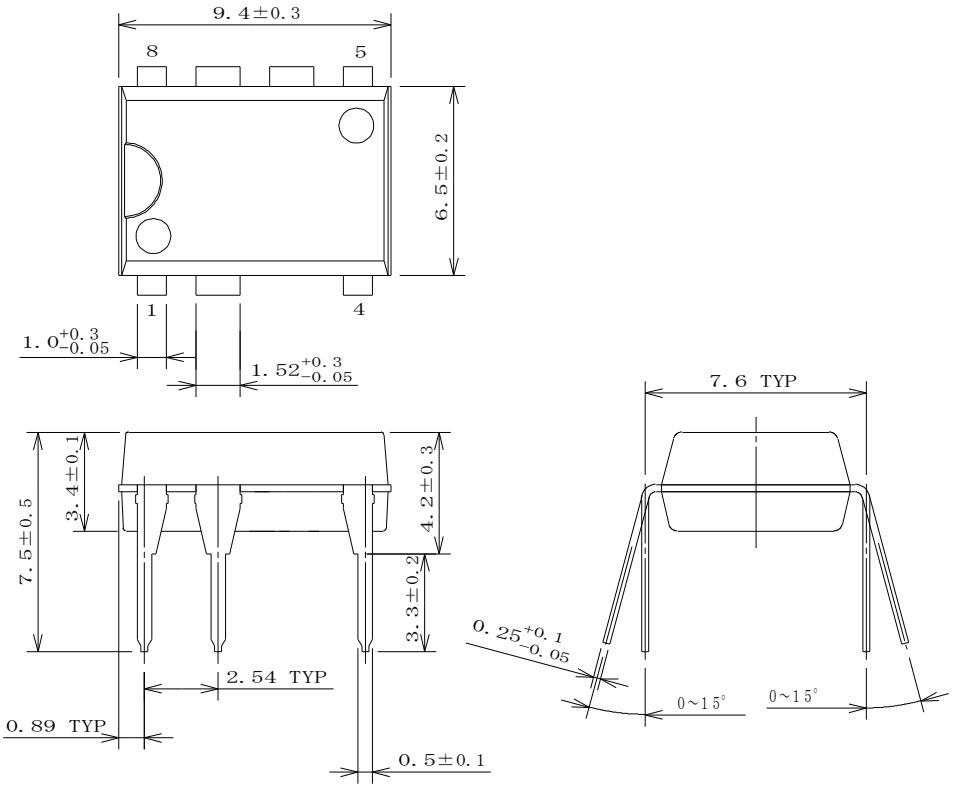
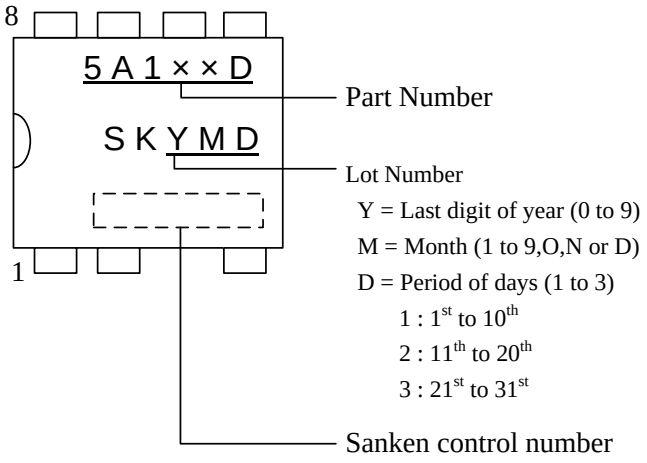


NOTES:
1) Unit : mm
2) Pb-free. Device composition compliant with the RoHS directive

9. Marking Diagram



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10. Operational Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

10.1 Startup Operation

Figure 10-1 shows the VCC pin peripheral circuit.

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{STARTUP}$ = 29 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{STARTUP}$ = − 2.1 mA, charges C4 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate startup time of IC, t_{START}, is calculated as follows:

$$t_{START} = C4 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STARTUP}|} \quad (1)$$

where,

t_{START}: Startup time of IC in second

$V_{CC(INT)}$: Initial voltage on VCC pin in V

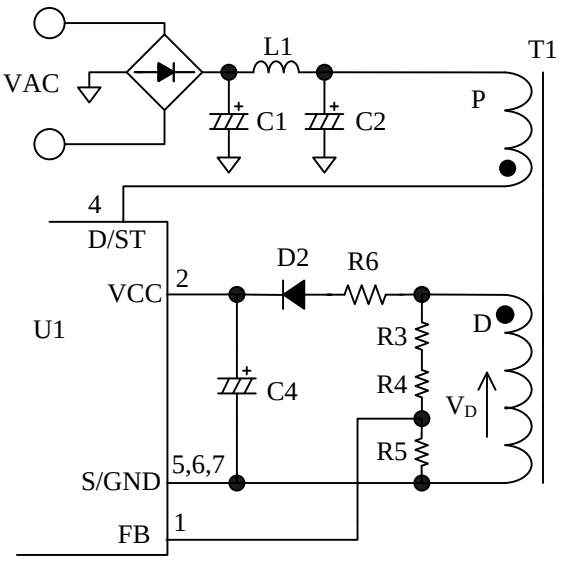

Figure 10-1 VCC pin peripheral circuit

10.2 Undervoltage Lockout (UVLO)

Figure 10-2 shows the relationship of VCC pin voltage and circuit current I_{CC}. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation and the circuit current I_{CC} increases. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

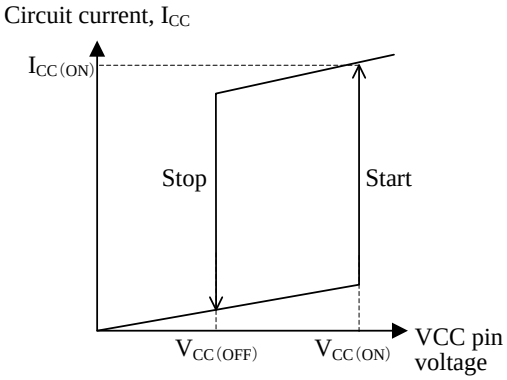

Figure 10-2 Relationship between VCC pin voltage and I_{CC}

10.3 Auxiliary Winding

Figure 10-3 shows VCC voltage behavior during the startup period. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V at startup, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. Since the Operation Stop Voltage $V_{CC(OFF)}$ = 8.1 V is low, the auxiliary winding voltage reaches to setting value before VCC pin voltage decreases to $V_{CC(OFF)}$. Thus control circuit continues the operation. The voltage from the auxiliary winding D in Figure 10-1 becomes a power source to the control circuit in operation. The approximate value of auxiliary winding voltage is about 12 V to 16 V, taking account of the winding turns of D winding so that VCC pin voltage satisfies Equation (2) within the specification of input and output voltage variation of power supply.

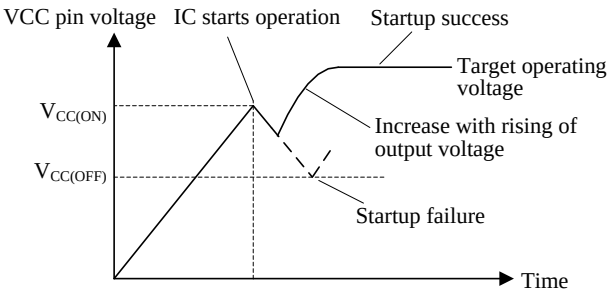

Figure 10-3 VCC pin voltage during startup period

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$$V_{CC(OFF)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 8.9\ (V) < V_{CC} < 27.5\ (V) \quad (2)$$

In addition, the auxiliary winding voltage V_D is determined as follows:

$$V_D = \frac{N_D}{N_S} \times (V_{OUT} + V_F) \quad (3)$$

where,

N_D: Turns of auxiliary winding of transformer
N_S: Turns of secondary side winding of transformer
V_{OUT}: Output voltage
V_F: Forward drop voltage of secondary side rectifier diode D50

When VCC pin voltage reaches to $V_{CC(OFF)}$ and a startup failure occurs as shown in Figure 10-3, increase the C4 value. Since the larger capacitance causes the longer startup time of IC, it is necessary to check and adjust the startup process based on actual operation in the application.

10.4 Soft Start Function

Figure 10-4 shows the behavior of VCC pin voltage and drain current during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 4.5 ms. During the soft start period, over current threshold is increased step-wisely (7 steps). This function reduces the voltage and the current stress of MOSFET and secondary side rectifier diode.

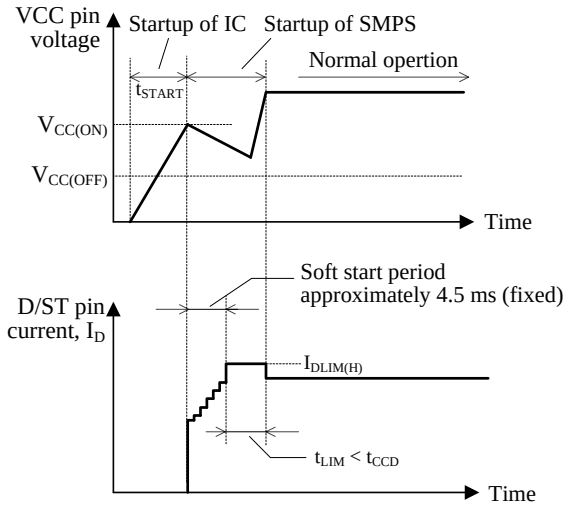

Figure 10-4 V_{CC} and I_D behavior during startup

Since the Leading Edge Blanking Function (refer to Section 10.8) is deactivated during the soft start period, there is the case that ON time is less than the leading edge blanking time, t_{BW} = 250 ns.

After the soft start period, D/ST pin current, I_D, is limited by the Drain Current Limit, $I_{DLIM(H)}$, until the output voltage increases to the target operating voltage. This period is given as t_{LIM}.

In case t_{LIM} is longer than the CC Operation Delay Time, t_{CCD} , the output power is limited by the CC mode.

Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{CCD} = 90 ms.

10.5 Primary Side Regulation (PSR)

The IC is for Primary Side Regulation (PSR). In PSR, the auxiliary winding voltage is divided by resistors (R3, R4 and R5) and is induced into FB pin as shown in Figure 10-5. The constant voltage output control is achieved by using FB pin voltage.

Figure 10-6 shows the detection timing of auxiliary winding voltage V_D. When the power MOSFET turns off, the energy stored in transformer is provided to secondary side of the circuit. Then the current I_{DO} flows through the secondary side rectifier diode. After the transfer of energy, power MOSFET continues off state and the free oscillation of V_D starts. During the free oscillation period, I_{DO} becomes zero.

The feedback signal is generated by sampling the shoulder of V_D waveform (point A in Figure 10-6). Thus the effect of V_F is minimized.

The Minimum Sampling Time, t_{FBMS}, is 2.2 µs (max.). Since the sampling time becomes the shortest in burst oscillation mode (refer to Section 10.10) , the sampling time should be more than t_{FBMS} (shown in Figure 10-6).

The ideal waveform of auxiliary winding voltage V_D is shown in Figure 10-6. The V_D waveform depends on the waveform of the primary winding P voltage. In order to reduce the transient surge of V_D waveform, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P as shown in Figure 10-5.

In order to improve the accuracy of V_D waveform sampling, the IC has sampling delay time, t_{FBD}, so that the surge component of the waveform at the turning off of power MOSFET is not sampled.

In case that the width of the surge component is longer than t_{FBD} = 0.9 µs, the width should be adjusted to be under t_{FBD}. It is achieved by adjusting the value of R1 and C3 and by reducing the peak and width of the surge component.

In addition, in order to realize the ideal V_D waveform shown in Figure 10-6, add the resistor R2 in series with the diode of CRD circuit to suppress the ringing of the waveform.

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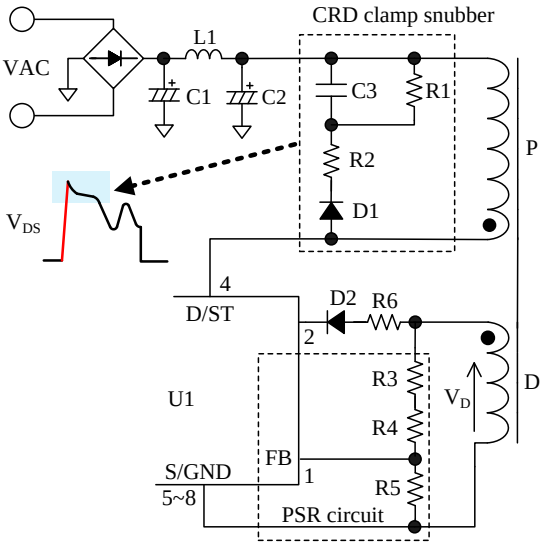

Figure 10-5 FB pin peripheral circuit

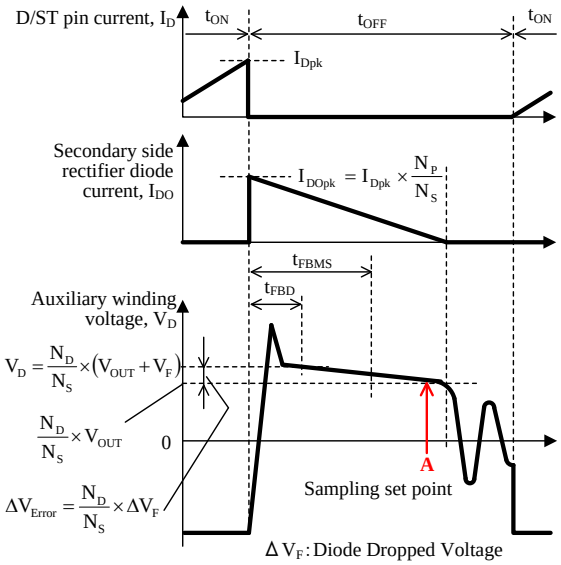

Figure 10-6 Detection timing of auxiliary winding voltage

output voltage when the output load becomes light. Accordingly, the output voltage of internal error amplifier (target voltage V_{SC}) decreases. As a result, the peak value of V_{ROCP} is controlled to be lower so that the peak of the drain current decreases. This control prevents the output voltage from increasing.

- Heavy Load Conditions
  The control circuit performs reverse operations to the former. The target voltage V_{SC} of internal comparator becomes higher and the peak drain current increases. This control prevents the output voltage from decreasing.

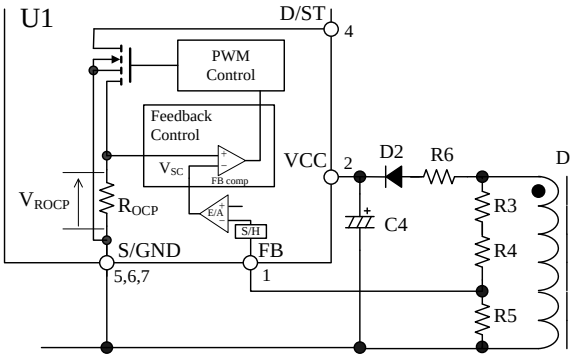

Figure 10-7 FB pin peripheral circuit

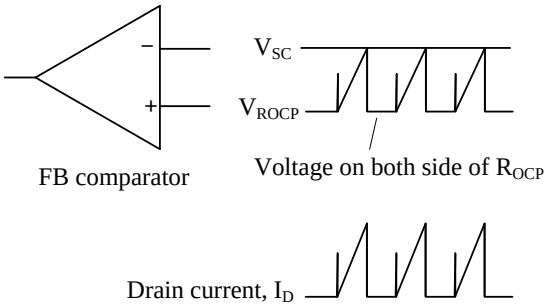

Figure 10-8 Drain current I_D and FB comparator in steady operation

10.6 Constant Voltage (CV) Control

The IC achieves the constant voltage (CV) control of the power supply output by using the peak-current-mode control method, which enhances the response speed and provides the stable operation.
The IC controls the peak value of the voltage of build-in sense resistor (V_{ROCP}) to be close to target voltage (V_{SC}), comparing V_{ROCP} with V_{SC} by internal FB comparator. Feedback Control circuit receives the sampling voltage which is the reversed auxiliary winding voltage by using error amplifier (refer to Figure 10-7 and Figure 10-8)

- Light Load Conditions
  The FB pin voltage increases with the increase of the

10.7 Constant Current (CC) Control

The IC operates in Constant Current (CC) Control when output current reaches to constant load and the state continues for more than the Constant Current Control Delay Time, t_{CCD} = 90 ms. In case the IC is in discontinuous operation, the CV/CC characteristic is as shown in Figure 10-9.

When output current reaches to constant load, MOSFET drain current is limited to the Drain Current Limit $I_{DLIM(H)}$. When the output voltage becomes low, the CC Control is maintained by lowering the oscillation frequency f_{OSC}. When the output voltage becomes low, the FB pin voltage becomes low. When FB pin voltage

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decreases to about 1.6 V or less, the IC is stops oscillation and restarts. The IC repeats the intermittent oscillation operation until the FB pin voltage keeps about 1.6 V or more after the output voltage increases.

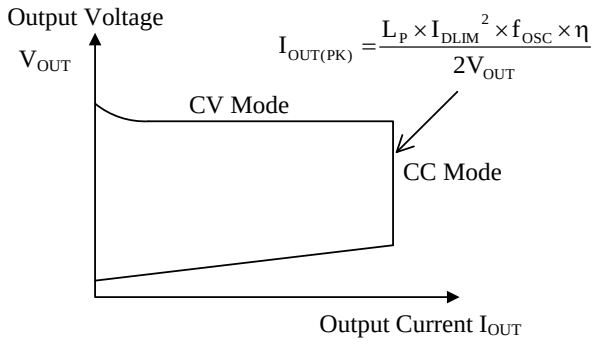

Figure 10-9 CV/CC characteristics

10.8 Leading Edge Blanking Function

The IC uses the peak-current-mode control method for the constant voltage control of output.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of FB comparator or overcurrent protection circuit (OCP) to the steep surge current in turning on a power MOSFET.

In order to prevent this operation, Leading Edge Blanking Time, t_{BW} = 250 ns is built-in.

In the period of t_{BW}, the IC does not respond to the surge voltage in turning on the power MOSFET.

10.9 Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

10.10 Auto Standby Function

Auto Standby Function automatically changes the oscillation mode to green mode or burst oscillation mode, when the output load becomes lower, the drain current I_D decreases and the oscillation frequency becomes lower gradually (Green Mode) as shown in Figure 10-10.

In order to reduce the switching loss, the number of switching is reduced in green mode and the switching operation is stopped during a constant period in burst oscillation mode.

The burst oscillation mode operates by the Standby Operation Cycle, T_{STBOP} = 1.3 ms and the switching frequency about 23 kHz. In light load, the number of minimum switching times is two times in T_{STBOP} (refer to Figure 10-11)

Since the oscillator of burst oscillation cycle setting and the oscillator of switching oscillation frequency setting are not synchronized each other, the switching frequency may be high at near the Standby Operation Threshold Voltage, V_{STBOP}.

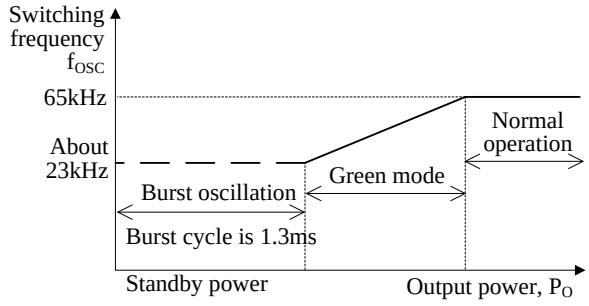

Figure 10-10 Relationship between P_O and f_{OSC}

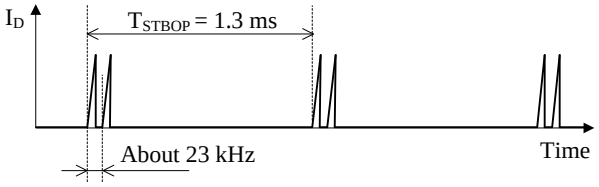

Figure 10-11 Switching waveform at burst oscillation

10.11 Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to Drain Current Limit.

When this OCP operation continues for more than the Constant Current Control Delay Time, t_{CCD} = 90 ms, Constant Current (CC) control is activated (refer to Section 10.7).

Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the actual drain peak current is, compared to the Drain Current Limit. Thus, the peak current has some variation depending on the AC input voltage in the drain current limitation state.

In order to reduce the variation of peak current in the drain current limitation state, the IC incorporates a built-in Input Compensation function.

The Input Compensation function superposes a signal with a constant slope (Figure 10-12) into the internal current detection signal and varies the internal threshold voltage.

When AC input voltage is low (ON Duty is broad),

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the Drain Current Limit after compensation increases. The difference of peak drain current become small compared with the case where the AC input voltage is high (ON Duty is narrow).

The compensation signal depends on ON Duty. The relation between the ON Duty and the drain current limit after compensation I_{DLIM}' is expressed as Equation (4). When ON Duty is broader than 27 %, the drain current limit becomes a constant value $I_{DLIM(H)}$.

$$I_{DLIM}' = \frac{I_{DLIM(H)} - I_{DLIM(L)}}{27(\%)} \times Duty + I_{DLIM(L)} \quad (4)$$

where,

Duty: MOSFET ON Duty (%)

$I_{DLIM(H)}$: Drain current limit (ON Duty ≥ 27 %)

$I_{DLIM(L)}$: Drain current limit (ON Duty = 0 %)

	$I_{DLIM(H)}$	$I_{DLIM(L)}$
STR5A162D	0.285 A	0.242 A
STR5A164D	0.41 A	0.34 A

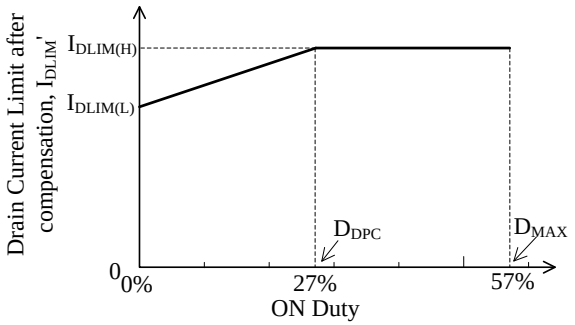

Figure 10-12 Relationship between ON Duty and Drain Current Limit after compensation

10.12 Overvoltage Protection (OVP)

When a voltage between VCC pin and S/GND terminal increases to $V_{CC(OVP)}$ = 29.3 V or more, OVP Function is activated and stops switching operation.

When OVP Function is activated, VCC pin voltage decreases to Operation Stop Voltage $V_{CC(OFF)}$ = 8.1 V. After that, the IC reverts to the initial state by UVLO (Undervoltage Lockout) circuit, and the IC starts operation when VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V by Startup Current. Thus the intermittent operation by UVLO is repeated in OVP condition.

This intermittent operation reduces the stress of parts such as power MOSFET and secondary side rectifier diode. In addition, this operation reduces power consumption because the switching period in this intermittent operation is short compared with oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

In case the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions such as FB pin open can be detected because the VCC pin voltage is proportional to FB pin voltage. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (5).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.3 \quad (5)$$

where,

$V_{OUT(NORMAL)}$: Output voltage in normal operation

$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

10.13 Thermal Shutdown Protection (TSD)

Figure 10-13 shows the TSD operational waveforms.

When the temperature of control circuit increases to $T_{j(TSD)}$ = 135 °C or more, Thermal Shutdown function (TSD) is activated, and the IC stops switching operation. After that, VCC pin voltage decreases. When the VCC pin voltage decreases to about 9.4 V, the bias assist function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.

When the temperature reduces to less than $T_{j(TSD)}$–$T_{j(TSD)HYS}$, the Bias Assist function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$. At that time, the IC stops operation by the UVLO circuit and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$, and the IC starts switching operation again. In this way, the intermittent operation by TSD and UVLO is repeated while there is an excess thermal condition.

When the fault condition is removed, the IC returns to normal operation automatically.

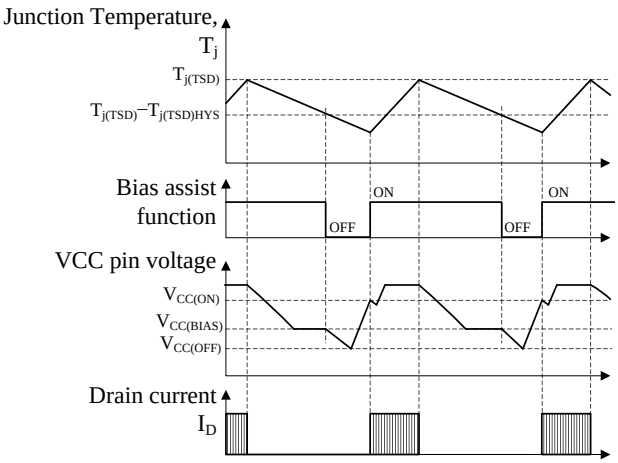

Figure 10-13 TSD operational waveforms

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11. Design Notes

11.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

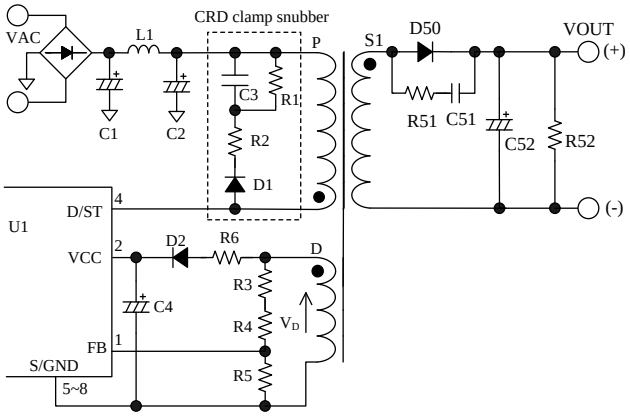

Figure 11-1 Peripheral circuit of FB pin and VCC pin

- **Output Electrolytic Capacitor**

  Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

- **FB Pin Peripheral Circuit and CRD Clamp Snubber**

  Figure 11-1 shows the FB pin peripheral circuit.
  The auxiliary winding voltage, V_D is divided by resistors (R3, R4 and R5) and induced into FB pin. The FB pin voltage is controlled to be Feedback Reference Voltage, $V_{FB(REF)}$ = 2.50 V.
  The value of R5 is about 3.3 kΩ to 10 kΩ.
  The value of R3 and R4 are calculated as follows:

$$R3+R4=\frac{\frac{N_D}{N_S}\times\left(V_{OUT}+V_F\right)-V_{FB(REF)}}{\frac{V_{FB(REF)}}{R5}-I_{FB(OP)}} \quad (6)$$

where,
N_D: Turns of auxiliary winding of transformer
N_S: Turns of secondary side winding of transformer
V_{OUT}: Output voltage
V_F: Forward drop voltage of secondary side rectifier diode D50
$V_{FB(REF)}$: Feedback Reference Voltage, 2.50 V
$I_{FB(OP)}$: Feedback Current, − 0.8 μA

In addition, the negative voltage is input to FB pin. As shown in Figure 11-2, the negative voltage, $V_{FW,}$ of V_D is calculated as follows:

$$V_{FW}=\frac{N_D}{N_P}\times V_{IN(AC)}\times\sqrt{2} \quad (7)$$

where,
$V_{IN(AC)}$: Input voltage
N_D : Turns of D winding
N_P : Turns of P winding

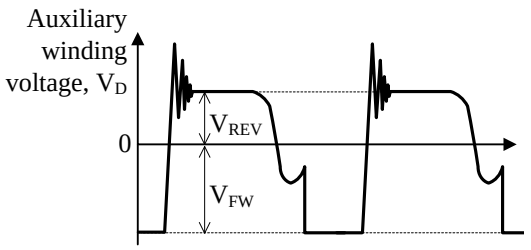

Figure 11-2 The auxiliary winding voltage waveform

The absolute maximum rating of FB Pin Source Current, I_{FB} is − 10 mA. The value of R3 and R4 are chosen so that the FB pin source current, $I_{FB(FW)}$, satisfies Equation (8) considered about surge.

$$I_{FB(FW)}=\frac{V_{FW}}{R3+R4}$$

$$=\frac{N_D}{N_P}\times\frac{V_{IN(AC)}}{R3+R4}\times\sqrt{2}\leq -5\text{mA} \quad (8)$$

There, the maximum input voltage substitutes in $V_{IN(AC)}$.
R3, R4 and R5 should be adjusted in actual operation condition.

The IC generates the feedback signal by sampled V_D waveform that is FB pin input signal. In order to improve the accuracy of V_D waveform sampling, it is necessary to realize the ideal V_D waveform for reducing the peak and width of the surge component and suppressing the ringing. Because the V_D waveform depends on the waveform of the primary winding P voltage, a clamp snubber circuit should be added on the primary winding P. The method of setting the value of the clamp snubber circuit is shown in Section 10.5.
In order to maintain the sampling accuracy during light load operation, an auxiliary switch diode SARS05 should be used as D1 where the approximate value of R2 is 220 Ω to 470 Ω. R2 should be adjusted to obtain proper V_D waveform in actual operation condition.

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• **VCC Pin Peripheral Circuit**

The reference value of C4 (see Figure 11-1) is generally from 4.7 µF to 2.2 µF. The startup time is determined by the value of C4 (refer to Section 10.1 Startup Operation).

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 11-3), and the Overvoltage Protection function (OVP) on the VCC pin may be activated. This happens because C4 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C4 peak charging, it is effective to add some value R6, of several tenths of ohms to several ohms, in series with D2 (see Figure 11-1). The optimal value of R6 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

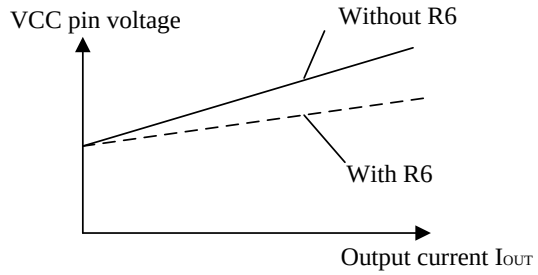

Figure 11-3 Variation of VCC pin voltage and power supply output current with / without R6 resistor

• **COMP Pin Peripheral Circuit**

Figure 11-4shows the COMP pin peripheral circuit.

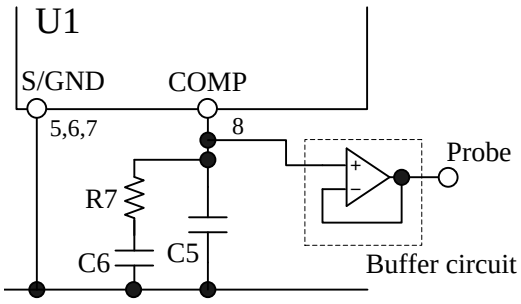

Figure 11-4 COMP pin peripheral circuit

The capacitor C5 between COMP pin and S/GND pin performs for high frequency noise reduction and phase compensation.

C5 should be connected to both COMP pin and S/GND pin as short as possible. The recommended value of C5 is 100 pF to 680 pF. The approximate value of both C6 and R7 are 680 pF to 2200 pF and 680 kΩ, respectively. These should be adjusted on actual operation.

Because the internal impedance of COMP pin is high, the measurement of COMP pin waveform by using the oscilloscope needs a caution.

Especially in light load condition, the probe of the oscilloscope may affect the control of IC. Thus the voltage-follower (buffer) circuit with high impedance Op Amp should be used for the measurement of COMP pin.

• **D/ST Pin**

The internal power MOSFET connected to D/ST pin (see Figure 11-1) is permanently damaged when the D/ST pin voltage and the current exceed the Absolute Maximum Ratings. Therefore, as shown in Figure 11-5, The D/ST pin voltage is tuned to be less than about 90 % of the Absolute Maximum Ratings (657 V) in all condition of actual operation, and the value of transformer and components should be selected based on actual operation in the application.

And the D/ST pin voltage in normal operation is tuned to be the Recommended Operating Conditions, $V_{D/ST(OP)} < 584$ V.

The fast recovery diodes are recommended for using as D2 and D51. The way of setting the value of the clamp snubber circuit is shown in Section 10.5.

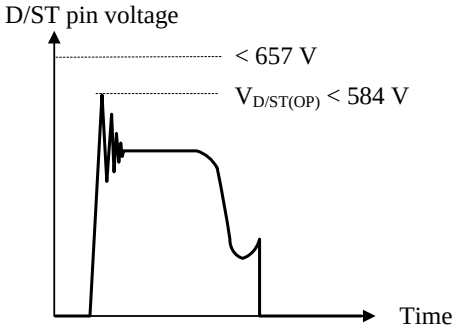

Figure 11-5 D/ST pin voltage waveform

• **Bleeder Resistance**

Since the IC employs the primary side regulation, the IC continues burst oscillation operation at light load in order to detect the state of secondary side.

In case the power supply is used under light load condition (input power is 25 mW or less at maximum input voltage) or no load condition, in order to prevent the increase of output voltage, the bleeder resistance, R52, is connected to both ends of the output capacitor, C52, as shown in Figure 11-1.

The value of R52 should be selected based on actual operation in the application after the R52

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which loss of R52 becomes about 10 mW is connected.

- **Transformer**

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage Protection function (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3···) should be maximized to improve the line-regulation of those outputs.

Figure 11-6 shows the winding structural examples of two outputs.

Winding structural example (a):

S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.

D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

Winding structural example (b)

P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.

D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.

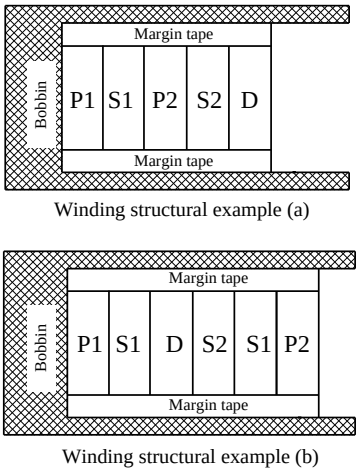

Figure 11-6 Winding structural examples

11.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 11-7 shows the circuit design example.

(1) Main Circuit Trace Layout:

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

If C2 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout

Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be connected at a single point grounding of point A as close to the S/GND pin as possible.

(3) VCC Trace Layout:

This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C4 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the S/GND pin is recommended.

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(4) COMP Trace Layout
C5, C6 and R7 are connected to COMP pin for phase compensation. These capacitors and resistor should be placed to shorten the trace between COMP pin and S/GND pin. In order to stabilize the operation of IC, a dedicated trace to S/GND pin is recommended.

(5) FB Trace Layout
The auxiliary winding voltage is divided by resistors and is induced to FB pin. In order to achieve the accurate primary side regulation, the trace between the resistors and FB pin should be as short as possible.

(6) Secondary Rectifier Smoothing Circuit Trace Layout:
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations
Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design. Since the copper area under the IC and the S/GND trace act as a heatsink, its traces should be as wide as possible.

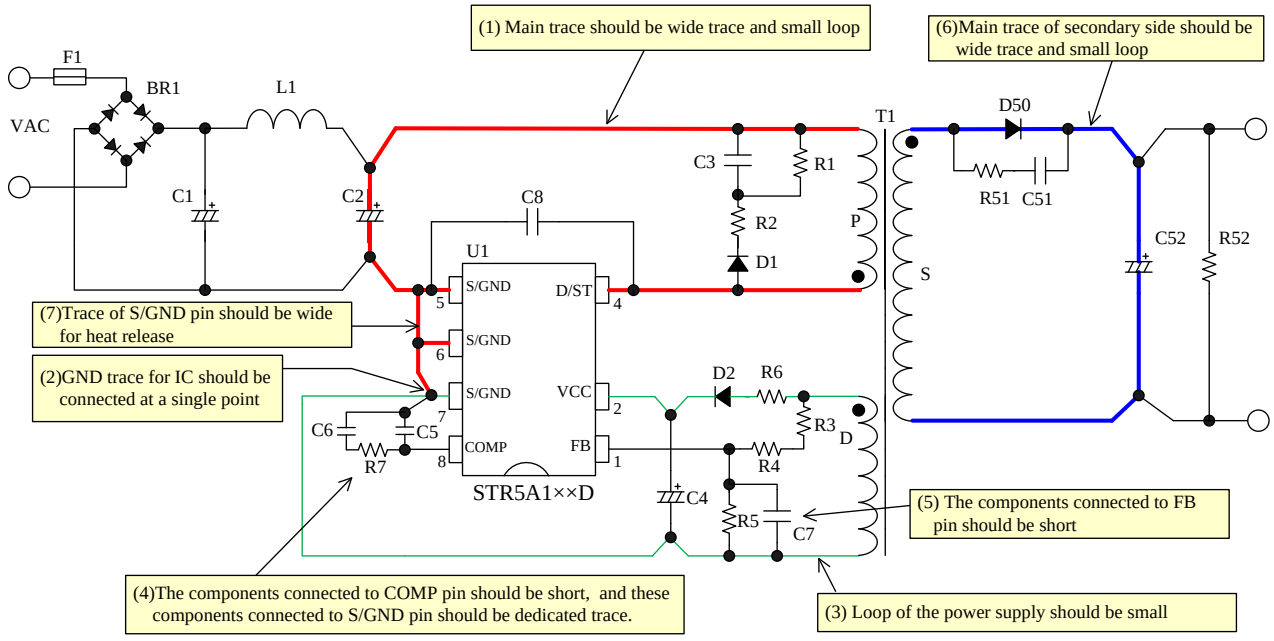

Figure 11-7 Example of peripheral circuit around the IC

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12. Pattern Layout Example

The following show the PCB pattern layout example and the circuit schematic with STR5A100D series.The above circuit symbols correspond to these of Figure 12-1.

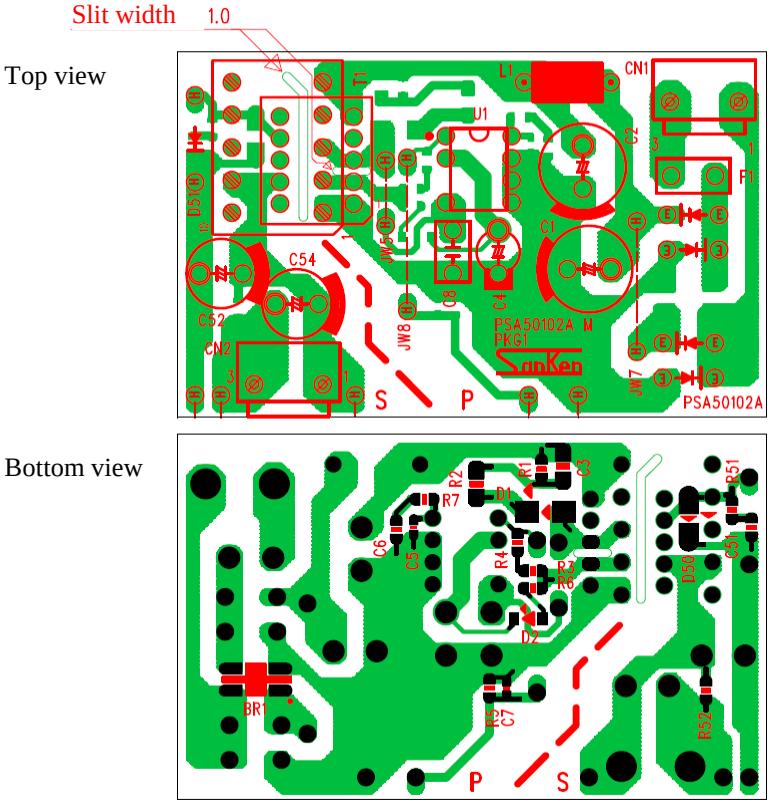

Figure 12-1 PCB circuit trace layout example

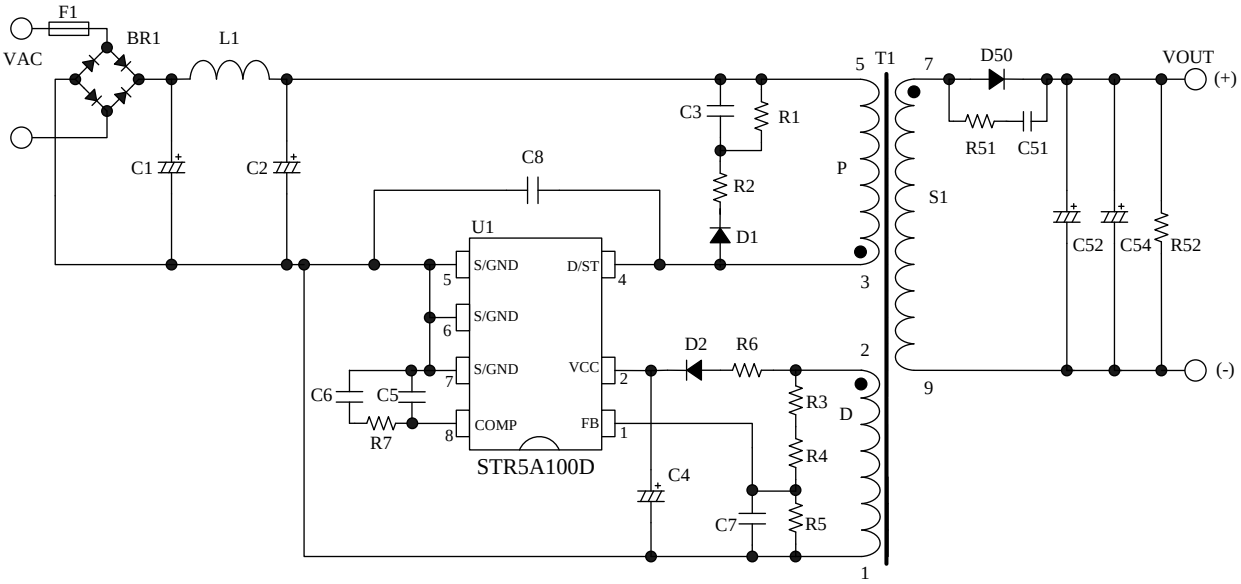

Figure 12-2 Circuit schematic for PCB circuit trace layout

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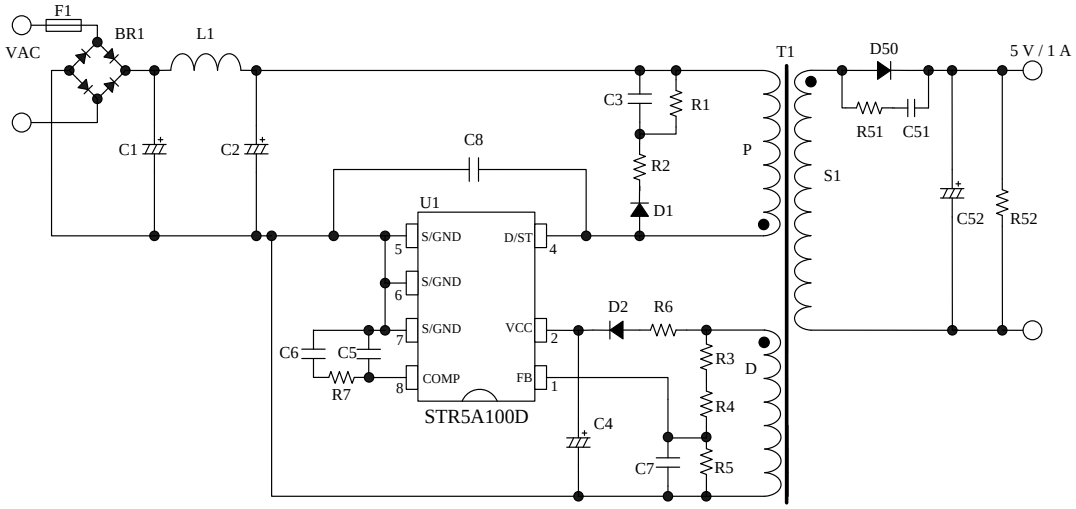
13. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

● Power supply specification

IC	STR5A164D
Input voltage	AC 85 V to AC 265 V
Maximum output power	5 W (max.)
Output voltage	5 V
Output current	1 A (max.)

● Circuit schematic



● Bill of materials

Symbol	Part type	Ratings[1]	Recommended Sanken Parts	Symbol	Part type	Ratings[1]	Recommended Sanken Parts
BR1	General	600 V, 1 A		R4 [2]	Chip	15 kΩ	
F1	Fuse	AC 250 V, 1 A		R5 [2]	Chip	4.7 kΩ	
L1* [2]	CM inductor	330 µH		R6 [2]	Chip	0 Ω	
C1	Electrolytic	400 V, 4.7 µF		R7 [2]	Chip	680 kΩ	
C2	Electrolytic	400 V, 4.7 µF		D1	General	800 V, 1 A	SARS05
C3	Ceramic, chip	630 V, 1000 pF		D2	Fast recovery, chip	FRD 200 V, 1 A	
C4	Electrolytic	50 V, 10 µF		U1	IC	STR5A164D	
C5 [2]	Ceramic, chip	330 pF		T1	Transformer	See the specification	
C6 [2]	Ceramic, chip	1000 pF		D50	Schottky	60 V, 3 A	SJPB-L6
C7 [2]	Ceramic, chip	Open		C51	Ceramic, chip	50 V, 2200 pF	
C8 [2]	Ceramic, chip	Open		C52 [2]	Electrolytic	10V, 470µF	
R1 [3]	Metal oxide, chip	470 kΩ		R51	Chip	22 Ω	
R2	Chip	270 Ω		R52* [2]	Chip	2.7 kΩ	
R3 [2]	Chip	3.9 kΩ					

[1] Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
[2] It is necessary to be adjusted based on actual operation in the application.
[3] Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

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● Transformer specification
- Primary inductance, L_P : 1.7 mH
- Core size : EI-16
- AL-value : 118 nH/N^2 (Center gap of about 0.3 mm)
- Winding specification

Winding	Symbol	Number of turns (T)	Wire diameter (mm)	Construction	Wire
Primary winding 1	P1	80	φ 0.16	Two layers, solenoid winding	Enameled Copper Wire
Primary winding 2	P2	40	φ 0.16	Single-layer, solenoid winding	Enameled Copper Wire
Auxiliary winding	D	18	φ 0.16 × 2	Single-layer, solenoid winding	Enameled Copper Wire
Output winding 1	S1	8	φ 0.3 × 2	Single-layer, solenoid winding	Triple insulated wire
Output winding 2	S2	8	φ 0.3 × 2	Single-layer, solenoid winding	Triple insulated wire

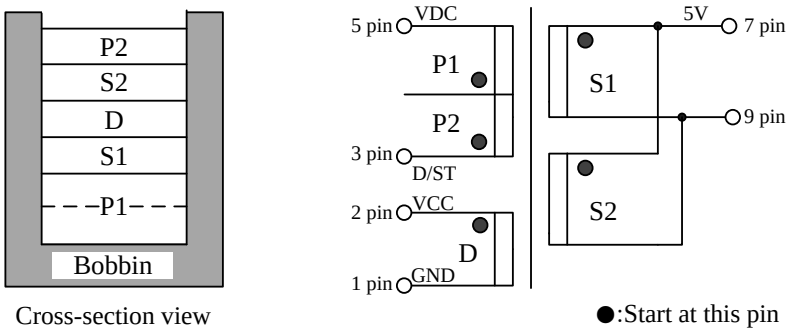

Figure 13-1 Example of transformer structure

Notes:
1) Coupling between D winding and S1 winding should be adjusted and be improved by applying the solid winding construction in D winding, for example.
2) The peak value of drain current I_D in normal operation is determined by L_P value. Since the slope of I_D is expressed as V_{DS}/L_P, the smaller the L_P value, the steeper the slope of I_D becomes. Thus the peak value of drain current becomes high as shown in Figure 13-2. The IC limits the peak current by drain current limit I_{DLIM} (Overcurrent state). If L_P value becomes small by variation, there is the case that the system is in overcurrent state. Then the designed output power cannot be achieved. Thus the L_P value should be determined after the confirmation in actual operation using minimum L_P value within the variation, where the peak current value should be less than I_{DLIM}(MIN) in minimum input voltage of power supply.

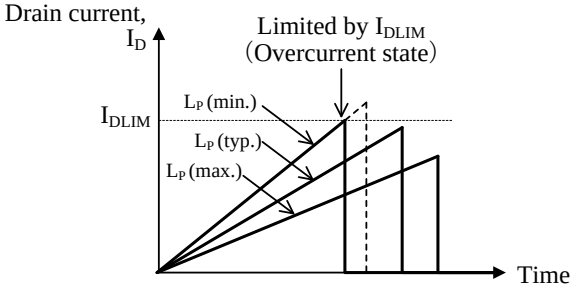

Figure 13-2 Relation between L_P and drain current I_D

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Important Notes

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DSGN-CEZ-16003

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