Off-Line PWM Controllers with Integrated Power MOSFET

STR3A200 Series

Data Sheet

Description

The STR3A200 series are power ICs for switching power supplies, incorporating a MOSFET and a current mode PWM controller IC.

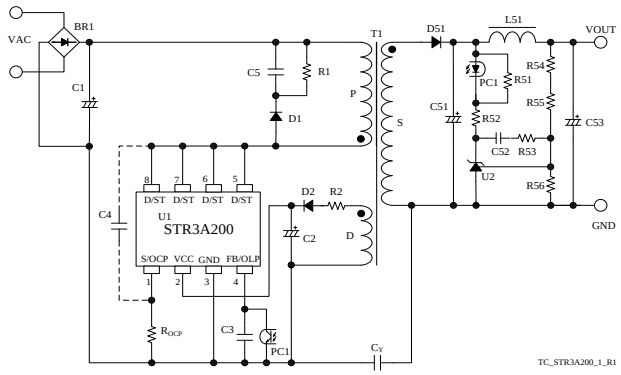
The low standby power is accomplished by the automatic switching between the PWM operation in normal operation and the burst-oscillation under light load conditions. The product achieves high cost-performance power supply systems with few external components.

Features

- Low Thermal Resistance Package
- Current Mode Type PWM Control
- Soft Start Function
- Auto Standby Function
  No Load Power Consumption < 15mW
- Operation Mode
  Normal Operation: PWM Mode
  Standby : Burst Oscillation Mode
- Random Switching Function
- Slope Compensation Function
- Leading Edge Blanking Function
- Bias Assist Function
- Protections

– Two Types of Overcurrent Protection (OCP) : Pulse-by-Pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
– Overload Protection (OLP) : Aauto-restart
– Overvoltage Protection (OVP) : Latched shutdown or auto-restart
– Thermal Shutdown (TSD) : Latched shutdown or auto-restart with hysteresis

Typical Application



Package

DIP8



Not to Scale

Selection Guide

- Electrical Characteristics

$f_{OSC(AVG)}$ = 67 kHz
V_{DSS}(min.) = 650 V

Products	OVP, TSD Operation
STR3A251	Latched shutdown
STR3A25×D	Auto restart

- MOSFET $R_{DS(ON)}$ and P_{OUT}*

Products	$R_{DS(ON)}$ (max.)	P_{OUT} (Adapter)		P_{OUT} (Open frame)	
		AC230V	AC85 ~265V	AC230V	AC85 ~265V
STR3A251	4.0 Ω	29.5 W	19.5 W	37 W	23 W
STR3A251D					
STR3A253D	1.9 Ω	37 W	27.5 W	53 W	35 W
STR3A255D	1.1 Ω	45 W	35 W	65 W	44 W

* The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, ON Duty, and thermal design affect the output power. It may be less than the value stated here.

Application

- AC/DC Adapter
- Large Home Appliance
- Other SMPSs (Switching Mode Power Supplies)

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, 5 pin = 6 pin = 7 pin = 8 pin.

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Notes
Drain Peak Current(1)	I_{DPEAK}	Single pulse	8 – 1	3.6	A	3A251 / 51D
				5.2		3A253D
				7.2		3A255D
Avalanche Energy(2)(3)	E_{AS}	I_{LPEAK} = 2.13 A	8 – 1	53	mJ	3A251 / 51D
		I_{LPEAK} = 2.46 A		72		3A253D
		I_{LPEAK} = 3.05 A		110		3A255D
S/OCP Pin Voltage	V_{OCP}		1 – 3	− 2 to 6	V	
VCC Pin Voltage	V_{CC}		2 – 3	32	V	
FB/OLP Pin Voltage	V_{FB}		4 – 3	− 0.3 to 14	V	
FB/OLP Pin Sink Current	I_{FB}		4 – 3	1.0	mA	
D/ST Pin Voltage	$V_{D/ST}$		8 − 3	− 1 to V_{DSS}	V	
Power MOSFET Allowable Power Dissipation(4)	P_{D1}	(5)	8 – 1	1.68	W	3A251 / 51D
				1.76		3A253D
				1.81		3A255D
Control Part Allowable Power Dissipation	P_{D2}		2 – 3	1.3	W	V_{CC} × I_{CC}
Operating Ambient Temperature	T_{OP}		−	− 40 to 125	°C	
Storage Temperature	T_{STG}		−	− 40 to 125	°C	
Channel Temperature	T_{ch}		−	150	°C	

(1) See 4.2 MOSFET Safe Operating Area Curves
(2) See Figure 4-2 Avalanche Energy Derating Coefficient Curve
(3) Single pulse, V_{DD} = 99 V, L = 20 mH
(4) See Section 4.3 T_A-P_{D1} Curve
(5) When embedding this hybrid IC onto the printed circuit board (cupper area in a 15 mm × 15 mm)

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2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 18 V, 5 pin = 6 pin = 7 pin = 8 pin.

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		2 − 3	13.8	15.0	16.2	V	
Operation Stop Voltage[(1)]	$V_{CC(OFF)}$		2 − 3	7.6	8.5	9.2	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	2 − 3	−	1.7	2.3	mA	
Startup Circuit Operation Voltage	$V_{ST(ON)}$		8 − 3	40	47	55	V	
Startup Current	$I_{CC(ST)}$	V_{CC} = 13.5 V	2 − 3	− 4.5	− 2.5	− 1.2	mA	
Startup Current Biasing Threshold Voltage	$V_{CC(BIAS)}$	I_{CC}=−500µA	2 − 3	8.0	9.6	10.5	V	
Normal Operation								
Average Switching Frequency	$f_{OSC(AVG)}$		8 − 3	60	67	73	kHz	
Switching Frequency Modulation Deviation	Δf		8 − 3	−	5.4	−	kHz	
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	4 − 3	− 170	− 130	− 90	µA	
Minimum Feedback Current	$I_{FB(MIN)}$		4 − 3	− 21	− 13	− 5	µA	
Standby Operation								
Oscillation Stop FB Voltage	$V_{FB(OFF)}$		4 − 3	1.06	1.16	1.26	V	3A251/ 51D /53D
				0.81	0.90	0.99		3A255D
Protection								
Maximum ON Duty	D_{MAX}		8 − 3	70	75	80	%	
Leading Edge Blanking (LEB) Time	t_{BW}		−	−	330	−	ns	
OCP Compensation Coefficient	DPC		−	−	17.3	−	mV/µs	
OCP Compensation Duty Cycle	D_{DPC}		−	−	36	−	%	
OCP Threshold Voltage at Zero Duty Cycle	$V_{OCP(L)}$		1 − 3	0.735	0.795	0.855	V	
OCP Threshold Voltage at 36% Duty Cycle	$V_{OCP(H)}$		1 − 3	0.843	0.888	0.933	V	
OCP Threshold Voltage during LEB Time	$V_{OCP(LEB)}$		1 − 3	−	1.69	−	V	
OLP Threshold Voltage	$V_{FB(OLP)}$		4 − 3	6.8	7.3	7.8	V	
OLP Operation Current	t_{OLP}		—	55	75	90	ms	
OLP Delay Time	$I_{CC(OLP)}$	V_{CC}= 12V	2 − 3	−	160	−	µA	
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		4 − 3	10.5	11.8	13.5	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		2 − 3	27.0	29.1	31.2	V	

[(1)] $V_{CC(BIAS)}$ > $V_{CC(OFF)}$ always.

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Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
TSD Operating Temperature	$T_{J(TSD)}$		—	127	145	−	°C	
TSD Hysteresis Temperature	$T_{J(TSD)HYS}$		−	−	80	−	°C	3A2××D
MOSFET								
Drain-to-Source Breakdown Voltage	V_{DSS}	I_{DS} = 300μA	8 − 1	650	−	−	V	
Drain Leakage Current	I_{DSS}	V_{DS} = V_{DSS}	8 − 1	−	−	300	μA	
On-resistance	$R_{DS(ON)}$	I_{DS} = 0.4A	8 − 1	−	−	4.0	Ω	3A251/ 51D
				−	−	1.9		3A253D
				−	−	1.1		3A255D
Switching Time	t_f		8 – 1	−	−	250	ns	
Thermal Resistance								
Channel-to-Case Thermal Resistance[(2)]	θ_{ch-C}		−	−	−	18	°C/W	3A251/ 51D/ 53D
				−	−	17	°C/W	3A255D

[(2)] θ_{ch-C} is thermal resistance between channel and case. Case temperature (T_C) is measured at the center of the case top surface.

3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.51	—	g

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4. Performance Curves

4.1 Derating Curves

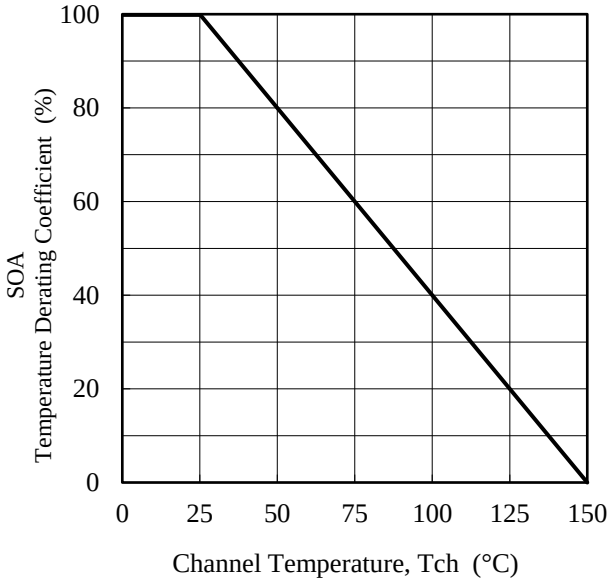

Figure 4-1. SOA Temperature Derating Coefficient Curve

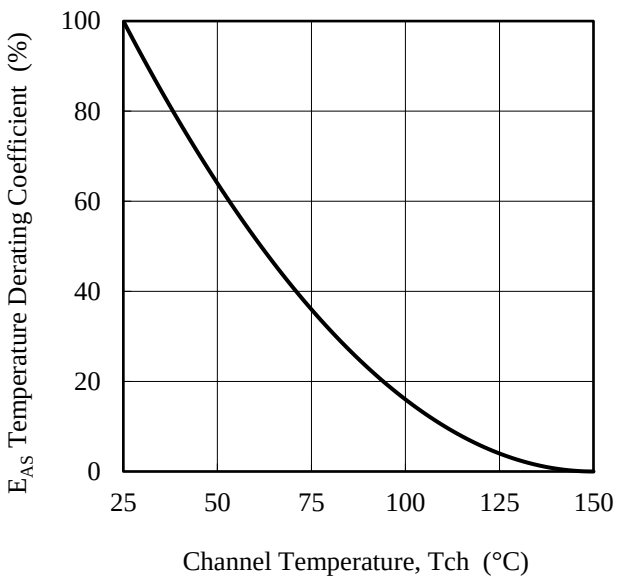

Figure 4-2. Avalanche Energy Derating Coefficient Curve

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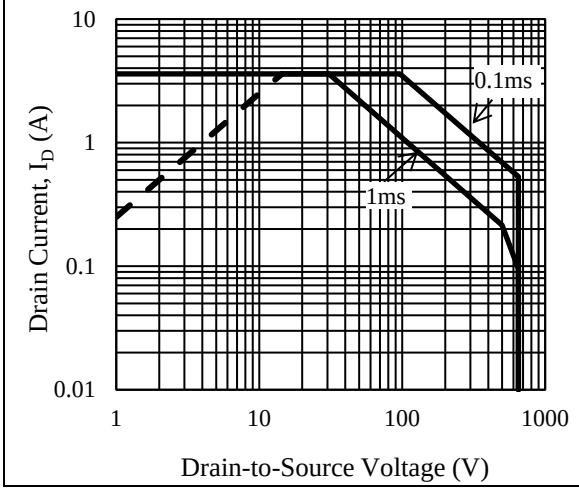
4.2 MOSFET Safe Operating Area Curves

When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from IC Figure 4-1.

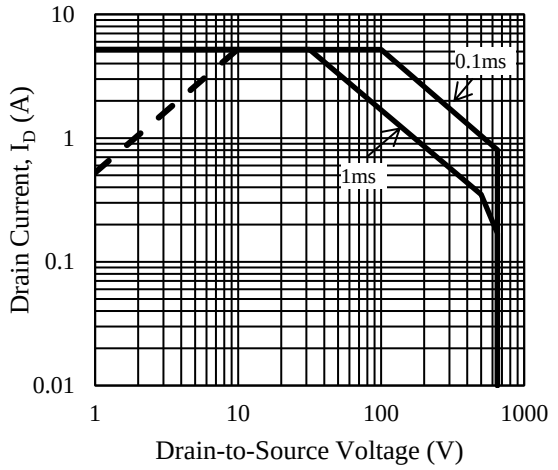
The broken line in the safe operating area curve is the drain current curve limited by on-resistance.

Unless specifically noted, T_A = 25 °C, single pulse.

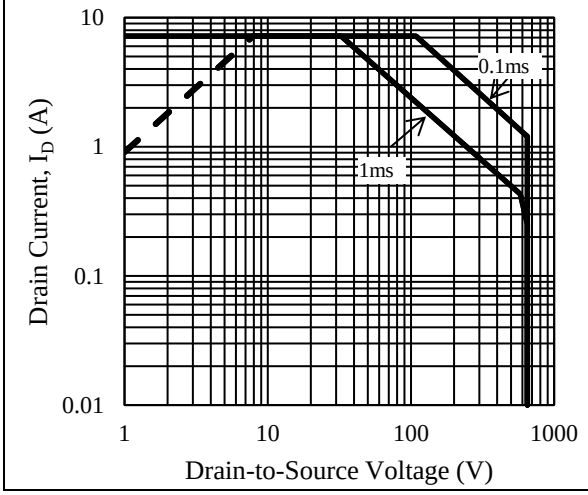
• **STR3A251/ 51D**



• **STR3A253D**



• **STR3A255D**



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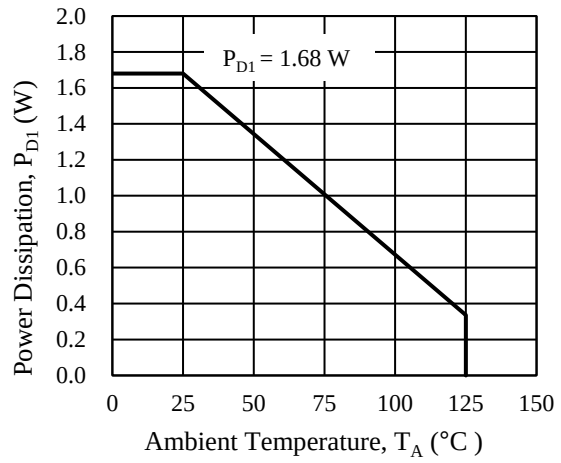
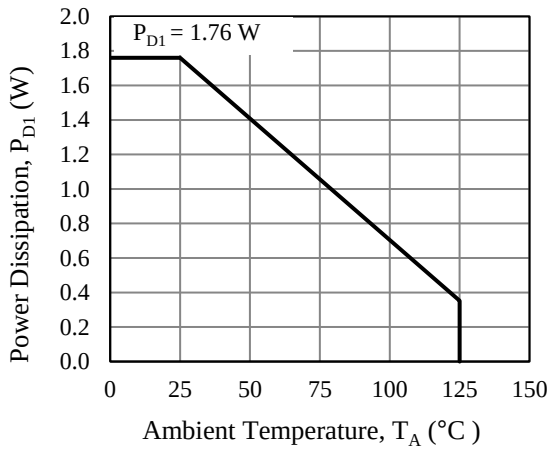
4.3 Ambient Temperature versus Power Dissipation Curves

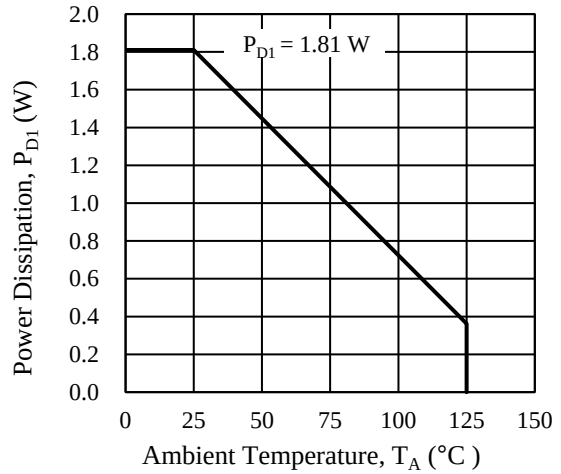
● STR3A251/ 51D



● STR3A253D



● STR3A255D



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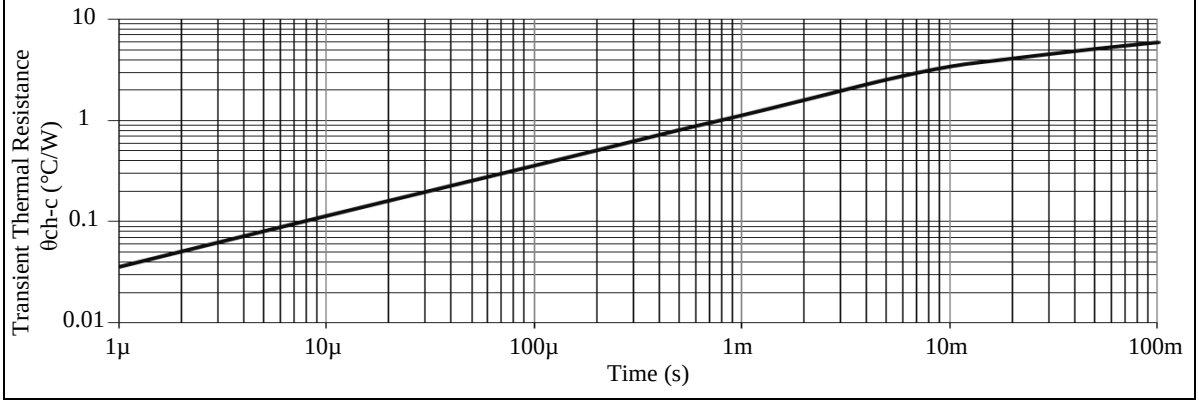
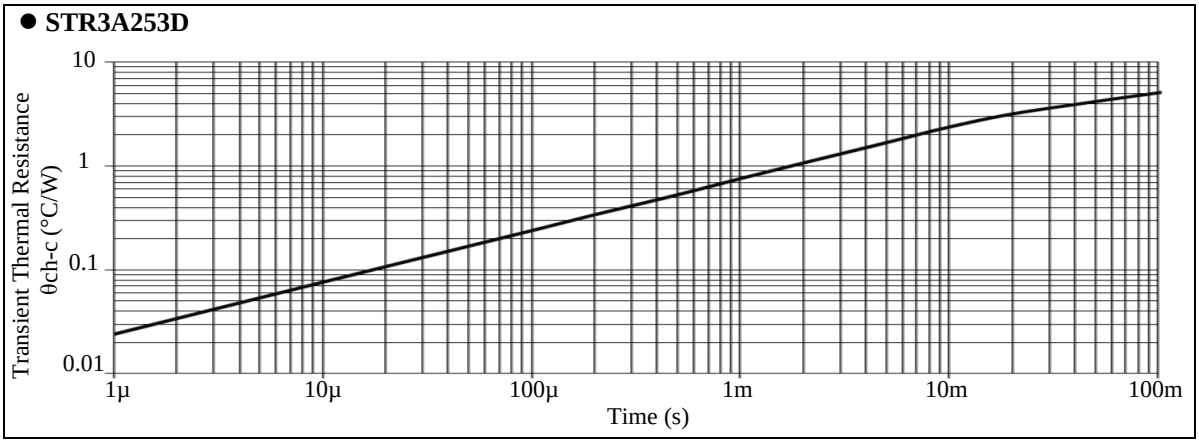
4.4 Transient Thermal Resistance Curves

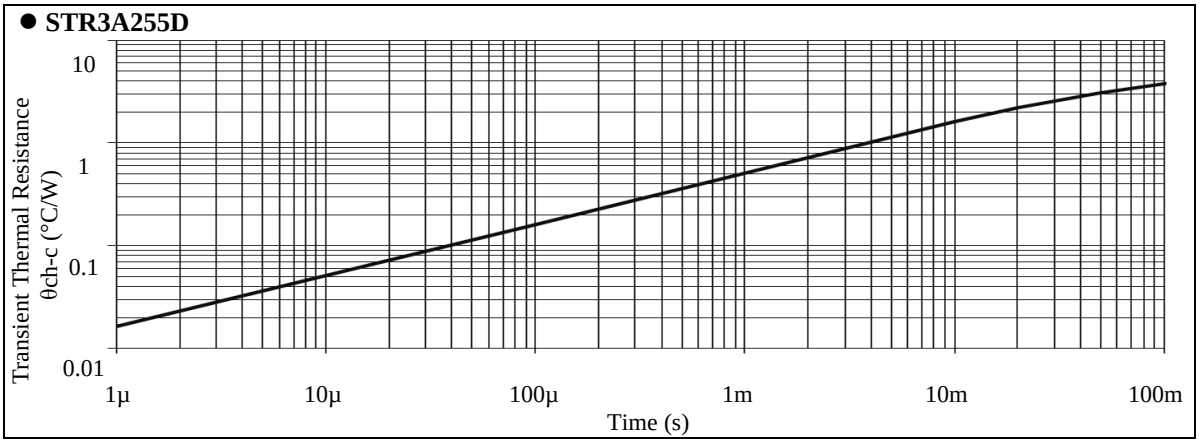
● **STR3A251/ 51D**



● **STR3A253D**



● **STR3A255D**



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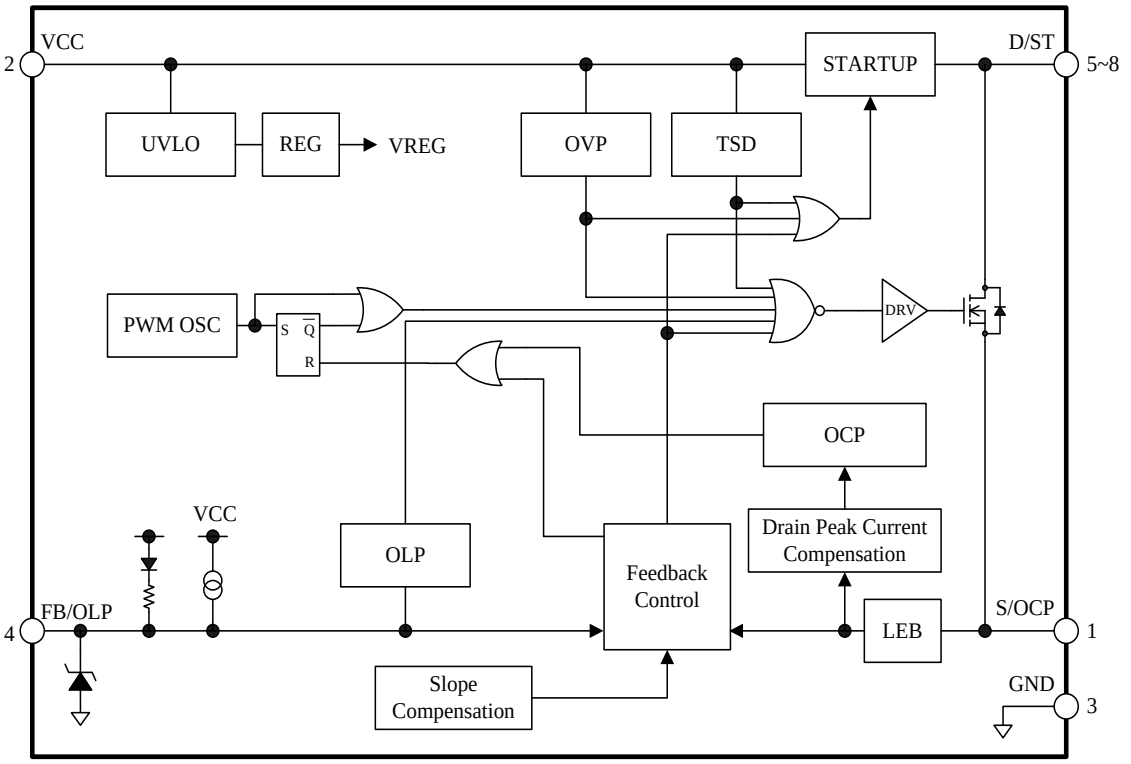
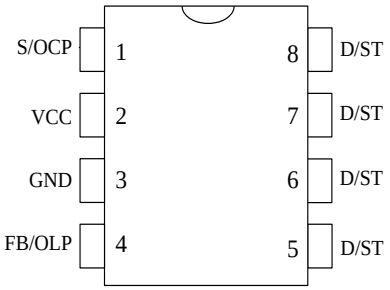
5. Block Diagram



6. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	S/OCP	MOSFET source; OCP signal input
2	VCC	Logic power supply input; OVP signal input
3	GND	Ground
4	FB/OLP	Constant voltage control signal input; OLP signal input
5	D/ST	MOSFET drain input; startup current input
6		
7		
8		

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7. Typical Application

The PCB traces of the D/ST pins should be as wide as possible, in order to enhance thermal dissipation.

In applications having a power supply specified such that VDS has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

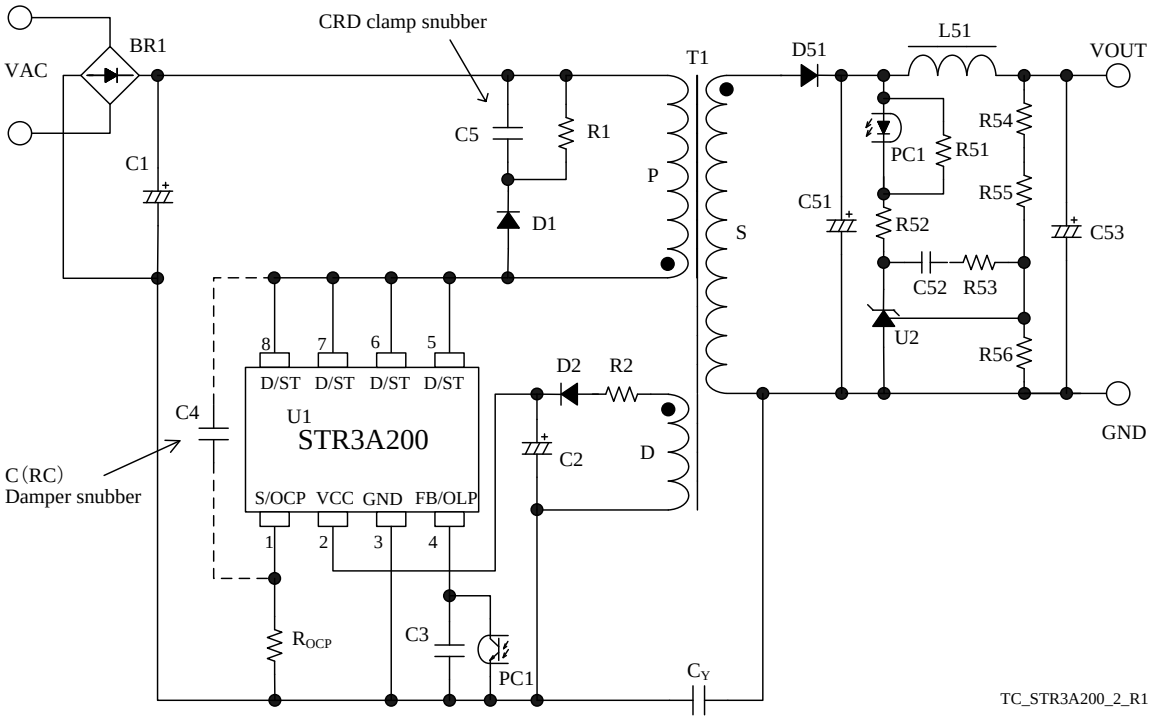

Figure 7-1. Typical Application

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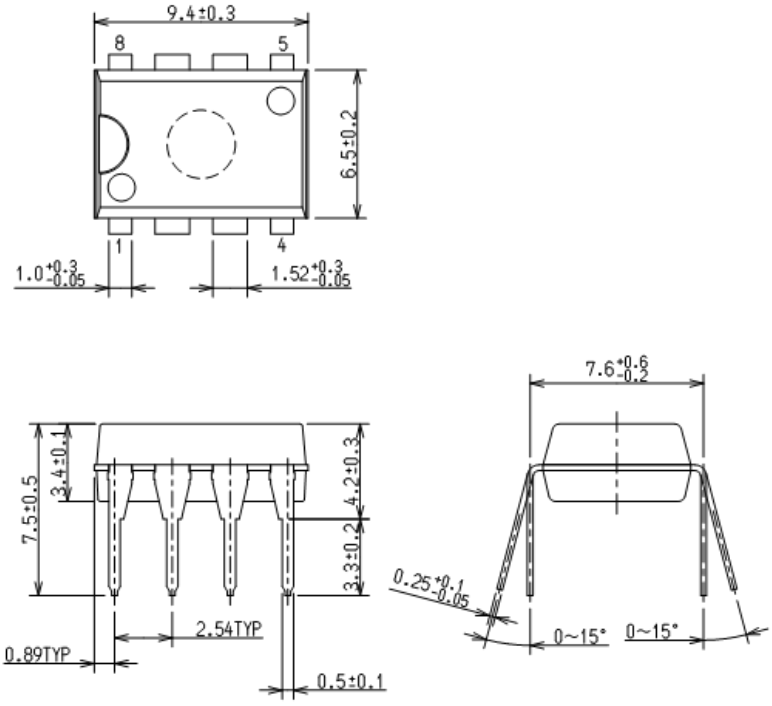
8. Physical Dimensions

● DIP8



NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Soldering Iron: 350 °C / 3.5 s, 1 time
  Soldering should be at a distance of at least 1.5 mm from the body of the product.

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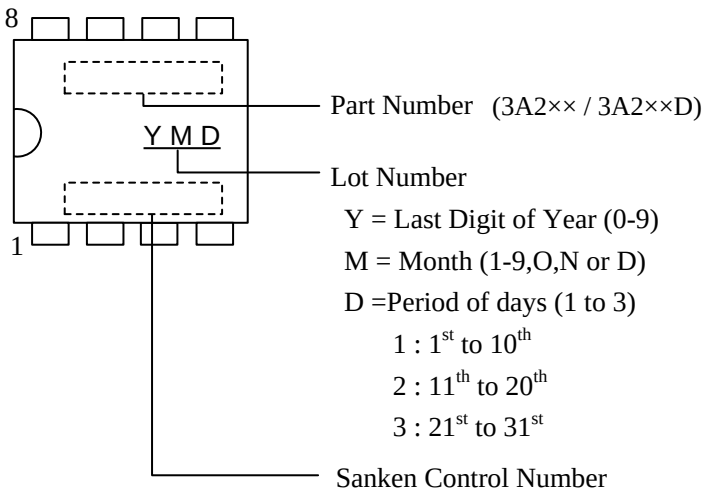
9. Marking Diagram



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10. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

10.1 Startup Operation

Figure 10-1 shows the circuit around the VCC pin.

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When the D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{ST(ON)}$ = 47 V, the startup circuit starts operation. During the startup process, the constant current, $I_{CC(ST)}$ = − 2.5 mA, charges C2 at the VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation. During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 10-1 becomes a power source to the VCC pin. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

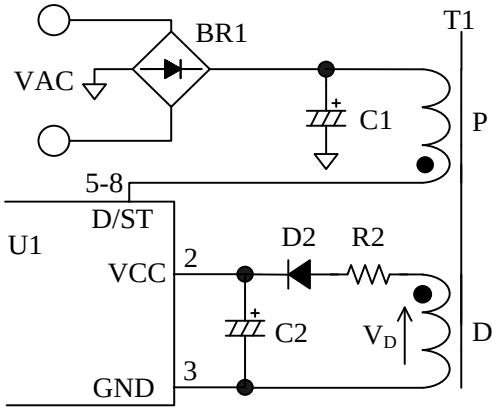

Figure 10-1. VCC Pin Peripheral Circuit

The approximate value of auxiliary winding voltage is about 18V, taking account of the winding turns of D winding so that the VCC pin voltage becomes Equation (1) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 10.5\ (V) < V_{CC} < 27.0\ (V) \quad (1)$$

The startup time of the IC is determined by C2 capacitor value. The approximate startup time t_{START} is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left| I_{CC(ST)} \right|} \quad (2)$$

Where,
t_{START} : Startup time of the IC (s)
$V_{CC(INT)}$: Initial voltage on the VCC pin (V)

10.2 Undervoltage Lockout (UVLO)

Figure 10-2 shows the relationship of the VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

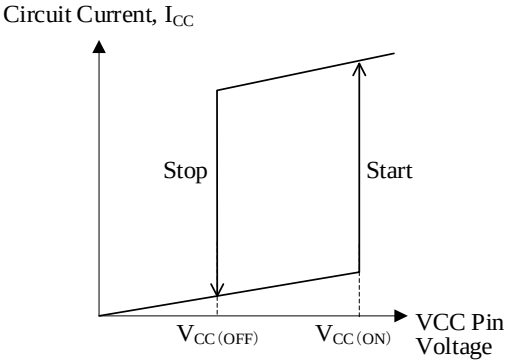

Figure 10-2 Relationship between VCC Pin Voltage and I_{CC}

10.3 Bias Assist Function

By the Bias Assist Function, the startup failure is prevented and the latched state is kept.

The Bias Assist Function is activated in the following condition. Where, $V_{FB(OFF)}$ is the FB/OLP Pin Oscillation Stop Threshold Voltage, $V_{CC(BIAS)}$ is the Startup Current Biasing Threshold Voltage.

- Auto restart type (STR3A2××D)
  When FB pin voltage is $V_{FB(OFF)}$ or less and VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.6 V, the Bias Assist Function is activated.

- Latched shutdown type (STR3A2××)
  When VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.6 V in the following condition, the Bias Assist Function is activated.
  FB pin voltage is $V_{FB(OFF)}$ or less
  or the IC is in the latched state due to activating the

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protection function.

When the Bias Assist Function is activated, the VCC pin voltage is kept almost constant voltage, $V_{CC(BIAS)}$ by providing the startup current, $I_{CC(ST)}$, from the startup circuit. Thus, the VCC pin voltage is kept more than $V_{CC(OFF)}$.

Since the startup failure is prevented by the Bias Assist Function, the value of C2 connected to the VCC pin can be small. Thus, the startup time and the response time of the Overvoltage Protection (OVP) become shorter.

The operation of the Bias Assist Function in startup is as follows. It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

Figure 10-3 shows the VCC pin voltage behavior during the startup period.

After the VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V at startup, the IC starts the operation. Then circuit current increases and the VCC pin voltage decreases. At the same time, the auxiliary winding voltage, V_D, increases in proportion to output voltage. These are all balanced to produce the VCC pin voltage.

When the VCC pin voltage is decrease to $V_{CC(OFF)}$ = 8.5 V in startup operation, the IC stops switching operation and a startup failure occurs.

When the output load is light at startup, the output voltage may become more than the target voltage due to the delay of feedback circuit. In this case, the FB pin voltage is decreased by the feedback control. When the FB pin voltage decreases to $V_{FB(OFF)}$ or less, the IC stops switching operation and the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist function is activated and the startup failure is prevented.

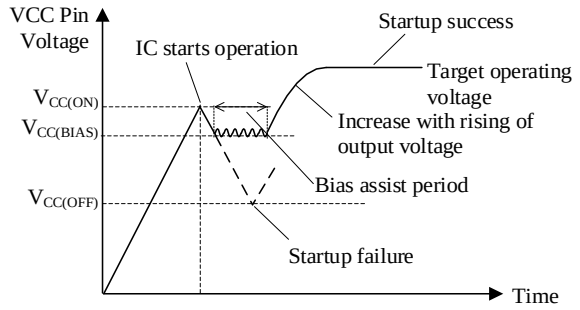

Figure 10-3. VCC Pin Voltage during Startup Period

10.4 Soft Start Function

Figure 10-4 shows the behavior of VCC pin voltage and drain current during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 8.75 ms. during the soft start period, overcurrent threshold is increased step-wisely (7 steps). This function reduces the voltage and the current stress of a power MOSFET and the secondary side rectifier diode.

Since the Leading Edge Blanking Function (refer to Section 10.6) is deactivated during the soft start period, there is the case that ON time is less than the leading edge blanking time, t_{BW} = 330 ns.

After the soft start period, D/ST pin current, I_D, is limited by the Overcurrent Protection (OCP), until the output voltage increases to the target operating voltage. This period is given as t_{LIM}. In case t_{LIM} is longer than the OLP Delay Time, t_{OLP}, the output power is limited by the Overload Protection (OLP) operation. Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{OLP} = 55 ms (min.).

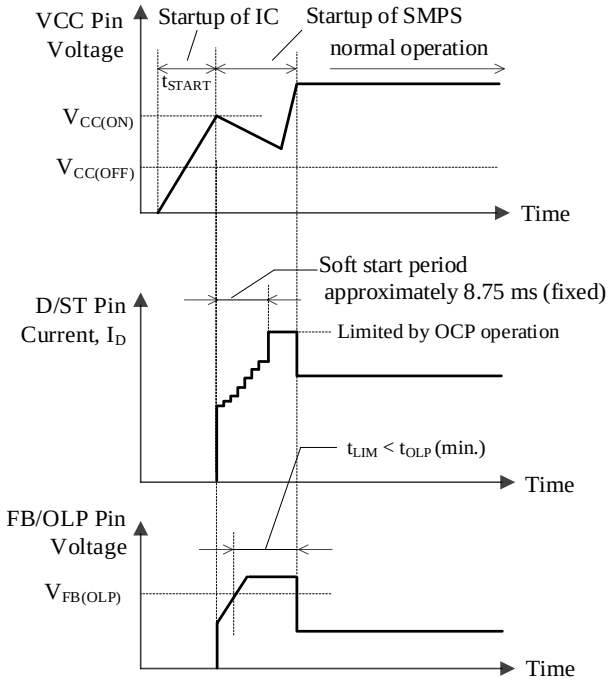

Figure 10-4. V_{CC} and I_D Waveforms during Startup

10.5 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (refer to Section 5.Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 10-5 and Figure 10-6.

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- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 10-7. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation Function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

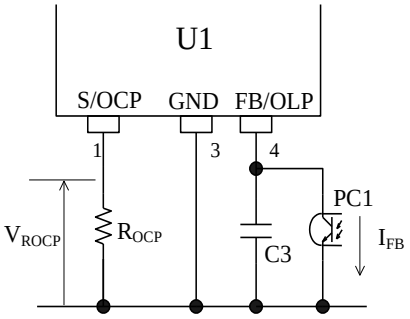

Figure 10-5. FB/OLP Pin Peripheral Circuit

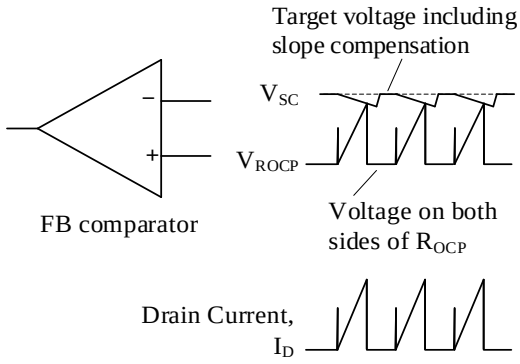

Figure 10-6. Drain Current, I_D, and FB Comparator Operation in Normal Operation

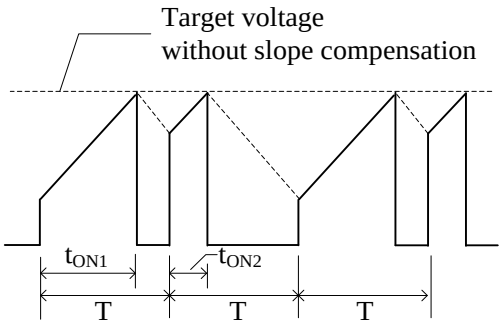

Figure 10-7. Drain current, I_D, Waveform in Subharmonic Oscillation

10.6 Leading Edge Blanking Function

The constant voltage control of output of the IC uses the peak-current-mode control method.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of a FB comparator or Overcurrent Protection (OCP) circuit to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking Time, t_{BW} = 330 ns is built-in. During t_{BW}, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V which is higher than the normal OCP threshold voltage in order not to respond to the turn-on drain current surge (refer to Section 10.9).

10.7 Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

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10.8 Automatic Standby Mode Function

Automatic standby mode is activated automatically when FB/OLP pin voltage decreases to $V_{FB(OFF)}$.

The operation mode becomes burst oscillation, as shown in Figure 10-8.

Burst oscillation mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

Generally, in order to improve efficiency under light load conditions, the frequency of the burst oscillation mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst oscillation mode, audible noises can be reduced.

If VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.6 V during the transition to the burst oscillation mode, the Bias Assist Function is activated and stabilizes the Standby mode operation, because the Startup Current, $I_{CC(ST)}$ is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist Function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and the secondary-side winding and/or reducing the value of R2 in Figure 11-2 (refer to Section 11.1)

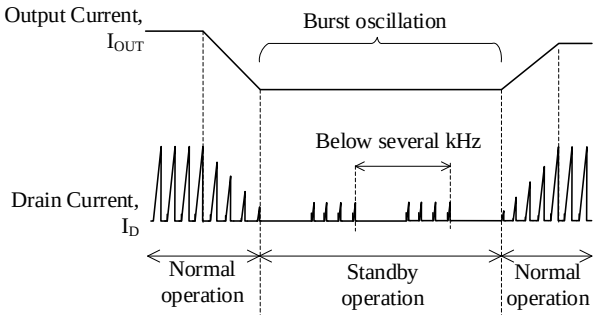

Figure 10-8. Auto Standby Mode Timing

10.9 Overcurrent Protection (OCP)

10.9.1 OCP Operation

Overcurrent Protection (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage.

During Leading Edge Blanking Time, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V which is higher than the normal OCP threshold voltage as shown in Figure 10-9. Changing to this threshold voltage prevents the IC from responding to the surge voltage in turning-on the power MOSFET. This function operates as protection at the condition such as output windings shorted or unusual withstand voltage of secondary-side rectifier diodes.

When the power MOSFET turns on, the surge voltage width of the S/OCP pin should be less than t_{BW}, as shown in Figure 10-9. In order to prevent surge voltage, pay extra attention to R_{OCP} trace layout (refer to Section 11.2). In addition, if a C (RC) damper snubber of Figure 10-10 is used, reduce the capacitor value of damper snubber.

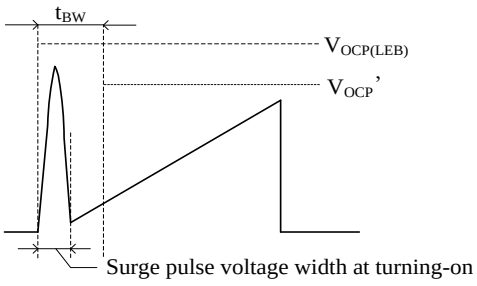

Figure 10-9. S/OCP Pin Voltage

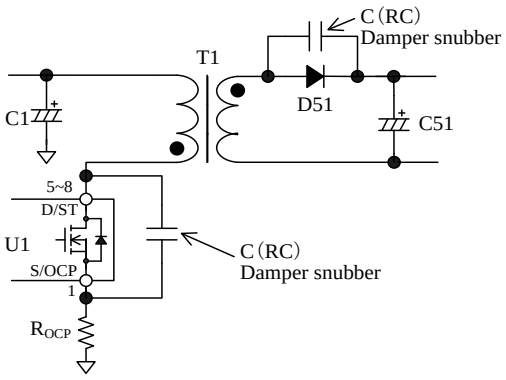

Figure 10-10. Damper Snubber

10.9.2 OCP Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to V_{OCP}. Thus, the peak current has some variation depending on AC input voltage in OCP state. In order to reduce the variation of peak current in OCP state, the IC has Input Compensation Function.

This function corrects OCP threshold voltage depending on AC input voltage, as shown in Figure 10-11.

When AC input voltage is low (ON Duty is broad), the OCP threshold voltage is controlled to become high. The difference of peak drain current become small compared with the case where the AC input voltage is high (ON Duty is narrow).

The compensation signal depends on ON Duty. The relation between the ON Duty and the OCP threshold voltage after compensation V_{OCP}' is expressed as

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Equation (3). When ON Duty is broader than 36 %, the V_{OCP}' becomes a constant value $V_{OCP(H)}$ = 0.888 V

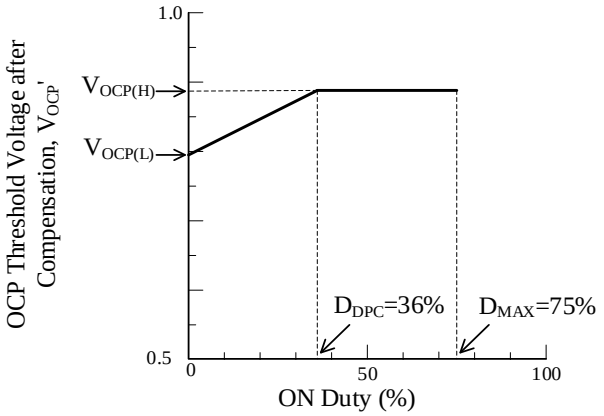

Figure 10-11. Relationship between Duty Cycle and Drain Current Limit after Compensation

$$V_{OCP}' = V_{OCP(L)} + DPC \times ONTime$$

$$= V_{OCP(L)} + DPC \times \frac{ONDuty}{f_{OSC(AVG)}} \quad (3)$$

Where,
$V_{OCP(L)}$: OCP Threshold Voltage at Zero ON Duty (V)
DPC: OCP Compensation Coefficient (mV/μs)
ONTime: On-time of power MOSFET (μs)
ONDuty: On duty of power MOSFET (%)
$f_{OSC(AVG)}$: Average PWM Switching Frequency (kHz)

10.10 Overload Protection (OLP)

Figure 10-12 shows the FB/OLP pin peripheral circuit, and Figure 10-13 shows each waveform for Overload Protection (OLP) operation.

When the peak drain current of I_D is limited by Overcurrent Protection operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 7.3 V or more for the OLP delay time, t_{OLP} = 75 ms or more, the OLP is activated, the IC stops switching operation.

During OLP operation, Bias Assist Function is disabled. Thus, VCC pin voltage decreases to $V_{CC(OFF)}$, the control circuit stops operation. After that, the IC reverts to the initial state by UVLO circuit, and the IC starts operation when VCC pin voltage increases to $V_{CC(ON)}$ by startup current. Thus the intermittent operation by UVLO is repeated in OLP state.

This intermittent operation reduces the stress of parts such as a power MOSFET and secondary side rectifier diodes. In addition, this operation reduces power consumption because the switching period in this intermittent operation is short compared with oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

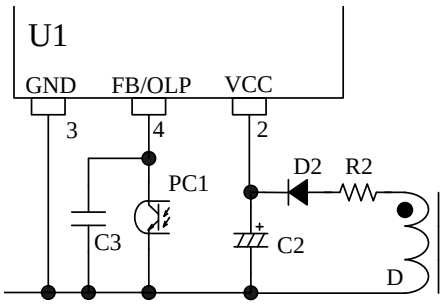

Figure 10-12. FB/OLP Pin Peripheral Circuit

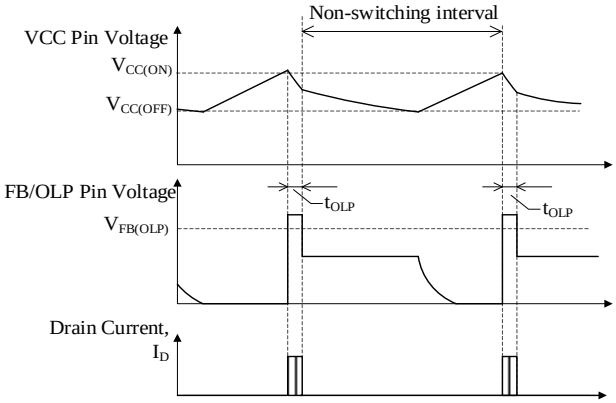

Figure 10-13. OLP Operational Waveforms

10.11 Overvoltage Protection (OVP)

When a voltage between the VCC pin and the GND pin increases to $V_{CC(OVP)}$ = 29.1 V or more, Overvoltage Protection (OVP) is activated. The IC has two operation types of OVP. One is the latched shutdown. The other is the auto restart.

When VCC pin voltage is provided by using auxiliary winding of transformer, the VCC pin voltage is proportional to output voltage. Thus, the VCC pin can detect the overvoltage conditions such as output voltage detection circuit open. The approximate value of the output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.1\ (V) \quad (4)$$

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Where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

10.11.1Latched Shutdown type (STR3A2××)

When the OVP is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$. Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

10.11.2Auto Restart Type (STR3A2××D)

When the OVP is activated, the IC stops switching operation. During OVP operation, the Bias Assist Function is disabled, the intermittent operation by UVLO is repeated (refer to Section 10.10). When the fault condition is removed, the IC returns to normal operation automatically (refer to Figure 10-14).

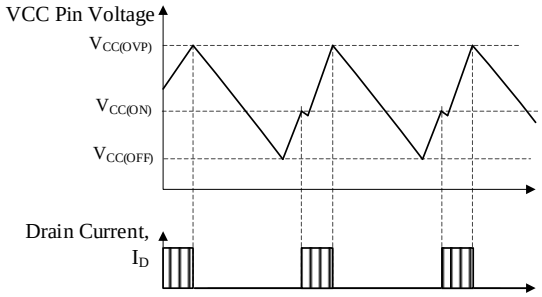

Figure 10-14. OVP Operational Waveforms

10.12 Thermal Shutdown (TSD)

When the temperature of control circuit increases to $T_{j(TSD)}$ = 145 °C or more, Thermal Shutdown (TSD) is activated. The IC has two operation types of TSD. One is latched shutdown, the other is auto restart.

10.12.1Latched Shutdown type (STR3A2××)

When the TSD is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.
Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

10.12.2Auto Restart Type (STR3A2××D)

Figure 10-15 shows the TSD operational waveforms.

When Thermal Shutdown (TSD) is activated, and the IC stops switching operation. After that, VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and the VCC pin voltage is kept to over the $V_{CC(OFF)}$.

When the temperature reduces to less than $T_{j(TSD)}-T_{j(TSD)HYS}$, the Bias Assist Function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$. At that time, the IC stops operation and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$, and the IC starts switching operation again.

In this way, the intermittent operation by the TSD and the UVLO is repeated while there is an excess thermal condition. When the fault condition is removed, the IC returns to normal operation automatically.

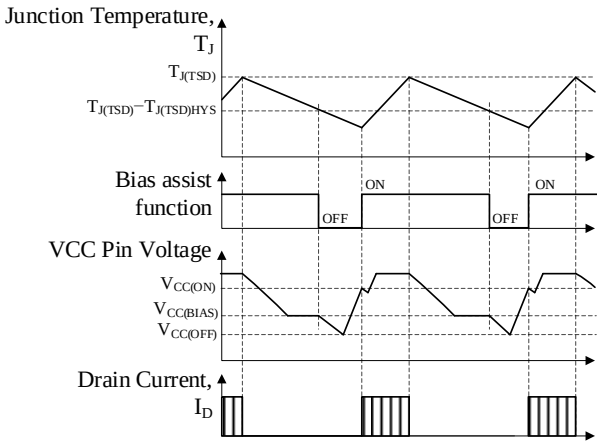

Figure 10-15. TSD Operational Waveforms

11. Design Notes

11.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

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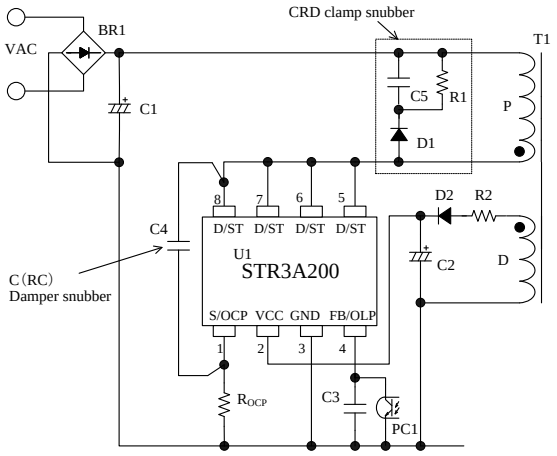

Figure 11-1. The IC Peripheral Circuit

- **Input and Output Electrolytic Capacitor**
  Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

- **S/OCP Pin Peripheral Circuit**
  In Figure 11-1, R_{OCP} is the resistor for the current detection. A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

- **VCC Pin Peripheral Circuit**
  The value of C2 in Figure 11-1 is generally recommended to be 10 µF to 47 µF (refer to Section 10.1 Startup Operation, because the startup time is determined by the value of C2)
  In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 11-2), and the Overvoltage Protection (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.
  For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 11-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

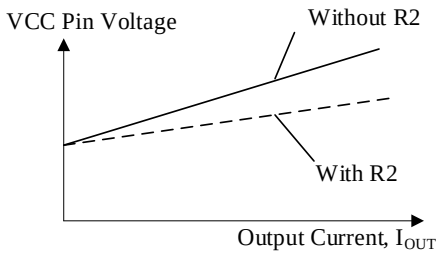

Figure 11-2. Variation of VCC Pin Voltage and Power

- **FB/OLP Pin Peripheral Circuit**
  C3 (see Figure 11-1) is for high frequency noise rejection and phase compensation, and should be connected close to the FB/OLP pin and the GND pin. The value of C3 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

- **Snubber Circuit**
  If the serge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 11-1);
  - A clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P.
  - A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/GND pin.
    In case the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

- **Peripheral circuit of secondary side shunt regulator**
  Figure 11-3 shows the secondary side detection circuit with the standard shunt regulator IC (U51).
  C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047 µF to 0.47 µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

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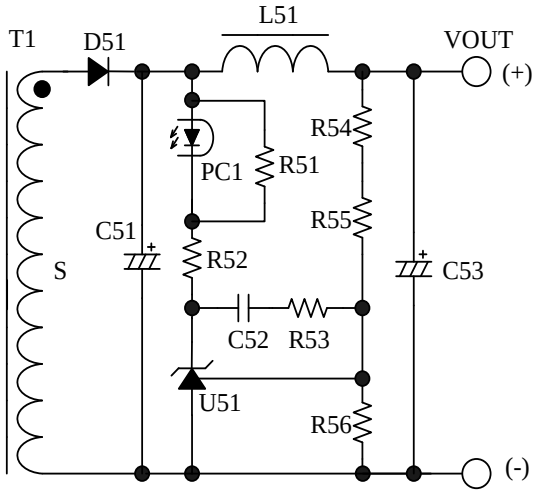

Figure 11-3. Peripheral Circuit of Secondary-side Shunt Regulator (U51)

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● **Transformer**

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage Protection (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3···) should be maximized to improve the line-regulation of those outputs.

Figure 11-4 shows the winding structural examples of two outputs.

Winding structural example (a):

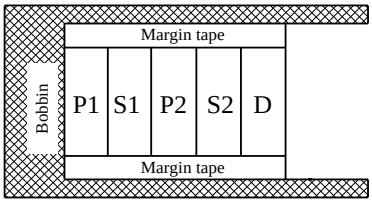
S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.

D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

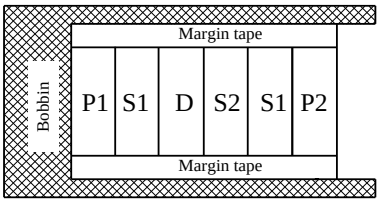
Winding structural example (b)

P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.

D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.



Winding structural example (a)



Winding structural example (b)

Figure 11-4. Winding Structural Examples

11.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 11-5 shows the circuit design example.

(1) Main Circuit Trace Layout:

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout

Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 11-5 as close to the R_{OCP} pin as possible.

(3) VCC Trace Layout:

This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other or additional capacitors for noise suppression are required, placing a high-frequency ceramic capacitor equivalent to X7R (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

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(4) R_{OCP} Trace Layout
R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 11-5) which is close to the base of R_{OCP}.

(5) FB/OLP Trace Layout
The components connected to FB/OLP pin should be as close to FB/OLP pin as possible. The trace between the components and FB/OLP pin should be as short as possible.

(6) Secondary Rectifier Smoothing Circuit Trace Layout:
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations
Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.

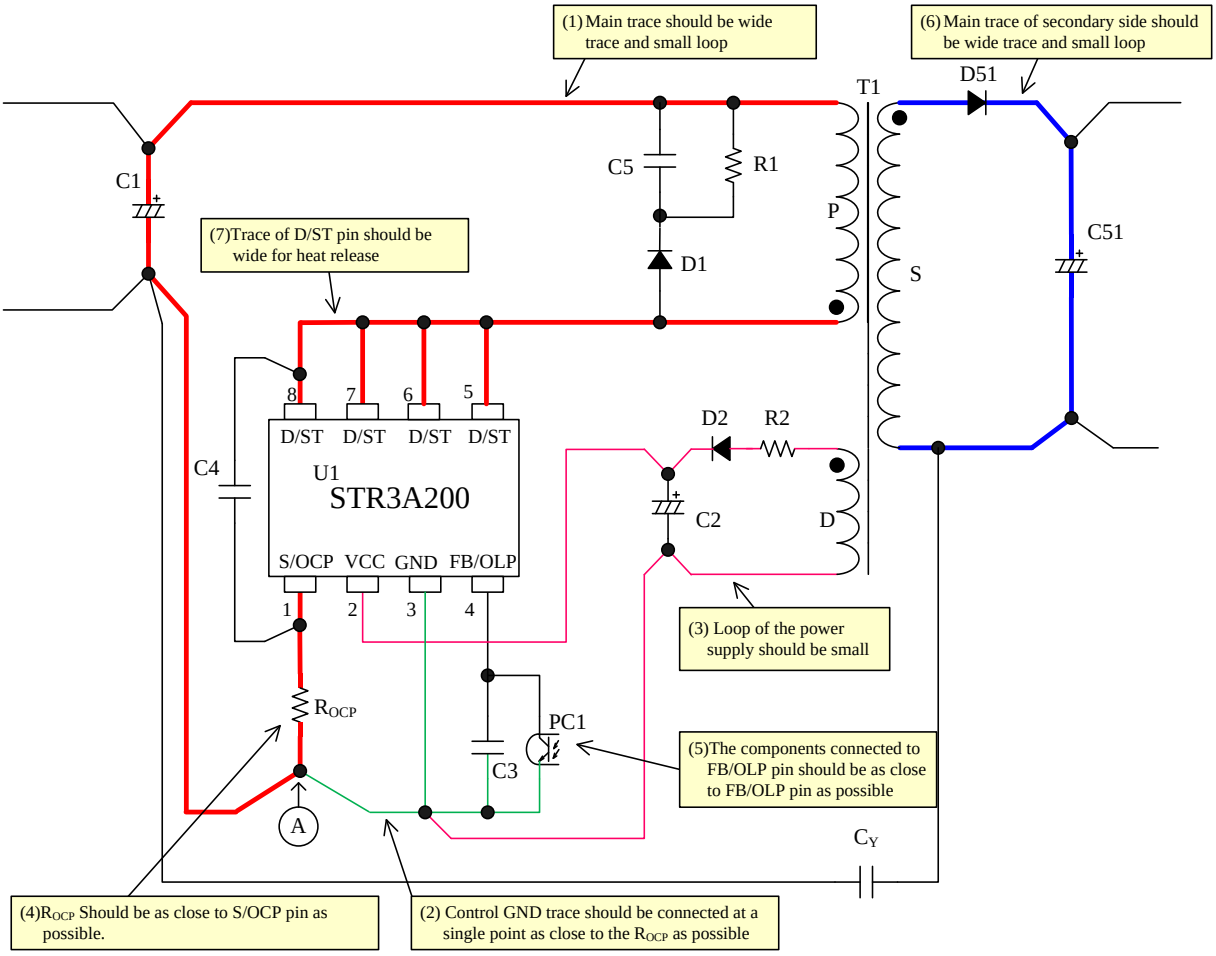

Figure 11-5. Peripheral Circuit Example around the IC

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12. Pattern Layout Example

The following show the two outputs PCB pattern layout example and the schematic of circuit using the STR3A200 series. The PCB pattern layout example is made usable to other ICs in common. The parts in Figure 12-1 are only used.

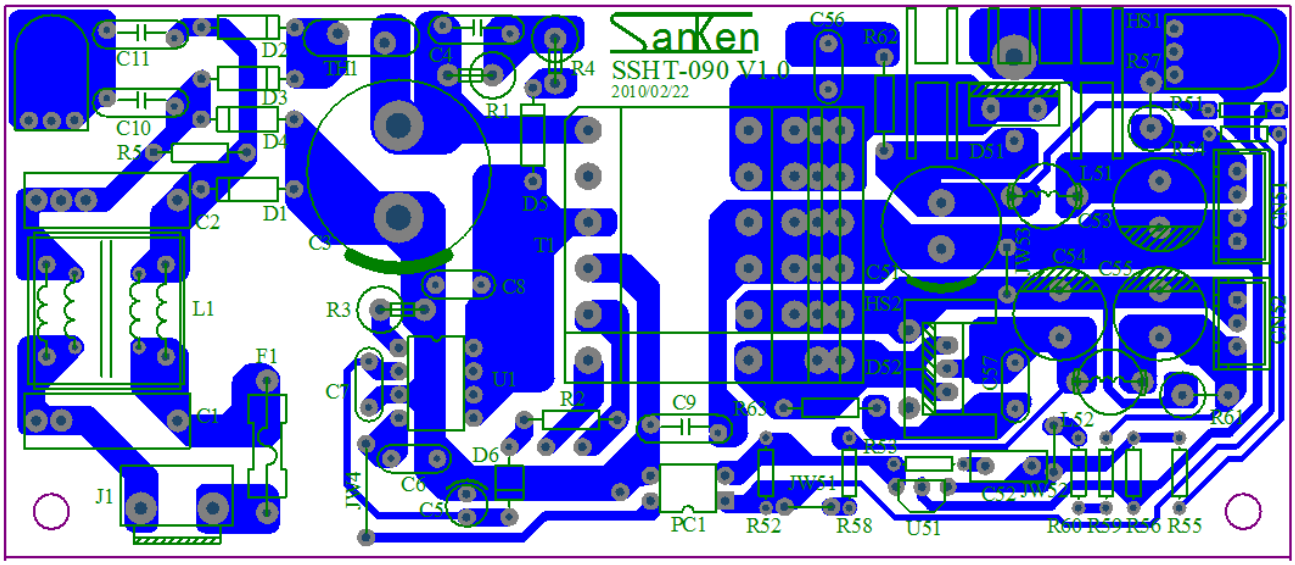

Figure 12-1. PCB Circuit Layout Example

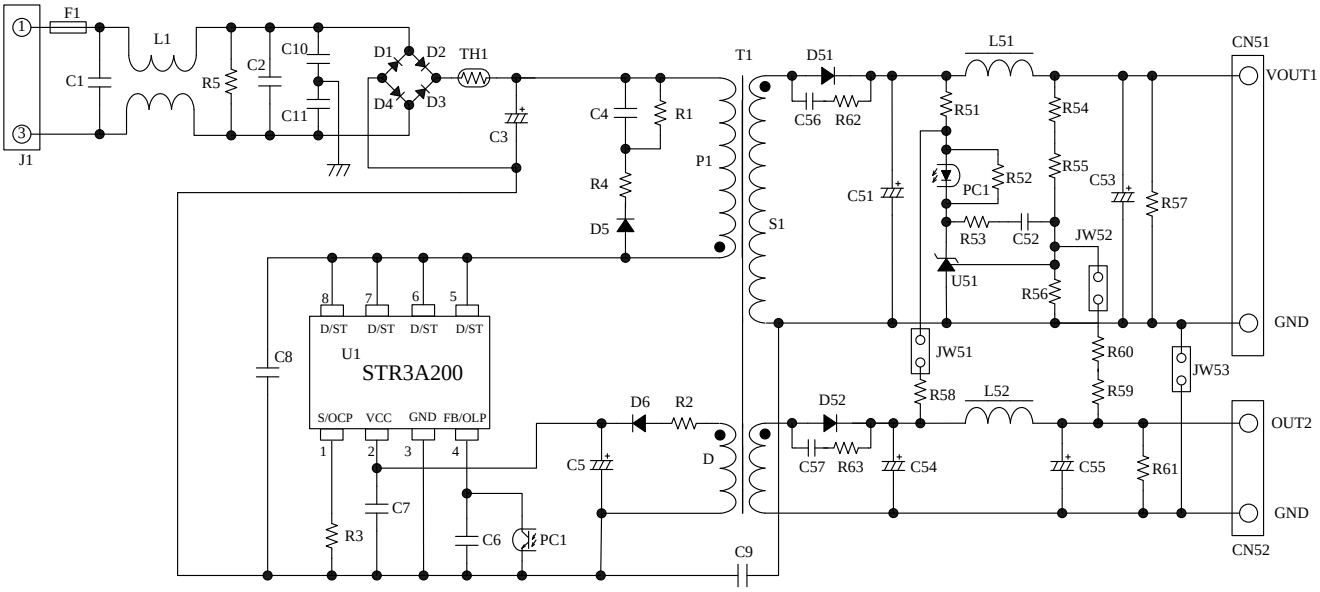

Figure 12-2. Circuit Schematic for PCB Circuit Layout

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13. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

- Power supply specification

IC	STR3A255D
Input voltage	AC85V to AC265V
Maximum output power	34.8 W (40.4 W peak)
Output 1	8 V / 0.5 A
Output 2	14 V / 2.2 A (2.6 A peak)

- Circuit schematic
  Refer to Figure 12-2

- Bill of materials

Symbol	Part type	Ratings(1)	Recommended Sanken Parts	Symbol	Part type	Ratings(1)	Recommended Sanken Parts
F1	Fuse	AC 250 V, 3 A		L51	Inductor	Short	
L1 (2)	CM inductor	3.3 mH		L52	Inductor	Short	
TH1 (2)	NTC thermistor	Short		D51	Schottky	90 V, 1.5 A	EK19
D1	General	600 V, 1 A	EM01A	D52	Schottky	150V, 10A	FMEN-210B
D2	General	600 V, 1 A	EM01A	C51 (2)	Electrolytic	680 µF, 25 V	
D3	General	600 V, 1 A	EM01A	C52 (2)	Ceramic	0.1 µF, 50 V	
D4	General	600 V, 1 A	EM01A	C53 (2)	Electrolytic	680 µF, 25 V	
D5	General	800 V, 1.2 A	SARS01	C54	Electrolytic	470 µF, 16 V	
D6	Fast recovery	200 V, 1 A	AL01Z	C55 (2)	Electrolytic	Open	
C1 (2)	Film, X2	0.1 µF, 275 V		C56 (2)	Ceramic	Open	
C2 (2)	Electrolytic	Open		C57 (2)	Ceramic	Open	
C3	Electrolytic	150 µF, 400 V		R51	General	Open	
C4	Ceramic	1000 pF, 2 kV		R52	General	1.5 kΩ	
C5	Electrolytic	22 µF, 50 V		R53 (2)	General	47 kΩ	
C6 (2)	Ceramic	0.01 µF		R54	General	Open, 1%	
C7 (2)	Ceramic	Open		R55	General	Open, 1%	
C8 (2)	Ceramic	15 pF / 2 kV		R56	General	10 kΩ, 1%	
C9	Ceramic, Y1	2200 pF, 250 V		R57	General	Open	
C10 (2)	Ceramic	Open		R58	General	1 kΩ	
C11 (2)	Ceramic	Open		R59 (2)	General	6.8 kΩ	
R1 (3)	Metal oxide	330 kΩ, 1 W		R60	General	39 kΩ, 1%	
R2 (2)	General	10 Ω		R61	General	Open	
R3 (2)	General	0.47 Ω, 1/2 W		R62 (2)	General	Open	
R4 (2)	General	47 Ω, 1 W		R63 (2)	General	Open	
R5 (3)	Metal oxide	Open		JW51		Short	
PC1	Photo-coupler	PC123 or equiv		JW52		Short	
U1	IC	—	STR3A255D	JW53		Short	
T1	Transformer	See the specification		U51	Shunt regulator	V_{REF} = 2.5 V TL431 or equiv	

(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

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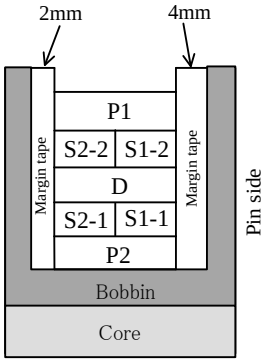
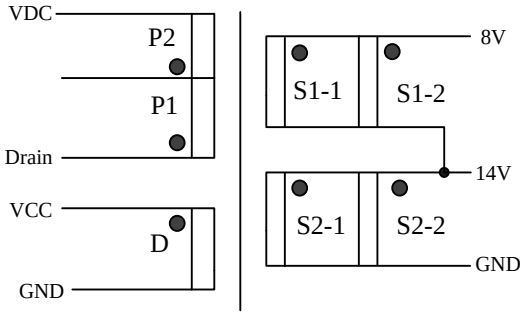
● Transformer specification

- Primary inductance, L_P : 518 μH
- Core size : EER-28
- Al-value : 245 nH/N^2 (Center gap of about 0.56 mm)
- Winding specification

Winding	Symbol	Number of turns (T)	Wire diameter (mm)	Construction
Primary winding	P1	18	φ 0.23 × 2	Single-layer, solenoid winding
Primary winding	P2	28	φ 0.30	Single-layer, solenoid winding
Auxiliary winding	D	12	φ 0.30 × 2	Solenoid winding
Output 1 winding	S1-1	6	φ 0.4 × 2	Solenoid winding
Output 1 winding	S1-2	6	φ 0.4 × 2	Solenoid winding
Output 2 winding	S2-1	4	φ 0.4 × 2	Solenoid winding
Output 2 winding	S2-2	4	φ 0.4 × 2	Solenoid winding



Cross-section view



●: Start at this pin

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