LLC Current-Resonant Off-Line Switching Controller

SSC3S931

Data Sheet

Description

The SSC3S931 is a controller with SMZ* method for LLC current resonant switching power supplies, incorporating a floating drive circuit for a high-side power MOSFET. The product includes useful functions such as the automatic dead time adjustment and the capacitive mode detection.

The product achieves high efficiency, low noise, and high cost-effective power supply systems with few external components.

*SMZ is the soft-switched multi-resonant zero current switch, and is achieved soft switching operation during all switching periods.

Package

SOP18



Not to scale

Features

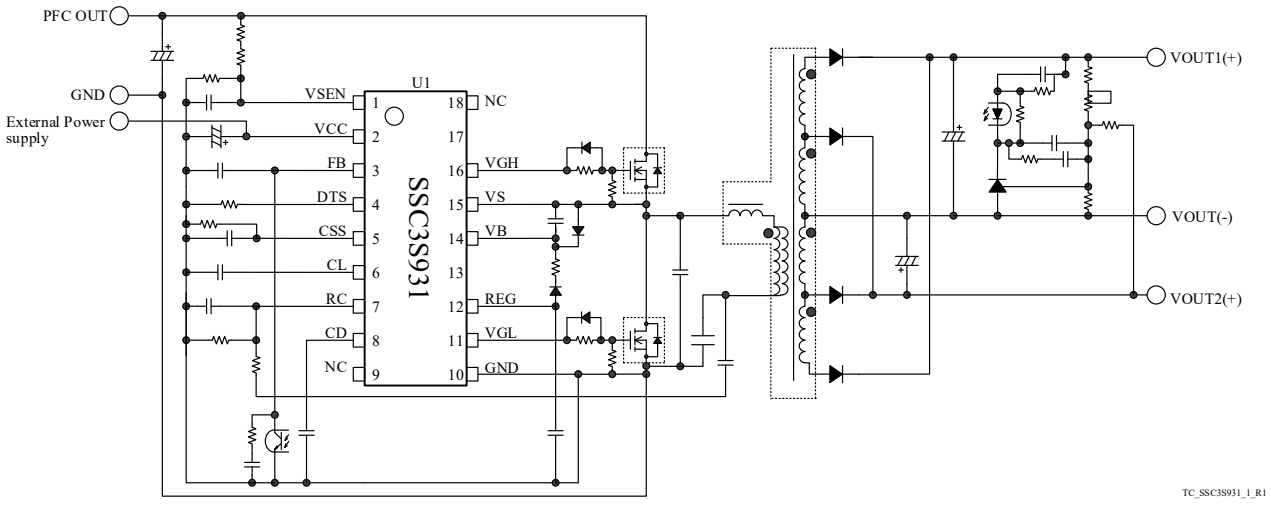
- Soft Start Function
- Capacitive Mode Detection Function
- Reset Detection Function
- Automatic Dead Time Adjustment Function
- Protections
  - High-side Driver UVLO: Auto-restart
  - VCC Pin Output Overvoltage Protection (VCC_OVP): Latched Shutdown
  - Input Overvoltage Protection (HVP): Latched Shutdown
  - Input Undervoltage Protection (UVP): Auto-restart
  - Overcurrent Protection (OCP): Auto-restart, peak drain current detection, 2-step detection
  - Overload Protection (OLP): Latched Shutdown
  - Optocoupler Open Protection (OOP): Latched Shutdown
  - Thermal Shutdown (TSD) : Latched Shutdown

Applications

Switching power supplies for electronic devices such as:

- Audio Visual (AV) Equipment
- Office Automation (OA) Equipment
- Industrial Apparatus
- Communication Facilities

Typical Application



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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25°C.

Characteristic	Symbol	Pins	Rating	Unit
VSEN Pin Sink Current	I_{SEN}	1 − 10	1.0	mA
Control Part Input Voltage	V_{CC}	2 − 10	−0.3 to 35	V
FB Pin Voltage	V_{FB}	3 − 10	−0.3 to 6	V
DTS Pin Voltage	V_{DTS}	4 − 10	−0.3 to V_{REG}	V
CSS Pin Voltage	V_{CSS}	5 − 10	−0.3 to 6	V
CL Pin Voltage	V_{CL}	6 − 10	−0.3 to 6	V
RC Pin Voltage	V_{RC}	7 − 10	−6 to 6	V
CD Pin Voltage	V_{CD}	8 − 10	−0.3 to 6	V
VGL Pin Voltage	V_{GL}	11 − 10	−0.3 to V_{REG} + 0.3	V
REG Pin Source Current	I_{REG}	12 − 10	−10.0	mA
Voltage Between VB Pin and VS Pin	V_B−V_S	14 − 15	−0.3 to 20.0	V
VS Pin Voltage	V_S	15 − 10	−1 to 600	V
VGH Pin Voltage	V_{GH}	16 − 10	V_S − 0.3 to V_B + 0.3	V
Operating Ambient Temperature	T_{OP}	—	−40 to 85	°C
Storage Temperature	T_{STG}	—	−40 to 125	°C
Junction Temperature	T_J	—	150	°C

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2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25 °C, V_{CC} is 15 V.

Characteristic	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Start Circuit and Circuit Current							
Operation Start Voltage	$V_{CC(ON)}$		2 − 10	10.5	11.9	13.1	V
Operation Stop Voltage	$V_{CC(OFF)}$		2 − 10	9.0	10.0	11.1	V
Circuit Current in Operation	$I_{CC(ON)}$		2 − 10	—	—	10.0	mA
Circuit Current in Non-Operation	$I_{CC(OFF)}$	V_{CC} = 10 V	2 − 10	—	0.7	1.5	mA
Circuit Current in Protection	$I_{CC(P)}$	V_{CC} = 12 V	2 − 10	—	2.0	2.7	mA
Latched State Release VCC Pin Threshold Voltage	$V_{CC(L.OFF)}$		2 − 10	9.0	10.0	11.1	V
Oscillator							
Minimum Frequency	$f_{(MIN)}$		11 – 10 16 – 15	27.5	31.5	35.5	kHz
Maximum Frequency	$f_{(MAX)}$		11 – 10 16 – 15	230	300	380	kHz
Minimum Dead-Time	$t_{d(MIN)}$		11 – 10 16 – 15	0.04	0.24	0.44	µs
Maximum Dead-Time	$t_{d(MAX)}$		11 – 10 16 – 15	1.20	1.65	2.20	µs
Externally Adjusted Minimum Frequency 1	$f_{(MIN)ADJ1}$	R_{CSS} = 30 kΩ	11 – 10 16 – 15	69	73	77	kHz
Externally Adjusted Minimum Frequency 2	$f_{(MIN)ADJ2}$	R_{CSS} = 77 kΩ	11 – 10 16 – 15	42.4	45.4	48.4	kHz
Feedback Control							
FB Pin Oscillation Start Threshold Voltage	$V_{FB(ON)}$		3 – 10	0.15	0.30	0.45	V
FB Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		3 – 10	0.05	0.20	0.35	V
FB Pin Maximum Source Current	$I_{FB(MAX)}$	V_{FB} = 0 V	3 – 10	−2.2	−1.6	−1.0	mA
FB Pin Reset Current	$I_{FB(R)}$	V_{CC} = 10 V, V_{FB} = 5.5 V	3 – 10	3.5	7.0	11.5	mA
Soft-start							
CSS Pin Charging Current	$I_{CSS(C)}$		5 – 10	−120	−105	−90	µA
CSS Pin Reset Current	$I_{CSS(R)}$	V_{CC} = 10V, V_{CSS} = 3 V	5 – 10	1.1	1.8	2.5	mA
Maximum Frequency in Soft-start	$f_{(MAX)SS}$		11 – 10 16 – 15	400	500	600	kHz
Dead Time							
DTS Pin Voltage in Normal Operation	$V_{DTS(OP)}$		4 – 10	0	1	2	V
DTS Pin Threshold Voltage	V_{DTS}		4 – 10	—	1.9	—	V
DTS Pin Source Current	I_{DTS}	V_{CC} = 10 V, V_{DTS}= 0 V	4 – 10	−12.0	−10.2	−8.5	µA
Reset Detection							
Maximum Reset Time	$t_{RST(MAX)}$		11 – 10 16 – 15	4	5	6	µs
Driver Circuit Power Supply							
REG Pin Output Voltage	V_{REG}		12 – 10	9.6	10.0	10.8	V

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Characteristic	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
High-side Driver							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		14 – 15	5.7	6.8	7.9	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		14 – 15	5.5	6.4	7.3	V
Driver Circuit							
VGL, VGH Pin Source Current 1	$I_{GL(SRC)1}$ $I_{GH(SRC)1}$	V_{REG} = 10.5 V, V_B = 10.5 V, V_{GL} = 0 V, V_{GH} = 0 V	11 – 10 16 – 15	—	–540	—	mA
VGL, VGH Pin Sink Current 1	$I_{GL(SNK)1}$ $I_{GH(SNK)1}$	V_{REG} = 10.5 V, V_B = 10.5 V, V_{GL} = 10.5 V, V_{GH} = 10.5 V	11 – 10 16 – 15	—	1.50	—	A
VGL, VGH Pin Source Current 2	$I_{GL(SRC)2}$ $I_{GH(SRC)2}$	V_{REG} = 11.5 V, V_B = 11.5 V, V_{GL} = 10 V, V_{GH} = 10 V	11 – 10 16 – 15	−140	−90	−40	mA
VGL, VGH Pin Sink Current 2	$I_{GL(SNK)2}$ $I_{GH(SNK)2}$	V_{REG} = 11.5 V, V_B = 11.5 V, V_{GL} = 1.5 V, V_{GH} = 1.5 V	11 – 10 16 – 15	140	230	360	mA
VCC Pin Overvoltage Protection (VCC_OVP)							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 10	30.0	32.0	34.0	V
Current Resonant and Overcurrent Protection(OCP)							
Capacitive Mode Detection Voltage 1	V_{RC1}		7 – 10	0.02	0.10	0.18	V
				−0.18	−0.10	−0.02	V
Capacitive Mode Detection Voltage 2	V_{RC2}		7 – 10	0.20	0.30	0.40	V
				−0.40	−0.30	−0.20	V
RC Pin Threshold Voltage (Low)	$V_{RC(L)}$		7 – 10	1.80	1.90	2.00	V
				−2.00	−1.90	−1.80	V
RC Pin Threshold Voltage (High)	$V_{RC(H)}$		7 – 10	2.62	2.80	2.98	V
				−2.98	−2.80	−2.62	V
CSS Pin Sink Current (Low)	$I_{CSS(L)}$	V_{CSS} = 3 V	5 – 10	1.1	1.8	2.5	mA
CSS Pin Sink Current (High)	$I_{CSS(H)}$	V_{CSS} = 3 V	5 – 10	13.0	20.5	28.0	mA
Overload Protection (OLP)							
CL pin OLP Threshold Voltage	$V_{CL(OLP)}$		6 – 10	3.9	4.2	4.5	V
CL Pin Source Current 1	$I_{CL(SRC)1}$	V_{CL} = 0.5 V	6 – 10	−29	−17	−5	µA
CL Pin Source Current 2	$I_{CL(SRC)2}$	V_{CL} = 3 V	6 – 10	−180	−135	−90	µA
CL Pin Sink Current	$I_{CL(SNK)}$	V_{CL} = 3 V	6 – 10	10	30	50	µA
Input Overvoltage Protection (HVP), Input Undervoltage Protection (UVP)							
VSEN Pin UVP Release Threshold Voltage	$V_{SEN(ON)}$		1 – 10	1.248	1.300	1.352	V
VSEN Pin UVP Threshold Voltage	$V_{SEN(OFF)}$		1 – 10	1.056	1.100	1.144	V
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$		1 – 10	5.3	5.6	5.9	V
VSEN Pin Clamp Voltage	$V_{SEN\ (CLAMP)}$		1 – 10	10.0	—	—	V

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Characteristic	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Optocoupler Open Protection (OOP)							
FB Pin Open Detection Threshold Voltage	$V_{FB(OOP)}$		3 – 10	4.2	4.6	5.0	V
CD Pin Threshold Voltage	V_{CD}		8 – 10	2.8	3.0	3.2	V
CD Pin Source Current	$I_{CD(SRC)}$	V_{CD} = 0 V	8 – 10	–29	–20	–11	µA
CD Pin Sink Current	$I_{CD(SNK)}$	V_{CD} = 2.5 V	8 – 10	28	43	58	µA
CD Pin Reset Current	$I_{CD(R)}$	V_{CD} = 2 V	8 – 10	1.0	2.5	4.0	mA
Thermal Shutdown (TSD)							
Thermal Shutdown Temperature	$T_{J(TSD)}$		—	140	—	—	°C
Thermal Resistance							
Junction to Ambient Thermal Resistance	θ_{J-A}		—	—	—	95	°C/W

3. Mechanical Characteristic

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.27	—	g

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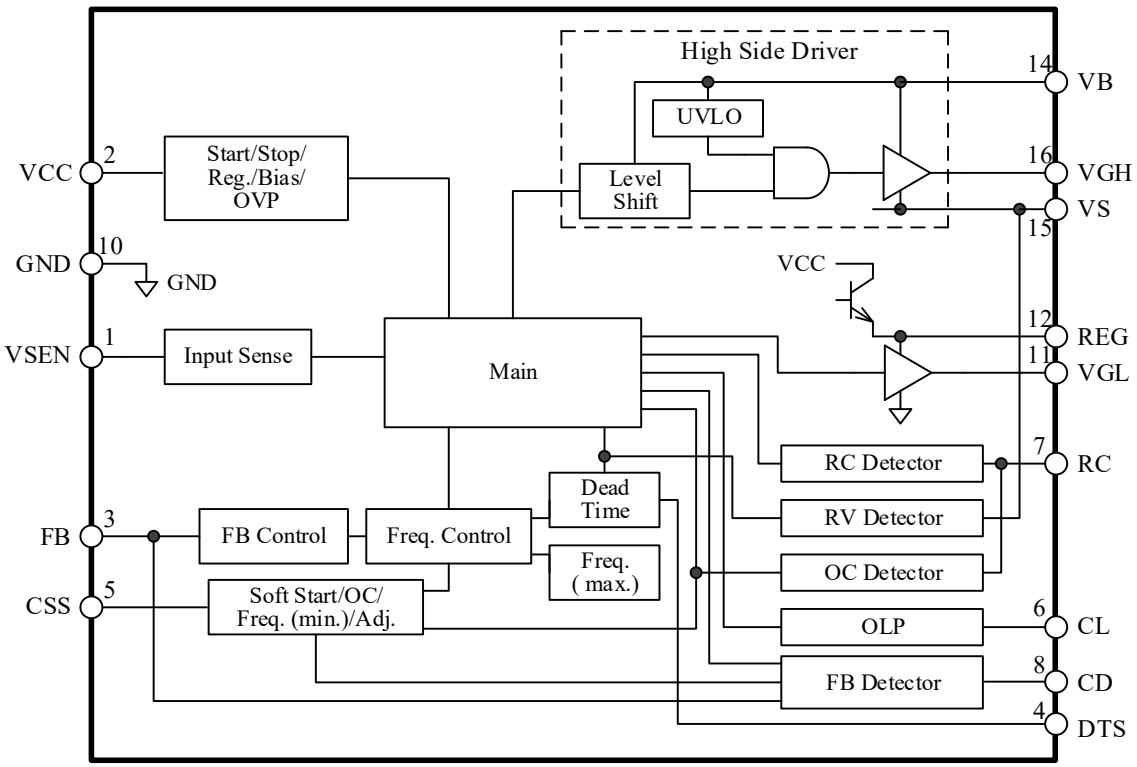
4. Block Diagram



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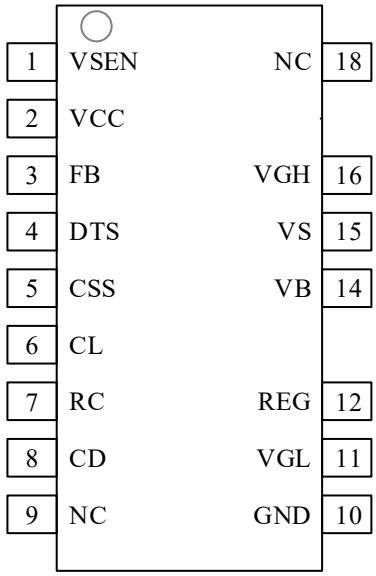
5. Pin Configuration Definitions



Number	Name	Description
1	VSEN	Mains input voltage detection signal input
2	VCC	Supply voltage input for the IC with VCC pin overvoltage protection (VCC_OVP)
3	FB	Feedback signal input for constant voltage control and optocoupler open protection (OOP) signal input
4	DTS	Dead time control selection: a fixed on the minimum value, or an automatically adjustment
5	CSS	Soft-start setting capacitor connection
6	CL	Overload detection (OLP) capacitor connection
7	RC	Resonant current detection signal input and overcurrent protection (OCP) signal input
8	CD	Delay time setting capacitor connection for optocoupler open protection (OOP)
9	NC	Not connected
10	GND	Ground
11	VGL	Low-side gate drive output
12	REG	Supply voltage output for gate drive circuit
13	—	Pin removed
14	VB	Supply voltage input for high-side driver with UVLO
15	VS	Floating ground for high-side driver
16	VGH	High-side gate drive output
17	—	Pin removed
18	NC	Not connected

6. Typical Application

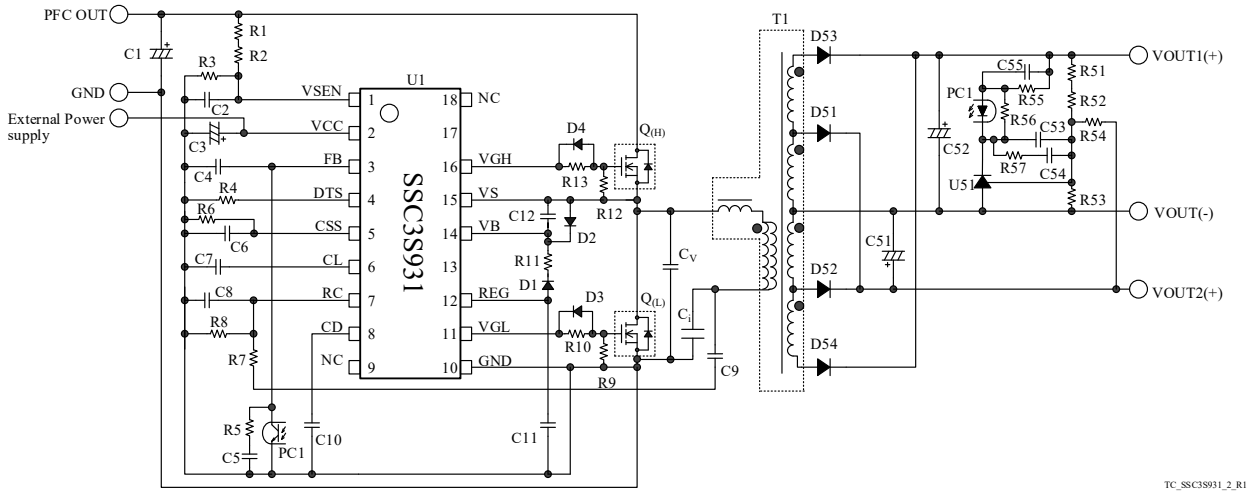


Figure 6-1. Typical Application

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7. Physical Dimensions

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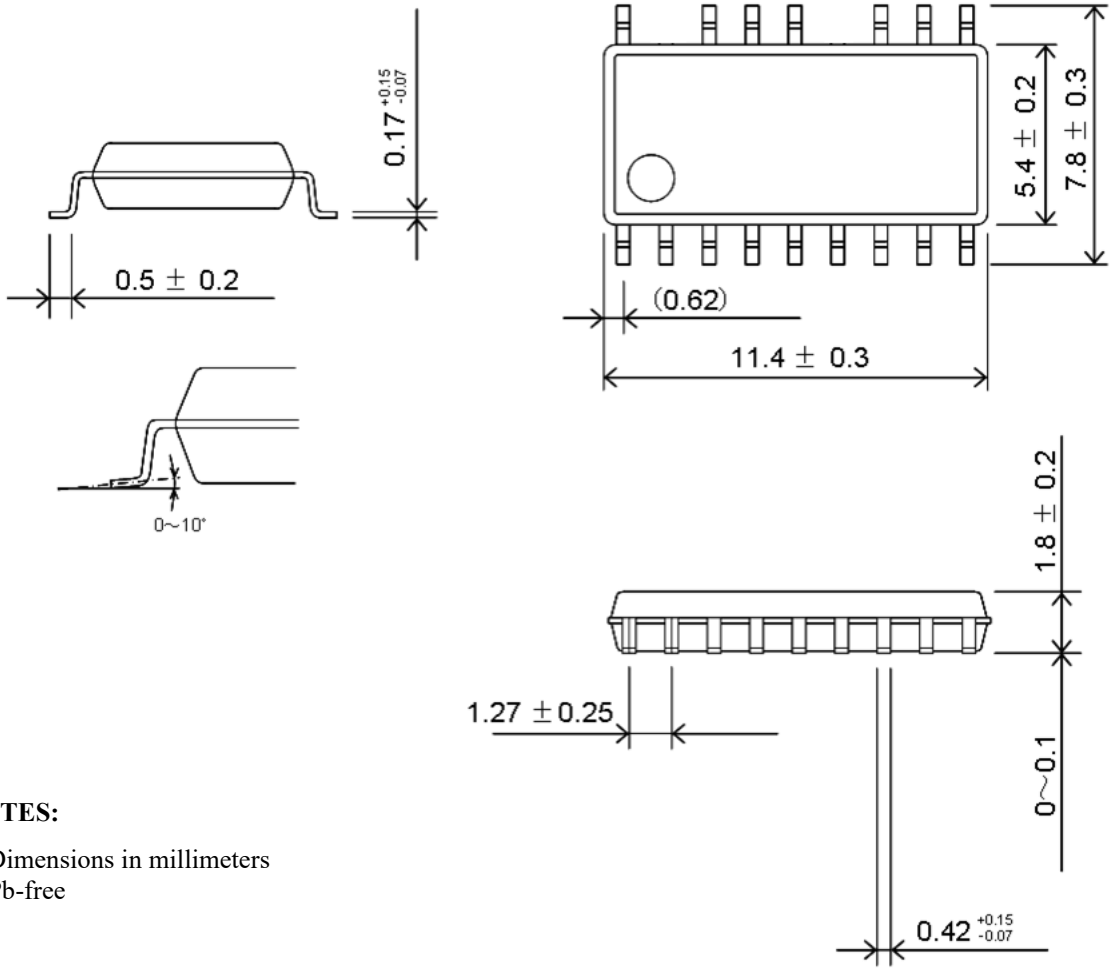
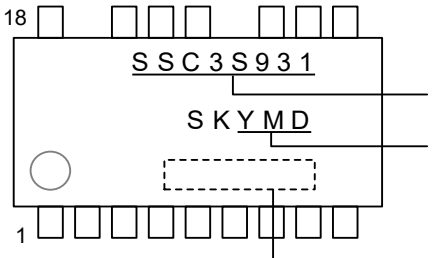


NOTES:

- Dimensions in millimeters
- Pb-free

8. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is a period of days:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

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9. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−). $Q_{(H)}$ and $Q_{(L)}$ indicate a high-side power MOSFET and a low-side power MOSFET respectively. Ci and C_V indicate a current resonant capacitor and a voltage resonant capacitor, respectively.

9.1 Resonant Circuit Operation

Figure 9-1 shows a basic RLC series resonant circuit.

The impedance of the circuit, $\dot{Z}$, is as the following Equation.

$$\dot{Z} = R + j\left(\omega L - \frac{1}{\omega C}\right), \quad (1)$$

where ω is angular frequency; and ω = 2πf.

Thus,

$$\dot{Z} = R + j\left(2\pi fL - \frac{1}{2\pi fC}\right). \quad (2)$$

When the frequency, f, changes, the impedance of resonant circuit will change as shown in Figure 9-2.

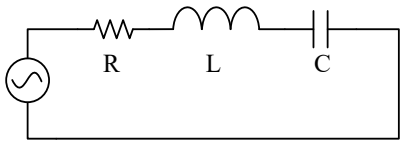

Figure 9-1. RLC Series Resonant Circuit

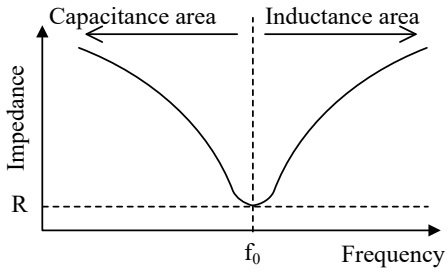

Figure 9-2. Impedance of Resonant Circuit

When 2πfL = 1/2πfC, $\dot{Z}$ of Equation (2) becomes the minimum value, R (see Figure 9-2). In the case, ω is calculated by Equation (3).

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \quad (3)$$

The frequency in which $\dot{Z}$ becomes minimum value is called a resonant frequency, f_0. The higher frequency area than f_0 is an inductance area. The lower frequency area than f_0 is a capacitance area.

From Equation (3), f_0 is as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (4)$$

Figure 9-3 shows the circuit of a current resonant power supply. The basic configuration of the current resonant power supply is a half-bridge converter. The switching devices, $Q_{(H)}$ and $Q_{(L)}$, are connected in series with V_{IN}. The series resonant circuit and the voltage resonant capacitor, C_V, are connected in parallel with $Q_{(L)}$. The series resonant circuit is consisted of the following components: the resonant inductor, L_R; the primary winding, P, of a transformer, T1; and the current resonant capacitor, C_i. The coupling between the primary and secondary windings of T1 is designed to be poor so that the leakage inductance increases. This leakage inductance is used for L_R. This results in a down sized of the series resonant circuit. The dotted mark with T1 describes the winding polarity, the secondary windings, S1 and S2, are connected so that the polarities are set to the same position as shown in Figure 9-3. In addition, the winding numbers of each other should be equal. From Equation (1), the impedance of a current resonant power supply is calculated by Equation (5). From Equation (4), the resonant frequency, f_0, is calculated by Equation (6).

$$\dot{Z} = R + j\left\{\omega(L_R + L_P) - \frac{1}{\omega Ci}\right\}, \quad (5)$$

$$f_0 = \frac{1}{2\pi\sqrt{(L_R + L_P) \times Ci}}, \quad (6)$$

where:
R is the equivalent resistance of load,
L_R is the inductance of the resonant inductor,
L_P is the inductance of the primary winding P, and
Ci is the capacitance of current resonant capacitor.

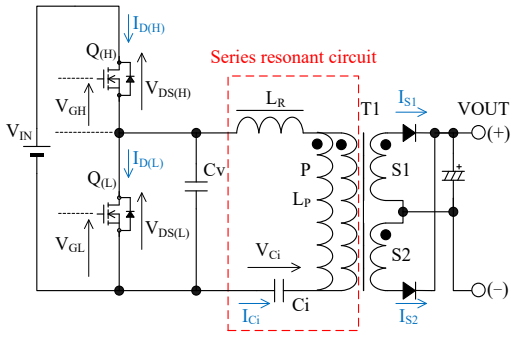

Figure 9-3. Current Resonant Power Supply Circuit

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In the current resonant power supply, $Q_{(H)}$ and $Q_{(L)}$ are alternatively turned on and off. The on and off times of them are equal. There is a dead time between the on periods of $Q_{(H)}$ and $Q_{(L)}$. During the dead time, $Q_{(H)}$ and $Q_{(L)}$ are in off status.

In the current resonant power supply, the frequency is controlled. When the output voltage decreases, the IC decreases the switching frequency so that the output power is increased to keep a constant output voltage. This must be controlled in the inductance area ($f_{SW} > f_0$). Since the winding current is delayed from the winding voltage in the inductance area, the turn-on operates in a ZCS (Zero Current Switching); and the turn-off operates in a ZVS (Zero Voltage Switching). Thus, the switching losses of $Q_{(H)}$ and $Q_{(L)}$ are nearly zero. In the capacitance area ($f_{SW} < f_0$), the current resonant power supply operates as follows: When the output voltage decreases, the switching frequency is decreased; and then, the output power is more decreased. Therefore, the output voltage cannot be kept constant. Since the winding current goes ahead of the winding voltage in the capacitance area, $Q_{(H)}$ and $Q_{(L)}$ operate in the hard switching. This results in the increases of a power loss. This operation in the capacitance area is called the capacitive mode operation. The current resonant power supply must be operated without the capacitive mode operation (for more details, see Section 9.8).

Figure 9-4 describes the basic operation waveform of current resonant power supply (see Figure 9-3 about the symbol in Figure 9-4). For the description of current resonant waveforms in normal operation, the operation is separated into a period A to F. In the following description:

$I_{D(H)}$ is the current of $Q_{(H)}$,
$I_{D(L)}$ is the current of $Q_{(L)}$,
$V_{F(H)}$ is the forwerd voltage of $Q_{(H)}$,
$V_{F(L)}$ is the forwerd voltage of $Q_{(L)}$,
I_L is the current of L_R,
V_{IN} is an input voltage,
V_{Ci} is Ci voltage, and
V_{CV} is C_V voltage.

The current resonant power supply operations in period A to F are as follows:

1) Period A
When $Q_{(H)}$ is on, an energy is stored into the series resonant circuit by $I_{D(H)}$ that flows through the resonant circuit and the transformer (see Figure 9-5). At the same time, the energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

2) Period B
After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 9-6).

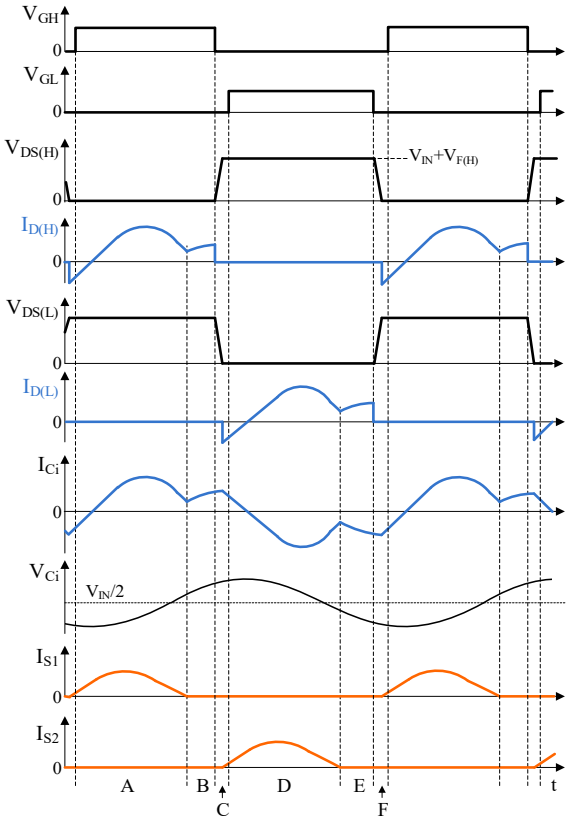

Figure 9-4. The Basic Operation Waveforms of Current Resonant Power Supply

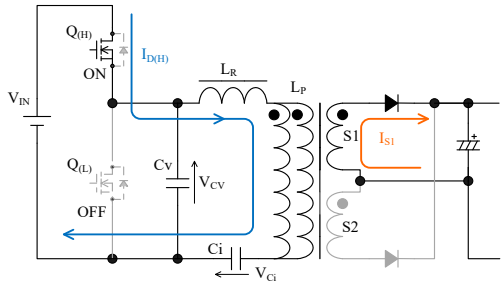

Figure 9-5. Operation in period A

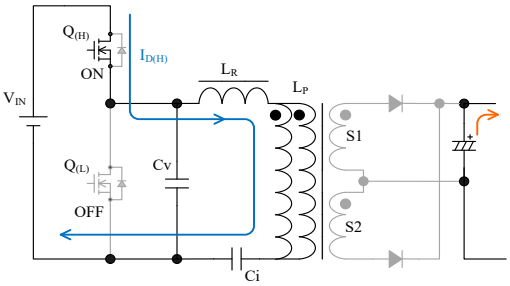

Figure 9-6. Operation in Period B

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3) Period C

C is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status. When $Q_{(H)}$ turns off, C_V is discharged by I_L that is supplied by the energy stored in the series resonant circuit applies (see Figure 9-7). When V_{CV} decreases to $V_{F(L)}$, $-I_{D(L)}$ flows through the body diode of $Q_{(L)}$; and V_{CV} is clamped to $V_{F(L)}$. After that, $Q_{(L)}$ turns on. Since $V_{DS(L)}$ is nearly zero at the point, $Q_{(L)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

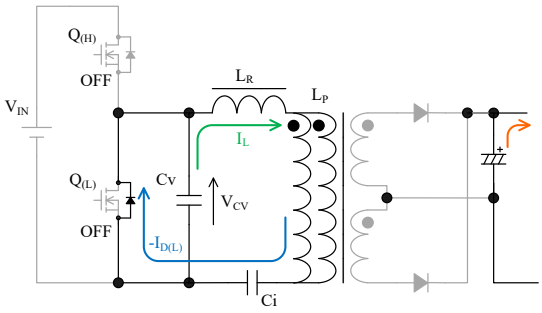

Figure 9-7. Operation in Period C

4) Period D

Immidiately after $Q_{(L)}$ turns on, $-I_{D(L)}$, which was flowing in Period C, continues to flow through $Q_{(L)}$ for a while. Then, $I_{D(L)}$ flows as shown in Figure 9-8; and V_{Ci} is applied the primary winding voltage of the transformer. At the same time, energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

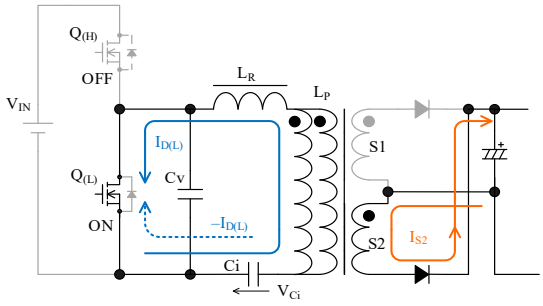

Figure 9-8. Operation in Period D

5) Period E

After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 9-9).

6) Period F

F is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status.

When $Q_{(L)}$ turns off, C_V is charged by $-I_L$ that is supplied by the energy stored in the series resonant circuit applies (see Figure 9-10). When V_{CV} increases to $V_{IN} + V_{F(H)}$, $-I_{D(H)}$ flows through body diode of $Q_{(H)}$; and V_{CV} is clamped to $V_{IN} + V_{F(H)}$. After that, $Q_{(H)}$ turns on. Since $V_{DS(H)}$ is nearly zero at the point, $Q_{(H)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

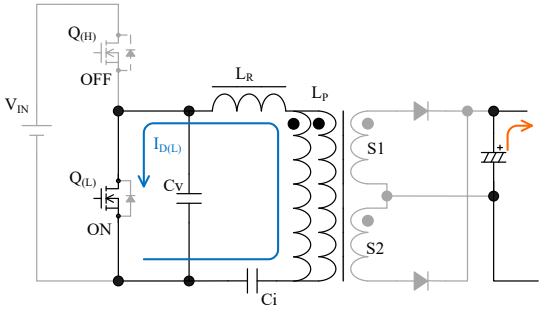

Figure 9-9. Operation in Period E

7) After the period F

Immidiately after $Q_{(H)}$ turns on, $-I_{D(H)}$, which was flowing in Period F, continues to flow through $Q_{(H)}$ for a while. Then, $I_{D(H)}$ flows again; and the operation returns to the period A. The above operation is repeated to transfer energy to the secondary side from the resonant circuit.

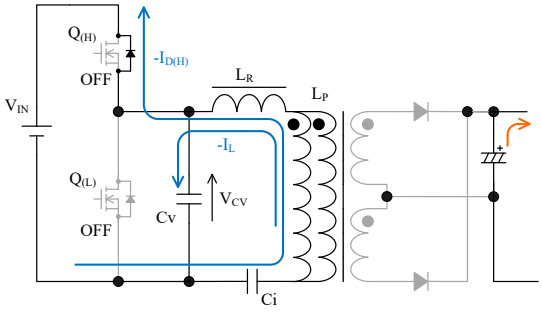

Figure 9-10. Operation in Period F

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9.2 Startup Operation

Figure 9-11 and Figure 9-12 show the VCC pin peripheral circuit and the startup waveforms, respectively. The VCC pin is a power supply input pin for a control circuit and is supplied from an external power supply. When the VCC pin voltage increases to the Operation Start Voltage, $V_{CC(ON)}$ = 11.9 V, the control circuit starts operation. When the VCC pin voltage decreases to the Operation Stop Voltage, $V_{CC(OFF)}$ = 10.0 V, the control circuit is stopped by the undervoltage lockout (UVLO) circuit, and returns to the state before startup (see Figure 9-13).

When the IC satisfies all following conditions, the IC starts a switching operation:

- VCC pin voltage ≥ $V_{CC(ON)}$ = 11.9 V
- VSEN pin voltage ≥ $V_{SEN(ON)}$ = 1.300 V
- FB pin voltage ≥ $V_{FB(ON)}$ = 0.30 V

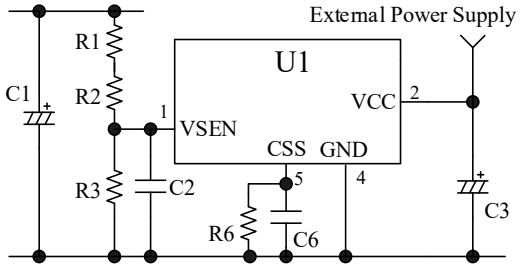

Figure 9-11. VCC Pin Peripheral Circuit

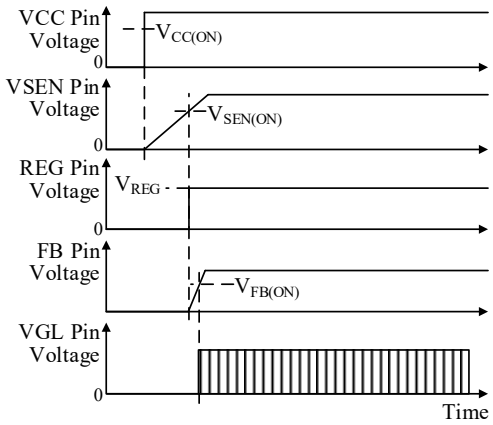

Figure 9-12. Startup Waveforms

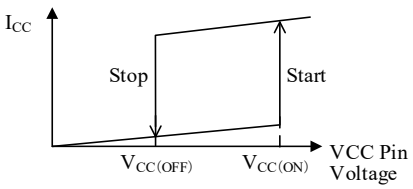

Figure 9-13. V_{CC} vs. I_{CC}

9.3 Soft Start Function

Figure 9-14 shows the soft start operation waveforms.

The IC has the soft start function to reduce stress of peripheral component, and to prevent the capacitive mode operation. During the soft start operation, C6 connected to the CSS pin is charged by the CSS Pin Charge Current, $I_{CSS(C)}$ = −105 µA. The oscillation frequency is varied according to the CSS pin voltage. The switching frequency ($f_{(MAX)SS}$ * = 500 kHz is maximum) gradually decreases according to rise the CSS pin voltage; at same time, output power increases. The IC operates with an oscillation frequency control that uses feedback signal after the output power increases. When the IC becomes any of the following conditions, C6 is discharged by the CSS Pin Reset Current, $I_{CSS(R)}$ = 1.8 mA.

- Wnen the VCC pin voltage decreases to the operation stop voltage, $V_{CC(OFF)}$ = 10.0 V, or less.
- When VSEN pin voltage is $V_{SEN(OFF)}$ = 1.100 V or less.
- When one or more following corresponding protections are activated: VCC_OVP, HVP, OLP, OOP, or TSD.

During the soft start operation, a CD pin voltage also increases. The CD pin voltage is used for the optocoupler open protection (OOP). Note that a startup failure may be occurred due to the OOP activation when the soft start period is too long. See the Section 9.14 for setting of C10 connected to the CD pin.

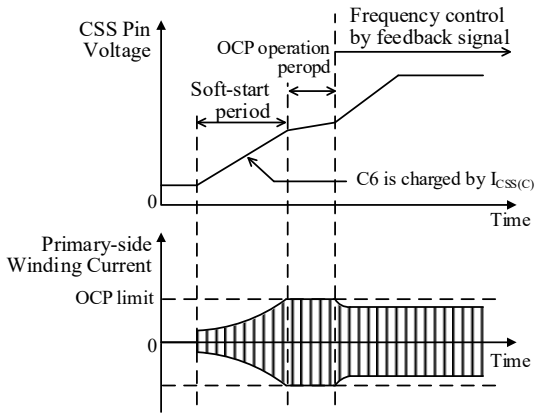

Figure 9-14. Soft Start Operation

* The maximum frequency during normal operation is $f_{(MAX)}$ = 300 kHz.

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9.4 Minimum and Maximum Switching Frequency Setting

The minimum switching frequency is determined by the resistance of R6 connected to the CSS pin. Figure 9-15 shows the relationship of R6 and $f_{(MIN)ADJ}$ that is the external adjustment minimum frequency.

The $f_{(MIN)ADJ}$ must be set more than the resonant frequency, f_0, under the condition of the minimum mains input voltage and the maximum output power. The maximum switching frequency, f_{MAX}, is determined by the inductance and the capacitance of a resonant circuit. The f_{MAX} must be set less than the maximum frequency, $f_{(MAX)}$ = 300 kHz.

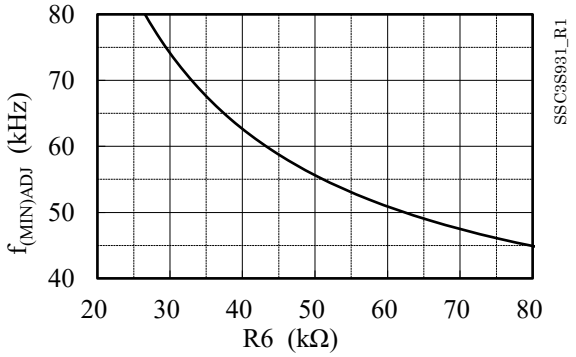

Figure 9-15. R6 vs. $f_{(MIN)ADJ}$

9.5 High-side Driver

Figure 9-16 shows the bootstrap circuit that drives $Q_{(H)}$, and is configured by D1, R11, and C12 (between the REG and VS pins).

When the $Q_{(H)}$ and $Q_{(L)}$ are an off and on statuses, the VS pin voltage becomes about ground level; and C12 is charged from the REG pin.

When the voltage between the VB and VS pins, V_{B-S}, increases to $V_{BUV(ON)}$ = 6.8 V or more, an internal high-side drive circuit starts an operation. When V_{B-S} decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the high-side drive circuit stops the operation. In case the both ends of C12 and D2 are shorted, the IC is protected by $V_{BUV(OFF)}$. D2 is for the protection against negative voltage of the VS pin

- D1
  D1 should be an ultrafast recovery diode of short recovery time and low reverse current. When the maximum mains input voltage of the apprication is 265VAC, it is recommended to use ultrafast recovery diode of V_{RM} = 600 V.

- C11, C12, and R11
  The values of C11, C12, and R11 are determined by total gate charge, Qg, of external MOSFET and voltage dip amount between the VB and VS pins in the minimum frequency operation.
  C11, C12, and R11 should be adjusted so that the voltage between the VB pin and the VS is more than $V_{BUV(ON)}$ = 6.8 V by measuring the voltage with a high-voltage differential probe.
  The reference value of C11 is 0.47μF to 1 μF.
  The time constant of C12 and R11 should be less than 500 ns. The value of C12 is 0.047μF to 0.1 μF. The value of R11 is 2.2 Ω to 10 Ω.
  C11 and C12 should be a film or a ceramic capacitor that has a low ESR and a low leakage current characteristics.

- D2
  D2 should be a Schottky diode that has a low forward voltage characteristics to avoid that V_{B-S} is −0.3 V or less, i.e., to use within its absolute maximum rating value.

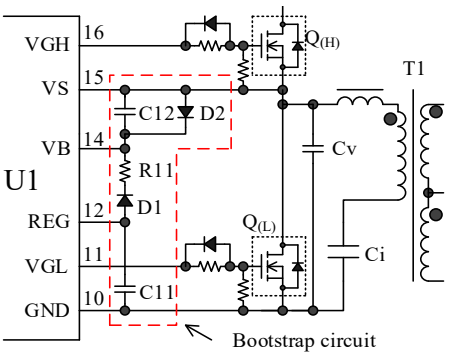

Figure 9-16. Bootstrap Circuit

9.6 Constant Voltage Control Operation

Figure 9-17 shows the FB pin peripheral circuit.

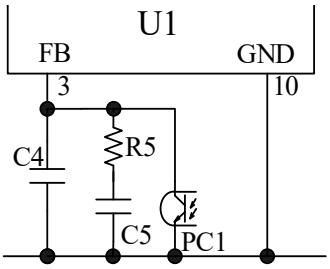

Figure 9-17. FB Pin Peripheral Circuit

The FB pin is sunk the feedback current by the photo-coupler, PC1, connected to the FB pin. As a result, the oscillation frequency is controlled to constant output voltage by the FB pin (in inductance area). Under slight load condition, the feedback current increases; and the FB pin voltage decreases. While the FB pin voltage decreases to the oscillation stop threshold voltage,

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$V_{FB(OFF)}$ = 0.20 V, or less, the IC stops switching operation. This operation reduces switching loss, and prevents the increasing of the secondary output voltage.

R5 and C5 are for a phase compensation adjustment. C4 is for a high frequency noise rejection. The secondary-side circuit should be designed so that the collector current of PC1 is >1.6 mA that is the absolute value of the maximum source current, $I_{FB(MAX)}$. Especially, the current transfer ratio, CTR, of the photo coupler should be taken an aging degradation into account.

9.7 Dead Time

The dead time is the period when both the high-side and the low-side power MOSFETs are off. If the dead time is shorter than a voltage resonant period (see Figure 9-18), the power MOSFETs turns on/off during the voltage resonant operation. In the case, the switching loss increases due to hard switching operation of the power MOSFETs.

The dead time is generated in the IC. The IC provides the following two dead time controls selected by the value of a resistor connected to the DTS pin: automatically adjustment, or fixed minimum value.

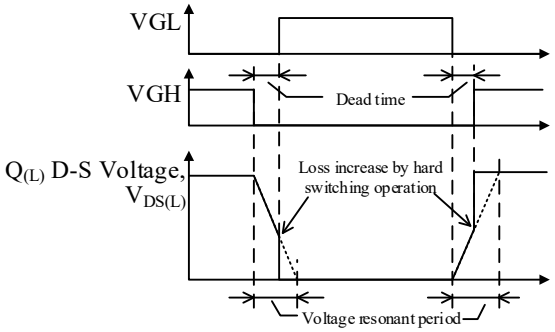

Figure 9-18. ZVS Failure Operation Waveform

9.7.1 When Using Automatic Dead Time Adjustment Function

When using the automatic dead time adjustment function, set the startup sequence as follows: Set the DTS pin voltage less than V_{DTS} = 1.9 V, and then apply $V_{CC(ON)}$ = 11.9 V or more to the VCC pin.

To set the DTS pin voltage less than 1.9 V connect a resistor between the DTS and GND pins. The resistance is about 100 kΩ with the effect of the DTS pin source current (I_{DTS} = −10.2 µA) taken into account.

This automatic dead time adjustment function operates so that the IC detects a voltage resonant period to automatically control the ZVS (Zero Voltage Switching) operation of $Q_{(H)}$ and $Q_{(L)}$. This function achieves the power supply application without a dead time adjustment for each power supply specification, if the voltage resonant period is varied according to the power supply specifications such as an input voltage and an output power. The VS pin detects the dv/dt periods on the rising and falling voltage waveforms between drain and source of the low-side power MOSFET (see Figure 9-19). The dead time is determined by the detected dv/dt period. As a result, the high-side and the low-side power MOSFETs are automatically controlled in the Zero Voltage Switching (ZVS) operation. This function operates in the period from $t_{d(MIN)}$ = 0.24 µs to $t_{d(MAX)}$ = 1.65 µs. Check that the Zero Current Switching (ZCS) operation period is about 600 ns (i.e., the period that the drain current flows through the body diode as shown in Figure 9-20) based on actual operation in the following conditions:

When an output power is minimum in a maximum input voltage specification.

When an output power is maximum in a minimum input voltage specification.

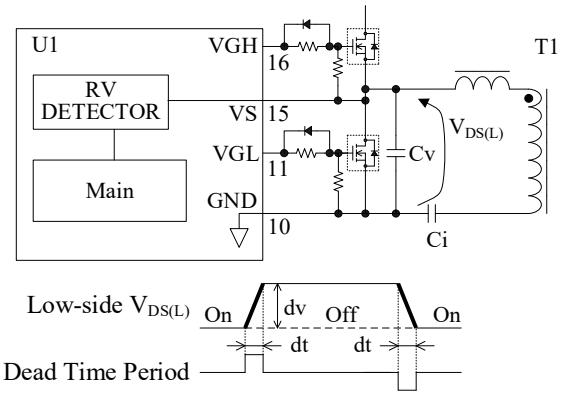

Figure 9-19. VS Pin and Dead Time Period

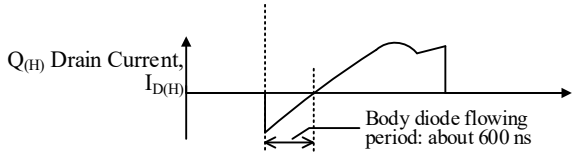

Figure 9-20. ZCS Check Point

9.7.2 When Using Fixed Minimum Dead Time Value

When using the fixed minimum dead time, set the startup sequence as follows: Apply V_{DTS} of 1.9 V or more to the DTS pin, and then add $V_{CC(ON)}$ = 11.9 V or more to the VCC pin.

Since the source current, I_{DTS} = −10.2 µA, flows through the DTS pin, the voltage is applied to DTS pin by the resistor connected between the DTS and GND pins. The resister should be set that the DTS pin voltage is 1.9 V or more.

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9.8 Capacitive Mode Detection Function

The resonant power supply should be operated in the inductance area shown in Figure 9-21. In the capacitance area, the power supply becomes the capacitive mode operation (see Section 9.1). To prevent the operation, the minimum oscillation frequency must be set higher than f_0 on each power supply specification. The IC has the capacitive mode operation detection function to keep the frequency always higher than f_0. Thus, the minimum oscillation frequency setting is unnecessary; and the power supply design is easier. In addition, the ability of transformer is improved because the operating frequency can be close to the resonant frequency, f_0.

The resonant current is detected by the RC pin to prevent the capacitive mode operation. When the capacitive mode is detected, C7 connected to the CL pin is charged by $I_{CL(SRC)1}$ = −17 μA. When the CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated to stop the switching operation in latched state. The detection voltage is changed V_{RC1} = ±0.10 V or V_{RC2} = ±0.30 V depending on the load (see Figure 9-23 and Figure 9-24).

The capacitive mode operation detection function operations as follows:

- **$Q_{(H)}$ On Period**
  Figure 9-22 shows the RC pin waveform in the inductance area. Figure 9-23 and Figure 9-24 show the RC pin waveform in the capacitance area.
  In the inductance area, the RC pin voltage does not cross $+V_{RCx}$ from higher to lower during the $Q_{(H)}$ on period (see Figure 9-22). On the contrary, in the capacitance area, the RC pin voltage crosses $+V_{RC1}$ from higher to lower. At this point, the capacitive mode operation is detected. Then, $Q_{(H)}$ is turned off; and $Q_{(L)}$ is turned on (see Figure 9-23 and Figure 9-24).

- **$Q_{(L)}$ On Period**
  Contrary to the case of $Q_{(H)}$, in the capacitance area, the RC pin voltage crosses $-V_{RCx}$ from lower to higher during the $Q_{(L)}$ on period. At this point, the capacitive mode operation is detected. Then, $Q_{(L)}$ is turned off; and $Q_{(H)}$ is turned on.

As above, to prevent the capacitive mode, the RC pin voltage is detected by pulse-by-pulse; and an operating frequency is synchronized with a capacitive mode operation frequency. C9, R7, and R8 should be set as follows:

The absolute value of the RC pin voltage is more than $|V_{RC2}|$ = 0.30 V; and

The RC pin voltage must be within the absolute maximum ratings of −6 to 6 V.

In addition, to set C9, R7, and R8, the settings described in Section 9.12 and the condition that the capacitive mode is easily caused (e.g., startup, turning off the mains input voltage, or output shorted) should be taken into account.

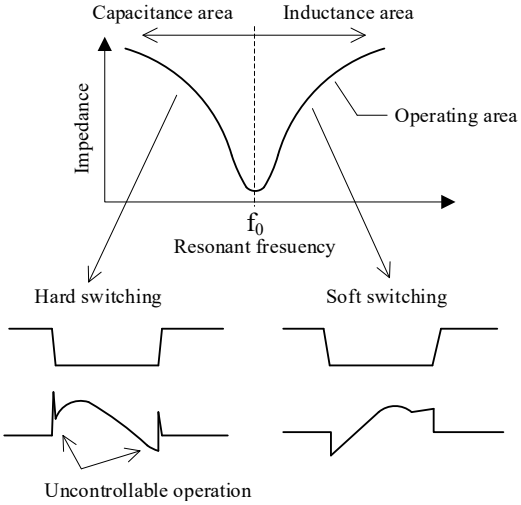

Figure 9-21. Operating Area of Resonant Power Supply

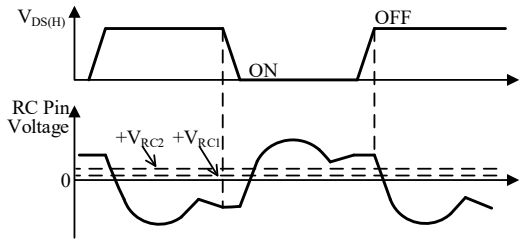

Figure 9-22. RC Pin Voltage in Inductance Area

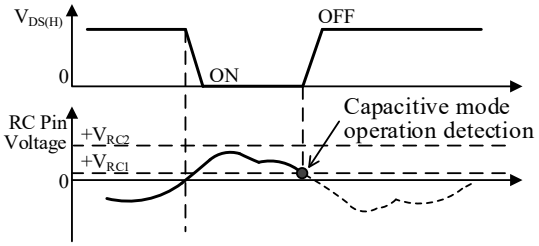

Figure 9-23. High-side Capacitive Mode Detection in Light Load

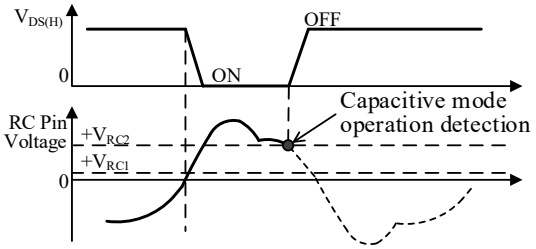

Figure 9-24. High-side Capacitive Mode Detection in Heavy Load

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9.9 Reset Detection Function

In the startup period, the feedback control for the output voltage is inactive. If a magnetizing current may not be reset in the on-period because of unbalanced operation, a negative current may flow just before a power MOSFET turns off. This causes a hard switching operation, increases the stresses of the power MOSFET. Where the magnetizing current means the circulating current applied for resonant operation, and flows only into the primary-side circuit. To prevent the hard switching, the IC has the reset detection function.

Figure 9-26 shows the high-side operation and the reference drain current waveforms in a normal resonant operation and a reset failure operation. To prevent the hard switching operation, the reset detection function operates such as an on period is extended until the absolute value of a RC pin voltage, $|V_{RC1}|$, increases to 0.10 V or more. When the on period reaches the maximum reset time, $t_{RST(MAX)}$ = 5 µs, the on-period expires at that moment, i.e., the power MOSFET turns off (see Figure 9-25).

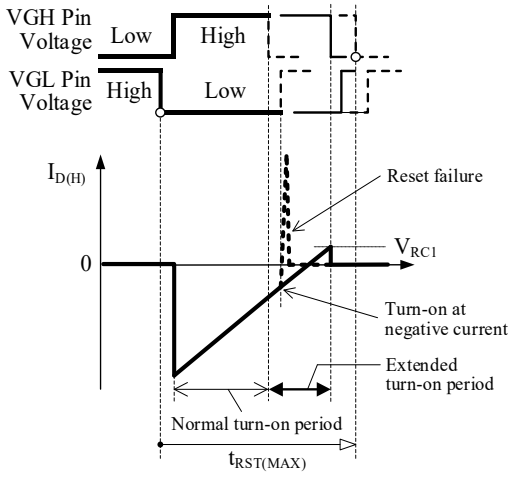

Figure 9-25. Reset Detection Operation Example at High-side On Period

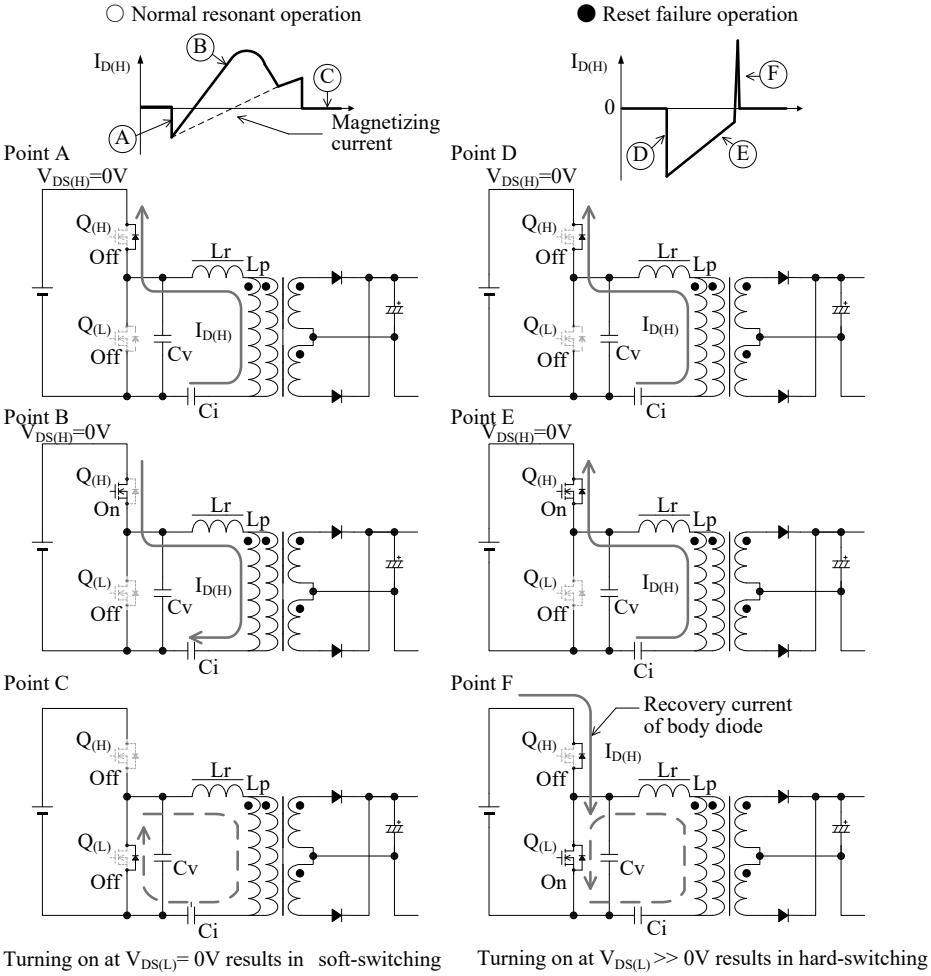

Figure 9-26. Reference High-side Operation and Drain Current Waveforms in Normal Resonant Operation and in Reset Failure Operation

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9.10 VCC Pin Overvoltage Protection (VCC_OVP)

When the voltage between the VCC and GND pins is applied to the VCC Pin OVP Threshold Voltage, $V_{CC(OVP)}$ = 32.0 V, or more, the VCC pin overvoltage protection (VCC_OVP) is activated; and the IC stops switching operation in a latched state. To release the latched state, decrease the VCC pin voltage to ≤$V_{CC(L.OFF)}$ of 10.0 V, or decrease the VSEN pin voltage to ≤$V_{SEN(OFF)}$ of 1.100 V, respectively.

The VCC pin input voltage must be set less than the its absolute maximum rating of 35 V.

9.11 Input Overvoltage Protection (HVP), Input Undervoltage Protection (UVP)

When the VSEN pin voltage reaches $V_{SEN(HVP)}$ of 5.6 V or more due to the increasing input voltage from a steady state, the input overvoltage protection (HVP) is activated; and the IC stops switching operation in a latched state. To release the latched state, decrease the VCC pin voltage to ≤$V_{CC(L.OFF)}$ of 10.0 V, or decrease the VSEN pin voltage to ≤$V_{SEN(OFF)}$ of 1.100 V, respectively.

On the other hand, when the VSEN pin voltage falls to $V_{SEN(OFF)}$ of 1.100 V or less due to the decreasing input voltage from a steady state, the input under voltage protection (UVP) is activated; and the IC stops the switching operation. Even if the IC is in the operating state (e.g., the VCC pin voltage is more than $V_{CC(OFF)}$), the UVP is prevailed, and is activated.

When the VSEN pin voltage increases to $V_{SEN(ON)}$ = 1.300 V or more depending on input voltage rising in the operating state, the IC restarts the switching operation. The DC input voltage at the HVP or the UVP activation is calculated as follows:

$$V_{IN(OP)} = V_{SEN(TH)} \times \left(1 + \frac{R1 + R2}{R3}\right). \quad (7)$$

Where $V_{IN(OP)}$ is the DC input voltage at the HVP or the UVP activation, and $V_{SEN(TH)}$ is the threshold voltage of the VSEN pin (see Table 9-1).

Table 9-1. VSEN Pin Threshold Voltage

Parameter	Symbol	$V_{SEN(TH)}$
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$	5.6 V
VSEN Pin UVP Threshold Voltage	$V_{SEN(OFF)}$	1.100 V
VSEN Pin UVP Release Threshold Voltage	$V_{SEN(ON)}$	1.300 V

R1 and R2 have a high resistance, and are applied high voltage. Thus, these should be taken into account as follows:

- Select a resistor designed against electromigration according to the specifications of the application.
- Use a combination of resistors in series for that to reduce each applied voltage.

R1 reference value is about 10 MΩ. C2 shown in Figure 9-27 is for reducing noises, and is set 1000 pF to 0.01 µF. The value of R1, R2, R3, and C2 should be selected based on actual operation in the application.

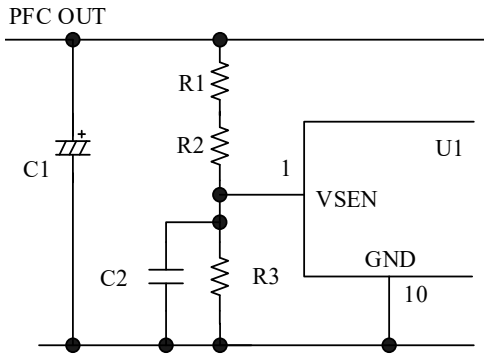

Figure 9-27. VSEN Pin Pherepheral Circuit

9.12 Overcurrent Protection (OCP)

For the overcurrent protection (OCP), the IC detects the drain current, I_D, on pulse-by-pulse basis, and limits output power. the OCP circuit achieves that C9 value can be smaller than Ci value. Where C9 is for shunt capacitor, and Ci is for current resonant capacitor (see Figure 9-28). This results in the reducing detection current through C9. Thus, the loss of the detection resistor, R8, is reduced; and the size of R8 can be smaller.

There is no convenient method that the accurate resonant current value is calculated using the parameter such as condition of a mains input or an output. Thus, C9, R7, and R8 should be adjusted based on actual operation in the application. The reference values for C8, C9, R7, and R8 and theirs adjustment methods are as follows:

- R8 and C9
  C9: 100pF to 330pF (around 1 % of Ci value).
  R8: Around 100 Ω.
  Given the current of the high side power MOSFET at ON state as $I_{D(H)}$. R8 is calculated Equation (8). The detection voltage of R8 is used for the detection of the capacitive mode operation (see Section 9.8) and overload detection (see Section 9.13). Therefore, overcurrent detection, capacitive mode operation, and overload detection should be taken into account in adjusting R8 and C9.

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$$R8 \approx \frac{|V_{RC(L)}|}{I_{D(H)}} \times \left(\frac{C9 + Ci}{C9}\right) \quad (8)$$

Where $I_{D(H)}$ is the current of the high-side power MOSFET at an on state, and $V_{RC(L)}$ is the RC Pin Threshold Voltage (Low) of ±1.90 V

- R7 and C8
  They are for high frequency noise reduction.
  R7: 100 Ω to 470 Ω
  C8: 100 pF to 1000 pF

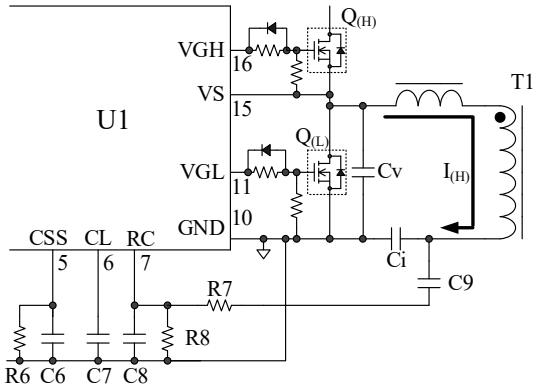

Figure 9-28. RC Pin Peripheral Circuit

The OCP operation has two level threshold voltages as follows:

9.12.1 Overcurrent Protection 1 (OCP1)

This is a first OCP level. When the absolute value of the RC pin voltage increases to more than $|V_{OC(L)}|$ of 1.90 V, C6 connected to the CSS pin is discharged by $I_{CSS(L)}$ = 1.8 mA. Thus, the switching frequency increases to prevent the output power rising. When the absolute value of the RC pin voltage decreases to $|V_{RC(L)}|$ or less during the C6 discharge, the C6 discharge is stopped.

9.12.2 Overcurrent Protection 2 (OCP2)

This is a second OCP level. When the absolute value of the RC pin voltage increases to more than $|V_{RC(H)}|$ = 2.80 V, the high speed OCP is activated. Then, the on/off statuses of power MOSFETs are inverted. At the same time, C6 is discharged by $I_{CSS(H)}$ = 20.5 mA. Thus, the switching frequency quickly increases to quickly prevent the output power rising. The OCP2 protects the IC from the exceeding overcurrent caused by the abnormal condition such as the output shorted.

When the absolute value of the RC pin voltage decreases to $|V_{RC(H)}|$ or less, the OCP level is transferred to OCP1 operation.

9.13 Overload Protection (OLP)

Figure 9-29 shows the overload protection (OLP) waveforms.

When the current flowing through the power MOSFET increases along with a rise in the output load, causing the absolute value of the RC pin voltage to exceed $|V_{RC(L)}|$ = 1.90 V, the IC enters an overload detection state.

In an overload detection state, the C7 connected to the CL pin is charged with $I_{CL(SRC)1}$ = −17 µA. When the absolute value of the RC pin voltage exceeds $|V_{RC(H)}|$ = 2.80 V, C7 is charged with the source current, $I_{CL(SRC)2}$ = −135 µA.

When the overload detection state continues and the CL pin voltage increases to $V_{CL(OLP)}$ = 4.2 V, the OLP is activated. When the OLP is activated, the switching operation stops in a latched state. To release the latched state, decrease the VCC pin voltage to ≤$V_{CC(L.OFF)}$ of 10.0 V, or decrease the VSEN pin voltage to ≤$V_{SEN(OFF)}$ of 1.100 V, respectively.

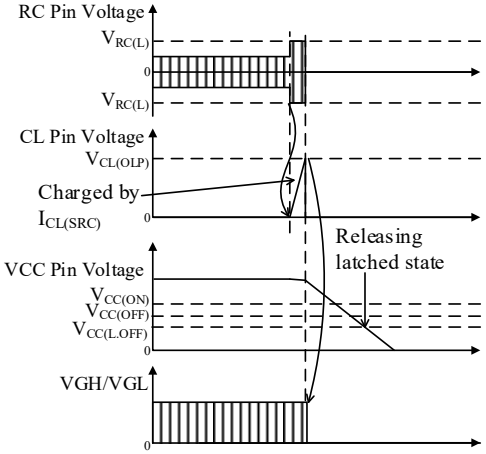

Figure 9-29. OLP Waveform

9.14 Optocoupler Open Protection (OOP)

In case the primary side of an optocoupler becomes open, a feedback current reduction due to the FB pin voltage rising result in the output voltage increases. To prevent the status the IC has the optocoupler open protection (OOP). The OOP is activated at following condition.

- When the FB pin voltage increases to higher than the CSS pin voltage, or
- When the FB pin voltage increases to the FB Pin Open Detection Threshold Voltage, $V_{FB(OOP)}$ = 4.6 V, or more.

After the OOP activation, C10 connected to the CD

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pin is charged by the CD Pin Source Current, $I_{CD(SRC)}$ = –20 µA. When the CD pin voltage increases to the CD Pin Threshold Voltage, V_{CD} = 3.0 V, the IC stops switching operation in a latched state. To release the latched state, decrease the VCC pin voltage to ≤$V_{CC(L.OFF)}$ of 10.0 V, or decrease the VSEN pin voltage to ≤$V_{SEN(OFF)}$ of 1.100 V, respectively.

The delay time is period until the switching operation stop from the OOP activation. The maximum delay time, t_{DLY_MAX}, is calculated by following equation.

$$t_{DLY_MAX} = \frac{V_{CD} \times C_{CD}}{|I_{CD(SRC)}|}, \quad (9)$$

where:
V_{CD} is the CD Pin Threshold Voltage of 3.0 V,
C_{CD} is the value of C10 connected to the CD pin (about 0.1 µF to 2.2 µF), and
$I_{CD(SRC)}$ is the CD Pin Source Current of –20 µA.

If C10 = 0.1 µF,

$$t_{DLY_MAX} = \frac{3.0\ V \times 0.1 \mu F}{|-20\ \mu A|} = 15\ ms\,.$$

During startup operation (see Section 9.3), the CD pin voltage increases because C10 is charged. C10 must be set the value with enough margins. To prevent a startup failure, C10 must be set enough large value so that the CD pin voltage is less than 3.0 V during startup period. In addition, the condition when the soft start period is longest (e.g., minimum input voltage and maximum output power) should be taken into account.

9.15 Thermal Shutdown (TSD)

When the junction temperature of the IC reach to the Thermal Shutdown Temperature $T_{J(TSD)}$ = 140 °C (min.), the thermal shutdown (TSD) is activated; and the IC stops switching operation in a latched state.

To release the latched state, decrease the VCC pin voltage to ≤$V_{CC(L.OFF)}$ of 10.0 V, or decrease the VSEN pin voltage to ≤$V_{SEN(OFF)}$ of 1.100 V, respectively.

10. Design Notes

10.1 External Components

Take care to use the proper rating and proper type of components.

10.1.1 Input and Output Electrolytic Capacitors

Apply proper derating to a ripple current, a voltage, and a temperature rise. It is required to use the high ripple current and low impedance type electrolytic capacitor that is designed for switch mode power supplies.

10.1.2 Resonant Transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce the effect of the eddy current and the skin effect, the wire of transformer should be used a bundle of fine litz wires.

10.1.3 Current Detection Resistor, R_{OCP}

To reduce the effect of the high frequency switching current flowing through R_{OCP}, choose the resister of a low internal inductance type. In addition, its allowable dissipation should be chosen suitable.

10.1.4 Current Resonant Capacitor, Ci

Since a large resonant current flows through Ci, Ci should be used a low loss and a high current capability capacitor such as a polypropylene film capacitor. In addition, Ci must be taken into account its frequency characteristic because a high frequency current flows.

10.1.5 Gate Pin Peripheral Circuit

The VGH and VGL pins are gate drive outputs for external power MOSFETs. These peak source and sink currents are –540 mA and 1.50 A, respectively.

To make a turn-off speed faster, connect the diode, D_S, as shown in Figure 10-1. When R_A and D_S is adjusted, the following contents should be taken into account: the power losses of power MOSFETs, gate waveforms (for a ringing reduction caused by a pattern layout, etc.), and EMI noises. To prevent the malfunctions caused by steep dv/dt at turn-off of power MOSFETs, connect R_{GS} of 10 kΩ to 100 kΩ between the Gate and Source pins of the power MOSFET with a minimal length of PCB traces. When these gate resistances are adjusted, the gate

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waveforms should be checked that the dead time is ensured as shown in Figure 10-2.

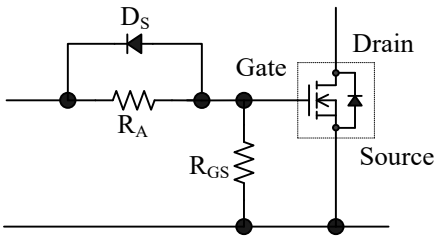

Figure 10-1. Power MOSFET Peripheral Circuit

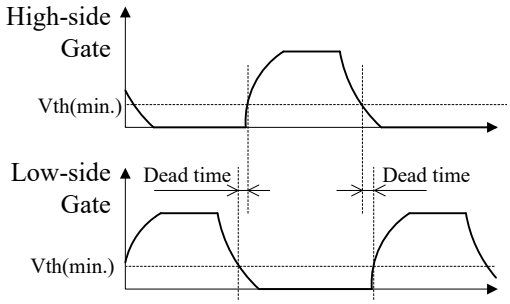

Figure 10-2. Dead Time Confirmation

10.2 PCB Trace Layout and Component Placement

The PCB circuit design and the component layout significantly affect a power supply operation, EMI noises, and power dissipation. Thus, to reduce the impedance of the high frequency traces on a PCB (see Figure 10-3), they should be designed as wide trace and small loop as possible. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

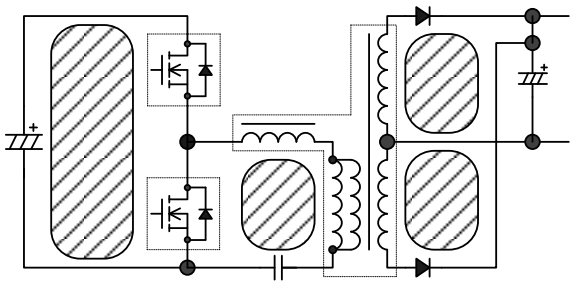

Figure 10-3. High Frequency Current Loops (Hatched Areas)

Figure 10-4 shows the circuit design example. The PCB trace design should be also taken into account as follows:

1) Main Circuit Trace
The main traces that switching current flows should be designed as wide trace and small loop as possible.

2) Control Ground Trace
If the large current flows through a control ground, it may cause varying electric potential of the control ground; and this may result in the malfunctions of the IC. Therefore, connect the control ground as close and short as possible to the GND pin at a single-point ground (or star ground) that is separated from the power ground.

3) VCC Trace
The trace for supplying power to the IC should be as small loop as possible. If C3 and the IC are distant from each other, a film capacitor C_f (about 0.1 µF to 1.0 µF) should be connected between the VCC and GND pins with a minimal length of PCB traces.

4) Trace of Peripheral Components for the IC Control
These components should be placed close to the IC, and be connected to the corresponding pin of the IC with as short trace as possible.

5) Trace of Bootstrap Circuit Components
These components should be connected to the IC pin with as short trace as possible. In addition, the loop for these should be as small as possible.

6) Secondary Side Rectifier Smoothing Circuit Trace
The traces of the rectifier smoothing loops carry the switching current. Thus it should be designed as wide trace and small loop as possible.

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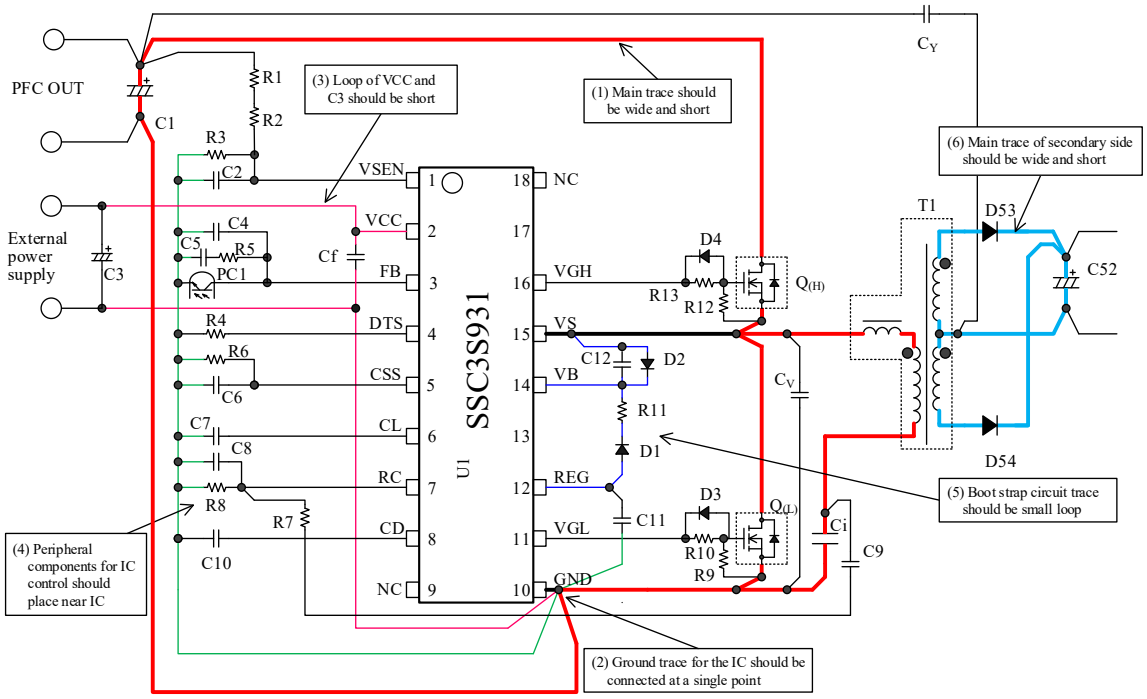

Figure 10-4. Peripheral Circuit Trace Example around the IC

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11. Pattern Layout Example

The following shows the PCB pattern layout example and the schematic of circuit using the SSC3S931. The circuit symbols correspond to these of Figure 11-1.

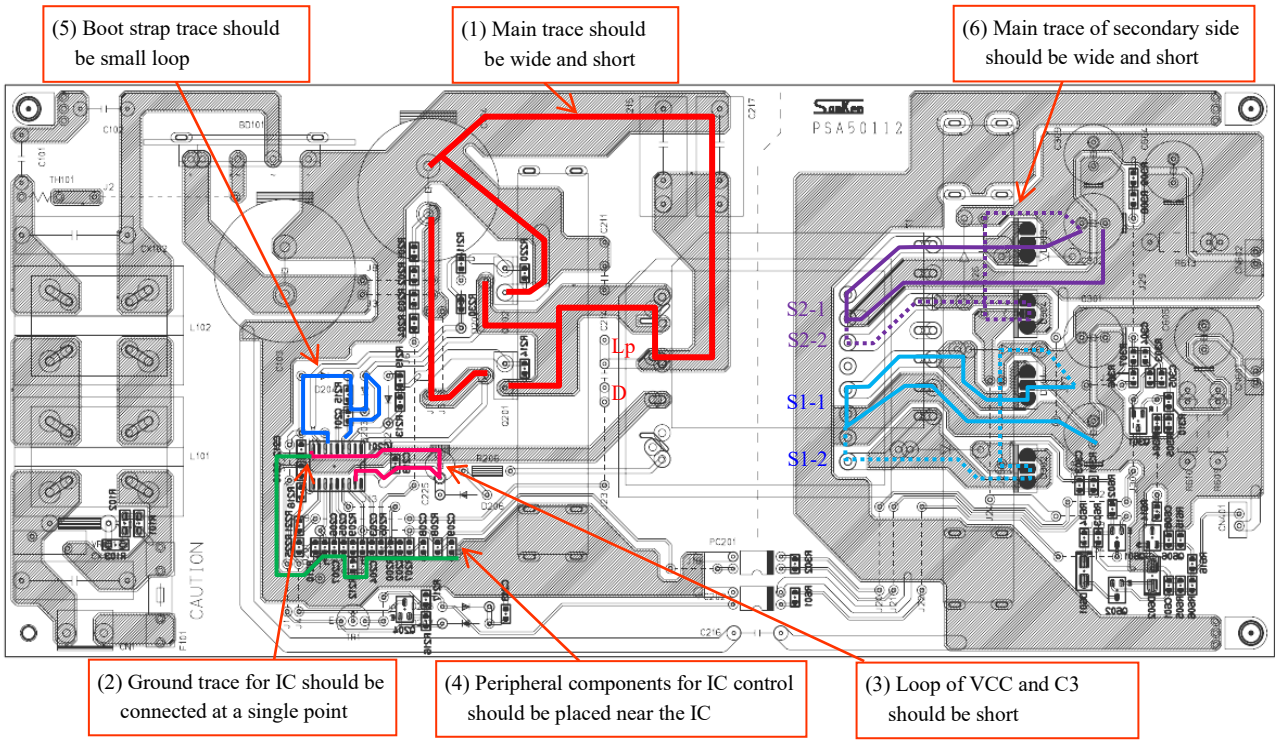

Figure 11-1. PCB circuit trace layout example

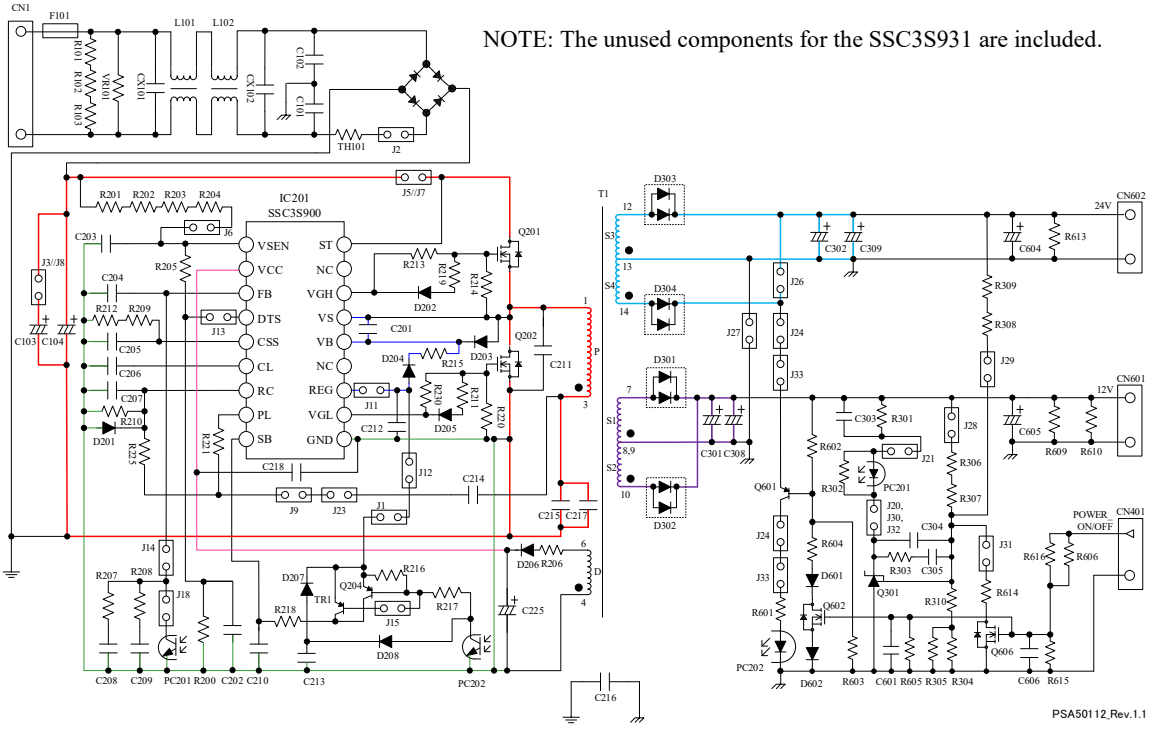

Figure 11-2. Circuit schematic for PCB circuit trace layout

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