LLC Current-Resonant Off-Line Switching Controller

SSC3S921

Data Sheet

Description

The SSC3S921 is a controller with SMZ* method for LLC current resonant switching power supplies, incorporating a floating drive circuit for a high-side power MOSFET. The IC includes useful functions such as Standby Function, Automatic Dead Time Adjustment, and Capacitive Mode Detection.

The IC achieves high efficiency, low noise and high cost-performance power supply systems with few external components.

*SMZ: Soft-switched Multi-resonant Zero Current switch, achieved soft switching operation during all switching periods.

Package

SOP18



Not to scale

Features

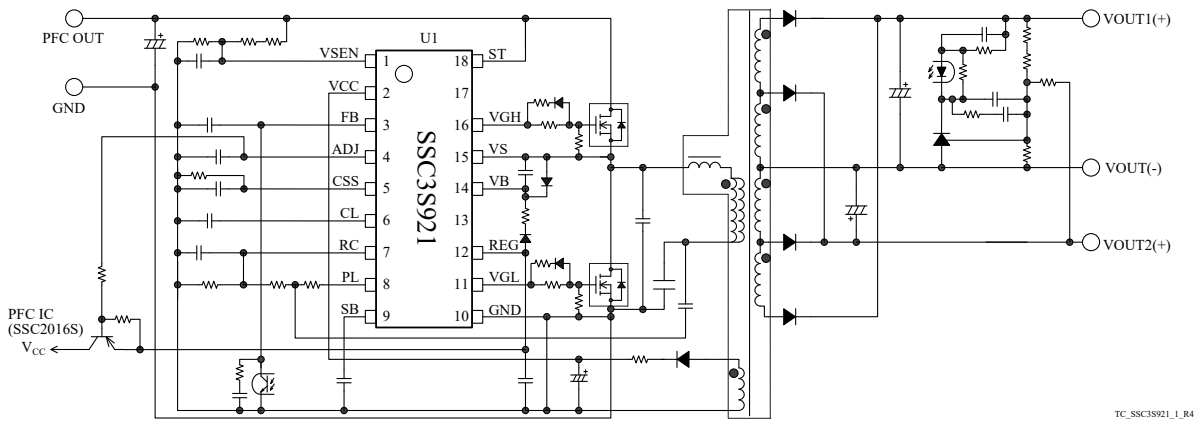
- Standby Mode Change Function
  - Output Power at Light Load: P_O = 125 mW (P_{IN} = 0.27 W, as a reference with discharge resistor of 1 MΩ for across the line capacitor)
  - Burst operation in standby mode
  - Soft-on/Soft-off function: reduces audible noise
- PFC IC ON/OFF Function: In standby operation, the IC turns off PFC IC.
- Soft-start Function
- Capacitive Mode Detection Function
- Reset Detection Function
- Automatic Dead Time Adjustment Function
- Input Electrolytic Capacitor Discharge Function
- Protections
  - Brown-In and Brown-Out Function:
  - High-side Driver UVLO: Auto-restart: Auto-restart
  - Overcurrent Protection (OCP): Auto-restart, peak drain current detection, 2-step detection
  - Overload Protection (OLP): Auto-restart
  - Overvoltage Protection (OVP): Auto-restart
  - REG Overvoltage Protection (REG_OVP): Latched shutdown
  - Thermal Shutdown (TSD): Auto-restart

Applications

Switching power supplies for electronic devices such as:

- Digital appliances: LCD television and so forth
- Office automation (OA) equipment: server, multi-function printer, and so forth
- Industrial apparatus
- Communication facilities

Typical Application



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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25°C.

Parameter	Symbol	Pins	Rating	Unit
VSEN Pin Sink Current	I_{SEN}	1 − 10	1.0	mA
Control Part Input Voltage	V_{CC}	2 − 10	−0.3 to 35	V
FB Pin Voltage	V_{FB}	3 − 10	−0.3 to 6	V
ADJ Pin Voltage	V_{ADJ}	4 − 10	−0.3 to V_{REG}	V
CSS Pin Voltage	V_{CSS}	5 − 10	−0.3 to 6	V
CL Pin Voltage	V_{CL}	6 − 10	−0.3 to 6	V
RC Pin Voltage	V_{RC}	7 − 10	−6 to 6	V
PL Pin Voltage	V_{PL}	8 − 10	−0.3 to 6	V
SB Pin Sink Current	I_{SB}	9 − 10	100	μA
VGL pin Voltage	V_{GL}	11 – 10	−0.3 to V_{REG} + 0.3	V
REG pin Source Current	I_{REG}	12 – 10	−10.0	mA
Voltage Between VB Pin and VS Pin	V_B–V_S	14 − 15	−0.3 to 20.0	V
VS Pin Voltage	V_S	15 − 10	−1 to 600	V
VGH Pin Voltage	V_{GH}	16 − 10	V_S − 0.3 to V_B + 0.3	V
ST Pin Voltage	V_{ST}	18 − 10	−0.3 to 600	V
Operating Ambient Temperature	T_{OP}	—	−40 to 85	°C
Storage Temperature	T_{STG}	—	−40 to 125	°C
Junction Temperature	T_J	—	150	°C

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2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25°C, V_{CC} is 19 V.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Start Circuit and Circuit Current							
Operation Start Voltage	$V_{CC(ON)}$		2 − 10	15.8	17.0	18.2	V
Operation Stop Voltage*	$V_{CC(OFF)}$		2 − 10	7.8	8.9	9.8	V
Startup Current Biasing Threshold Voltage*	$V_{CC(BIAS)}$		2 − 10	9.0	9.8	10.6	V
Circuit Current in Operation	$I_{CC(ON)}$		2 − 10	—	—	10.0	mA
Circuit Current in Non-operation	$I_{CC(OFF)}$	V_{CC} = 11 V	2 − 10	—	0.7	1.5	mA
Startup Current	I_{ST}		18 − 10	3.0	6.0	9.0	mA
Protection Operation Release Threshold Voltage*	$V_{CC(P.OFF)}$		2 − 10	7.8	8.9	9.8	V
REG Pin Overvoltage Protection Release Threshold Voltage	$V_{CC(L.OFF)}$		2 − 10	2.0	5.0	8.0	V
Circuit Current in Protection	$I_{CC(P)}$	V_{CC} = 10 V	2 − 10	—	0.7	1.5	mA
Oscillator							
Minimum Frequency	$f_{(MIN)}$		11 – 10 16 – 15	27.5	31.5	35.5	kHz
Maximum Frequency	$f_{(MAX)}$		11 – 10 16 – 15	230	300	380	kHz
Minimum Dead-Time	$t_{d(MIN)}$		11 – 10 16 – 15	0.04	0.24	0.44	µs
Maximum Dead-Time	$t_{d(MAX)}$		11 – 10 16 – 15	1.20	1.65	2.20	µs
Externally Adjusted Minimum Frequency 1	$f_{(MIN)ADJ1}$	R_{CSS} = 30 kΩ	11 – 10 16 – 15	69	73	77	kHz
Externally Adjusted Minimum Frequency 2	$f_{(MIN)ADJ2}$	R_{CSS} = 77 kΩ	11 – 10 16 – 15	42.4	45.4	48.4	kHz
Feedback Control							
FB Pin Oscillation Start Threshold Voltage	$V_{FB(ON)}$		3 – 10	0.15	0.30	0.45	V
FB Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		3 – 10	0.05	0.20	0.35	V
FB Pin Maximum Source Current	$I_{FB(MAX)}$	V_{FB} = 0 V	3 – 10	−300	−195	−100	µA
FB Pin Reset Current	$I_{FB(R)}$		3 – 10	2.5	5.0	7.5	mA
Soft-start							
CSS Pin Charging Current	$I_{CSS(C)}$		5 – 10	−120	−105	−90	µA
CSS Pin Reset Current	$I_{CSS(R)}$	V_{CC} = 11V	5 – 10	1.1	1.8	2.5	mA
Maximum Frequency in Soft-start	$f_{(MAX)SS}$		11 – 10 16 – 15	400	500	600	kHz
Standby							
SB Pin Standby Threshold Voltage	$V_{SB(STB)}$		9 – 10	4.5	5.0	5.5	V
SB Pin Oscillation Start Threshold Voltage	$V_{SB(ON)}$		9 – 10	0.5	0.6	0.7	V

* $V_{CC(OFF)} = V_{CC(P.OFF)} < V_{CC(BIAS)}$ always.

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Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
SB Pin Oscillation Stop Threshold Voltage	$V_{SB(OFF)}$		9 – 10	0.4	0.5	0.6	V
SB Pin Clamp Voltage	$V_{SB(CLAMP)}$		9 – 10	7	8.5	10	V
SB Pin Source Current	$I_{SB(SRC)}$		9 – 10	−17	−10	−3	µA
SB Pin Sink Current	$I_{SB(SNK)}$		9 – 10	3	10	17	µA
CSS Pin Standby Release Threshold Voltage	$V_{CSS(STB)}$		5 – 10	1.35	1.50	1.65	V
PFC ON/OF Function							
ADJ Pin Voltage in Normal Operation	$V_{ADJ(L)}$	I_{ADJ} = 100 µA	4 – 10	0	1	2	V
ADJ Pin Voltage in Standby Operation	$V_{ADJ(H)}$	I_{ADJ} = −100 µA	4 – 10	8.5	9.9	10.8	V
Overload Protection (OLP)							
CL pin OLP Threshold Voltage	$V_{CL(OLP)}$		6 – 10	3.9	4.2	4.5	V
CL Pin Source Current	$I_{CL(SRC)}$		6 – 10	−29	−17	−5	µA
Brown-In and Brown-Out							
VSEN Pin Threshold Voltage (On)	$V_{SEN(ON)}$		1 – 10	1.248	1.300	1.352	V
VSEN Pin Threshold Voltage (Off)	$V_{SEN(OFF)}$		1 – 10	1.056	1.100	1.144	V
VSEN Pin Clamp Voltage	$V_{SEN\ (CLAMP)}$		1 – 10	10.0	—	—	V
Reset Detection							
Maximum Reset Time	$t_{RST(MAX)}$		11 – 10 16 – 15	4	5	6	µs
Driver Circuit Power Supply							
VREG Pin Output Voltage	V_{REG}		12 – 10	9.6	10.0	10.8	V
High-side Driver							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		14 – 15	5.7	6.8	7.9	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		14 – 15	5.5	6.4	7.3	V
Driver Circuit							
VGL,VGH Pin Source Current 1	$I_{GL(SRC)1}$ $I_{GH(SRC)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 0V V_{GH} = 0V	11 – 10 16 – 15	—	–540	—	mA
VGL,VGH Pin Sink Current 1	$I_{GL(SNK)1}$ $I_{GH(SNK)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 10.5V V_{GH} = 10.5V	11 – 10 16 – 15	—	1.50	—	A
VGL,VGH Pin Source Current 2	$I_{GL(SRC)2}$ $I_{GH(SRC)2}$	V_{REG} = 11.5V V_B = 11.5V V_{GL} = 10V V_{GH} = 10V	11 – 10 16 – 15	−140	−90	−40	mA
VGL,VGH Pin Sink Current 2	$I_{GL(SNK)2}$ $I_{GH(SNK)2}$	V_{REG} = 12V V_B = 12V V_{GL} = 1.5V V_{GH} = 1.5V	11 – 10 16 – 15	140	230	360	mA

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Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Current Resonant and Overcurrent Protection (OCP)							
Capacitive Mode Detection Voltage 1	V_{RC1}		7 – 10	0.02	0.10	0.18	V
				−0.18	−0.10	−0.02	V
Capacitive Mode Detection Voltage 2	V_{RC2}		7 – 10	0.4	0.50	0.6	V
				−0.6	−0.50	−0.4	V
RC Pin Threshold Voltage (Low)	$V_{RC(L)}$		7 – 10	1.42	1.50	1.58	V
				−1.58	−1.50	−1.42	V
RC Pin Threshold Voltage (High speed)	$V_{RC(S)}$		7 – 10	2.15	2.30	2.45	V
				−2.45	−2.30	−2.15	V
CSS Pin Sink Current (Low)	$I_{CSS(L)}$		5 – 10	1.1	1.8	2.5	mA
CSS Pin Sink Current (High speed)	$I_{CSS(S)}$		5 – 10	13.0	20.5	28.0	mA
Overvoltage Protection (OVP)							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 10	30.0	32.0	34.0	V
REG Pin OVP Threshold Voltage	$V_{CC(REG)}$		12 – 10	11.5	12.4	13.5	V
Thermal Shutdown (TSD)							
Thermal Shutdown Temperature	$T_{J(TSD)}$		—	140	—	—	°C
Thermal Resistance							
Junction to Ambient Thermal Resistance	θ_{J-A}		—	—	—	95	°C/W

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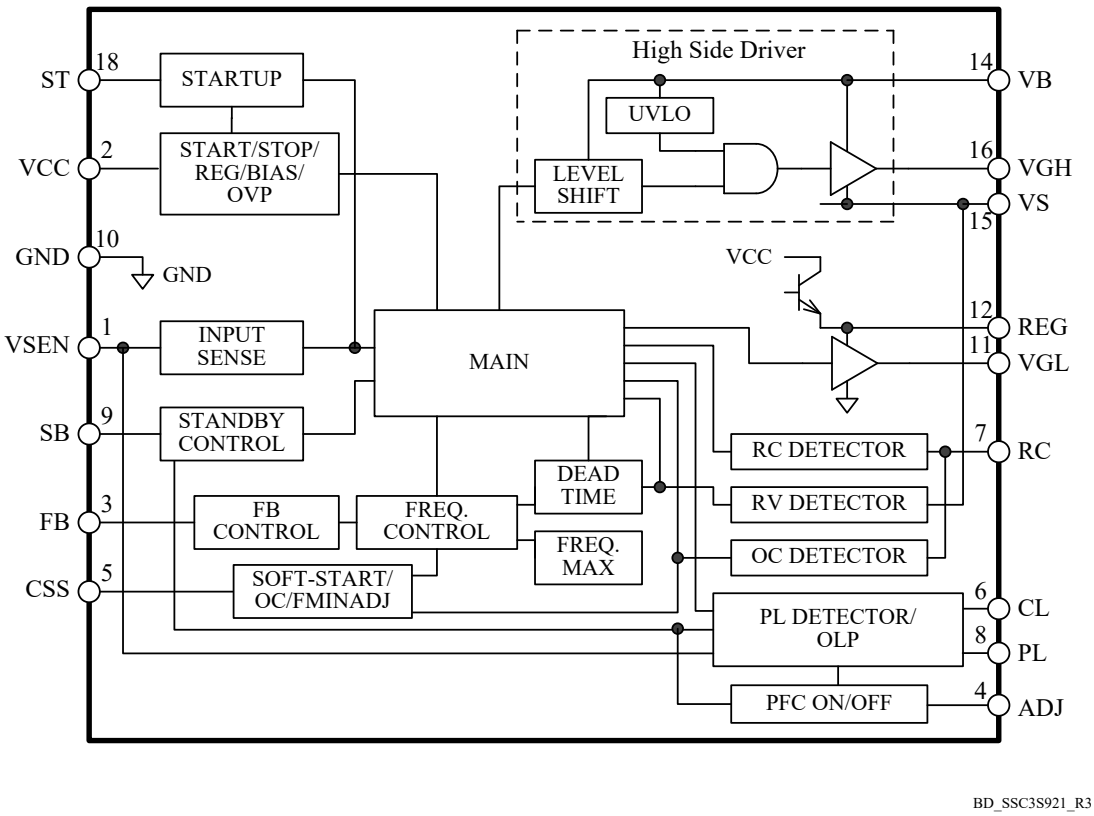
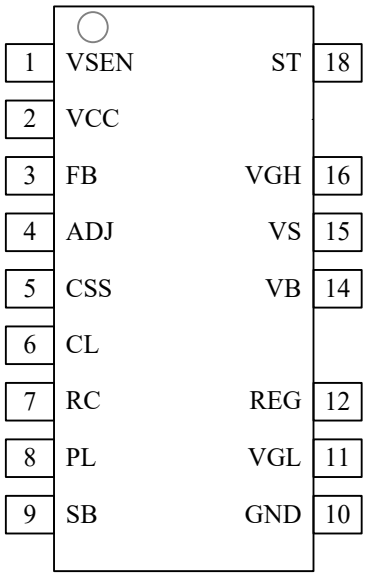
3. Block Diagram



4. Pin Configuration Definitions



Number	Name	Functions
1	VSEN	The mains input voltage detection signal input
2	VCC	Supply voltage input for the IC, and Overvoltage Protection (OVP) signal input
3	FB	Feedback signal input for constant voltage control
4	ADJ	PFC ON/OFF signal output
5	CSS	Soft-start capacitor connection
6	CL	Load current detection capacitor connection
7	RC	Resonant current detection signal input, and Overcurrent Protection (OCP) signal input
8	PL	Resonant current detection signal input for OLP
9	SB	Standby mode change signal input
10	GND	Ground
11	VGL	Low-side gate drive output
12	REG	Supply voltage output for gate drive circuit
13	–	(Pin removed)
14	VB	Supply voltage input for high-side driver
15	VS	Floating ground for high-side driver
16	VGH	High-side gate drive output
17	(NC)	—
18	ST	Startup current input

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5. Typical Application

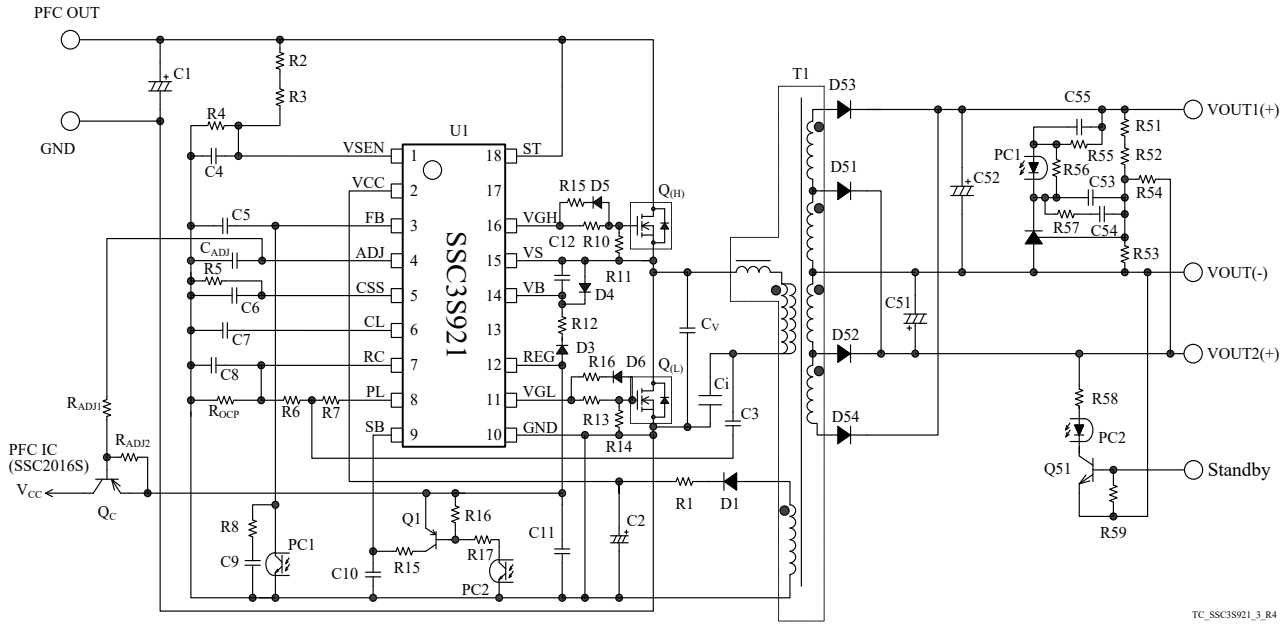

Figure 5-1 Typical application

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6. External Dimensions

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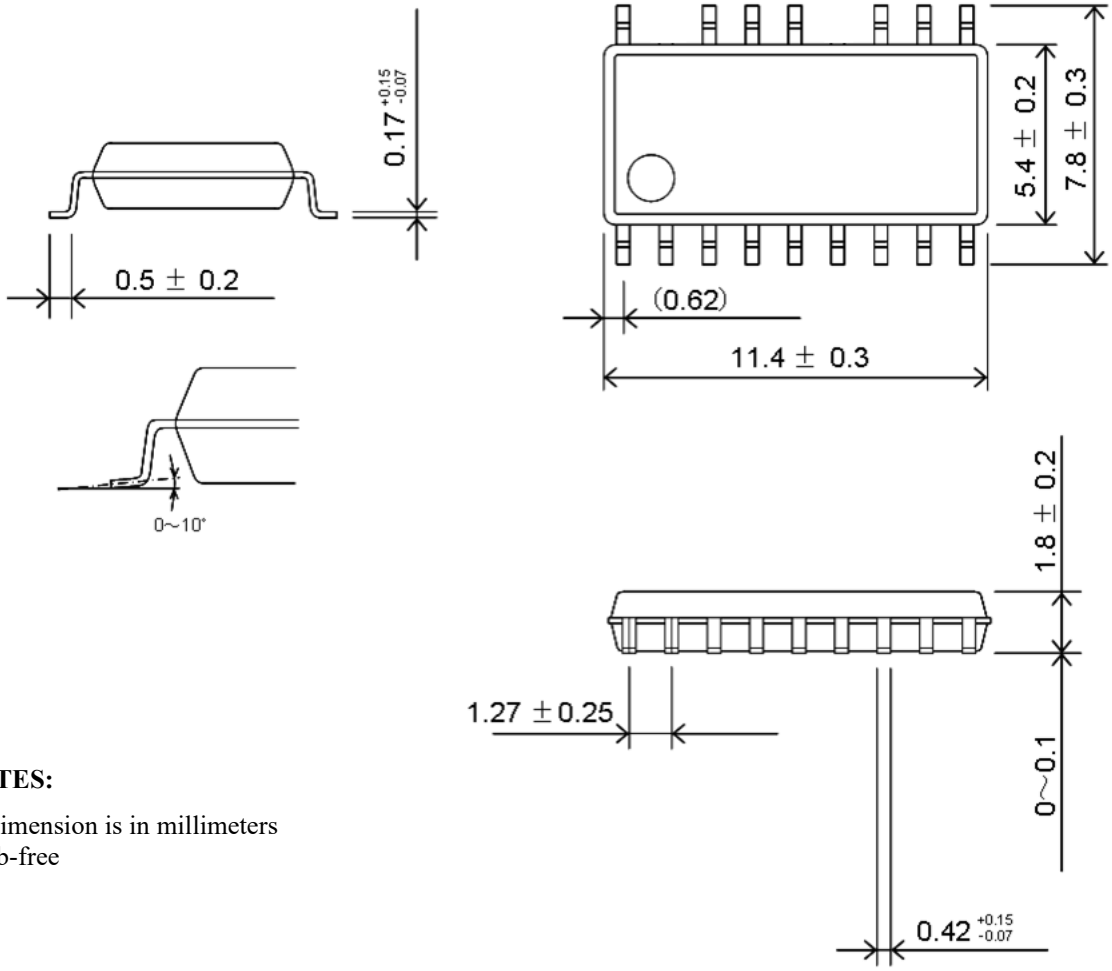
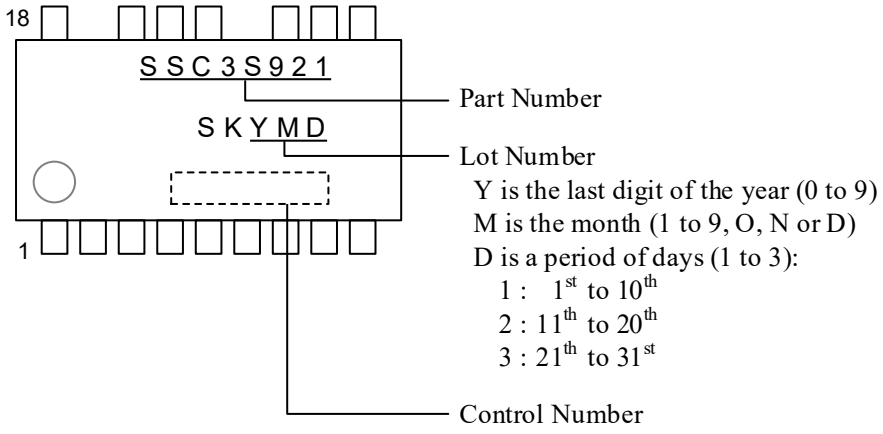


NOTES:

- Dimension is in millimeters
- Pb-free

7. Marking Diagram



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8. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−). $Q_{(H)}$ and $Q_{(L)}$ indicate a high-side power MOSFET and a low-side power MOSFET respectively. Ci and C_V indicate a current resonant capacitor and a voltage resonant capacitor, respectively.

8.1 Resonant Circuit Operation

Figure 8-1 shows a basic RLC series resonant circuit.

The impedance of the circuit, Ż, is as the following Equation.

$$\dot{Z} = R + j\left(\omega L - \frac{1}{\omega C}\right), \quad (1)$$

where ω is angular frequency; and ω = 2πf.

Thus,

$$\dot{Z} = R + j\left(2\pi fL - \frac{1}{2\pi fC}\right). \quad (2)$$

When the frequency, f, changes, the impedance of resonant circuit will change as shown in Figure 8-2.

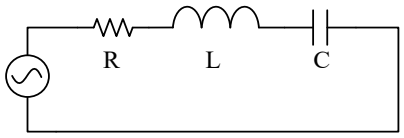

Figure 8-1. RLC Series Resonant Circuit

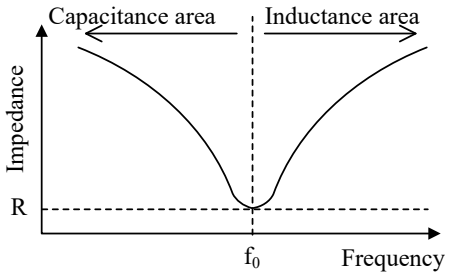

Figure 8-2. Impedance of Resonant Circuit

When 2πfL = 1/2πfC, Ż of Equation (2) becomes the minimum value, R (see Figure 8-2). In the case, ω is calculated by Equation (3).

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \quad (3)$$

The frequency in which Ż becomes minimum value is called a resonant frequency, f_0. The higher frequency area than f_0 is an inductance area. The lower frequency area than f_0 is a capacitance area.

From Equation (3), f_0 is as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (4)$$

Figure 8-3 shows the circuit of a current resonant power supply. The basic configuration of the current resonant power supply is a half-bridge converter. The switching devices, $Q_{(H)}$ and $Q_{(L)}$, are connected in series with V_{IN}. The series resonant circuit and the voltage resonant capacitor, C_V, are connected in parallel with $Q_{(L)}$. The series resonant circuit is consisted of the following components: the resonant inductor, L_R; the primary winding, P, of a transformer, T1; and the current resonant capacitor, C_i. The coupling between the primary and secondary windings of T1 is designed to be poor so that the leakage inductance increases. This leakage inductance is used for L_R. This results in a down sized of the series resonant circuit. The dotted mark with T1 describes the winding polarity, the secondary windings, S1 and S2, are connected so that the polarities are set to the same position as shown in Figure 8-3. In addition, the winding numbers of each other should be equal. From Equation (1), the impedance of a current resonant power supply is calculated by Equation (5). From Equation (4), the resonant frequency, f_0, is calculated by Equation (6).

$$\dot{Z} = R + j\left\{\omega(L_R + L_P) - \frac{1}{\omega Ci}\right\}, \quad (5)$$

$$f_0 = \frac{1}{2\pi\sqrt{(L_R + L_P) \times Ci}}, \quad (6)$$

where:
R is the equivalent resistance of load,
L_R is the inductance of the resonant inductor,
L_P is the inductance of the primary winding P, and
Ci is the capacitance of current resonant capacitor.

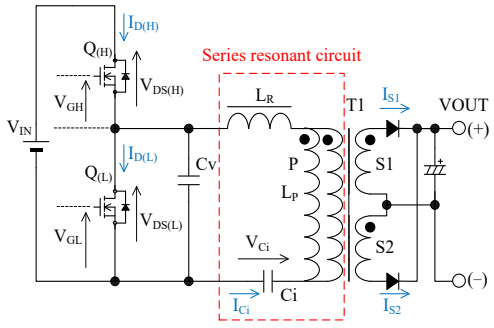

Figure 8-3. Current Resonant Power Supply Circuit

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In the current resonant power supply, $Q_{(H)}$ and $Q_{(L)}$ are alternatively turned on and off. The on and off times of them are equal. There is a dead time between the on periods of $Q_{(H)}$ and $Q_{(L)}$. During the dead time, $Q_{(H)}$ and $Q_{(L)}$ are in off status.

In the current resonant power supply, the frequency is controlled. When the output voltage decreases, the IC decreases the switching frequency so that the output power is increased to keep a constant output voltage. This must be controlled in the inductance area ($f_{SW} < f_0$). Since the winding current is delayed from the winding voltage in the inductance area, the turn-on operates in a ZCS (Zero Current Switching); and the turn-off operates in a ZVS (Zero Voltage Switching). Thus, the switching losses of $Q_{(H)}$ and $Q_{(L)}$ are nearly zero. In the capacitance area ($f_{SW} < f_0$), the current resonant power supply operates as follows: When the output voltage decreases, the switching frequency is decreased; and then, the output power is more decreased. Therefore, the output voltage cannot be kept constant. Since the winding current goes ahead of the winding voltage in the capacitance area, $Q_{(H)}$ and $Q_{(L)}$ operate in the hard switching. This results in the increases of a power loss. This operation in the capacitance area is called the capacitive mode operation. The current resonant power supply must be operated without the capacitive mode operation (for more details, see Section 8.12).

Figure 8-4 describes the basic operation waveform of current resonant power supply (see Figure 8-3 about the symbol in Figure 8-4). For the description of current resonant waveforms in normal operation, the operation is separated into a period A to F. In the following description:

$I_{D(H)}$ is the current of $Q_{(H)}$,
$I_{D(L)}$ is the current of $Q_{(L)}$,
$V_{F(H)}$ is the forwerd voltage of $Q_{(H)}$,
$V_{F(L)}$ is the forwerd voltage of $Q_{(L)}$,
I_L is the current of L_R,
V_{IN} is an input voltage,
V_{Ci} is Ci voltage, and
V_{CV} is C_V voltage.

The current resonant power supply operations in period A to F are as follows:

1) Period A
When $Q_{(H)}$ is on, an energy is stored into the series resonant circuit by $I_{D(H)}$ that flows through the resonant circuit and the transformer (see Figure 8-5). At the same time, the energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

2) Period B
After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 8-6).

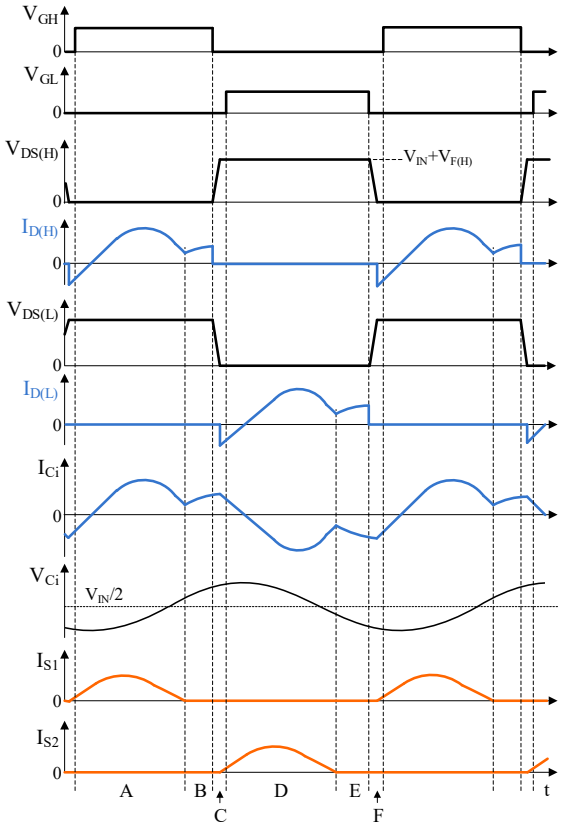

Figure 8-4. The Basic Operation Waveforms of Current Resonant Power Supply

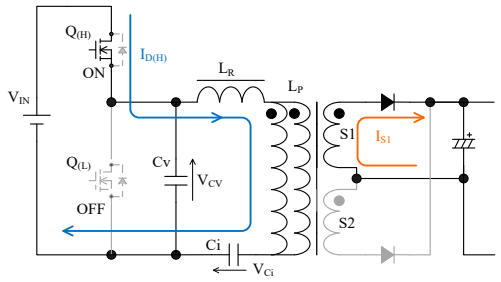

Figure 8-5. Operation in period A

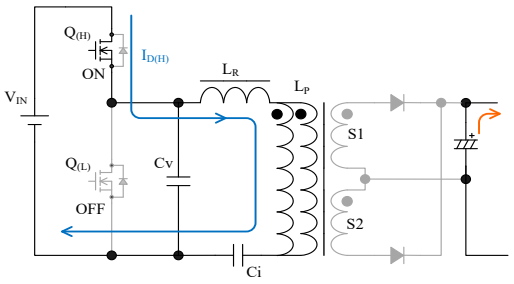

Figure 8-6. Operation in Period B

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3) Period C

C is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status. When $Q_{(H)}$ turns off, C_V is discharged by I_L that is supplied by the energy stored in the series resonant circuit applies (see Figure 8-7). When V_{CV} decreases to $V_{F(L)}$, $-I_{D(L)}$ flows through the body diode of $Q_{(L)}$; and V_{CV} is clamped to $V_{F(L)}$. After that, $Q_{(L)}$ turns on. Since $V_{DS(L)}$ is nearly zero at the point, $Q_{(L)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

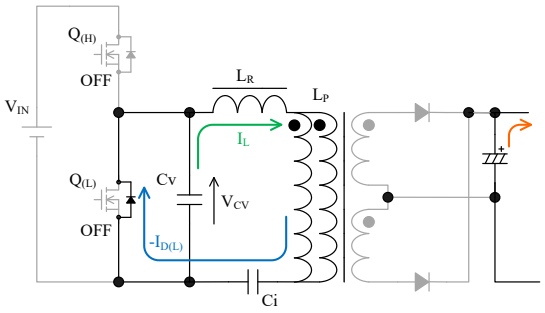

Figure 8-7. Operation in Period C

4) Period D

Immidiately after $Q_{(L)}$ turns on, $-I_{D(L)}$, which was flowing in Period C, continues to flow through $Q_{(L)}$ for a while. Then $I_{D(L)}$ flows as shown in Figure 8-8; and V_{Ci} is applied the primary winding voltage of the transformer. At the same time, energy is transferred to the secondary circuit. When the primary winding voltage can not keep the on status of the secondary rectifier, the energy transmittion to the secondary circuit is stopped.

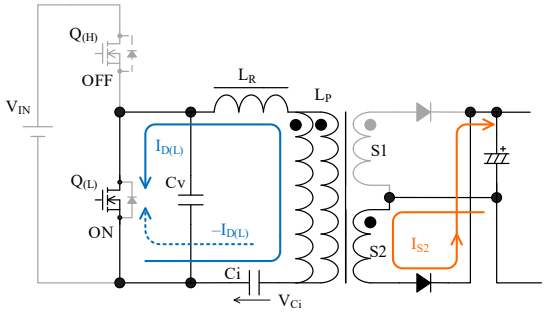

Figure 8-8. Operation in Period D

5) Period E

After the secondary side current becomes zero, the resonant current flows to the primary side only to charge Ci (see Figure 8-9).

6) Period F

F is the dead-time period. $Q_{(H)}$ and $Q_{(L)}$ are in off status.

When $Q_{(L)}$ turns off, C_V is charged by $-I_L$ that is supplied by the energy stored in the series resonant circuit applies (see Figure 8-10). When V_{CV} decreases to $V_{IN} + V_{F(H)}$, $-I_{D(H)}$ flows through body diode of $Q_{(H)}$; and V_{CV} is clamped to $V_{IN} + V_{F(H)}$. After that, $Q_{(H)}$ turns on. Since $V_{DS(H)}$ is nearly zero at the point, $Q_{(H)}$ operates in the ZVS and the ZCS; thus, the switching loss achieves nearly zero.

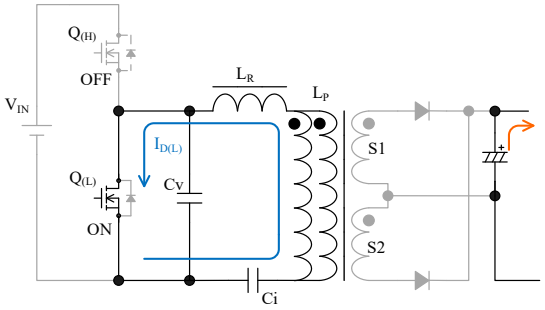

Figure 8-9. Operation in Period E

7) After the period F

Immidiately after $Q_{(H)}$ turns on, $-I_{D(H)}$, which was flowing in Period F, continues to flow through $Q_{(H)}$ for a while. Then, $I_{D(H)}$ flows again; and the operation returns to the period A. The above operation is repeated to transfer energy to the secondary side from the resonant circuit.

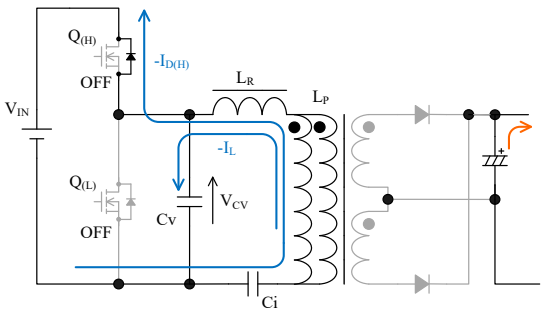

Figure 8-10. Operation in Period F

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8.2 Startup Operation

Figure 8-11 shows the VCC pin peripheral circuit. Figure 8-12 shows the startup operational waveforms.

The power supply starts as follows:

1) The mains input voltage is provided, and the VSEN pin voltage increases to the on-threshold voltage, $V_{SEN(ON)}$ = 1.300 V, or more.
2) The startup current, I_{ST}, which is a constant current of 6.0 mA is provided from the IC to capacitor C2 connected to the VCC pin, C2 is charged.
3) C_{ADJ} is charged by I_{ADJ} = −10μA to increase the ADJ pin voltage.
4) When the VCC pin voltage increases to the operation start voltage, $V_{CC(ON)}$ = 17.0 V, the REG pin voltage is output. At the same time, the ADJ pin outputs the PFC ON signal, and the PFC control IC is activated. The VCC pin voltage is decreased by the power dissipation of the IC.
5) When the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.8 V, the C9 connected to FB pin starts to be charged. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, or more, the swiching operation starts.

After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

During the IC operation, the rectified voltage from the auxiliary winding voltage, V_D, in Figure 8-11 is a power source to the VCC pin.

The winding turns of the winding D should be adjusted so that the VCC pin voltage is applied to equation (7) within the specification of the mains input voltage range and output load range of the power supply. The target voltage of the winding D is about 19 V.

$$V_{CC(BIAS)} < V_{CC} < V_{CC(OVP)}$$

$$\Rightarrow 9.8\ (V) < V_{CC} < 32.0\ (V) \qquad (7)$$

The startup time, t_{START}, is determined by the value of C2 and C6 connected to the CSS pin. Since the startup time for C6 is much smaller than that for C2, the startup time is approximately given as below:

$$t_{START} \approx C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{CC(ST)}|} \qquad (8)$$

where:

t_{START} is the startup time in s,

$V_{CC(INT)}$ is the initial voltage of the VCC pin in V, and

I_{ST} is the startup current, 6.0 mA

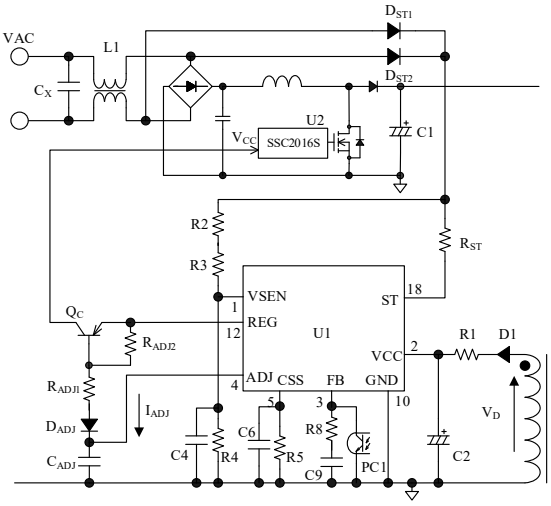

Figure 8-11. VCC Pin Peripheral Circuit

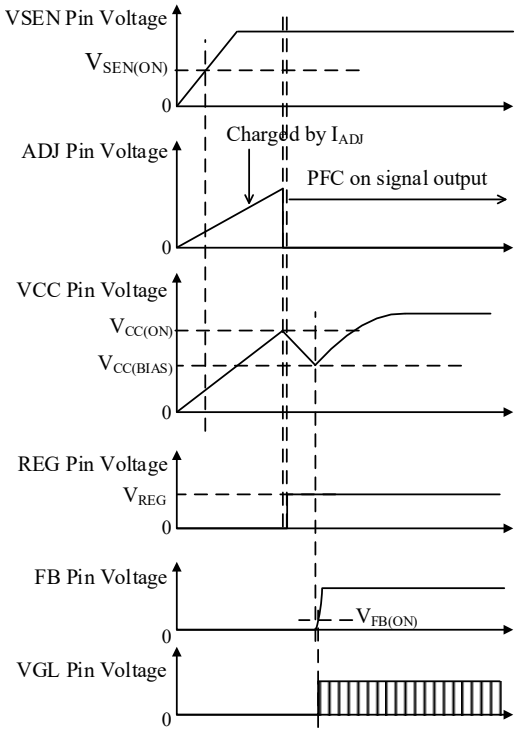

Figure 8-12. Startup Operation When PFC ON/OFF Function is Enabled

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8.3 Undervoltage Lockout (UVLO)

Figure 8-13 shows the relationship of V_{CC} and I_{CC}.

After the IC starts operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation by the Undervoltage Lockout (UVLO) Function and reverts to the state before startup again.

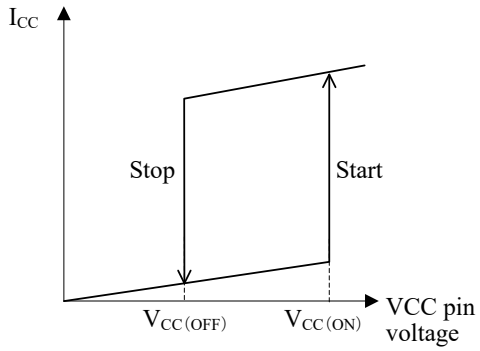

Figure 8-13. V_{CC} versus I_{CC}

8.4 Bias Assist Function

Figure 8-14 shows the VCC pin voltage behavior during the startup period.

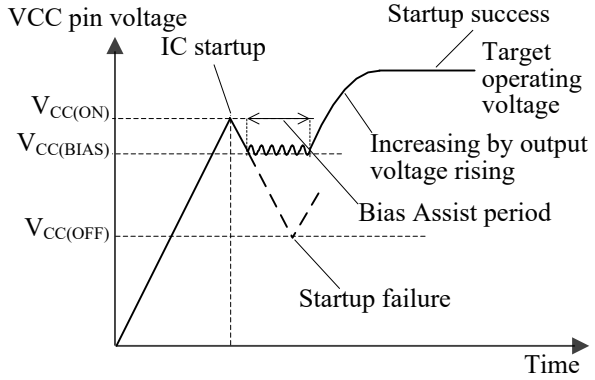

Figure 8-14. VCC pin voltage during startup period

When the conditions of Section 8.2 are fulfilled, the IC starts operation. Thus, the circuit current, I_{CC}, increases, and the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping due to the increase of I_{CC} and rising due to the increase of the auxiliary winding voltage, V_D.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation and a startup failure occurs.

In order to prevent this, when the VCC pin voltage decreases to the startup current threshold biasing voltage, $V_{CC(BIAS)}$ = 9.8 V, the Bias Assist Function is activated.

While the Bias Assist Function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current, I_{ST}, from the startup circuit.

It is necessary to check the startup process based on actual operation in the application, and adjust the VCC pin voltage, so that the startup failure does not occur.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ and the Bias Assist Function is activated, the power loss increases.

Thus, VCC pin voltage in normal operation should be set more than $V_{CC(BIAS)}$ by the following adjustments.

- The turns ratio of the auxiliary winding to the secondary-side winding is increased.
- The value of C2 in Figure 8-11 is increased and/or the value of R1 is reduced.

During all protection operation, the Bias Assist Function is disabled.

8.5 Soft Start Function

Figure 8-15 shows the Soft-start operation waveforms.

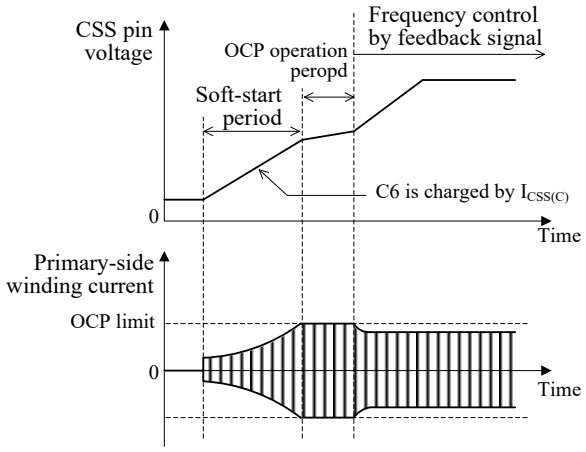

Figure 8-15. Soft-start operation

The IC has Soft Start Function to reduce stress of peripheral component and prevent the capacitive mode operation.

During the soft start operation, C6 connected to the CSS pin is charged by the CSS Pin Charge Current, $I_{CSS(C)}$ = −105 µA. The oscillation frequency is varied by the CSS pin voltage. The switching frequency gradually decreases from $f_{(MAX)SS}$* = 500 kHz at most, according to the CSS pin voltage rise. At same time, output power

* The maximum frequency during normal operation is $f_{(MAX)}$ = 300 kHz.

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increases. When the output voltage increases, the IC is operated with an oscillation frequency controlled by feedback.

When the IC becomes any of the following conditions, C6 is discharged by the CSS Pin Reset Current, $I_{CSS(R)}$ = 1.8 mA.

- The VCC pin voltage decreases to the operation stop voltage, $V_{CC(OFF)}$ = 8.9 V, or less.
- The VSEN pin voltage decreases to the off-threshold voltage, $V_{SEN(OFF)}$ = 1.100 V, or less.
- Any of protection operations in protection mode (OVP, OLP or TSD) is activated.

8.6 Minimum and Maximum Switching Frequency Setting

The minimum switching frequency is adjustable by the value of R5 (R_{CSS}) connected to the CSS pin. The relationship of R5 (R_{CSS}) and the externally adjusted minimum frequency, $f_{(MIN)ADJ}$, is shown in Figure 8-16.

The $f_{(MIN)ADJ}$ should be adjusted to more than the resonant frequency, f_O, under the condition of the minimum mains input voltage and the maximum output power.

The maximum switching frequency, f_{MAX}, is determined by the inductance and the capacitance of the resonant circuit. The f_{MAX} should be adjusted to less than the maximum frequency, $f_{(MAX)}$ = 300 kHz.

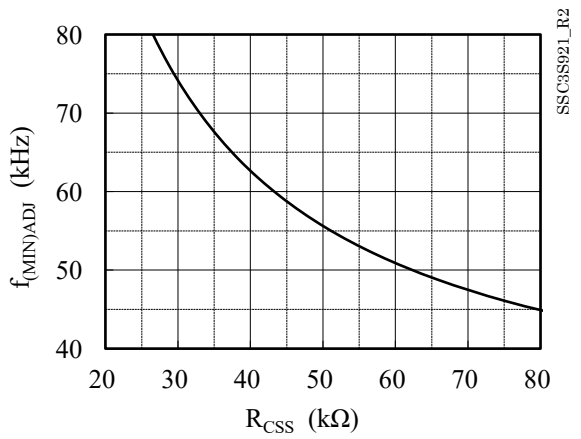

Figure 8-16. R5 (R_{CSS}) versus $f_{(MIN)ADJ}$

8.7 High-side Driver

Figure 8-17 shows a bootstrap circuit. The bootstrap circuit is for driving to $Q_{(H)}$ and is made by D3, R12 and C12 between the REG pin and the VS pin.

When $Q_{(H)}$ is OFF state and $Q_{(L)}$ is ON state, the VS pin voltage becomes about ground level and C12 is charged from the REG pin.

When the voltage of between the VB pin and the VS pin, V_{B-S}, increases to $V_{BUV(ON)}$ = 6.8 V or more, an internal high-side drive circuit starts operation. When V_{B-S} decreases to $V_{BUV(OFF)}$ = 6.4 V or less, its drive circuit stops operation. In case the both ends of C12 and D4 are short, the IC is protected by $V_{BUV(OFF)}$. D4 for protection against negative voltage of the VS pin

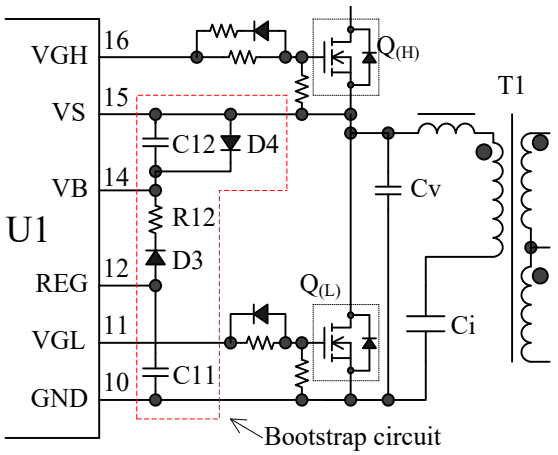

Figure 8-17. Bootstrap circuit

- D3
  D3 should be an ultrafast recovery diode of short recovery time and low reverse current. When the maximum mains input voltage of the apprication is 265VAC, it is recommended to use ultrafast recovery diode of V_{RM} = 600 V

- C11, C12, and R12
  The values of C11, C12, and R12 are determined by total gate charge, Qg, of external MOSFET and voltage dip amount between the VB pin and the VS pin in the burst mode of the standby mode change.
  C11, C12, and R12 should be adjusted so that the voltage between the VB pin and the VS is more than $V_{BUV(ON)}$ = 6.8 V by measuring the voltage with a high-voltage differential probe.
  The reference value of C11 is 0.47µF to 1 µF.
  The time constant of C12 and R12 should be less than 500 ns. The values of C12 and R22 are 0.047µF to 0.1 µF, and 2.2 Ω to 10 Ω.
  C11 and C12 should be a film type or ceramic capacitor of low ESR and low leakage current.

- D4
  D4 should be a Schottky diode of low forward voltage, V_F, so that the voltage between the VB pin and the VS pin must not decrease to the absolute maximum ratings of −0.3 V or less.

8.8 Constant Voltage Control Operation

Figure 8-18 shows the FB pin peripheral circuit. The

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FB pin is sunk the feedback current by the photo-coupler, PC1, connected to FB pin. As a result, since the oscillation frequency is controlled by the FB pin, the output voltage is controlled to constant voltage (in inductance area).

The feedback current increases under slight load condition, and thus the FB pin voltage decreases. While the FB pin voltage decreases to the oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, or less, the IC stops switching operation. This operation reduces switching loss, and prevents the increasing of the secondary output voltage. In Figure 8-18, R8 and C9 are for phase compensation adjustment, and C5 is for high frequency noise rejection.The secondary-side circuit should be designed so that the collector current of PC1 is more than 195 µA which is the absolute value of the maximum source current, $I_{FB(MAX)}$. Especially the current transfer ratio, CTR, of the photo coupler should be taken aging degradation into consideration.

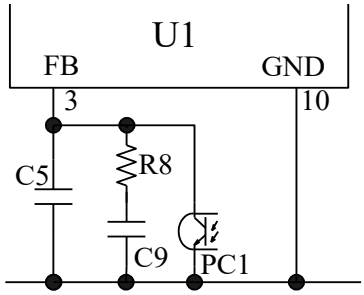

Figure 8-18. FB pin peripheral circuit

8.9 Standby Function

The IC has the Standby Function in order to increase circuit efficiency in light load. When the Standby Function is activated, the IC operates in the burst oscillation mode as shown in Figure 8-19.

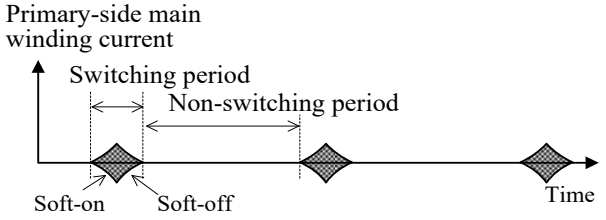

Figure 8-19. Standby waveform

The burst oscillation has periodic non-switching intervals. Thus, the burst mode reduces switching losses. Generally, to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. In addition, the IC has the Soft-on and the Soft-off Function in order to suppress rapid and sharp fluctuation of the drain current during the burst mode. thus, the audible noises can be reduced (see Section 8.9.2). The operation of the IC changes to the standby operation by the external signal (see Section 8.9.1).

8.9.1 Standby Mode Changed by External Signal

Figure 8-20 shows the standby mode change circuit with external signal. Figure 8-21 shows the standby change operation waveforms. When the standby terminal of Figure 8-20 is provided with the L signal, Q1 turns off, C10 connected to the SB pin is discharged by the sink current, $I_{SB(SNK)}$ = 10 µA, and the SB pin voltage decreases. When the SB pin voltage decrease to the SB Pin Oscillation Stop Threshold Voltage, $V_{SB(OFF)}$ = 0.5 V, the operation of the IC is changed to the standby mode. When SB pin voltage is $V_{SB(OFF)}$ = 0.5 V or less and FB pin voltage is Oscillation Stop Threshold Voltage $V_{FB(OFF)}$ = 0.20 V or less, the IC stops switching operation. When the standby terminal is provided with the H signal and the SB pin voltage increases to Standby Threshold Voltage $V_{SB(STB)}$ = 5.0 V or more, the IC returns to normal operation.

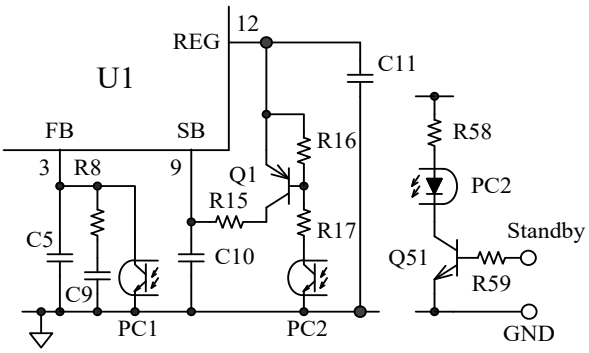

Figure 8-20. Standby mode change circuit

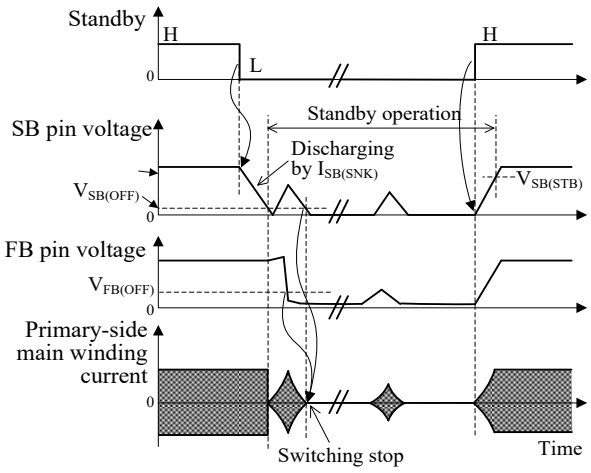

Figure 8-21. Standby change operation waveforms

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8.9.2 Burst Oscillation Operation

In standby operation, the IC operates burst oscillation where the peak drain current is suppressed by Soft-On /Soft-off Function in order to reduce audible noise from transformer. During burst oscillation operation, the switching oscillation is controlled by the SB pin voltage.

Figure 8-22 shows the burst oscillation operation waveforms.

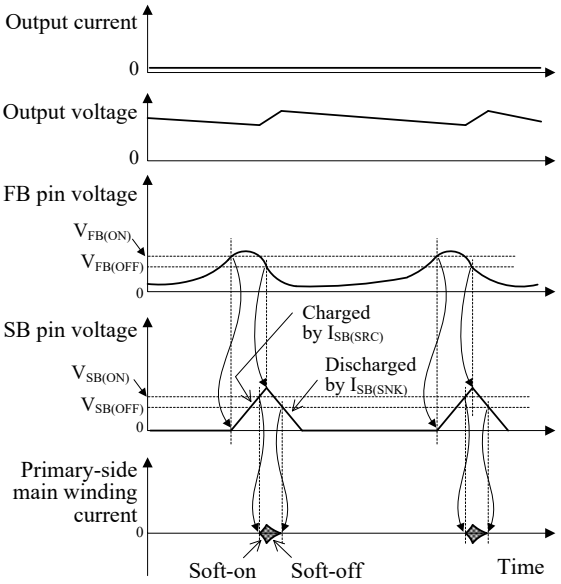

Figure 8-22. Burst oscillation operation waveforms

When the SB pin voltage decreases to $V_{SB(OFF)}$ = 0.5 V or less and the FB pin voltage decreases to $V_{FB(OFF)}$ = 0.20 V or less, the IC stops switching operation and the output voltage decreases. Since the output voltage decreases, the FB pin voltage increases. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, C10 is charged by $I_{SB(SRC)}$ = −10 µA, and the SB pin voltage gradually increases. When the SB pin voltage increases to the oscillation start threshold voltage, $V_{SB(ON)}$ = 0.6 V, the IC resumes switching operation, controlling the frequency control by the SB pin voltage. Thus, the output voltage increases (Soft-on). After that, when FB pin voltage decrease to oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, C10 is discharged by $I_{SB(SNK)}$ = 10 µA and SB pin voltage decreases. When the SB pin voltage decreases to $V_{SB(OFF)}$ again, the IC stops switching operation. Thus, the output voltage decreases (Soft-off).

The SB pin discharge time in the Soft-on and Soft-off Function depends on C10. When the value of C10 increases, the Soft-On/Soft-off Function makes the peak drain current suppressed, and makes the burst period longer. Thus, the output ripple voltage may increase and/or the VCC pin voltage may decrease. If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.8 V, the Bias Assist Function is always activated, and it results in the increase of power loss (see Section 8.4).

Thus, it is necessary to adjust the value of C10 while checking the input power, the output ripple voltage, and the VCC pin voltage. The reference value of C10 is about 0.001 µF to 0.1 µF.

8.9.3 PFC ON/OFF Function

Figure 8-23 shows the operational waveform of PFC ON/OFF Output Function. When output power decreases and SB pin voltage reaches $V_{SB(OFF)}$ = 0.5 V, the PFC ON/OFF Function activates and ADJ pin voltage increases to the ADJ Pin Voltage in Standby Operation, $V_{ADJ(H)}$ = V_{REG} = 10.0 V. When output power increases and SB pin voltage reaches $V_{SB(STB)}$ = 5.0 V, the ADJ pin voltage decreases to ADJ Pin Voltage in Normal Operation, $V_{ADJ(L)}$ = 1 V. Using the signal, the power supply of PFC control IC can be turned on/off when the IC becomes standby operation. When the operation starting voltage of PFC IC, $V_{CC(ON)_PFC}$, is less than V_{REG}, the PFC circuit on/off system can be realized by low component count as shown in Figure 8-24. SSC2016S that is Sanken PFC control IC is recommended.

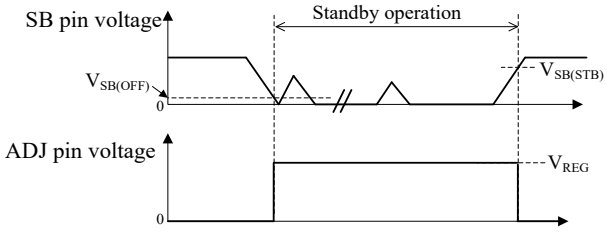

Figure 8-23. PFC ON/OFF Function

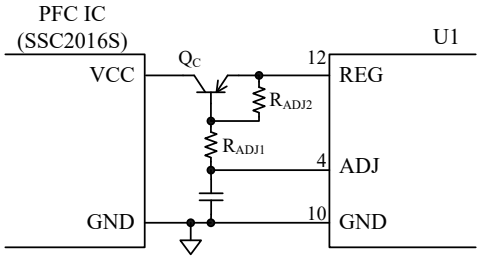

Figure 8-24. Typical circuit that PFC IC is stopped by the ADJ pin signal ($V_{CC(ON)_PFC}$ < V_{REG})

8.10 Automatic Dead Time Adjustment Function

The dead time is the period when both the high-side and the low-side power MOSFETs are off.

As shown in Figure 8-25, if the dead time is shorter than the voltage resonant period, the power MOSFET is

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turned on and off during the voltage resonant operation. In this case, the power MOSFET turned on and off in hard switching operation, and the switching loss increases. The Automatic Dead Time Adjustment Function is the function that the ZVS (Zero Voltage Switching) operation of $Q_{(H)}$ and $Q_{(L)}$ is controlled automatically by the voltage resonant period detection of IC. The voltage resonant period is varied by the power supply specifications (input voltage and output power, etc.). However, the power supply with this function is unnecessary to adjust the dead time for each power supply specification.

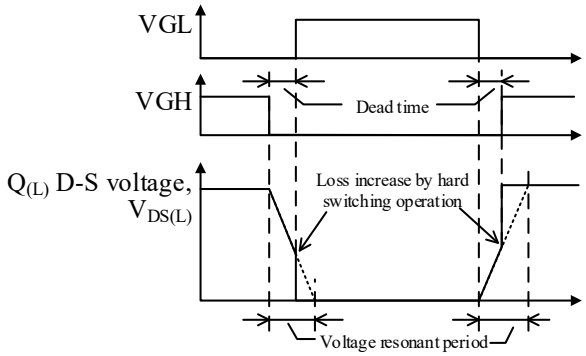

Figure 8-25. ZVS failure operation waveform

As shown in Figure 8-26, the VS pin detects the dv/dt period of rising and falling of the voltage between drain and source of the low-side power MOSFET, $V_{DS(L)}$, and the IC sets its dead time to that period. This function controls so that the high-side and the low-side power MOSFETs are automatically switched to Zero Voltage Switching (ZVS) operation. This function operates in the period from $t_{d(MIN)}$ = 0.24 µs to $t_{d(MAX)}$ = 1.65 µs.

In minimum output power at maximum input voltage and maximum output power at minimum input voltage, the ZCS (Zero Current Switching) operation of IC (the drain current flows through the body diode is about 600 ns as shown in Figure 8-27), should be checked based on actual operation in the application.

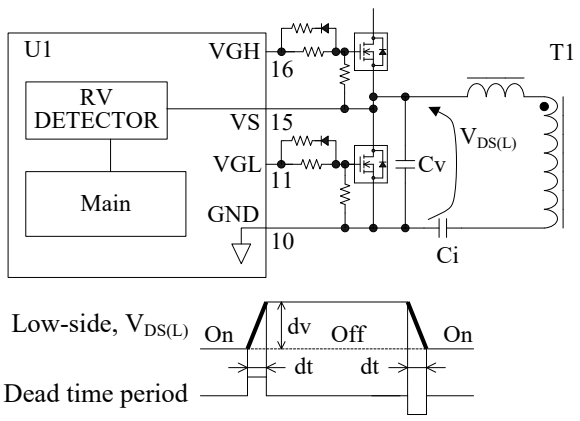

Figure 8-26. VS pin and dead time period

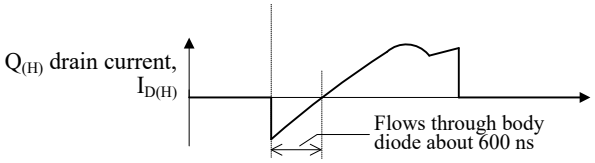

Figure 8-27. ZCS check point

8.11 Brown-In and Brown-Out Function

Figure 8-28 shows the VSEN pin peripheral circuit. This function detects the mains input voltage, and stops switching operation during low mains input voltage, to prevent exceeding input current and overheating.

R2 to R4 set the detection voltage of this function. When the VCC pin voltage is higher than $V_{CC(ON)}$, this function operates depending on the VSEN pin voltage as follows:

- When the VSEN pin voltage is more than $V_{SEN(ON)}$ = 1.300 V, the IC starts.
- When the VSEN pin voltage is less than $V_{SEN(OFF)}$ = 1.100 V, the IC stops switching operation.

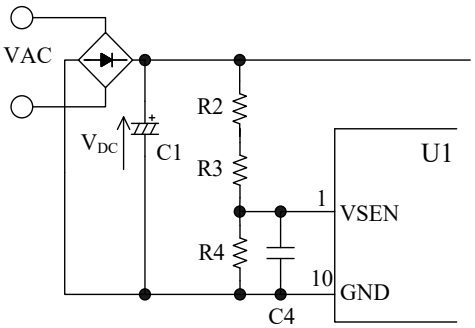

Figure 8-28. VSEN pin peripheral circuit

Given, the DC input voltage when the IC starts as $V_{IN(ON)}$, the DC input voltage when the switching operation of the IC stops as $V_{IN(OFF)}$. $V_{IN(ON)}$ is calculated by Equation (9). $V_{IN(OFF)}$ is calculated by Equation (10). Thus, the relationship between $V_{IN(ON)}$ and $V_{IN(OFF)}$ is Equation (11).

$$V_{IN(ON)} \approx V_{SEN(ON)} \times \frac{R2 + R3 + R4}{R4} \quad (9)$$

$$V_{IN(OFF)} \approx V_{SEN(OFF)} \times \frac{R2 + R3 + R4}{R4} \quad (10)$$

$$V_{IN(OFF)} \approx \frac{V_{SEN(OFF)}}{V_{SEN(ON)}} \times V_{IN(ON)} \quad (11)$$

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The detection resistance is calculated from Equation (9) as follows:

$$R2 + R3 \approx \frac{V_{IN(ON)} - V_{SEN(ON)}}{V_{SEN(ON)}} \times R4 \qquad (12)$$

Because R2 and R3 are applied high DC voltage and are high resistance, the following should be considered:

- Select a resistor designed against electromigration according to the requirement of the application, or
- Use a combination of resistors in series for that to reduce each applied voltage

The reference value of R2 is about 10 MΩ.

C4 shown in Figure 8-28 is for reducing ripple voltage of detection voltage and making delay time. The value is 0.1 µF or more, and the reference value is about 0.47 µF.

The value of R2, R3 and R4 and C4 should be selected based on actual operation in the application.

8.12 Capacitive Mode Detection Function

The resonant power supply is operated in the inductance area shown in Figure 8-29. In the capacitance area, the power supply becomes the capacitive mode operation (see Section 8.1). In order to prevent the operation, the minimum oscillation frequency is needed to be set higher than f_0 on each power supply specification. However, the IC has the capacitive mode operation Detection Function kept the frequency higher than f_0. Thus, the minimum oscillation frequency setting is unnecessary and the power supply design is easier. In addition, the ability of transformer is improved because the operating frequency can operate close to the resonant frequency, f_0.

The resonant current is detected by the RC pin, and the IC prevents the capacitive mode operation. When the capacitive mode is detected, C7 connected to the CL pin is charged by $I_{CL(SRC)}$ = −17 µA. When the CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.18). The detection voltage is changed to V_{RC1} = ±0.10 V or V_{RC2} = ±0.50 V depending on the load as shown in Figure 8-31 and Figure 8-32.

The Capacitive Mode Operation Detection Function operations as follows:

- **Period in which the $Q_{(H)}$ is ON**
  Figure 8-30 shows the RC pin waveform in the inductance area, and Figure 8-31 and Figure 8-32 shows the RC pin waveform in the capacitance area.
  In the inductance area, the RC pin voltage doesn't cross the plus side detection voltage in the downward direction during the on period of $Q_{(H)}$ as shown in Figure 8-30. On the contrary, in the capacitance area, the RC pin voltage crosses the plus side detection voltage in the downward direction. At this point, the capacitive mode operation is detected. Thus, $Q_{(H)}$ is turned off, and $Q_{(L)}$ is turned on, as shown in Figure 8-31 and Figure 8-32.

- **Period in which the $Q_{(L)}$ is on**
  Contrary to the above of $Q_{(H)}$, in the capacitance area, the RC pin voltage crosses the minus side detection voltage in the upward directiont during the on period of $Q_{(L)}$ At this point, the capacitive mode operation is detected. Thus, $Q_{(L)}$ is turned off and $Q_{(H)}$ is turned on.

As above, since the capacitive mode operation is detected by pulse-by-pulse and the operating frequency is synchronized with the frequency of the capacitive mode operation, and the capacitive mode operation is prevented. In addition to the adjusting method of R_{OCP}, C3, and R6 in Section 1.1, R_{OCP}, C3, and R6 should be adjusted so that the absolute value of the RC pin voltage increases to more than $|V_{RC2}|$ = 0.50 V under the condition caused the capacitive mode operation easily, such as startup, turning off the mains input voltage, or output shorted. The RC pin voltage must be within the absolute maximum ratings of −6 to 6 V.

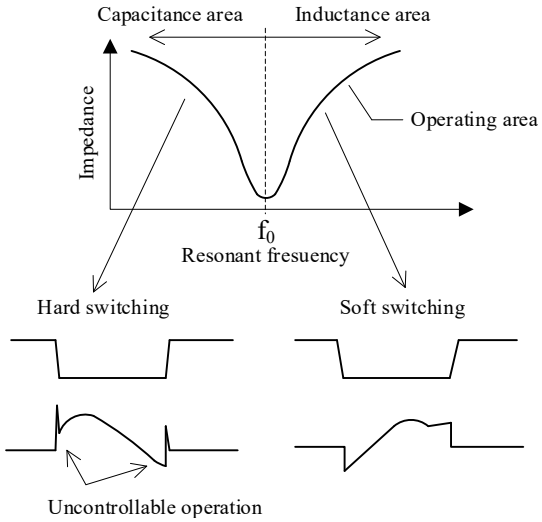

Figure 8-29. Operating area of resonant power supply

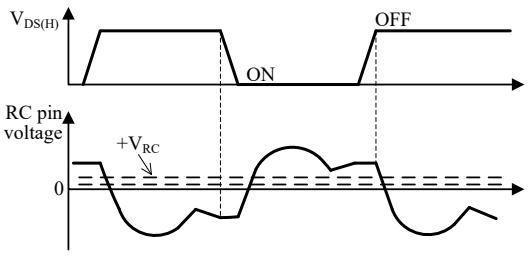

Figure 8-30. RC pin voltage in inductance area

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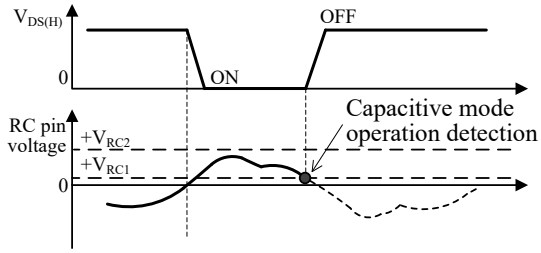

Figure 8-31. High side capacitive mode detection in light load

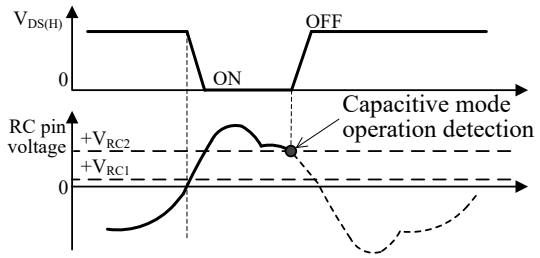

Figure 8-32. High side capacitive mode detection in heavy load

8.13 Input Electrolytic Capacitor Discharge Function

Figure 8-33 shows an application that residual voltage of the input capacitor, C1, is reduced after turning off the mains input voltage. R2 is connected to the AC input lines through D7 and D8. Just after turning off the mains input voltage, the VSEN pin voltage decreases to $V_{SEN(OFF)}$ = 1.100 V according to a short time of the time constant with R2 to R4 and C4, and C1 is discharged by the equivalent to I_{ST} = 6.0 mA.

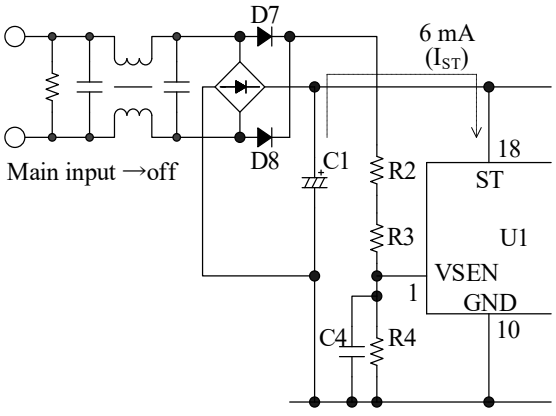

Figure 8-33. Input capacitor discharge

8.14 Reset Detection Function

In the startup period, the feedback control for the output voltage is inactive. If a magnetizing current may not be reset in the on-period because of unbalanced operation, a negative current may flow just before a power MOSFET turns off. This causes a hard switching operation, increases the stresses of the power MOSFET. Where the magnetizing current means the circulating current applied for resonant operation, and flows only into the primary-side circuit. To prevent the hard switching, the IC has the reset detection function.

Figure 8-35 shows the high-side operation and the reference drain current waveforms in a normal resonant operation and a reset failure operation. To prevent the hard switching operation, the reset detection function operates such as an on period is extended until the absolute value of a RC pin voltage, $|V_{RC1}|$, increases to 0.10 V or more. When the on period reaches the maximum reset time, $t_{RST(MAX)}$ = 5 µs, the on-period expires at that moment, i.e., the power MOSFET turns off (see Figure 8-34).

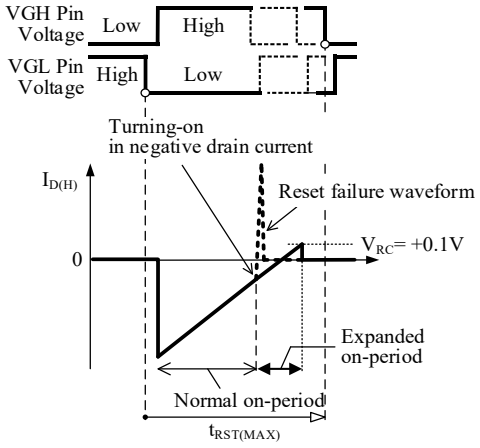

Figure 8-34. Reset Detection Operation Example at High-side On Period

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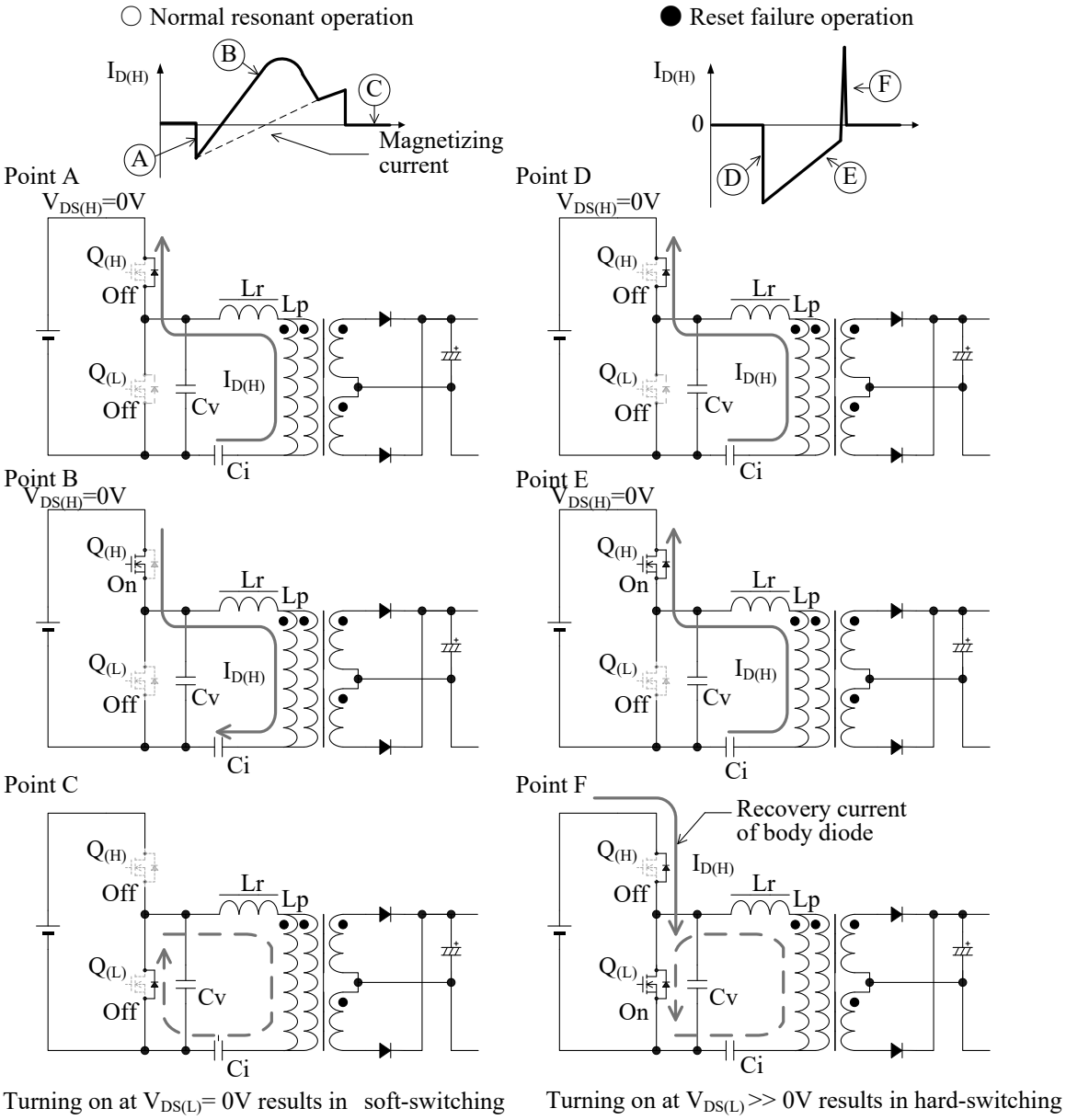

Figure 8-35. Reference High-side Operation and Drain Current Waveforms in Normal Resonant Operation and in Reset Failure Operation

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8.15 Overvoltage Protection (OVP)

When the voltage between the VCC pin and the GND pin is applied to the OVP threshold voltage, $V_{CC(OVP)}$ = 32.0 V, or more, the Overvoltage Protection (OVP) is activated, and the IC stops switching operation in protection mode. After stopping, the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the Undervoltage Lockout (UVLO) Function is activated, and the IC reverts to the state before startup again.

After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$ = 17.0 V, and the IC restarts. During the protection mode, restart and stop are repeated. When the fault condition is removed, the IC returns to normal operation automatically. When the auxiliary winding supplies the VCC pin voltage, the OVP is able to detect an excessive output voltage, such as when the detection circuit for output control is open in the secondary-side circuit because the VCC pin voltage is proportional to the output voltage.

The output voltage of the secondary-side circuit at OVP operation, $V_{OUT(OVP)}$, is approximately given as below:

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 32(V) \quad (13)$$

where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

8.16 REG Overvoltage Protection (REG_OVP)

The IC has REG Overvoltage Protection (REG_OVP) for the overvoltage of the REG pin.

When the REG pin voltage increases to REG Pin OVP Threshold Voltage, $V_{REG(OVP)}$ = 12.4 V, the REG_OVP is activated and the IC stops switching operation at latched state. Releasing the latched state is done by dropping the VCC pin voltage below REG Pin Overvoltage Protection Release Threshold Voltage, $V_{CC(L.OFF)}$ = 5.0 V.

8.17 Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) detects the drain current, I_D, on pulse-by-pulse basis, and limits output power. In Figure 8-36, this circuit enables the value of C3 for shunt capacitor to be smaller than the value of Ci for current resonant capacitor, and the detection current through C3 is small. Thus, the loss of the detection resistor, R_{OCP}, is reduced, and R_{OCP} is a small-sized one available. There is no convenient method to calculate the accurate resonant current value according to the mains input and output conditions, and others. Thus, R_{OCP}, C3, and C6 should be adjusted based on actual operation in the application. The following is a reference adjusting method of R_{OCP}, C3, R6, and C8:

- C3 and R_{OCP}
  C3 is 100pF to 330pF (around 1 % of Ci value).
  R_{OCP} is around 100 Ω.
  Given the current of the high side power MOSFET at ON state as $I_{D(H)}$. R_{OCP} is calculated Equation (14).
  The detection voltage of R_{OCP} is used the detection of the capacitive mode operation (see Section 8.12). Therefore, setting of R_{OCP} and C3 should be taken account of both OCP and the capacitive mode operation.

$$R_{OCP} \approx \frac{|V_{RC(L)}|}{I_{D(H)}} \times \left(\frac{C3 + Ci}{C3}\right) \quad (14)$$

- R6 and C8 are for high frequency noise reduction.
  R6 is 100 Ω to 470 Ω. C6 is 100 pF to 1000 pF.

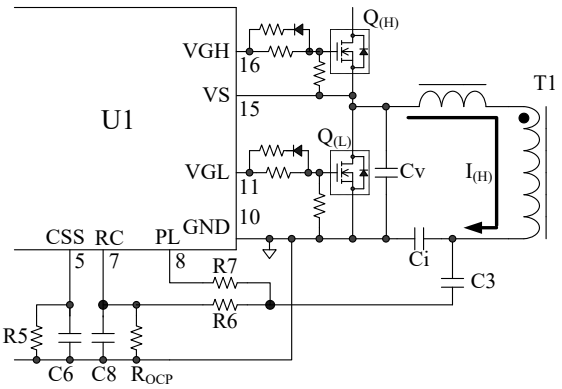

Figure 8-36. RC pin peripheral circuit

The OCP operation has two-step threshold voltage as follows:

Step I, RC pin threshold voltage (Low), $V_{RC(L)}$:
This step is active first. When the absolute value of the RC pin voltage increases to more than $|V_{OC(L)}|$ = 1.50 V, C6 connected to the CSS pin is discharged by $I_{CSS(L)}$ = 1.8 mA. Thus, the switching frequency increases, and the output power is limited. During discharging C6, when the absolute value of the RC pin voltage decreases to $|V_{RC(L)}|$ or less, the discharge stops.

Step II, RC pin threshold voltage (High-speed), $V_{RC(S)}$:
This step is active second. When the absolute value of the RC pin voltage increases to more than $|V_{RC(S)}|$ = 2.30 V, the high-speed OCP is activated, and power MOSFETs reverse on and off. At the same time, C6 is discharged by $I_{CSS(S)}$ = 20.5 mA. Thus, the switching

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frequency quickly increases, and the output power is quickly limited. This step operates as protections for exceeding overcurrent, such as the output shorted.

When the absolute value of the RC pin voltage decreases to $|V_{RC(S)}|$ or less, the operation is changed to the above Step I.

8.18 Overload Protection (OLP)

Figure 8-37 shows the Overload Protection (OLP) waveforms.

When the absolute value of RC pin voltage increases to $|V_{RC(L)}| = 1.50$ V by increasing of output power, the Overcurrent Protection (OCP) is activated. After that, the C7 connected to CL pin is charged by $I_{CL(SRC)} = -17$ µA. When the OCP state continues and CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated.

When CL pin voltage becomes the threshold voltage of OLP, $V_{CL(OLP)} = 4.2$ V, the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.15). When the fault condition is removed, the IC returns to normal operation automatically.

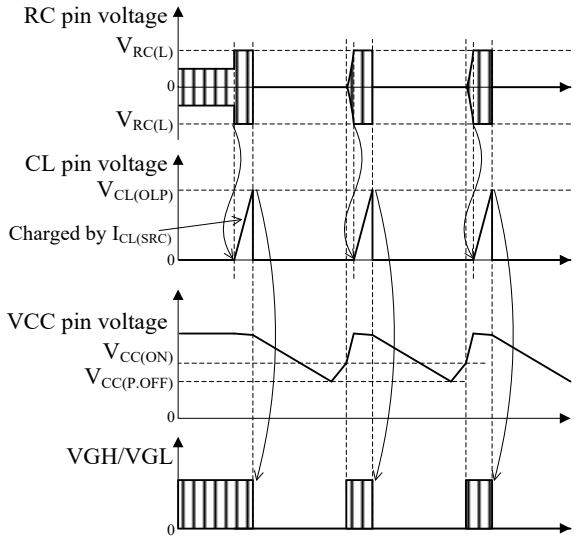

Figure 8-37. OLP waveform

- **PL Pin and CL Pin Setup:**
  The primary-side winding current as shown in Figure 8-38 includes the magnetizing current not transferred to the secondary-side circuit, and the load current proportional to the output current.
  The current separated from the primary-side winding current by C3 flows to the PL pin. As shown in Figure 8-39, the primary-side winding current flows to the C7 connected to CL pin during the high side power MOSFET turning on. The magnetizing current becomes zero by charging and discharging. Only the load current is charged to C7. As a result, the CL pin voltage is proportional to the output current.
  On actual operation of the application, C7 connected to the CL pin should be adjusted so that ripple voltage of the CL pin reduces. R7 connected to the PL pin should be adjusted so that the OLP at the minimum mains input voltage is activated before the OCP limited by the low threshold voltage of OCP, $V_{RC(L)}$.
  The PL pin voltage and the CL pin voltage must be within the absolute maximum ratings of −0.3 to 6 V, by adjusting R7, in the OCP operation point at the minimum mains input voltage.
  When the proportional voltage to the output current is unused, the PL pin should be pulled down by the resistance of about 47 kΩ connected between PL pin and GND pin.

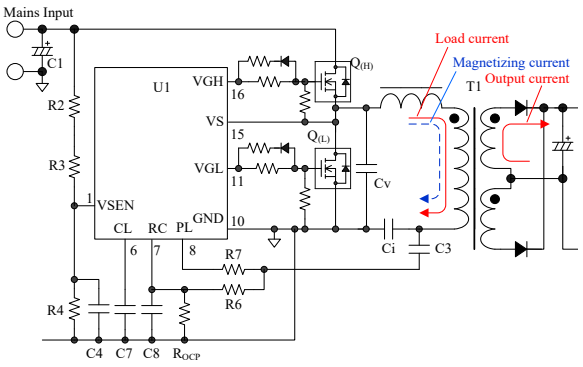

Figure 8-38. the peripheral circuit of PL pin and CL pin

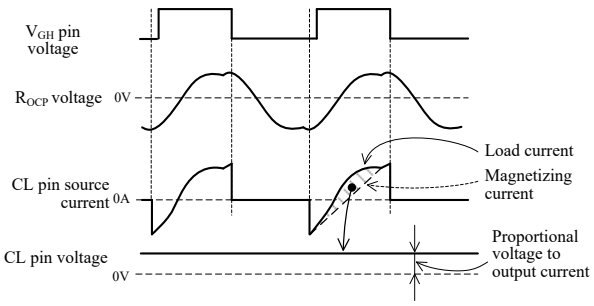

Figure 8-39. The waveforms of CL pin

8.19 Thermal Shutdown (TSD)

When the junction temperature of the IC reach to the Thermal Shutdown Temperature $T_{J(TSD)} = 140$ °C (min.), Thermal Shutdown (TSD) is activated and the IC stops switching operation. When the VCC pin voltage is decreased to $V_{CC(P.OFF)} = 8.9$ V or less and the junction temperature of the IC is decreased to less than $T_{J(TSD)}$, the IC restarts.

During the protection mode, restart and stop are repeated. When the fault condition is removed, the IC returns to normal operation automatically.

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9. Design Notes

9.1 External Components

Take care to use the proper rating and proper type of components.

9.1.1 Input and Output Electrolytic Capacitors

Apply proper derating to a ripple current, a voltage, and a temperature rise. It is required to use the high ripple current and low impedance type electrolytic capacitor that is designed for switch mode power supplies.

9.1.2 Resonant Transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce the effect of the eddy current and the skin effect, the wire of transformer should be used a bundle of fine litz wires.

9.1.3 Current Detection Resistor, R_{OCP}

To reduce the effect of the high frequency switching current flowing through R_{OCP}, choose the resister of a low internal inductance type. In addition, its allowable dissipation should be chosen suitable.

9.1.4 Current Resonant Capacitor, Ci

Since a large resonant current flows through Ci, Ci should be used a low loss and a high current capability capacitor such as a polypropylene film capacitor. In addition, Ci must be taken into account its frequency characteristic because a high frequency current flows.

9.1.5 Gate Pin Peripheral Circuit

The VGH and VGL pins are gate drive outputs for external power MOSFETs. These peak source and sink currents are –540 mA and 1.50 A, respectively.

To make a turn-off speed faster, connect the diode, D_S, as shown in Figure 9-1. When R_A and D_S is adjusted, the following contents should be taken into account: the power losses of power MOSFETs, gate waveforms (for a ringing reduction caused by a pattern layout, etc.), and EMI noises. To prevent the malfunctions caused by steep dv/dt at turn-off of power MOSFETs, connect R_{GS} of 10 kΩ to 100 kΩ between the Gate and Source pins of the power MOSFET with a minimal length of PCB traces. When these gate resistances are adjusted, the gate waveforms should be checked that the dead time is ensured as shown in Figure 9-2.

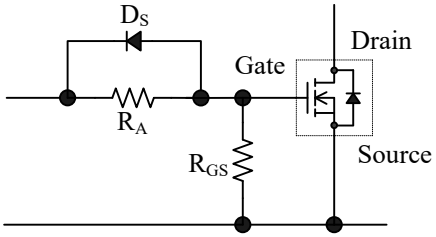

Figure 9-1. Power MOSFET Peripheral Circuit

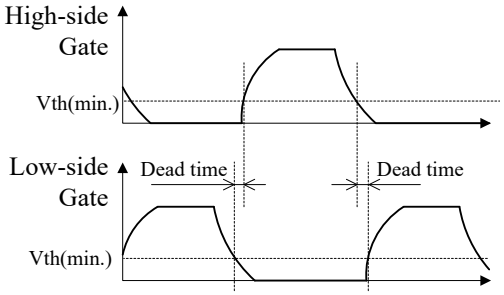

Figure 9-2. Dead Time Confirmation

9.2 PCB Trace Layout and Component Placement

The PCB circuit design and the component layout significantly affect a power supply operation, EMI noises, and power dissipation. Thus, to reduce the impedance of the high frequency traces on a PCB (see Figure 9-3), they should be designed as wide trace and small loop as possible. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

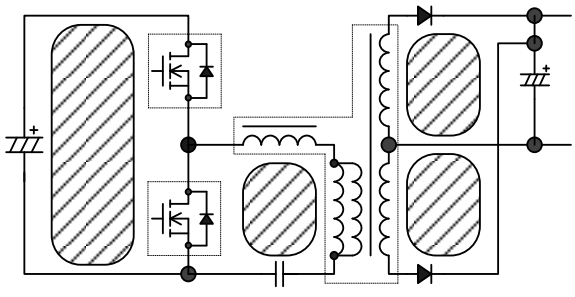

Figure 9-3. High frequency current loops (hatched areas)

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Figure 9-4 shows the circuit design example. The PCB trace design should be also taken into account as follows:

1) Main Circuit Trace
The main traces that switching current flows should be designed as wide trace and small loop as possible.

2) Control Ground Trace
If the large current flows through a control ground, it may cause varying electric potential of the control ground; and this may result in the malfunctions of the IC. Therefore, connect the control ground as close and short as possible to the GND pin at a single-point ground (or star ground) that is separated from the power ground.

3) VCC Trace
The trace for supplying power to the IC should be as small loop as possible. If C3 and the IC are distant from each other, a film capacitor C_f (about 0.1 µF to 1.0 µF) should be connected between the VCC and GND pins with a minimal length of PCB traces.

4) Trace of Peripheral Components for the IC Control
These components should be placed close to the IC, and be connected to the corresponding pin of the IC with as short trace as possible.

5) Trace of Bootstrap Circuit Components
These components should be connected to the IC pin with as short trace as possible. In addition, the loop for these should be as small as possible.

6) Secondary Side Rectifier Smoothing Circuit Trace
The traces of the rectifier smoothing loops carry the switching current. Thus it should be designed as wide trace and small loop as possible.

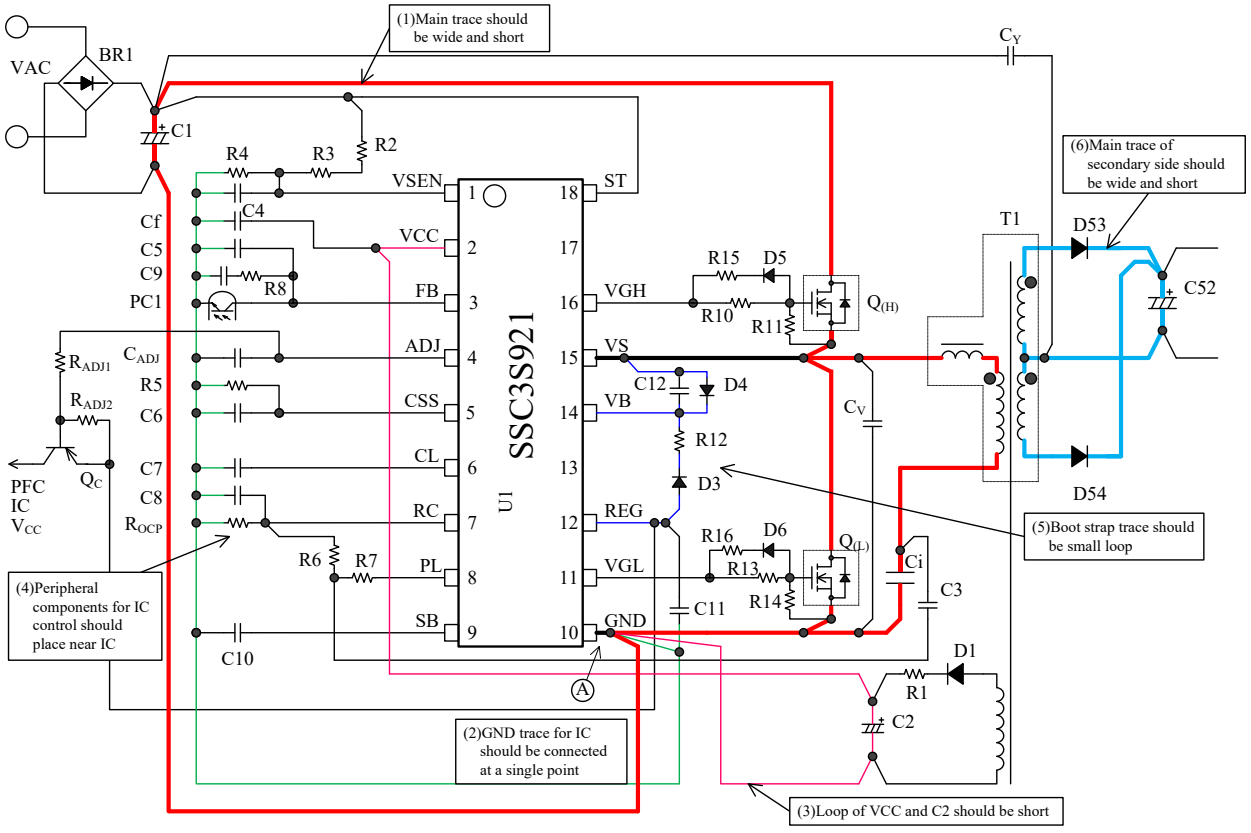

Figure 9-4. Peripheral circuit trace example around the IC

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10. Pattern Layout Example

The following shows the PCB pattern layout example and the schematic of circuit using the SSC3S921.

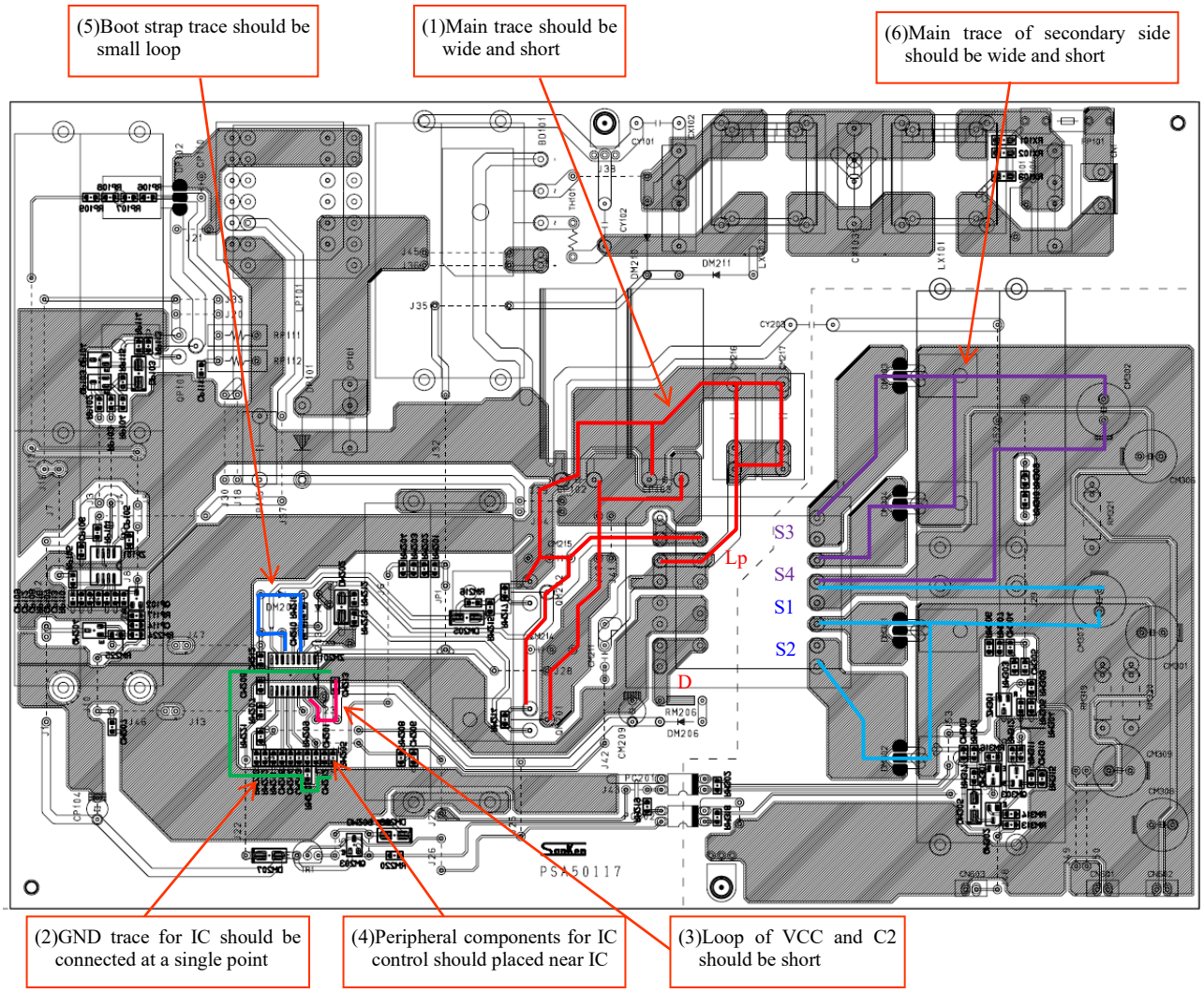

Figure 10-1. PCB pattern layout example

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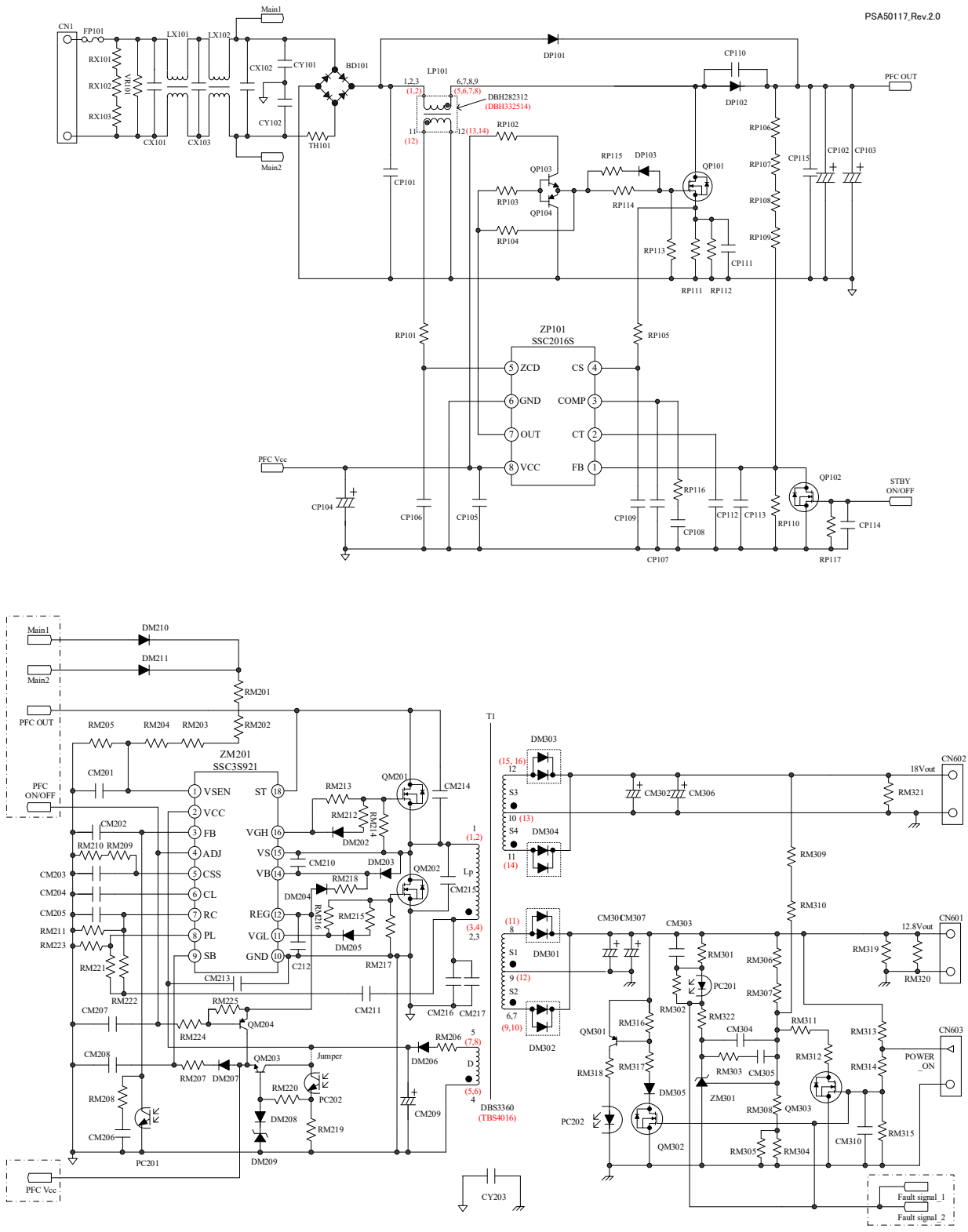

Figure 10-2. PCB pattern layout example circuit

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Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

Teklif isteyin

www.entegreci.com | **destek@entegreci.com** | **0850 305 90 34**

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