Quasi-Resonant Off-Line Switching Control ICs

SSC1S310A Series

Data Sheet

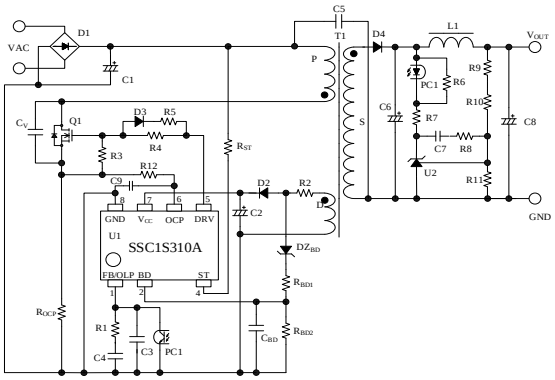
Description

SSC1S310A series is the controller ICs of a quasi-resonant mode for a switching power supplies. The IC incorporates a startup circuit and a standby function to reduce a power consumption and standby power. In normal operation, the quasi-resonant mode operation achieves high efficiency and low noise. In addition, in medium to low load conditions, the operation mode is automatically changes the quasi-resonant mode to the bottom-skip mode to improve efficiency. The IC is provided in the SOIC8 package. The power supply that is a low component counts and a high performance-to-cost can be achieved by the rich set of protection features.

Features

- Multi-Mode Control
  (High efficiency operation in all range of loads)
- Automatic Standby Function
  (Standby power is inproved by burst oscillation mode)
- Input Power at No Load:
  <30mW at 100 VAC
  <50mW at 230 VAC
- Bottom-Skip Function
  (Switching loss in medium to low loads is reduced)
- Step-on Burst Oscillation Function
  (Transformer audible noises are reduced)
- Bias Assist Function
- Soft-Start Function
- Adjustable Startup Voltage
- Maximum On-time Limitation Function
- VCC Operational Range Expanded
- Leading Edge Blanking (LEB) Function
  (External Filter Components are reduced)
- Protection Functions
  Overcurrent Protection (OCP): Pulse-by-pulse
  Overvoltage Protection (OVP)
  Overload Protection (OLP)
  Thermal Shutdown (TSD)

Typical Application



Packages

SOIC8



Not to scale

Specifications

- V_{CC} Maximum rating: 35 V
- Operation Start Voltage, $V_{CC(ON)}$: 15.1 V (typ.)
- PWM Operation Frequency, f_{OSC}: 21.0 kHz (typ.)
- Maximum On-time, $t_{ON(MAX)}$: 40.0 µs (typ.)

Selection Guide

Part Number	Protection Operation (OVP, OLP, TSD)
SSC1S311A	Auto-restart
SSC1S312A	Latched Shutdown

Applications

- Digital Appliance
- Office Automation (OA) Equipment
- White Goods
- Industrial Apparatus
- Communication Facilities

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Pins	Rating	Unit
Supply Voltage of Control Part	V_{CC}		7 − 8	35	V
Startup Pin Voltage	V_{ST}		4 − 8	−0.3 to 600	V
OCP Pin Voltage	V_{OCP}		6 − 8	−2.0 to 6.0	V
FB Pin Voltage	V_{FB}		1 − 8	−0.3 to 7.0	V
FB Pin Current	I_{FB}		1 − 8	10.0	mA
BD Pin Voltage	V_{BD}		2 − 8	−6.0 to 6.0	V
Allowable Power Dissipation	P_D		—	0.14	W
Operating Ambient Temperature	T_{OP}		—	−40 to 125	°C
Storage Temperature	T_{stg}		—	−40 to 125	°C
Junction Temperature	T_j		—	150	°C

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 20 V.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		7−8	13.8	15.1	17.3	V
Operation Stop Voltage[1]	$V_{CC(OFF)}$		7−8	8.4	9.4	10.7	V
Circuit Current in Operation	$I_{CC(ON)}$		7−8	—	1.3	3.7	mA
Circuit Current in Non-Operation	$I_{CC(OFF)}$	V_{CC} = 13 V	7−8	—	4.5	50	µA
Startup Circuit Operation Voltage	$V_{START(ON)}$		4−8	18	21	24	V
Startup Current	$I_{CC(STARTUP)}$	V_{CC} = 13 V	7−8	−4.5	−3.1	−1.0	mA
Startup Current Supply Threshold Voltage[1]	$V_{CC(BIAS)}$		7−8	9.5	11.0	12.5	V
PWM Operation Frequency	f_{OSC}		5−8	18.4	21.0	24.4	kHz
Soft-Start Operation Period	t_{SS}		5−8	—	6.05	—	ms
Normal Operation							
Bottom-Skip Operation Threshold Voltage 1	$V_{OCP(BS1)}$		6−8	0.487	0.572	0.665	V
Bottom-Skip Operation Threshold Voltage 2	$V_{OCP(BS2)}$		6−8	0.200	0.289	0.380	V
Quasi-Resonant Operation Threshold Voltage 1[2]	$V_{BD(TH1)}$		2−8	0.14	0.24	0.34	V

[1] $V_{CC(BIAS)} > V_{CC(OFF)}$

[2] $V_{BD(TH1)} > V_{BD(TH2)}$

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Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Quasi-Resonant Operation Threshold Voltage 2[(2)]	$V_{BD(TH2)}$		2−8	0.07	0.17	0.27	V
Maximum Feedback Current	$I_{FB(MAX)}$		1−8	−320	−205	−120	µA
Standby Operation							
Standby Operation Threshold Voltage	$V_{FB(STBOP)}$		1−8	0.45	0.80	1.15	V
Protection Operation							
Maximum On-time	$t_{ON(MAX)}$		5−8	30.0	40.0	50.0	µs
Leading Edge Blanking Time	t_{BW}		5−8	—	495	—	ns
Overcurrent Detection Threshold Voltage (Normal Operation)	$V_{OCP(H)}$		6−8	0.820	0.910	1.000	V
Overcurrent Detection Threshold Voltage (Input Compensation in Operation)	$V_{OCP(L)}$	V_{BD} = −3 V	6−8	0.560	0.660	0.760	V
BD Pin Current	$I_{BD(O)}$	V_{BD} = −3 V	2−8	−250	−83	−30	µA
OLP Bias Current	$I_{FB(OLP)}$	$V_{FB/OLP}$ = 5V	1−8	−15	−10	−5	µA
OLP Threshold Voltage	$V_{FB(OLP)}$		1−8	5.50	5.96	6.40	V
Circuit Current after OLP	$I_{CC(OLP)}$		7−8	—	575	—	µA
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		7−8	28.5	31.5	34.0	V
FB Pin Maximum Voltage in Feedback Operation	$V_{FB(MAX)}$	I_{FB} = −12 µA	1−8	3.70	4.05	4.40	V
Thermal Shutdown Temperature	$T_{j(TSD)}$		—	135	—	—	°C
Drive Circuit							
DRV Pin Output Voltage	V_{DRV}		5−8	7.5	8.1	8.7	V
DRV Pin Source Current (Peak)	$I_{DRV(SO)}$		5−8	—	−150	—	mA
DRV Pin Sink Current (Peak)	$I_{DRV(SI)}$		5−8	—	608	—	mA
Thermal Characteristics							
Thermal Resistance	θ_{j-A}		—	—	—	180	°C /W

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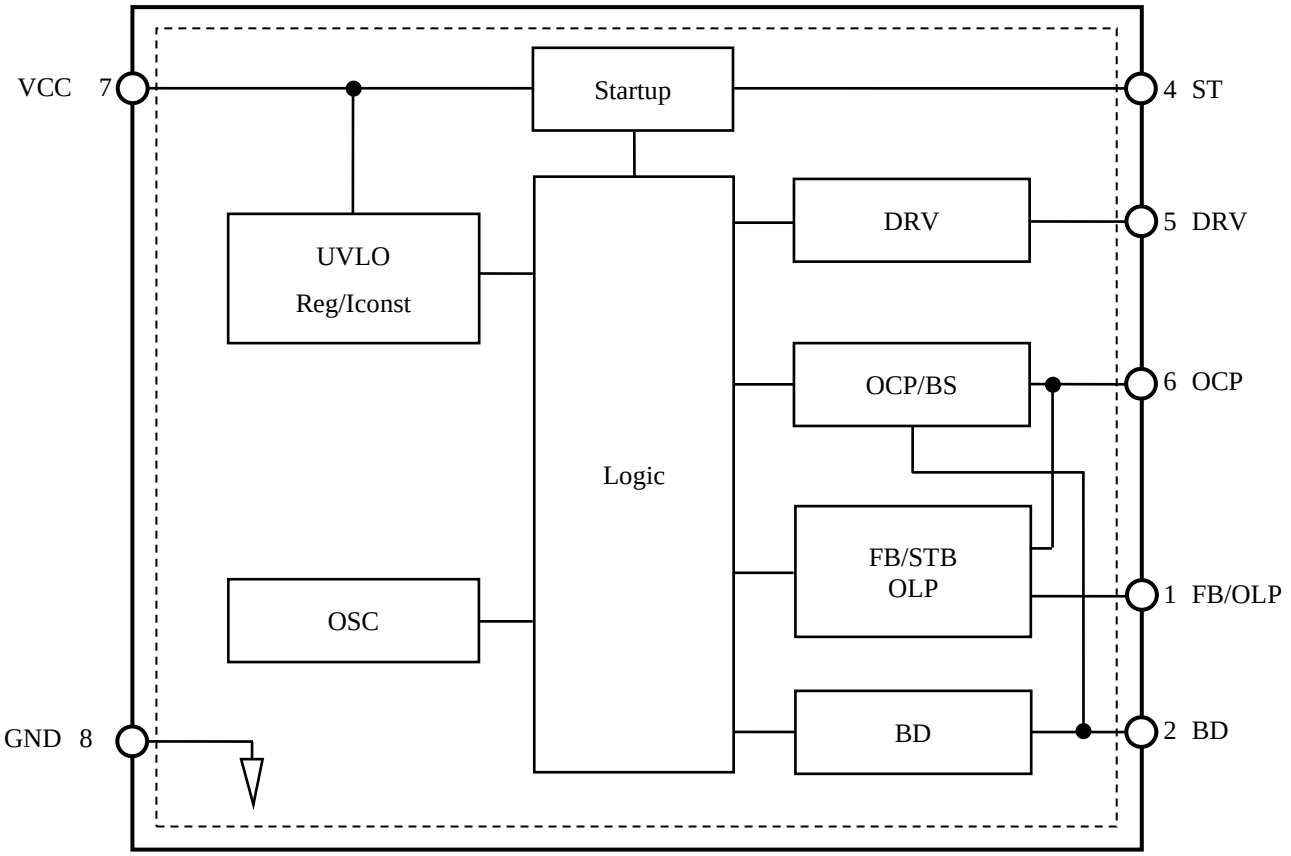
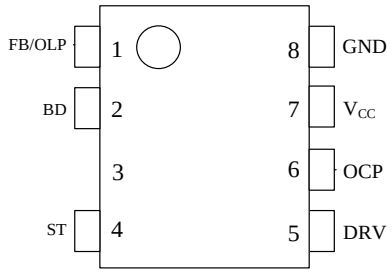
3. Block Diagram



4. Pin Configuration Definitions



Number	Name	Function
1	FB/OLP	Constant voltage control, standby control, and Overload detection signal input
2	BD	Bottom detection and input compensation signal input
3	—	(Pin removed)
4	ST	Startup current input
5	DRV	Gate drive output
6	OCP	Overcurrent detection signal input
7	VCC	Supply voltage input and overvoltage detection signal input
8	GND	Ground

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5. Typical Applications

The startup voltage of Figure 5-1 is about 21 V which is Startup Circuit Operation Voltage, $V_{START(ON)}$. When the startup voltage increases more than this, Figure 5-2 is available, adding DZ_{ST} in series with the ST pin.
The startup voltage after adding DZ_{ST}, $V_{START(ON)}'$ is calculated as follows:

$$V_{START(ON)}' = V_{START(ON)} + V_{ZST} \quad (1)$$

where:
$V_{START(ON)}$ is the Startup Circuit Operation Voltage, about 21 V, and
V_{ZST} is the zener voltage of DZ_{ST}.

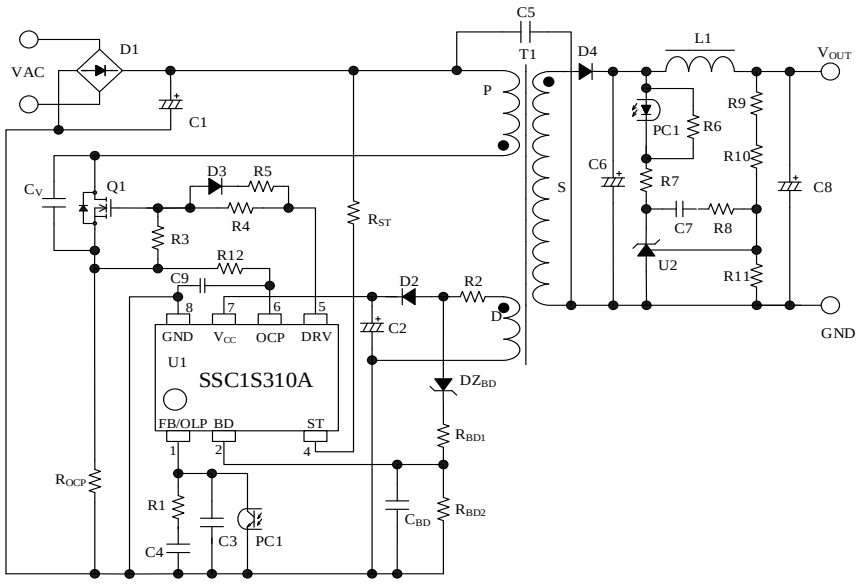

Figure 5-1. Application Circuit Example 1

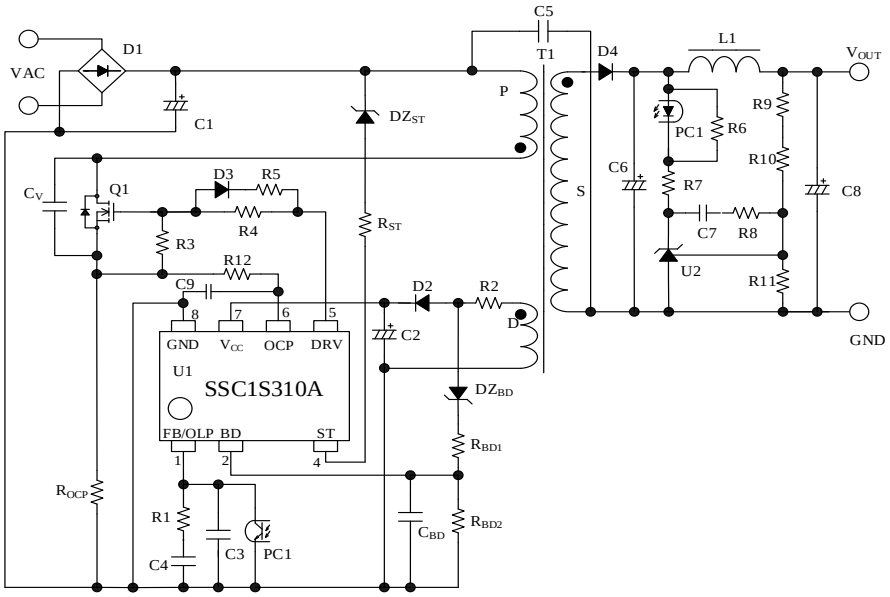

Figure 5-2. Application Circuit Example 2 (Adjustable Startup Voltage)

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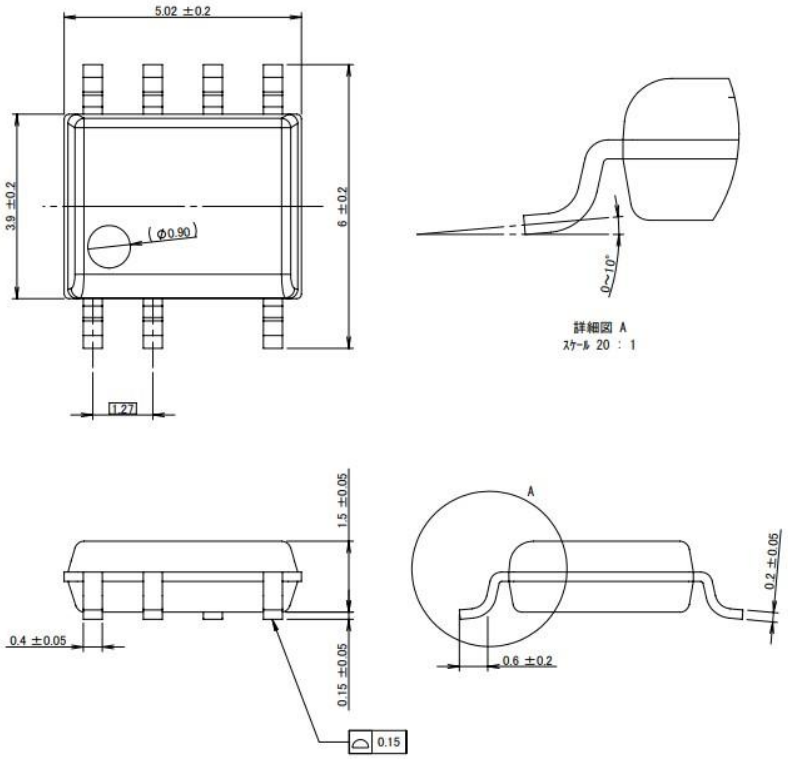
6. Physical Dimensions

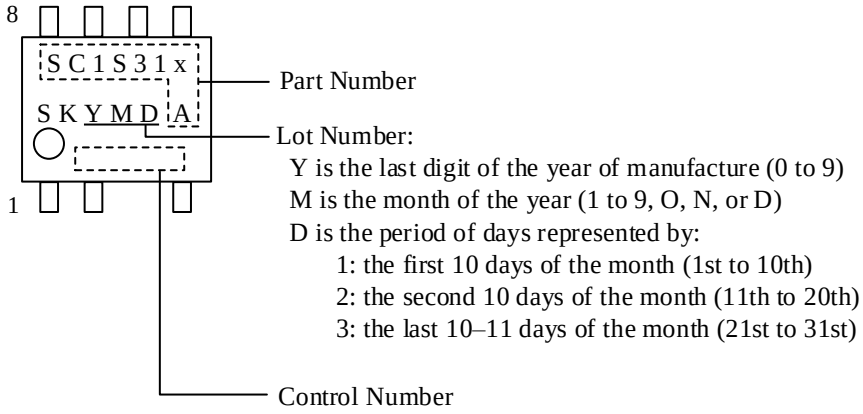
● **SOIC8**



NOTES:

- Dimensions in millimeters
- Pb-free

7. Marking Diagram



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8. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

8.1. Startup Operation

8.1.1. Startup Period

Figure 8-1 shows VCC pin peripheral circuit.

The built-in startup circuit is connected to the ST pin, and it generates a constant current, $I_{CC(STARTUP)}$ = –3.1 mA, to charge capacitor C2 connected to the VCC pin. During this process, when the VCC pin voltage reaches $V_{CC(ON)}$ = 15.1 V, the control circuit starts operation. After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

The approximate startup time, t_{START}, is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left|I_{CC(STARTUP)}\right|} \quad (2)$$

where:
t_{START} is the startup time in s, and
$V_{CC(INT)}$ is the initial voltage of the VCC pin in V.

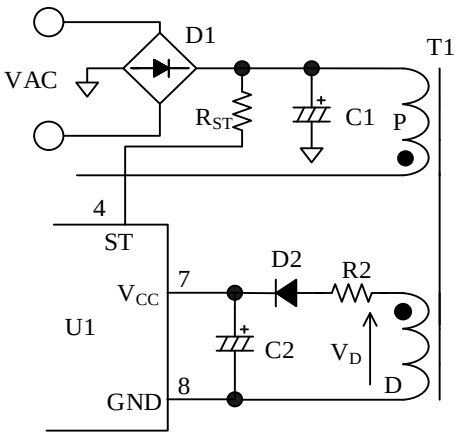

Figure 8-1. VCC Pin Periheral Circuit

8.1.2. Undervoltage Lockout (UVLO) Circuit

Figure 8-2 shows the relationship of V_{CC} and I_{CC}. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.1 V, the control circuit starts operation and the circuit current, I_{CC}, increases. In operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the control circuit stops operation, by the UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

The voltage rectified the auxiliary winding voltage, V_D, in Figure 8-1 becomes a power source to the control circuit after the operation start.

The VCC pin voltage should become as follows within the specification of input voltage range and the output load range of power supply, taking account of the winding turns of the D winging. The target voltage of the VCC pin voltage is about 20 V.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.})$$

$$\rightarrow 12.5\ \text{V} < V_{CC} < 28.5V \quad (3)$$

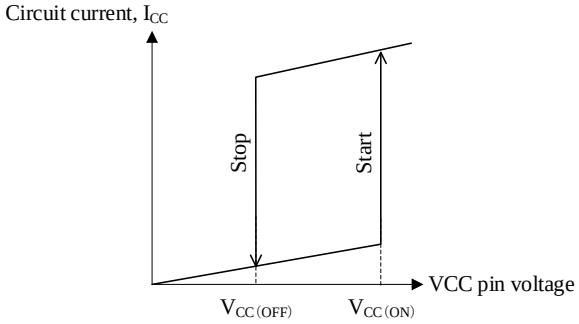

Figure 8-2. VCC vs. I_{CC}

8.1.3. Bias Assist Function

Figure 8-3 shows the VCC pin voltage behavior during the startup period. When the VCC pin voltage reaches $V_{CC(ON)}$ = 15.1 V, the control circuit starts operation, the circuit current, I_{CC}, increases, and thus the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping by the increase of I_{CC} and rising by the increase of the auxiliary winding voltage, V_D.

Just at the turning-off of the power MOSFET, a surge voltage occurs at the output winding. If the feedback control is activated by the surge voltage under light load condition at startup, and the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, a startup failure can occur, because the output power is restricted and the output voltage decreases. In order to prevent this, during a state of operating feedback control (that is, the FB/OLP pin voltage is $V_{FB(STBOP)}$ = 0.8 V or less), when the VCC pin voltage falls to the Startup Current Supply Threshold Voltage, $V_{CC(BIAS)}$ = 11.0 V, the bias assist function is activated. While the bias assist function is operating, the

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decrease of the VCC pin voltage is suppressed by providing the startup current, $I_{CC(STARTUP)}$, from the Startup circuit. By the bias assist function, the use of a small value C2 capacitor is allowed, resulting in shortening startup time. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the overvoltage protection can also be shortened. It is required to check and adjust the process so that poor starting conditions may be avoided.

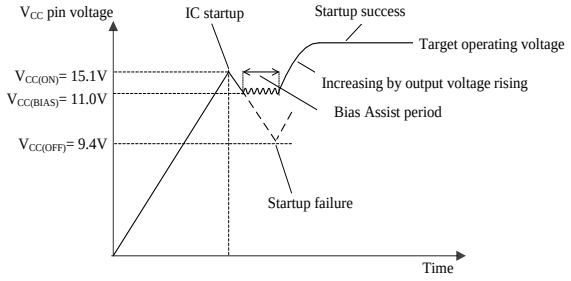

Figure 8-3. V_{CC} during Startup Period

8.1.4. Auxiliary Winding

In actual switch-mode power supply (SMPS) circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output of the SMPS (see Figure 8-4), and the Overvoltage Protection (OVP) on VCC pin may be activated.

This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C2 peak charging, it is effective to add some value R2, of about 2.2 Ω to 82 Ω, in series with D2 (see Figure 8-5). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

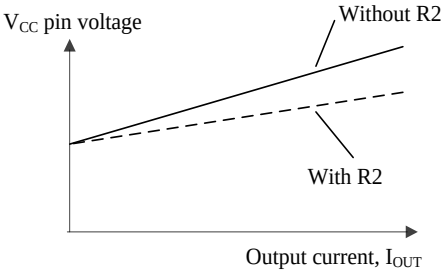

Figure 8-4. V_{CC} versus I_{OUT} with/without resistor R2

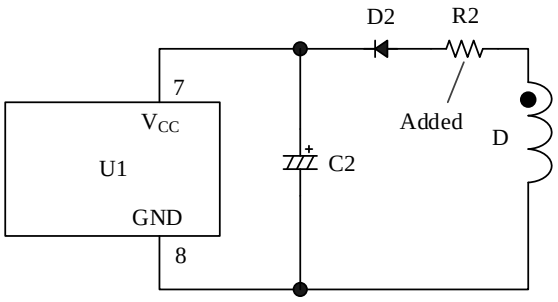

Figure 8-5. VCC pin peripheral circuit with R2

The variation of VCC pin voltage becomes worse if:

- The coupling between the primary and secondary windings of the transformer gets worse and the surge voltage increases (low output voltage, large current load specification, for example).
- The coupling of the auxiliary winding, D, and the secondary side stabilization output winding (winding of the output line which is controlling constant voltage) gets worse and it is subject to surge voltage.

In order to reduce the influence of surge voltages on the VCC pin, alternative structures of the auxiliary winding, D, can be used as examples of transformer structural designs see Figure 8-6.

- Winding structural example (a)

- Separating the auxiliary winding D from the primary side windings P1 and P2.
- The primary side winding is divided into two windings, P1 and P2.

- Winding structural example (b)

- Placing the auxiliary winding D within the secondary winding S1 in order to improve the coupling of those windings.
- The output winding S1 is a stabilized output winding controlled to constant voltage.

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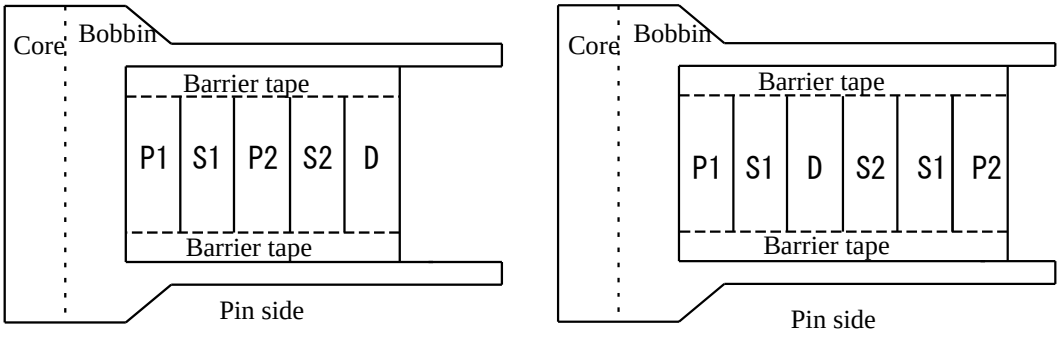

Winding Structure Example (a)

Winding Structure Example (B)

P1, P2: Primary winding
S1: Secondary winding of which the output voltage is controlled constant
S2: Secondary winding
D: Auxiliary winding for VCC

Figure 8-6. Winding Structure Example

8.1.5. Soft-Start Function

Figure 8-7 shows the behavior of VCC pin voltage and the drain current during the startup period.

The IC activates the soft-start function during the startup period. The soft-start operation period, t_{SS}, is internally set to 6.05 ms, and the overcurrent protection (OCP) threshold voltage steps up in four steps during this period. This reduces the voltage and current stress on the power MOSFET and on the secondary-side rectifier. During the soft-start operation period, the operation is in PWM operation with PWM operation frequency of f_{OSC} = 21.0 kHz. In addition, because the soft-start operation period is fixed internally, it is necessary to confirm and adjust the VCC pin voltage and the overload protection (OLP) delay time during startup, based on actual operation in the application.

8.1.6. Operational Mode at Startup

As shown in Figure 8-7 because the auxiliary winding voltage is low at startup, there is a certain period when the quasi-resonant signal has not yet reached a regulated level (Quasi-Resonant Operation Threshold Voltage 1, $V_{BD(TH1)}$, is 0.24 V or more, and the effective pulse width for the quasi-resonant signal is 1.0µs or more). During this period, the operation is in PWM operation with PWM operation frequency of f_{OSC} = 21.0 kHz. Then, when the output voltage rises, the auxiliary winding voltage will rise, and when a quasi-resonant signal reaches the regulated level, quasi-resonant operation will begin. In addition, during the soft-start operation period, t_{SS}, the operation is in PWM operation, even if the quasi-resonant signal reaches the regulated level.

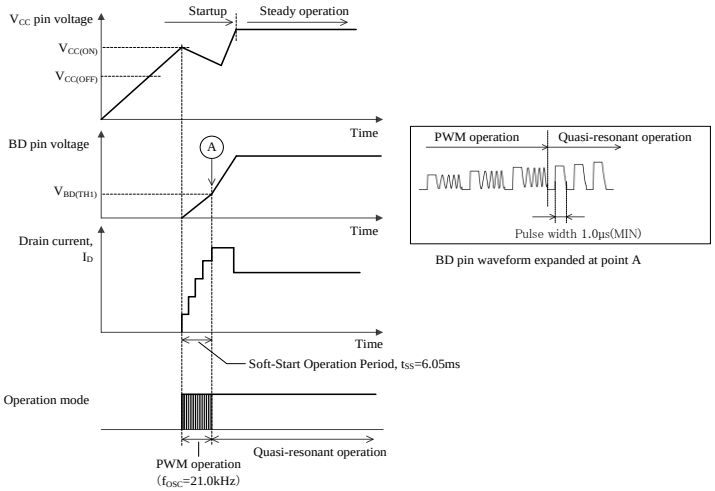

Figure 8-7. Operational Mode in Startup

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8.2. Constant Voltage Control Operation

The constant output voltage control function uses the current mode control (peak current mode), which enhances response speed and provides stable operation.

This IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}. V_{SC} is internally generated from the FB/OLP pin voltage (see Figure 8-8 and Figure 8-9).

- **Light Load Conditions**

When load conditions become lighter, the output voltage, V_{OUT}, rises, and the feedback current from the error amplifier on the secondary side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases and the peak value of V_{ROCP} are controlled to be low, and the peak drain current of I_D decreases. This control prevents the output voltage from increasing.

- **Heavy Load Conditions**

When load conditions become greater, the control circuit performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases. This control prevents the output voltage from decreasing.

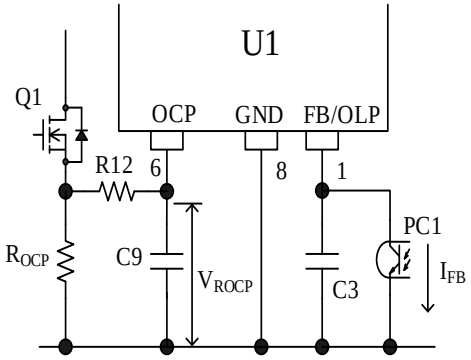

Figure 8-8. FB/OLP Peripheral Circuit

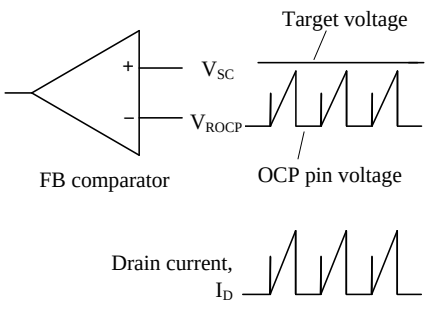

Figure 8-9. Drain Current, I_D, and FB Comparator Operation in Normal Operation

In the current-mode control method, the FB comparator and/or the OCP comparator may respond to the surge voltage resulting from the drain surge current in turning-on the power MOSFET, and may turn off the power MOSFET irregularly. Leading Edge Blanking, t_{BW} = 495 ns, is built-in to prevent these comparators from malfunction caused by the surge voltage resulting from turning-on the power MOSFET.

As shown in Figure 8-10, when the power MOSFET turns on, if the drain current surge pulse width is large, the following adjustments are required so that the surge pulse width falls within t_{BW}.

- For the PCB trace layout of the current detection resistor, R_{OCP}, See Section 9.5.
- Match the turn-on timing to a V_{DS} bottom point.
- Lower the value of the voltage resonant capacitor, C_V, and the value of the capacitor in the secondary side snubber circuit.
- Add a CR filter with R12 and C9 to the OCP pin as shown in Figure 8-8.
  The CR filter should be determined according to the surge voltage level. It is necessary to check and adjust the CR filter values because they change the OCP detection level and the load condition switched to burst oscillation mode at standby.
  When the CR filter is unnecessary, make R12 short and C9 open.
  When it is added, the target value of R12 is 100 to 330Ω, and that of C9 is 470pF to 680pF.

$V_{OCP(H)}'$ of Figure 8-10 is the overcurrent detection threshold voltage after input compensation in Section 8.8.

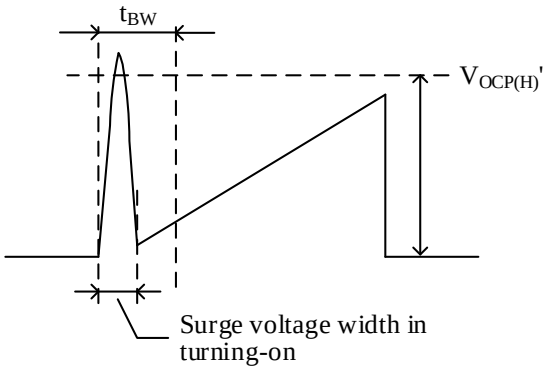

Figure 8-10. OCP Pin Voltage Waveform

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8.3. Quasi-Resonant Operation and Bottom-On Timing

8.3.1. Quasi-Resonant Operation

Figure 8-11 shows the circuit of a flyback converter. A flyback converter is a system which transfers the energy stored in the transformer to the secondary side when the primary side power MOSFET is turned off. After the energy is completely transferred to the secondary, when the MOSFET keeps turning off, the MOSFET drain node begins free oscillation based on the L_P of the transformer and C_V across the drain and source pins. The quasi-resonant operation is the V_{DS} bottom-on operation that turns-on the MOSFET at the bottom point of V_{DS} free oscillation. Figure 8-12 shows an ideal V_{DS} waveform during bottom-on operation. Using bottom-on operation, switching loss and switching noise are reduced and it is possible to obtain converters with high efficiency and low noise. This IC performs bottom-on operation not only during normal quasi-resonant operation, but also during bottom-skip quasi-resonant operation. This allows reduction of the operation frequency during light load conditions, to improve efficiency across the full range of loads.

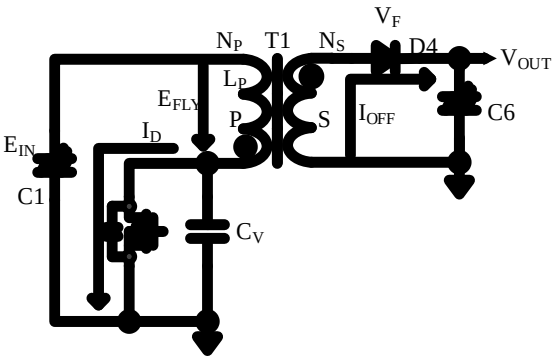

Figure 8-11. Basic Flyback Converter Circuit

In Figure 8-11, symbols means as follows:

E_{IN} is input voltage,

E_{FLY} is flyback voltage,

$$E_{FLY} = \frac{N_P}{N_S} \times (V_{OUT} + V_F),$$

N_P is primary side number of turns,

N_S is secondary side number of turns,

V_{OUT} is output voltage,

V_F is forward voltage drop of the secondary side rectifier,

I_D is drain current of power MOSFET,

I_{OFF} is secondary side rectifier flowing current while the power MOSFET is off,

C_V is voltage resonant capacitor, and

L_P is primary side inductance.

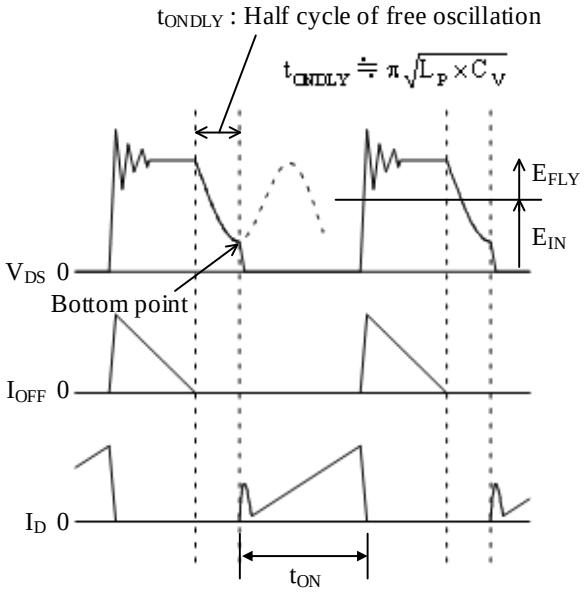

Figure 8-12. Ideal bottom-on operation waveform (Power MOSFET turn-on at a bottom point of a V_{DS} waveform)

8.3.2. Bottom-On Timing

Figure 8-13 shows the voltage waveform of the BD pin peripheral circuit and auxiliary winding, D.

The following setup is required with the BD pin.

- Bottom-on timing setup (described here, below)
- OCP input compensation value setup (see Section 8.8)

The components DZ_{BD}, R_{BD1}, R_{BD2}, and C_{BD}, are connected to the BD pin peripheral circuit as shown in Figure 8-13, with values that are determined with the above-mentioned steps 1) and 2).

This delay time, t_{ONDLY}, for bottom-on, from the start of V_{DS} free oscillation to the timing of turning-on the power MOSFET, is created by exploiting the auxiliary winding voltage, which synchronizes to the drain voltage V_{DS} waveform.

The voltage on either end of R_{BD1} and R_{BD2} is the voltage subtracted the forward voltage drop, V_F, of DZ_{BD} from the flyback voltage, E_{rev1}, of the auxiliary winding, D. The quasi-resonant signal, E_{rev2}, on the BD pin, is the voltage divided the former voltage by R_{BD1} and R_{BD2}. The delay time, t_{ONDLY}, is adjusted by E_{rev2} and C_{BD}.

After the power MOSFET turns off, while the quasi-resonant signal increases to the Quasi-Resonant Operation Threshold Voltage 1, $V_{BD(TH1)}$ = 0.24 V, the power MOSFET remains off. After that, when E_{rev2} decreases enough to cross the Quasi-Resonant Operation Threshold Voltage 2, $V_{BD(TH2)}$ = 0.17 V, the power MOSFET turns on again.

In addition, at this point, the threshold voltage

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automatically increases to $V_{BD(TH1)}$ to prevent malfunction of the quasi-resonant operation from noise interference.

- **R_{BD1} and R_{BD2} Setup**

R_{BD1} and R_{BD2} must set the range for the quasi-resonant signal, $V_{BD(TH1)}$ = 0.34 V(max.) or more under input and output conditions where V_{CC} becomes lowest, but less than the absolute maximum rating of the BD pin, 6.0 V, under conditions where V_{CC} becomes highest. The target voltage of E_{rev2} is about 3.0 V, and the effective pulse width must be 1.0 µs or more between the two points $V_{BD(TH1)}$ = 0.34 V (max.) and $V_{BD(TH2)}$ = 0.27 V (max.)

- **C_{BD} Setup**

The delay time, t_{ONDLY}, after which the power MOSFET turns on, is adjusted by the value of C_{BD}, so that the power MOSFET turns on at the bottom-on of V_{DS} as shown in Figure 8-12, while the power MOSFET drain voltage, V_{DS}, the drain current, I_D, and the quasi-resonant signal, under the maximum input voltage and the maximum output power. An initial reference value for C_{BD} is about 1000pF.

The following show how to adjust the turn-on point:

- If the turn-on point precedes the bottom of the V_{DS} signal (see Figure 8-14), it causes higher switching losses. In that situation, after confirming the initial turn-on point, delay the turn-on point by increasing the C_{BD} value gradually, so that the turn-on will match the bottom point of V_{DS}.
- In the converse situation, if the turn-on point lags behind the V_{DS} bottom point (see Figure 8-15), it causes higher switching losses also. After confirming the initial turn-on point, advance the turn-on point by decreasing the C_{BD} value gradually, so that the turn-on will match the bottom point of V_{DS}.

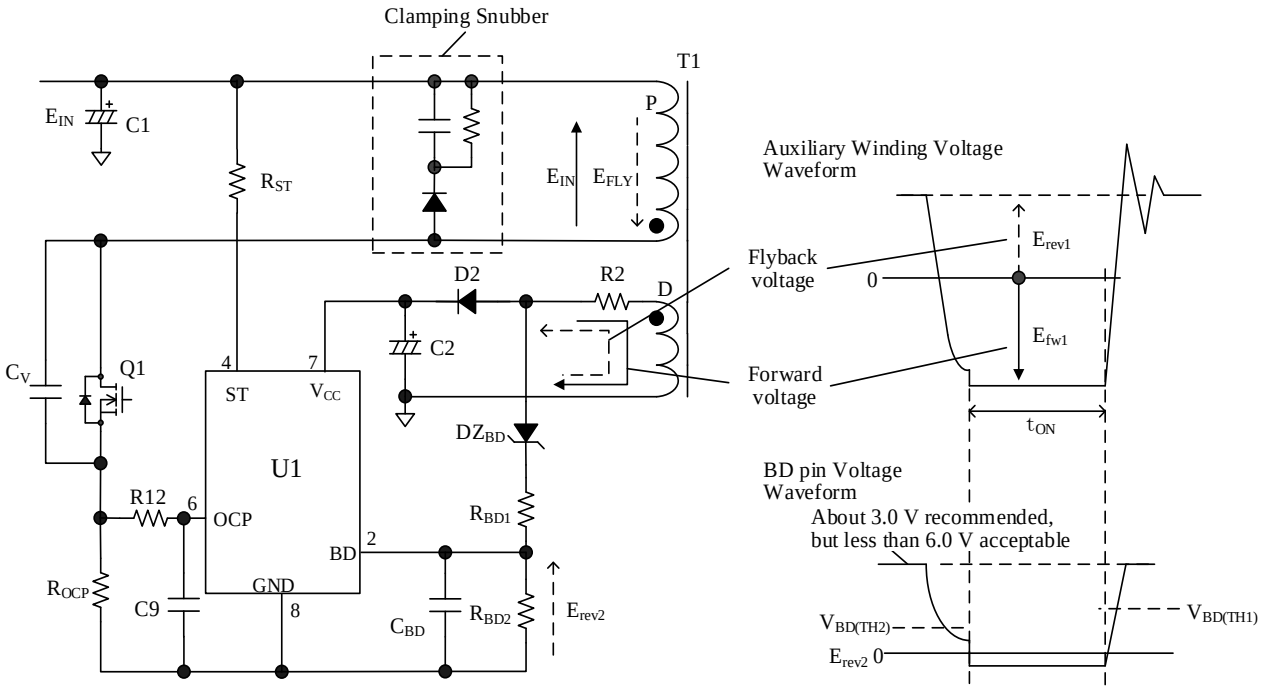

Figure 8-13. BD Pin Peripheral Circuit (Left) and Auxiliary Winding Voltage (Right)

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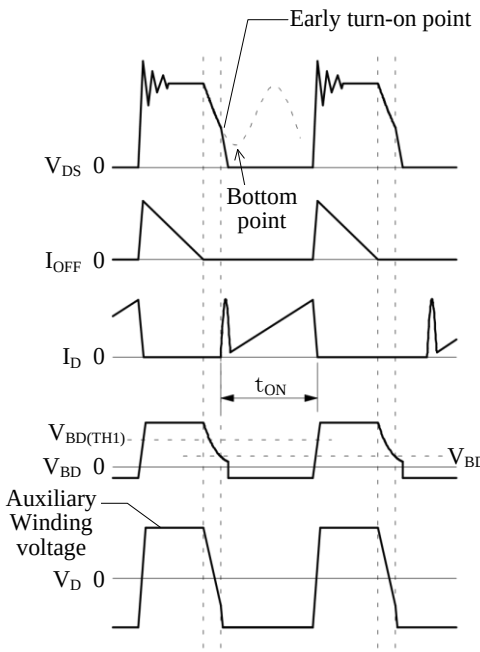

Figure 8-14. When the Turn-on of a V_{DS} Waveform Occurs before a Bottom Point

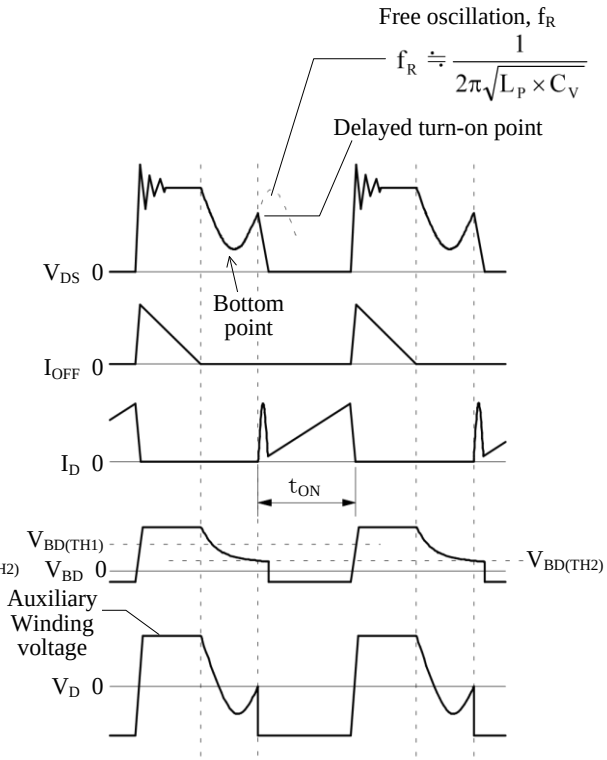

Figure 8-15. When the Turn-on of a V_{DS} Waveform Occurs after a Bottom Point

8.3.3. BD Pin Blanking Time

Figure 8-16 shows two different BD pin waveforms, comparing transformer coupling conditions between the primary and secondary winding. The poor coupling tends to happen in a low output voltage transformer design with high N_P/N_S turns ratio (N_P and N_S indicate the number of turns of the primary winding and secondary winding, respectively), and it results in high leakage inductance. The poor coupling causes high surge voltage ringing at the power MOSFET drain pin when it turns off. That high surge voltage ringing is coupled to the auxiliary winding and then the inappropriate quasi-resonant signal occurs.

The BD pin has a blanking period of 250ns(max.) to avoid the IC reacting to it, but if the surge voltage period continues that value or more, the IC responds to it and repeatedly turns the power MOSFET on and off at high frequency. This result in an increase of the MOSFET power dissipation and temperature, and the power MOSFET can be damaged.

The following adjustments are required when such high frequency operation occurs.

- C_{BD} must be connected near the BD pin and the GND pin.
- The circuit trace loop between the BD pin and the GND pin must be separated from any traces carrying high current.
- The coupling of the primary winding and the auxiliary winding must be good.
- The clamping snubber circuit (see Figure 8-13) must be adjusted properly.

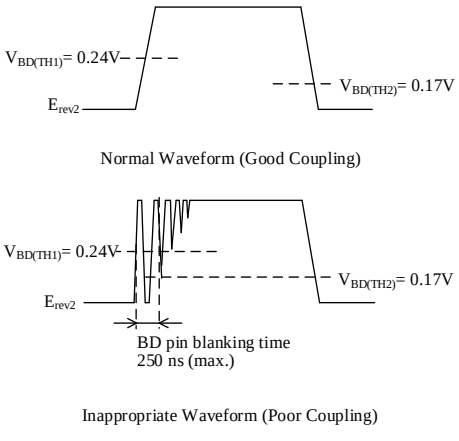

Figure 8-16. The Difference of BD Pin Voltage Waveform by the Coupling Condition of the Transformer; Good Coupling Versus Inappropriate Coupling

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8.3.4. Bottom Skip Quasi-Resonant Operation

In order to reduce switching losses during light to medium load conditions, in addition to quasi-resonant operation, the bottom skip function is built in, to limit the rise of the power MOSFET operation frequency. This function monitors the power MOSFET drain current (in fact, the OCP pin voltage), it automatically changes to normal quasi-resonant operation during heavy load conditions, and it also changes to bottom skip quasi-resonant operation during light to medium loads.

Figure 8-17 shows the operation state transition diagram of the output load from light load to heavy load. Figure 8-18 shows that from heavy load to light load. As these are state change diagrams without input compensation of OCP, the overcurrent detection threshold voltage shows just a $V_{OCP(H)}$ = 0.910 V.

This IC has a built-in automatic multi-mode control which changes among the following three operational modes according to the output loading state: auto standby mode, one bottom-skip quasi-resonant operation, and normal quasi-resonant operation.

- The mode is changed from one bottom-skip quasi-resonant operation to normal quasi-resonant operation (Figure 8-17), when load is increased from one bottom-skip operation, the MOSFET peak drain current value increases, the on-time widens, and thus the peak value of the OCP pin voltage increases.
  When the load is increased further and the OCP pin voltage increases to $V_{OCP(BS1)}$, the mode is changed to normal quasi-resonant operation.
- The mode is changed from normal quasi-resonant operation to one bottom-skip quasi-resonant operation (Figure 8-18), when load is reduced from normal quasi-resonant operation, the MOSFET peak drain current value decreases, the on-time shortens, and thus the peak value of the OCP pin voltage decreases.
  When the load is reduced further and the OCP pin voltage decreases to $V_{OCP(BS2)}$, the mode is changed to one bottom-skip quasi-resonant operation. This suppresses the rise of the operation frequency.

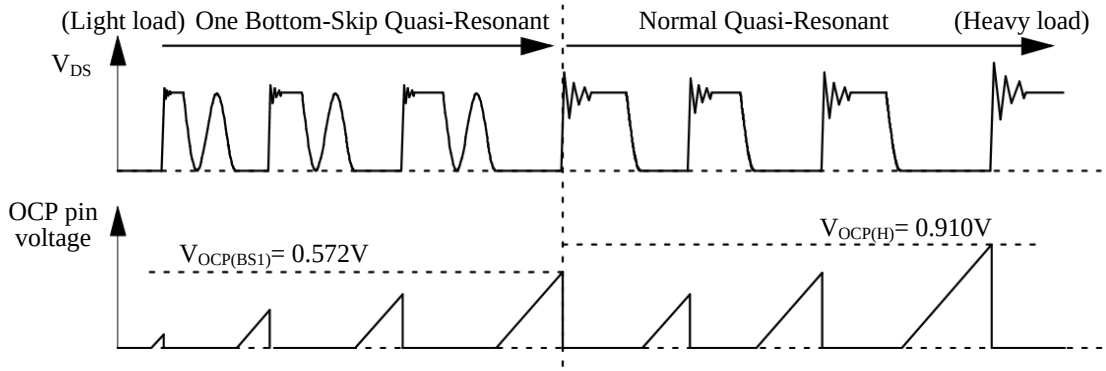

Figure 8-17. Operation State Transition Diagram from Light Load to Heavy Load Conditions

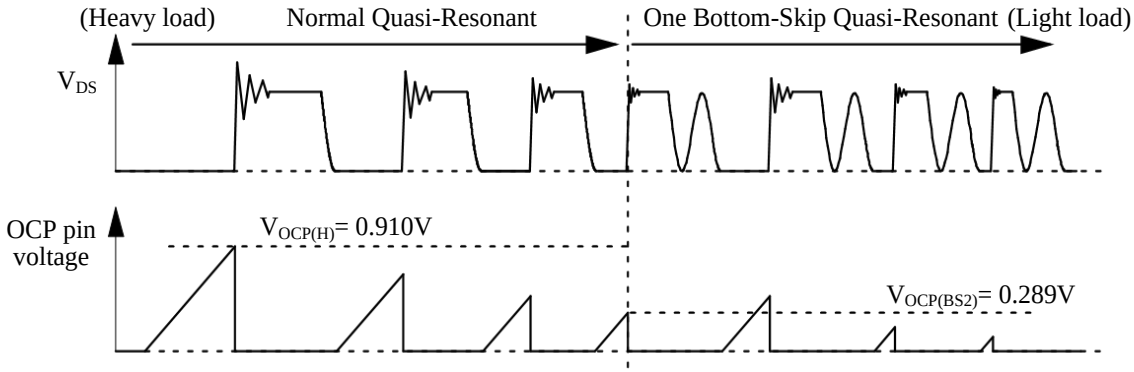

Figure 8-18. Operation State Transition Diagram from Heavy Load to Light Load Conditions

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As shown in Figure 8-19, in the process of the increase and decrease of load current, hysteresis is imposed at the time of each operational mode change. For this reason, the switching waveform does not become unstable near the threshold voltage of a change, and this enables the IC to switch in a stable operation.

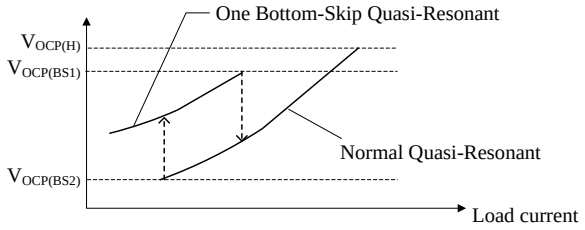
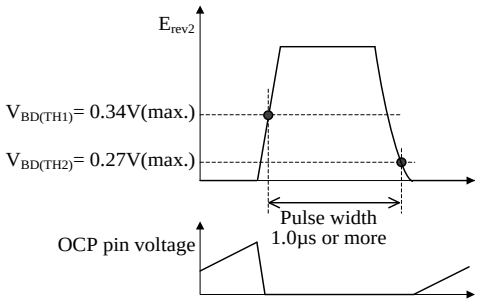
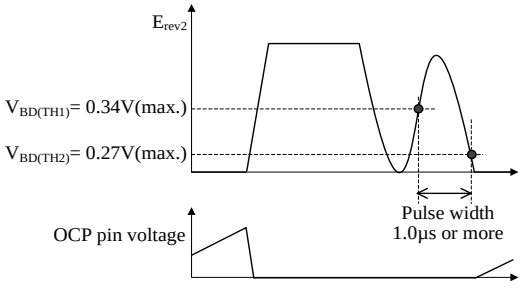


Figure 8-19. Hysteresis at the Time of an Operational Mode Change

Figure 8-20 shows the effective pulse width of quasi-resonant signal waveform under light load condition. In order to perform stable normal quasi-resonant operation and one bottom-skip operation, it is necessary to ensure that the pulse width of the quasi-resonant signal is 1.0 µs or more under the conditions of minimum input voltage and minimum output power. The pulse width of the quasi-resonant signal, E_{rev2}, is defined as the interval between $V_{BD(TH1)}$ = 0.34 V(max.) on the rising edge, and $V_{BD(TH2)}$ = 0.27 V(max.) on the falling edge of the pulse.



(a) Normal Quasi-Resonant Operation



(b) One Bottom-Skip Quasi-Resonant Operation

Figure 8-20. Effective Pulse Width of a Quasi-Resonant Signal

8.4. Auto Standby Function

The auto standby function automatically changes the IC operation mode to standby mode with burst oscillation, when the MOSFET drain current, I_D, decreases during light loads.

The OCP pin circuit monitors I_D. When the OCP pin voltage decreases to the standby state threshold voltage (about 9% compared to $V_{OCP(H)}$ = 0.910 V), the auto standby function changes switching mode to standby mode (see Figure 8-21).

The burst oscillation mode is controlled, so that when the FB/OLP pin voltage decreases to $V_{FB(STBOP)}$, the IC stops switching operation, and when it increases to that value or more, the IC starts switching operation. Because the burst oscillation mode has a certain interval of off-time, switching losses are reduced and efficiency is improved under light load conditions.

Generally, a burst interval is set to several kilohertz or less, in order to improve the efficiency during light loads. In this low frequency, audible noise may occur from the transformer. However, this IC keeps the peak drain current low during burst oscillation mode, and suppresses the audible noise of the transformer further by enabling the step-on burst oscillation function, which expands the pulse width gradually.

During the transition stage to burst oscillation mode, if the VCC pin voltage decreases to the Startup Current Supply Threshold Voltage, $V_{CC(BIAS)}$ = 11.0 V, the bias assist function is activated. Because this function provides the startup current, $I_{CC(STARTUP)}$ to the VCC pin, in order to prevent the fall of the VCC pin voltage, it enables stable standby operation. If the bias assist function operates during normal operation (which includes burst oscillation mode periods), the power consumption of the IC increases. Therefore, in order to always keep the VCC pin voltage more than $V_{CC(BIAS)}$, it is necessary to adjust the turn ratio between the auxiliary winding and secondary winding of the transformer, and/or minimize the value of R2 shown in Figure 8-5.

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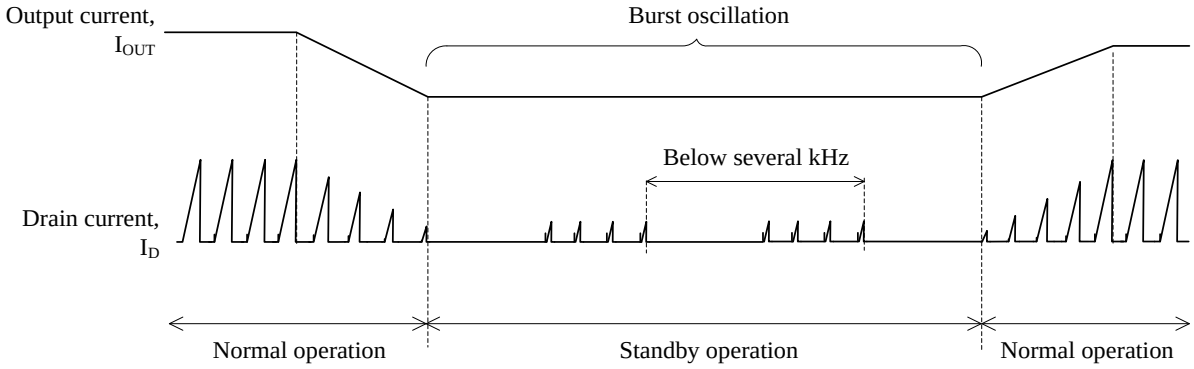

Figure 8-21. Auto Standby Mode Timing

8.5. Overvoltage Protection (OVP)

When the voltage between the VCC pin and GND pin increases to the OVP Operation Threshold Voltage, $V_{CC(OVP)}$ = 31.5 V, the overvoltage protection (OVP) is activated, and switching operation is stopped. The IC has two operation types of the OVP. One is the auto restart. The other is latched shutdown.

When the auxiliary winding supplies the VCC pin voltage, the VCC pin voltage is proportional to the output voltage. Thus, an excessive output voltage of the secondary side when the output control circuit is open can be detected by the OVP.

The output voltage of the secondary side at the OVP activation, $V_{OUT(OVP)}$, is calculated approximately as follows:

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 31.5 \text{ (V)} \quad (4)$$

Where, $V_{OUT(NORMAL)}$ is output voltage in normal operation, and $V_{CC(NORMAL)}$ is VCC pin voltage in normal operation

- **Auto-restart Type: SSC1S311A**

When the OVP is activated, the IC stops switching operation. The VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, because the bias assist function is disabled during the OVP operation. Then, the control circuit stops operation by the UVLO (undervoltage lockout) circuit, and the IC reverts to the state before startup. When the VCC pin voltage is increased to $V_{CC(ON)}$ = 15.1 V by the startup current, the control circuit returns to normal operation again. In this way, the intermittent oscillation is repeated by the UVLO circuit during the excess voltage condition. The intermittent oscillation reduces the stresses of a component such as the power MOSFET and the secondary rectifier diode. Also, power consumption in the intermittent operation is minimized because switching period is shorter than oscillation stop period. When the fault condition is removed, the IC returns to normal operation automatically.

- **Latched Shutdown Type: SSC1S312A**

When the OVP is activated, the IC stops switching operation in the latched state. For keeping the latched state, the bias assist function is activated when VCC pin voltage decreases to $V_{CC(BIAS)}$. As a result, the VCC pin voltage is kept to over the $V_{CC(OFF)}$. Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

8.6. Overload Protection (OLP)

Figure 8-22 shows the FB/OLP pin peripheral circuit.

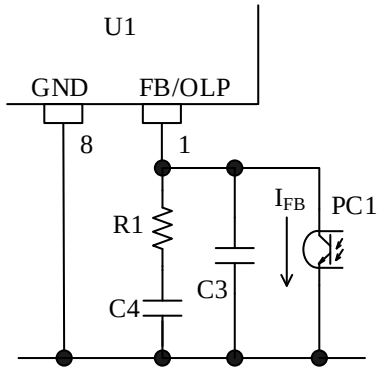

Figure 8-22. FB/OLP Pin Peripheral Circuit

When the drain peak current is limited by the OCP operation, the output voltage, V_{OUT}, decreases, and then the feedback current from the secondary photo-coupler, I_{FB}, becomes zero. As a result, the capacitor, C4, is charged, and the FB/OLP pin voltage increases. When

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the FB/OLP pin voltage increase to $V_{FB(MAX)}$ = 4.05 V, the capacitor C4 is charged by $I_{FB(OLP)}$ = −10 µA. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 5.96 V, the overload protection (OLP) is activated, and switching operation is stopped.

The time of the FB/OLP pin voltage from $V_{FB(MAX)}$ = 4.05 V to $V_{FB(OLP)}$ = 5.96 V is defined as the OLP Delay Time, t_{DLY}. Because the capacitor C3 for phase compensation is small compared to C4, the approximate value of t_{DLY} is determined as follows:

$$t_{DLY} \approx \frac{V_{FB(OLP)} - V_{FB(MAX)}}{\left|I_{FB(OLP)}\right|} \times C4 \quad (5)$$

If $V_{FB(OLP)}$ = 5.96 V, $V_{FB(MAX)}$ = 4.05 V, $I_{FB(OLP)}$ = −10µA, and C4 = 4.7µF, the value of t_{DLY} is approximately 0.9s. The recommended value of R1 is 47 kΩ.

The IC has two operation types of the OLP. One is the auto restart. The other is latched shutdown.

- **Auto-restart Type: SSC1S311A**

Figure 8-23 shows the auto-restart OLP operation waveforms. When the OLP is activated, the switching operation is stopped, and the bias assist function is disabled. Then an intermittent oscillation is repeated by the UVLO circuit (for more details, see Section 8.5). When the fault condition is removed, the IC returns to normal operation automatically.

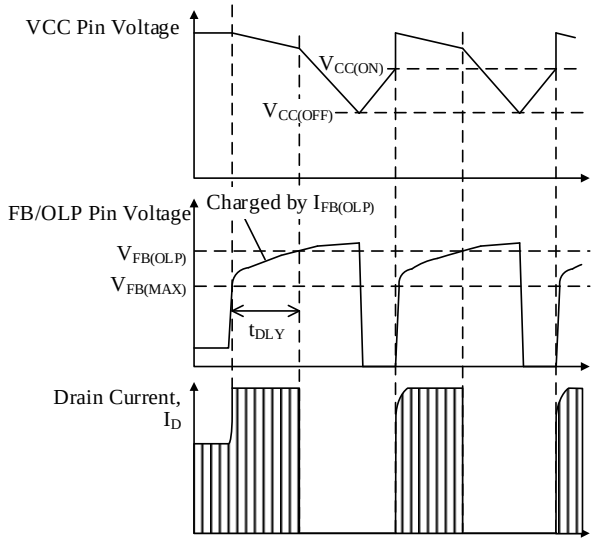

Figure 8-23. Auto-restart Type OLP Operation Waveforms

- **Latched Shutdown Type: SSC1S312A**

Figure 8-24 shows the auto-restart OLP operation waveforms. When the OLP is activated, the IC stops switching operation in the latched state. For keeping the latched state, the bias assist function is activated when VCC pin voltage decreases to $V_{CC(BIAS)}$. As a result, the VCC pin voltage is kept to over the $V_{CC(OFF)}$.

Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

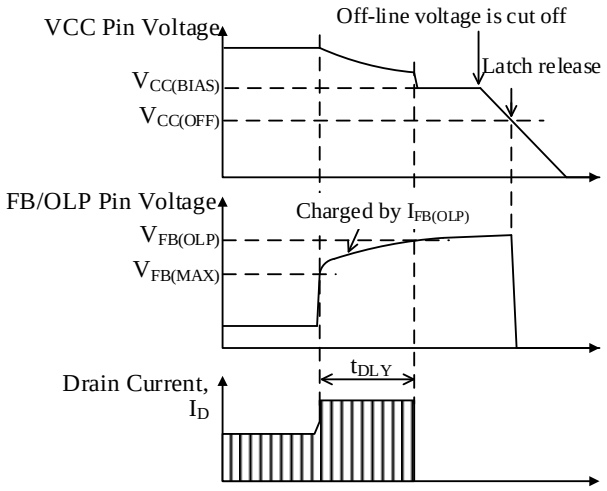

Figure 8-24. Latched Shutdown Type OLP Operation Waveforms

8.7. Thermal Shutdown (TSD)

If the temperature of the IC reaches more than the Thermal Shutdown Temperature $T_{j(TSD)}$ = 135°C(min.), the Thermal Shutdown (TSD) is activated, and the IC stops switching operation.

The IC has two operation types of the TSD. One is the auto restart. The other is latched shutdown.

- **Auto-restart Type: SSC1S311A**

When the OLP is activated, the switching operation is stopped, and the bias assist function is disabled. Then an intermittent oscillation is repeated by the UVLO circuit (for more details, see Section 8.5). When the fault condition is removed and the temperature of the internal control circuit is decreases to $T_{j(TSD)}$ or less, the IC returns to normal operation automatically.

- **Latched Shutdown Type: SSC1S312A**

When the TSD is activated, the IC stops switching operation in the latched state. For keeping the latched state, the bias assist function is activated when VCC pin voltage decreases to $V_{CC(BIAS)}$. As a result, the VCC pin voltage is kept to over the $V_{CC(OFF)}$.

Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

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8.8. Overcurrent Protection (OCP)

The overcurrent protection circuit (OCP) detects each peak drain current of the power MOSFET on pulse-by-pulse basis, by the current detection resistor, R_{OCP}. When the OCP pin voltage reaches the OCP threshold, the IC turns off the power MOSFET and limits the output power.

8.8.1. Overcurrent Input Compensation Function

When using a quasi-resonant converter with universal input (85 to 265 VAC), if the output power is set constant, then because higher input voltages have higher frequency, the MOSFET peak drain current becomes low. Because R_{OCP} is fixed, the OCP point in the higher input voltage will shift further into the overload area. Thus, the output current at OCP point in the maximum input voltage, $I_{OUT(OCP)}$, approximately doubles relative to that in the minimum input voltage (see the curve of I_{OUT} without input compensation of Figure 8-25). In order to suppress this phenomenon, this IC has the overcurrent input compensation function. As for determining an input compensation value, it is necessary to avoid excessive input compensation for the output current specification, I_{OUT}. When excessive input compensation is applied, $I_{OUT(OCP)}$ may be below I_{OUT} in the situation where the input voltage is high. Therefore, it is necessary to ensure that $I_{OUT(OCP)}$ remains more than I_{OUT} across the full range of input voltage, such as the curve of I_{OUT} with appropriate input compensation in Figure 8-25.

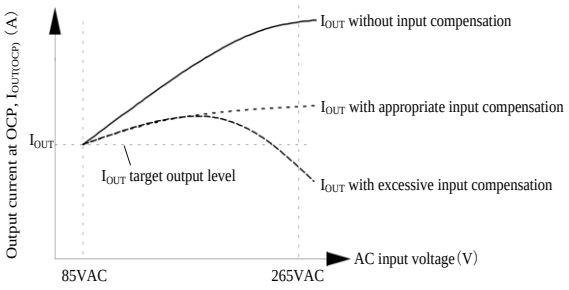

Figure 8-25. OCP Circuit Input Compensation

Figure 8-26 shows an overcurrent input compensation circuit, and Figure 8-27 shows E_{fw1} and E_{fw2} relative to the input voltage. Also, Figure 8-28 shows the relationship between the overcurrent threshold voltages after input compensation, $V_{OCP(H)}'$, and the BD pin voltage, E_{fw2}. The overcurrent input compensation function compensates the overcurrent detection threshold voltage (normal operation), $V_{OCP(H)}$, according to the input voltage. The forward voltage, E_{fw1}, is proportional to the input voltage, the voltage passed through DZ_{BD} from E_{fw1} is biased by either end of R_{BD1} and R_{BD2}, and thus the BD pin voltage is provided the voltage on R_{DB2} divided by the divider of R_{BD1} and R_{BD2}.

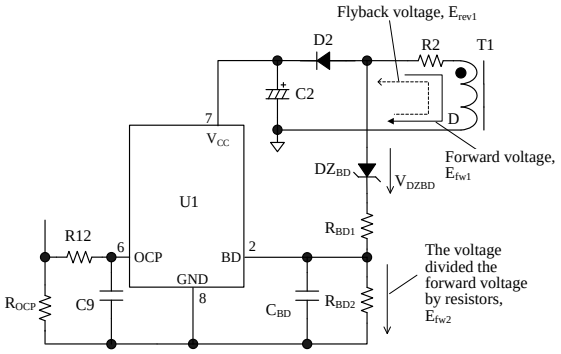

Figure 8-26. Overcurrent Input Compensation Circuit

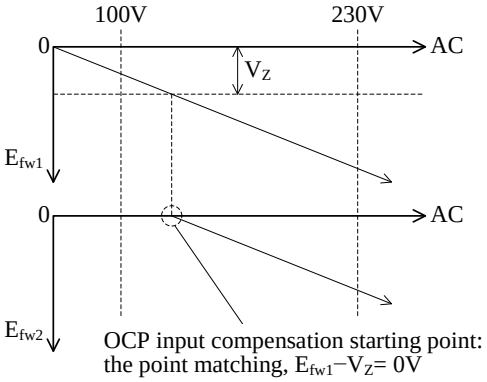

Figure 8-27. E_{fw1} and E_{fw2} Voltage Relative to AC Input Voltage

Figure 8-28 shows the relationship between the overcurrent detection threshold voltage after input voltage compensation, $V_{OCP(H)}'$, and E_{fw2}. Read the value of $V_{OCP(H)}'$ according to E_{fw2} in Figure 8-28.

- DZ_{BD} setting:
  The starting voltage for input compensation is set by the Zener voltage, V_Z, of DZ_{BD}. According to the input voltage specification or transformer specification, it is required to be V_Z = 6.8 to 30 V.
- R_{BD1} setting: see Section 8.3.2
- The recommended value of R_{BD2}: 1.0 kΩ

Overcurrent input compensation should be adjusted so that the variance of the output current, $I_{OUT(OCP)}$, at an OCP point, is minimized at the high and low input voltage. In addition, the input compensation must be adjusted so that $I_{OUT(OCP)}$ remains more than the output current specification, I_{OUT}, across the full range of input voltage, such as the curve of I_{OUT} with appropriate input compensation in Figure 8-25.

If $V_{OCP(H)}'$ is compensated to the Bottom-Skip

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Operation Threshold Voltage, $V_{OCP(BS1)}$, or less, the IC will change from one bottom-skip operation to normal quasi-resonant operation, and thus will raise the operation frequency and will provide output power. Therefore, switching losses in normal quasi-resonant operation is higher than that in bottom-skip operation. In this case, when the input compensation is compensated to $V_{OCP(BS1)}$ or less, the temperature of the power MOSFET should be checked in normal quasi-resonant operation switched from bottom-skip operation, by changing load condition. E_{fw2}, which includes surge voltage, must be within the absolute maximum rating of the BD pin voltage (–6.0 V to 6.0 V) at the maximum input voltage. Figure 8-29 shows each voltage waveform for the input voltage in normal quasi-resonant operation.

- Point A: $V_{DZBD} \geq E_{fw1}$
  E_{fw2} will be produced negative voltage, and the detection voltage for an overcurrent event is the Overcurrent Detection Threshold Voltage (normal operation), $V_{OCP(H)}$.
- Point B to Point D: $V_{DZBD} < E_{fw1}$
  When the input voltage increases and E_{fw1} exceeds the Zener voltage, V_Z, of D_{ZBD}, E_{fw2} will be produced as a negative voltage to compensate the Overcurrent Detection Threshold Voltage (normal operation), $V_{OCP(H)}$.

E_{fw2} is generally adjusted to the BD pin voltage of E_{fw2} = –3.0 V at the maximum input voltage. Adjustment of E_{fw2} will change the overcurrent detection threshold voltage by an overcurrent input compensation function. Therefore, E_{fw2} must be adjusted while checking the input compensation starting point and the amount of input compensation. Also, the variations of the overcurrent detection threshold voltage after input compensation, $V_{OCP(H)}'$, can be calculated by the minimum and maximum values shown in Figure 8-28.

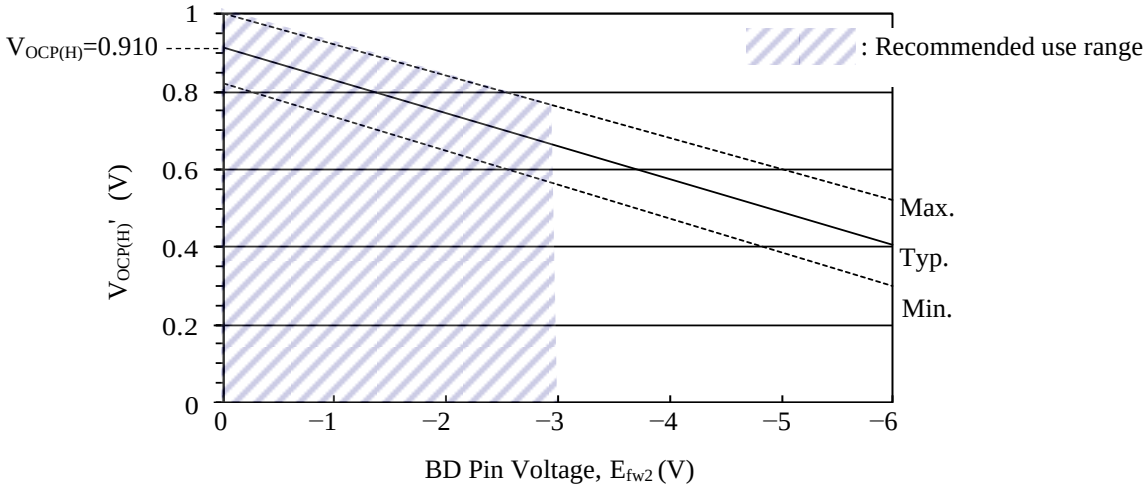

Figure 8-28. Overcurrent Threshold Voltage after Input Compensation, $V_{OCP(H)}'$ (Reference for Design Target Values)

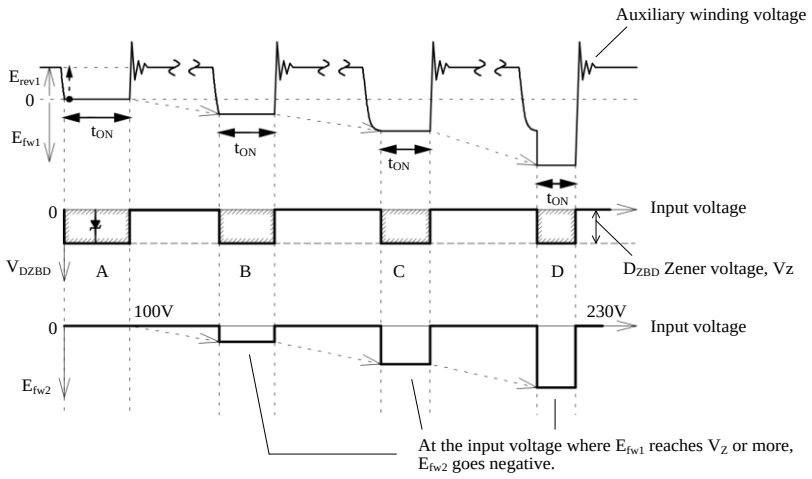

Figure 8-29. Each Voltage Waveform for the Input Voltage in Normal Quasi-Resonant Operation

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8.8.2. Reference BD Pin Peripheral Components Setting

This example demonstrates the determination of external component values for the BD pin peripheral circuit. It assumes universal input (85 VAC to 265 VAC) is being used, and input compensation begins from the input voltage of 120 VAC. The transformer is assumed to have primary winding with N_P = 40T, and an auxiliary winding with N_D = 5 (turn).

To determine the Zener voltage, V_Z, of D_{ZBD}, E_{fw1} at 120 VAC is calculated as follows:

$$E_{fw1} = \frac{N_D}{N_P} \times V_{IN(AC)} \times \sqrt{2} \quad (6)$$

$$= \frac{5\ \text{turn}}{40\ \text{turn}} \times 120\ \text{VAC} \times \sqrt{2} = 21.2\ \text{V}.$$

The Zener diode rating, V_Z, is chosen to be 22 V, a standard value.

R_{BD1} results in E_{fw2} = –3.0 V at the maximum input voltage of 265 VAC, as follows:

$$R_{BD1} = \frac{R_{BD2}}{|E_{fw2}|} \times \left(\frac{N_D}{N_P} \times V_{IN(AC)} \times \sqrt{2} - Z_{BD} - |E_{fw2}| \right) \quad (7)$$

$$= \frac{1\ \text{k}\Omega}{|-3\text{V}|} \times \left(\frac{5\ \text{turn}}{40\ \text{turn}} \times 265\ \text{VAC} \times \sqrt{2} - 22\ \text{V} - |-3\text{V}| \right)$$

$$= 7.28\ \text{k}\Omega\ .$$

The R_{BD1} rating is chosen to be 7.5 kΩ of the E series.

Choosing R_{BD2} = 1.0kΩ, the $|E_{fw2}|$ value at 265 VAC can be calculated as follows:

$$E_{fw2} = \frac{R_{BD2}}{R_{BD1} + R_{BD2}} \times (|E_{fw1}| - Z_{BD}) \quad (8)$$

$$= \frac{1\ \text{k}\Omega}{7.5\ \text{k}\Omega + 1\ \text{k}\Omega} \times \left(\frac{5\ \text{turn}}{40\ \text{turn}} \times 265\ \text{VAC} \times \sqrt{2} - 22\ \text{V} \right)$$

$$= 2.92\ \text{V}.$$

Referring to Figure 8-28, when compensated by E_{fw2} = –2.92 V, the overcurrent threshold voltage after input compensation, $V_{OCP(H)}'$, is set to about 0.66 V (typ.).

When R_{BD2} = 1 kΩ, R_{BD1} = 7.5 kΩ, V_F = 0.7 V, and E_{rev1} = 20 V, E_{rev2} of Figure 8-13 can be calculated as follows:

$$E_{fw2} = \frac{R_{BD2}}{R_{BD1} + R_{BD2}} \times (E_{rev1} - V_F) \quad (9)$$

$$= \frac{1\ \text{k}\Omega}{7.5\ \text{k}\Omega + 1\ \text{k}\Omega} \times (20\ \text{V} - 0.7\ \text{V}) = 2.27\ \text{V}.$$

In this case, the quasi-resonant voltage E_{rev2} meets the design guidelines: it is Quasi-Resonant Operation Threshold Voltage 1, $V_{BD(TH1)}$ = 0.24 V or more, and E_{fw2} and E_{rev2} are kept within the limits of the Absolute Maximum Rating (–6.0 V to 6.0 V) of the BD pin.

8.8.3. Reference Example of No Overcurrent Input Compensation Required

When the input voltage is narrow range, or provided from a pre-regulator such as PFC of active filter, the variation of the input voltage is small. Thus, the variation of OCP point may become less than that of the universal input voltage specification. When overcurrent input compensation is not required, the input compensation function can be disabled by substituting a high-speed diode for the Zener diode (DZ_{BD}), and by keeping the BD pin voltage from being negative voltage.

In addition, the following formula shows the reverse voltage of a high-speed diode. The high-speed selection should take account of its derating.

$$E_{fw1} = \frac{N_D}{N_P} \times \text{Maximum input voltage} \quad (10)$$

8.9. Maximum On-Time Limitation Function

When the input voltage is low or in a transient state such that the input voltage turns on or off, the on-time of the power MOSFET is limited to the Maximum On-Time, $t_{ON(MAX)}$ = 40.0 µs (see Figure 8-30). Thus, the peak drain current is limited, and the audible noise of the transformer is suppressed.

In designing a power supply, the on-time must be less than $t_{ON(MAX)}$. If such a transformer is used that the on-time is $t_{ON(MAX)}$) or more, under the condition with the minimum input voltage and the maximum output power, the output power would become low. In that case, the transformer should be redesigned taking into consideration the following:

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- Inductance, L_P, of the transformer should be lowered in order to raise the operation frequency.
- Lower the primary and the secondary turns ratio, N_P/N_S, to lower the duty cycle.

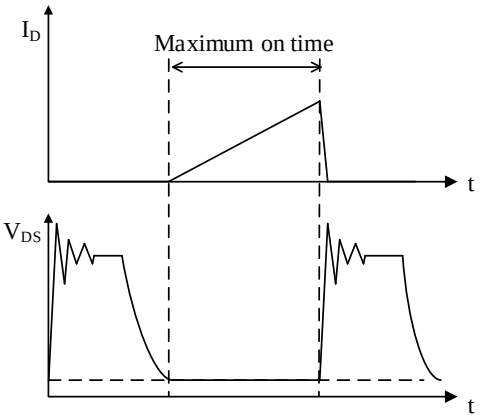

Figure 8-30. Confirmation of Maximum On-time

8.10. DRV Pin Peripheral Components

Figure 8-31 shows the peripheral circuit around DRV pin. The DRV pin is the gate drive pin for driving the external power MOSFET. The output voltage, V_{DRV}, is 7.5 V (min.), the peak source current and peak sink current are −150 mA and 608 mA, respectively. It is necessary to choose the external power MOSFET of which the gate threshold voltage, $V_{GS(th)}$ is less than V_{DRV} enough across the full temperature range in the application.

R4, R5, and D3 should be adjusted considering power losses of the power MOSFET, gate waveform (reduction of ringing caused by pattern layout, and others), and EMI noise, based on actual operation in the application.

R3 prevents malfunctions caused by steep dv/dt at turning off the power MOSFET. It is recommended to place a resistor of 10kΩ to 100kΩ close to Gate and Source of the power MOSFET.

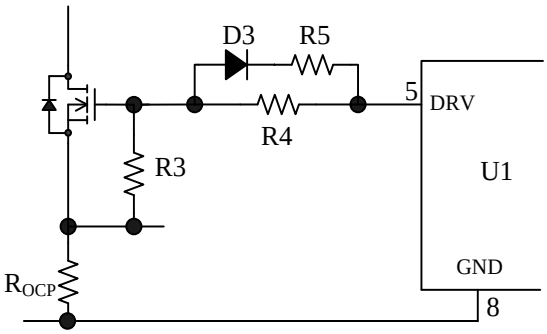

Figure 8-31. DRV Pin Peripheral Circuit

9. Design Notes

9.1. Peripheral Components

Take care to use properly rated and proper type of components.

- Input and output electrolytic capacitor
  Apply proper design margin to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch-mode power supplies, is recommended, depending on their purposes.
- Transformer
  Apply proper design margin to core temperature rise by core loss and copper loss. Because switching currents contain high frequency currents, the skin effect may become a consideration. In consideration of the skin effect, choose a suitable wire gauge in consideration of rms current and a current density of about 3 to 4A/mm^2. If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

- Current detection resistor, R_{OCP}
  A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

9.2. Transformer Design

The design of the transformer is fundamentally the same as the power transformer of a Ringing Choke Converter (RCC) system: a self-excitation type flyback converter.

However, because the duty cycle will change due to the quasi-resonant operations delaying the turn-on, the duty cycle needs to be compensated.

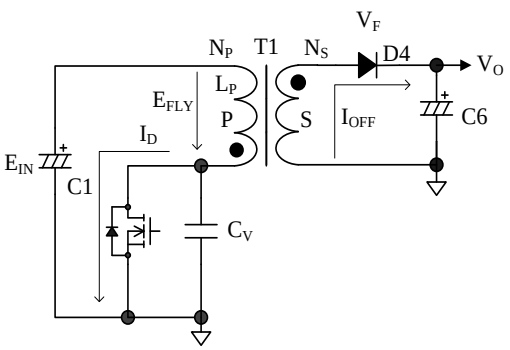

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Figure 9-1. Quasi-resonant Circuit

When the duty cycle, D_{ON}, is calculated by the ratio of the primary turns, N_P, and the secondary turns, N_S, the inductance, L_P' on the primary side, taking into consideration the delay time, can be calculated by Equation(11).

$$L_P' = \frac{\left(E_{IN(MIN)} \times D_{ON}\right)^2}{\left(\sqrt{\frac{2 \times P_O \times f_0}{\eta_1}} + E_{IN(MIN)} \times D_{ON} \times f_0 \times \pi \times \sqrt{C_V}\right)^2} \quad (11)$$

where:
P_O is the maximum output power,
f_O is the minimum operation frequency of quasi-resonant operation,
C_V is the voltage resonance capacitor connected between the drain and source of the power MOSFET,
η_1 is the transformer efficiency,
D_{ON} is the duty cycle at the minimum input voltage:

$$D_{ON} = \frac{E_{FRY}}{E_{IN(MIN)} + E_{FRY}}.$$

$E_{IN(MIN)}$ is the C1 voltage of Figure 9-1 at the minimum input voltage,
E_{FLY} is the flyback voltage:

$$E_{FRY} = \frac{N_D}{N_P} \times (V_O + V_F), \text{and}$$

V_F is the forward voltage drop of D4.

Each parameter, such as the peak drain current, I_{DP}, is calculated as follows:

$$t_{ONDLY} = \pi\sqrt{L_P' \times C_V} \quad (12)$$

$$D_{ON}' = D_{ON}(1 - f_0 \times t_{ONDLY}) \quad (13)$$

$$I_{IN} = \frac{P_O}{\eta_2} \times \frac{1}{E_{IN(MIN)}} \quad (14)$$

$$I_{DP} = \frac{2 \times I_{IN}}{D_{ON}'} \quad (15)$$

$$N_P = \sqrt{\frac{L_P'}{AL - value}} \quad (16)$$

$$N_S = \frac{N_P \times (V_O + V_F)}{E_{FRY}} \quad (17)$$

where:
t_{ONDLY} is the delay time of quasi-resonant operation,
I_{IN} is the average input current,
η_2 is the conversion efficiency of the power supply,
I_{DP} is the peak drain current
D_{ON}' is the duty cycle after compensation, and
V_O is the secondary side output voltage

The minimum operation frequency of quasi-resonant operation, f_O, can be calculated by Equation (18)

In transformer design, AL-value and N_P must be set in a way that the ferrite core does not saturate. Here, use ampere turn value (AT), the result of $I_{DP} \times N_P$ and the graph of NI-Limit (AT) versus AL-value (Figure 9-2 is an example of it). NI-Limit is the limit that the ampere turn value should not exceed; otherwise the core saturates.

When choosing a ferrite core to match the relationship of NI-Limit (AT) versus AL-value, it is recommended to set the calculated NI-Limit value below about 30% from the NI-Limit curve of ferrite core data, as shown in the hatched area containing the design point in Figure 9-2, to provide a design margin in consideration of temperature effects and other variations.

$$f_0 = \left(\frac{-\sqrt{\frac{2P_O}{\eta_1}} + \sqrt{\frac{2P_O}{\eta_1} + \frac{4\pi\left(E_{IN(MIN)} \times D_{ON}\right)^2 \times \sqrt{C_V}}{\sqrt{L_P'}}}}{2\pi\sqrt{C_V} \times E_{IN(MIN)} \times D_{ON}} \right)^2 \quad (18)$$

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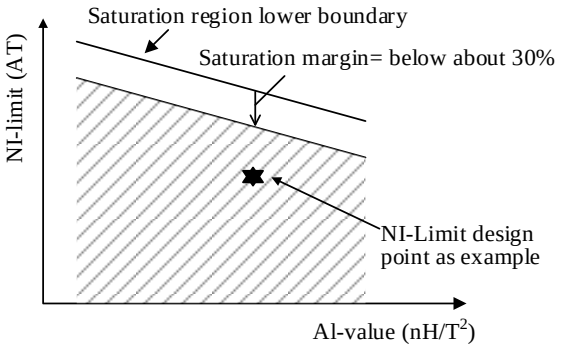

Figure 9-2. Example of NI-limit vs. AL-value Characteristics

9.3. Protection against Negative Input Voltage at Start-up Pin

If the ST pin voltage is applied more negative voltage than −0.3 V, the IC may be out of normal operation, and thus either a diode or a resistor must be added, as shown in Figure 9-3. The diode or resistor should be chosen in the following specification. In addition, it is necessary to check the operation based on actual operation across the full range of input voltage in the application.

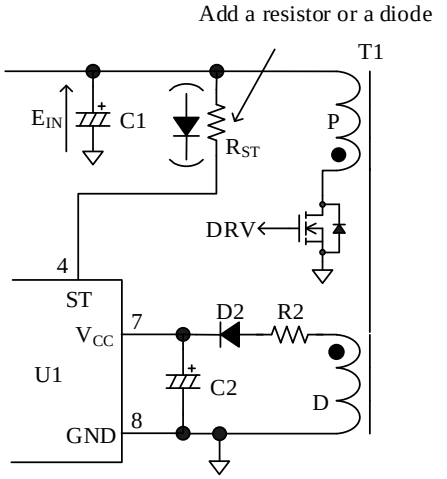

Figure 9-3. ST Pin Countermeasure against Negative Applied Voltage

- **The recommended specification of additional diode or resistor**

- The case of resistor, R_{ST}

  type of resistors, such as metal oxide film.
  The minimum value: 5.6 kΩ
  The maximum value: Meet Equation (19).

$$\left|I_{CC(STARTUP)}(\text{min.})\right| \times R_{ST} + V_{START(ON)}(\text{max.}) \ll E_{IN}(\text{min.}) \quad (19)$$

Where:
$I_{CC(STARTUP)}$(min.) is −4.5 mA,
$V_{START(ON)}$(max.) is 24 V, and
E_{IN}(min.) is the C1 voltage at the minimum input voltage.

The value of R_{ST} in universal input range (85 VAC to 265 VAC) is 5.6 kΩ to 15 kΩ.

- Diode characteristics

  Peak reverse voltage, V_{RM}: >35 V
  Forward current, I_F: >4.5 mA
  Reverse recovery time, trr: <27 μs
  Reverse current, I_R: <100 μA

9.4. Phase Compensation

A typical phase compensation circuit with a secondary shunt regulator (U2) is shown in Figure 9-4. The value of C7 is recommended to be about 0.047 μF to 0.47μF, and should be chosen based on actual operation in the application. Place C3 between the FB/OLP pin and the GND pin, as shown in Figure 9-5, to perform high frequency noise reduction and phase compensation. The value of C3 is recommended to be about 470pF to 0.01μF, and should be chosen based on actual operation in the application.

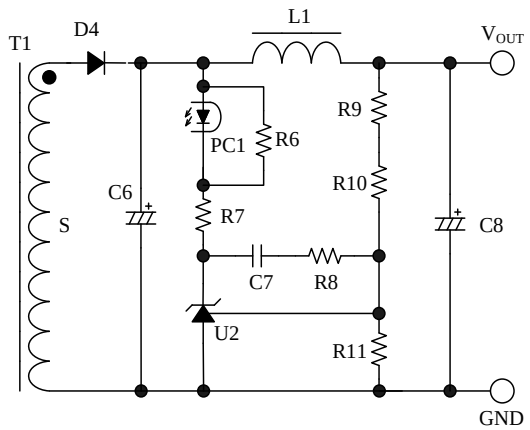

Figure 9-4. Peripheral Circuit around Secondary Shunt Regulator (U2)

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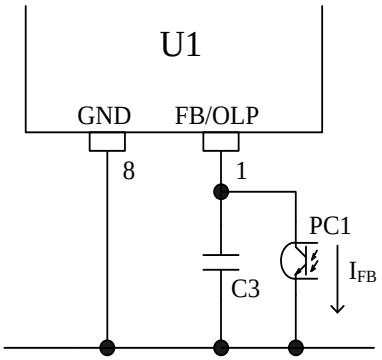

Figure 9-5. FB/OLP Peripheral Circuit

9.5. PCB trace layout and Component placement

PCB design and component layout significantly affect operation, EMI noise, and power dissipation. Therefore, pay extra attention to these designs. In general, where high frequency current traces form a loop, as shown in Figure 9-6, wide, short traces, and small circuit loops are important to reduce line impedance. In addition, earth ground traces affect radiated EMI noise, and the same measures should be taken into account. Switch-mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines. Furthermore, because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it when preparing a thermal design.

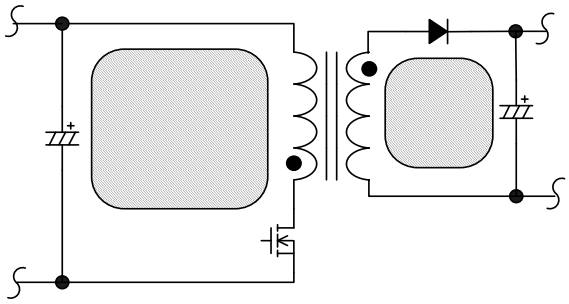

Figure 9-6. High Frequency Current Loops (Hatched Areas)

Figure 9-7 shows a circuit layout design example.

- **IC Peripheral Circuit**

(1) Power MOSFET and OCP Trace Layout
This is the main trace containing switching currents, and thus it should be as wide and short as possible.
If C1 and the IC are distant from each other, an electrolytic capacitor or film capacitor (about 0.1μF and with proper voltage rating) near the IC or the transformer is recommended to reduce impedance of the high frequency current loop.

(2) GND Trace Layout:
This trace also must be as wide and short as possible.
If C2 and the IC are distant from each other, placing a capacitor (approximately 0.1 μF to 1.0μF film capacitor) close to the VCC pin and the GND pin is recommended.

(3) R_{OCP} Trace Layout
R_{OCP} should be placed as close as possible to the peripheral components of OCP pin. The connection between the power ground of main trace and the control circuit ground should be connected by a single point ground (point A in Figure 9-7) to remove common impedance, and to avoid interference from switching currents to the control circuit.

- **Secondary Rectifier Trace Layout**

This trace should be as wide as possible. If the loop distance is lengthy, leakage inductance resulting from the long loop may increase surge voltage at turning off the power MOSFET. Proper secondary trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

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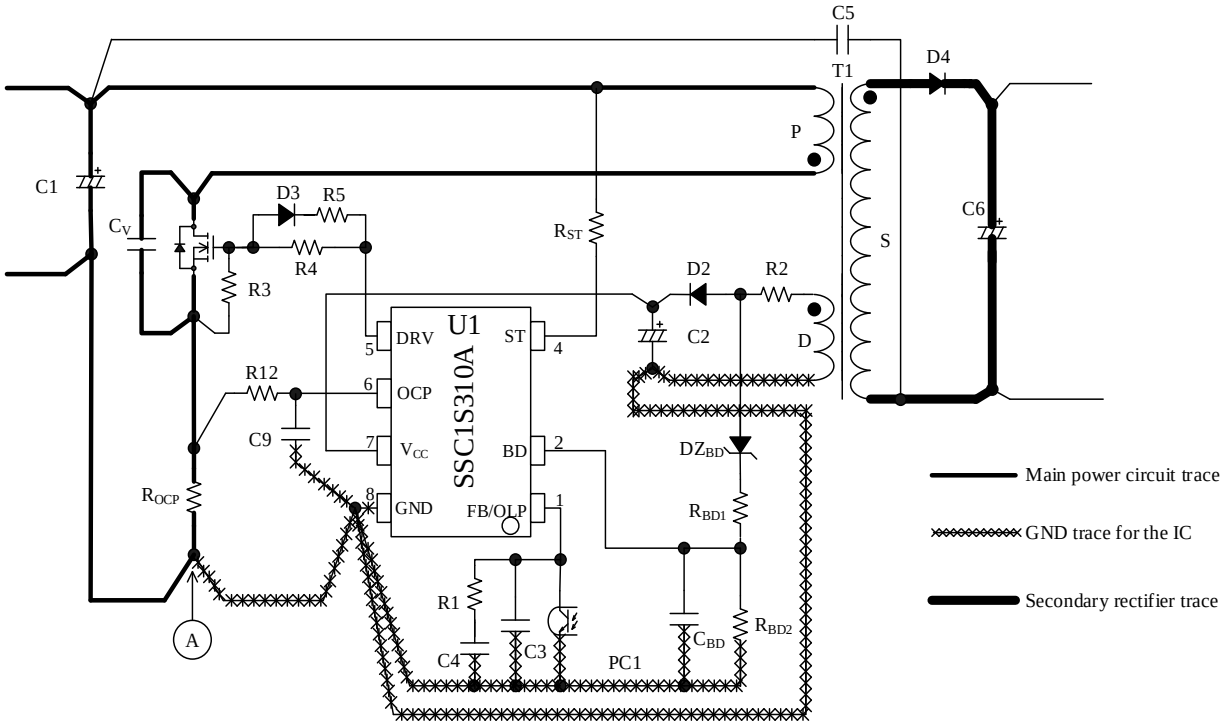

Figure 9-7. Peripheral Circuit Example around the IC

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