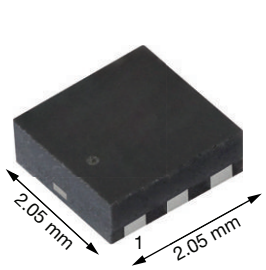
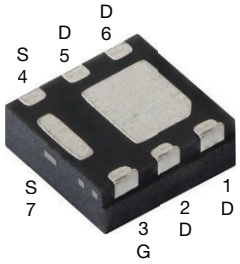
Automotive P-Channel 20 V (D-S) 175 °C MOSFET

PowerPAK® SC-70W-6L Single



Top View



Bottom View

Marking Code: QYXXXX

FEATURES

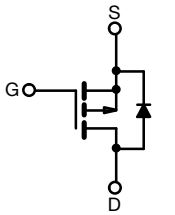
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ (Ω) at V_{GS} = -4.5 V	0.0250
$R_{DS(on)}$ (Ω) at V_{GS} = -2.5 V	0.0420
I_D (A)	-9
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA407CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	± 12	
Continuous drain current [a]	T_C = 25 °C	I_D	-9	A
	T_C = 125 °C		-9	
Continuous source current (diode conduction) [a]		I_S	-9	
Pulsed drain current [b]		I_{DM}	-36	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	-15	
Single pulse avalanche energy		E_{AS}	11.25	mJ
Maximum power dissipation	T_C = 25 °C	P_D	13.6	W
	T_C = 125 °C		4.5	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [c]	R_{thJA}	90	°C/W
Junction-to-case (drain)		R_{thJF}	11	

Notes

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Not intended for continuous use with positive gate voltage > 3.0 V

For technical questions, contact: automostechsupport@vishay.com

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = -250 µA		-20	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA		-0.6	-1.0	-1.3	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = -20 V	-	-	-1	µA
		V_{GS} = 0 V	V_{DS} = -20 V, T_J = 125 °C	-	-	-50	
		V_{GS} = 0 V	V_{DS} = -20 V, T_J = 175 °C	-	-	-150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = -4.5 V	V_{DS} ≥ 5 V	-8	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -4.5 V	I_D = -4.5 A	-	0.0202	0.0250	Ω
		V_{GS} = -4.5 V	I_D = -4.5 A, T_J = 125 °C	-	-	0.0337	
		V_{GS} = -4.5 V	I_D = -4.5 A, T_J = 175 °C	-	-	0.0381	
		V_{GS} = -2.5 V	I_D = -3 A	-	0.0338	0.0420	
Forward transconductance [b]	g_{fs}	V_{DS} = -10 V, I_D = -4 A		-	20	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = -10 V, f = 1 MHz	-	1500	2100	pF
Output capacitance	C_{oss}			-	219	310	
Reverse transfer capacitance	C_{rss}			-	195	275	
Total gate charge [c]	Q_g	V_{GS} = -4.5 V	V_{DS} = -10 V, I_D = -8 A	-	15.7	24	nC
Gate-source charge [c]	Q_{gs}			-	3.6	-	
Gate-drain charge [c]	Q_{gd}			-	4.6	-	
Gate resistance	R_g	f = 1 MHz		1.2	2.45	3.7	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = -10 V, R_L = 4 Ω I_D ≅ -2.5 A, V_{GEN} = -4.5 V, R_g = 1 Ω		-	16	24	ns
Rise time [c]	t_r			-	22	33	
Turn-off delay time [c]	$t_{d(off)}$			-	29	44	
Fall time [c]	t_f			-	10	15	
Source-Drain Diode Ratings and Characteristics							
Pulsed current [a]	I_{SM}			-	-	-36	A
Forward voltage	V_{SD}	I_F = -4.5 A, V_{GS} = 0		-	-0.81	-1.2	V
Body diode reverse recovery time	t_{rr}	I_F = -2 A, di/dt = 100 A/µs		-	13	26	ns
Body diode reverse recovery charge	Q_{rr}			-	6	12	nC
Reverse recovery fall time	t_a			-	7	-	ns
Reverse recovery rise time	t_b			-	6	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-0.8	-	A

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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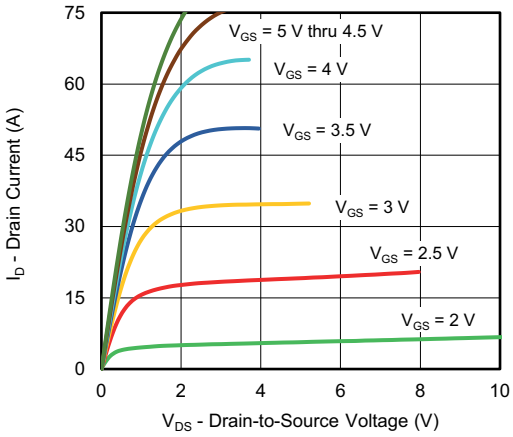
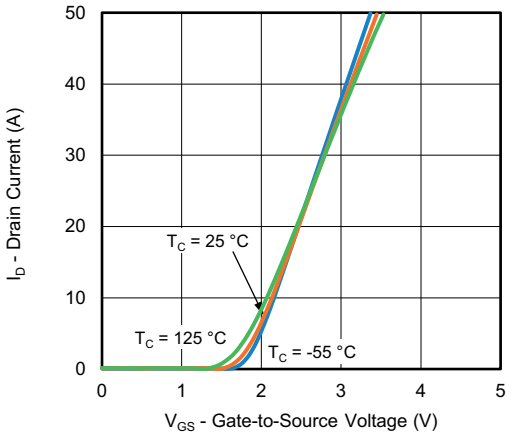
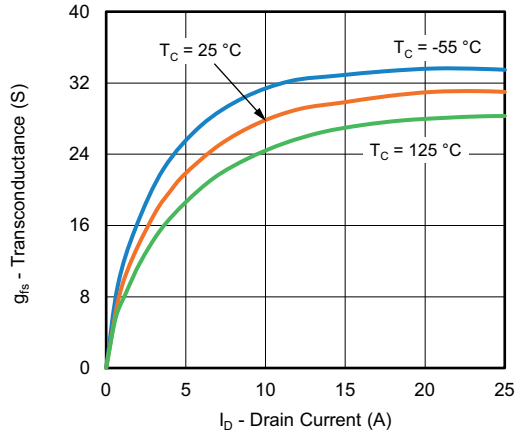
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



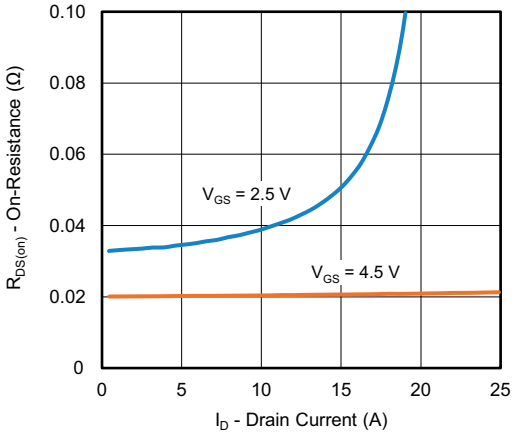
Output Characteristics



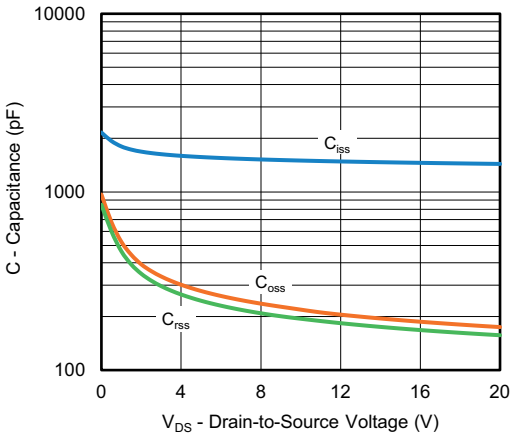
Transfer Characteristics



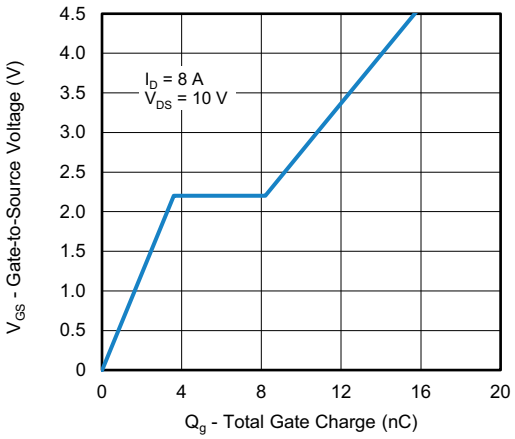
Transconductance



On-Resistance vs. Drain Current



Capacitance



Gate Charge

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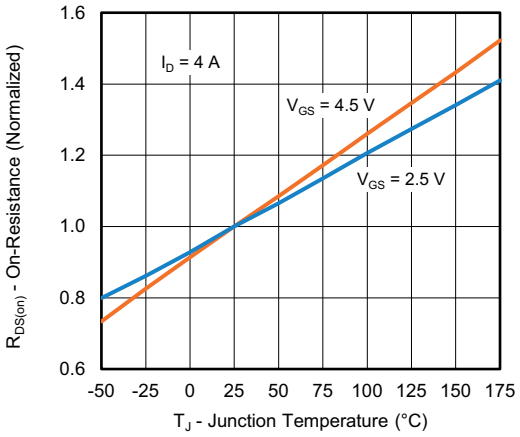
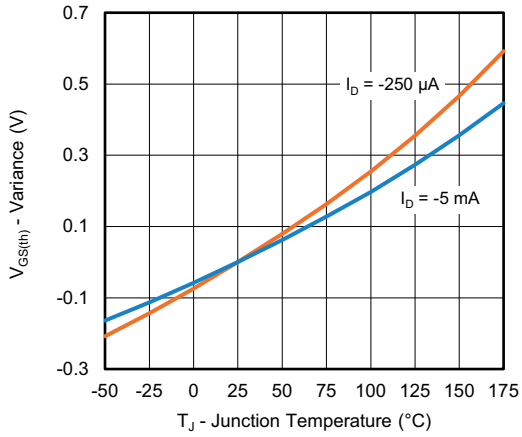
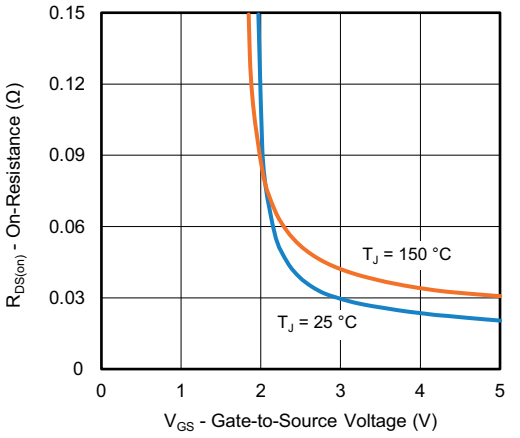


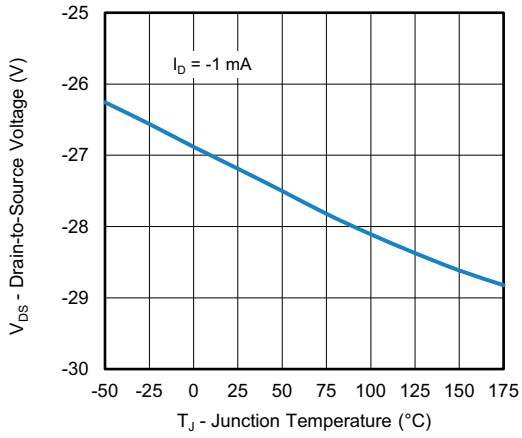
On-Resistance vs. Junction Temperature



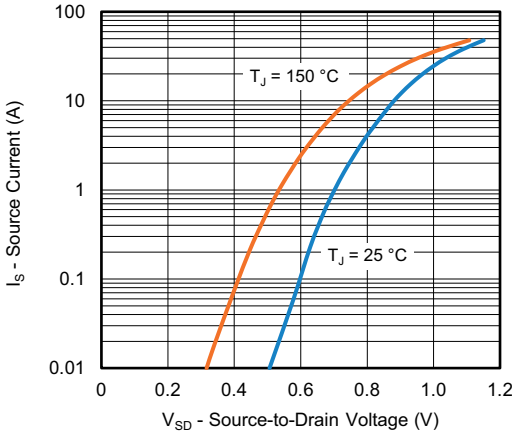
Threshold Voltage



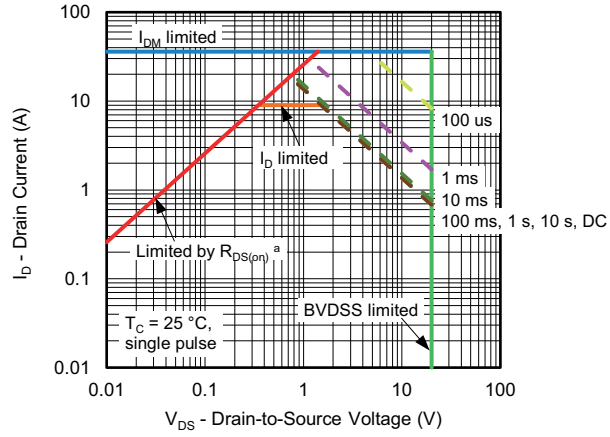
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Source-Drain Diode Forward Voltage



Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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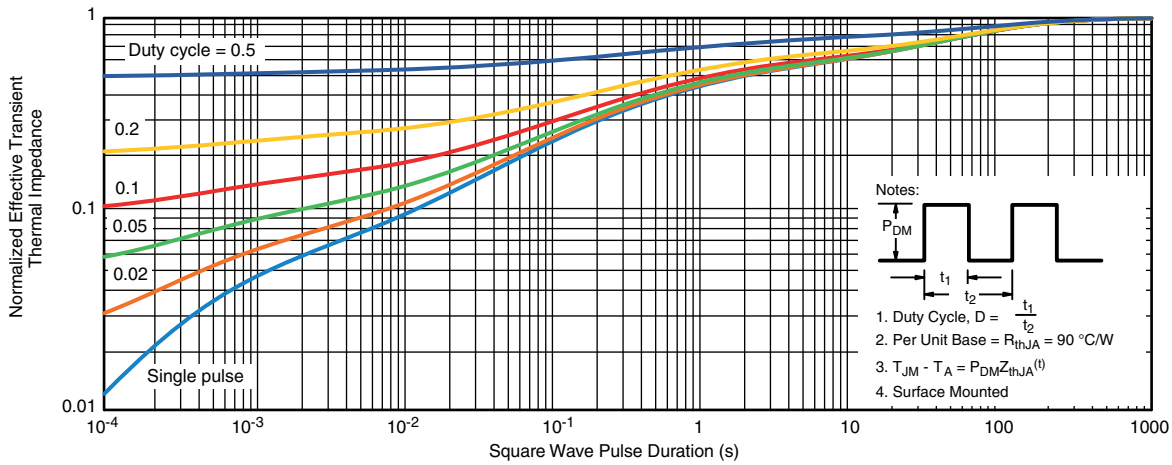
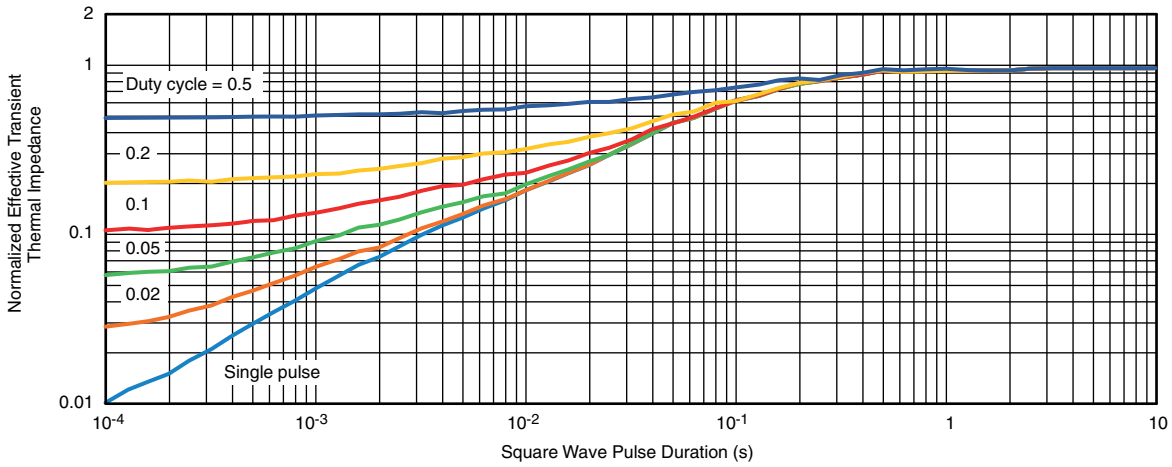


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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