Primary-side Regulation
PWM Controller for Automotive Applications

SPF8201

Data Sheet

Description

The SPF8201 is power IC for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC. The IC is suitable for switching power supply such as flyback circuit. The IC has a high accuracy error amplifier and provides a stable output voltage.

When the load of the power supply circuit becomes light, the operation of IC becomes the burst oscillation mode in order to improve the circuit efficiency.

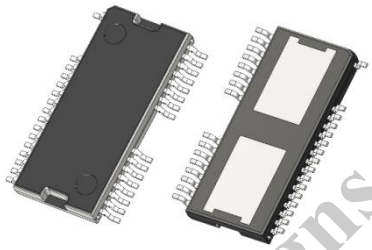
By employing the primary-side regulation, the IC realizes low component counts and design-friendliness, leading to downsizing and standardization of the power supply circuit.

Features

- AEC-Q100 Qualified
- Current Mode Type PWM Control
  (Switching frequency can be adjusted by external capacitor)
- Reducing External Component Count by Primary-side Regulation
- Built-in High Efficiency Error Amplifier
  (V_{FB} = 2.5 V ± 2%, − 40 °C to 125 °C)
- Operation Mode
  Normal Operation: PWM Mode
  Light Load Operation: Burst Oscillation
- Soft Start
  (Startup time can be adjusted by external capacitor)
- Drive Output Stop Function
- Protections:
  Overcurrent Protection (OCP):Pulse-by-Pulse
  Overload Protection (OLP): Auto-restart
  Thermal Shutdown Protection (TSD) with Hysteresis: Auto-restart

Package

HSOP40



Not to scale

Specifications

- Power MOSFET
  Breakdown Voltage (DC): 600 V
  Breakdown Voltage (Pulse): 800 V
  Maximum On-resistance (25 °C): 6.5 Ω
  Drain Peak Current (Pulse): 3 A
- Maximum Power Supply Voltage, V_{CC}: 36 V
- Adjustable Switching Frequency (20 kHz to 200 kHz)

Applications

For following isolation auxiliary power supply:

- Inverter
- On-board Charger (OBC)
- Battery Management System (BMS)

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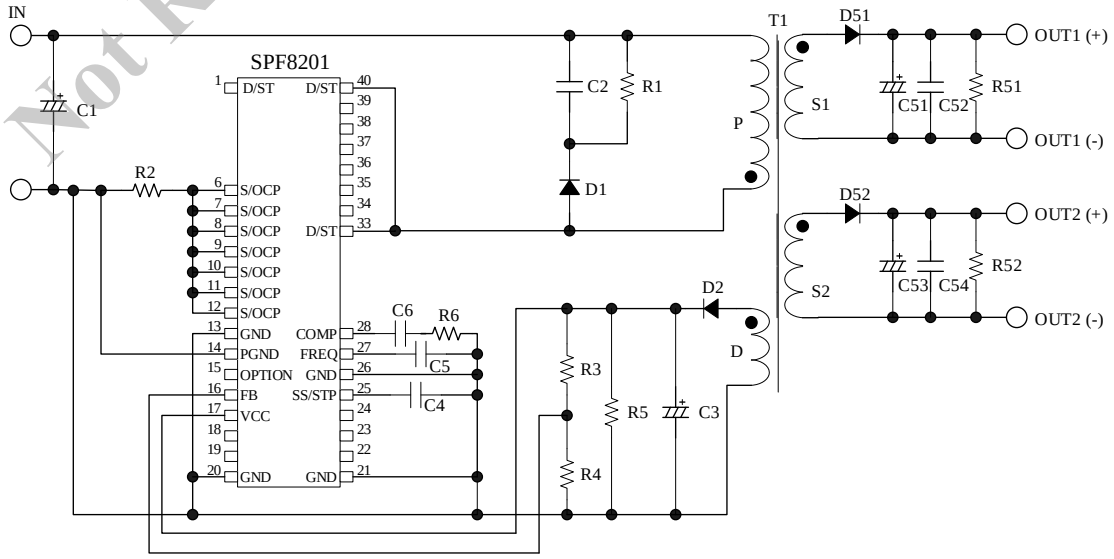
Typical Application



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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit	Remark
D/ST Pin Voltage	$V_{D/ST}$	DC T_J = −40 °C to 125 °C[1]	600	V	
		Pulse (t < 1 µs) T_J = −40 °C to 125 °C[1]	800	V	
Power MOSFET Drain-to-Source Voltage	V_{DS}	DC T_J = −40 °C to 125 °C[1]	600	V	
		Pulse (t < 1 µs) T_J = −40 °C to 125 °C[1]	800	V	
Power MOSFET Drain Current (Peak)	I_D	Single pulse	3	A	
PGND Pin Voltage	V_{PG}		−0.3 to 0.3	V	
S/OCP Pin Voltage	$V_{S/OCP}$		−2 to 6	V	
FB Pin Voltage	V_{FB}		−0.3 to 6	V	
VCC Pin Voltage	V_{CC}		−0.3 to 36	V	
SS/STP Pin Voltage	$V_{SS/STP}$		−0.3 to 6	V	
FREQ Pin Voltage	V_{FREQ}		−0.3 to 6	V	
COMP Pin Voltage	V_{COMP}		−0.3 to 6	V	
Power Dissipation	P_D	T_C = 25 °C	35.7	W	
		[2]	2.1	W	
Junction Temperature	T_J		−40 to 150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	

[1] Guaranteed by design when the junction temperature, T_J, is less than 25 °C.
[2] Mounted on the glass-epoxy board (115 mm × 38 mm in size, 1.6 mm in thickness).

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2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
VCC Pin Voltage	V_{CC}		—	—	28	V	
Switching Frequency	f_{OSC}		20	—	200	kHz	

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3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = −40 °C to 125 °C, V_{CC} = 16 V (after the V_{CC} exceeds the Operation Start Voltage, $V_{CC(ON)}$, once, and sets to 16 V).

The following electrical characteristics are design assurance value in T_A = −40 °C to 125 °C. The shipping test temperature of the products is 25 °C and 125 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		13.1	15.3	16.5	V	
Operation Stop Voltage	$V_{CC(OFF)}$		7.0	8.3	9.6	V	
Circuit Current in Operation	$I_{CC(ON)}$	VCC > $V_{CC(ON)}$	—	3.4	3.6	mA	
Circuit Current in Non-operation	$I_{CC(OFF)}$	VCC < $V_{CC(ON)}$	—	0.15	0.40	mA	
Startup Current	$I_{STARTUP}$	D/ST = 300 V, VCC = 0 V	1.0	2.5	4.0	mA	
Normal Operation							
SS/STP Pin High Threshold Voltage	V_{HSS}		1.1	1.2	1.3	V	
SS/STP Pin Low Threshold Voltage	V_{LSS}		0.1	1.2	1.3	V	
SS/STP Pin Source Current	$I_{SRC(SS)}$	SS/STP = 0.1 V	−26	−18	−10	µA	
SS/STP Pin Sink Current	$I_{SNK(SS)}$	SS/STP = 1.3 V	10	18	26	µA	
Switching Frequency	f_{OSC}	FREQ = 200 pF, T_J = 25 °C	90	100	110	kHz	
		FREQ = 200 pF, T_J = −40 °C to 125 °C	85	—	115	kHz	
FREQ Pin Source Current	$I_{SRC(FREQ)}$	FREQ = 0.1 V	−22	−28	−34	µA	
FREQ Pin High Threshold Voltage	V_{HF}		1.1	1.2	1.31	V	
FREQ Pin Low Threshold Voltage	V_{LF}		0.1	0.2	0.3	V	
Maximum Duty Cycle	D_{MAX}	FREQ = 200 pF	43.0	47.0	49.9	%	
Feedback Voltage	V_{FB}		2.45	2.50	2.55	V	
Burst Operation Threshold Voltage	V_{BST}		—	0.29	0.40	V	
Minimum On-time	$t_{ON(MIN)}$	FREQ = 200 pF	—	450	—	ns	
D/ST Pin Input Current	$I_{D/ST}$	D/ST–GND D/ST = 600 V	—	200	500	µA	
Protection Function							
Leading Edge Blanking Time*	t_{BW}	FREQ = 200 pF	—	250	—	ns	
OCP Threshold Voltage	V_{OCP}		0.46	0.50	0.54	V	
OLP Delay Time	t_{OLP}	SS/STP = 0.01 µF	24	38	52	ms	
Drive Stop SS/STP Pin Threshold Voltage	V_{STS}		3.5	4.0	4.5	V	

* Guaranteed by design.

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Drive Recovery SS/STP Pin Threshold Voltage	V_{STR}		3.1	3.6	4.1	V	
Thermal Shutdown Operating Temperature*	$T_{JH(TSD)}$		151	165	—	°C	
Thermal Shutdown Release Temperature*	$T_{JL(TSD)}$		—	150	—	°C	
Power MOSFET							
Drain-to-Source Leakage Current	I_{DSS}	D/ST = 600 V, T_J = 25 °C	—	—	10	µA	
		D/ST = 600 V, T_J = 125 °C	—	—	100	µA	
Power MOSFET On-resistance	$R_{DS(ON)}$	I_D = 0.5 A, T_J = 25 °C	—	5.6	6.5	Ω	
		I_D = 0.5 A, T_J = 125 °C	—	—	13	Ω	
Switching Time	t_r	D/ST = 10 V, R_{LOAD} = 100 Ω, see Figure 3-1	—	—	350	ns	
	t_f	D/ST = 10 V, R_{LOAD} = 100 Ω, see Figure 3-1	—	—	350	ns	

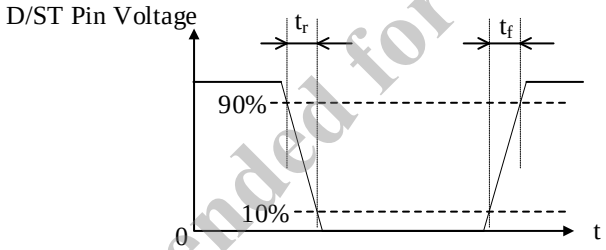

Figure 3-1. Definition of Switching Time

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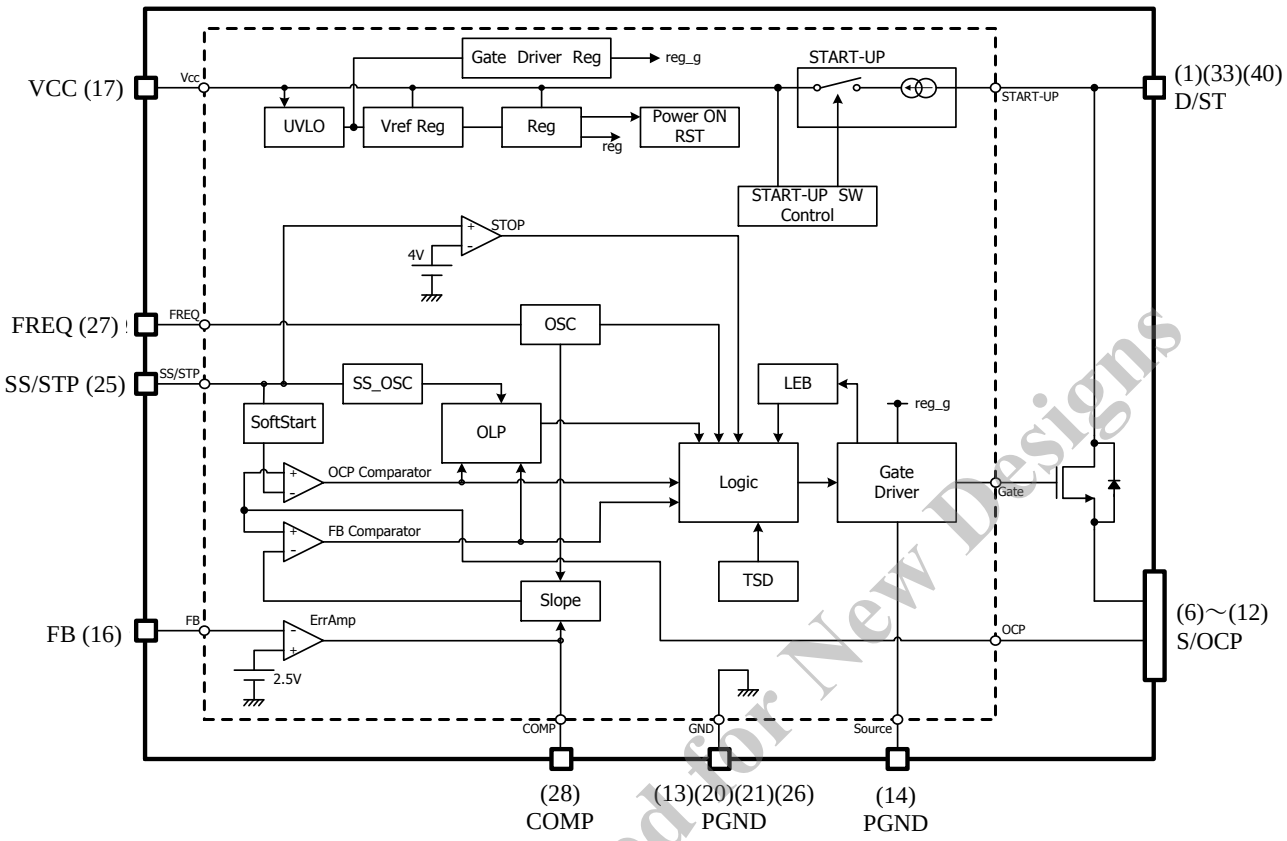
4. Block Diagram



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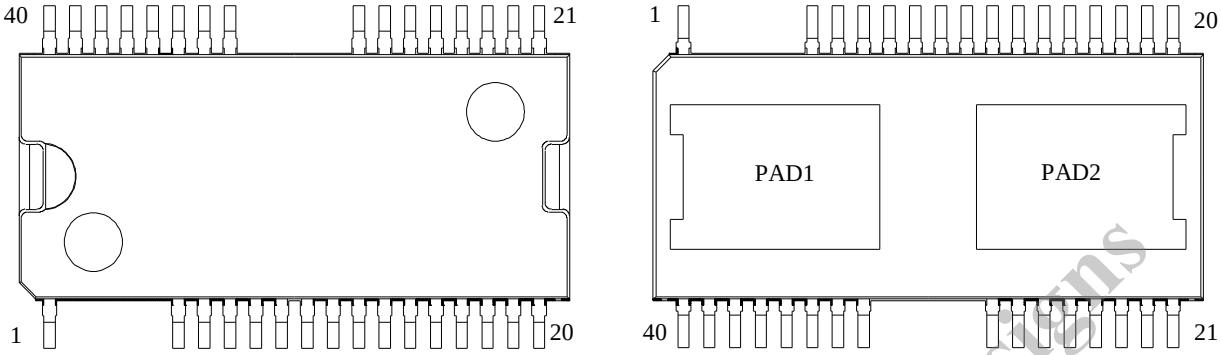
5. Pin Configuration Definitions

1, 33 and 40 pins are internally connected to the heatsink PAD1 (D/ST).
13, 20 and 21 pins are internally connected to the heatsink PAD2 (GND).



Pin Number	Pin Name	Functions	Pin Number	Pin Name	Functions
1	D/ST	Power MOSFET drain and startup current input	21	GND	Ground
2	—	(Pin removed)	22	(NC)	(Not connected)
3			23		
4			24		
5			25	SS/STP	Connecting capacitor for soft-start time and OLP delay time setting, and the DRIVE pin stop signal input
6	S/OCP	Power MOSFET source and Overcurrent Protection (OCP) signal input	26	GND	Control ground
7			27	FREQ	Connecting capacitor for switching frequency setting
8			28	COMP	Connecting capacitor for phase compensation
9			29	—	(Pin removed)
10			30		
11			31		
12			32		
13	GND	Ground	33	D/ST	Power MOSFET drain and startup current input
14	PGND	Power ground (Ground for gate drive)	34	(NC)	(Not connected)
15	OPTION	Test pin (connection prohibited, the pin must be open)	35		
16	FB	Constant voltage control signal input	36		
17	VCC	Power supply voltage input	37		
18	(NC)	(Not connected)	38		
19			39		
20	GND	Ground	40	D/ST	Power MOSFET drain and startup current input
PAD1	D/ST	Power MOSFET drain and startup current input	PAD2	GND	Ground

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6. Typical Application

In applications having a power supply specified such that the drain pin of external power MOSFET has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (C2, R1, and D1) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor or a resistor-capacitor combination should be added between the drain pin and the source pin.

The GND pins (13, 20, 21, and 26 pins) should be all shorted on the PCB.

The S/OCP pins (6 pin to 12 pin) should be all shorted on the PCB.

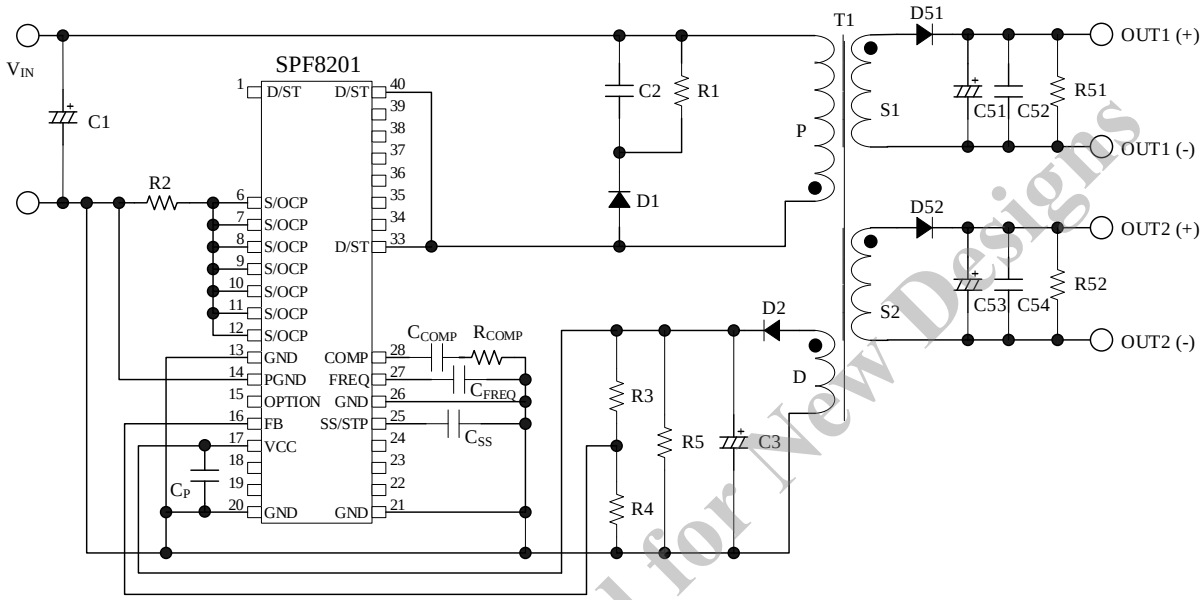

Figure 6-1. Typical Application

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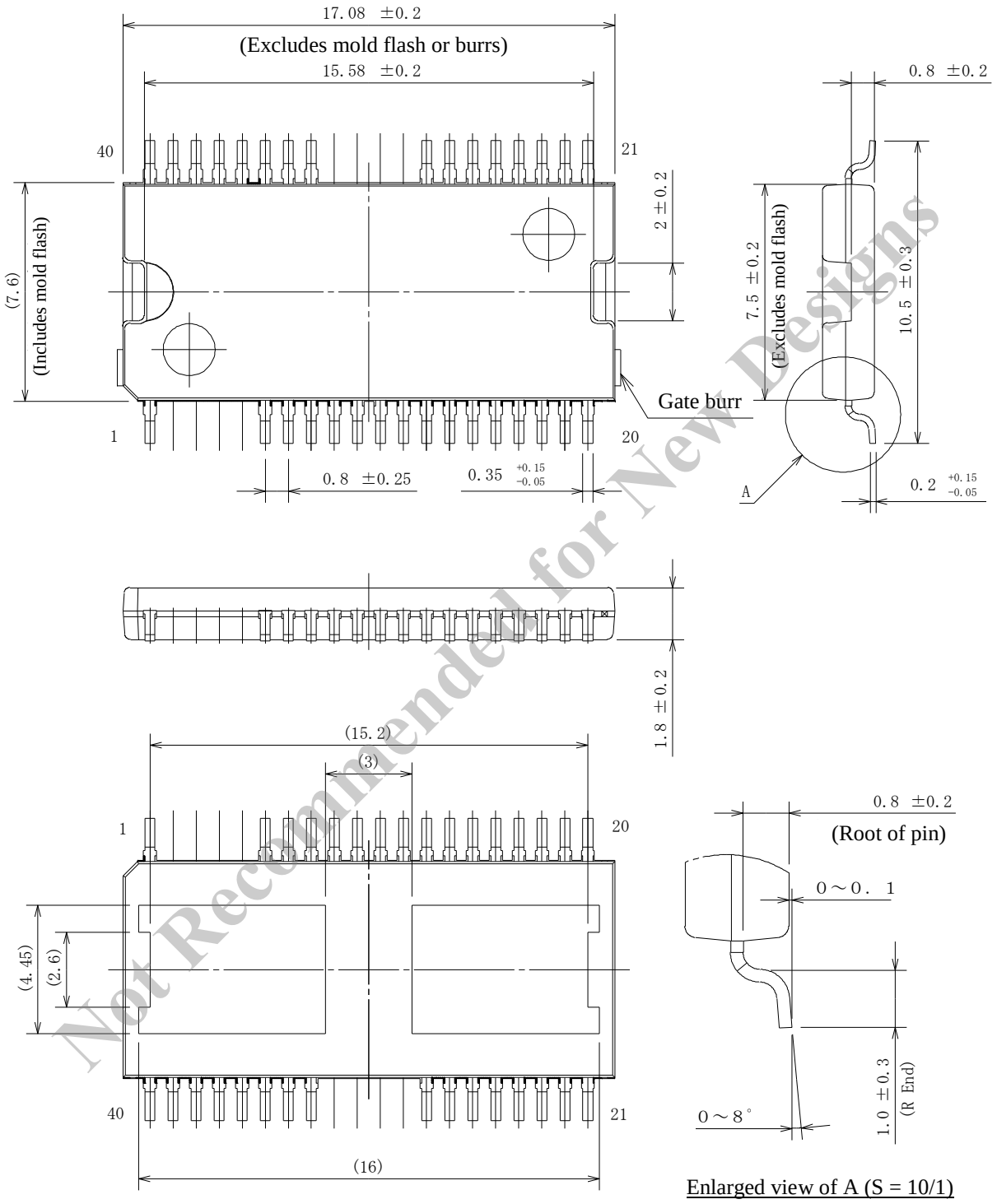
7. Physical Dimensions

● **HSOP40 Package**



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NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)

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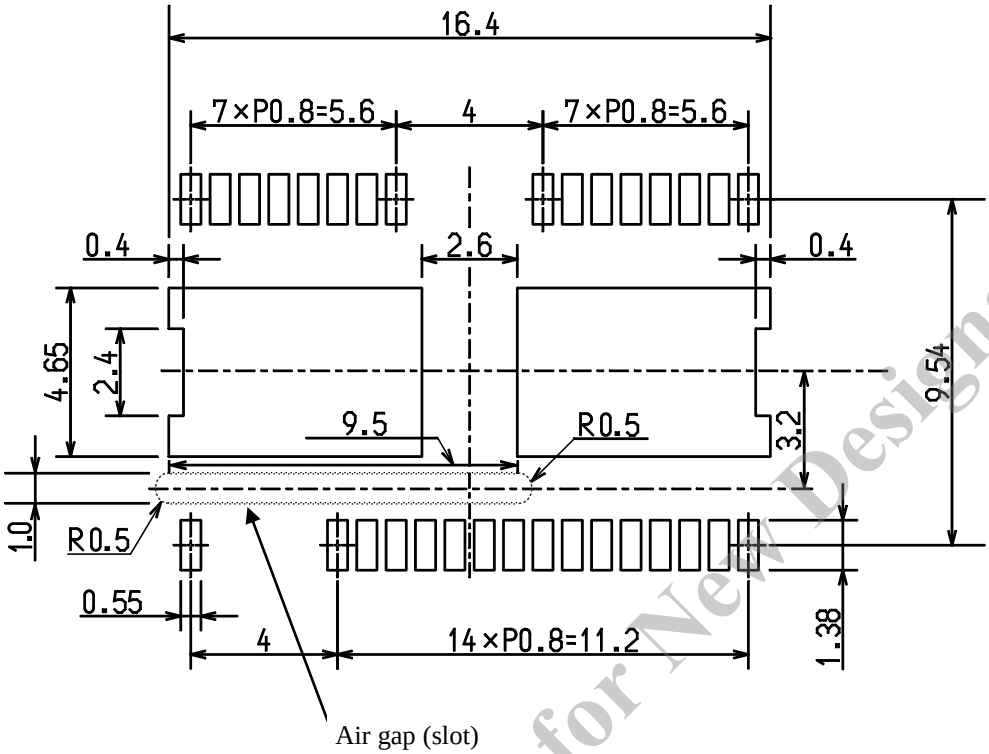
● **HSOP40 Land Pattern Example**
For increasing a creepage distance, add an air gap (slot) on the board as needed.



8. Marking Diagram



Part Number

Lot Number

Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

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9. Operational Description

Unless otherwise specified, the characteristics values are shown in typical value. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

9.1. Pin Descriptions

9.1.1. D/ST

The D/ST pin is connected to power MOSFET drain and IC startup circuit.

9.1.2. VCC

The VCC pin is the power input pin of the IC.

When the VCC pin voltage fluctuates greatly, the IC may malfunction. To suppress high frequency noise, a ceramic capacitor, C_P, must be placed as close as possible to the VCC pin, and must be connected as short as possible. C_P is about 0.1 µF.

9.1.3. FB

The FB pin is the input of the output voltage feedback signal. The IC controls the FB pin voltage to V_{FB} = 2.50 V (see Section 9.4).

9.1.4. GND and PGND

The GND pin is the IC control ground and the PGND pin is the ground for internal gate drive circuit.

The GND pins (13, 20, and 21 pins) are internally connected to the heatsink (GND). These pins should be connected 26 pin (the GND pin) on the PCB.

The fluctuation of the control ground potential may cause the malfunction of the IC. The control ground trace should be separated from PGND pin trace or power ground and connected to the GND pin as short as possible. Please pay attention to design of the control ground trace to avoid the effect from the high frequency current line.

9.1.5. SS/STP

The SS/STP pin has three functions as follows:

- Setting the soft start time (see Section 9.3)
- Stopping the drive (see Section 9.7)
- Setting the OLP (Overload Protection) delay time (see Section 9.9)

The capacitor, C_{SS}, for setting the soft start time and the OLP delay time is connected to the SS/STP pin. These both functions should be taken into account in setting the value of C_{SS}.

In normal operation, the CSS pin voltage becomes sawtooth waveform. The SS/STP pin charges the C_{SS} by $I_{SRC(SS)}$ = −18 µA, and discharges the C_{SS} by $I_{SNK(SS)}$ = 18 µA when the SS/STP pin voltage reaches V_{HSS} = 1.2 V. The SS/STP pin starts to charge again when the SS/STP pin voltage decreases to V_{LSS} 1.2 V.

9.1.6. FREQ

The FREQ pin is connected to the capacitor, C_{FREQ}, for setting the frequency of the internal oscillation. For the setting of oscillation frequency, see Section 9.6.

9.1.7. COMP

The COMP pin is the output pin of an internal error amplifier. The capacitor for phase compensation, C_{COMP}, and the resistor, R_{COMP}, are connected in series to the COMP pin as shown in Figure 9-1. The values of capacitor and resistor are set according to the actual operation.

C4 and R7 are for the noise reduction filter.

Table 9-1 shows the reference characteristic of the internal error amplifier.

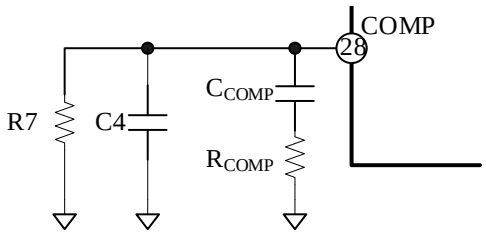

Figure 9-1. COMP Pin Peripheral Circuit

Table 9-1. Reference Characteristic of Internal Error Amplifier

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output High Voltage	V_{CMPH}	2.4	—	—	V
Output Low Voltage	V_{CMPL}	—	—	0.2	V
Output Current	I_{COMP}	±80	±120	±160	µA
Transformer Conductance	gm	1100	1500	1900	µA/V

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9.1.8. S/OCP

The S/OCP pin is the detection pin of the drain current of the built-in power MOSFT, and is internally connected to source of the power MOSFET. The current detection resistor, R_{OCP}, is connected between the S/OCP pin and the GND pin. The drain current value detected by the S/OCP pin is used for the output voltage control (see Section 9.4) and the overcurrent protection.

For the setting of overcurrent detection resistor, see Section 9.8.

9.2. IC Startup

The IC incorporates the startup circuit. The circuit is connected to the D/ST pin. When the power supply voltage, V_{IN}, is applied, the internal startup circuit is activated. Then, the constant current, $I_{STARTUP}$ = 2.5 mA, charges electrolytic capacitor, C3, connected to the VCC pin. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the control circuit starts operation. After the IC starts switching operation, the VCC pin voltage is the rectified auxiliary winding voltage, V_D, as shown in Figure 9-2.

After switching operation begins, the startup circuit turns off automatically to eliminate the power dissipation by the startup circuit.

The relation between the VCC pin and circuit current is shown in Figure 9-3. After the control circuit is activated, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.3 V, the control circuit stops operation and reverts to the state before startup.

Adjust the winding turns of D so that the VCC pin voltage becomes in the range of Equation (1) within the input and output variation range of the power supply specification.

$$V_{CC(OFF)}(\max.) < V_{CC} < V_{CC}(\max.)$$

That is:

$$9.6\ (V) < V_{CC} < 28\ (V) \quad (1)$$

When the voltage is detected by the auxiliary winding as shown in Figure 9-2, adjust the winding turns of D so that the VCC pin voltage becomes in the range of Equation (2).

$$V_{CC(ON)}(\max.) < V_{CC} < V_{CC}(\max.)$$

That is:

$$16.5\ (V) < V_{CC} < 28\ (V) \quad (2)$$

During the period from the IC operation start to the rise of V_D, power is supplied from C3 to the IC. In this period, C3 value must be set so that the VCC pin voltage keeps more than $V_{CC\ (OFF)}$. Generally, the approximate value of C3 capacitance is 10 µF to 47 µF. C3 should be selected by confirming the actual operation.

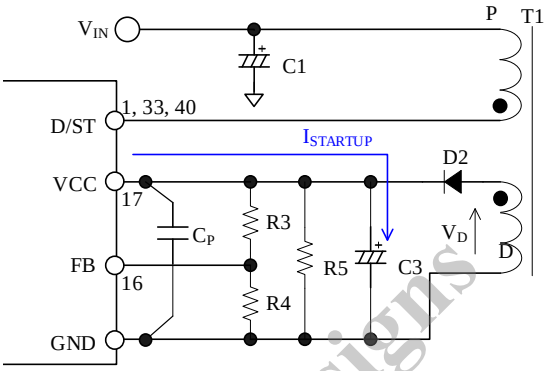

Figure 9-2. VCC Pin Peripheral Circuit

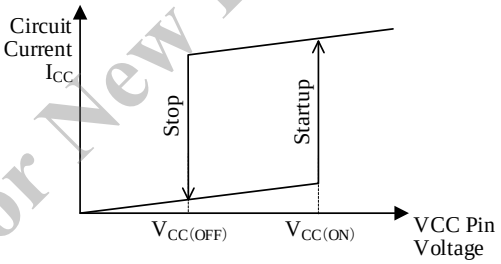

Figure 9-3. VCC Pin Voltage and Circuit Current, I_{CC}

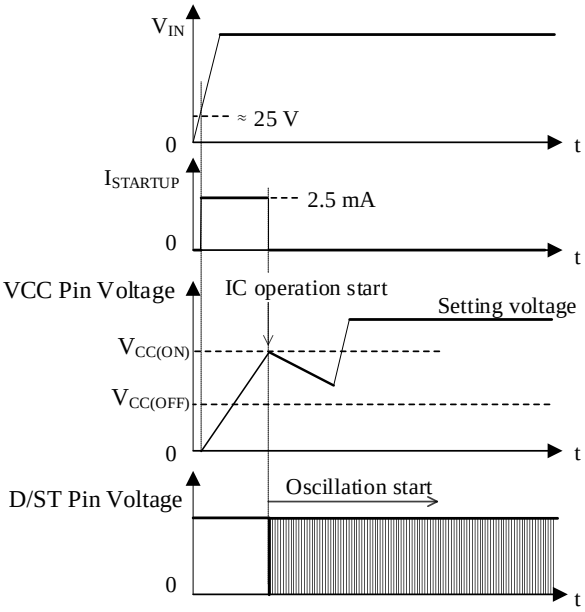

Figure 9-4. Startup Operation

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9.3. Soft Start Function

The IC operates by soft start in the power supply startup. This reduces the voltage and current stress of the power MOSFET and the secondary rectifier diode.

The soft start period is set by the capacitor, C_{SS}, connected to the SS/STP pin. When the VCC pin voltage is $V_{CC(ON)}$ or higher after the power is applied, the IC starts the operation; and the C_{SS} is charged by the SS/STP pin source current, $I_{SRC(SS)}$ = −18 µA.

When the power is supplied, the SS/STP pin voltage starts increasing. The OCP threshold voltage also increases proportional to the SS/STP pin voltage until the SS/STP pin voltage reaches V_{HSS} = 1.2 V. Thus, the drain current gradually increases in this period. When once the SS/STP pin voltage reaches the V_{HSS}, the OCP threshold voltage is fixed at V_{OCP} = 0.50 V. The approximate time of soft start operation, t_{SS}, is calculated by the following equation.

$$t_{SS}\,(s) = V_{HSS} \times \frac{C_{SS}}{|I_{SRC(SS)}|}$$

$$= 1.2\ V \times \frac{C_{SS}\,(\mu F)}{|-18\ \mu A|} \quad (3)$$

The C_{SS} value must be set with the delay time of OLP, t_{OLP}, taken into account. If the C_{SS} value is too small, the overload protection is activated in the startup; and the startup failure may be caused. The recommended C_{SS} value is 0.01 µF to 0.47 µF, and should be determined by confirming the actual operation.

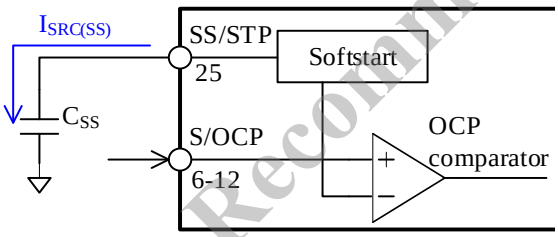

Figure 9-5. SS/STP Pin Peripheral Circuit

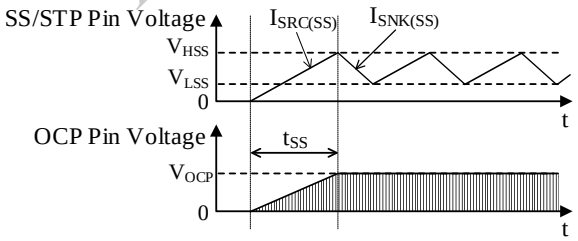

Figure 9-6. Soft Start Operation

9.4. Constant Voltage Control

The output voltage control of switching power supply uses the current-mode control method that provides the high speed response and stable operation. The IC has the error amplifier between the FB pin and the COMP pin, and controls the FB pin voltage to V_{FB} = 2.50 V.

Without an optocoupler, the secondary output voltage is controlled by detecting the voltage coupled by the secondary output and the transformer in the primary side, using the auxiliary winding, D, as shown in Figure 9-7. The relation between the smoothing voltage, V_D, and the secondary output voltage, V_{OUT}, is determined by the ratio of the auxiliary winding turns, N_D, and the secondary winding turns, N_S, as shown in Equation (4).

$$V_{OUT} = \frac{N_D}{N_S} \times V_D \quad (4)$$

V_D is divided by resistors. The divided voltage is input to the FB pin. The IC controls the FB pin voltage to V_{FB} = 2.50 V. Thus, the smoothing voltage, V_D, is calculated by the following equation.

$$V_D = \frac{(R3 + R4)}{R4} \times V_{FB} \quad (5)$$

The secondary output voltage, V_{OUT}, is calculated by the following equation.

$$V_{OUT} = \frac{N_D}{N_S} \times \frac{(R3 + R4)}{R4} \times V_{FB} \quad (6)$$

The actual V_{OUT} and the calculated value in Equation (6) do not match because of the leakage inductance between the secondary-side winding and the auxiliary winding, and the difference of the forward voltage, V_F, between the secondary rectifier diode, D51, and the auxiliary winding diode, D2. Therefore, R3 and R4 must be adjusted by confirming the actual operation.

Where N_D = N_S and V_{OUT} = V_D, the accuracy of the secondary output voltage is improved by using the same diode products for D51 and D2.

When there is a big difference of power dissipation between the auxiliary winding and the secondary side, the load regulation is degraded due to the leakage inductance of a transformer. In this case, the dummy resistor, R5, is connected across the auxiliary winding. The value of R5 is adjusted by confirming the actual operation since it differs depending on the power supply specification.

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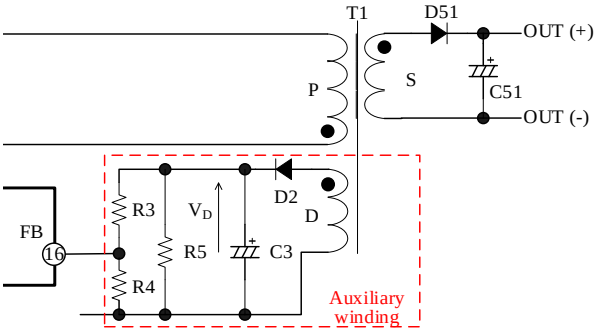

Figure 9-7. Detection by Auxiliary Winding

The voltage control operation in light/heavy load is as follows (see Figure 9-8):

- **Light Load Conditions**

When the auxiliary winding voltage, V_D, and the FB pin voltage increase according to the output voltage rise, the COMP pin voltage decreases. The IC generates the target value of the FB comparator by adding the slope compensation signal to the COMP pin voltage. The IC controls the duty cycle by comparing the peak of the target value and the S/OCP pin voltage (the drain current of the power MOSFET detected by detection resistor).

When the COMP pin voltage decreases, the target value of the FB comparator drops. As a result, the drain peak current of the power MOSFET decreases to suppress the output voltage rise.

- **Heavy Load Conditions**

In this case, contrary to the operation describe above, the target voltage of FB comparator increases. As a result, the drain peak current also increases to suppress the output voltage drop.

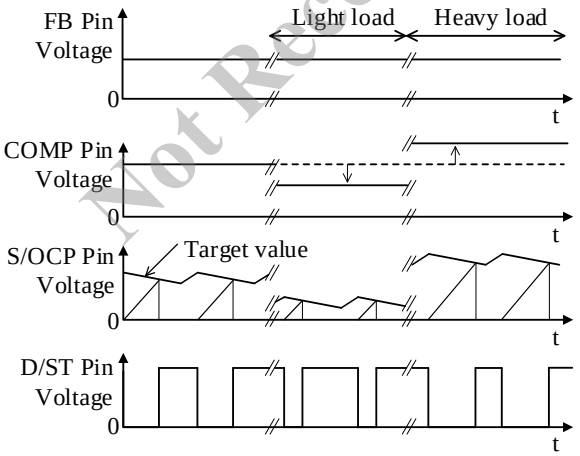

Figure 9-8. Constant Voltage Operation

9.5. Burst Function in Light Load

When the output voltage of the power supply decreases, the on-time of the power MOSFET shortens due to the COMP pin voltage reduction. As a result, the output voltage is controlled to be constant. However, the on-time of the power MOSFET cannot be shorter than the Minimum On-time, $t_{ON(MIN)}$. Therefore, the operation of the IC is automatically switched to the burst oscillation operation (intermittent oscillation) in light load.

When the COMP pin voltage decreases to Burst Operation Threshold Voltage, V_{BURST} = 0.29 V or lower, the power MOSFET is turned off. Then, the output voltage decreases, resulting in the decrease of FB pin voltage. This increases the COMP pin voltage; and the power MOSFET oscillates again. As just described, the output voltage is controlled to be constant by repeating the burst oscillation in light load.The following factors depend on the application circuit and the power supply specification.

- the burst oscillation period and duty cycle
- the oscillation stop period of the power MOSFET

9.6. Oscillation Frequency Setting

The oscillation frequency of the power MOSFET is set by the capacitor, C_{FREQ}, connected to the FREQ pin (see Figure 9-9).

The waveform of the FREQ pin voltage becomes sawtooth due to the charge/discharge of C_{FREQ}. C_{FREQ} is charged by $I_{SRC(FREQ)}$ = −28 µA as shown in Figure 9-10. When the FREQ pin voltage reaches V_{HF} = 1.2 V, C_{FREQ} is discharged by the internal switch. When the FREQ pin voltage decreases to V_{LF} = 0.2 V, C_{FREQ} is charged by $I_{SRC(FREQ)}$ again.

The oscillation frequency of the power MOSFET is determined by the frequency of the sawtooth waveform. In addition, the maximum duty cycle is controlled by the ratio of charge and discharge. For the setting of oscillation frequency of the power MOSFET, see Figure 9-11.

To avoid unstable switching cycle due to the influence such as parasitic inductance, C_{FREQ} must be used a ceramic capacitor (chip type), and be placed as close to the FREQ pin as possible. Ultimately, it is required to be set C_{FREQ} by confirming the actual operation.

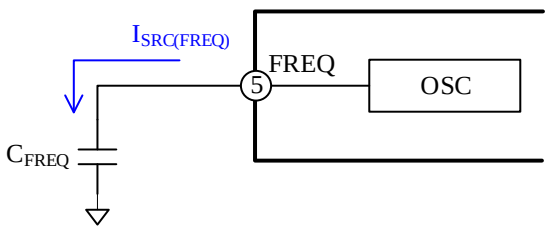

Figure 9-9. FREQ Pin Peripheral Circuit

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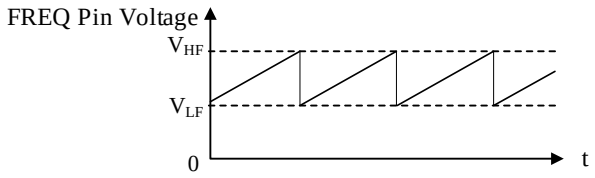

Figure 9-10. FREQ Pin Voltage Waveform

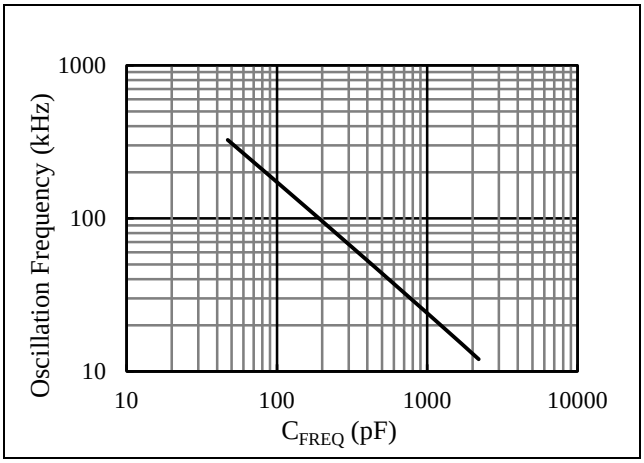

Figure 9-11. Oscillation Frequency vs. C_{FREQ} (Reference)

9.7. Drive Stop Function

The IC has the drive stop function. When a voltage is externally applied to the SS/STP pin, the function is activated, forcibly fixes the power MOSFET off, and stops the oscillation. When the SS/STP pin voltage increases to V_{STS} = 4.0 V or more, the power MOSFET is fixed off. When the SS/STP pin voltage is V_{STR} = 3.6 V or less after the external applied voltage is stopped, the IC starts oscillating again.

The SS/STP pin input voltage must be set less than 6 V.

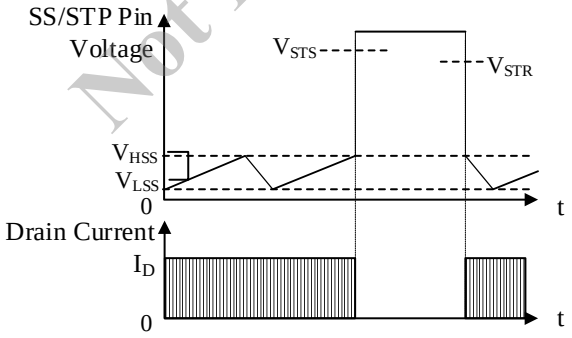

Figure 9-12. Operational Waveform of Drive Stop Function

9.8. Overcurrent Protection (OCP)

The IC has the pulse-by-pulse Overcurrent Protection (OCP). When the S/OCP pin voltage exceeds the OCP Threshold Voltage, V_{OCP} = 0.50 V, at every switching cycle, the OCP is activated. When the OCP is activated, the power MOSFET is turned off, resulting in suppressing the peak of drain current.

A high frequency switching current flows to the detection resistor. If the resistor with high internal inductance is used, the malfunctions may be caused. The resistor with low internal inductance and high surge capability must be selected.

In addition, when the IC malfunctions due to surges in switching operation, the RC filter is added to the S/OCP pin.

● **Design Example of Current Detection Resistor**

The value of the current detection resistor, R_{OCP}, is set according to the following calculation example in discontinuous operation as a reference. Since the R_{OCP} and the calculation example do not match in continuous operation, it is required to ultimately adjust by confirming the actual operation.

The peak drain current, I_{PEAK}, in discontinuous operation is calculated by the following equation.

$$I_{PEAK} = \frac{2 \times P_{OUT}}{\eta \times V_{IN} \times D} \quad (7)$$

Where:
V_{IN} is input voltage,
P_{OUT} is output power,
η is efficiency, and
D is duty cycle of the power MOSFET.

The relation between the power, P, and the drain current, I_D, is shown in the following equation.

$$P = \frac{1}{2} \times L \times {I_D}^2 \quad (8)$$

The drain current is proportional to $\sqrt{P}$. If the OCP is designed to operate at 130% of the rated load (the maximum output power at the minimum input voltage), the peak of drain current at the OCP operation point is about 114% ($\sqrt{130\%}$) of I_{PEAK} at the rated load.

The current detection resistor, R_{OCP}, is calculated by the following equation.

$$R_{OCP} = \frac{V_{OCP} \times \eta \times V_{IN(MIN)} \times D_{(MAX)}}{114\% \times 2 \times P_{OUT(MAX)}} \quad (9)$$

Where:
$D_{(MAX)}$ is the duty cycle at the minimum input voltage,
$V_{IN(MIN)}$ and the maximum output power, $P_{OUT(MAX)}$,
η is efficiency, and
V_{OCP} is the OCP Threshold Voltage (0.50 V).

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The waveform of the current flowing through the R_{OCP} becomes triangular in discontinuous operation. The RMS current is calculated by the following equation.

$$I_{RMS} = I_{PEAK} \times \sqrt{\frac{D_{(MAX)}}{3}} \quad (10)$$

The power consumption of R_{OCP} is calculated by the following equation.

$$P_{ROCP} = R_{OCP} \times {I_{RMS}}^2 \quad (11)$$

9.9. Overload Protection (OLP)

The IC has the Overload Protection (OLP). When the overload state (where the peak of drain current is limited by OCP, or the power MOSFET operates in the maximum duty cycle) continues for a certain time, t_{OLP}, the OLP is activated; and the power MOSFET oscillation is stopped. This reduces the stress of the power MOSFET and the secondary rectifier diode.

The delay time of the OLP, t_{OLP}, is determined by the capacitance of C_{SS} connected to the SS/STP pin. When C_{SS} is 0.01 µF, t_{OLP} becomes 38 ms. In another capacitance, the approximate value of t_{OLP} can be calculated by the following equation.

$$t_{OLP}(\text{ms}) = 38\ \text{ms} \times \frac{C_{SS}\ (\text{nF})}{0.01\ \mu\text{F}} \quad (12)$$

The soft start time in Section 9.3 should be taken into account in setting the C_{SS} capacitance.

The oscillation stop period of the power MOSFET is 7 × t_{OLP}. The power MOSFET repeats oscillation and stop on an 8 × t_{OLP} cycle until the overload state is dissolved.

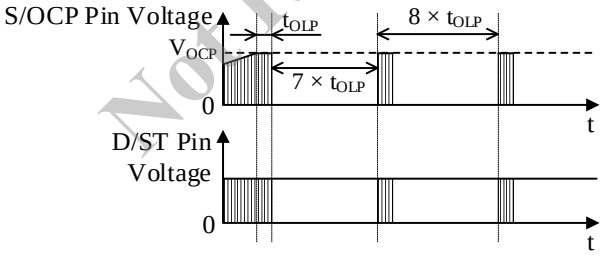

Figure 9-13. Overload Protection Operation

9.10. Thermal Shutdown (TSD)

The IC has the Thermal Shutdown (TSD). When the junction temperature of the IC reaches $T_{JH(TSD)}$ = 165 °C, TSD is activated; and the power MOSFET oscillation is stopped. When the junction temperature of the IC decreases to $T_{JL(TSD)}$ = 150 °C or lower due to the oscillation stop, TSD is released; and the power MOSFET oscillation is restarted.

TSD protects the IC from overheating in abnormal operation, and does not guarantee the operation including reliability for a state that the heat generation continues for a long time.

10. Design Notes

10.1. External Components

Components fit for the use condition should be used.

10.1.1. Input and Output Electrolytic Capacitor

It is required to apply proper derating to ripple current, voltage, and temperature rise.

Also, to reduce the ripple voltage, low ESR type for switching power supply is recommended.

10.1.2. VCC Pin Peripheral Circuit

In actual power supply circuits, when VCC pin voltage increases due to the output current, I_{OUT} (see Figure 10-1), the Overvoltage Protection (OVP) may be activated. This happens because C3 is charged to a peak voltage on the auxiliary winding, D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off. For alleviating C2 peak charging, it is effective to add the resistor, R_{CC}, of several tenths of ohms to several ohms, in series with D2 (see Figure 10-2). Adding the R_{CC} and the dummy resistor, R5, (see Section 9.4) is also effective.

The optimal value of R_{CC} should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

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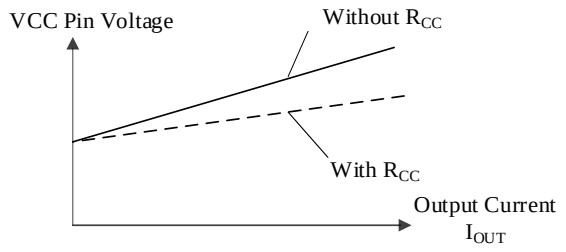

Figure 10-1. Output Current I_{OUT} vs. VCC Pin Voltage

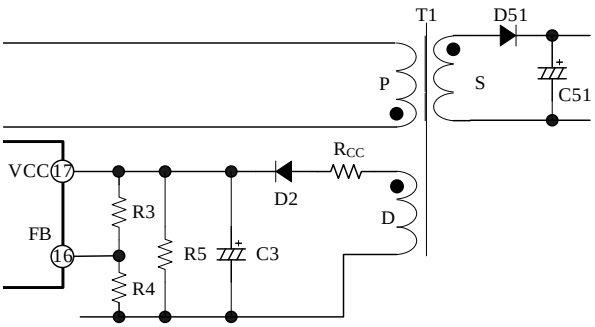

Figure 10-2. VCC Pin Peripheral Circuit

10.1.3. Secondary-side Rectifier Diode Peripheral Circuit

Figure 10-3 shows the peripheral circuit of the secondary rectifier diode, D51. To reduce the noise of D51, add a ceramic capacitor, C_{SD}, in parallel with D51 as shown in Figure 10-3 as needed. Also, if there is abnormal ringing in the drain current waveform on the primary-side, R_{SD} should be added to suppress this ringing and stabilizes power supply operation.

Care must be taken for the part temperatures of C_{SD} and R_{SD}.

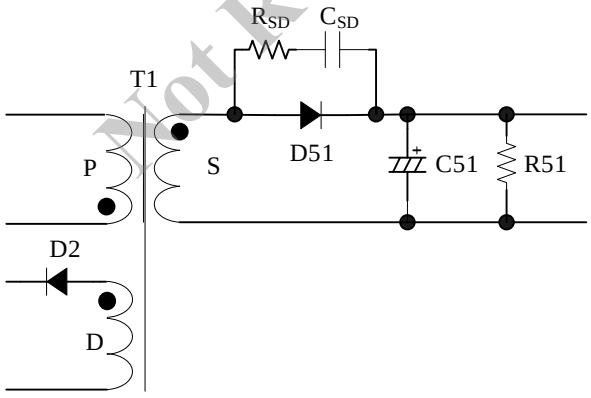

Figure 10-3. Secondary Rectifier Diode Peripheral Circuit

10.1.4. Transformer

It is required to set design margin properly for temperature rise due to copper loss and iron loss. Since the switching current contains high frequency components, the skin effect must be taken into account.

For this reason, the wire diameter of the winding for the transformer should be selected taking the RMS of the operating current into account, and the current density should be 4 A/mm^2 to 6 A/mm^2. If the further countermeasures against temperature are required due to such as the skin effect, the following contents should be taken into account to increase the winding surface area.

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire diameter.

Also, since the change rate of output voltage increases in the following cases, care must be taken for the winding position of the auxiliary winding, D, in transformer design.

- When the coupling between the primary-side winding and the secondary-side winding of the transformer is poor (e.g., low output voltage specifications or high output current specifications).
- When the coupling between the auxiliary winding, D, and output winding is poor.

10.2. PCB Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, the trace layouts and component placements on the PCB play an important role in circuit designing. High frequency and high voltage current loops must be as small as possible with wide trace in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

In addition, the following contents should be taken into account in the design of PCB trace layout.

Figure 10-4 shows the peripheral circuit example around the IC.

(1) Main Circuit
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible. If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 µF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground
Since the operation of the IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should

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be separated from main trace and connected as close to the current detection resistor, R2, as possible.

(3) VCC Pin

Since the trace of C3 from the auxiliary winding is a trace in which high frequency current flows, it should be as wide trace and small loop as possible. The traces connecting from C3 to the VCC pin, the GND pin, R3, R4, and R5 must be designed so that they do not run cross or parallel with the high-frequency current flowing trace .

If C3 and the IC are distant from each other, placing a capacitor such as film capacitor, C_P (about 0.1 µF to 1.0 µF), close to the VCC pin and the GND pin is recommended.

(4) Current Detection Resistor, R2

R2 should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be close to R2.

(5) Secondary Rectifier Smoothing Circuit

This is the secondary main circuit trace carrying the switching current. This trace must be as wide layout and small loop as possible. If the impedance of this trace is lowered, the surge voltage at turning off the power MOSFET is decreased. The proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(6) Thermal Considerations

Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, care should be taken for thermal design. The heat is released from the D/ST pin trace including an exposed pad. Therefore, the trace must be designed as wide as possible.

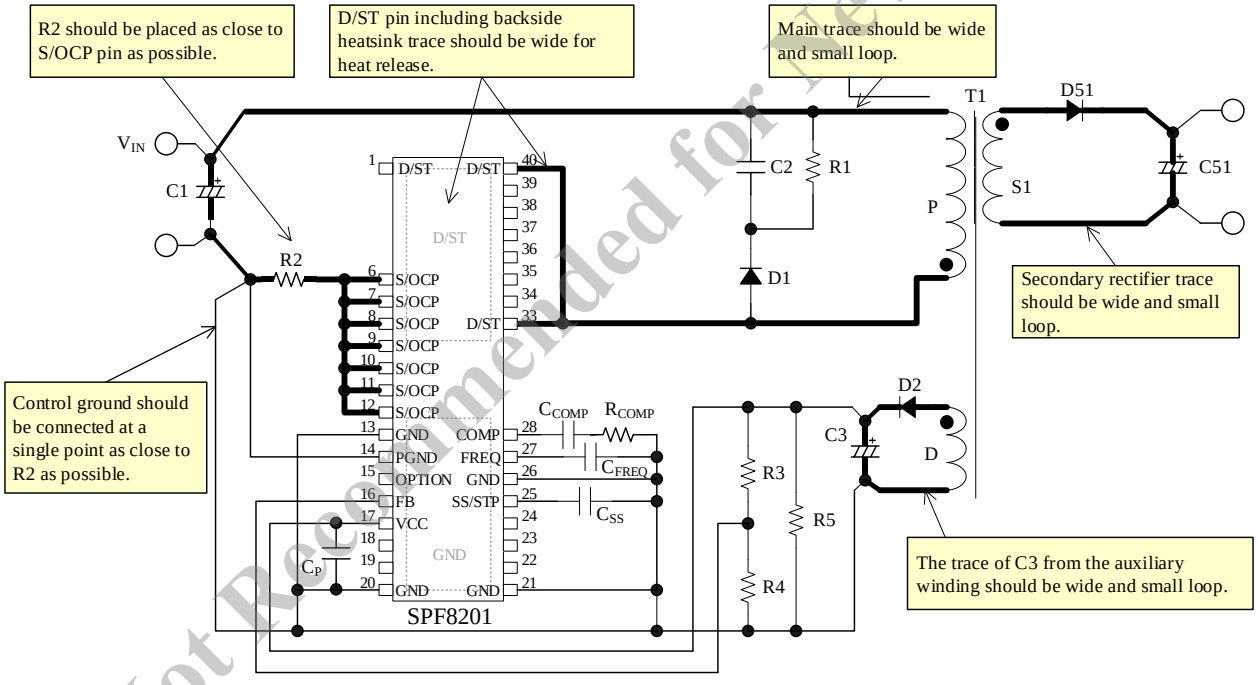

Figure 10-4. Peripheral Circuit Example around the IC

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11. Pattern Layout Example

The following show the three outputs PCB pattern layout example and the schematic of circuit using SPF8201. The PCB pattern layout example is made usable both primary side detection and secondary side detection methods.

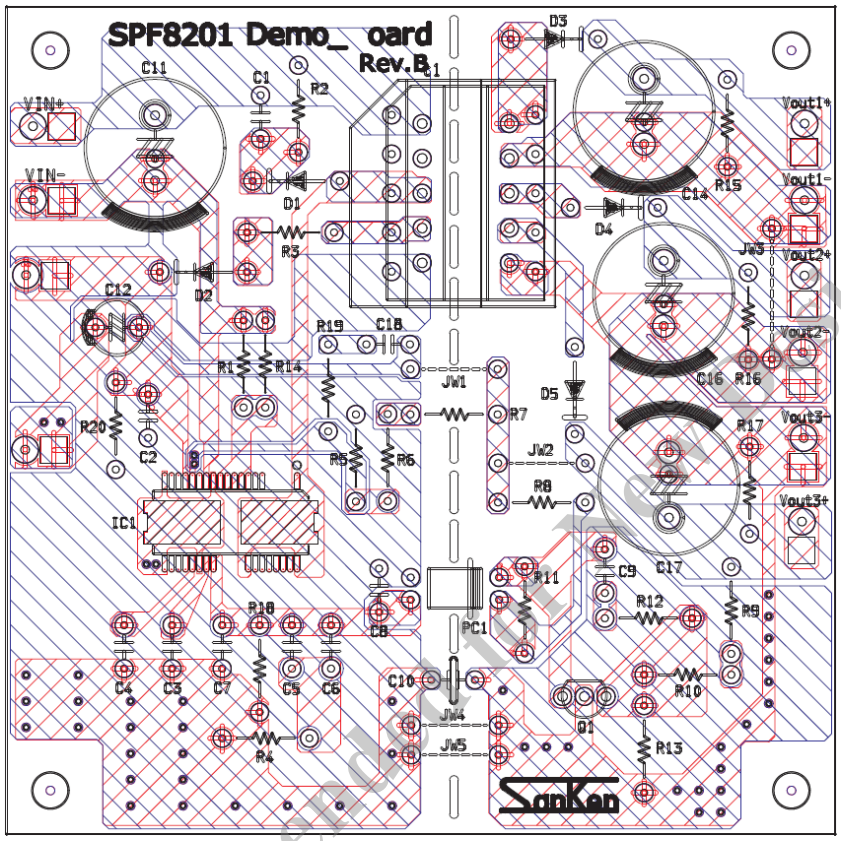

Figure 11-1. 2-layer PCB Layout Example

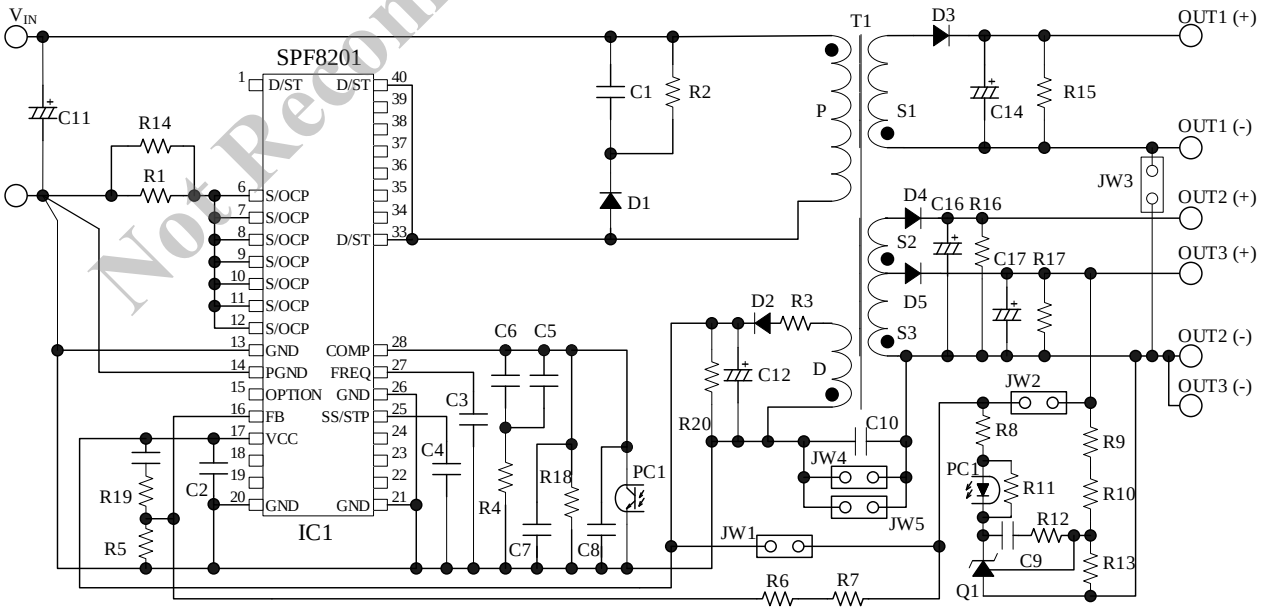

Figure 11-2. Circuit Schematic for the PCB Layout Example

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12. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

12.1. Power supply specification

IC	SPF8201
Input Voltage	100 VDC to 400 VDC
Maximum Output Power	5.5 W
Output 1	15 V, 0.3 A
Output 2	—
Output 2	5 V, 0.2 A

12.2. Circuit schematic

See Figure 11-2.

12.3. Bill of materials

Symbol	Part type	Ratings	Recommended Sanken Parts	Symbol	Part type	Ratings	Recommended Sanken Parts
C1	Ceramic	0.01 µF, 630 V		JW4	General	Open	
C2	Ceramic	0.1 µF, 50 V		JW5	General	Open	
C3	Ceramic	330 pF, 50 V		PC1	Photo-coupler	Open	
C4	Ceramic	0.047 µF, 50 V		Q1	Shunt regulator	Open	
C5	Ceramic	0.1 µF, 50 V		R1	General	1.5 Ω, 1/2 W	
C6	Ceramic	Open		R2	General	150 kΩ, 1/2 W	
C7	Ceramic	0.01 µF, 50 V		R3	General	33 Ω, 1/2 W	
C8	Ceramic	Open		R4	General	22 kΩ, 1/4 W	
C9	Ceramic	Open		R5	General	2.2 kΩ, 1/4 W	
C10	Ceramic	470 pF, 2 kV		R6	General	13 kΩ, 1/4 W	
C11	Electrolytic	6.8 µF, 450 V		R7	General	1.2 kΩ, 1/4 W	
C12	Electrolytic	47 µF, 35 V		R8	General	Open	
C14	Electrolytic	470 µF, 25 V		R9	General	Open	
C16	Electrolytic	Open		R10	General	Open	
C17	Electrolytic	1000 µF, 10 V		R11	General	Open	
C18	Ceramic	1 µF, 50 V		R12	General	Open	
D1	Fast recovery	1000 V, 0.5 A	EG01C	R13	General	Open	
D2	Fast recovery	400 V, 0.7 A	EG01	R14	General	Open	
D3	Fast recovery	400 V, 1 A		R15	General	10 kΩ, 1/4 W	
D4	Fast recovery	Open		R16	General	Open	
D5	Fast recovery	200 V, 1 A		R17	General	10 kΩ, 1/4 W	
IC1	—		SPF8201	R18	General	33 kΩ, 1/4 W	
JW1	General	560 Ω, 1/4 W		R19	General	10 kΩ, 1/4 W	
JW2	General	Open		R20	General	22 kΩ, 1/4 W	
JW3	General	0 Ω		T1	Transformer	See Section 12.4	

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12.4. Transformer specification

- Primary Inductance, L_P: 518 µH
- Core Size: EER-28
- Al-value: 245 nH/N^2 (Center gap of about 0.56 mm)
- Winding Specification: See Table 12-1 and Figure 12-1

Table 12-1. Winding Specification

Winding	Symbol	Number of Turns (T)	Wire Diameter (mm)	Construction
Primary Winding	P1	46	φ 0.26	Solenoid winding
Primary Winding	P2	59	φ 0.26	Solenoid winding
Auxiliary Winding	D	31	φ 23	Space winding
Output 1 Winding	S1	24	φ 0.32 × 2	Solenoid winding
Output 2 Winding	S2	—	—	—
Output 3 Winding	S3	9	φ 0.26	Space winding

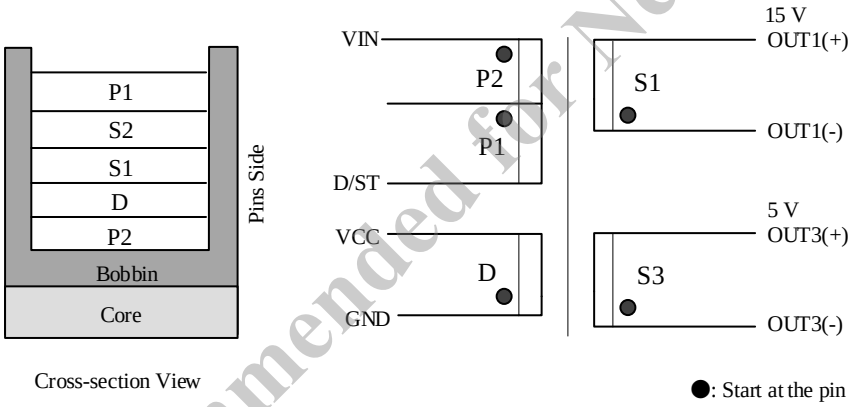

Figure 12-1. Winding Structure

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DSGN-AEZ-16003

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