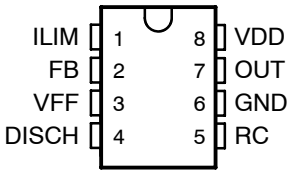
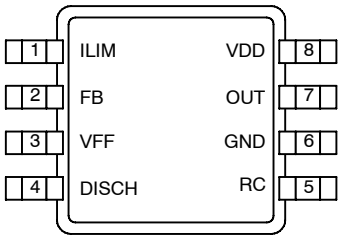
SLUS473B – NOVEMBER 1999 – REVISED OCTOBER 2010

- **Greater Than 4-MHz Operation**
- **Integrated Oscillator / Voltage Feed Forward Compensation**
- **>4:1 Input Voltage Range**
- **25-ns Current Limit Delay**
- **Programmable Maximum Duty Cycle Clamp**
- **Optocoupler Interface**
- **50-μA Start-Up Current**
- **4.2-mA Operating Current @ 1 MHz**
- **Smallest Footprint of the 8-pin MSOP Package Minimizes Board Area and Height**

D, OR P PACKAGE
(TOP VIEW)



DGK PACKAGE
(TOP VIEW)



description

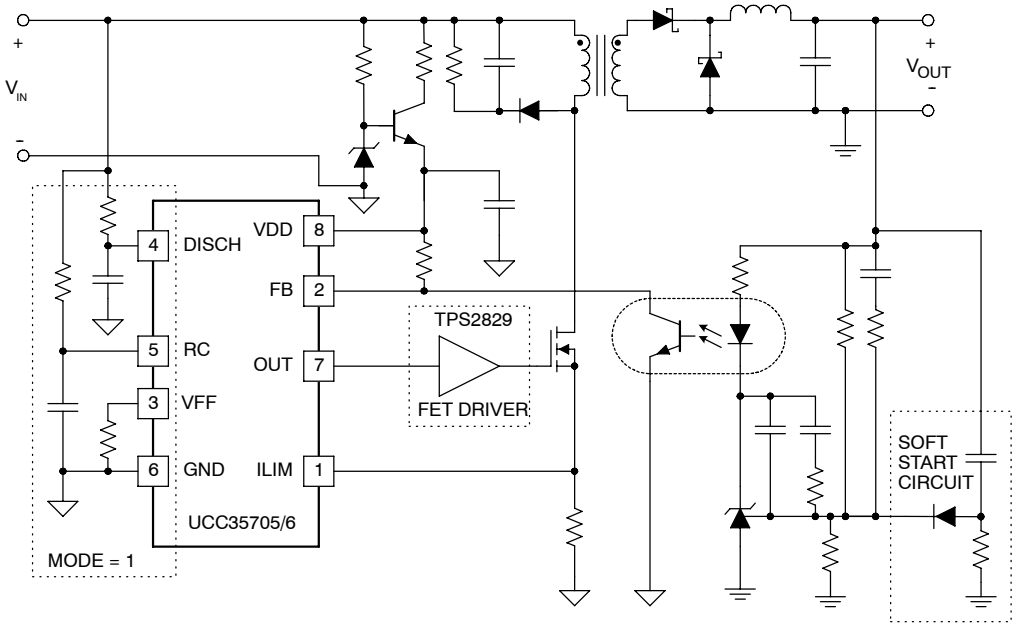
The UCC35705 and UCC35706 devices are 8-pin voltage mode primary side controllers with fast over-current protection. These devices are used as core high-speed building blocks in high performance isolated and non-isolated power converters.

UCC35705/UCC35706 devices feature a high speed oscillator with integrated feed-forward compensation for improved converter performance. A typical current sense to output delay time of 25 ns provides fast response to overload conditions. The IC also provides an accurate programmable maximum duty cycle clamp for increased protection which can also be disabled for the oscillator to run at maximum possible duty cycle.

Two UVLO options are offered. The UCC35705 with lower turn-on voltage is intended for dc-to-dc converters while the higher turn-on voltage and the wider UVLO range of the UCC35706 is better suited for offline applications.

The UCC35705/UCC35706 family is offered in 8-pin MSOP (DGK), SOIC (D) and PDIP (P) packages.

typical application schematic



UDG-99181

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage . . . . . 15 V
Input voltage (VFF,RC,ILIM) . . . . . 7 V
Input voltage (FB) . . . . . 15 V
Input current (DISCH) . . . . . 1 mA
Output current (OUT) dc . . . . . ±20 mA
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Junction temperature, T_J . . . . . –55°C to 150°C
Lead temperature (soldering, 10 sec.) . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Power Supply Control Data Book (TI Literature Number SLUD003)* for thermal limitations and considerations of packages.

AVAILABLE OPTIONS

$T_A = T_J$	Packaged Devices			
	UVLO Option	SOIC-8 Small Outline (D)†	PDIP-8 Plastic Dip (P)	MSOP-8 Small Outline (DGK)†
–40°C to 85°C	8.8V/8V	UCC25705D	UCC25705P	UCC25705DGK
	12V/8V	UCC25706D	UCC25706P	UCC25706DGK
0°C to 70°C	8.8V/8V	UCC35705D	UCC35705P	UCC35705DGK
	12V/8V	UCC35706D	UCC35706P	UCC35706DGK

† D (SOIC–8) and DGK (MSOP–8) packages are available taped and reeled. Add R suffix to device type (e.g. UCC35705DR) to order quantities of 2500 devices per reel for SOIC-8 and 2000 devices per reel for the MSOP-8.

electrical characteristics, V_{DD} = 11 V, V_{IN} = 30 V, R_T = 47 k, R_{DISCH} = 400 k, R_{FF} = 14 k, C_T = 220 pF, C_{VDD} = 0.1 μF, and no load on the outputs, 0°C ≤ T_A ≤ 70°C for the UCC3570x and –40°C ≤ T_A ≤ 85°C for the UCC2570x, $T_A = T_J$, (unless otherwise specified)

UVLO section (UCCx5705)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold		8.0	8.8	9.6	V
Stop threshold		7.4	8.2	9.0	V
Hysteresis		0.3	0.6	1.0	V

UVLO section (UCCx5706)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold		11.2	12.0	12.8	V
Stop threshold		7.2	8.0	8.8	V
Hysteresis		3.5	4.0	4.5	V

supply current section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start-up current	V_{DD} = UVLO start – 1 V, V_{DD} comparator off		30	90	μA
I_{DD} active	V_{DD} comparator on, oscillator running at 1 MHz		4.2	5.0	mA

electrical characteristics, V_{DD} = 11 V, V_{IN} = 30 V, R_T = 47 k, R_{DISCH} = 400 k, R_{FF} = 14 k, C_T = 220 pF, C_{VDD} = 0.1 μF, and no load on the outputs, 0°C ≤ T_A ≤ 70°C for the UCC3570x and –40°C ≤ T_A ≤ 85°C for the UCC2570x, T_A = T_J, (unless otherwise specified)

line sense section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Low line comparator threshold		0.95	1.00	1.05	V
Input bias current (VFF)		–100		100	nA

oscillator section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	VFF = 1.2 V to 4.8 V	0.9	1.0	1.1	MHz
CT peak voltage	VFF = 1.2 V, See Note 1		1.2		V
	VFF = 4.8 V, See Note 1		4.8		V
CT valley voltage	See Note 1		0		V

NOTE 1: Ensured by design. Not production tested.

current limit section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current		0.2	–0.2	–1	μA
Current limit threshold		180	200	220	mV
Propagation delay, ILIM to OUT	50 mV overdrive		25	35	ns

pulse width modulator section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FB input impedance	V_{FB} = 3 V	30	50	90	kΩ
Minimum duty cycle	V_{FB} < 2 V			0	%
Maximum duty cycle	V_{FB} = V_{DD}, F_{OSC} = 1 MHz	70	75	80	%
	V_{DISCH} = 0 V, F_{OSC} = 1 MHz		93		%
PWM gain	VFF = 2.5 V, MODE = 1		12		%/V
Propagation delay, PWM to OUT			65	120	ns

output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOH	I_{OUT} = –5 mA, V_{DD} – output		0.3	0.6	V
VOL	I_{OUT} = 5 mA		0.15	0.4	V
Rise time	C_{LOAD} = 50 pF		10	25	ns
Fall time	C_{LOAD} = 50 pF		10	25	ns

pin descriptions

DISCH: A resistor to VIN sets the oscillator discharge current programming a maximum duty cycle. When grounded, an internal comparator switches the oscillator to a quick discharge mode. A small 100-pF capacitor between DISCH and GND may reduce oscillator jitter without impacting feed-forward performance. I_{DISCH} must be between 25 μA and 250 μA over the entire V_{IN} range.

FB: Input to the PWM comparator. This pin is intended to interface with an optocoupler. Input impedance is 50-kΩ typical.

GND: Ground return pin.

ILIM: Provides a pulse-by-pulse current limit by terminating the PWM pulse when the input is above 200 mV. This provides a high speed (25 ns typical) path to reset the PWM latch, allowing for a pulse-by-pulse current limit.

OUT: The output is intended to drive an external FET driver or other high impedance circuits, but is not intended to directly drive a power MOSFET. This improves the controller's noise immunity. The output resistance of the PWM controller, typically 60 Ω pull-up and 30 Ω pull-down, will result in excessive rise and fall times if a power MOSFET is directly driven at the speeds for which the UCC35705/6 is optimized.

RC: The oscillator can be configured to provide a maximum duty cycle clamp. In this mode the on–time is set by RT and CT, while the off-time is set by RDISCH and CT. Since the voltage ramp on CT is proportional to VIN, feed-forward action is obtained. Since the peak oscillator voltage is also proportional to VIN, constant frequency operation is maintained over the full power supply input range. When the DISCH pin is grounded, the duty cycle clamp is disabled. The RC pin then provides a low impedance path to ground CT during the off time.

VDD: Power supply pin. This pin should be bypassed with a 0.1-μF capacitor for proper operation. The undervoltage lockout function of the UCC35705/6 allows for a low current startup mode and ensures that all circuits become active in a known state. The UVLO thresholds on the UCC35705 are appropriate for a dc-to-dc converter application. The wider UVLO hysteresis of the UCC35706 (typically 4 V) is optimized for a bootstrap startup mode from a high impedance source.

VFF: The feed-forward pin provides the controller with a voltage proportional to the power supply input voltage. When the oscillator is providing a duty cycle clamp, a current of $2 \times I_{DISCH}$ is sourced from the VFF pin. A single resistor RFF between VFF and GND then set VFF to:

$$VFF \approx VIN \times \left(\frac{2 \times R_{FF}}{2 \times R_{FF} + R_{DISCH}} \right)$$

When the DISCH pin is grounded and the duty cycle clamp is not used, the internal current source is disabled and a resistor divider from VIN is used to set VFF. In either case, when the voltage on VFF is less than 1.0 V, both the output and oscillator are disabled.

pin descriptions (continued)

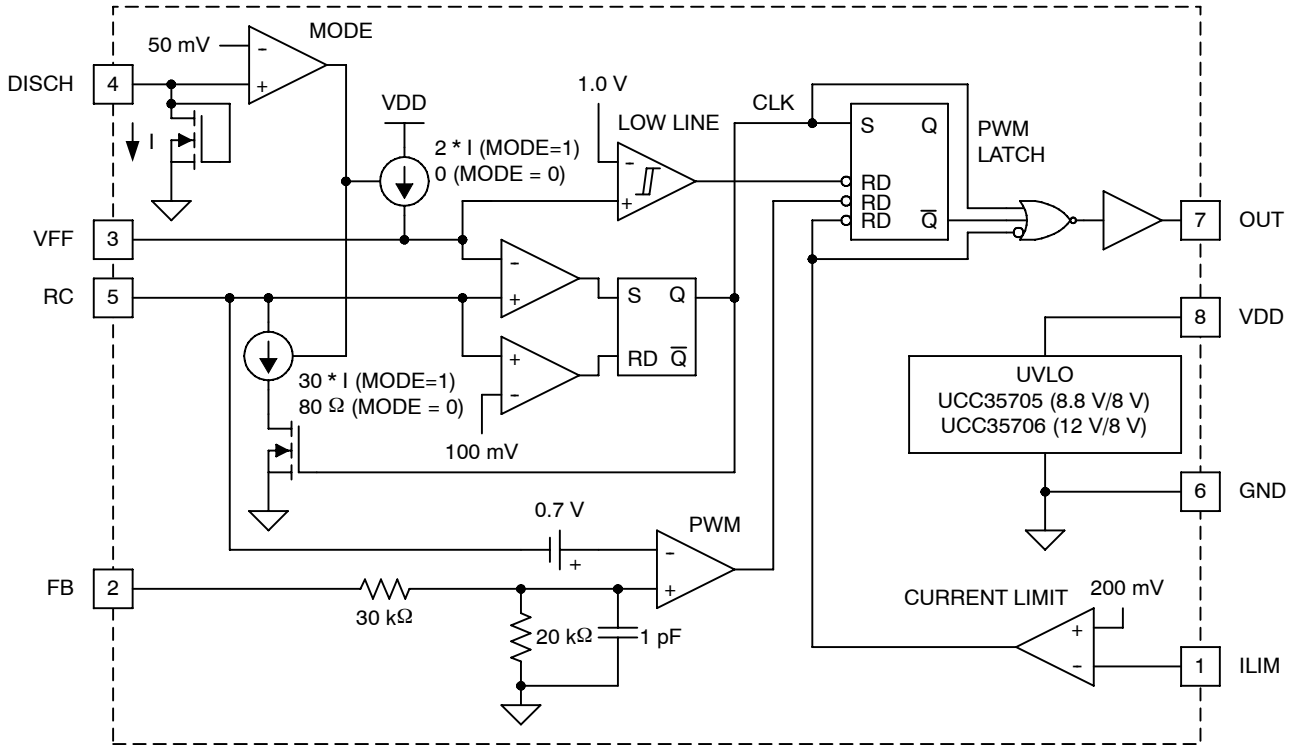

Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION

oscillator and PWM

The oscillator can be programmed to provide a duty cycle clamp or be configured to run at the maximum possible duty cycle.

The PWM latch is set during the oscillator discharge and is reset by the PWM comparator when the C_T waveform is greater than the feedback voltage. The voltage at the FB pin is attenuated before it is applied to the PWM comparator. The oscillator ramp is shifted by approximately 0.65-V at room temperature at the PWM comparator. The offset has a temperature coefficient of approximately –2 mV/°C.

The ILIM comparator adds a pulse by pulse current limit by resetting the PWM latch when V_{ILIM} > 200 mV. The PWM latch is also reset by a low line condition (V_{FF} <1.0 V).

All reset conditions are dominant; asserting any output will force a zero duty cycle output.

oscillator with duty cycle clamp (MODE = 1)

The timing capacitor CT is charged from ground to VFF through RT. The discharge path is through an on-chip current sink that has a value of 30 × I_{DISCH}, where I_{DISCH} is the current through the external resistor RDISCH. Since the charge and discharge currents are both proportional to VIN, their ratio, and the maximum duty cycle remains constant as VIN varies.

FUNCTIONAL DESCRIPTION

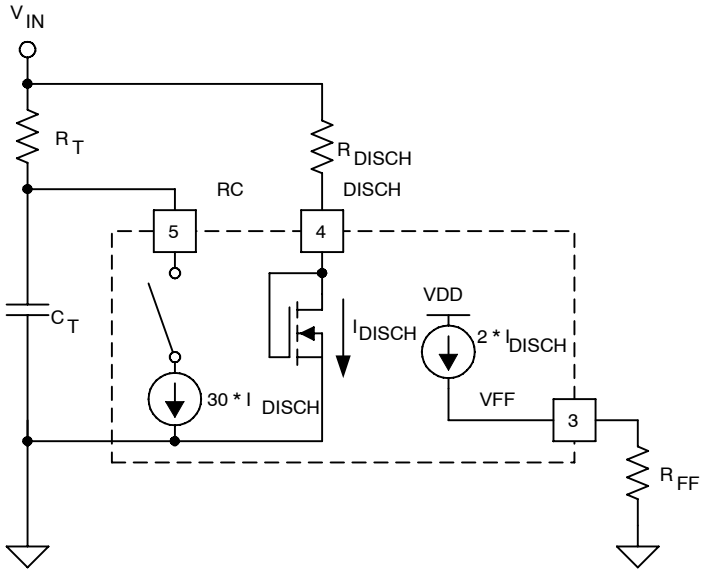

Figure 2. Duty Cycle Clamp (MODE = 1)

The on-time is approximately:

$$T_{ON} = \propto \times R_T \times C_T \quad \text{where } \propto = \frac{V_{FF}}{V_{IN}} \approx \frac{2 \times R_{FF}}{R_{DISCH}}$$

The off-time is:

$$T_{OFF} = \propto \times \frac{C_T \times \left(R_T \times R_{DISCH}\right)}{\left(30 \times R_T - R_{DISCH}\right)}$$

The frequency is:

$$f = \left(\frac{1}{\propto \times R_T \times C_T}\right) \times \frac{1}{1 + \frac{R_{DISCH}}{\left(30 \times R_T - R_{DISCH}\right)}}$$

The maximum duty cycle is:

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \left(1 - \frac{R_{DISCH}}{30 \times R_T}\right)$$

FUNCTIONAL DESCRIPTION

component selection for oscillator with duty cycle clamp (MODE = 1)

For a power converter with the following specifications:

- $V_{IN(min)}$ = 18 V
- $V_{IN(max)}$ = 75 V
- $V_{IN(shutdown)}$ = 15 V
- F_{OSC} = 1 MHz
- D_{MAX} = 0.78 at $V_{IN(min)}$

In this mode, the on-time is approximately:

- $T_{ON(max)}$ = 780 ns
- $T_{OFF(min)}$ = 220 ns
- $V_{FF(min)} = \frac{18}{15} = 1.20$ V

(1) Pick C_T = 220 pF.

(2) Calculate R_T.

$$R_T = \frac{V_{IN(min)} \times T_{ON(max)}}{V_{FF(min)} \times C_T}$$

R_T = 51.1 kΩ

(3) R_{DISCH}

$$R_{DISCH} = \frac{30 \times R_T}{1 + \left[\frac{\left(\frac{V_{FF(min)}}{V_{IN(min)}} \right) \times R_T \times C_T}{T_{OFF(min)}} \right]}$$

R_{DISCH} = 383 kΩ.

I_{DISCH} must be between 25 μA and 250 μA over the entire VIN range.

With the calculated values, I_{DISCH} ranges from 44 μA to 193 μA, within the allowable range. If I_{DISCH} is too high, C_T must be decreased.

(4) R_{FF}

$$R_{FF} = \frac{V_{FF(min)} \times R_{DISCH}}{2 \times \left(V_{IN(min)} - 1 \right)}$$

The nearest 1% standard value to the calculated value is 13.7 k.

FUNCTIONAL DESCRIPTION

oscillator without duty cycle clamp (MODE = 0)

In this mode, the timing capacitor is discharged through a low impedance directly to ground. The DISCH pin is externally grounded. A comparator connected to DISCH senses the ground connection and disables both the discharge current source and VFF current source. A resistor divider is now required to set VFF.

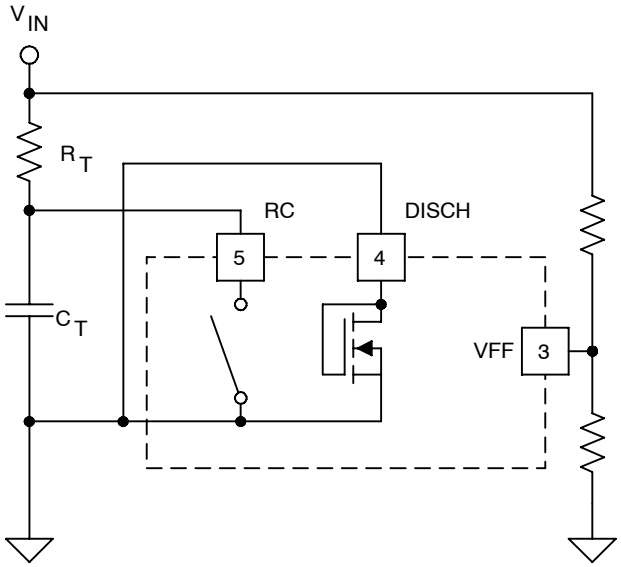

Figure 3. Ocsillator Without Clamp (MODE = 0)

In this mode, the on-time is approximately:

$$T_{ON} = \propto \times R_T \times C_T \quad \text{where} \propto = \frac{V_{FF}}{V_{IN}}$$

The off-time is:

$$T_{OFF} \approx 75 \text{ ns}$$

The frequency is:

$$f = \frac{1}{\propto \times R_T \times C_T + 75 \text{ ns}}$$

FUNCTIONAL DESCRIPTION

component selection for oscillator without duty cycle clamp (MODE = 0)

For a power converter with the following specifications:

- $V_{IN(min)}$ = 18 V
- $V_{IN(max)}$ = 75 V
- $V_{IN(shutdown)}$ = 15 V
- F_{OSC} = 1 MHz

With these specifications,

$$V_{FF(min)} = \frac{18}{15} = 1.2\ V$$

(1) Pick C_T = 220 pF

(2) Calculate R_T.

$$R_T = \frac{\frac{V_{IN(min)}}{V_{FF(min)}} \times \left(\frac{1}{F_{OSC}} - 75\ ns\right)}{C_T}$$

TYPICAL CHARACTERISTICS

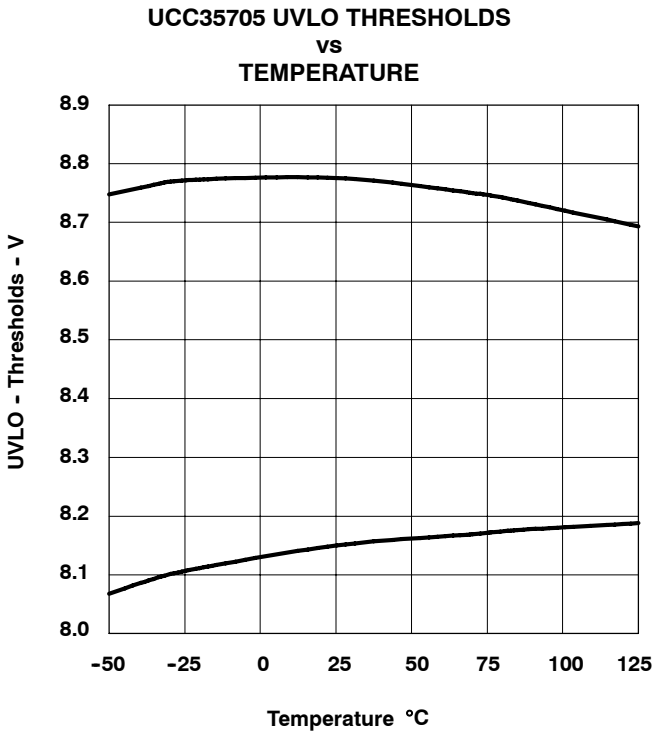

Figure 4

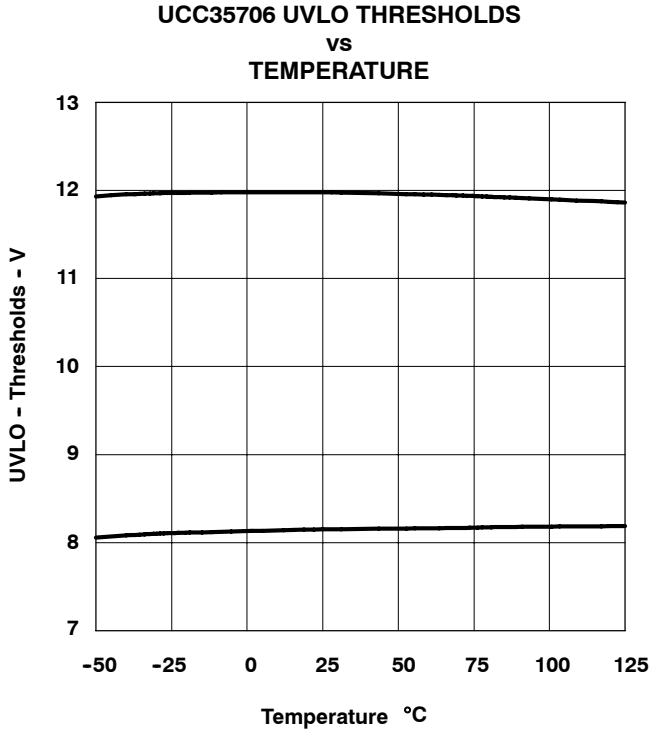

Figure 5

TYPICAL CHARACTERISTICS

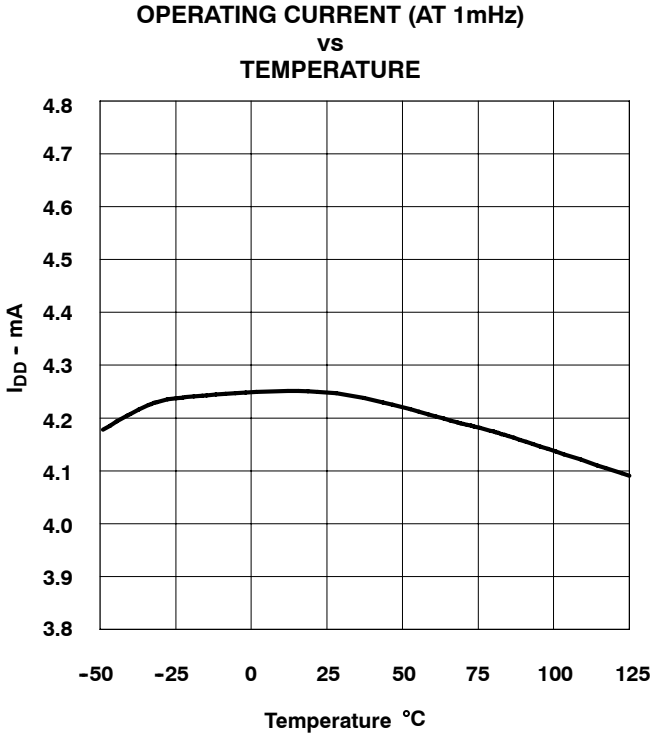

Figure 6

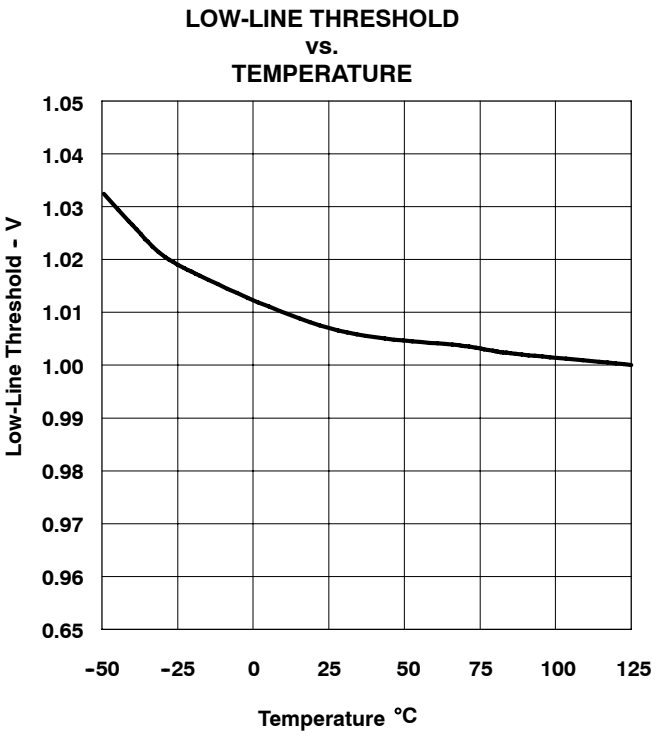

Figure 7

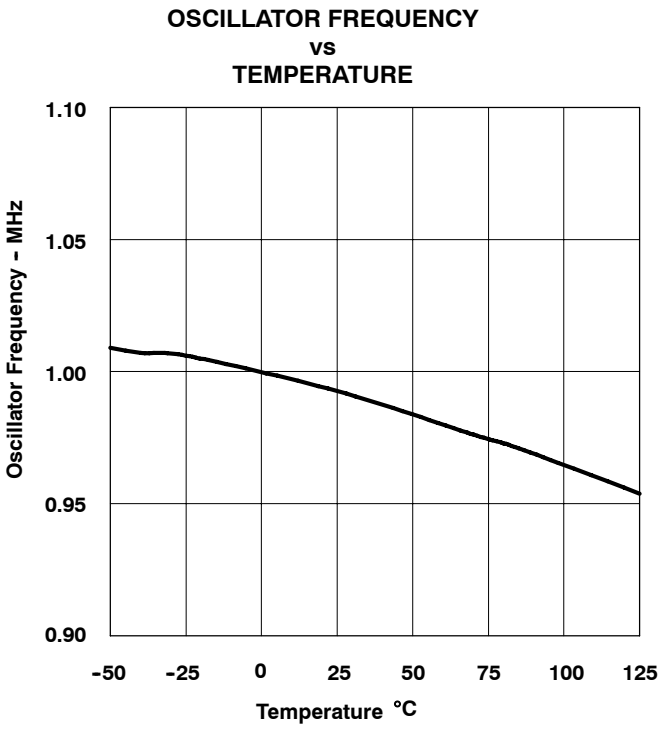

Figure 8

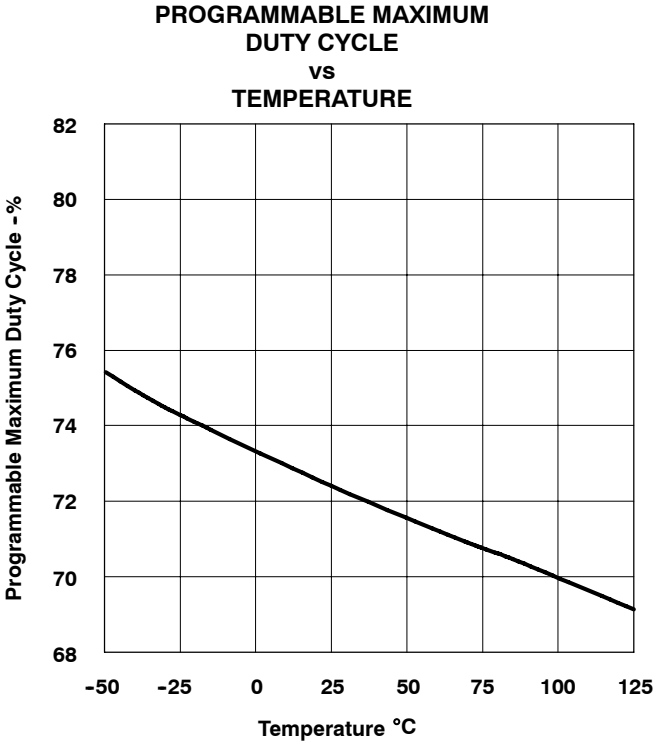

Figure 9

TYPICAL CHARACTERISTICS

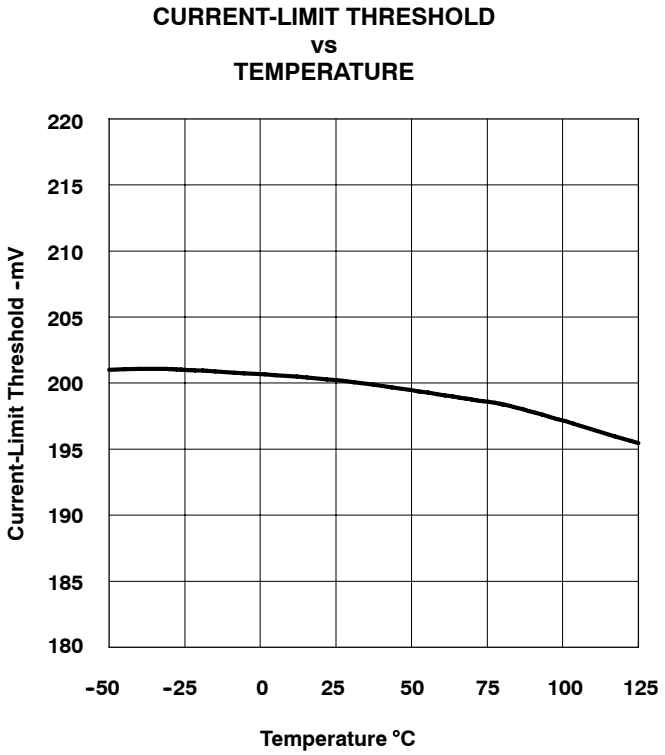

Figure 10

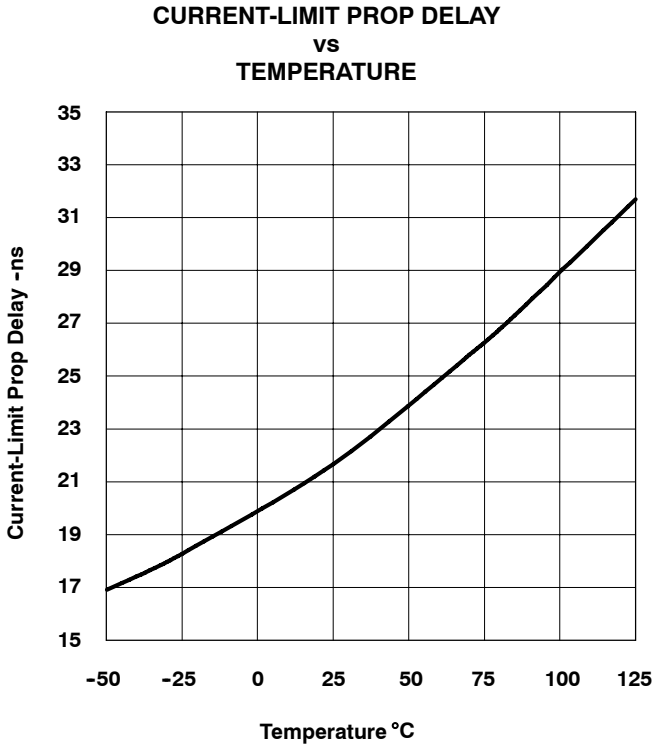

Figure 11

Revision History

Revision SLUS473A, March 2001 to SLUS473B:

- Modified "T_{OFF}" and "f" equation on page 6.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC25705D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25705D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25705DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25705DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25705DGKTR	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25705DGKTR.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25705DTR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25705DTR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25705
UCC25706D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25706
UCC25706D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25706
UCC25706DGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 85	25706
UCC35705D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35705
UCC35705D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35705
UCC35705DGK	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	35705
UCC35705DGK.A	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	35705
UCC35705DGKG4	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	35705
UCC35705DTR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35705
UCC35705DTR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35705
UCC35706D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35706
UCC35706D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35706
UCC35706DGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	0 to 70	35706

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC25706 :

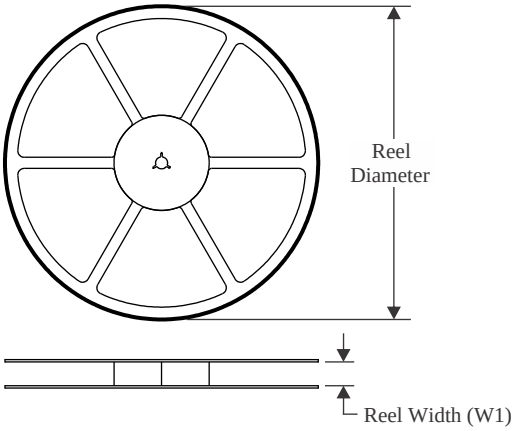
- Automotive : UCC25706-Q1

NOTE: Qualified Version Definitions:

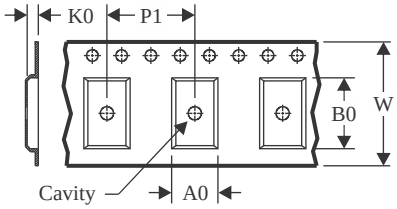
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

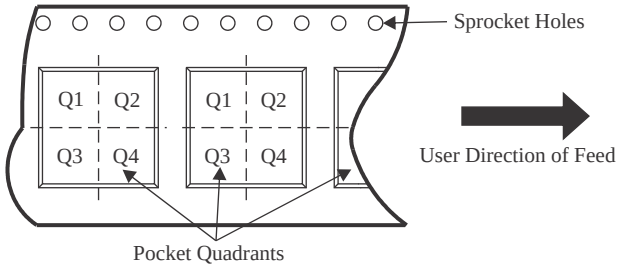


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

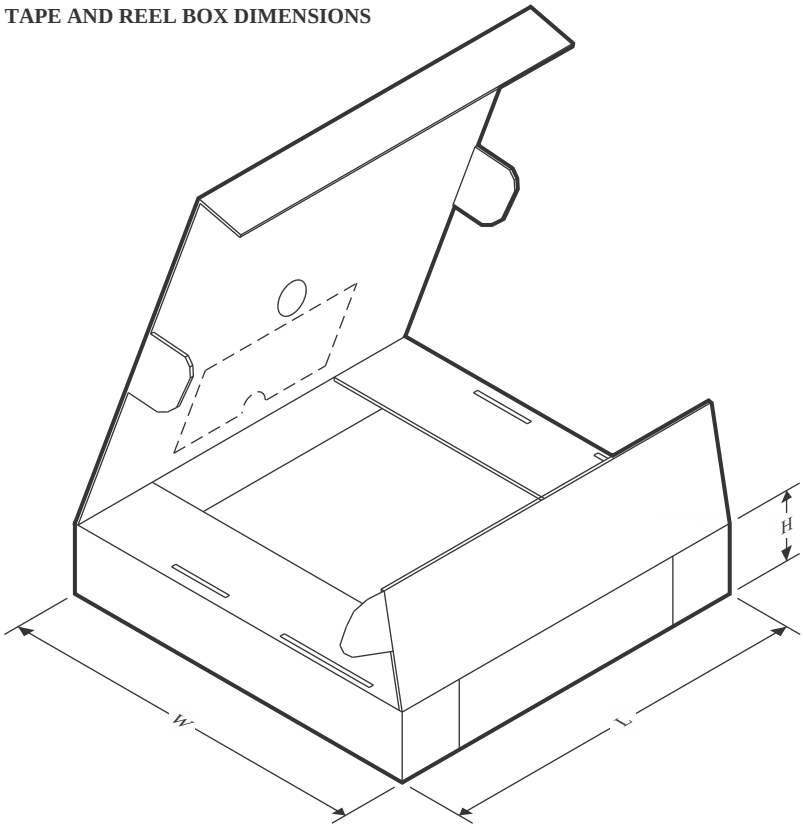
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC35705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

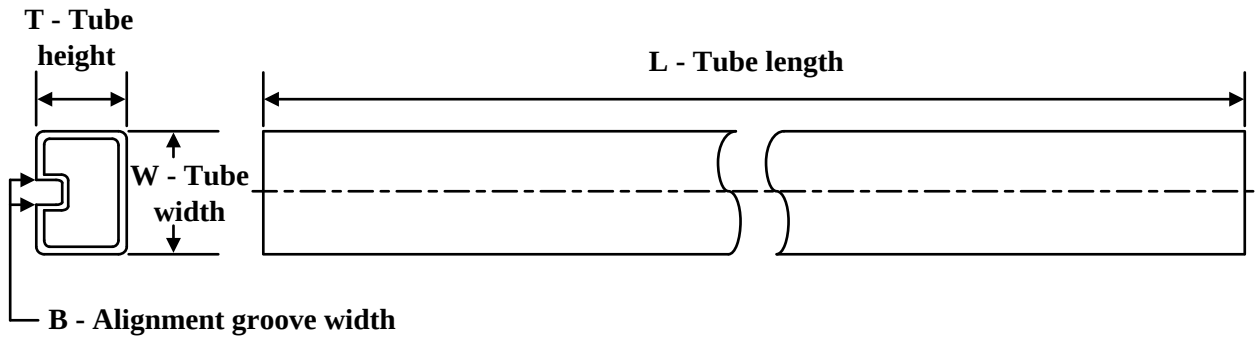
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25705DTR	SOIC	D	8	2500	353.0	353.0	32.0
UCC35705DTR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

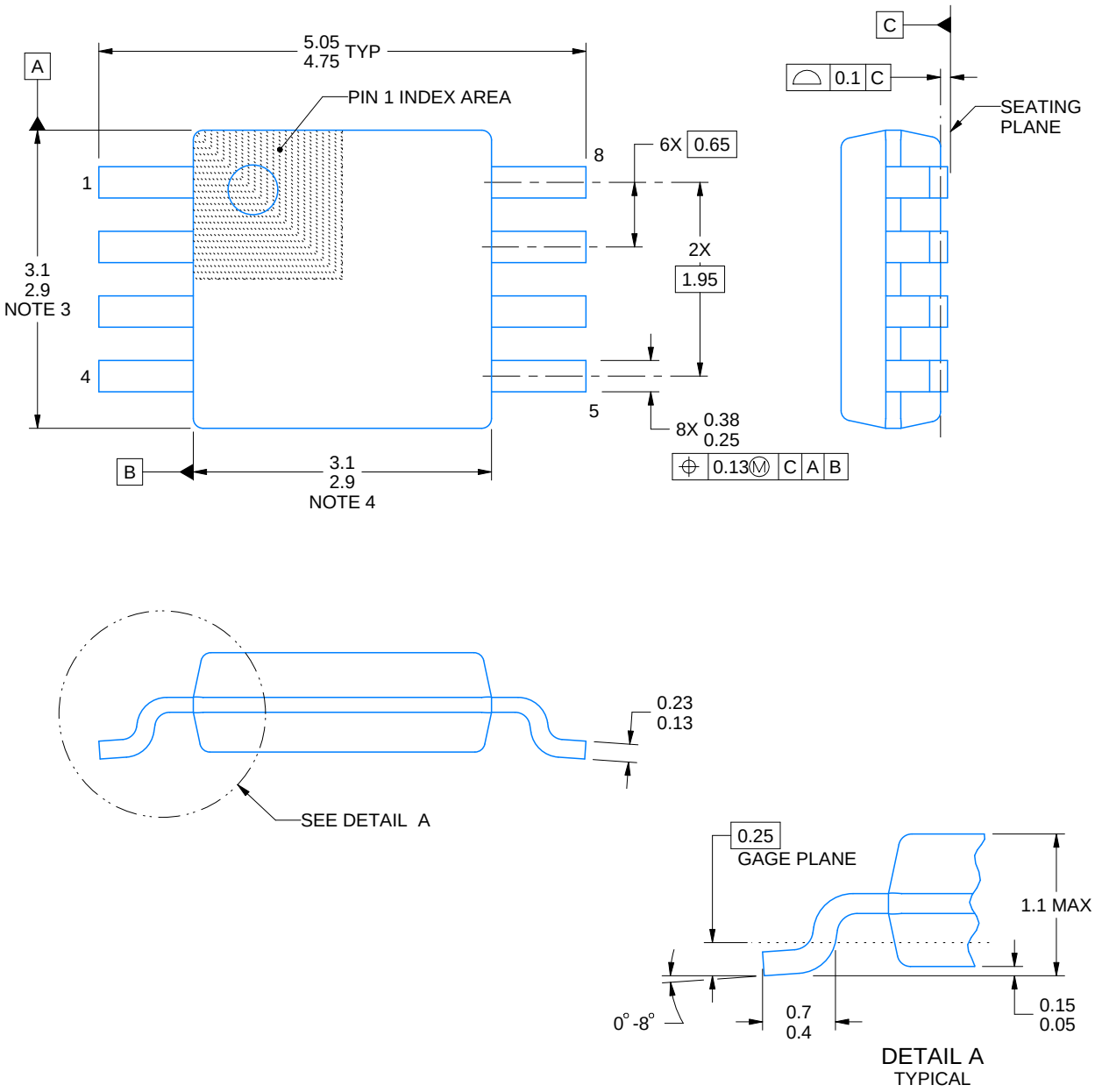
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC25705D	D	SOIC	8	75	506.6	8	3940	4.32
UCC25705D.A	D	SOIC	8	75	506.6	8	3940	4.32
UCC25705DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC25705DGK.A	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC25706D	D	SOIC	8	75	506.6	8	3940	4.32
UCC25706D.A	D	SOIC	8	75	506.6	8	3940	4.32
UCC35705D	D	SOIC	8	75	506.6	8	3940	4.32
UCC35705D.A	D	SOIC	8	75	506.6	8	3940	4.32
UCC35705DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC35705DGK.A	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC35705DGKG4	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC35706D	D	SOIC	8	75	506.6	8	3940	4.32
UCC35706D.A	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

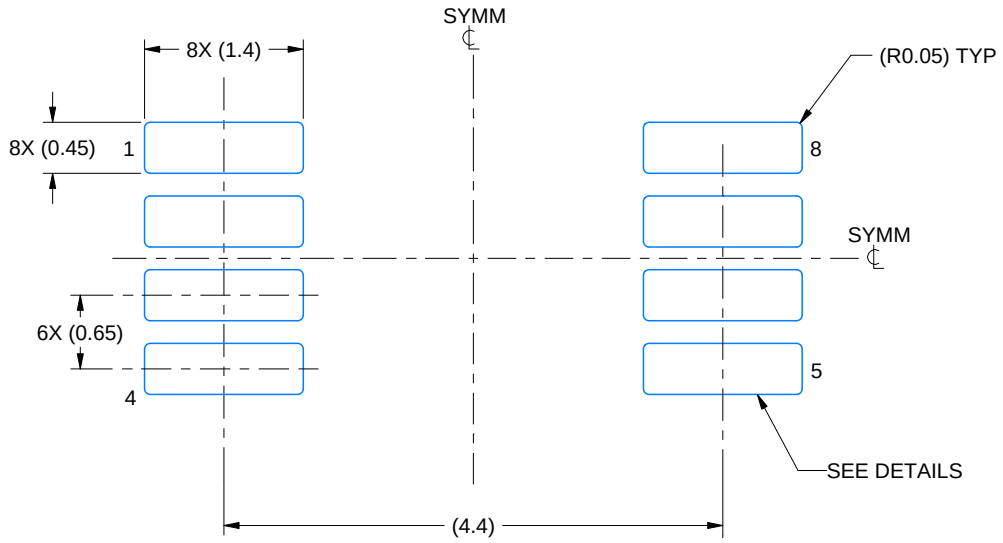
SMALL OUTLINE PACKAGE



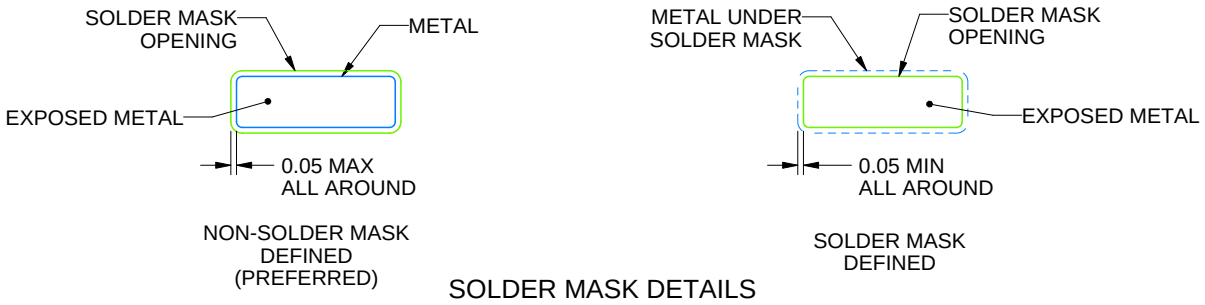
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

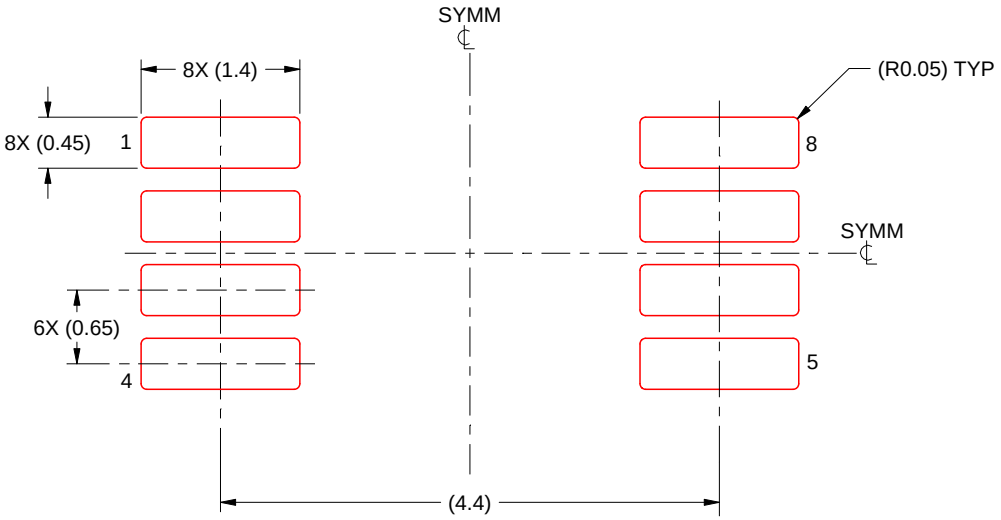


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

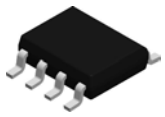


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

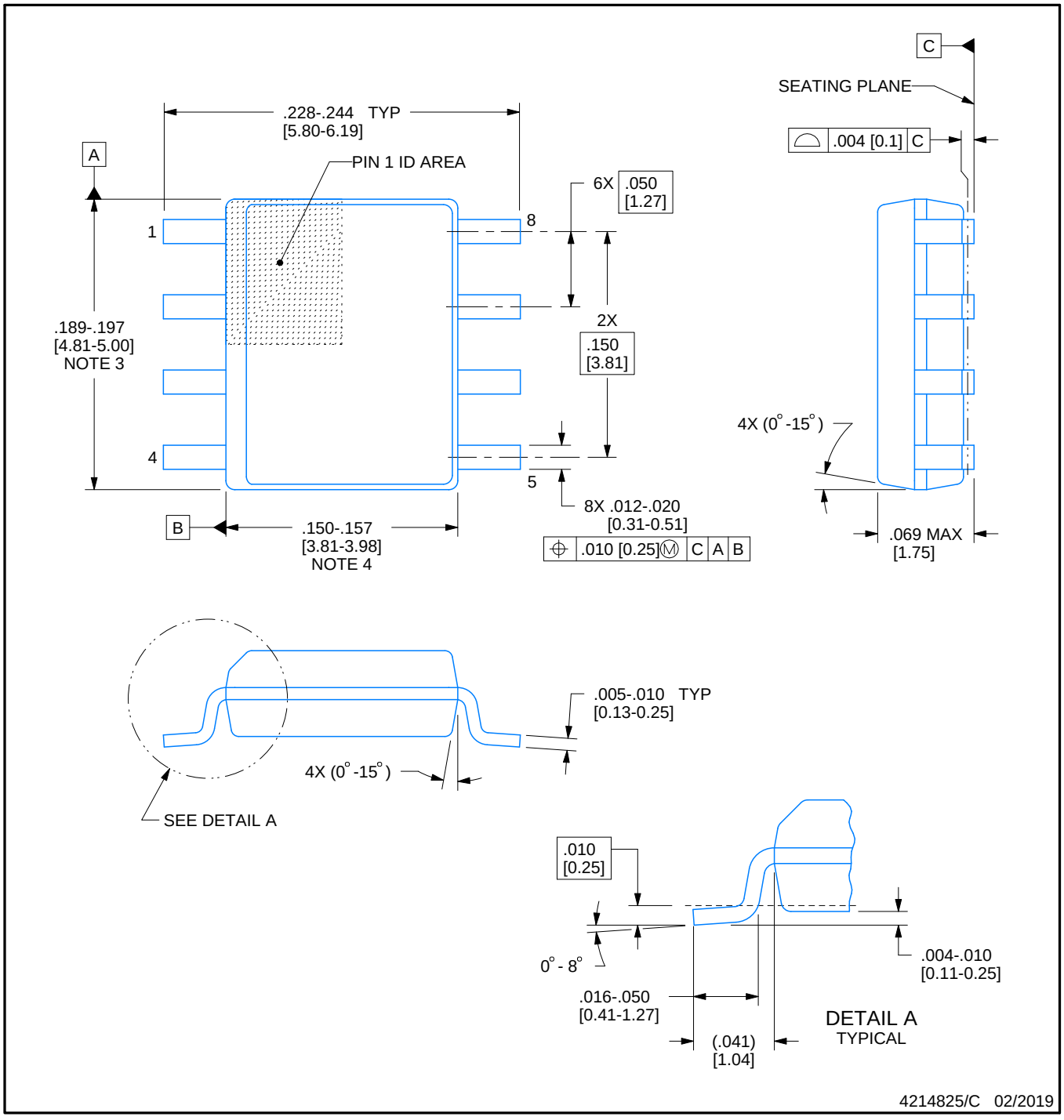


PACKAGE OUTLINE

D0008A

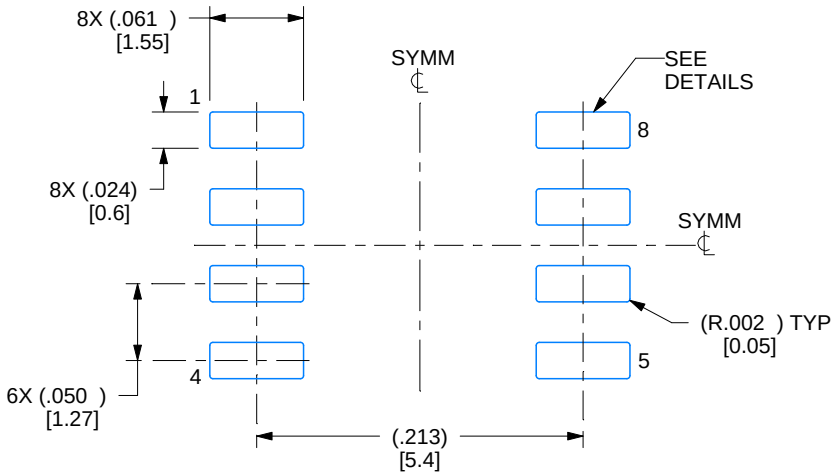
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

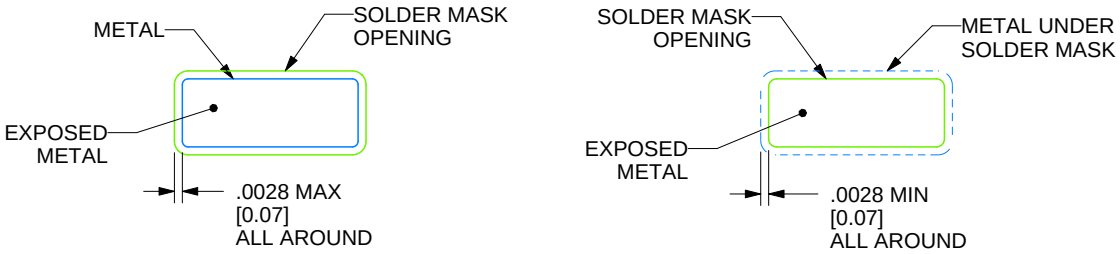


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

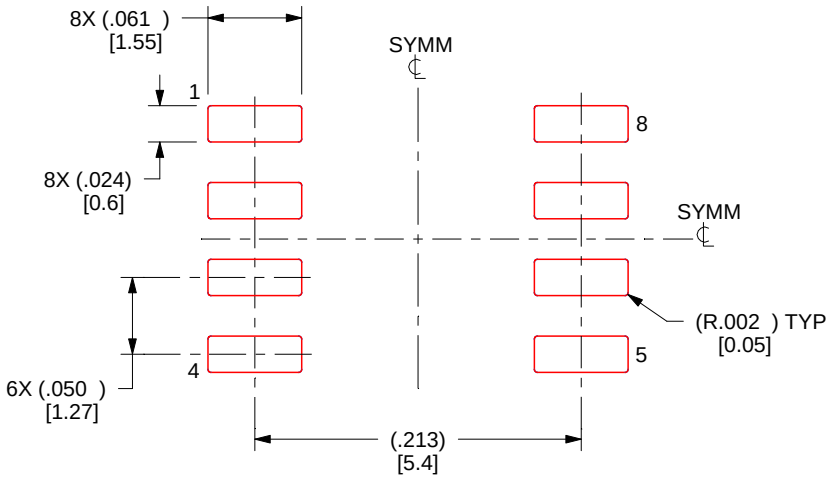
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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