Single Ended Active Clamp/Reset PWM

FEATURES

- Provides Auxiliary Switch Activation Complementary to Main Power Switch Drive
- Programmable deadtime (Turn-on Delay) Between Activation of Each Switch
- Voltage Mode Control with Feedforward Operation
- Programmable Limits for Both Transformer Volt- Second Product and PWM Duty Cycle
- High Current Gate Driver for Both Main and Auxiliary Outputs
- Multiple Protection Features with Latched Shutdown and Soft Restart
- Low Supply Current (100 μA Startup, 1.5 mA Operation)

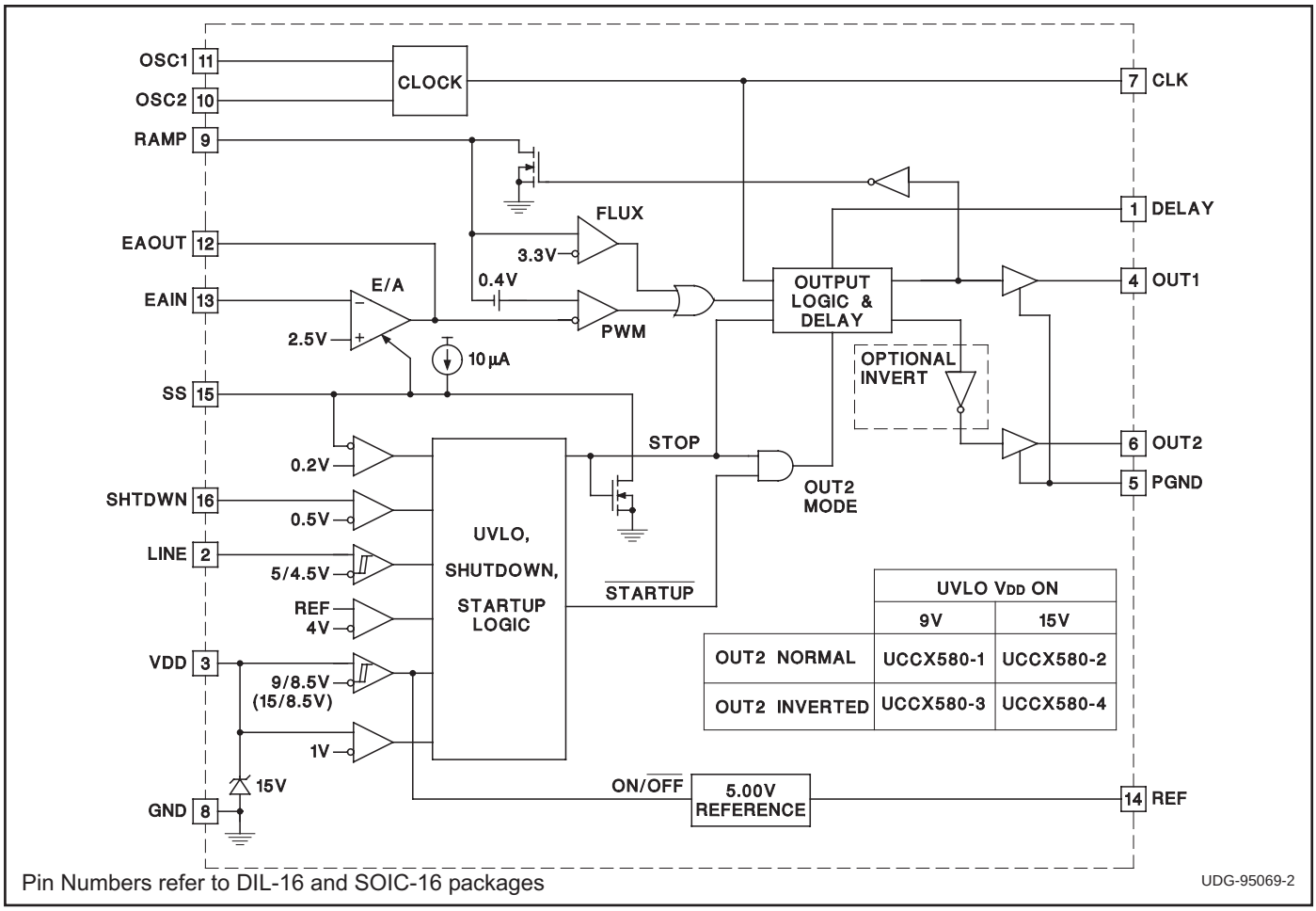
DESCRIPTION

The UCC3580 family of PWM controllers is designed to implement a variety of active clamp/reset and synchronous rectifier switching converter topologies. While containing all the necessary functions for fixed frequency, high performance pulse width modulation, the additional feature of this design is the inclusion of an auxiliary switch driver which complements the main power switch, and with a programmable deadtime or delay between each transition. The active clamp/reset technique allows operation of single ended converters beyond 50% duty cycle while reducing voltage stresses on the switches, and allows a greater flux swing for the power transformer. This approach also allows a reduction in switching losses by recovering energy stored in parasitic elements such as leakage inductance and switch capacitance.

The oscillator is programmed with two resistors and a capacitor to set switching frequency and maximum duty cycle. A separate synchronized ramp provides a voltage feedforward pulse width modulation and a programmed maximum volt-second limit. The generated clock from the oscillator contains both frequency and maximum duty cycle information.

(continued)

BLOCK DIAGRAM



Pin Numbers refer to DIL-16 and SOIC-16 packages

UDG-95069-2

DESCRIPTION (cont.)

The main gate drive output (OUT1) is controlled by the pulse width modulator. The second output (OUT2) is intended to activate an auxiliary switch during the off time of the main switch, except that between each transition there is deadtime where both switches are off, programmed by a single external resistor. This design offers two options for OUT2, normal and inverted. In the -1 and -2 versions, OUT2 is normal and can be used to drive PMOS FETs. In the -3 and -4 versions, OUT2 is inverted and can be used to drive NMOS FETs. In all versions, both the main and auxiliary switches are held off prior to startup and when the PWM command goes to zero duty cycle. During fault conditions, OUT1 is held off while OUT2 operates at maximum duty cycle with a guaranteed off time equal to the sum of the two deadtimes.

Undervoltage lockout monitors supply voltage (VDD), the precision reference (REF), input line voltage (LINE), and the shutdown comparator (SHTDWN). If after any of these four have sensed a fault condition, recovery to full operation is initiated with a soft start. VDD thresholds, on and off, are 15V and 8.5V for the -2 and -4 versions, 9V and 8.5V for the -1 and -3 versions.

The UCC1580-x is specified for operation over the military temperature range of -55°C to 125°C. The UCC2580-x is specified from -40°C to 85°C. The UCC3580-x is specified from 0°C to 70°C. Package options include 16-pin surface mount and dual in-line.

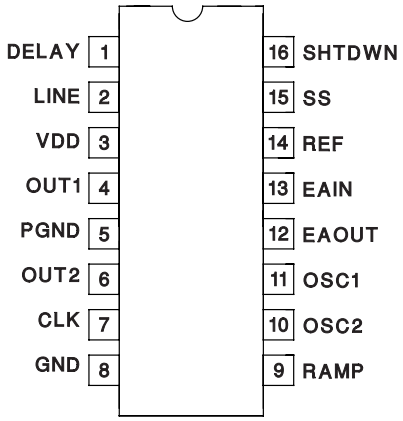
ABSOLUTE MAXIMUM RATINGS

VDD	16V
I_{VDD}	25mA
LINE, RAMP	0.3V to VDD + 1V
I_{LINE}, I_{RAMP}	5mA
DELAY	5.3V
I_{DELAY}	5mA
I_{OUT1} (tpw < 1 s and Duty Cycle < 10%)	0.6A to 1.2A
I_{OUT2} (tpw < 1 s and Duty Cycle < 10%)	0.4A to 0.4A
I_{CLK}	100mA to 100mA
OSC1, OSC2, SS, SHTDWN, EAIN	0.3V to REF + 0.3V
I_{EAOUT}	5mA to 5mA
I_{REF}	30mA
PGND	0.2V to 0.2V
Storage Temperature	-65°C to +150°C
Junction Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



ORDER INFORMATION



ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications are over the full temperature range, VDD = 12V, R1 = 18.2 k , R2 = 4.41 k , C_T = 130 pF, R3 = 100 k , C_{OUT1} = 0 F, C_{OUT2} = 0 F. T_A = 0°C to 70°C for the UCC3580, -40°C to 85°C for the UCC2580, -55°C to 125°C for the UCC1580, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Frequency		370	400	430	kHz
CLK Pulse Width		650	750	850	ns
CLK V_{OH}	I_{CLK} = 3 mA	4.3	4.7		V
CLK V_{OL}	I_{CLK} = 3 mA		0.3	0.5	V
Ramp Generator Section					
Ramp V_{OL}	I_{RAMP} = 100 μA		50	100	mV
Flux Comparator Vth		3.16	3.33	3.50	V
Pulse Width Modulator Section					
Minimum Duty Cycle	OUT1, EAOUT = VOL			0	%
Maximum Duty Cycle	OUT1, EAIN = 2.6 V	63	66	69	%
PWM Comparator Offset		0.1	0.4	0.9	V
Error Amplifier Section					
EAIN	EAOUT = EAIN	2.44	2.5	2.56	V
I_{EAIN}	EAOUT = EAIN		150	400	nA
EAOUT, VOL	EAIN = 2.6 V, I_{EAOUT} = 100 μA		0.3	0.5	V
EAOUT, VOH	EAIN = 2.4 V, I_{EAOUT} = 100 μA	4	5	5.5	V
AVOL		70	80		dB
Gain Bandwidth Product	f = 100 kHz (Note 1)	2	6		MHz
Softstart/Shutdown Section					
Start Duty Cycle	EAIN = 2.4 V		0		%
SS V_{OL}	I_{SS} = 100 μA		100	350	mV
SS Restart Threshold			400	550	mV
I_{SS}			–20	–35	μA
SHTDWN V_{TH}		0.4	0.5	0.6	V
I_{SHTDWN}			50	150	nA
Undervoltage Lockout Section					
VDD On	UCC3580-2,-4	14	15	16	V
	UCC3580-1,-3	8	9	10	V
VDD Off		7.5	8.5	9.5	V
LINE On		4.7	5	5.3	V
LINE Off		4.2	4.5	4.8	V
I_{LINE}	LINE = 6 V		50	150	nA
Supply Section					
VDD Clamp	I_{VDD} = 10 mA	14	15	16	V
I_{VDD} Start	VDD < VDD On		160	250	A
I_{VDD} Operating	No Load		2.5	3.5	mA
Output Drivers Section					
OUT1 V_{SAT} High	I_{OUT1} = 50 mA		0.4	1.0	V
OUT1 V_{SAT} Low	I_{OUT1} =100 mA		0.4	1.0	V
OUT2 V_{SAT} High	I_{OUT2} = 30 mA		0.4	1.0	V
OUT2 V_{SAT} Low	I_{OUT2} = 30 mA		0.4	1.0	V
OUT1 Fall Time	C_{OUT1} = 1nF, Rs = 3		20	50	ns
OUT1 Rise Time	C_{OUT1} = 1nF, Rs = 3		40	80	ns
OUT2 Fall Time	C_{OUT2} = 300pF, Rs = 10		20	50	ns
OUT2 Rise Time	C_{OUT2} = 300pF, R_S = 10		20	40	ns

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications are over the full temperature range, VDD = 12V, R1 = 18.2 k , R2 = 4.41 k , C_T = 130 pF, R3 = 100 k , C_{OUT1} = 0 F, C_{OUT2} = 0 F. T_A = 0°C to 70°C for the UCC3580, -40°C to 85°C for the UCC2580, -55°C to 125°C for the UCC1580, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Drivers Section (cont.)					
Delay 1 OUT2 to OUT1	R3 = 100 kΩ, $C_{OUT1} = C_{OUT2}$ = 15 pF	90	120	160	ns
	$T_A = T_J$ = 25°C	100	120	140	ns
Delay 2 OUT1 to OUT2	R3 = 100 kΩ, $C_{OUT1} = C_{OUT2}$ = 15 pF	110	170	250	ns
	$T_A = T_J$ = 25°C	140	170	200	ns
Reference Section					
REF	I_{REF} = 0	4.875	5	5.125	V
Load Regulation	I_{REF} = 0 mA to 1 mA		1	20	mV
Line Regulation	VDD = 10 V to 14 V		1	20	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CLK: Oscillator clock output pin from a low impedance CMOS driver. CLK is high during guaranteed off time. CLK can be used to synchronized up to five other UCC3580 PWMs.

DELAY: A resistor from DELAY to GND programs the nonoverlap delay between OUT1 and OUT2. The delay times, Delay1 and Delay2, are shown in Figure 1 and are as follows:

$$Delay\,1 = 1.1pF \bullet R3$$

Delay2 is designed to be larger than Delay1 by a ratio shown in Figure 2.

EAIN: Inverting input to the error amplifier. The noninverting input of the error amplifier is internally set to 2.5V. EAIN is used for feedback and loop compensation.

EAOUT: Output of the error amplifier and input to the PWM comparator. Loop compensation components connect from EAOUT to EAIN.

GND: Signal Ground.

LINE: Hysteretic comparator input. Thresholds are 5.0V and 4.5V. Used to sense input line voltage and turn off OUT1 when the line is low.

OSC1 & OSC2: Oscillator programming pins. A resistor connects each pin to a timing capacitor. The resistor connected to OSC1 sets maximum on time. The resistor connected to OSC2 controls guaranteed off time. The combined total sets frequency with the timing capacitor. Frequency and maximum duty cycle are approximately given by:

$$\text{Frequency} = \frac{1.44}{(R1 + R2) \bullet (CT + 27pF)}$$

$$\text{Maximum Duty Cycle} = \frac{R1}{R1 + R2}$$

Maximum Duty Cycle for OUT1 is slightly less due to Delay1 which is programmed by R3.

OUT1: Gate drive output for the main switch capable of sourcing up to 0.5A and sinking 1A.

OUT2: Gate drive output for the auxiliary switch with 0.3A drive current capability.

PGND: Ground connection for the gate drivers. Connect PGND to GND at a single point so that no high frequency components of the output switching currents are in the ground plane on the circuit board.

RAMP: A resistor (R4) from RAMP to the input voltage and a capacitor (CR) from RAMP to GND programs the feedforward ramp signal. RAMP is discharged to GND when CLK is high and allowed to charge when CLK is low. RAMP is the line feedforward sawtooth signal for the PWM comparator. Assuming the input voltage is much greater than 3.3V, the ramp is very linear. A flux comparator compares the ramp signal to 3.3V to limit the maximum allowable volt-second product:

Volt-Second Product Clamp = 3.3 • R4 • CR.

REF: Precision 5.0V reference pin. REF can supply up to 5mA to external circuits. REF is off until VDD exceeds 9V (–1 and –3 versions) or activates the 15V clamp (–2 and –4 versions) and turns off again when VDD droops below 8.5V. Bypass REF to GND with a 1μF capacitor.

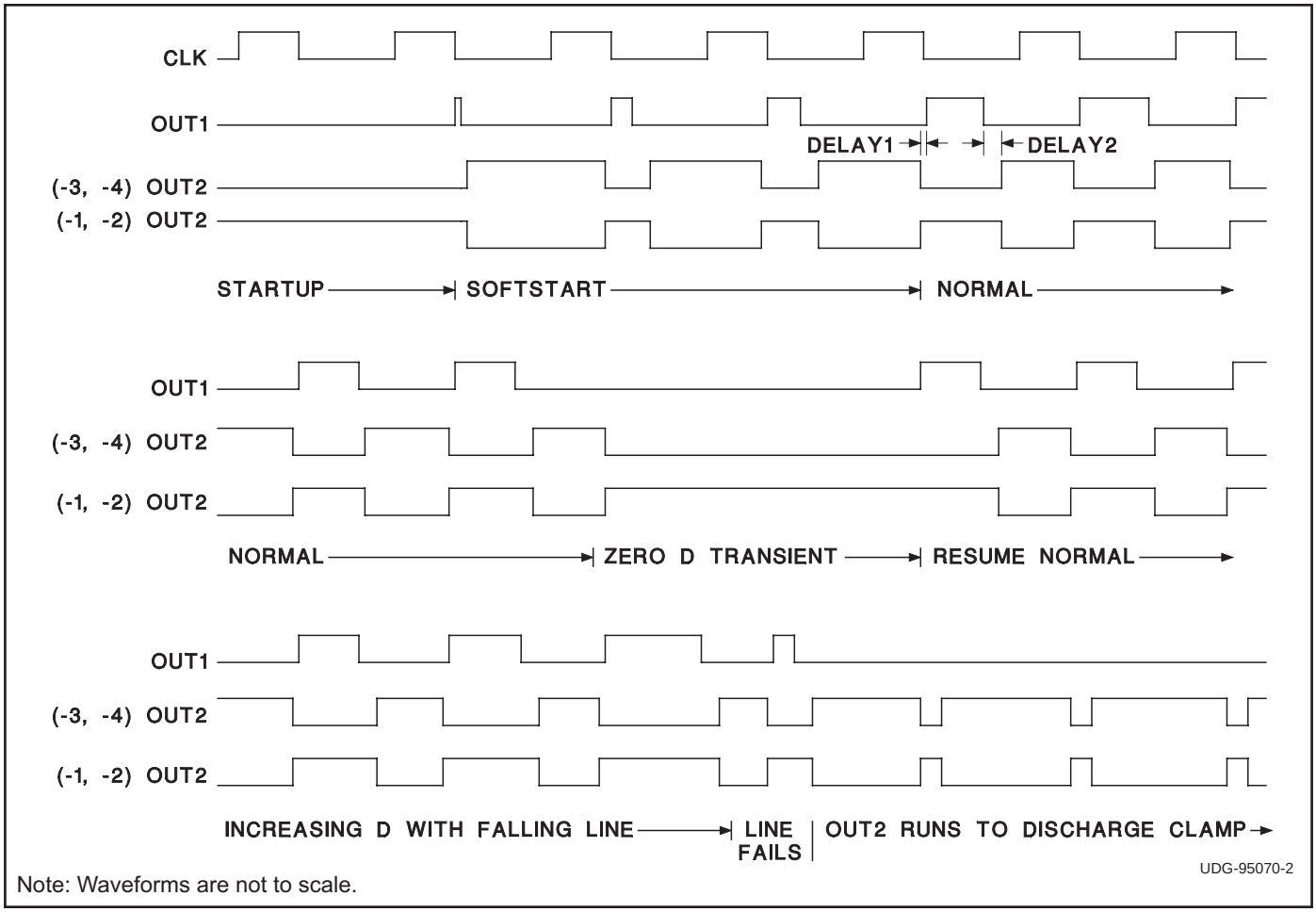
SHTDWN: Comparator input to stop the chip. The threshold is 0.5V. When the chip is stopped, OUT1 is low and OUT2 continues to oscillate with guaranteed off time equal to two non-overlap delay times. OUT2 continues to switch after SHTDWN is asserted until the voltage on VDD falls below VCS (typically 4 V) in order to discharge the clamp capacitor.

PIN DESCRIPTIONS (cont.)

SS: A capacitor from SS to ground programs the soft start time. During soft start, EAOUT follows the amplitude of SS's slowly increasing waveform until regulation is achieved.

VDD: Chip power supply pin. VDD should be bypassed to PGND. The –1 and –3 versions require VDD to exceed 9V to start and remain above 8.5V to continue running. A shunt clamp from VDD to GND limits the supply voltage to 15V. The –2 and –4 versions do not start until

APPLICATION INFORMATION



Note: Waveforms are not to scale.

Figure 1. Output time relationships.

UVLO and Startup

For self biased off-line applications, -2 and -4 versions (UVLO on and off thresholds of 15V and 8.5V typical) are recommended. For all other applications, -1 and -3 versions provide the lower on threshold of 9V. The IC requires a low startup current of only 160μA when VDD is under the UVLO threshold, enabling use of a large trickle charge resistor (with corresponding low power dissipation) from the input voltage. VDD has an internal clamp at 15V which can sink up to 10mA. Measures should be taken not to exceed this current. For -2 and -4 versions, this clamp must be activated as an indication of reaching the UVLO on threshold. The internal reference (REF) is brought up when the UVLO on threshold is crossed. The startup logic ensures that LINE and REF are above and SHTDWN is below their respective thresholds before outputs are asserted. LINE input is useful for monitoring actual input voltage and shutting off the IC if it falls below a programmed value. A resistive divider should be used to connect the input voltage to the LINE input. This feature can protect the power supply from excessive currents at low line voltages.

APPLICATION INFORMATION (cont.)

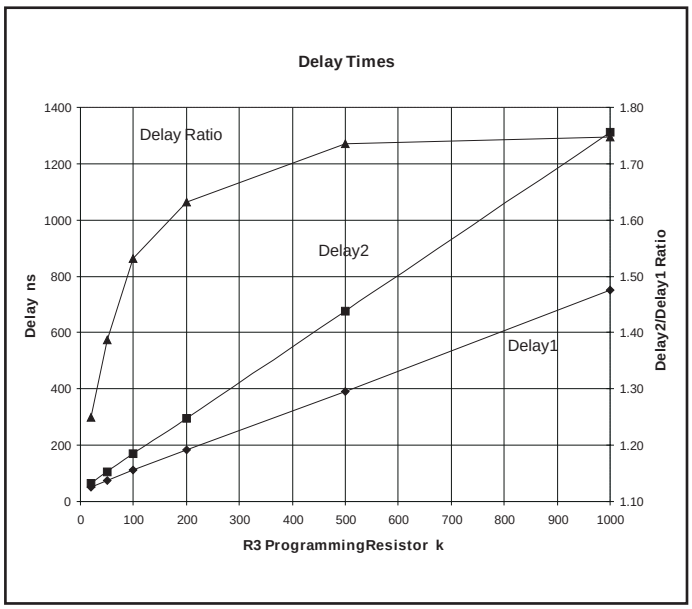


Figure 2. Delay times.

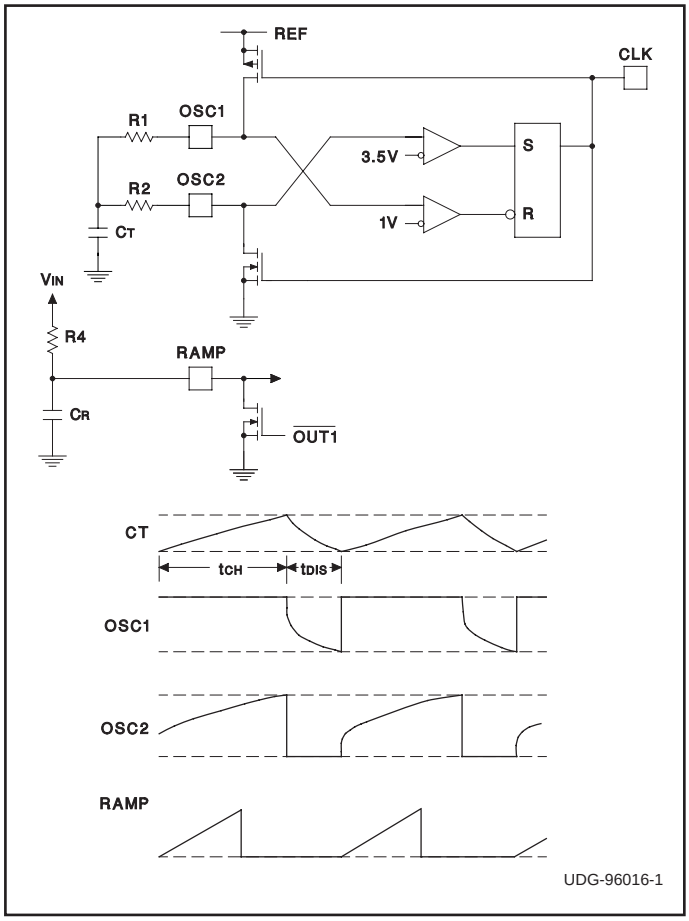


Figure 3. Oscillator and ramp circuits.

The soft start pin provides an effective means to start the IC in a controlled manner. An internal current of 20 A begins charging a capacitor connected to SS once the startup conditions listed above have been met. The voltage on SS effectively controls maximum duty cycle on OUT1 during the charging period. OUT2 is also controlled during this period (see Figure 1). Negation of any of the startup conditions causes SS to be immediately discharged. Internal circuitry ensures full discharge of SS (to 0.3V) before allowing charging to begin again, provided all the startup conditions are again met.

Oscillator

Simplified oscillator block diagram and waveforms are shown in Figure 3. OSC1 and OSC2 pins are used to program the frequency and maximum duty cycle. Capacitor CT is alternately charged through R1 and discharged through R2 between levels of 1.67 V and 3.3 V. The charging and discharging equations for CT are given by

$$VC(charge) = V_{REF} \bullet \left(1 - \frac{2}{3} \bullet e^{-t/\tau_1}\right)$$

$$VC(discharge) = \frac{2}{3} \bullet V_{REF} \bullet e^{-t/\tau_2}$$

where $\tau_1 = R1 \bullet CT$ and $\tau_2 = R2 \bullet CT$. The charge time and discharge time are given by

$t_{CH} = 0.69 \bullet R1 \bullet C_T$ and $t_{DIS} = 0.69 \bullet R2 \bullet C_T$

The CLK output is high during the discharge period. It blanks the output to limit the maximum duty cycle of OUT1. The frequency and maximum duty cycle are given by

$$Frequency = \frac{1.44}{(R1 + R2) \bullet (CT + 27\ pF)}$$

$$Maximum\ Duty\ Cycle = \frac{R1}{R1 + R2}$$

Maximum Duty Cycle for OUT1 will be slightly less due to Delay1 which is programmed by R3.

Voltage Feedforward and Volt-Second Clamp

UCC3580 has a provision for input voltage feedforward. As shown in Figure 3, the ramp slope is made proportional to input line voltage by converting it into a charging current for CR. This provides a first order cancellation of the effects of line voltage changes on converter performance. The maximum volt-second clamp is provided to protect against transient saturation of the transformer core. It terminates the OUT1 pulse when the RAMP voltage exceeds 3.3V. If the feedforward feature is not used, the ramp can be generated by tying R4 to REF. However, the linearity of ramp suffers and in this case the maximum volt-second clamp is no longer available.

APPLICATION INFORMATION (cont.)

Output Configurations

The UCC3580 family of ICs is designed to provide control functions for single ended active clamp circuits. For different implementations of the active clamp approach, different drive waveforms for the two switches (main and auxiliary) are required. The -3 and -4 versions of the IC supply complementary non-overlapping waveforms (OUT1 and OUT2) with programmable delay which can be used to drive the main and auxiliary switches. Most active clamp configurations will require one of these outputs to be transformer coupled to drive a floating switch (e.g. Figure 5). The -1 and -2 versions have the phase of OUT2 inverted to give overlapping waveforms. This configuration is suitable for capacity coupled driving of a ground referenced p-channel auxiliary switch with the OUT2 drive while OUT1 is directly driving an n-channel main switch (e.g. Figure 4).

The programmable delay can be judiciously used to get zero voltage turn-on of both the main and auxiliary switches in the active clamp circuits. For the UCC3580, a single pin is used to program the delays between OUT1 and OUT2 on both sets of edges. Figure 1 shows the relationships between the outputs. Figure 2 gives the ratio between the two delays. During the transition from main to auxiliary switch, the delay is not very critical for ZVS turn-on. For the first half of OUT1 off-time, the body diode of the auxiliary switch conducts and OUT2 can be turned on any time. The transition from auxiliary to main switch is more critical. Energy stored in the parasitic inductance(s) at the end of the OUT2 pulse is used to discharge the parasitic capacitance across the main switch during the delay time. The delay (Delay 1) should be optimally programmed at 1/4 the resonant period determined by parasitic capacitance and the resonant inductor (transformer leakage and/or magnetizing inductances, depending on the topology). However, depending on other circuit parasitics, the resonant behavior can change, and in some cases, ZVS turn-on may not be obtainable. It can be shown that the optimum delay time is independent of operating conditions for a specific circuit and should be determined specifically for each circuit.

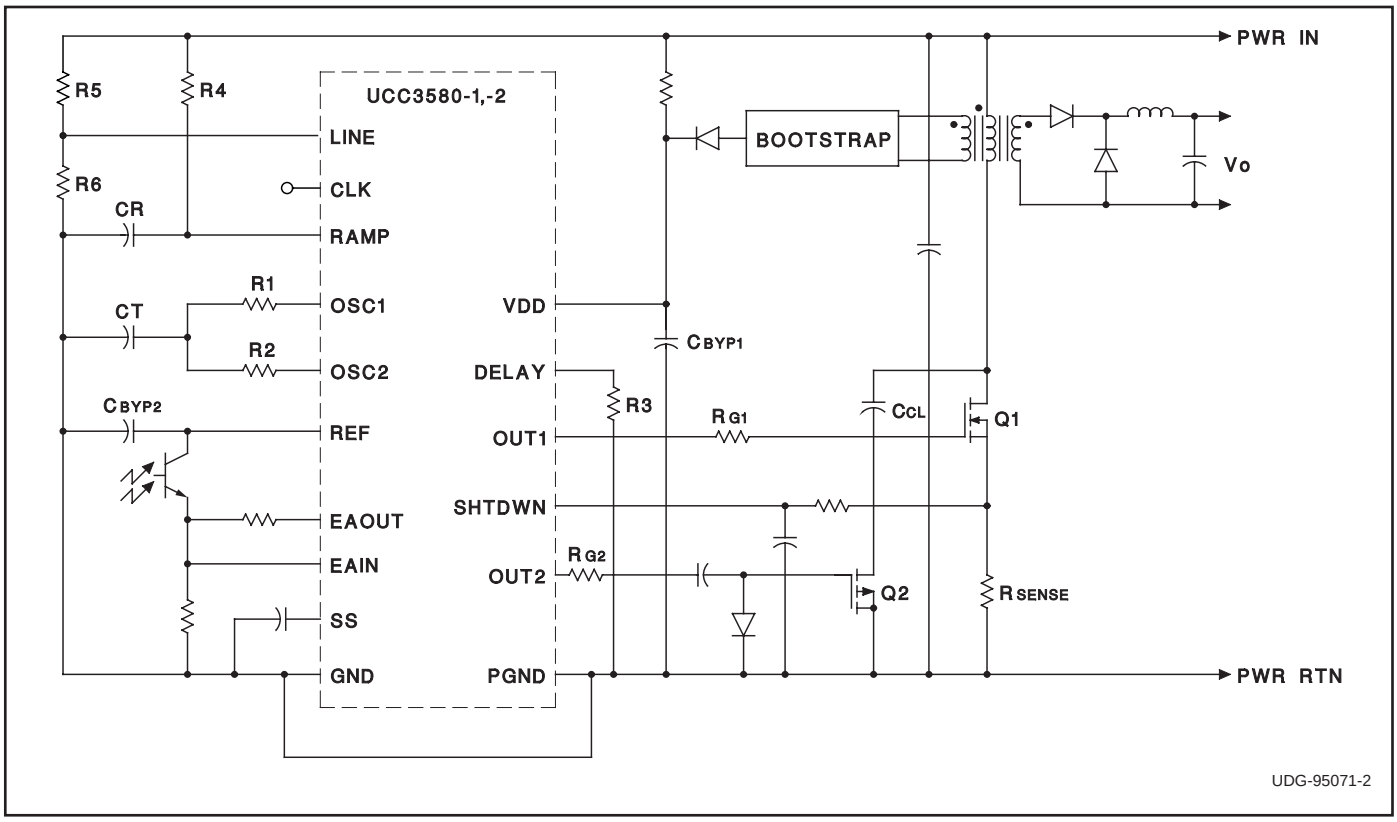


Figure 4. Active clamp forward converter.

APPLICATION INFORMATION (cont.)

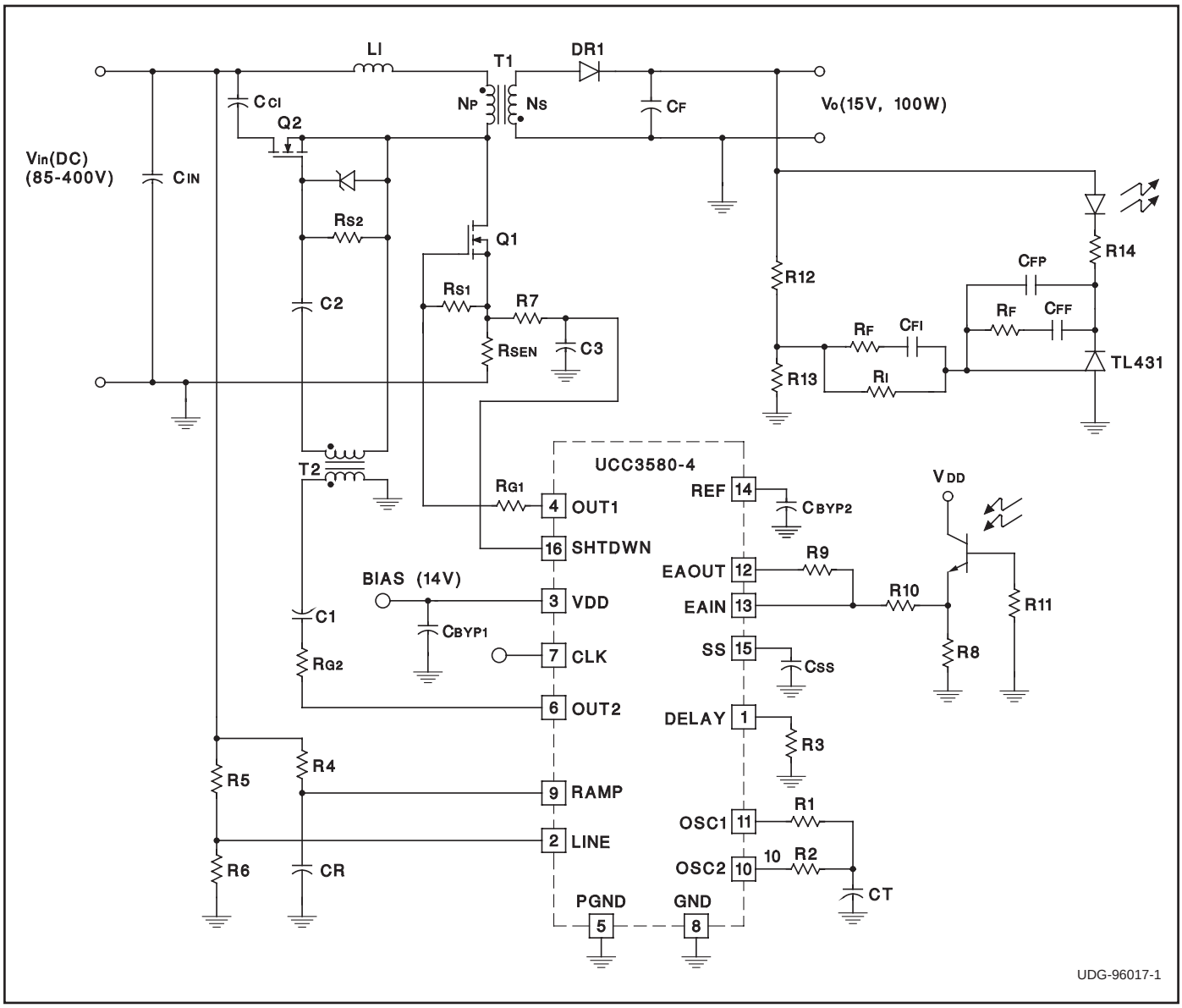


Figure 5. Off-line active clamp flyback converter.

The use of active reset in a flyback power converter topology may be covered by U.S. Patent No. 5,402,329 owned by Technical Witts, Inc., and for which Unitrode offers users a paid up license for application of the UCC1580 product family.

APPLICATION INFORMATION (cont.)

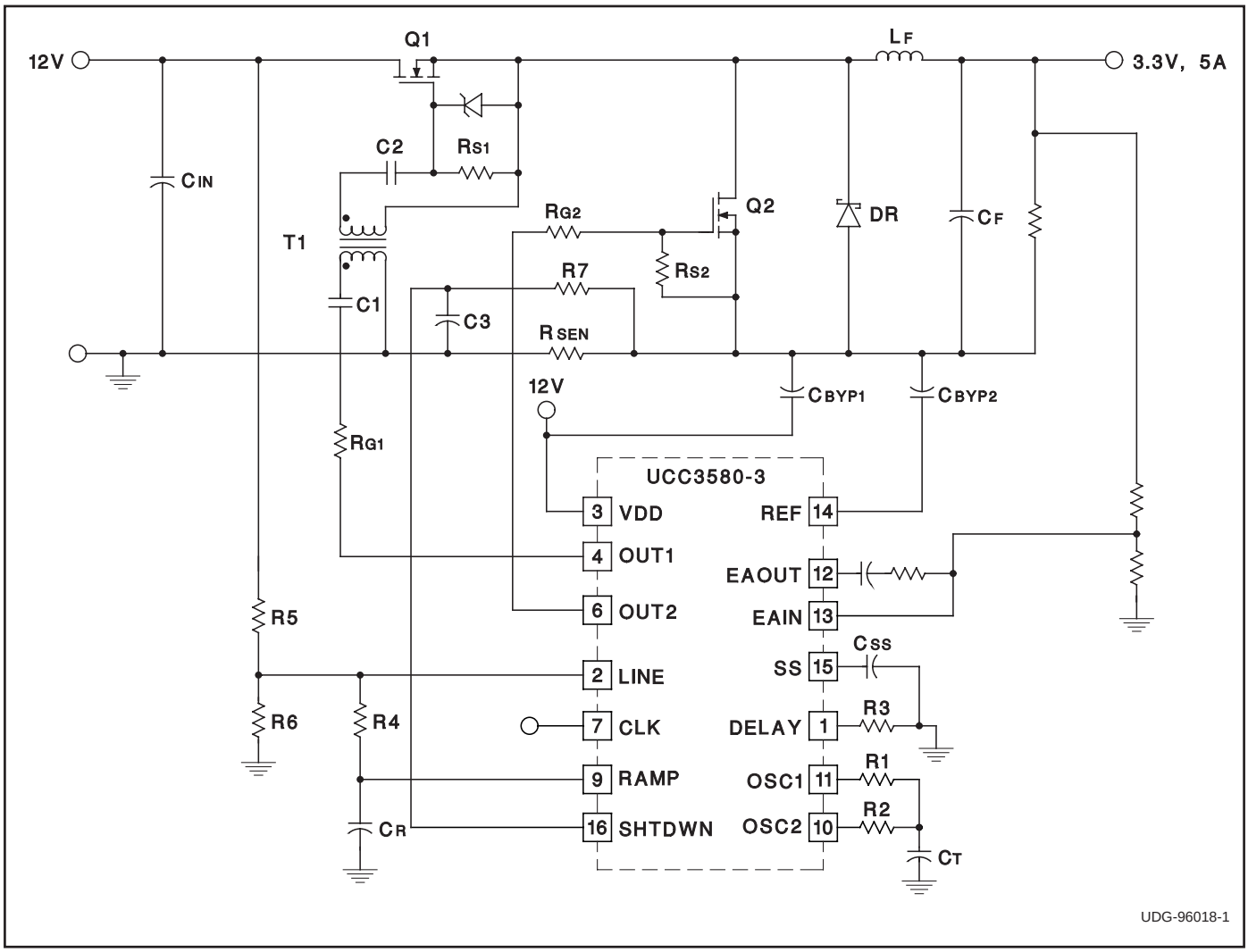


Figure 6. UCC3580 used in a synchronous rectifier application.

REVISION	DATE	COMMENT
SLUS292B	MAY 2005	Updated OSC frequency and maximum duty cycle, CT charge and discharge equations. Updated SHTDWN pin description. Updated typical CT value used for measurements in electrical characteristics table.
SLUS292C	MAY 2005	Removed Q package from datasheet.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2580D-1	NRND	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-1
UCC2580D-1.A	NRND	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-1
UCC2580D-2	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	UCC2580D-2
UCC2580D-3	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-3
UCC2580D-3.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-3
UCC2580D-4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	UCC2580D-4
UCC2580DTR-1	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-1
UCC2580DTR-1.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-1
UCC2580DTR-2	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-2
UCC2580DTR-2.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-2
UCC2580DTR-3	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-3
UCC2580DTR-3.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2580D-3
UCC3580D-1	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	UCC3580D-1
UCC3580D-2	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	UCC3580D-2
UCC3580D-3	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	UCC3580D-3
UCC3580D-4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	UCC3580D-4
UCC3580DTR-1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-1
UCC3580DTR-1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-1
UCC3580DTR-2	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-2
UCC3580DTR-2.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-2
UCC3580DTR-3	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-3
UCC3580DTR-3.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-3
UCC3580DTR-4	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-4
UCC3580DTR-4.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3580D-4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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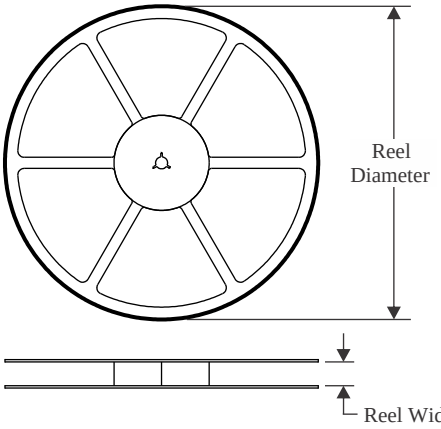
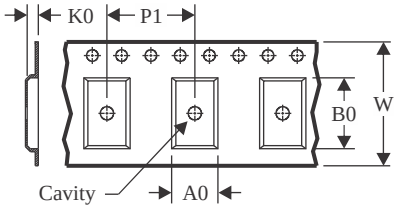
TAPE AND REEL INFORMATION

REEL DIMENSIONS

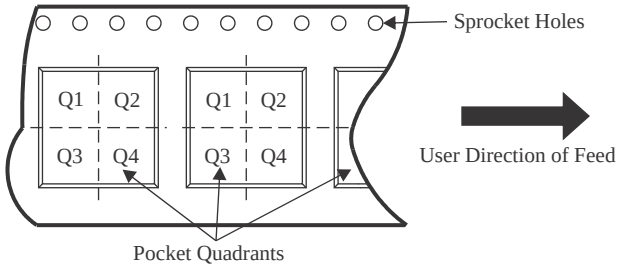


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

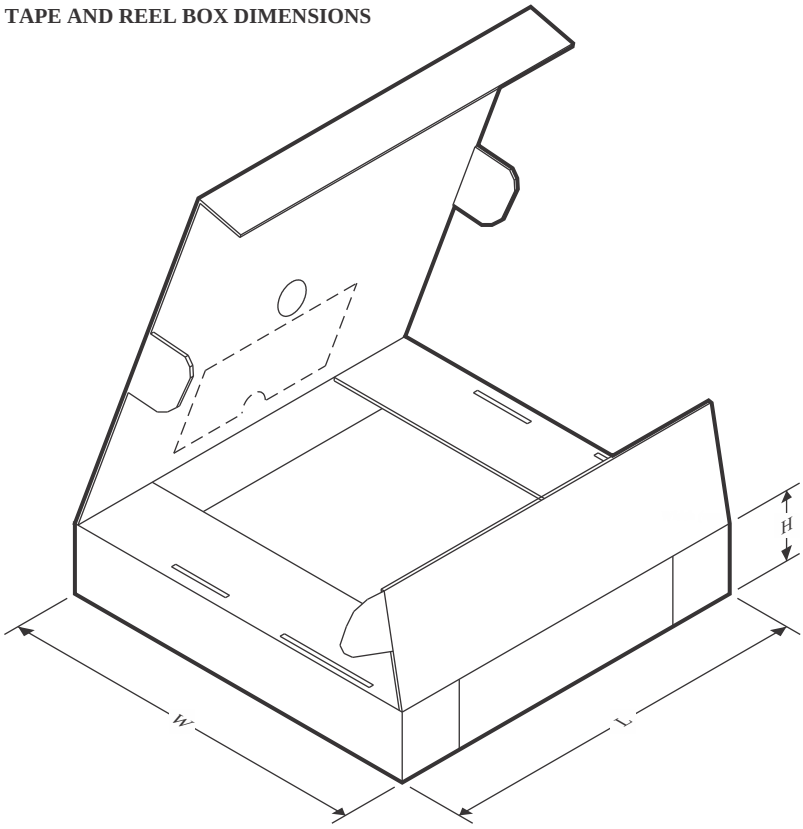
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2580DTR-1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC2580DTR-2	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC2580DTR-3	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3580DTR-1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3580DTR-2	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3580DTR-3	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3580DTR-4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

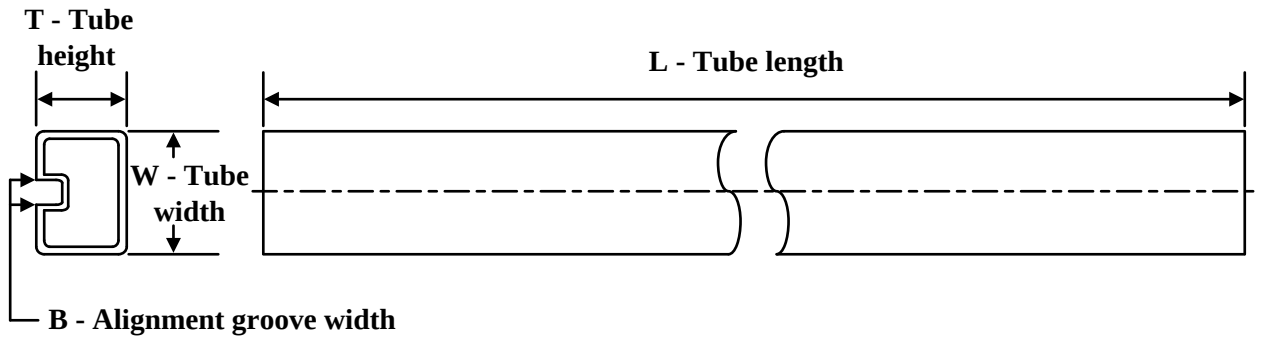
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2580DTR-1	SOIC	D	16	2500	340.5	336.1	32.0
UCC2580DTR-2	SOIC	D	16	2500	340.5	336.1	32.0
UCC2580DTR-3	SOIC	D	16	2500	340.5	336.1	32.0
UCC3580DTR-1	SOIC	D	16	2500	340.5	336.1	32.0
UCC3580DTR-2	SOIC	D	16	2500	353.0	353.0	32.0
UCC3580DTR-3	SOIC	D	16	2500	353.0	353.0	32.0
UCC3580DTR-4	SOIC	D	16	2500	340.5	336.1	32.0

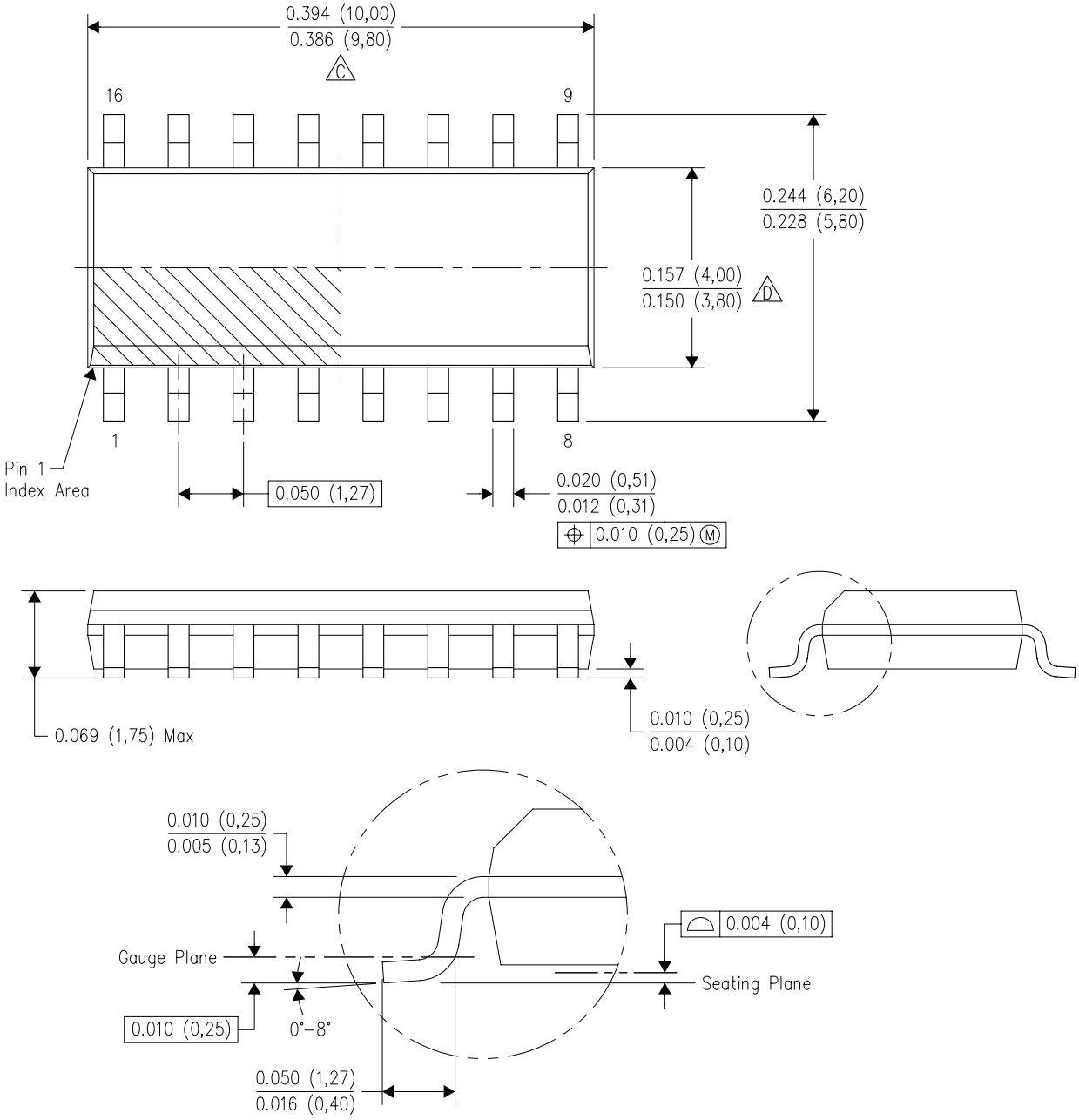
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC2580D-1	D	SOIC	16	40	507	8	3940	4.32
UCC2580D-1.A	D	SOIC	16	40	507	8	3940	4.32
UCC2580D-3	D	SOIC	16	40	507	8	3940	4.32
UCC2580D-3.A	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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