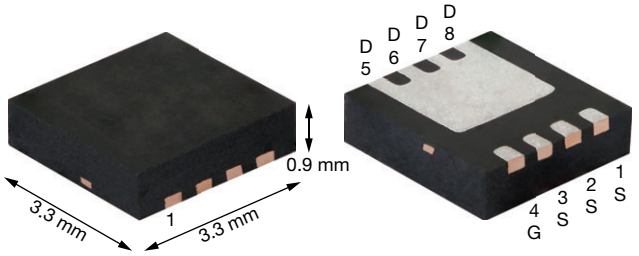
N-Channel 40 V (D-S) Fast Switching MOSFET

PowerPAK® 1212-8SH



Top View Bottom View

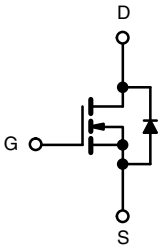
FEATURES

- TrenchFET® power MOSFET
- PWM optimized
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- Intermediate switch
- Synchronous buck



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.0078
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0100
Q_g typ. (nC)	15
I_D (A)	16.4
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH116DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	10 s	STEADY STATE	UNIT
Drain-source voltage		V_{DS}	40	40	V
Gate-source voltage		V_{GS}	± 20	± 20	
Continuous drain current (T_J = 150 °C) [a]	T_A = 25 °C	I_D	16.4	10.5	A
	T_A = 70 °C		13.1	8.4	
Pulsed drain current		I_{DM}	60	60	
Continuous source current (diode conduction) [a]		I_S	3.2	1.3	
Avalanche current	L = 0 1 mH	I_{AS}	15	15	
Avalanche energy		E_{AS}	11	11	mJ
Maximum power dissipation [a]	T_A = 25 °C	P_D	3.8	1.5	W
	T_A = 70 °C		2	0.8	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [b, c]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a]	t ≤ 10 s	R_{thJA}	24	33	°C/W
	Steady state		65	81	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.9	2.4	

Notes

a. Surface mounted on 1" x 1" FR4 board
b. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.5	-	2.5	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55 °C	-	-	5	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	40	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 16.4 A	-	0.0065	0.0078	Ω
		V_{GS} = 4.5 V, I_D = 14.5 A	-	0.0083	0.0100	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 16.4 A	-	68	-	S
Diode forward voltage [a]	V_{SD}	I_S = 3.2 A, V_{GS} = 0 V	-	0.8	1.2	V
Dynamic [b]						
Total gate charge	Q_g	V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 16.4 A	-	15	23	nC
Gate-source charge	Q_{gs}		-	6.7	-	
Gate-drain charge	Q_{gd}		-	5.1	-	
Gate resistance	R_g	f = 1 MHz	0.7	1.4	2.1	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 20 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 6 Ω	-	10	15	ns
Rise time	t_r		-	10	15	
Turn-off delay time	$t_{d(off)}$		-	36	55	
Fall time	t_f		-	10	15	
Source-drain reverse recovery time	t_{rr}	I_F = 3.2 A, di/dt = 100 A/µs	-	30	60	
Body diode reverse recovery charge	Q_{rr}		-	26	52	nc

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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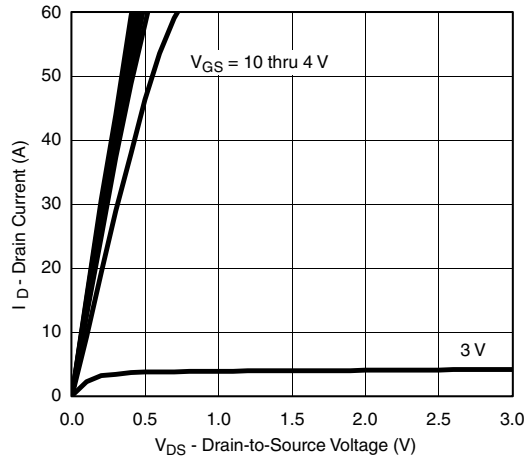
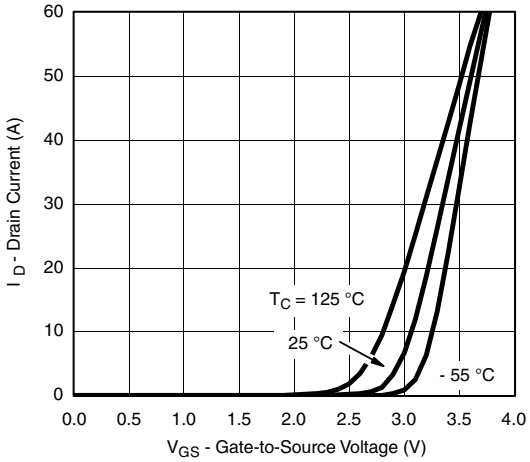
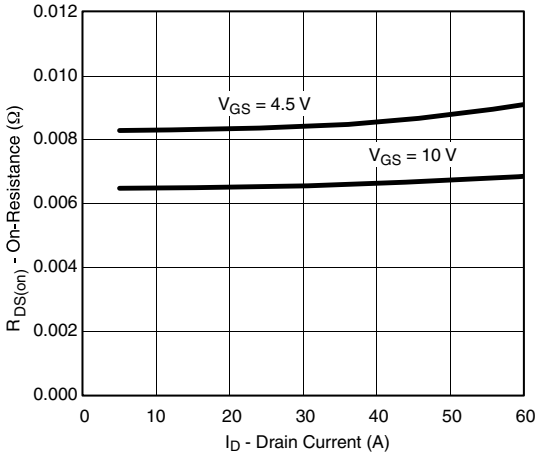
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



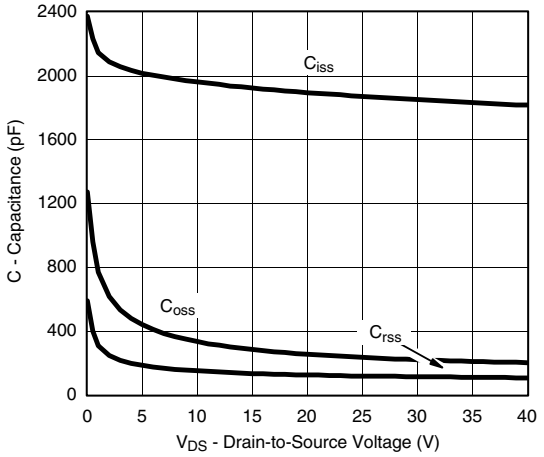
Output Characteristics



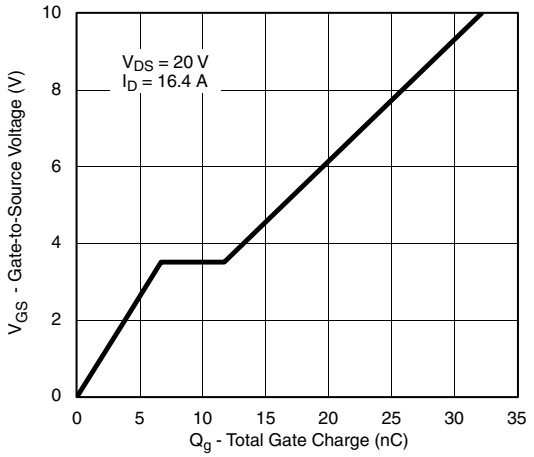
Transfer Characteristics



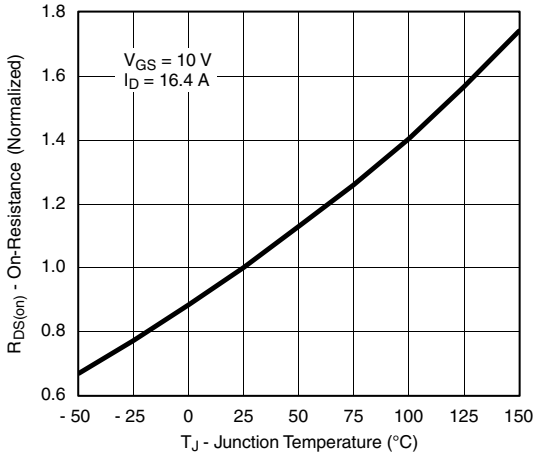
On-Resistance vs. Drain Current



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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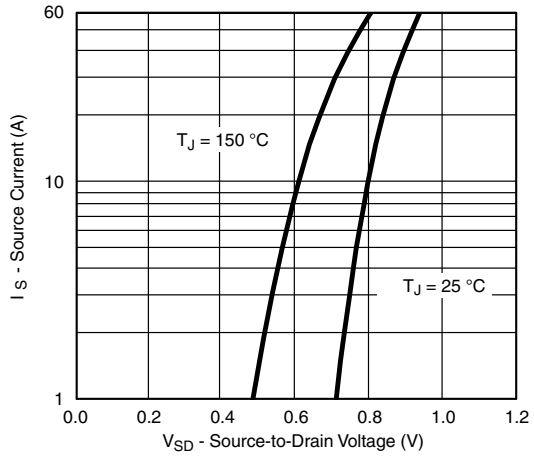
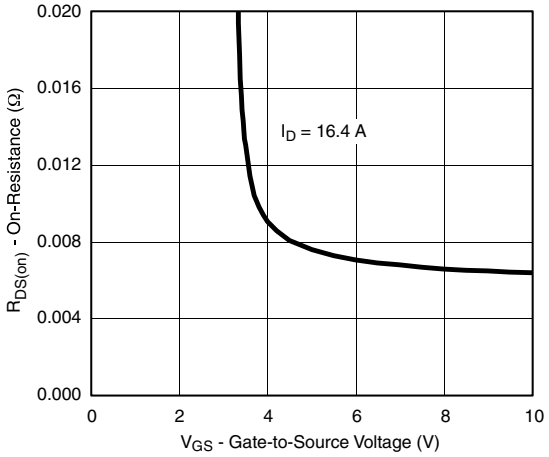
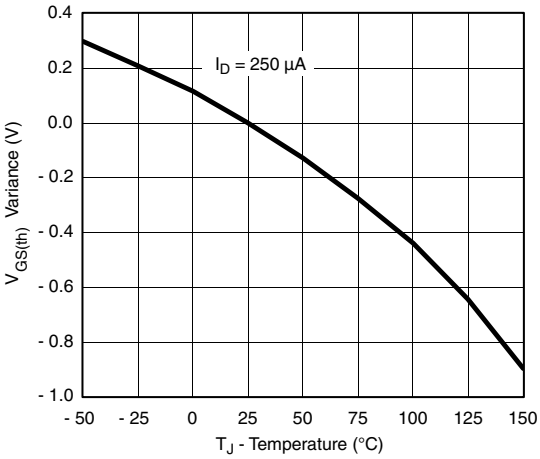


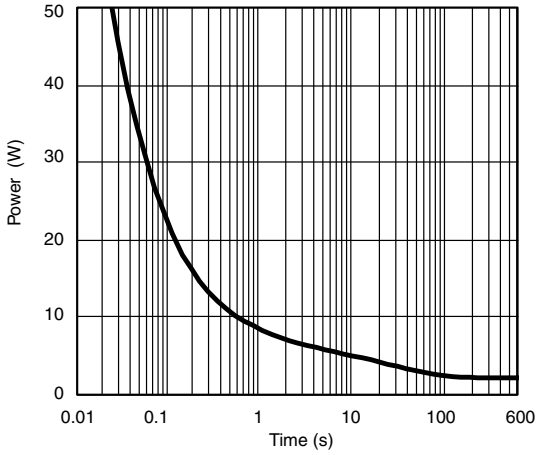
Source-Drain Diode Forward Voltage



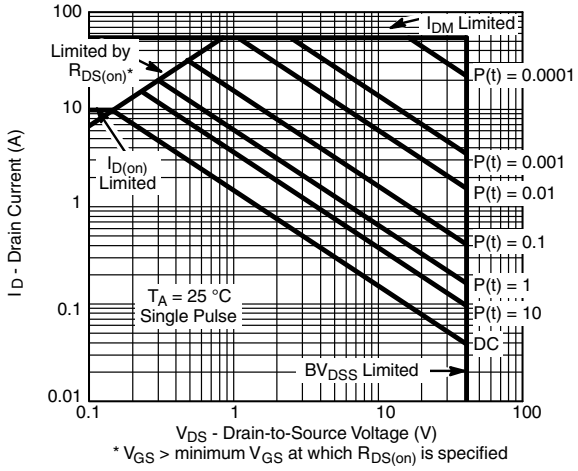
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area

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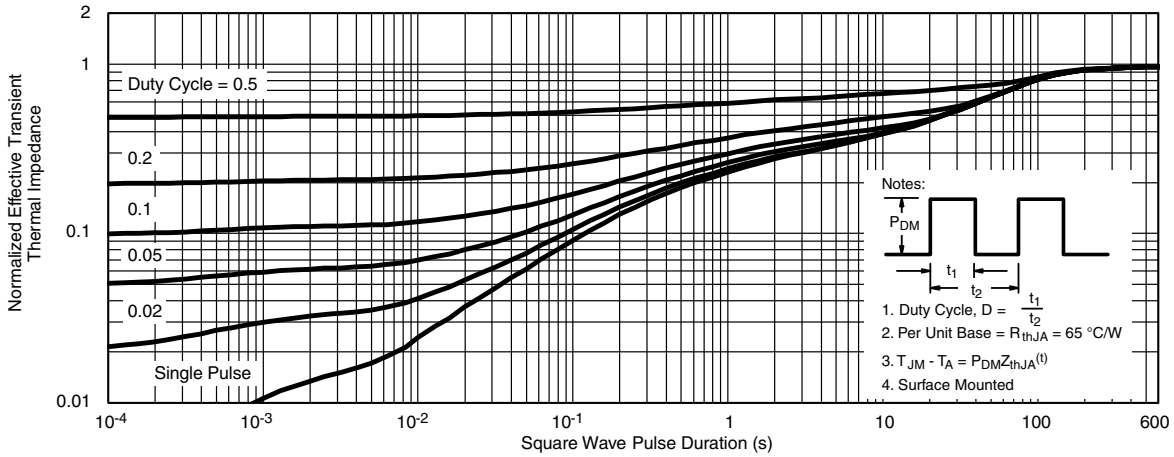
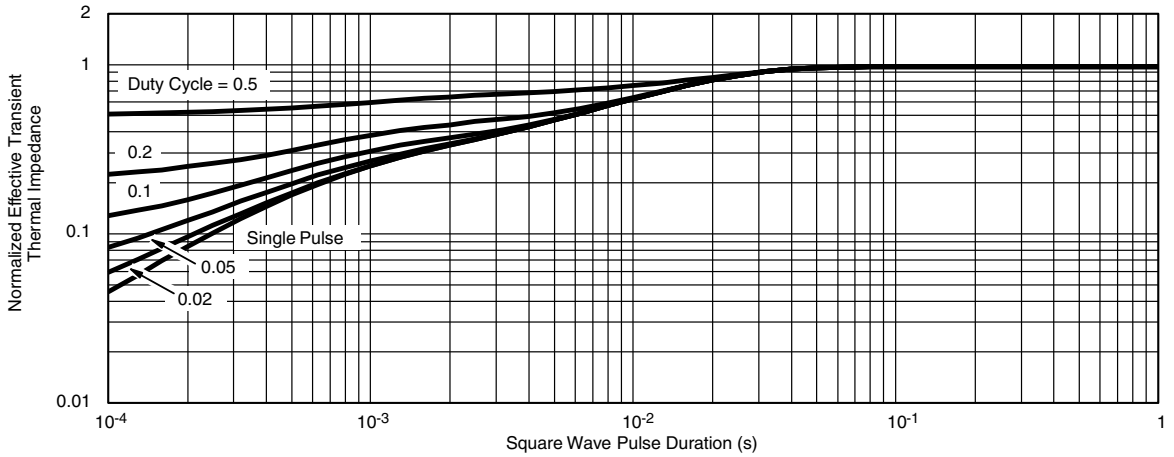


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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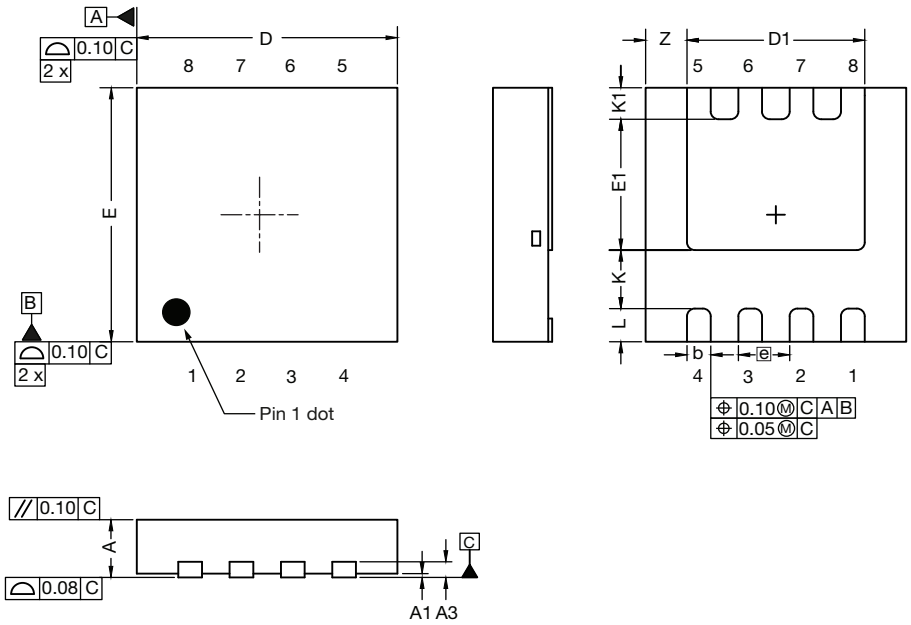
Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: S20-0930-Rev. C, 07-Dec-2020 DWG: 6062						

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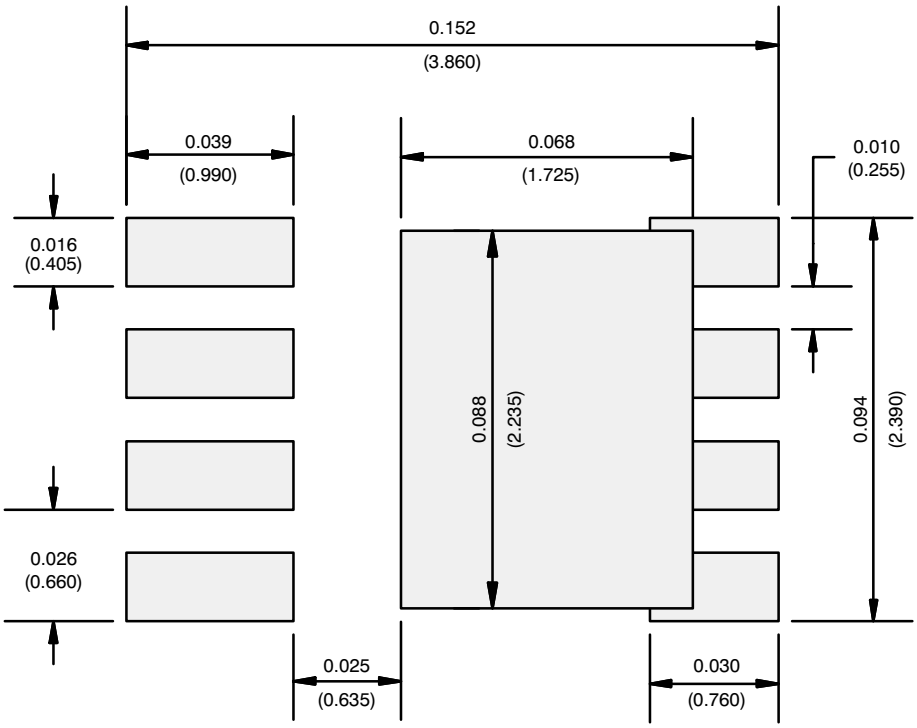
RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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