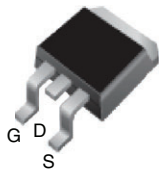
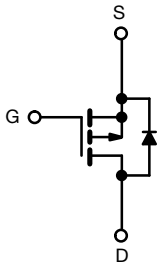
## Power MOSFET

D²PAK (TO-263)




P-Channel MOSFET

### FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available

HALOGEN FREE Available

**Note**

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | -200 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = -10 V | 1.5 |
| $Q_g$ max. (nC) | 22 | |
| $Q_{gs}$ (nC) | 12 | |
| $Q_{gd}$ (nC) | 10 | |
| Configuration | Single | |

### DESCRIPTION

The power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

| ORDERING INFORMATION | | |
|---|---|---|
| Package | D²PAK (TO-263) | D²PAK (TO-263) |
| Lead (Pb)-free and Halogen-free | SiHF9620S-GE3 | SiHF9620STRL-GE3 [a] |
| Lead (Pb)-free | IRF9620SPbF | IRF9620STRLPbF [a] |

**Note**

a. See device orientation

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | -200 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current | $V_{GS}$ at -10 V | $T_C$ = 25 °C | $I_D$ | -3.5 | A |
| | | $T_C$ = 100 °C | | -2.0 | |
| Pulsed Drain Current [a] | | | $I_{DM}$ | -14 | |
| Linear Derating Factor | | | | 0.32 | W/°C |
| Linear Derating Factor (PCB mount) [e] | | | | 0.025 | |
| Inductive Current, Clamp | | | $I_{LM}$ | -14 | A |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 40 | W |
| Maximum Power Dissipation (PCB mount) [e] | $T_A$ = 25 °C | | | 3.0 | |
| Peak Diode Recovery dV/dt [c] | | | dV/dt | -5.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering Recommendations (Peak temperature) [d] | For 10 s | | | 300 | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
b. Not Applicabl
c. $I_{SD} \leq$ -3.5 A, dI/dt ≤ 95 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C
d. 1.6 mm from case
e. When mounted on 1" square PCB (FR-4 or G-10 material)



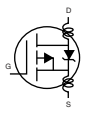
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| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB mount) [a] | $R_{thJA}$ | - | - | 40 | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | - | 3.1 | |

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material)

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0, $I_D$ = -250 µA | | -200 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = -1 mA | | - | -0.22 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | | -2.0 | - | -4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -200 V, $V_{GS}$ = 0 V | | - | - | -100 | µA |
| | | $V_{DS}$ = -160 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | -500 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -10 V | $I_D$ = -1.5 A [b] | - | - | 1.5 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = -50 V, $I_D$ = -1.5 A | | 1.0 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = -25 V, f = 1.0 MHz, see fig. 10 | | - | 350 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 100 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 30 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = -10 V | $I_D$ = -4.0 A, $V_{DS}$ = -160 V, see fig. 11 and 18 [b] | - | - | 22 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 12 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 10 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -100 V, $I_D$ = -1.5 A, $R_G$ = 50 Ω, $R_D$ = 67 Ω, see fig. 17 [b] | | - | 15 | - | ns |
| Rise Time | $t_r$ | | | - | 25 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 20 | - | |
| Fall Time | $t_f$ | | | - | 15 | - | |
| Gate Input Resistance | $R_g$ | f = 1 MHz, open drain | | 0.9 | - | 5.7 | Ω |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact  | | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | -3.5 | A |
| Pulsed Diode Forward Current [a] | $I_{SM}$ | | | - | - | -14 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = -3.5 A, $V_{GS}$ = 0 V [b] | | - | - | -7.0 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = -3.5 A, dI/dt = 100 A/µs [b] | | - | 300 | 450 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | - | 1.9 | 2.9 | nC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %



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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

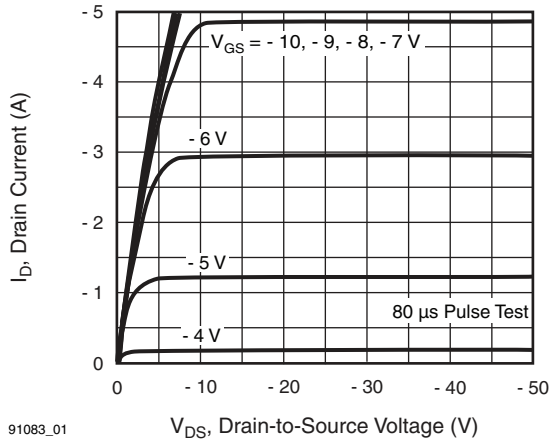



**Fig. 1 - Typical Output Characteristics**

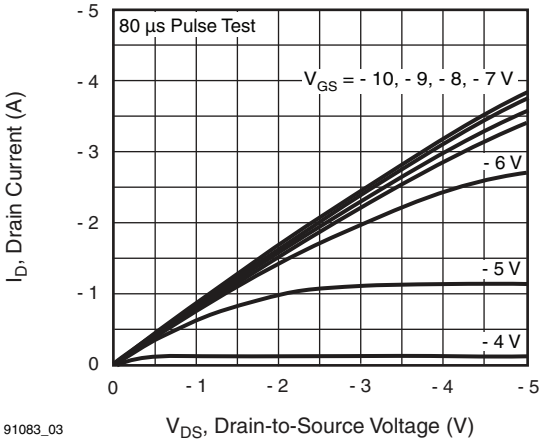



**Fig. 3 - Typical Saturation Characteristics**

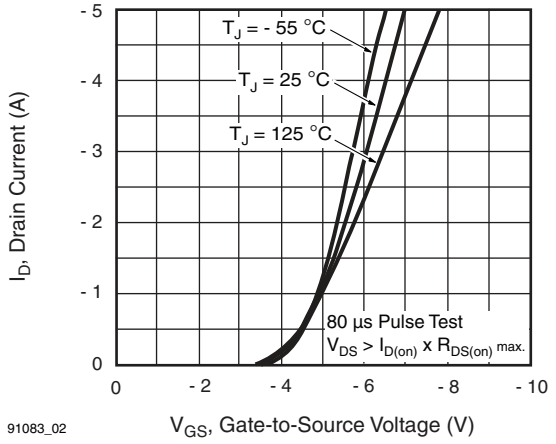



**Fig. 2 - Typical Transfer Characteristics**

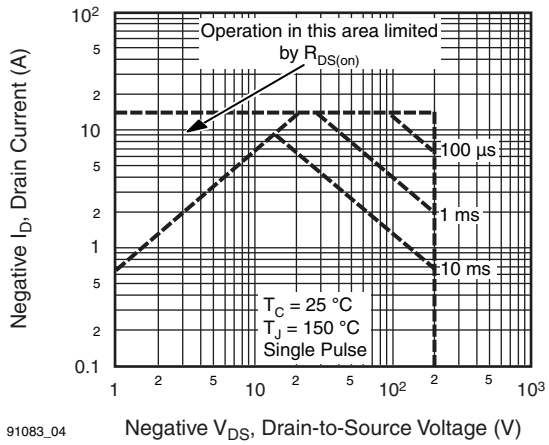



**Fig. 4 - Maximum Safe Operating Area**

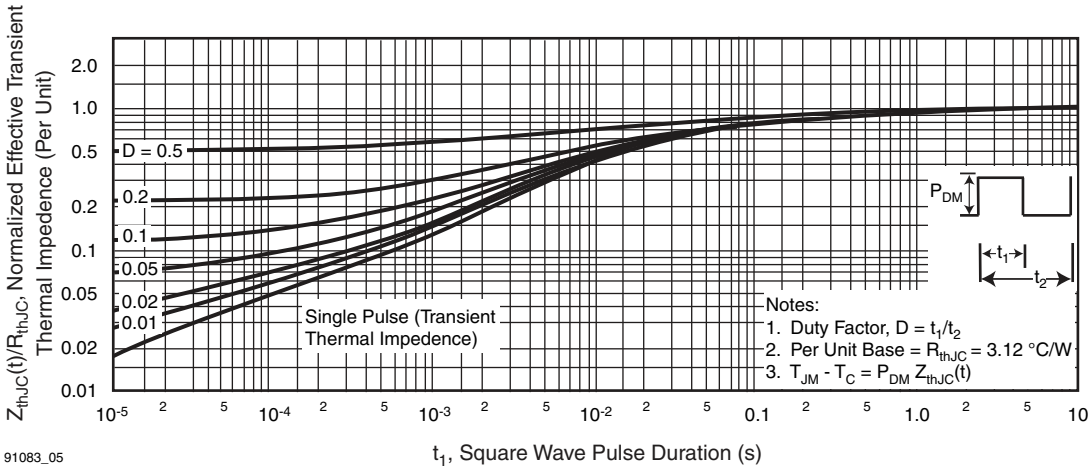



**Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration**


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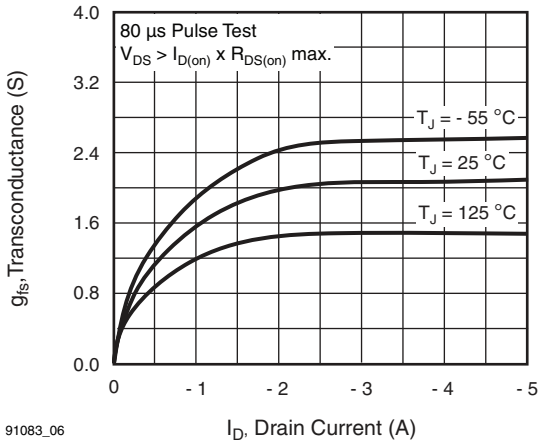



Fig. 6 - Typical Transconductance vs. Drain Current

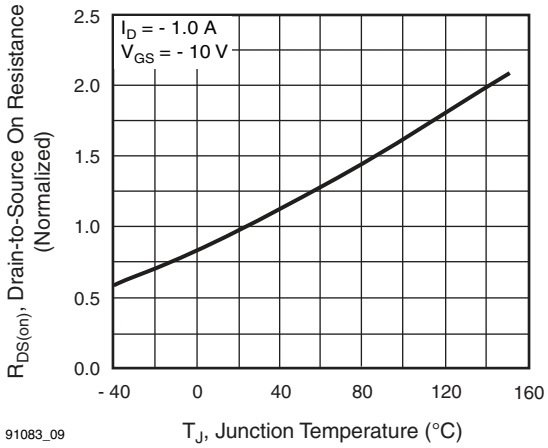



Fig. 9 - Normalized On-Resistance vs. Temperature

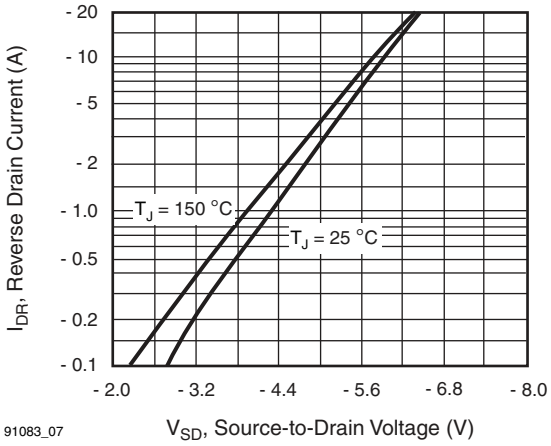



Fig. 7 - Typical Source-Drain Diode Forward Voltage

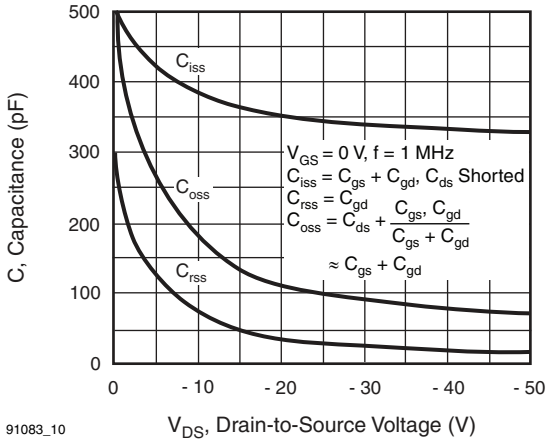



Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

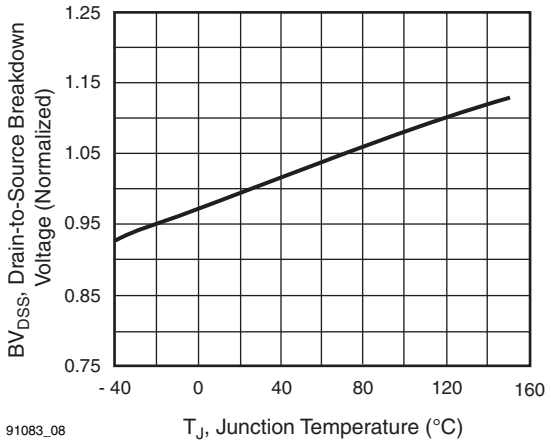



Fig. 8 - Breakdown Voltage vs. Temperature

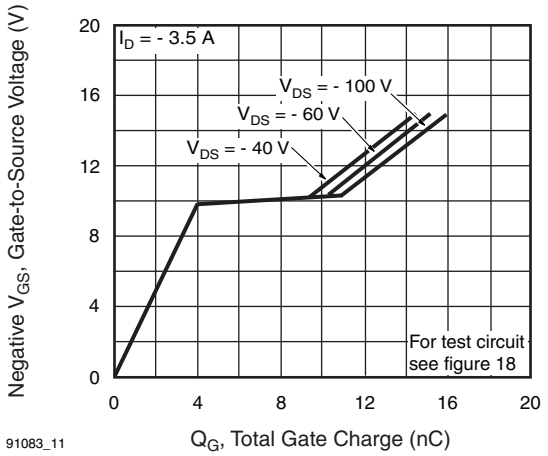



Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage


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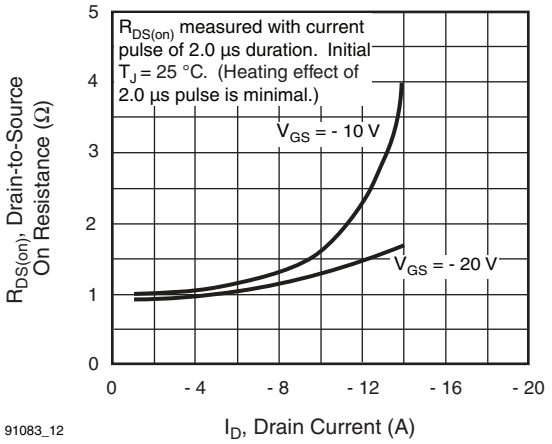



**Fig. 12 - Typical On-Resistance vs. Drain Current**

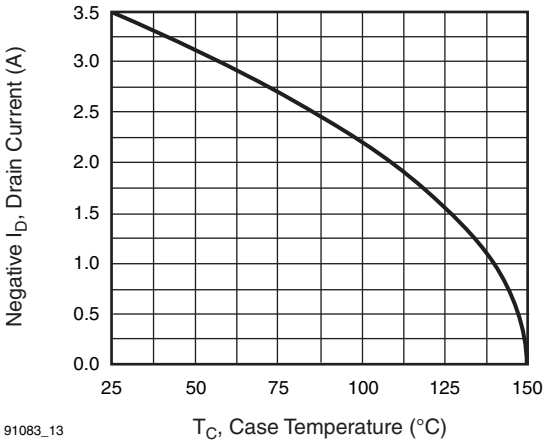



**Fig. 13 - Maximum Drain Current vs. Case Temperature**

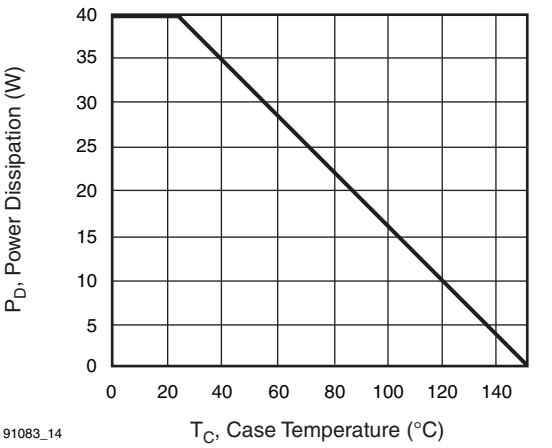



**Fig. 14 - Power vs. Temperature Derating Curve**

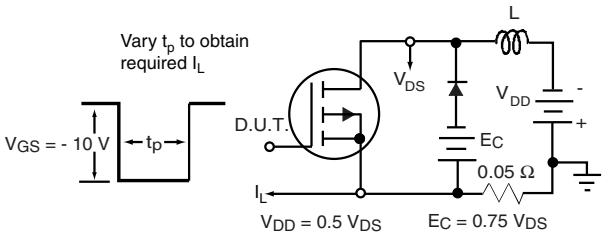



**Fig. 15 - Clamped Inductive Test Circuit**

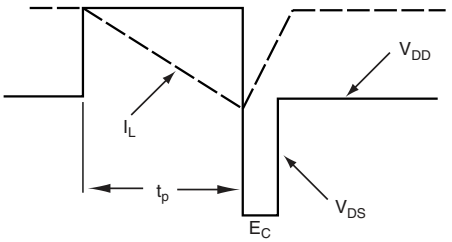



**Fig. 16 - Clamped Inductive Waveforms**

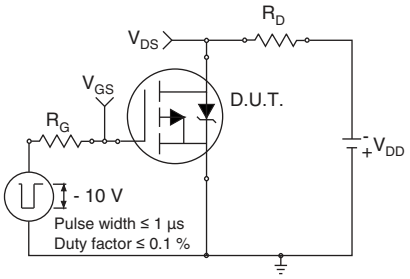



**Fig. 17a - Switching Time Test Circuit**

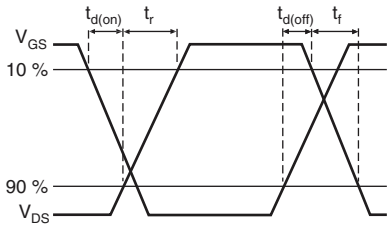



**Fig. 17b - Switching Time Waveforms**


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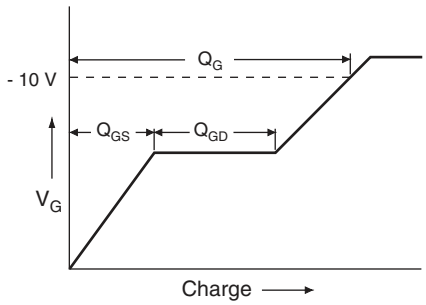



**Fig. 18a - Basic Gate Charge Waveform**

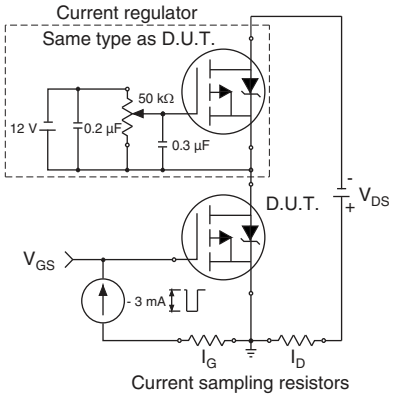
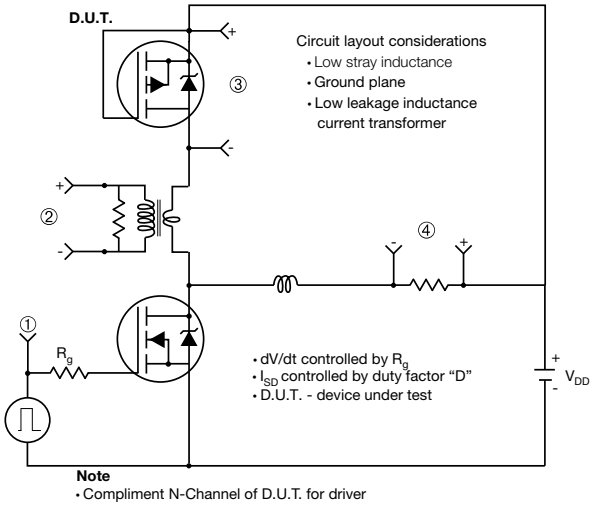



**Fig. 18b - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**



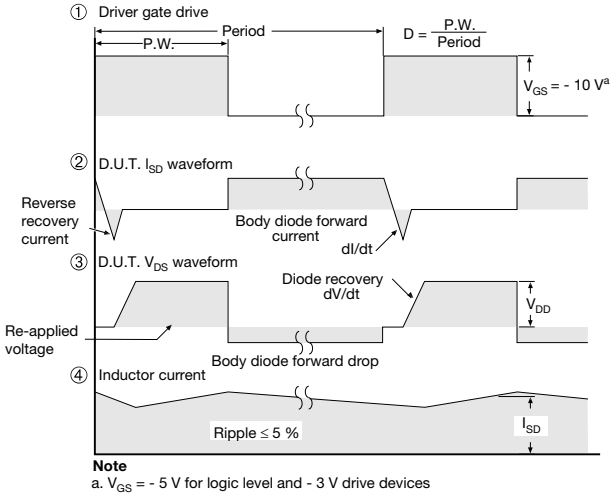
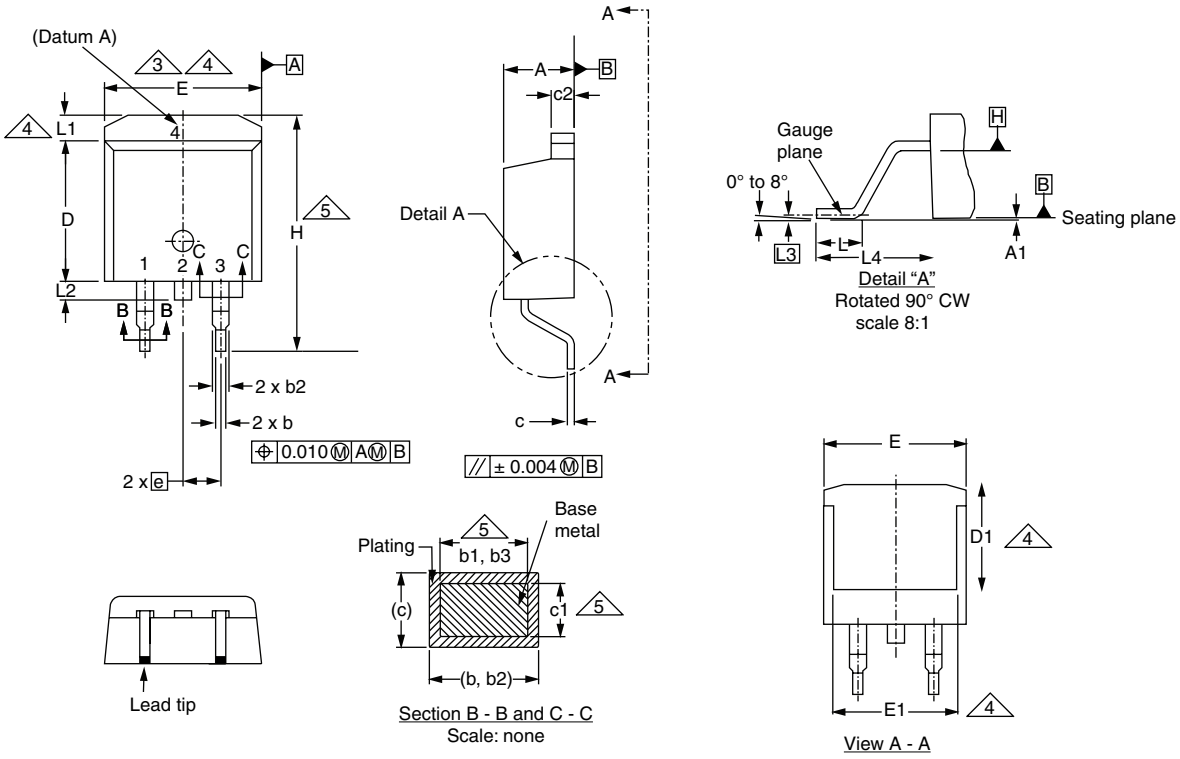




**Fig. 19 - For P-Channel**

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## TO-263AB (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

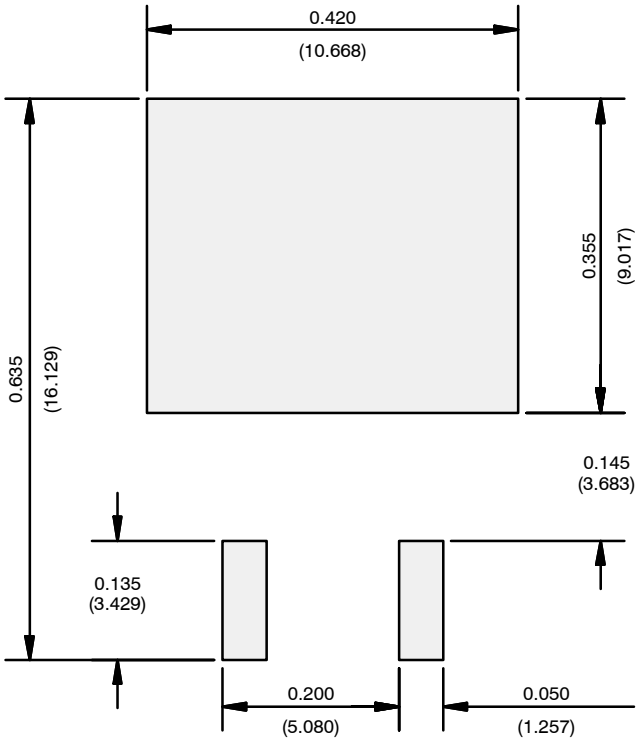
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

## RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

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