RAA214020

Ultra Low Noise, High PSRR, LDO

The RAA214020 is an ultra-low noise, high-PSRR, low-dropout voltage regulator. The LDO operates from an input voltage range of 2.7V to 5.5V and can source a maximum 2A load. The output is adjustable with external feedback resistors anywhere from 0.9V up to 5.5V-$V_{DROPOUT}$.

The RAA214020 has a low output noise of 6.3µV_{RMS} typical and high PSRR which makes it well-suited for post-regulation in low-noise applications.

The operating quiescent current is typically 195µA and drops to a couple nanoamps typical at room temperature when in shutdown making it great for portable applications.

The LDO features ±1.5% output voltage accuracy (over line, load, and temperature), input UVLO with hysteresis, enable control, internal current limit, thermal shutdown protection with hysteresis, power-good indication, and fast start-up.

The LDO is stable with a minimum 22µF ceramic output capacitor and is available in a 10 Ld 3mmx3mm DFN package great for compact system boards.

Features

- Input Voltage Range: 2.7V to 5.5V
- Max Output Current: 2A
- Max Dropout Voltage: 540mV at 2A and 3.3 V_{OUT}
- Low RMS output noise: 6.3µV_{RMS} (10Hz to 100kHz)
- Output Voltage Adjustable: 0.9V to 5.5V-$V_{DROPOUT}$
- Noise Spectral Density:
  - 184nV/√Hz at 10Hz
  - 79nV/√Hz at 10kHz
- High PSRR for $V_{HEADROOM}$ = 1.7V:
  - 100kHz: 64dB at 2A and 77dB at 500mA
  - 1MHz: 50dB at 2A and 55dB at 500mA
- Output Voltage Accuracy: ±1.5% over line, load, and temperature
- Fast start-up: 200µs at $V_{HEADROOM}$ = 3.7V
- Typical shutdown current: 200nA at 125°C
- Overvoltage indication, and overcurrent and over-temperature fault protection

Applications

- High Speed Analog: VCO, ADC, DAC, LVDS
- Clock and Timing
- RF and Wireless
- IoT and Smart Utilities
- 4G and 5G Telecom

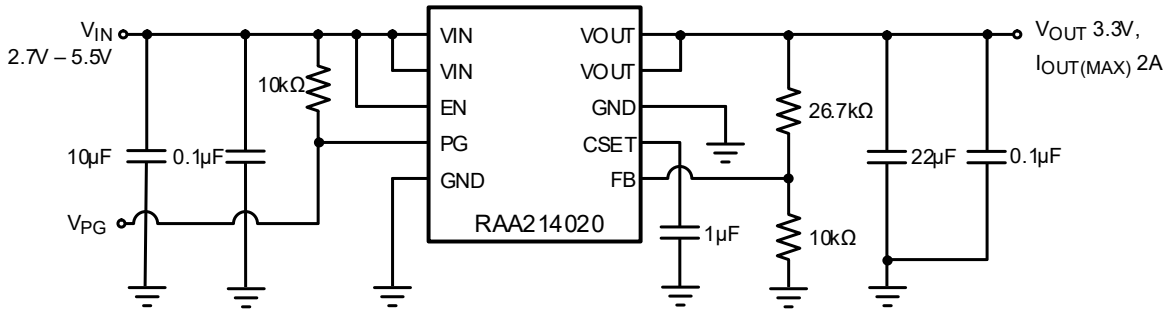


Figure 1. Typical Application Circuit

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1. Overview

1.1 Block Diagram

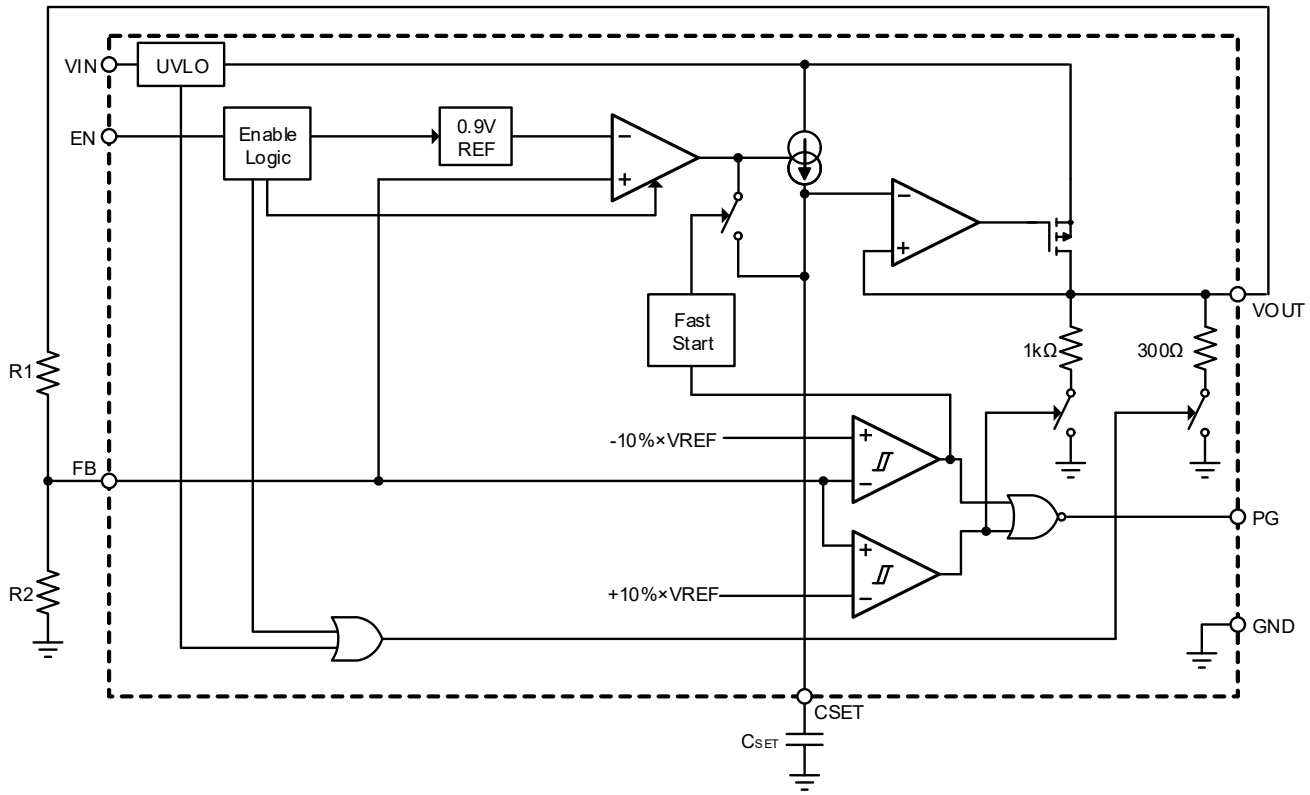
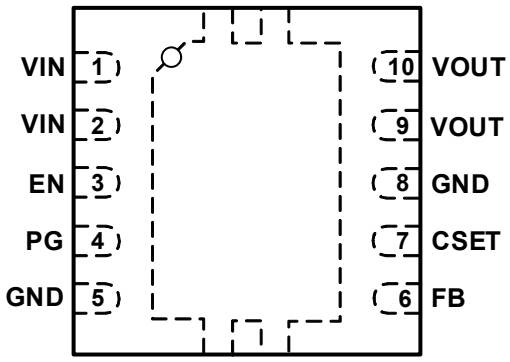


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2	VIN	VIN are the input voltage pins that supply power to the regulator. The RAA214020 requires a minimum ceramic bypass capacitor of 10µF.
3	EN	EN is the ENABLE pin. Setting this pin LOW disables the LDO and setting it HIGH enables the LDO. **IMPORTANT:** This pin should not be left floating. Instead, tie it to the VIN pins for automatic enabling.
4	PG	PG is the power-good pin. It is an open-drain logic output that can monitor the output voltage. This pin is OPEN when VOUT is within 90% and 110% of its final value. When the output voltage is outside of this range, the pin pulls LOW, indicating a fault is detected. If this pin is used, Renesas recommends tying this pin HIGH with a 10kΩ - 100kΩ pull-up resistor to ensure a proper logic HIGH level. If the pin is not being used, this pin can be left floating.
5	GND	GND is the ground pin. This pin must be tied to ground.
6	FB	FB is the voltage feed back pin. The FB pin is internally set to 0.9V (±1.5%) through the band gap circuitry. The external voltage divider formed around this pin sets the LDO output voltage. See Adjusting the Output Voltage Using External Feedback Resistors for more information on setting the output voltage
7	CSET	CSET pin is the noise reduction pin. To optimize the output noise and PSRR performance, connect a 1µF capacitor as close as possible between this pin and ground. Larger capacitor values can control the output voltage start-up time.
8	GND	GND is the ground pin. Pin must be tied to ground.
9, 10	VOUT	VOUT are the output voltage pins that supply power to the load. For stable operation across the full temperature range, input range, output range, and load extremes, a minimum 22µF capacitor is required from VOUT to GND.
EPAD		EPAD is the exposed pad on the bottom of the package. To ensure proper electrical and thermal performance, solder the exposed pad to the PCB ground plane and tie it directly to the ground Pin 5 and Pin 8. See Guidelines for more layout guidelines for this pin.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN, VOUT		+6.5	V
EN, PG, FB, CSET		+6.5	V
All Other Pins	GND - 0.3	V_{CC} - 0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	3		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
10 Ld 3x3 DFN Package	32	9

1. θ_{JA} was measured in free air with the component mounted on a 4-layer FR-4 PCB (3in x 3in) with 2oz Cu top layer traces and two 1oz Cu buried planes (3inx3in each) with 6 thermal vias underneath the component thermal e-pad that connects to the thermal planes.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{IN}	2.7	5.5	V
Ambient Temperature	-40	+125	°C
Output Voltage	0.9	V_{IN}-V_{DO}	V

3.4 Electrical Specifications

Default test conditions unless otherwise specified: T_J = - 40°C to +125°C, V_{IN} = V_{OUT} + 0.5V or 2.7V whichever is greater, C_{IN} = 10µF, C_{OUT} = 22µF, unless otherwise noted. Typical values are at T_J = +25°C. **Boldface limits apply across the operating temperature range (-40°C to +125°C).**

Parameters	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
Power Supply						
Input Voltage Range	V_{IN}		**2.7**		**5.5**	V
Input Supply UVLO	$V_{UVLO(IN)}$	V_{IN} Rising	**2.2**	2.3	**2.45**	V
Input Supply UVLO Hysteresis	$V_{HYS(IN)}$		**0.03**	0.23	**0.3**	V
Output Current	I_{OUT}				**2.0**	A
V_{IN} Quiescent Current	I_Q (V_{IN})	V_{OUT} = 3.3V, V_{IN} = 5V	**50**	195	**300**	µA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_J = +125°C		200		nA
Output						
Output Voltage Range	V_{OUT}	V_{IN} = 2.7V to 5.5V	**0.9**		**VIN-VDO**	V
FB voltage	V_{FB}		**0.8865**	0.90	**0.9135**	V
Output Voltage Accuracy		Initial at I_{OUT} = 10mA, T_J = +25°C	-1.0		1.0	%
		Initial at I_{OUT} = 10mA to 2A	**-1.5**		**1.5**	%
Line Regulation		V_{IN} = 2.7V to 5.5V, I_{OUT} = 1mA		0.1		%/V
Load Regulation		I_{OUT} = 1mA to 2A		1		mV
Dropout Voltage	V_{DO}	V_{IN} = 3.3V, I_{OUT} = 2A		340	**540**	mV
Internal Current Limit	ILIM	V_{IN} = 2.7V to 5.5V, V_{OUT} = 0V		3.3		A
Start-Up Time		V_{IN} = 5.5V, V_{OUT} = 1.8V, I_{OUT} = 2A, C_{SET} = 1µF, C_{OUT} = 22µF		200		µs
Thermal Shutdown	T_{SHDN}	Rising		155		°C
Thermal Shutdown Hysteresis				10		°C
Noise						
Output Noise Spectral Density		I_{OUT} = 2.0A, Frequency = 10Hz, C_{OUT} = 22µF, C_{SET} = 1µF		184		nV/√(Hz)
		I_{OUT} = 2.0A, Frequency = 100Hz, C_{OUT} = 22µF, C_{SET} = 1µF		79		nV/√(Hz)
		I_{OUT} = 2.0A, Frequency = 1kHz, C_{OUT} = 22µF, C_{SET} = 1µF		34		nV/√(Hz)
		I_{OUT} = 2.0A, Frequency = 10kHz, C_{OUT} = 22µF, C_{SET} = 1µF		20		nV/√(Hz)
Output RMS Noise		I_{OUT} = 2.0A, Frequency = 10Hz to 100kHz, C_{OUT} = 22µF, C_{SET} = 1µF		6.3		µV RMS

Default test conditions unless otherwise specified: T_J = - 40°C to +125°C, V_{IN} = V_{OUT} + 0.5V or 2.7V whichever is greater, C_{IN} = 10µF, C_{OUT} = 22µF, unless otherwise noted. Typical values are at T_J = +25°C. **Boldface limits apply across the operating temperature range (-40°C to +125°C). (Cont.)**

Parameters	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
PSRR						
PSRR	PSRR1	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{OUT} = 2A, C_{OUT} = 22µF, V_{IN} = 5V, V_{OUT} = 3.3V		81		dB
	PSRR2	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{OUT} = 2A, C_{OUT} = 22µF, V_{IN} = 5V, V_{OUT} = 3.3V		80		dB
	PSRR3	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{OUT} = 2A, C_{OUT} = 22µF, V_{IN} = 5V, V_{OUT} = 3.3V		64		dB
	PSRR4	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{OUT}= 2A, C_{OUT} = 22µF, V_{IN} = 5V, V_{OUT} = 3.3V		50		dB
EN Input Pin						
EN Input voltage threshold	EN_{VTH}		**1.2**	1.25	**1.33**	V
EN Threshold Hysteresis	EN_{HYS}		**0.035**	0.059	**0.1**	V
EN Leakage		V_{EN} = 5.5V		32	**100**	nA
PG Output Pin						
PG V_{OUT} Overvoltage	PG_{OV}	V_{OUT} Rising		8.2		%
PG V_{OUT} Undervoltage	PG_{UV}	V_{OUT} Falling		-11.5		%
PG Threshold Hysteresis OV	$PG_{HYST(OV)}$	For both OV Thresholds		1.2		%
PG Threshold Hysteresis UV	$PG_{HYST(UV)}$	For both UV Thresholds		-1.4		%
PG Delay		V_{OUT} Rising	**0.1**	0.17	**0.3**	µs
		V_{OUT} Falling	**0.8**	1.2	**2**	µs
PG VOL	PG_{VOL}	I_{PG} = 1mA		130	**250**	mV

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Graphs

4.1 Output Noise

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated.

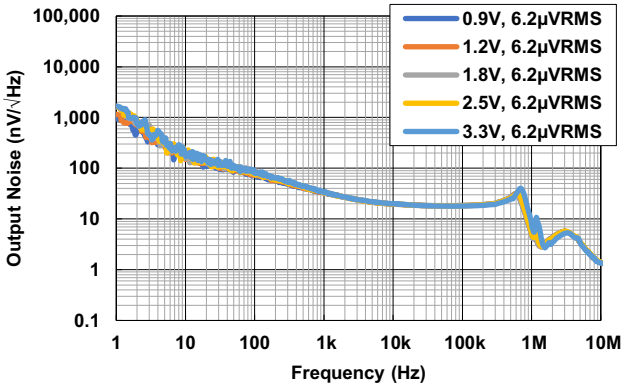


Figure 3. Output Noise vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 2V, I_{OUT} = 500mA)

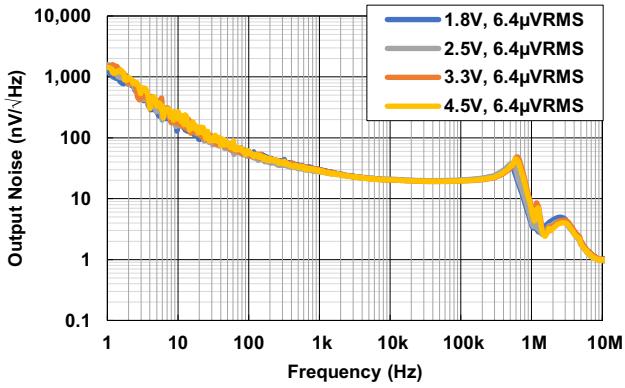


Figure 4. Output Noise vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 1V, I_{OUT} = 2A)

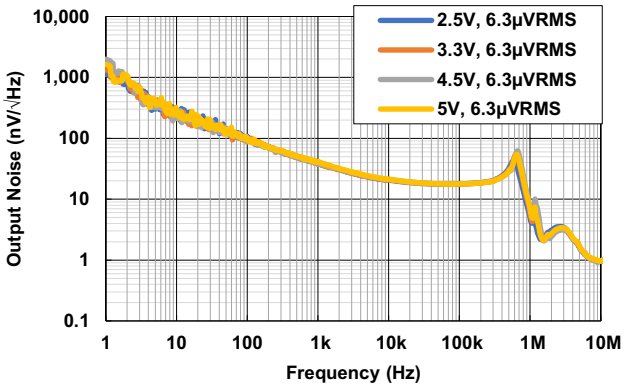


Figure 5. Output Noise vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 500mV, I_{OUT} = 500mA)

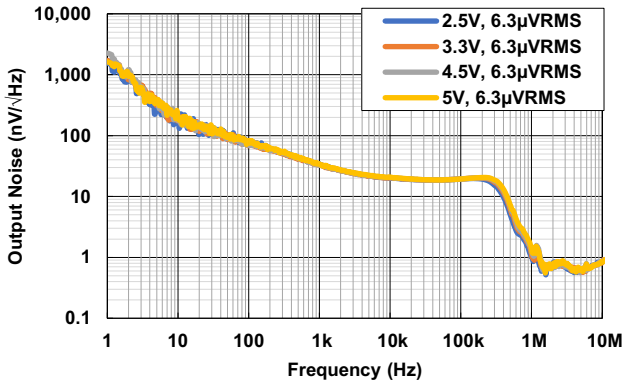


Figure 6. Output Noise vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 500mV, I_{OUT} = 2A)

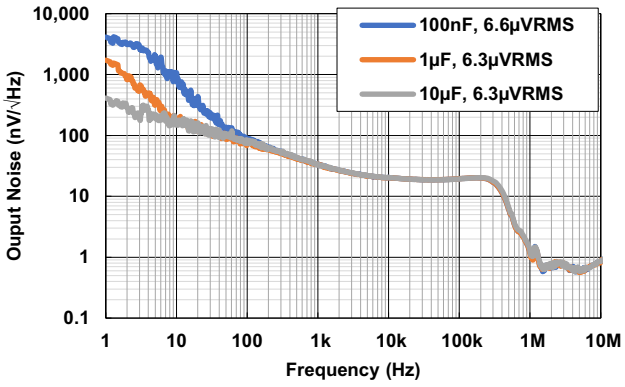


Figure 7. Output Noise vs Frequency for Various C_{SET} (V_{IN} = V_{OUT} + 500mV, I_{OUT} = 2A)

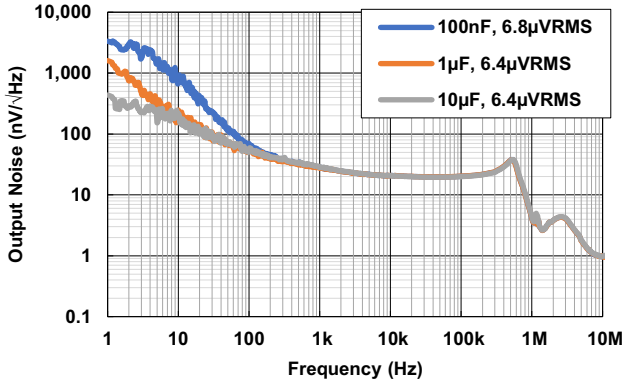


Figure 8. Output Noise vs Frequency for Various C_{SET} (V_{IN} = V_{OUT} + 1V, I_{OUT} = 2A)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

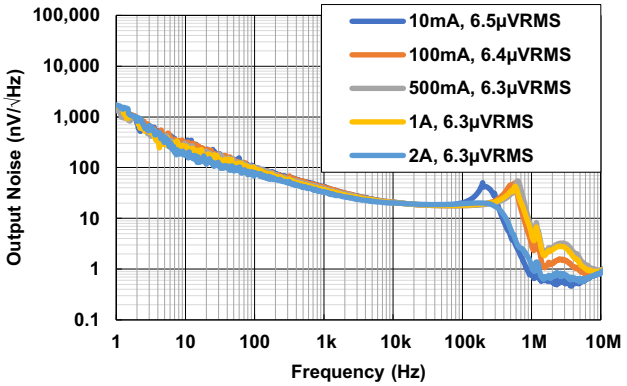


Figure 9. Output Noise vs Frequency for Various I_{OUT} (V_{IN} = V_{OUT} + 500mV, I_{OUT} = 2A)

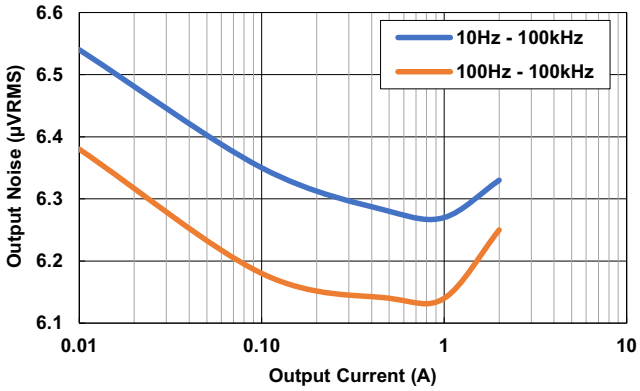


Figure 10. Integrated Output Noise vs I_{OUT} for Various Bandwidths (V_{IN} = V_{OUT} + 500mV, I_{OUT} = 2A)

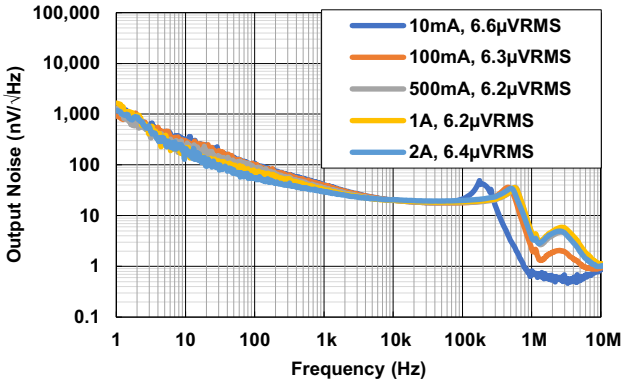


Figure 11. Output Noise vs Frequency for Various I_{OUT} (V_{IN} = V_{OUT} + 1V, I_{OUT} = 2A)

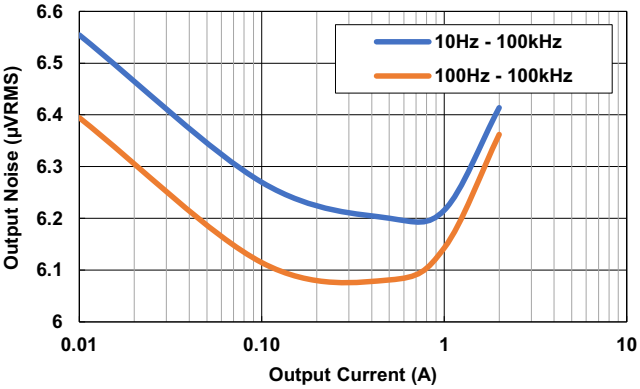


Figure 12. Integrated Output Noise vs I_{OUT} for Various Bandwidths (V_{IN} = V_{OUT} + 1V, I_{OUT} = 2A)

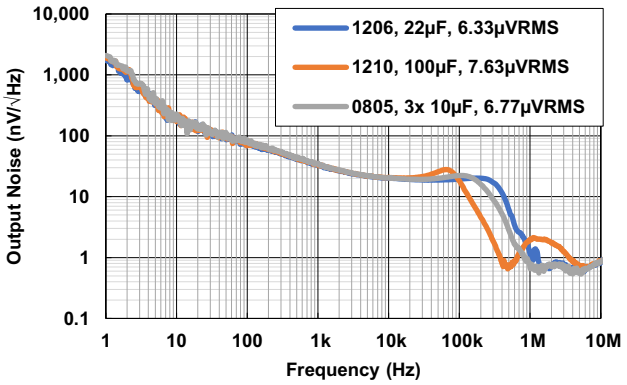


Figure 13. Output Noise vs Frequency for Various C_{OUT} (V_{IN} = V_{OUT} + 500mV, I_{OUT} = 2A)

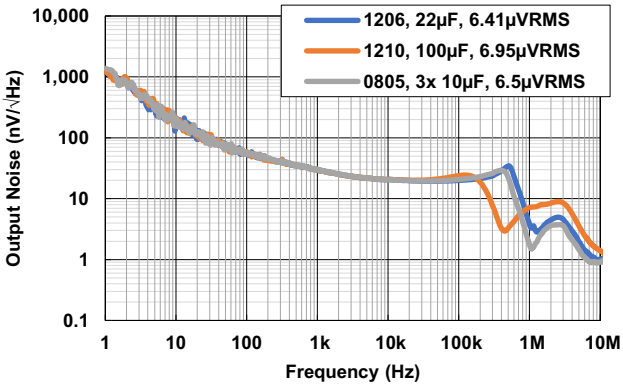


Figure 14. Output Noise vs Frequency for Various C_{OUT} (V_{IN} = V_{OUT} + 1V, I_{OUT} = 2A)

4.2 PSRR

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated.

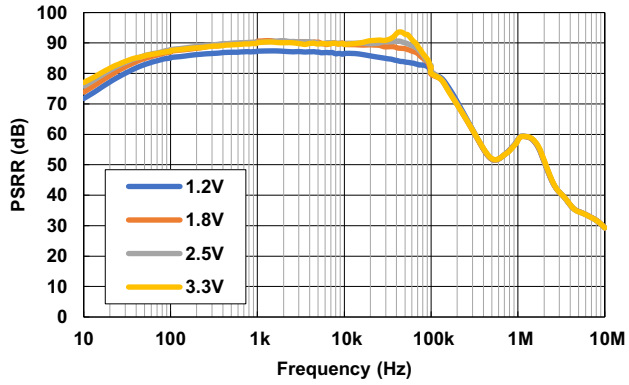


Figure 15. PSRR vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 2V, I_{OUT} = 500mA)

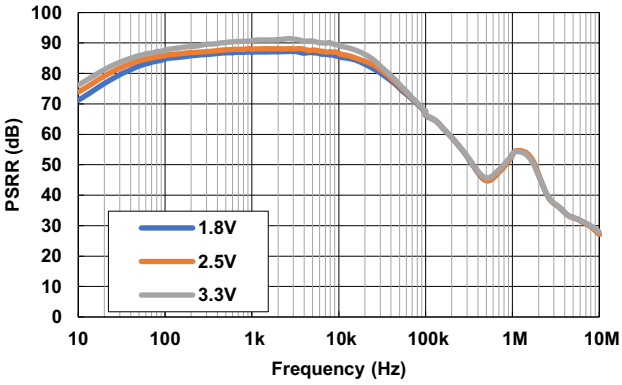


Figure 16. PSRR vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 1.2V, I_{OUT} = 500mA)

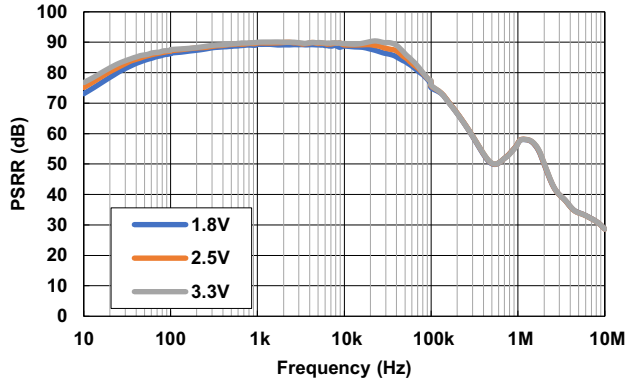


Figure 17. PSRR vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 1.7V, I_{OUT} = 500mA)

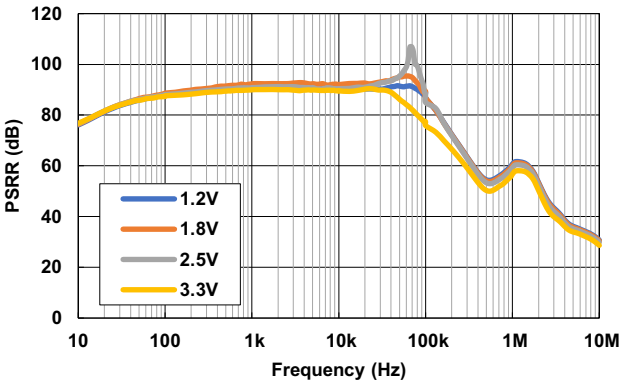


Figure 18. PSRR vs Frequency for Various V_{OUT} (V_{IN} = 5V, I_{OUT} = 500mA)

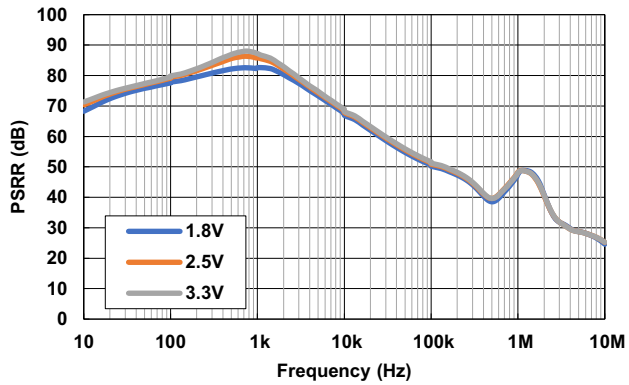


Figure 19. PSRR vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 1.2V, I_{OUT} = 2A)

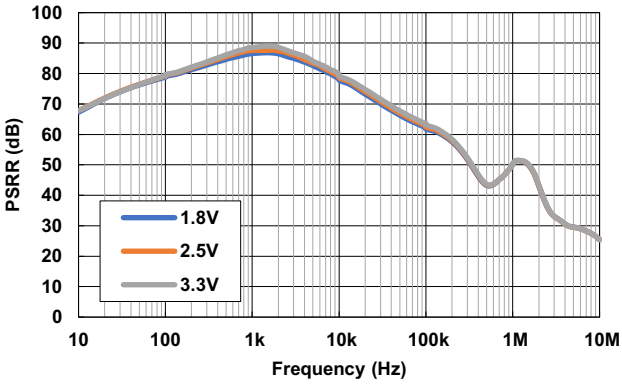


Figure 20. PSRR vs Frequency for Various V_{OUT} (V_{IN} = V_{OUT} + 1.7V, I_{OUT} = 2A)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

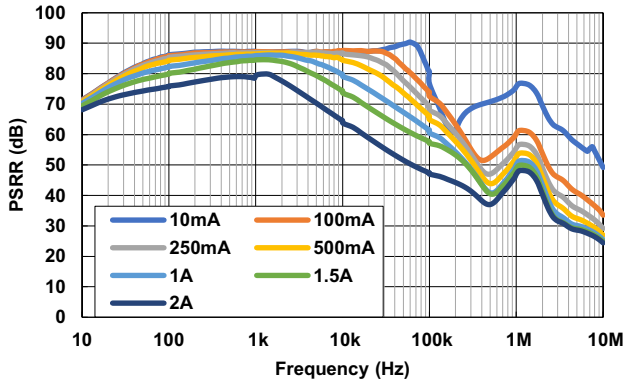


Figure 21. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 2.95V, V_{OUT} = 1.8V)

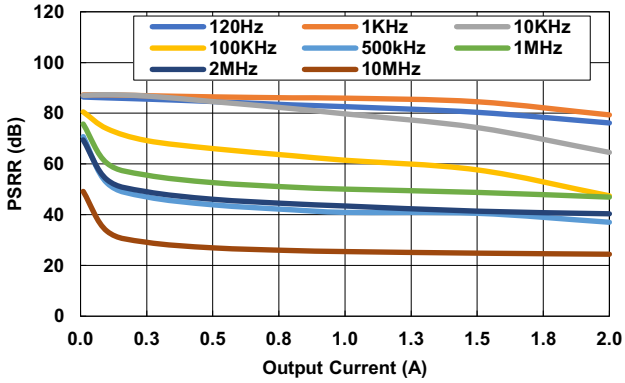


Figure 22. PSRR vs I_{OUT} for Various Frequencies (V_{IN} = 2.95V, V_{OUT} = 1.8V)

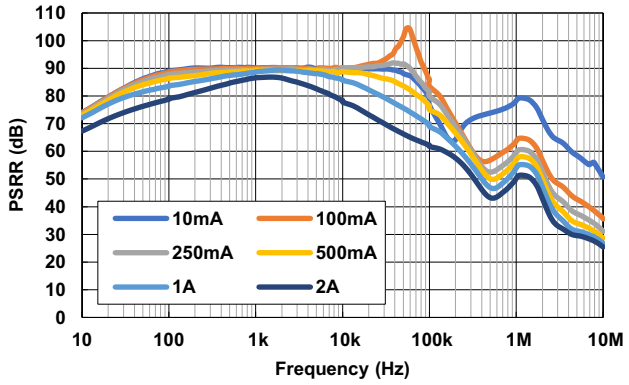


Figure 23. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 3.5V, V_{OUT} = 1.8V)

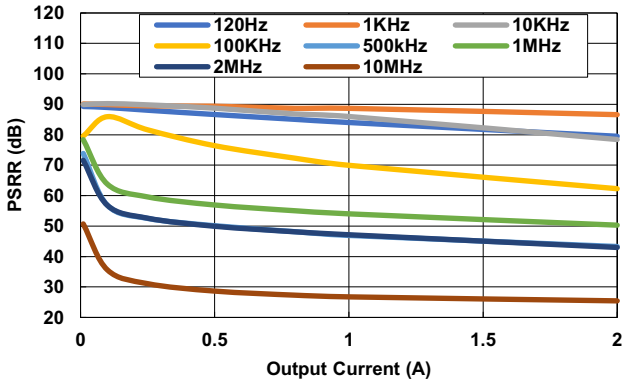


Figure 24. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 3.5V, V_{OUT} = 1.8V)

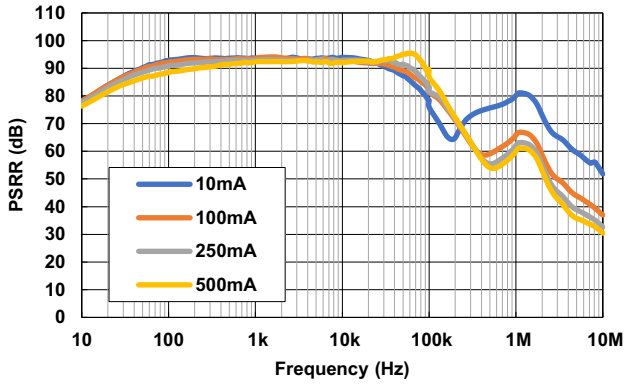


Figure 25. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 5V, V_{OUT} = 1.8V)

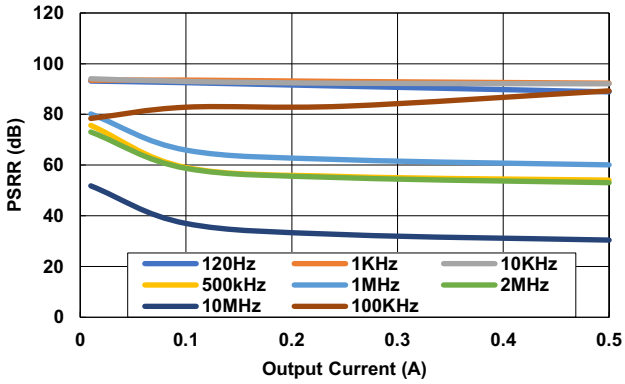


Figure 26. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 5V, V_{OUT} = 1.8V)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

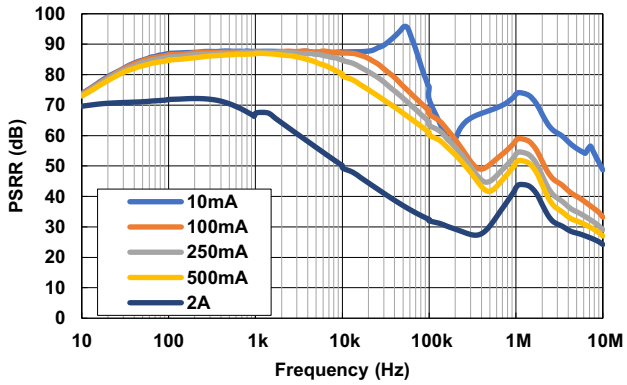


Figure 27. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 3.25V, V_{OUT} = 2.5V)

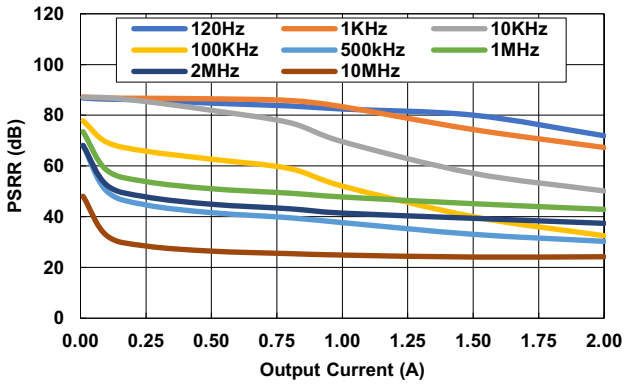


Figure 28. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 3.25V, V_{OUT} = 2.5V)

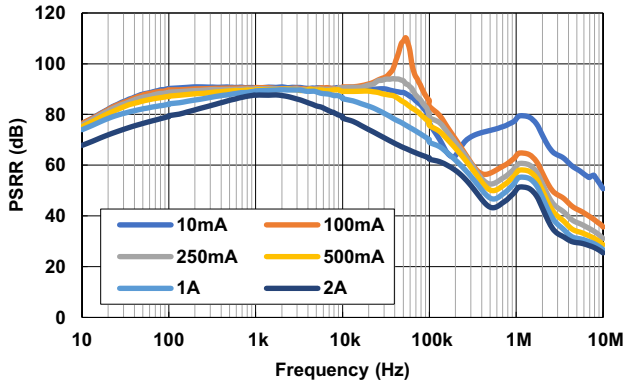


Figure 29. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 4.2V, V_{OUT} = 2.5V)

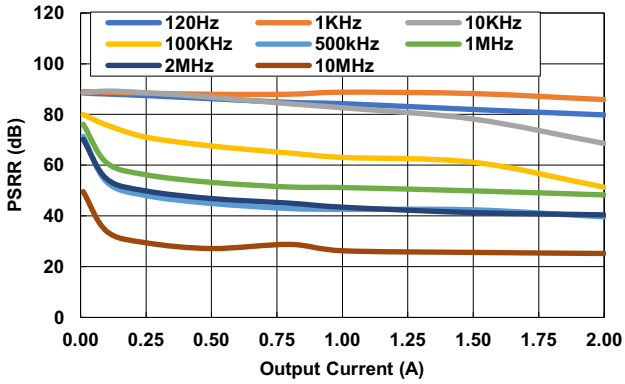


Figure 30. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 4.2V, V_{OUT} = 2.5V)

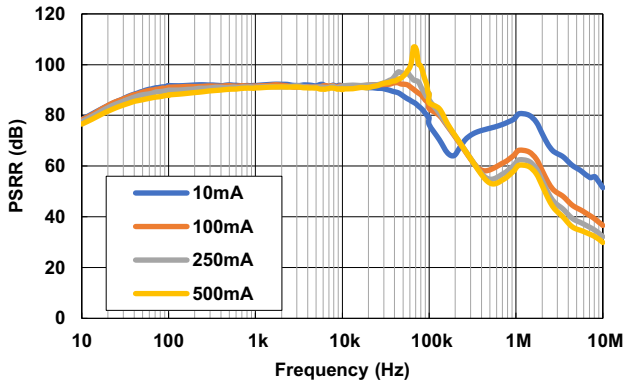


Figure 31. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 5V, V_{OUT} = 2.5V)

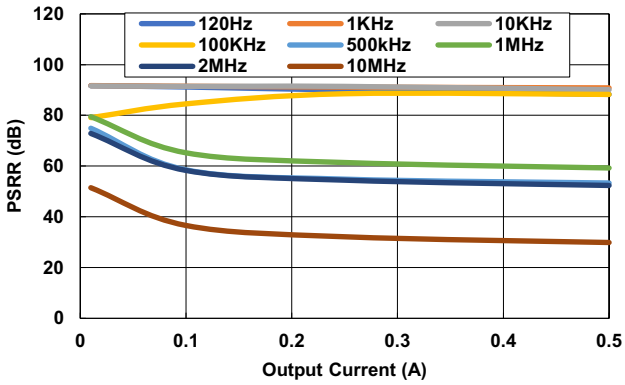


Figure 32. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 5V, V_{OUT} = 2.5V)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

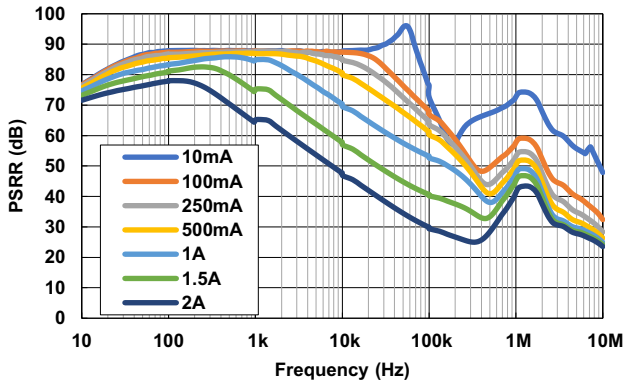


Figure 33. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 4V, V_{OUT} = 3.3V)

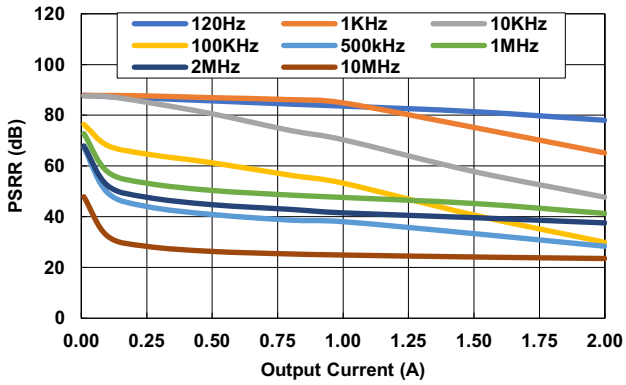


Figure 34. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 4V, V_{OUT} = 3.3V)

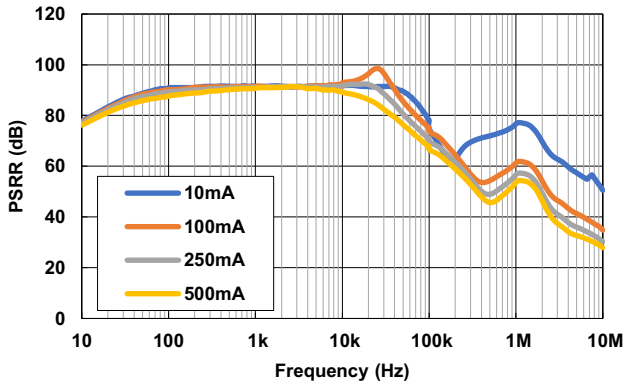


Figure 35. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 4.5V, V_{OUT} = 3.3V)

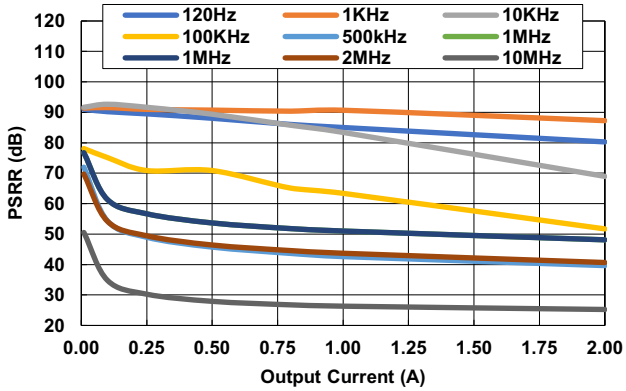


Figure 36. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 4.5V, V_{OUT} = 3.3V)

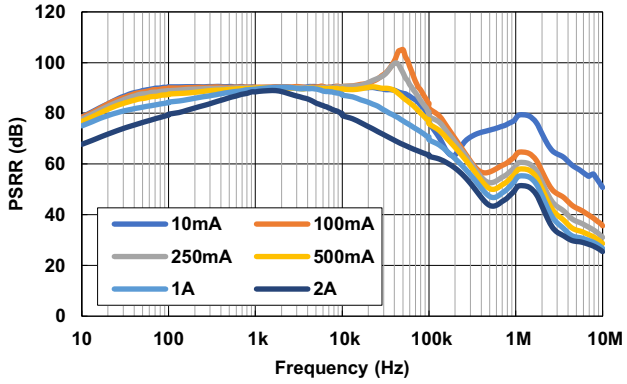


Figure 37. PSRR vs Frequency for Various I_{OUT} (V_{IN} = 5V, V_{OUT} = 3.3V)

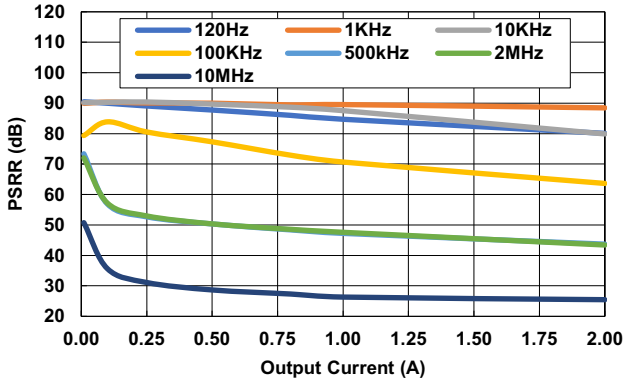


Figure 38. PSRR vs I_{OUT} Various Frequencies (V_{IN} = 5V, V_{OUT} = 3.3V)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

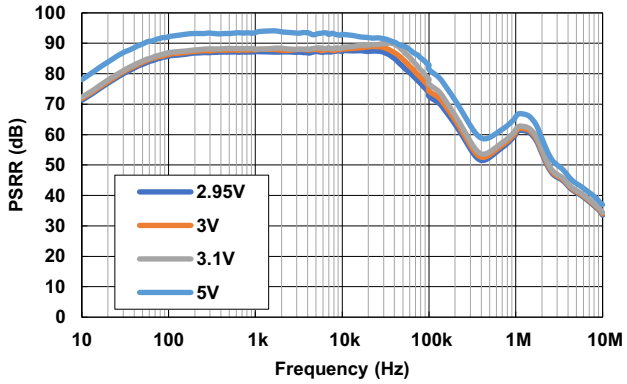


Figure 39. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 1.8V, I_{OUT} = 100mA)

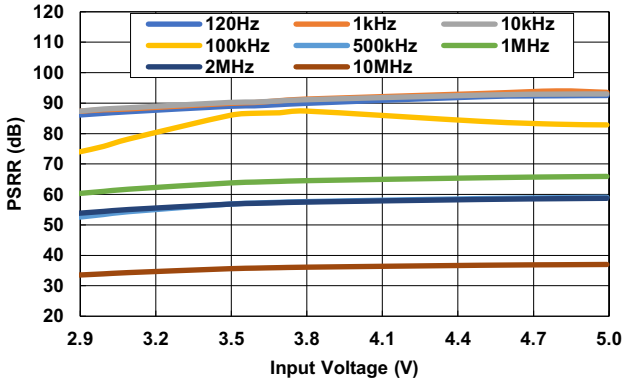


Figure 40. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 1.8V, I_{OUT} = 100mA)

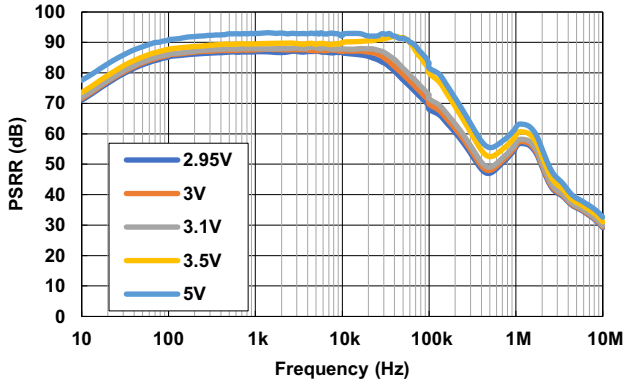


Figure 41. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 1.8V, I_{OUT} = 250mA)

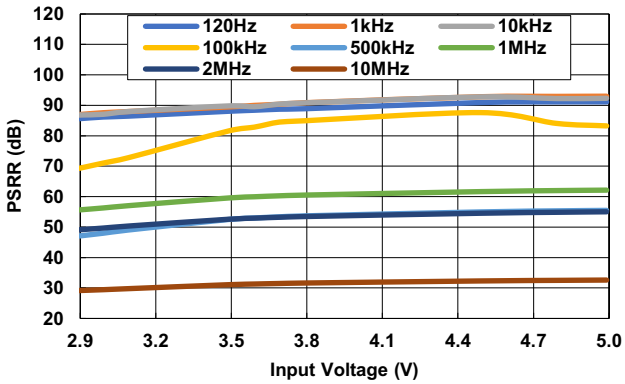


Figure 42. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 1.8V, I_{OUT} = 250mA)

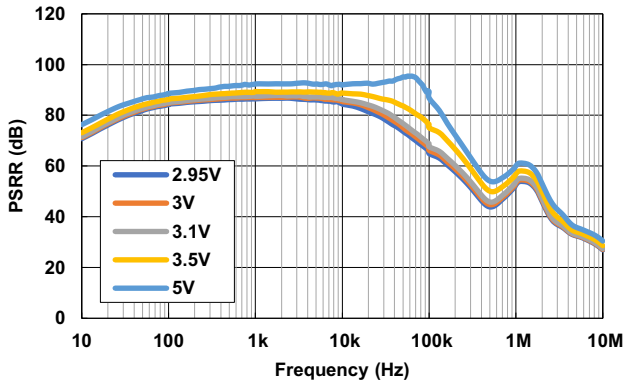


Figure 43. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 1.8V, I_{OUT} = 500mA)

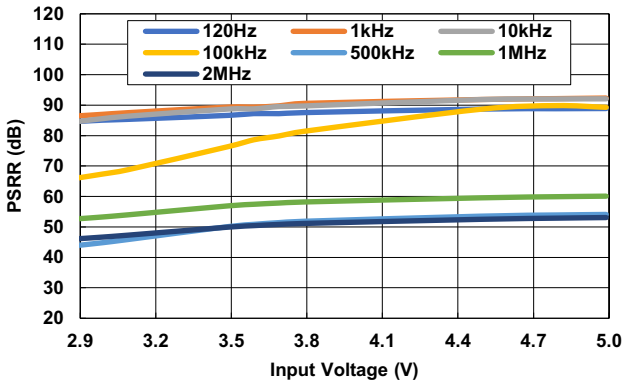


Figure 44. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 1.8V, I_{OUT} = 500mA)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

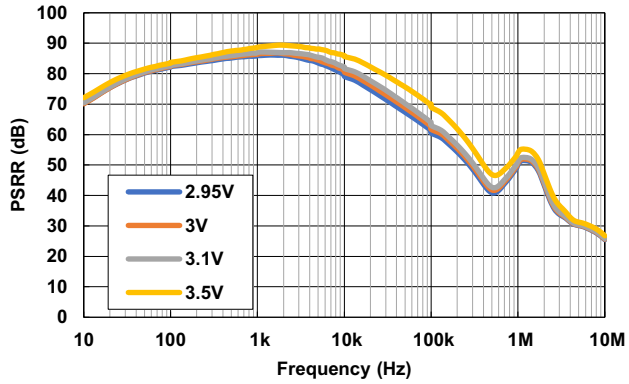


Figure 45. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 1.8V, I_{OUT} = 1A)

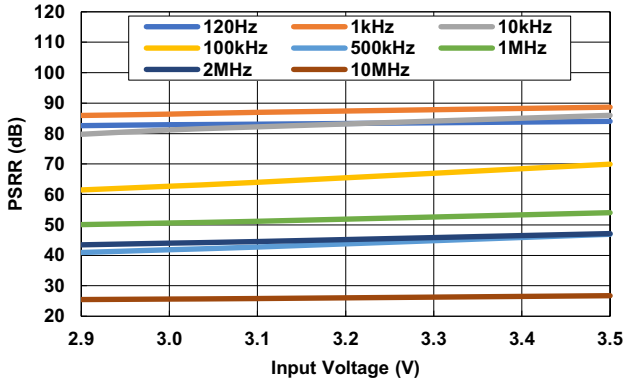


Figure 46. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 1.8V, I_{OUT} = 1A)

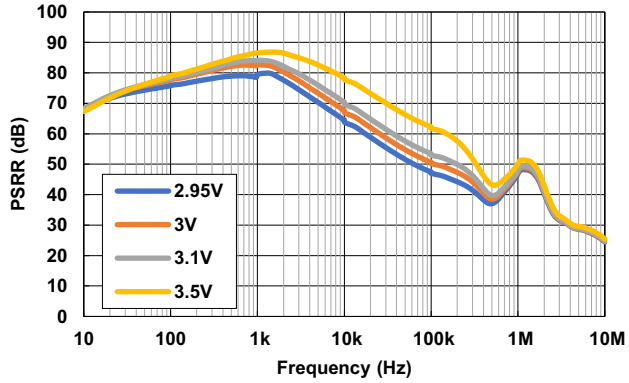


Figure 47. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 1.8V, I_{OUT} = 2A)

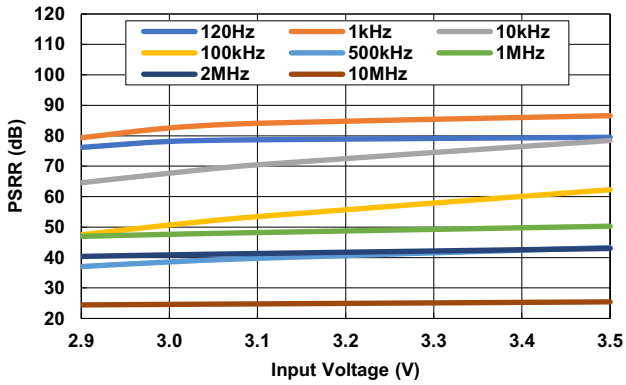


Figure 48. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 1.8V, I_{OUT} = 2A)

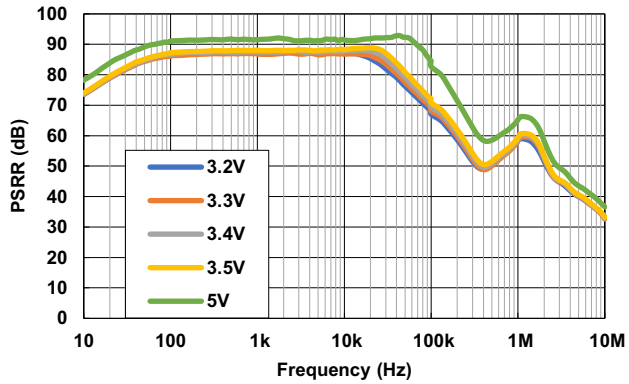


Figure 49. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 2.5V, I_{OUT} = 100mA)

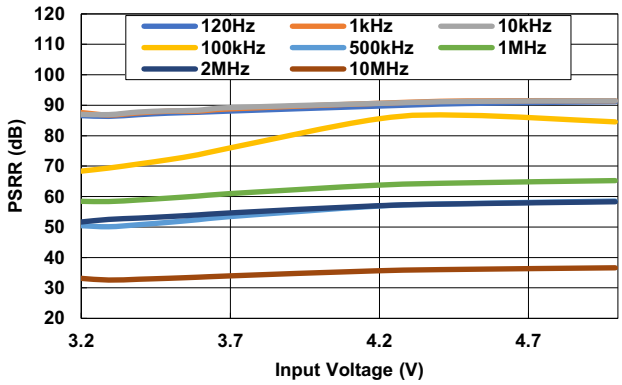


Figure 50. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 2.5V, I_{OUT} = 100mA)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

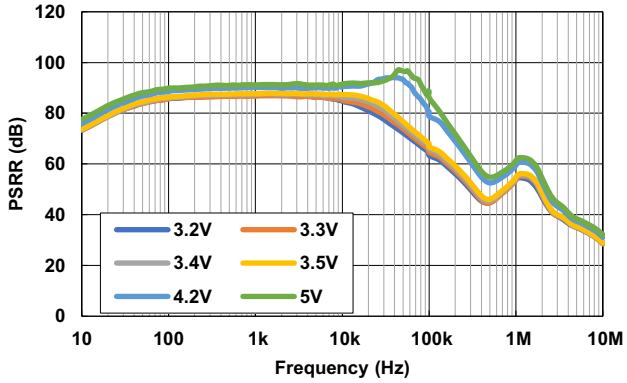


Figure 51. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 2.5V, I_{OUT} = 250mA)

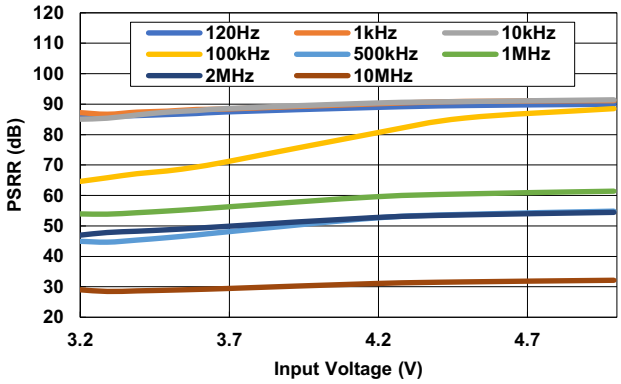


Figure 52. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 2.5V, I_{OUT} = 250mA)

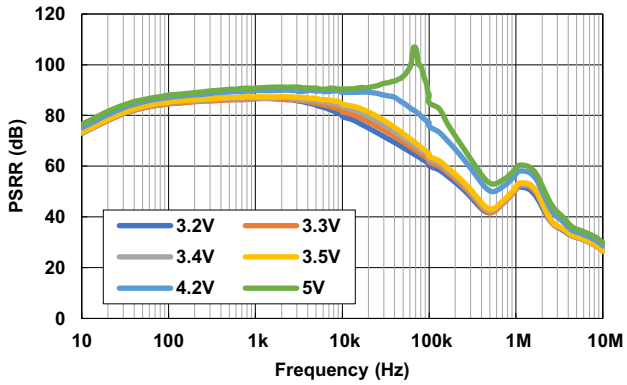


Figure 53. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 2.5V, I_{OUT} = 500mA)

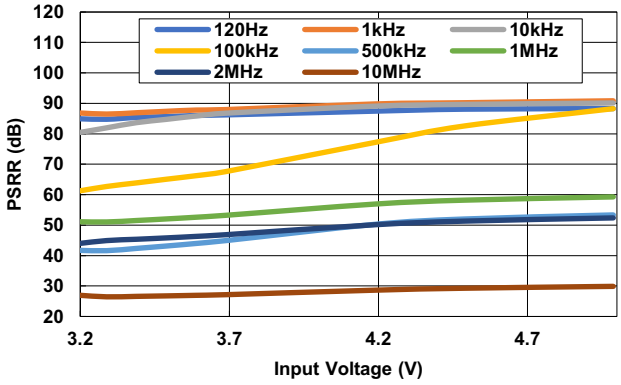


Figure 54. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 2.5V, I_{OUT} = 500mA)

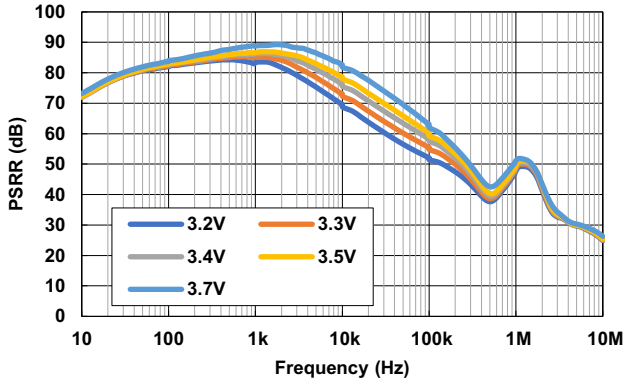


Figure 55. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 2.5V, I_{OUT} = 1A)

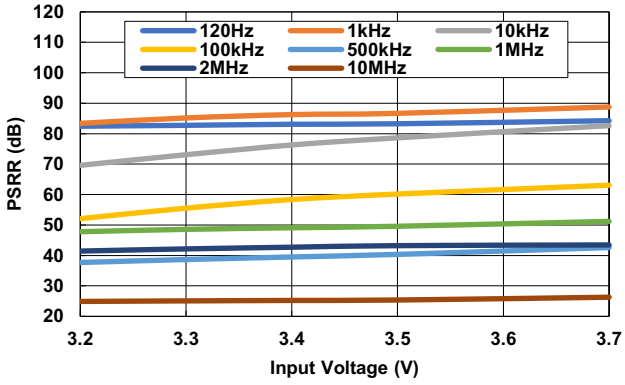


Figure 56. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 2.5V, I_{OUT} = 1A)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

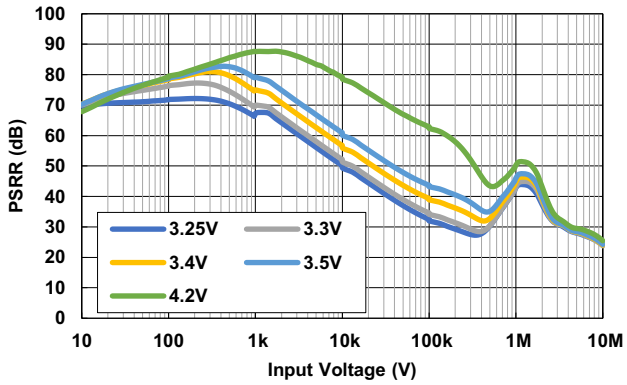


Figure 57. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 2.5V, I_{OUT} = 2A)

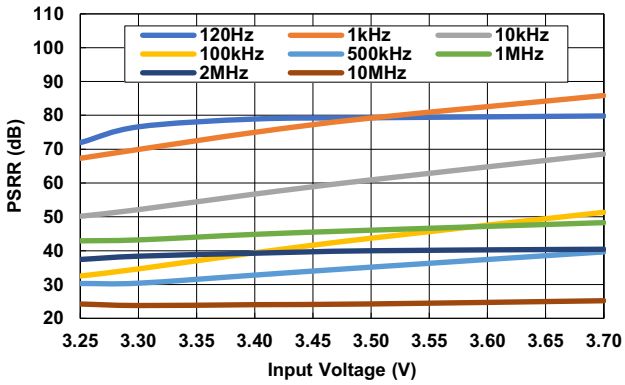


Figure 58. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 2.5V, I_{OUT} = 2A)

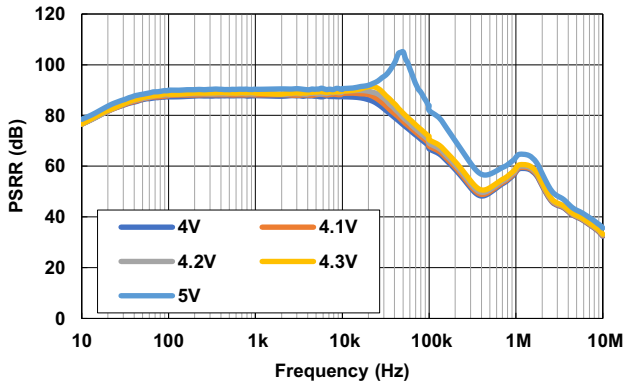


Figure 59. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 3.3V, I_{OUT} = 100mA)

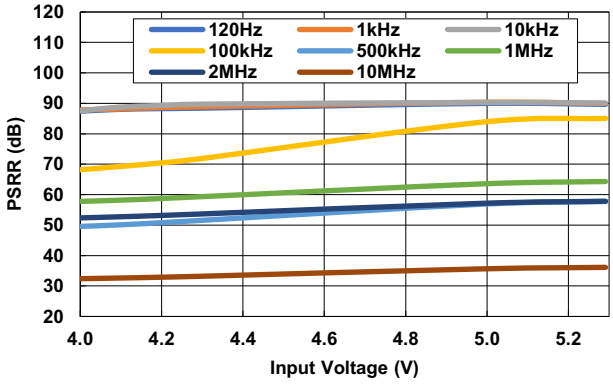


Figure 60. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 3.3V, I_{OUT} = 100mA)

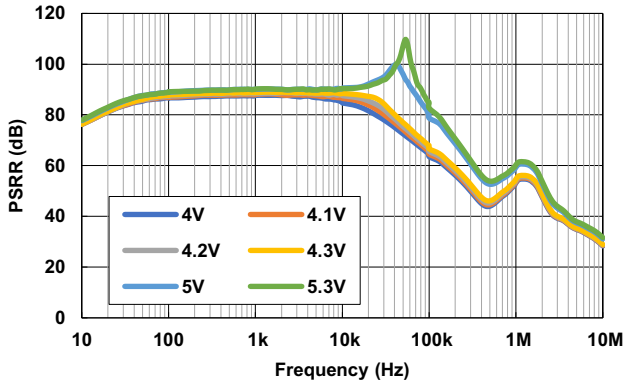


Figure 61. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 3.3V, I_{OUT} = 250mA)

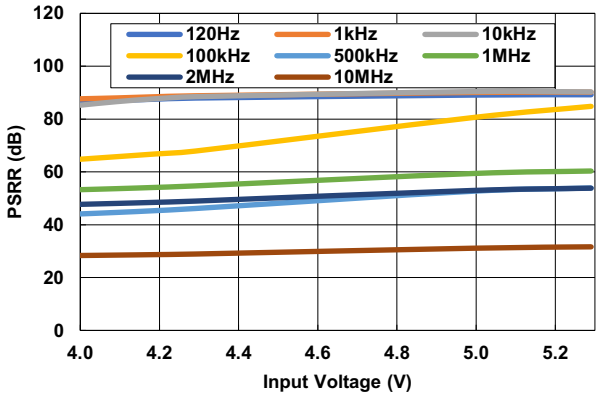


Figure 62. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 3.3V, I_{OUT} = 250mA)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

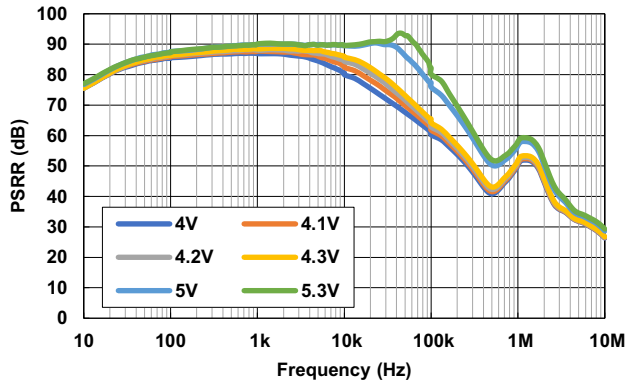


Figure 63. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 3.3V, I_{OUT} = 500mA)

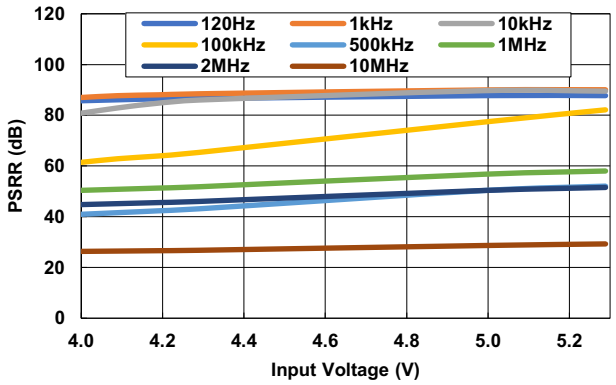


Figure 64. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 3.3V, I_{OUT} = 500mA)

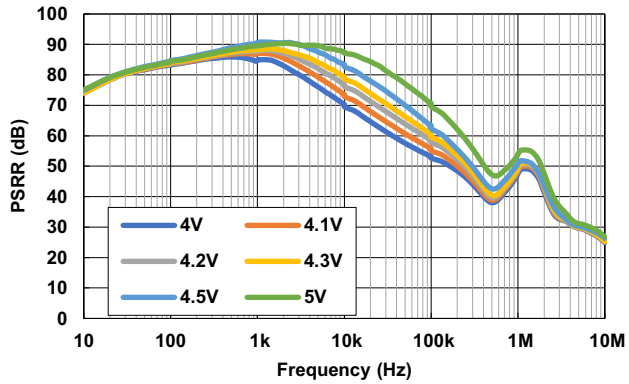


Figure 65. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 3.3V, I_{OUT} = 1A)

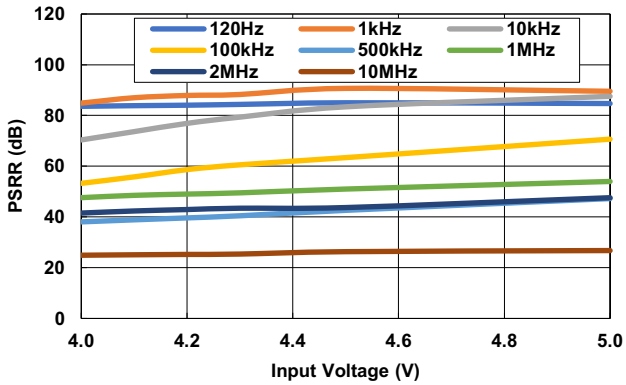


Figure 66. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 3.3V, I_{OUT} = 1A)

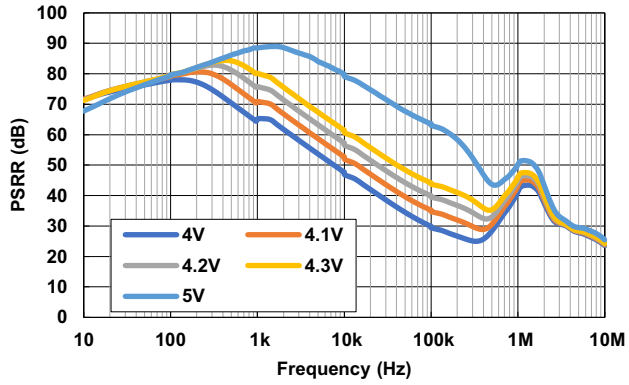


Figure 67. PSRR vs Frequency for Various V_{IN} (V_{OUT} = 3.3V, I_{OUT} = 2A)

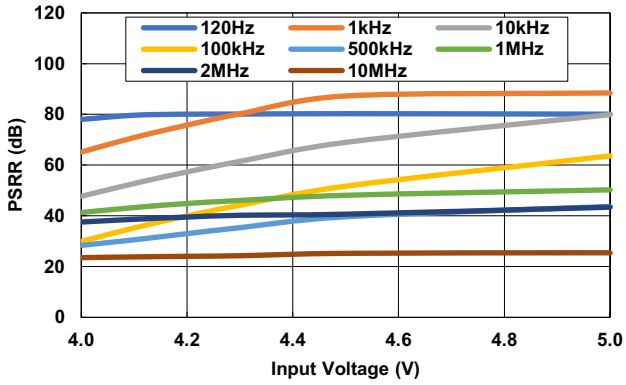


Figure 68. PSRR vs V_{IN} Various Frequencies (V_{OUT} = 3.3V, I_{OUT} = 2A)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

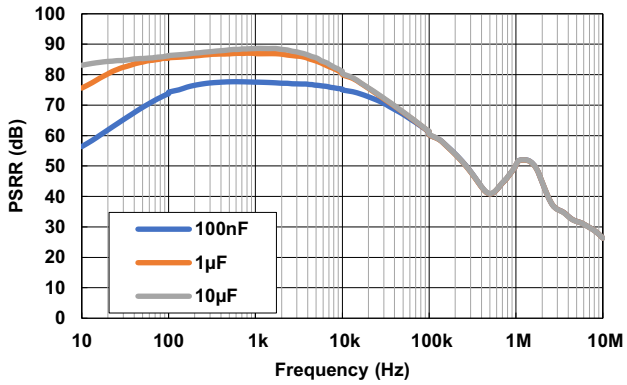


Figure 69. PSRR vs Frequency for Various C_{SET} (V_{IN} = 4V, V_{OUT} = 3.3V, I_{OUT} = 500mA)

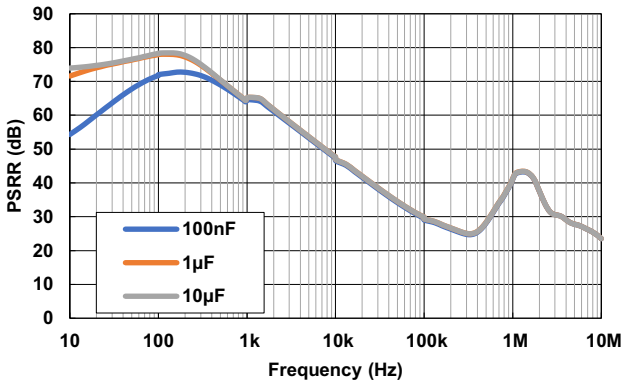


Figure 70. PSRR vs Frequency for Various C_{SET} (V_{IN} = 4V, V_{OUT} = 3.3V, I_{OUT} = 2A)

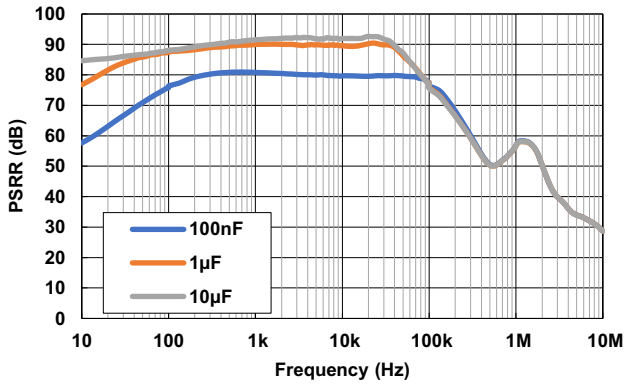


Figure 71. PSRR vs Frequency for Various C_{SET} (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 500mA)

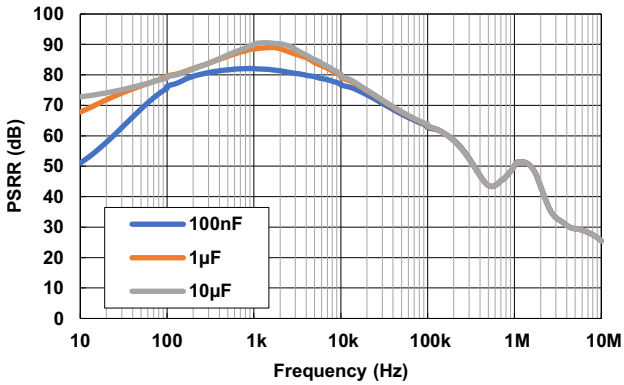


Figure 72. PSRR vs Frequency for Various C_{SET} (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A)

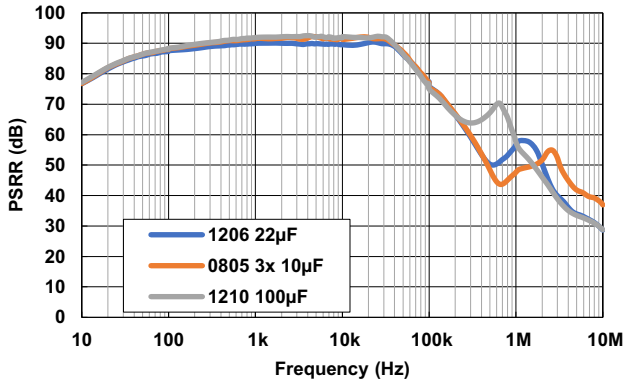


Figure 73. PSRR vs Frequency for Various C_{OUT} (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 500mA)

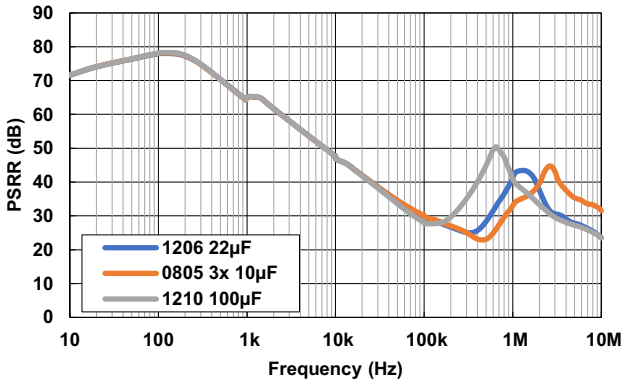


Figure 74. PSRR vs Frequency for Various C_{OUT} (V_{IN} = 4V, V_{OUT} = 3.3V, I_{OUT} = 2A)

4.3 Load Transient

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated.

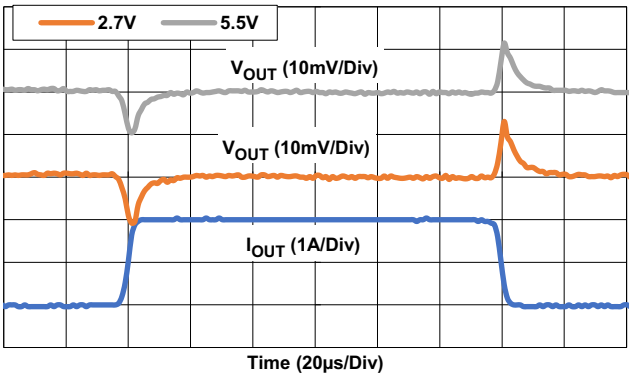


Figure 75. Load Transient Response for Various V_{IN} (V_{OUT} = 1.8V, ΔI_{OUT} = 100mA to 2A at 500mA/µs)

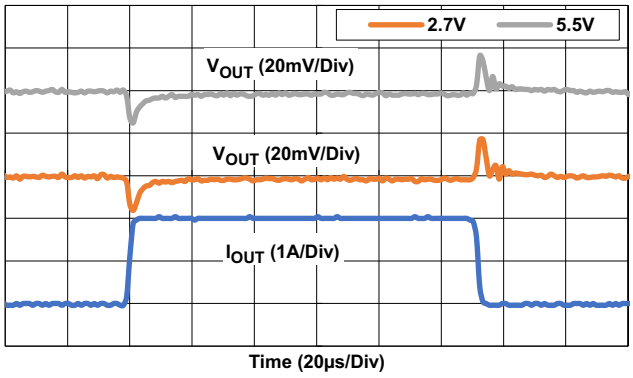


Figure 76. Load Transient Response for Various V_{IN} (V_{OUT} = 1.8V, ΔI_{OUT} = 100mA to 2A at 1A/µs)

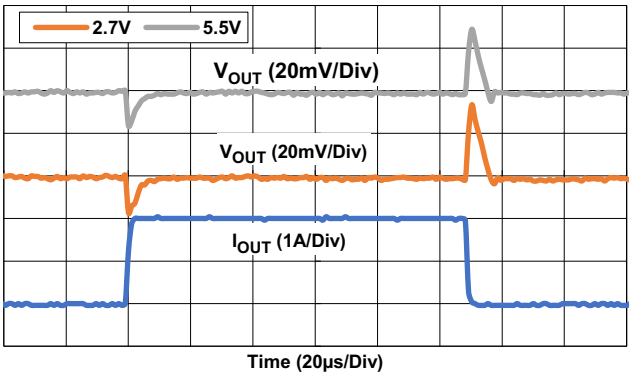


Figure 77. Load Transient Response for Various V_{IN} (V_{OUT} = 1.8V, ΔI_{OUT} = 100mA to 2A at 2A/µs)

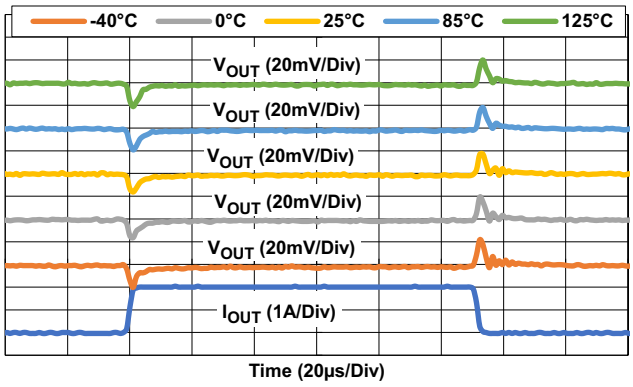


Figure 78. Load Transient Response for Various Temperatures (V_{IN} = 2.7V, V_{OUT} = 1.8V, ΔI_{OUT} = 100mA to 2A at 1A/µs)

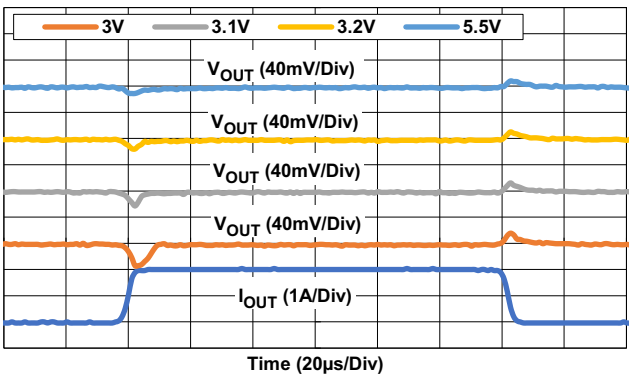


Figure 79. Load Transient Response for Various V_{IN} (V_{OUT} = 2.5V, ΔI_{OUT} = 100mA to 2A at 500mA/µs)

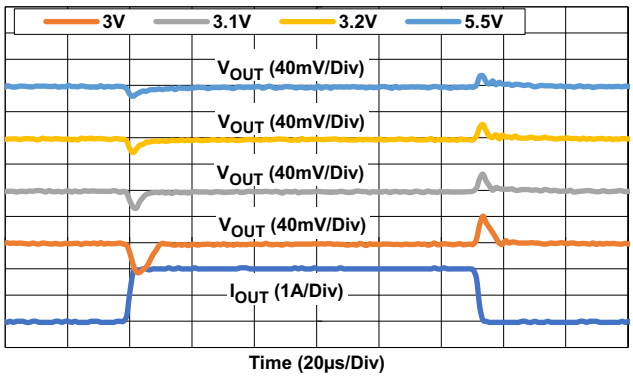


Figure 80. Load Transient Response for Various V_{IN} (V_{OUT} = 2.5V, ΔI_{OUT} = 100mA to 2A at 1A/µs)

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

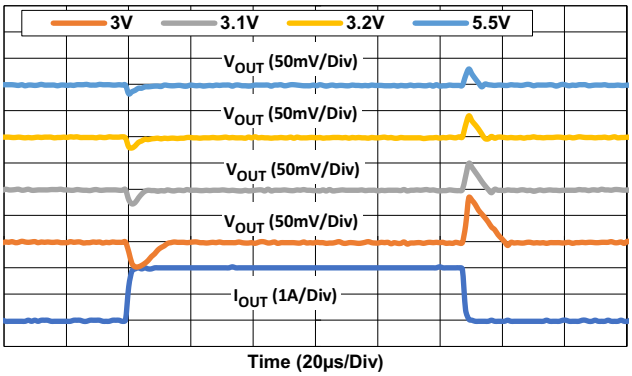


Figure 81. Load Transient Response for Various V_{IN} (V_{OUT} = 2.5V, ΔI_{OUT} = 100mA to 2A at 2A/µs)

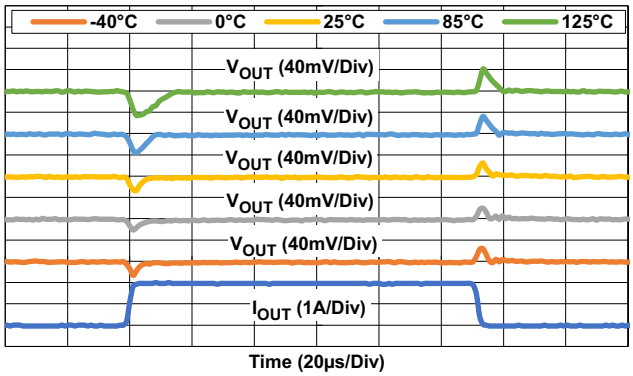


Figure 82. Load Transient Response for Various Temperatures (V_{IN} = 3.1V, V_{OUT} = 2.5V, ΔI_{OUT} = 100mA to 2A at 1A/µs

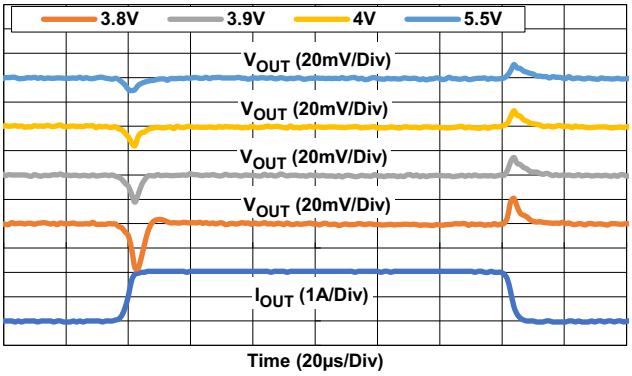


Figure 83. Load Transient Response for Various V_{IN} (V_{OUT} = 3.3V, ΔI_{OUT} = 100mA to 2A at 500mA/µs

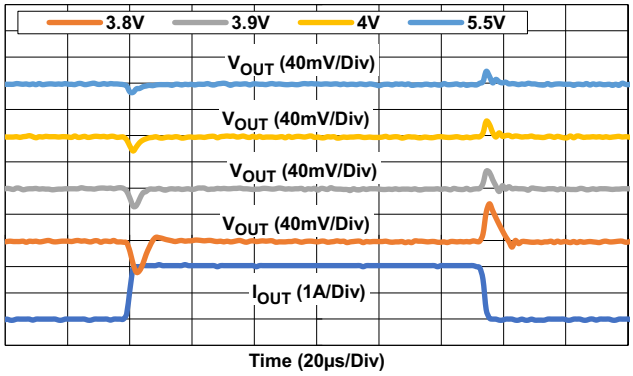


Figure 84. Load Transient Response for Various V_{IN} (V_{OUT} = 3.3V, ΔI_{OUT} = 100mA to 2A at 1A/µs

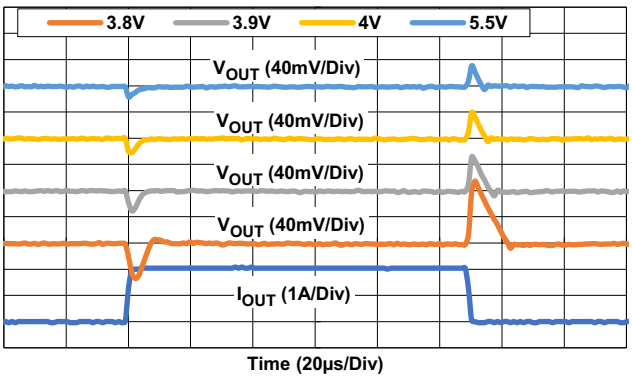


Figure 85. Load Transient Response for Various V_{IN} (V_{OUT} = 3.3V, ΔI_{OUT} = 100mA to 2A at 2A/µs

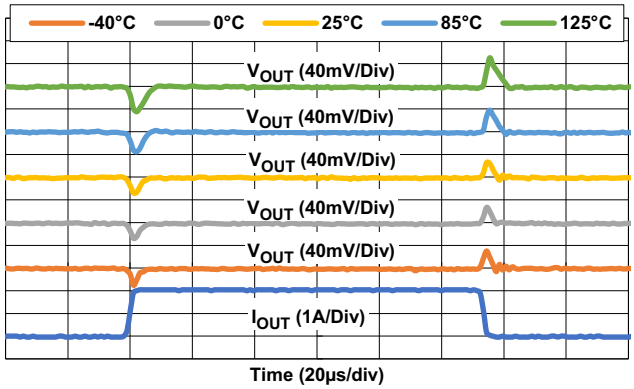


Figure 86. Load Transient Response for Various Temperatures (V_{IN} = 3.9V, V_{OUT} = 3.3V, ΔI_{OUT} = 100mA to 2A at 1A/µs

C_{SET} = 1µF, C_{OUT} = 22µF, unless otherwise stated. (Cont.)

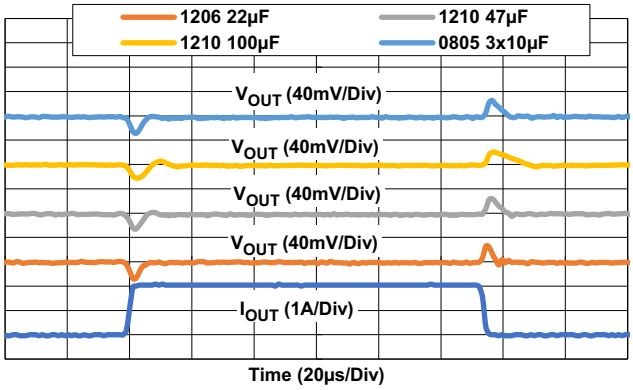


Figure 87. Load Transient Response for Various C_{OUT} (V_{IN} = 3.9V, V_{OUT} = 3.3V, ΔI_{OUT} = 100mA to 2A at 1A/µs

4.4 Dropout Voltage

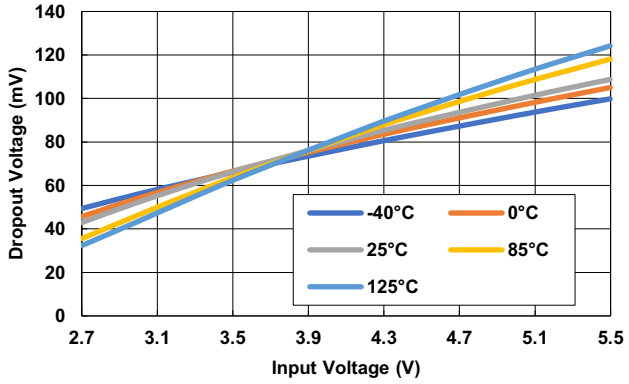


Figure 88. Dropout Voltage vs Output Current for Various Temperatures (I_{OUT} = 100mA)

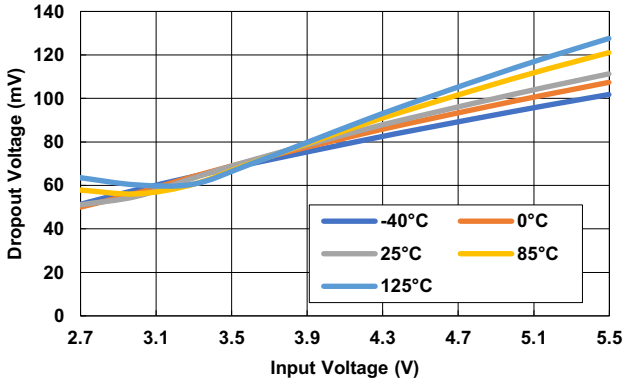


Figure 89. Dropout Voltage vs Output Current for Various Temperatures (I_{OUT} = 250mA)

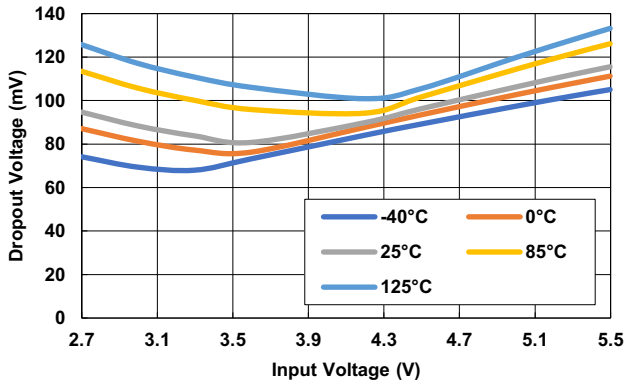


Figure 90. Dropout Voltage vs Output Current for Various Temperatures (I_{OUT} = 500mA)

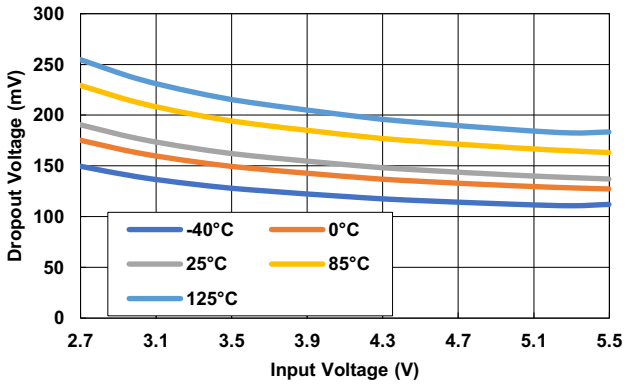


Figure 91. Dropout Voltage vs Output Current for Various Temperatures (I_{OUT} = 1A)

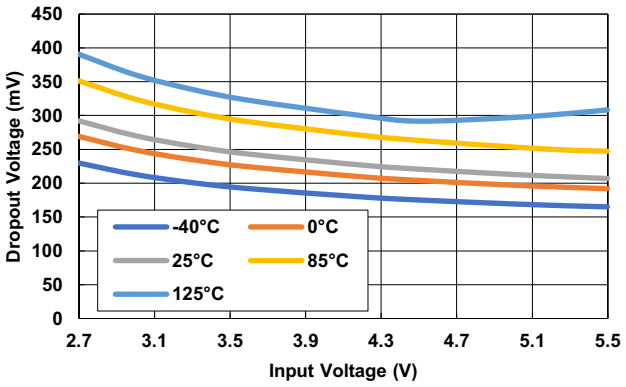


Figure 92. Dropout Voltage vs Output Current for Various Temperatures (I_{OUT} = 1.5A)

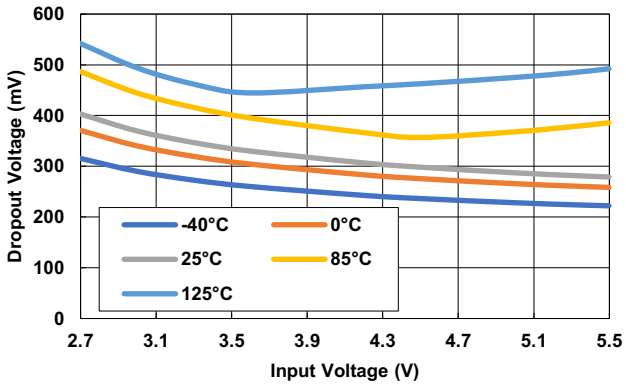


Figure 93. Dropout Voltage vs Output Current for Various Temperatures (I_{OUT} = 2A)

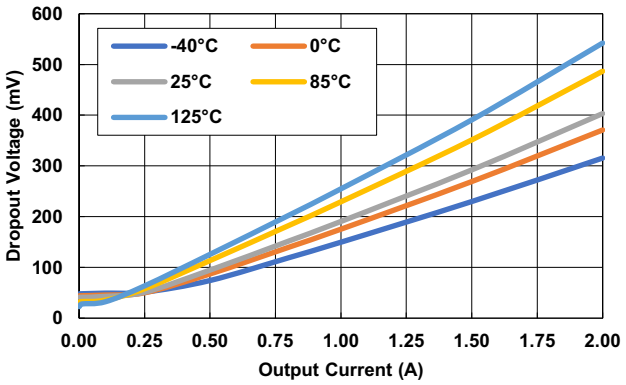


Figure 94. Dropout Voltage vs Output Current for Various Temperatures (V_{IN} = 2.7V)

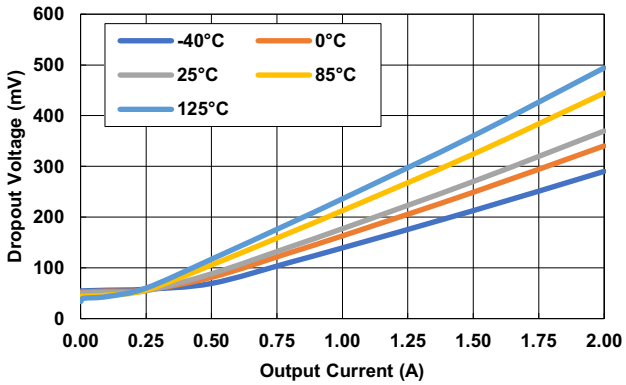


Figure 95. Dropout Voltage vs Output Current for Various Temperatures (V_{IN} = 3.3V)

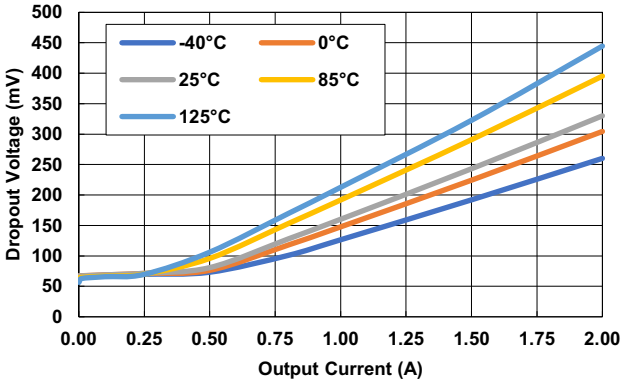


Figure 96. Dropout Voltage vs Output Current for Various Temperatures (V_{IN} = 3.6V)

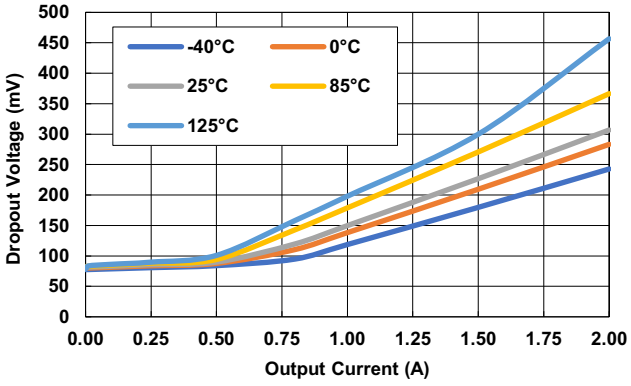


Figure 97. Dropout Voltage vs Output Current for Various Temperatures (V_{IN} = 4.2V)

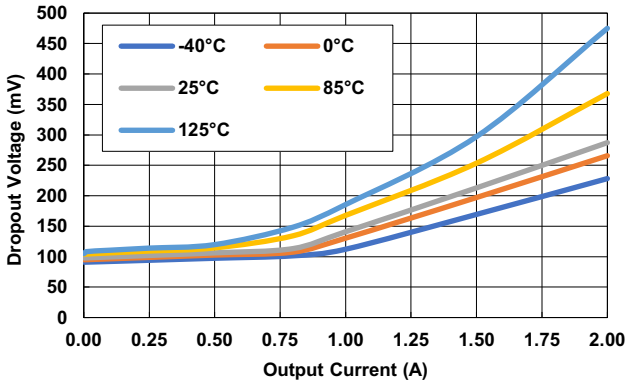


Figure 98. Dropout Voltage vs Output Current for Various Temperatures (V_{IN} = 5V)

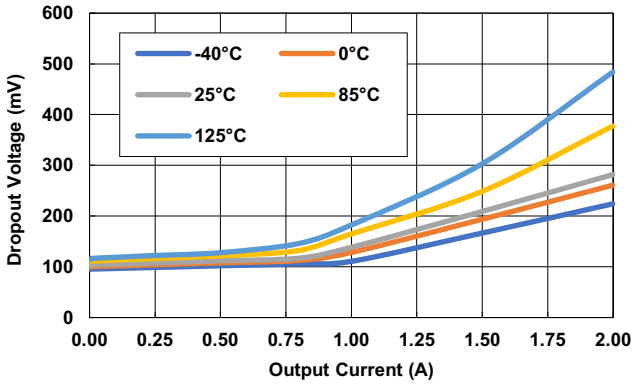


Figure 99. Dropout Voltage vs Output Current for Various Temperatures (V_{IN} = 5.3V)

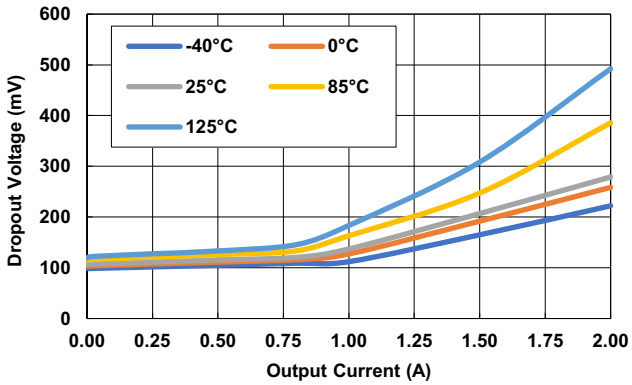


Figure 100. Dropout Voltage vs Output Current for Various Temperatures (V_{IN} = 5.5V)

4.5 General Performance

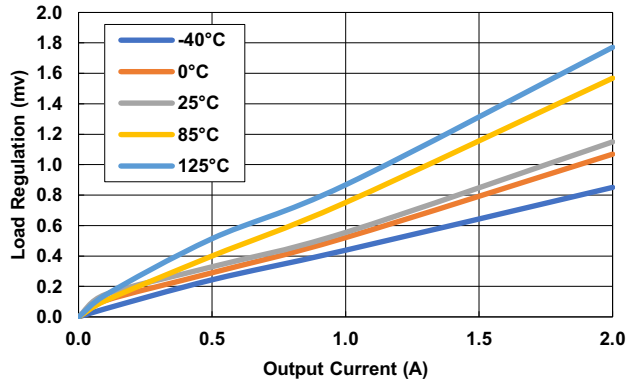


Figure 101. Load Regulation vs Output Current (V_{IN} = 2.7V, V_{OUT} = 0.9V, ΔI_{OUT} = 1mA to 2A)

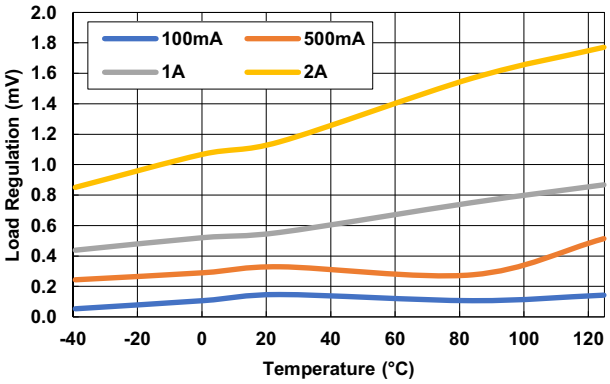


Figure 102. Load Regulation vs Temperature (V_{IN} = 2.7V, V_{OUT} = 0.8V, ΔI_{OUT} = 1mA to 2A)

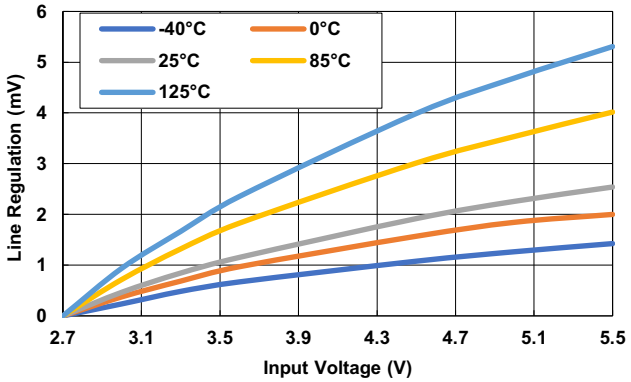


Figure 103. Line Regulation vs Input Voltage for Various Temperatures (V_{OUT} = 0.9V, I_{OUT} = 1mA, ΔV_{IN} = 2.7V to 5.5V)

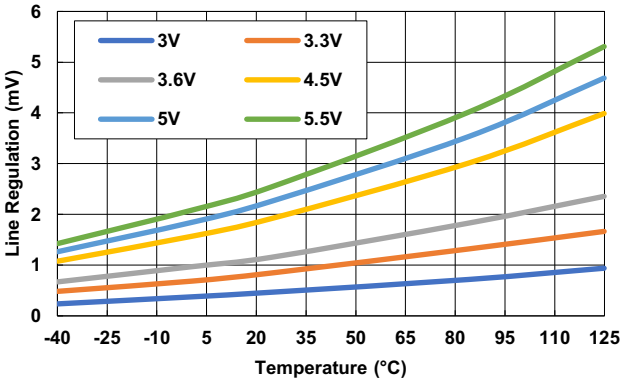


Figure 104. Line Regulation vs Temperature for Various V_{IN} (V_{OUT} = 0.9V, I_{OUT} = 1mA, ΔV_{IN} = 2.7V to 5.5V)

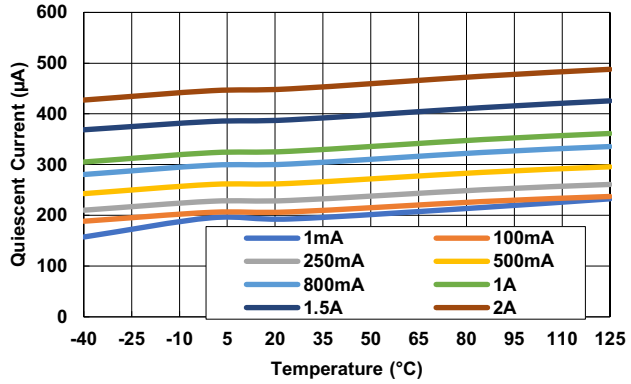


Figure 105. Quiescent Current vs Temperature for Various I_{OUT} (V_{IN} = 2.7V, V_{OUT} = 0.9V)

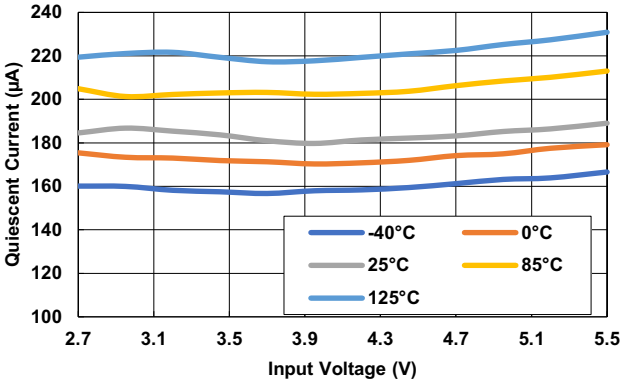


Figure 106. Quiescent Current vs Input Voltage for Various Temperatures (V_{OUT} = 0.9V, I_{OUT} = 0mA)

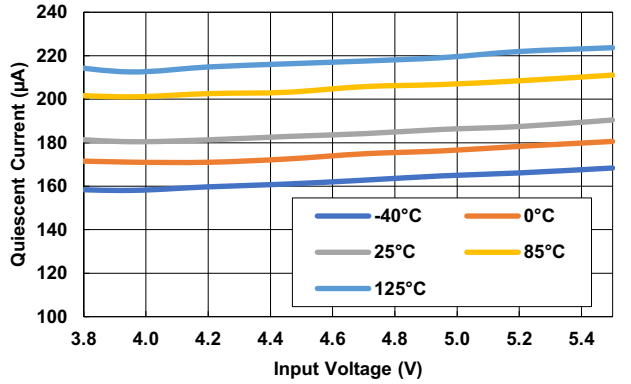


Figure 107. Quiescent Current vs Input Voltage for Various Temperatures (V_{OUT} = 3.3V, I_{OUT} = 0mA)

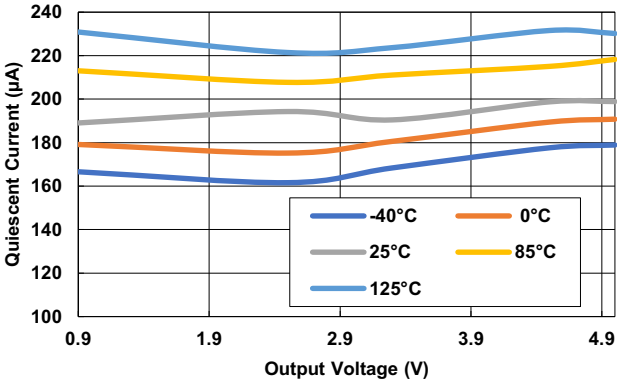


Figure 108. Quiescent Current vs Output Voltage for Various Temperatures (V_{IN}= 5.5V, I_{OUT} = 0mA)

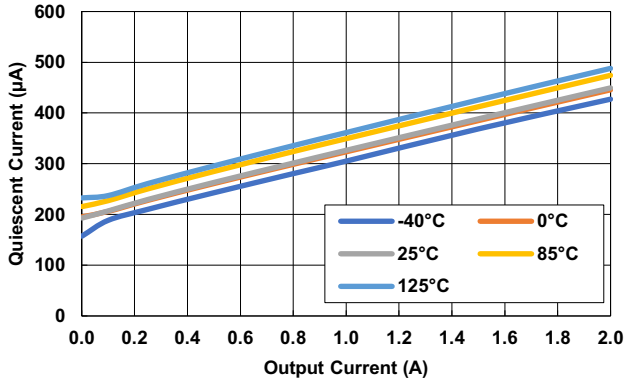


Figure 109. Quiescent Current vs Output Current for Various Temperatures (V_{IN} = 5.5V, I_{OUT} = 0mA)

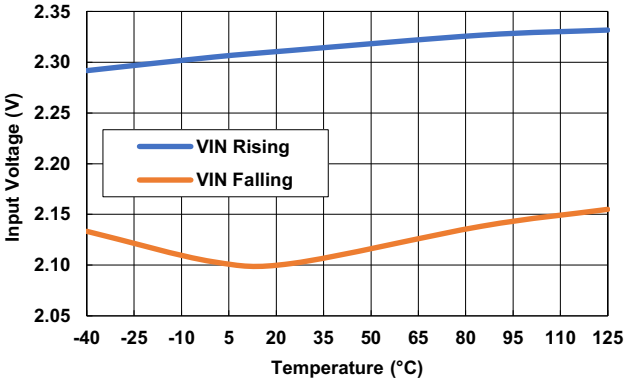


Figure 110. Input Voltage UVLO Thresholds vs Temperature

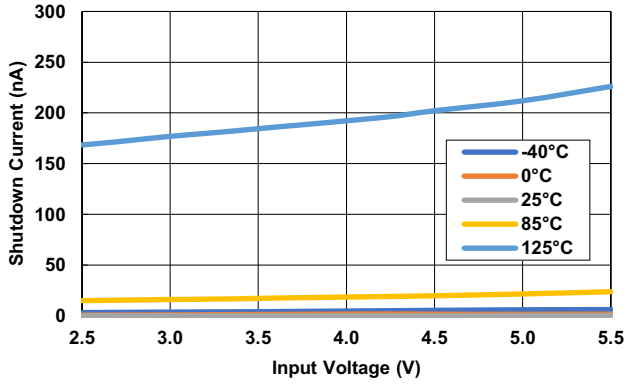


Figure 111. Shutdown Current vs Input Voltage for Various Temps. (V_{EN} = 0V)

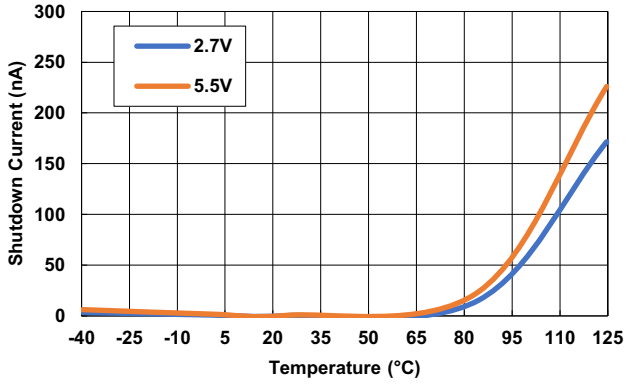


Figure 112. Shutdown Current vs Temp. for Various Input Voltages (V_{EN} = 0V)

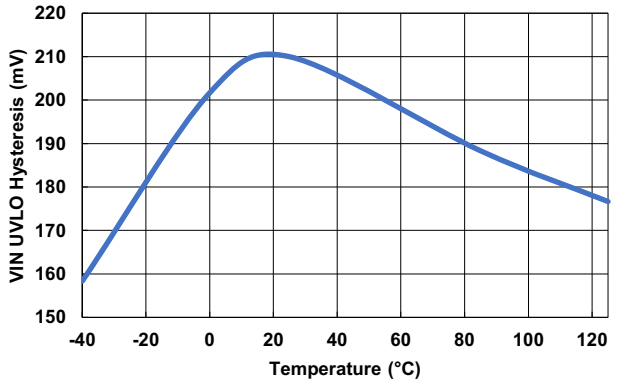


Figure 113. Input Voltage UVLO Hysteresis vs Temperature

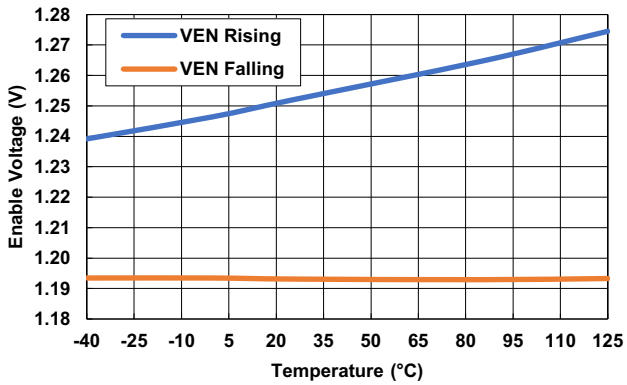


Figure 114. Enable Voltage Thresholds vs Temperature (V_{IN} = 2.7V)

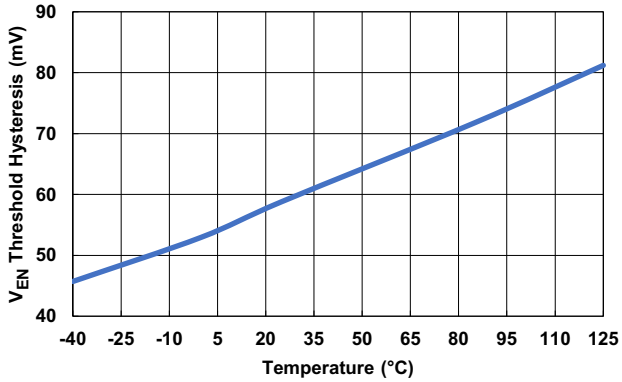


Figure 115. Enable Voltage Hysteresis vs Temperature (V_{IN} = 2.7V)

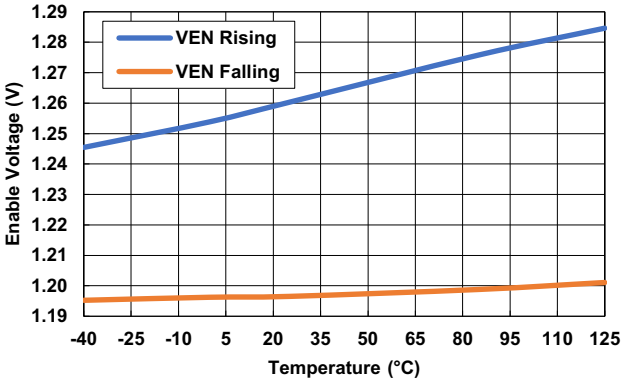


Figure 116. Enable Voltage Thresholds vs Temperature (V_{IN} = 5.5V)

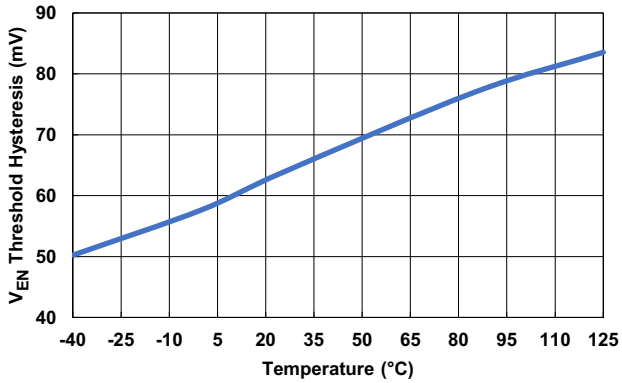


Figure 117. Enable Voltage Hysteresis vs Temperature (V_{IN} = 5.5V)

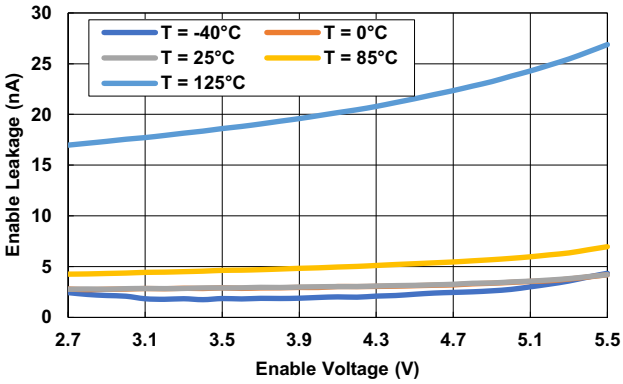


Figure 118. EN Leakage vs Enable Voltage Across Various Temperatures

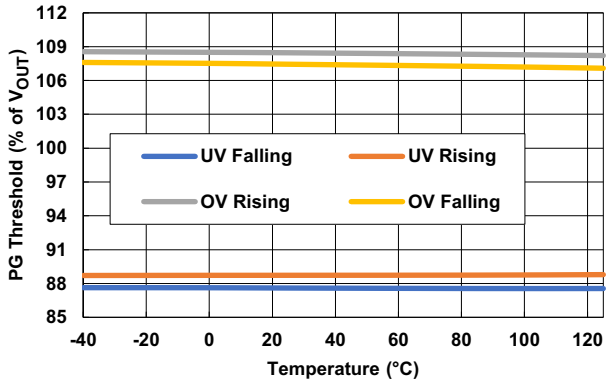


Figure 119. PG Thresholds vs Temperature (V_{IN} = 2.7V)

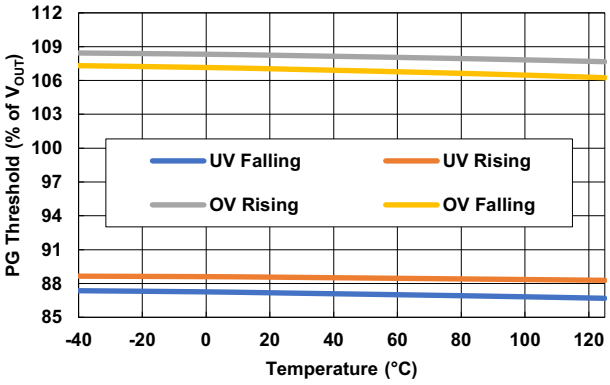


Figure 120. PG Thresholds vs Temperature (V_{IN} = 5.5V)

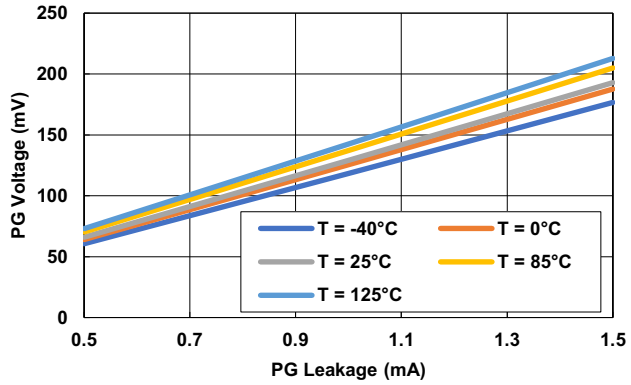


Figure 121. PG Voltage vs PG Sinking Current

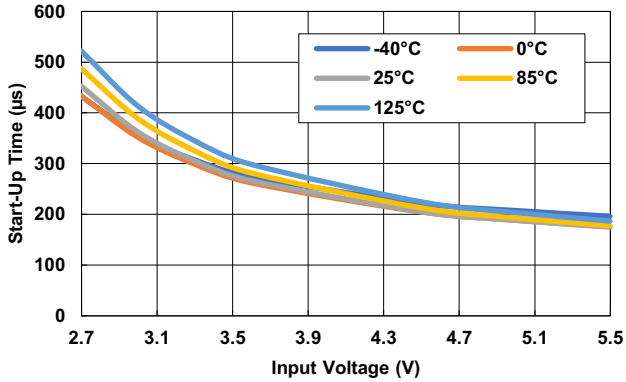


Figure 122. Start-Up Time vs Input Voltage (V_{OUT} = 1.8V, C_{SET} = 1µF, C_{OUT} = 22µF)

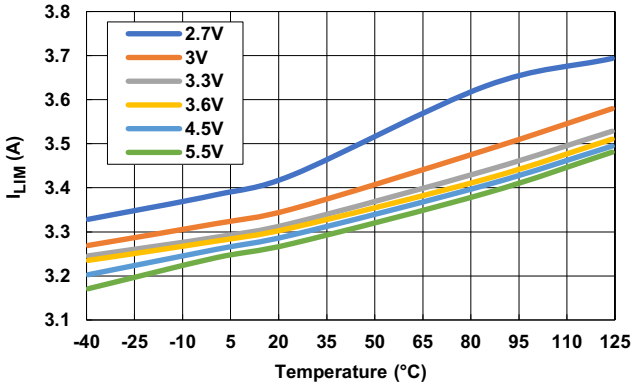


Figure 123. I_{LIM} vs Temperature for Various Input Voltages (V_{OUT} = 1.8V)

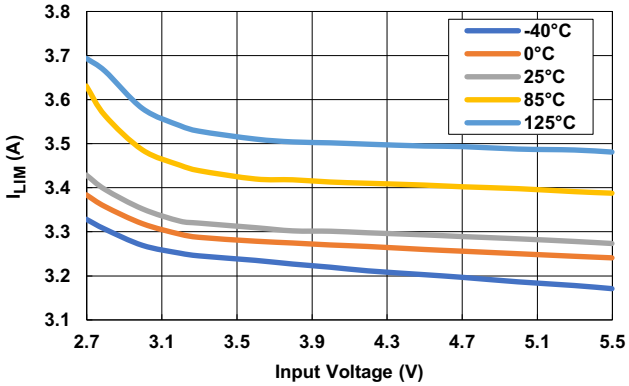


Figure 124. I_{LIM} vs Input Voltage for Various Temperatures (V_{OUT} = 1.8V)

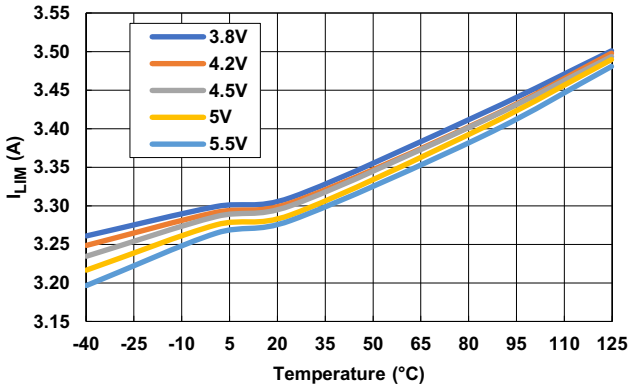


Figure 125. I_{LIM} vs Temperature for Various Input Voltages (V_{OUT} = 3.3V)

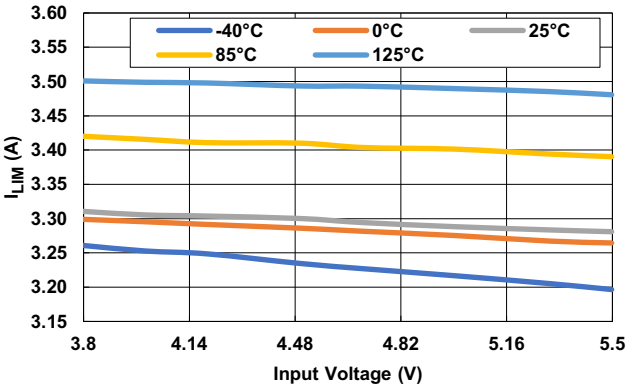


Figure 126. I_{LIM} vs Input Voltage for Various Temperatures (V_{OUT} = 3.3V)

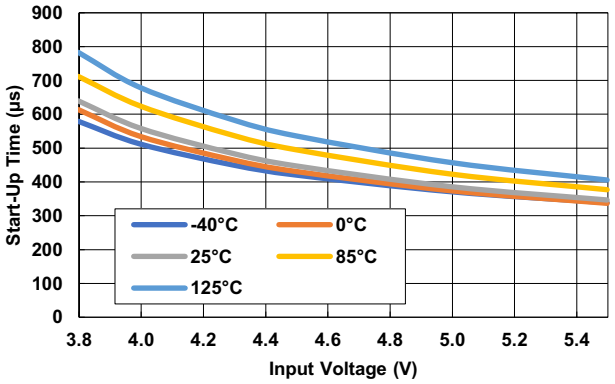


Figure 127. Start-Up Time vs Input Voltage (V_{OUT} = 3.3V, C_{SET} = 1µF, C_{OUT} = 22µF)

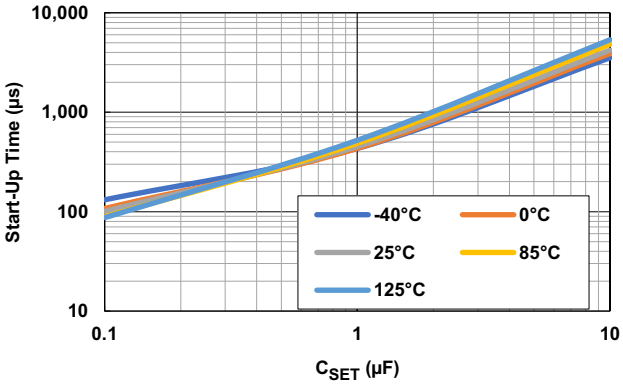


Figure 128. Start-Up Time vs C_{SET} for Various Temperatures (V_{IN} = 2.7V, V_{OUT} = 1.8V, C_{SET} = 1µF, C_{OUT} = 22µF)

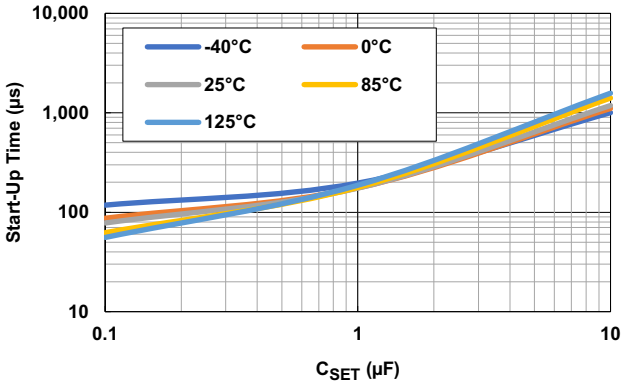


Figure 129. Start-Up Time vs C_{SET} for Various Temperatures (V_{IN} = 5.5V, V_{OUT} = 1.8V, C_{SET} = 1µF, C_{OUT} = 22µF)

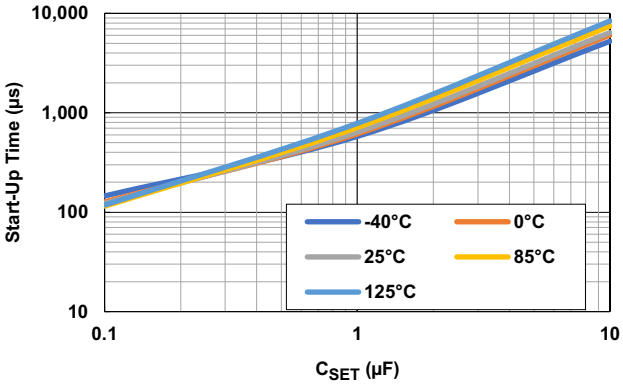


Figure 130. Start-Up Time vs C_{SET} for Various Temperatures (V_{IN} = 3.8V, V_{OUT} = 3.3V, C_{SET} = 1µF, C_{OUT} = 22µF)

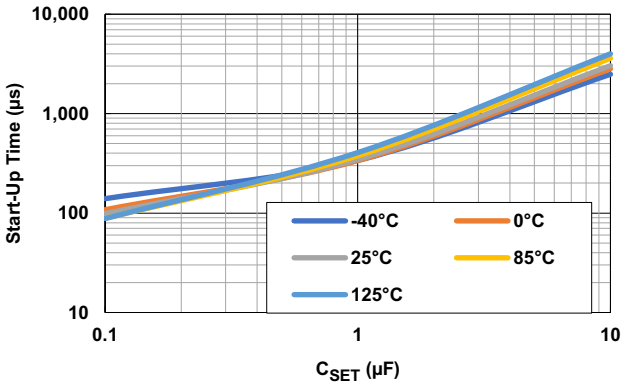


Figure 131. Start-Up Time vs C_{SET} for Various Temperatures (V_{IN} = 5.5V, V_{OUT} = 3.3V, C_{SET} = 1µF, C_{OUT} = 22µF)

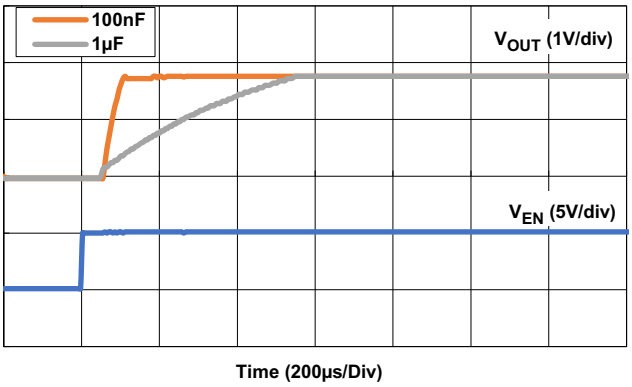


Figure 132. Start-Up Time for Various C_{SET} Capacitors (V_{IN} = 2.7V, V_{OUT} = 1.8V, I_{OUT} = 2A, C_{OUT} = 22µF)

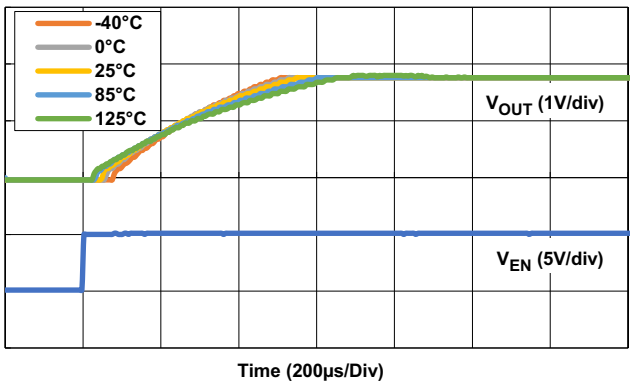


Figure 133. Start-Up Time for Various Temperatures (V_{IN} = 2.7V, V_{OUT} = 1.8V, I_{OUT} = 2A, C_{SET} = 1µF, C_{OUT} = 22µF)

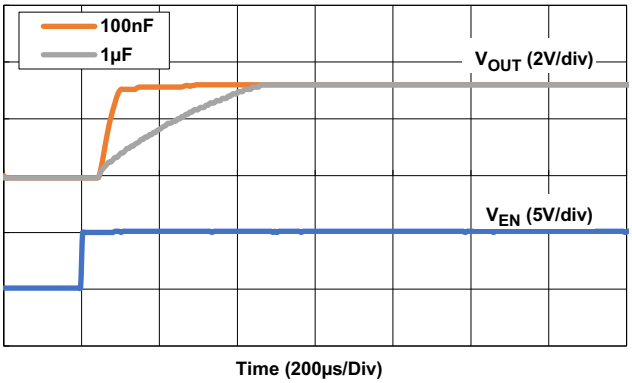


Figure 134. Start-Up Time for Various C_{SET} Capacitors (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A, C_{OUT} = 22µF)

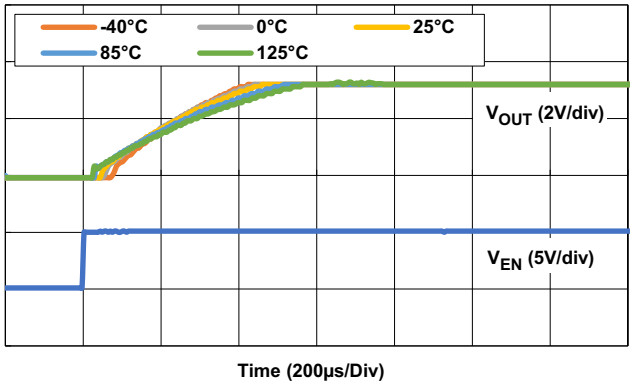


Figure 135. Start-Up Time for Various Temperatures (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A, C_{SET} = 1µF, C_{OUT} = 22µF)

5. Applications Information

5.1 Overview

The RAA214020 is an ultra-low noise, high PSRR, low-dropout (LDO) voltage regulator that is ideal for low noise applications. The LDO operates from an input voltage of 2.7V to 5.5V while sourcing a maximum 2A load with ±1.5% accuracy over line, load, and temperature. The output voltage can be adjusted with external feedback divider resistors from 0.9V up to 5.5V-V_{DO}. The LDO draws 195µA quiescent current typical at no-load and has 200nA of shutdown current typical at 125°C making it ideal for portable applications.

The RAA214020 is designed and tested with a 22µF minimum output capacitor, 10µF input capacitor, and a 1µF noise reduction filter (C_{SET}) capacitor. The LDO is available in a 3x3mm 10 Ld DFN package and operates with a junction temperature (T_J) of -40°C to 125°C.

The RAA214020 integrates the following additional features in this small package:

- Ultra-low output noise
- High Power Supply Ripple Rejection (PSRR)
- Undervoltage Lockout (UVLO)
- Enable control
- Internal current limit protection
- Thermal shutdown protection
- Power-Good (PG) indication
- Output capacitor automatic discharge

5.2 Theory of Operation of PMOS LDOs

Like the majority of LDOs with a PMOS pass transistor, the RAA214020 DC output voltage (V_{OUT}) regulation can be a modeled with a voltage reference (V_{REF}), PMOS pass-transistor, error amplifier and feedback (FB) resistors as shown in Figure 136.

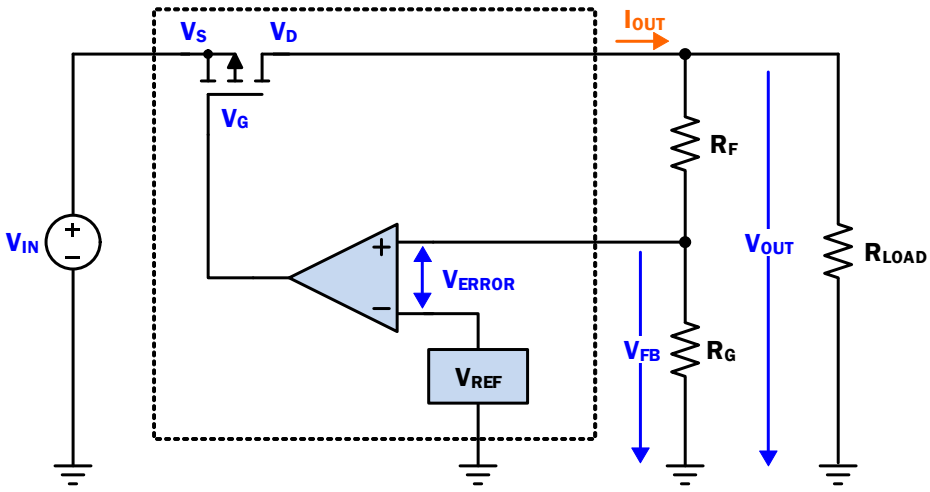


Figure 136. Simple PMOS LDO Regulator Block Diagram

The PMOS pass transistor can be modeled as a variable resistor ($r_{DS(ON)}$) that is controlled by the error amplifier to maintain a constant DC output voltage for changes in load current (I_{OUT}). Assuming the input voltage (V_{IN})

remains constant, the $r_{DS(ON)}$ is adjusted for a given I_{OUT} to set V_{OUT}. This relationship is summarized in Equation 1.

(EQ. 1) $$V_{OUT} = V_{IN} - I_{OUT} \times R_{DS(ON)}$$

V_{OUT} is set using the FB resistor divider, which sets V_{OUT} to a value that corresponds to Equation 2.

(EQ. 2) $$V_{OUT} = V_{FB} \times \left(\frac{RF}{RG} + 1\right)$$

The error amplifier compares V_{FB} with the fixed V_{REF} voltage and works to minimize the difference or error voltage between V_{FB} and V_{REF} by changing the gate voltage of the PMOS pass transistor and therefore the $r_{DS(ON)}$.

If the I_{OUT} suddenly increases because of decreased load resistance, V_{OUT} decreases because the regulator has not responded to the change and the $r_{DS(ON)}$ is set too high. V_{FB} correspondingly decreases and is below the V_{REF} voltage therefore, increasing the error voltage. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more negative relative to the FET source to decrease the $r_{DS(ON)}$, which increases the output voltage bringing it back into regulation.

By similar logic, a sudden decrease in I_{OUT} because of increased load resistance causes V_{OUT} to increase because the $r_{DS(ON)}$ is set too low. V_{FB} is then higher than the fixed V_{REF} voltage increasing the error. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more positive relative to the FET source to increase the $r_{DS(ON)}$, which decreases the output voltage bringing it back into regulation.

For a more detailed explanation of the DC regulation operation of a PMOS LDO regulator, see *R16AN0008: Fundamental Theory of PMOS Low-Dropout Voltage Regulators*.

5.3 Functional Description

5.3.1 AC Performance

5.3.1.1 Ultra-Low Output Noise

The LDO output noise is the internally-generated noise created largely by the band-gap voltage reference (V_{REF}) and the error amplifier. It is commonly represented in units of nV/√Hz for a specific frequency or as an integrated root-mean square (RMS) value in µV over a range of frequencies typically 10Hz to 100kHz or 100Hz to 100kHZ.

The RAA214020 output noise is largely independent of V_{OUT} and does not require a feed-forward capacitor to achieve low output noise. For optimal low-noise, Renesas recommends using a 1µF C_{SET} capacitor. See C_{SET} Capacitor for selecting the correct C_{SET} capacitor.

5.3.1.2 High Power Supply Ripple Rejection (PSRR)

The PSRR is how much attenuation or rejection the LDO control loop offers to externally generated VIN noise, such as from a switching regulator. Although PSRR represents a loss in the input noise signal, it is common to see it represented as a positive decibel (dB) number. Mathematically, PSRR is represented as a logarithmic ratio between an input and output ripple sinusoid signal at a specific frequency as shown in Equation 3.

(EQ. 3) $$PSRR = 20 \times \log\left(\frac{V_{IN(RIPPLE)}(f)}{V_{OUT(RIPPLE)}(f)}\right)$$

The PSRR for the RAA214020 is largely independent of the output voltage. It is dependent on the headroom voltage, output current, and C_{SET} capacitor. For optimal PSRR performance, a1µF C_{SET} capacitor is recommended. See C_{SET} Capacitor for selecting the correct C_{SET} capacitor.

Table 1 lists the PSRR for different headroom voltages rails for 2A, 1A, 500mA, and 100mA loads at 120Hz, 1kHz, 10kHz, and 1MHz.

Table 1. Typical PSRR in dB for C_{SET} = 1µF and C_{OUT} = 22µF

$V_{HEADROOM}$	I_{OUT}	120Hz	1kHz	10kHz	100kHz	500kHz	1MHz	10MHz
800mV	100mA	88	88	89	69	56	58	33
800mV	500mA	86	88	85	63	52	51	26
800mV	1A	84	87	73	56	39	48	25
800mV	2A	79	70	52	35	30	43	24
1.7V	100mA	90	90	90	85	57	64	36
1.7V	500mA	87	89	90	77	47	55	33
1.7V	1A	84	89	87	70.	47	54	27
1.7V	2A	80	88	79	64	43	50	25

5.3.1.3 Load Transient Response

The load-step transient response is the output voltage response of the LDO because of a step change in load current. The magnitude of the undershoot is directly proportional to the amount of output capacitance and the slew rate of the load current step.

If the undershoot takes V_{OUT} below -10% of its programmed value, the PG circuitry responds by connecting C_{SET} to the fast start-up circuitry to rapidly bring V_{OUT} back to within ±10% of its programmed value.

During sudden decreases in I_{OUT}, the V_{OUT} increases and overshoots. The LDO responds to the overshoot by turning off the main pass-transistor and waits for C_{OUT} to discharge. If the V_{OUT} overshoot takes V_{OUT} above +10 of its programmed value, the PG circuitry responds by connecting a 1kΩ pull-down resistor to quickly discharge the C_{OUT} and brings V_{OUT} back to within ±10% of its programmed value. The 1kΩ remains connected if V_{OUT} is above +10% of its programmed value.

A larger output capacitance value can marginally decrease the overshoot and undershoot magnitude. However, doing so can increase the response time of the LDO to undershoots and overshoots, in addition to increasing the output noise. See Output Capacitor for selecting the correct output capacitor.

5.3.2 UVLO

The RAA214020 integrates an internal UVLO circuit to keep the output voltage safely disabled if the input voltage is below the UVLO threshold (2.5V typical). When the input voltage is above the UVLO threshold, the part is enabled and the output voltage ramps up. The UVLO hysteresis prevents input voltage noise from causing the output to oscillate.

When V_{IN} is below the UVLO, an internal 300Ω discharge resistor connects the LDO output to ground to quickly discharge the output capacitor. The resistor is connected to the output capacitor if the input voltage is greater than 1V but less than the UVLO threshold of 2.5V typical. Figure 137 illustrates the UVLO operation.

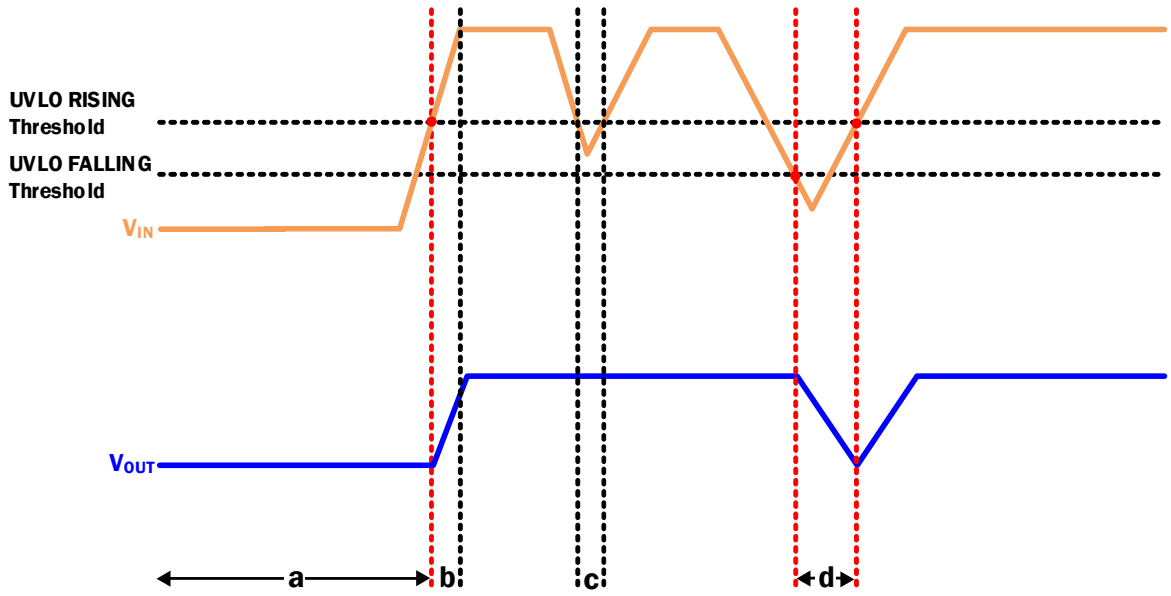


Figure 137. UVLO Operation

Starting with V_{IN}= 0V and V_{OUT} = 0V:

- **a, d** The LDO is disabled and the internal 300Ω discharge resistor is connected to the output voltage as long as the input voltage is between 1V to 2.5V.
- **b** The LDO is enabled and starts to rise. The 300Ω discharge resistor is disconnected from output voltage.
- **c** The LDO remains enabled and the 300Ω discharge resistor remains disconnected.

5.3.3 Enable Control

The RAA214020 uses the EN pin voltage (V_{EN}) to enable or disable the LDO. If V_{EN} is less than the V_{EN} threshold, the LDO is disabled. If V_{EN} is greater than the V_{EN} threshold, the LDO is enabled. The V_{EN} hysteresis prevents enable voltage noise from causing the output to oscillate. When the LDO is disabled, the shutdown current is typically a couple of nanoamps.

When V_{EN} is below the V_{EN} threshold and the input voltage is greater than or equal to 1V, the same 300Ω discharge resistor controlled by the UVLO circuitry is connected between the LDO output and GND to quickly discharge the output capacitor.

The EN pin can be directly connected to the input voltage for automatic start-up or connected to a logic controller such as an MCU of FPGA. Some logic pins use an open-collector or open-drain transistor to pull LOW and float when HIGH. Make sure to connect a 1kΩ or 10kΩ pull-up resistor to ensure proper logic HIGH. To ensure proper Enable control operation, the V_{EN} signal source should be capable of swinging above and below the threshold values.

5.3.4 Integrated Protection Features

5.3.4.1 Internal Current Limit (ILIM)

The Internal current limit (ILIM) circuitry limits the maximum output current the LDO can source during fault conditions such as short-circuits or start-up inrush current. ILIM is set above the normal output current rating of the RAA214020 (2A).

During a short-circuit fault, the LDO becomes a constant current source and as a result any decrease in load resistance causes a decrease in the output voltage. This relationship is summarized in Equation 4.

(EQ. 4) $V_{OUT} = IILIM \times R_{FAULT}$

When the short or overcurrent condition is removed, the LDO returns to regulation. Because of the high power dissipation caused by overcurrent faults, the LDO may begin to cycle ON and OFF because the die junction temperature (T_J) is exceeding thermal fault conditions (+155°C) and subsequently cooling down to +145°C when the LDO is disabled.

5.3.4.2 Thermal Protection

The RAA214020 is protected against thermal overloads caused by current limit protection or high ambient temperature (T_A).

When the die junction temperature (T_J) exceeds +155°C, the thermal shutdown circuit disables the LDO reducing the output current (I_{OUT}) to 0A and therefore reducing the output voltage (V_{OUT}) to 0V allowing the LDO to cool. A 10°C hysteresis is included to prevent the LDO from uncontrollably heating and cooling.

Prolonged exposure to a T_J exceeding +125°C reduces the long-term stability and life of the LDO. Therefore, it is important that the design considers the T_A the LDO works in, the thermal resistance between T_J and T_A (θ_{JA}), and any fault conditions that can cause the T_J to exceed the recommended operating range. In some applications, a heat sink may need to be implemented. See Power Dissipation and Thermals to determine the maximum junction temperature for an application.

5.3.5 Power-Good (PG) Indication

The Power-Good (PG) pin is an open-drain NMOS-FET. The PG pin circuitry works by monitoring the FB voltage to indicate whether the output voltage is within ±10% of 0.9V. When the output voltage is ±10% outside of its programmed value, the PG circuitry drives the NMOS FET ON and indicates LOW on the PG pin. When the output voltage is within ±10% of its programmed value, the PG circuitry drives the NMOS-FET OFF and the PG pin becomes HIGH.

When the output voltage is below the PG Undervoltage (UV) thresholds, the fast-start up circuitry is activated to bring V_{OUT} within the ±10% window. When the output voltage is above the PG Overvoltage (OV) thresholds, a 1kΩ pull-down resistor connects V_{OUT} to GND to discharge the output capacitor and bring the output voltage back within the ±10% window. Figure 138 illustrates the PG operation.

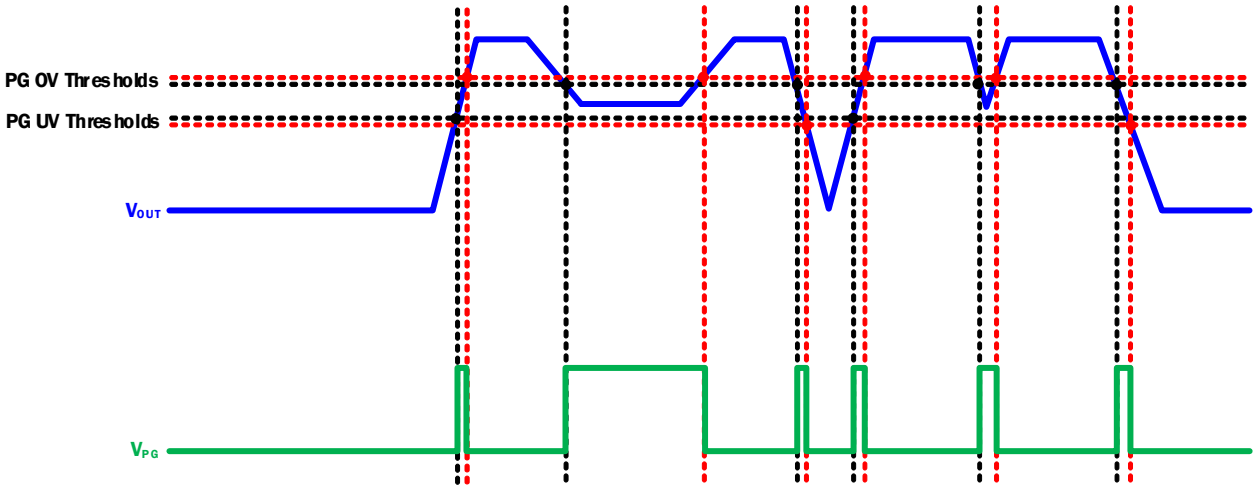


Figure 138. PG Operation

A 10kΩ or 100kΩ pull-up resistor is recommended to tie PG pin to V_{IN}, V_{OUT}, or an external supply to ensure a proper HIGH voltage to any downstream logic device such as an MCU or FPGA. If the PG pin is not being used, it can be left floating.

5.3.6 DC Performance

5.3.6.1 Dropout Voltage

The dropout voltage (V_{DO}) is defined as the voltage drop across the primary, current-carrying pass-transistor in the ohmic region of operation at a rated load current, input voltage, and junction temperature. The LDO performance is negatively affected in the dropout region. For proper DC regulation, the LDO input voltage must be some margin higher than the output voltage.

5.3.6.2 Output Current

The RAA214020 remains stable and in regulation with no external load.

5.3.7 Output Capacitor Automatic Discharge

The RAA214020 features a 300Ω and 1kΩ discharge resistor to rapidly discharge the output capacitor. The 300Ω discharge resistor is controlled by the ENABLE circuitry and UVLO circuitry, and the 1kΩ discharge resistor is controlled by the PG circuitry.

The 300Ω discharge resistor is connected to the LDO output when either the enable voltage is below the V_{EN} threshold, or the input voltage is below the UVLO threshold but greater than or equal to 1V. If the input voltage collapses faster than the discharge circuitry can discharge the output capacitor, the output voltage may be greater than the input voltage. In this case, C_{OUT} discharges through the PMOS transistor body diode.

The 1kΩ discharge resistor is connected to the LDO output when V_{OUT} overshoots above 10% final value. Without it, the regulator would have to wait a long time for C_{OUT} to discharge during rapid, large load steps from full-load to little or no-load.

5.4 Voltage Requirements

5.4.1 Input Voltage

The RAA214020 operates with an input voltage of 2.7V to 5.5V on the VIN pin. The input supply must be able to supply enough current to keep the input voltage from drooping during load steps or high load currents.

For proper voltage regulation the input voltage must be chosen so that it is higher than the sum of the output voltage and the maximum dropout voltage expected for a given application as expressed in Equation 5.

(EQ. 5) $$V_{IN} > V_{OUT} + V_{DROPOUT(MAX)}$$

The difference between V_{IN} and V_{OUT} required for proper regulation is commonly called the headroom voltage ($V_{HEADROOM}$).

5.4.2 Adjusting the Output Voltage Using External Feedback Resistors

The RAA214020 output voltage (V_{OUT}) can be programmed down to 0.9V and up to 5.5V-V_{DO} using the feedback (FB) resistors, R_F and R_G, as shown in Figure 139.

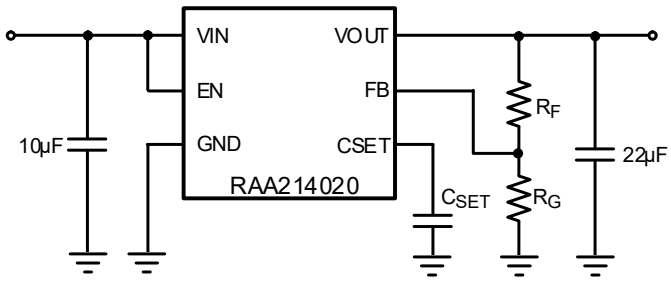


Figure 139. RAA214020 Simplified Application Schematic

V_{OUT} is calculated using Equation 6.

(EQ. 6) $$V_{OUT} = 0.9V \times \left(1 + \frac{R_F}{R_G}\right)$$

Similarly, the R_F and R_G resistors are calculated for any target output voltage by rearranging Equation 6 to get Equation 7 and solving for R_F.

(EQ. 7) $$R_F = R_G \times \left(\frac{V_{OUT(TARGET)}}{0.9V} - 1\right)$$

Table 2 suggests the FB resistor values to get some common voltage rails with 0.1% error. These resistors are commercially available in 0.1% tolerances. This table is not exhaustive and there may be other R_F and R_G resistor combinations that can provide better accuracy.

Table 2. Recommended R_F and R_G Feedback Resistor Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	V_{OUT} Error (%)
1	1.13	10.2	-0.03
1.2	3.4	10.2	0.0
1.5	6.8	10.2	0.0
1.8	10	10	0.0
1.9	1.11	10	-0.05
2.5	17.8	10	0.08
3	28.0	12.0	0.0
3.3	26.7	10.0	0.0
4.2	37.4	10.2	0.0
4.5	56.0	14.0	0.0
5	48.7	10.7	0.08

5.5 External Bypass Capacitor Selection

The RAA214020 is stable with C_{IN}, C_{OUT}, and C_{SET} bypass capacitors. Multilayer ceramic capacitors (MLCC) are an excellent choice for bypass capacitors because of their small size, low ESR, low ESL, and wide operating temperature. They are not without their problems though. Ceramic capacitor values can vary with the DC bias voltage, temperature, and tolerance. Therefore, Renesas recommends that the capacitors are de-rated.

X5R, X7R, and C0G capacitors are recommended. Low cost Y5V and Z5U capacitors are acceptable if they are properly derated. To ensure the performance of the RAA214020, it is important that the effects of DC bias voltage, temperature, and tolerances for a chosen capacitor are evaluated.

Place the bypass capacitors as close as is practical to their respective pins to minimize trace inductance.

5.5.1 Input Capacitor

The minimum input capacitor required on the VIN pin for proper operation and stability is 10µF. A 10µF input capacitor also helps reduce the negative effects of large input impedances because of long input traces or high source-impedances. Additional bypass capacitors with different self-resonant frequencies can be paralleled with 10µF to keep the input impedance low across a wider frequency range, if required. However, care should be taken to avoid introducing anti-resonance in the circuit.

When output capacitor values larger than 22µF are used, increase the input capacitor to match it. Input capacitors greater than 10µF can also help minimize input voltage droops during large changes in load current and during start-up and do not affect stability. **IMPORTANT:** Ensure that the combination of trace and wire inductance, and the input capacitor chosen do not cause unwanted ringing because of the resonance formed by the LC tank circuit. Keep input traces and wires short to minimize resonance.

5.5.2 Output Capacitor

The RAA214020 is stable with a 22µF minimum ceramic output capacitor on the VOUT pin.

A larger value output capacitor generally improves the transient response because of large changes in load current but can also increase the load transient response time because of the decreased loop bandwidth. A disadvantage to increasing the output capacitor value is increased output noise and longer load transient response times.

The high frequency PSRR can be improved to target specific frequencies such as from a switching regulator if the output capacitor PSRR peak is chosen to equal the switching frequency of the upstream supply noise.

Additional output capacitors can be paralleled with the 22µF to improve PSRR and output noise performance across a wider frequency range.

5.5.3 C_{SET} Capacitor

The RAA214020 requires a minimum 100nF C_{SET} bypass capacitor on the CSET pin for stability. Increasing the C_{SET} value reduces the output noise and increases PSRR and the start-up time.

Some ceramic capacitors experience a piezoelectric response that causes the capacitor to generate noise when exposed to mechanical stress or thermal transients. Most high dielectric type (X5R and X7R) have a piezoelectric response. This appears as increased low-frequency noise on the output. To remedy this, Renesas recommends using low dielectric type ceramic capacitors such as NP0 or C0G capacitors that have negligible piezoelectric effects.

Note: Large leakage currents on the CSET pin can cause DC offsets and adds additional noise to the output voltage. Therefore leakage currents around this pin should be minimized.

5.5.3.1 Noise Optimization

For low-noise applications, a 1µF C_{SET} capacitor is optimal. Larger capacitor values can be used with little benefit in lowering the internally generated output voltage noise for frequencies above 10Hz.

5.5.3.2 Fast Start-Up

The RAA214020 incorporates fast start-up circuitry by default to rapidly charge the C_{SET} capacitor. This decreases the output voltage ramp-time because the C_{SET} node voltage sets the output voltage as well. The RAA214020 switches to the normal regulation circuitry when V_{OUT} reaches 90% of its final value.

When switching between the fast start-up circuitry and the normal regulation circuitry, the C_{SET} capacitor experiences a sudden open-circuit, which exercises the dielectric absorption of the capacitor. Depending on the amount of dielectric absorption of the C_{SET} capacitor, the switch between the fast start-up circuitry and the normal regulation circuitry can cause the output voltage to droop by 10s of millivolts during startup. Depending on the value of the output capacitor, the droop can take a second or longer to recover. The Dielectric absorption can depend on package size, voltage rating, dielectric material, and even manufacturer technology. Therefore, the C_{SET} capacitor needs to be evaluated if minimizing the output voltage droop is important.

5.5.3.3 Start-Up Time

The start-up time of the RAA214020 can be adjusted by changing the headroom voltage and the value of the C_{SET} capacitor. The start-up time of the RAA214020 is defined as the as the time it takes for the output voltage to rise to 90% of its programmed value as soon as the V_{EN} crosses its threshold.

- Increasing the headroom voltage or decreasing the C_{SET} capacitor decreases the start-up time.
- Decreasing the headroom voltage or increasing the C_{SET} capacitor increases the start-up time.

When using capacitor values larger than 1uF, the dielectric absorption effect can be more noticeable because large value capacitors can have more dielectric absorption. Furthermore, the droop noticeably takes longer to recover because the LDO has switched over to the normal regulation circuitry and therefore does not have the benefit of fast charging from the fast-start circuitry.

5.6 Power Dissipation and Thermals

To ensure reliable operation, the die junction temperature (T_J) of the RAA214020 must not exceed +125°C. In applications with high ambient temperature (T_A), large headroom voltages ($V_{HEADROOM}$), and large load currents (I_{OUT}), the heat dissipated in the package can become large enough to cause the T_J to exceed the maximum operating temperature of +125°C.

5.6.1 Power Dissipation

The Power Dissipation (PD) is calculated using Equation 8.

(EQ. 8) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times IQ(V_{IN})$$

Because the power dissipation contribution from the quiescent (or ground current) is typically small compared to the current the LDO needs to supply to a load, it can be ignored and Equation 8 simplifies to Equation 9.

(EQ. 9) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, to lower the power dissipated inside the die, the $V_{HEADROOM}$ and/or the I_{OUT} can be decreased.

5.6.2 The Junction Temperature and Thermal Resistance

The junction temperature (T_J) is the sum of the environmental ambient temperature (T_A) and the temperature rise in the T_J because of power dissipation, which is calculated using Equation 10 if the ambient temperature, Power Dissipation, and θ_{JA} are known.

(EQ. 10) $$T_J = T_A + \theta_{JA} \times PD$$

The θ_{JA} is the thermal resistance between the junction temperature and ambient temperature and is largely dependent on the device package and the PCB design. The θ_{JA} includes the thermal resistance of the junction to

the bottom thermal pad ($\theta_{JC(BOTTOM)}$) and the resistance of the junction to the top of the package ($\theta_{JC(TOP)}$). These two thermal resistances are determined by the package features, dimensions, areas, thicknesses, and materials and therefore are fixed.

The remaining thermal resistance that makes up θ_{JA} largely depends on the total PCB copper area, copper weight, location of the thermal planes, and location of the IC on the PCB, amongst other things. Therefore, to compare the θ_{JA} of different products it is important to ensure the PCB layouts are similar, which is why the JEDEC standard exists.

5.6.2.1 θ_{JA} for Different Copper Area Sizes

Table 3 shows typical θ_{JA} values of the 10 Ld 3x3mm DFN package for various PCB copper areas and the JEDEC std. board to illustrate how the θ_{JA} can be improved with attention to board layout. See the Guidelines for layout recommendations.

Table 3. Typical Theta JA Values for the 10Ld 3x3 DFN Package for Various PCB Copper Areas (4-layer)

PCB Type	FR-4 PCB Size	Top Cu Detail	Bottom Cu Detail	2 Buried Cu Planes tkn	Buried Cu Planes size		# PCB thermal vias Under Pkg	θ_{JA} of 10ld 3x3mm DFN (°C/W)
					(mm)	(inch)		
JEDEC std. PCB	76.2mmx 114.3mm	JEDEC std. 0.25mm wide (2oz thick) traces extend from the pkg.	No meaningful Cu on bottom	1-oz each	74.2mmx 74.2mm	2.92”x2.92”	4 (which touch 1 buried plane)	50 (JEDEC)
Eval PCB	76.2mmx 76.2mm	0.25mm wide (2oz thick) traces extend from the pkg.	2-oz, 76.2mmx76.2mm	1-oz each	76.2mmx 76.2mm	3” x 3”	6 (which touch 2 buried planes and bottom plane)	32
Eval PCB	50.8mmx 50.8mm	0.25mm wide (2oz thick) traces extend from the pkg.	2-oz, 50.8mmx50.8mm	1-oz each	50.8mmx 50.8mm	2” x2”	6 (which touch 2 buried planes and bottom plane)	39
Eval PCB	25.4mmx 25.4mm	0.25mm wide (2oz thick) traces extend from the pkg.	2-oz, 25.4mm x 25.4mm	1-oz each	25.4mmx 25.4mm	1” x 1”	6 (which touch 2 buried planes and bottom plane)	58

The following figures provide information about the recommended maximum power dissipation for target Junction Temperatures for the same boards listed in Table 3.

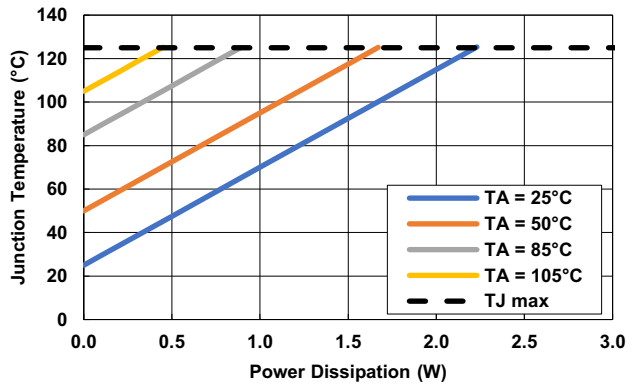


Figure 140. Power Dissipation vs Junction Temperature for Various T_A on the JEDEC Standard PCB

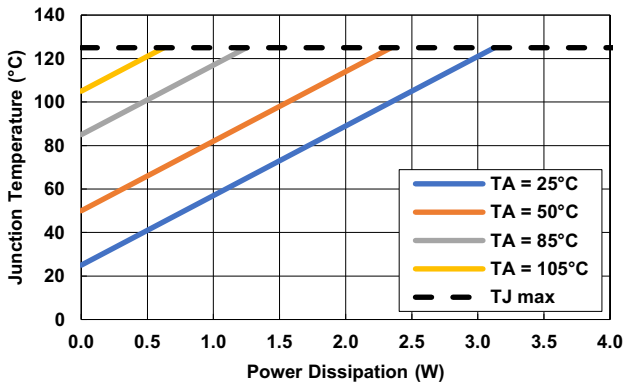


Figure 141. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 3x3" PCB

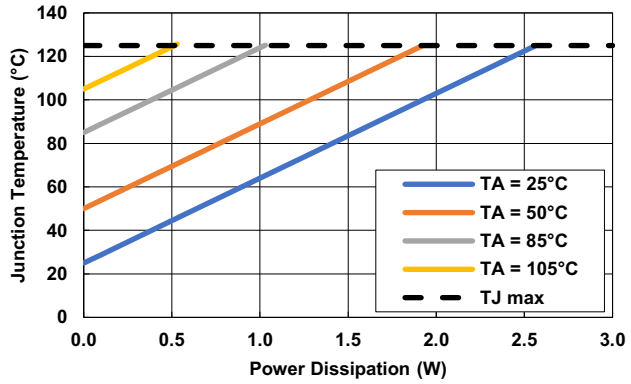


Figure 142. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 2x2" PCB

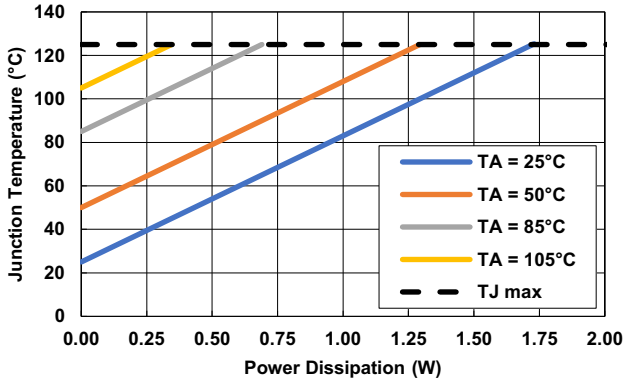


Figure 143. Power Dissipation vs Junction Temperature for Various T_A on a Thermally Optimized 1x1" PCB

To maximize the Theta JA required for a design while keeping copper area size to a minimum, use Figure 144 to determine the heat sinking area required.

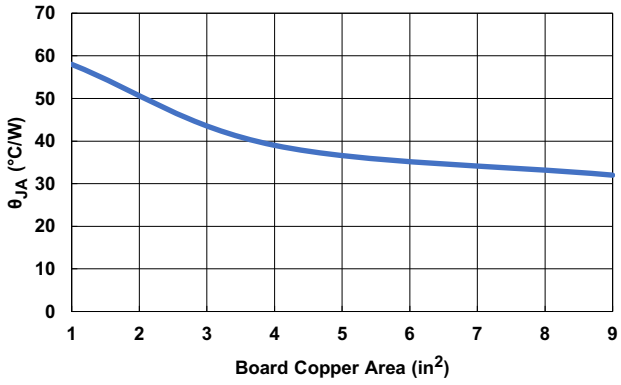


Figure 144. θ_{JA} vs Copper Area Sizes

5.7 Layout

5.7.1 Guidelines

The following are recommendations for the RAA214020 to achieve optimal performance:

- Place all the required components for the RAA214020 on the same layer as the IC.
- Place a minimum capacitance of 10µF ceramic input capacitor to the VIN and GND pins of the LDO as close as practical.
- Place a minimum capacitance of 22µF ceramic output capacitor to the VOUT and GND pins of the LDO as close as practical
- The package thermal EPAD is the largest heat conduction path for the package. It should be soldered to a copper pad on the PCB underneath the part. The PCB thermal pad should have as many plated vias to increase the heat flow from the package thermal EPAD to the inner PCB areas and/or the bottom PCB area. Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow. For efficient heat transfer, it is important that the vias have low thermal resistance. Do not use thermal relief patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane. The top copper GND layer, that the EPAD is connected to is the least thermally resistant path for heat flow. To this end, minimize the components and traces that cut this layer.

Figure 145 illustrates the recommended layout scheme.

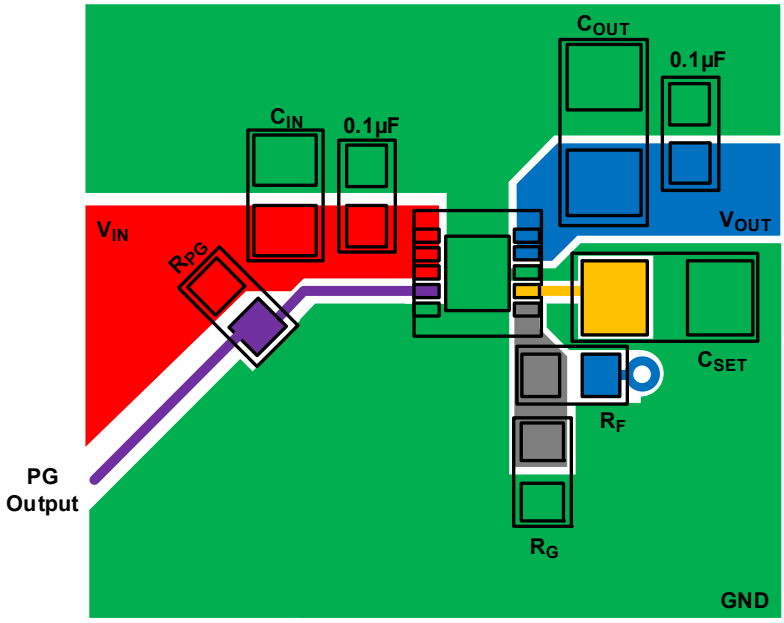


Figure 145. Layout Scheme

6. RAA214020 SPICE Model

The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, PSRR, Gain, and Phase. The DC parameters are output voltage accuracy, dropout voltage, fast mode startup, and output current limit. The model uses typical parameters given in the Electrical Specifications. The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figure 146 through Figure 148 show the characterization vs simulation results for the PSRR, Noise Voltage, and Closed Loop Gain vs Frequency.

The spice model can be found at RAA214020. The webpage provides the subcircuit .opj file with built in test circuits. Also included is the validation data of the model.

6.1 Characterization vs Simulation Results

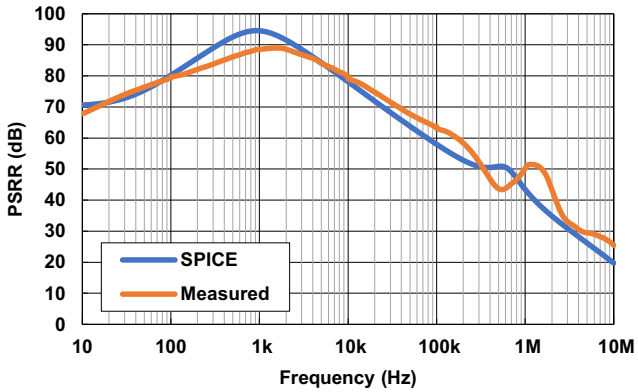


Figure 146. PSRR vs Frequency for SPICE Compared to Measured Results (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A, C_{SET} = 1µF, C_{OUT} = 22µF)

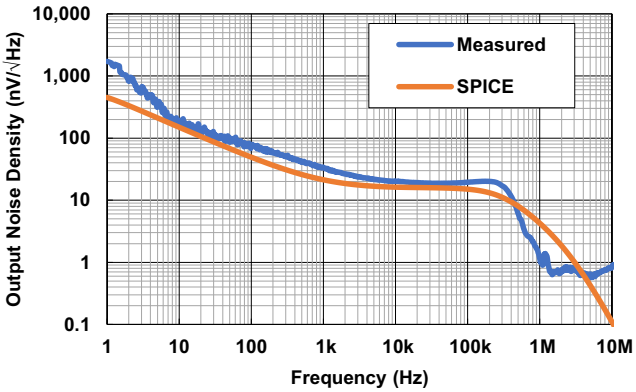


Figure 147. Output Noise vs Frequency for SPICE Compared to Measured Results (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A, C_{SET} = 1µF, C_{OUT} = 22µF)

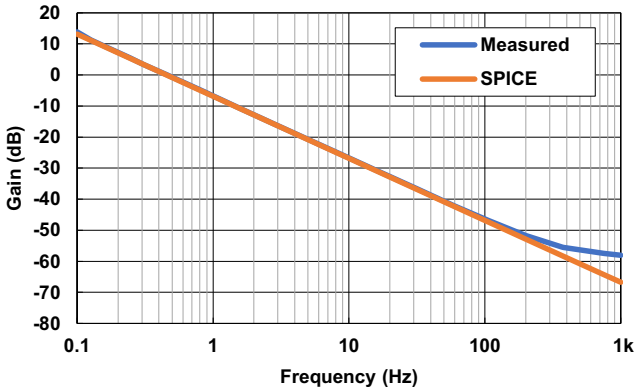
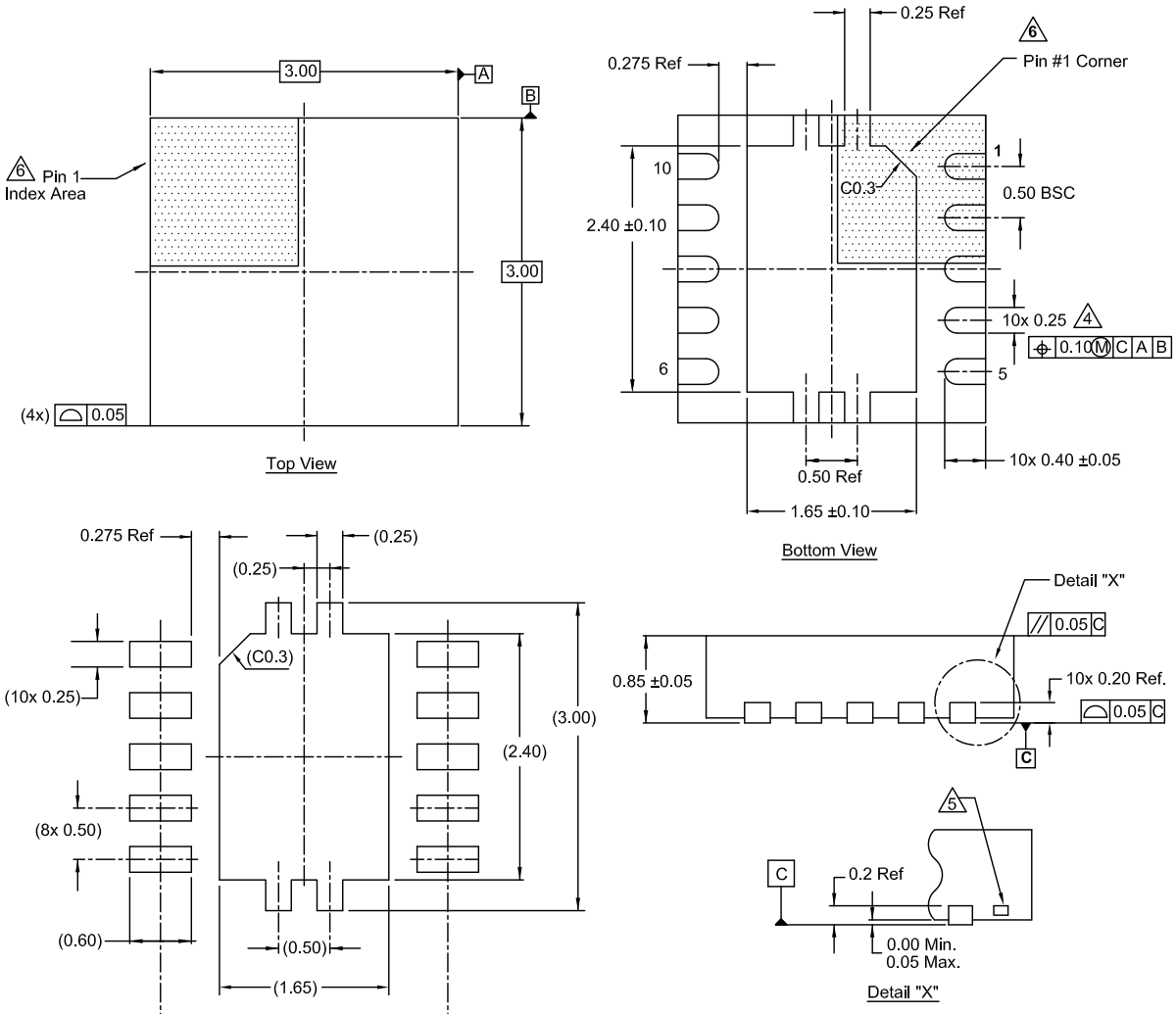


Figure 148. Gain vs Frequency for SPICE Compared to Measured Results (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A, C_{SET} = 1µF, C_{OUT} = 22µF, Phase = 90° to 200kHz)

7. Package Outline Drawing

For the most recent package outline drawing, see L10.3x3F.

L10.3x3F
10 Lead Dual Flat No-Leads Plastic Package
Rev 0, 1/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.

8. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA214020GNP#MD0	020	10 Ld DFN	L10.3x3F	Reel, 250	-40 to +125°C
RAA214020GNP#HD0				Reel, 6k	
RTKA214020DE0010BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA214020 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 4. Key Differences Between Family of Parts

Part Number	Minimum V_{OUT} (V)	Output Voltage Adjustable	Package
RAA214020	0.9	Yes, through External Feedback Resistors	3 × 3mm 10 Ld DFN
RAA214023	0.8	Yes, through External Feedback Resistors or convenient IC pins	3.5 × 3.5 mm 20 Ld QFN or 5 × 5 mm 20 Ld QFN

9. Revision History

Rev.	Date	Description
2.01	Dec 17, 2021	Updated Figure 132.
2.00	Oct 22, 2021	Updated description on page 1. Updated Features section. Updated Figures 1, 2, 101, 102, 129 Updated Tables 1, 2, and 4. Updated HBM ESD value from 2kV to 3kV. Updated heading on Electrical Specification table. Updated the typical values for the following parameters: Load Regulation, Internal Current Limit, Start-Up Time, Thermal Shutdown, Thermal Shutdown Hysteresis, PSRR2, and PSRR3 Added Figures 111, 112, 123, 124, 125, 126, 132, 133, 134, and 135. Updated the following sections: Application Overview, Theory of Operation of PMOS LDOs, Ultra-Low Output Noise, High Power Supply Ripple Rejection (PSRR), Load Transient Response, UVLO, Enable Control, Internal Current Limit (ILIM), Thermal Protection, Power-Good (PG) Indication, External Bypass Capacitor Selection, Input Capacitor, Output Capacitor, Fast Start-Up, and Start-Up Time
1.00	Jun 2, 2021	Initial release

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(Rev.1.0 Mar 2020)

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