MOSFET – Power, P-Channel, DPAK

-60 V, -12 A

NTD2955, NVD2955

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low-voltage, high-speed switching applications in power supplies, converters, and power motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer an additional safety margin against unexpected voltage transients.

Features

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Designed for Low-Voltage, High-Speed Switching Applications and to Withstand High Energy in the Avalanche and Commutation Modes
- NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

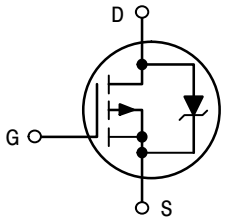
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	−60	Vdc
Gate-to-Source Voltage − Continuous − Non-repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current − Continuous @ T_a = 25 °C − Single Pulse ($t_p \le 10$ ms)	I_D I_{DM}	−12 −18	Adc Apk
Total Power Dissipation @ T_a = 25 °C	P_D	55	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy − Starting T_J = 25 °C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 12 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	216	mJ
Thermal Resistance − Junction-to-Case − Junction-to-Ambient (Note 1) − Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.73 71.4 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in. from case for 10 seconds	T_L	260	°C

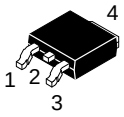
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in pad size (Cu area = 1.127 in^2).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu area = 0.412 in^2).

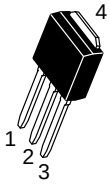
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−60 V	155 mΩ @ −10 V, 6 A	−12 A



P-Channel

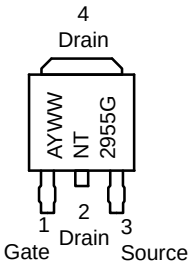


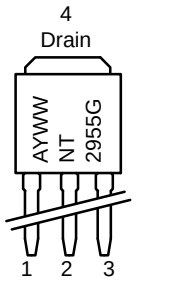
DPAK
CASE 369C
STYLE 2



IPAK
CASE 369D
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS





A	= Assembly Location*
NT2955/NV2955	= Specific Device Code (DPAK)
NT2955	= Specific Device Code (IPAK)
Y	= Year
WW	= Work Week
G	= Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = −0.25 mA) (Positive Temperature Coefficient)	$V_{(BR)DSS}$	−60 −	− 67	− −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = −60 Vdc, T_J = 25 °C) (V_{GS} = 0 Vdc, V_{DS} = −60 Vdc, T_J = 150 °C)	I_{DSS}	− −	− −	−10 −100	μAdc
Gate-Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	−	−	−100	nAdc
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μAdc) (Negative Temperature Coefficient)	$V_{GS(th)}$	−2.0 −	−2.8 4.5	−4.0 −	Vdc mV/°C
Static Drain-Source On-State Resistance (V_{GS} = −10 Vdc, I_D = −6.0 Adc)	$R_{DS(on)}$	−	0.155	0.180	Ω
Drain-to-Source On-Voltage (V_{GS} = −10 Vdc, I_D = −12 Adc) (V_{GS} = −10 Vdc, I_D = −6.0 Adc, T_J = 150 °C)	$V_{DS(on)}$	− −	−1.86 −	−2.6 −2.0	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6.0 Adc)	g_{FS}	−	8.0	−	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = −25 Vdc, V_{GS} = 0 Vdc, F = 1.0 MHz)	C_{iss}	−	500	750	pF
Output Capacitance		C_{oss}	−	150	250	
Reverse Transfer Capacitance		C_{rss}	−	50	100	
SWITCHING CHARACTERISTICS (Notes 3 and 4)						
Turn-On Delay Time	(V_{DD} = −30 Vdc, I_D = −12 A, V_{GS} = −10 V, R_G = 9.1 Ω)	$t_{d(on)}$	−	10	20	ns
Rise Time		t_r	−	45	85	
Turn-Off Delay Time		$t_{d(off)}$	−	26	40	
Fall Time		t_f	−	48	90	
Gate Charge	(V_{DS} = −48 Vdc, V_{GS} = −10 Vdc, I_D = −12 A)	Q_T	−	15	30	nC
		Q_{GS}	−	4.0	−	
		Q_{GD}	−	7.0	−	
DRAIN-SOURCE DIODE CHARACTERISTICS (Note 3)						
Diode Forward On-Voltage (I_S = 12 Adc, V_{GS} = 0 V) (I_S = 12 Adc, V_{GS} = 0 V, T_J = 150 °C)		V_{SD}	− −	−1.6 −1.3	−2.5 −	Vdc
Reverse Recovery Time (I_S = 12 A, dI_S/dt = 100 A/μs, V_{GS} = 0 V)		t_{rr}	−	50	−	ns
		t_a	−	40	−	
		t_b	−	10	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.10	−	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

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TYPICAL PERFORMANCE CURVES (T_J = 25 °C unless otherwise noted)

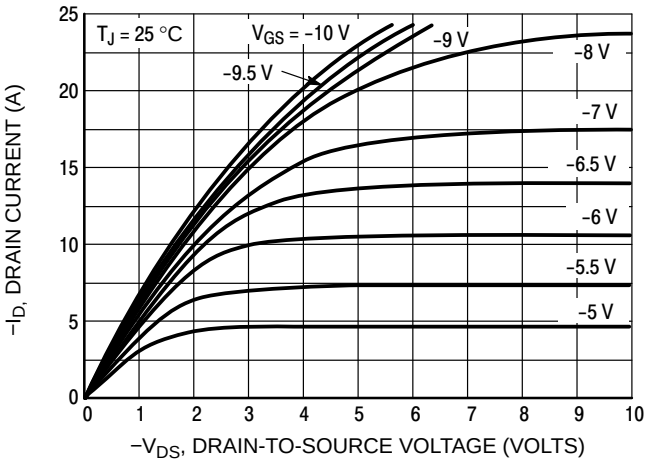


Figure 1. On-Region Characteristics

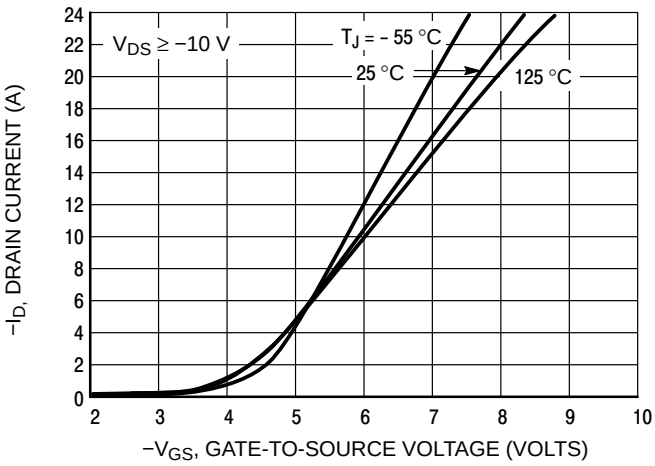


Figure 2. Transfer Characteristics

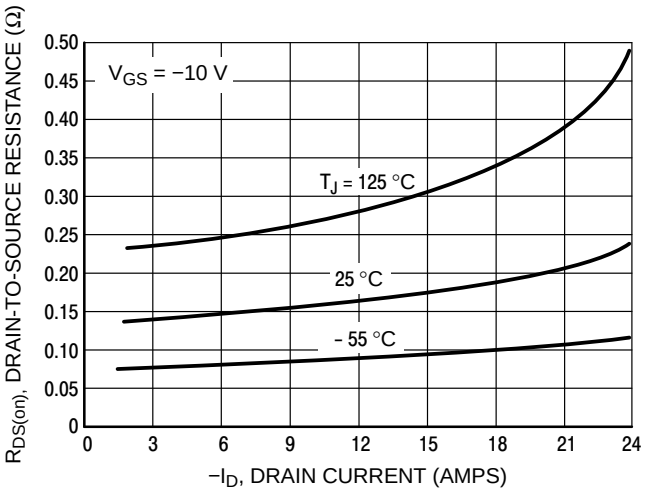


Figure 3. On-Resistance versus Drain Current and Temperature

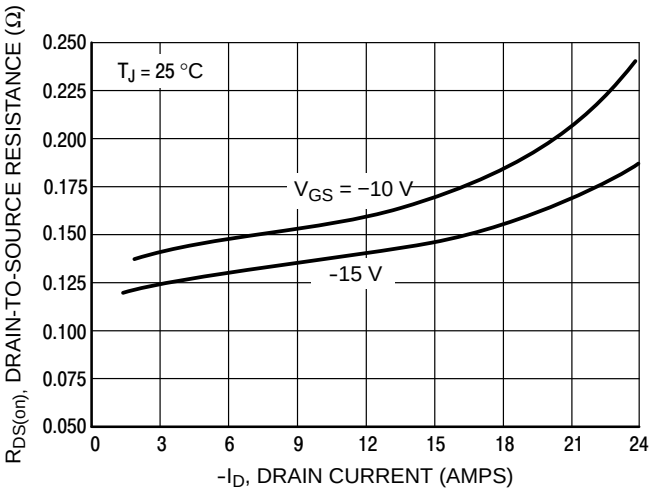


Figure 4. On-Resistance versus Drain Current and Gate Voltage

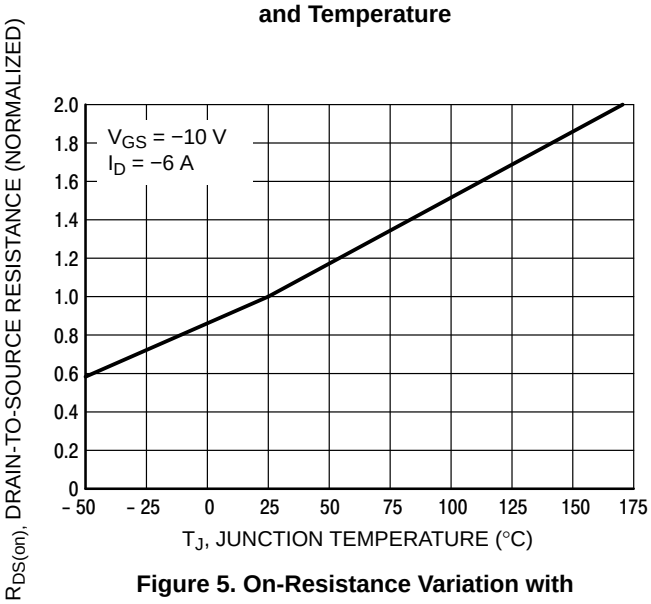


Figure 5. On-Resistance Variation with Temperature

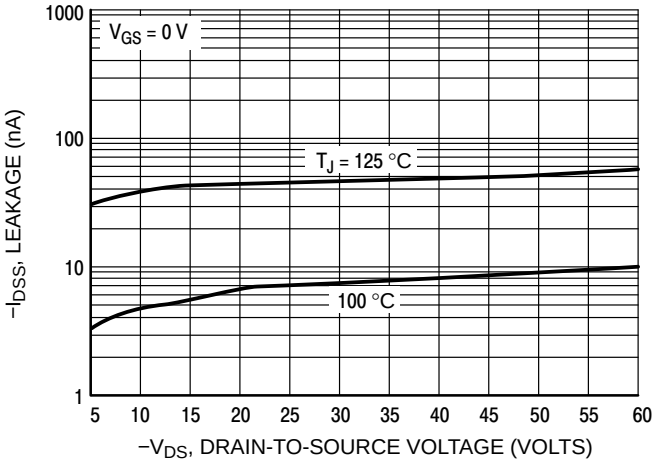


Figure 6. Drain-To-Source Leakage Current versus Voltage

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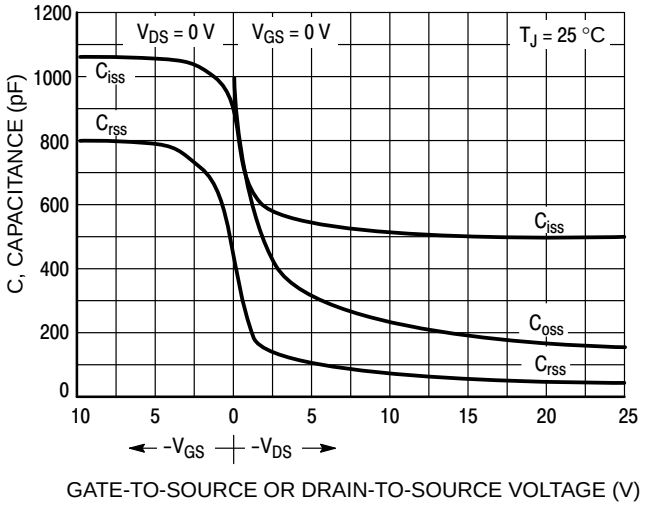


Figure 7. Capacitance Variation

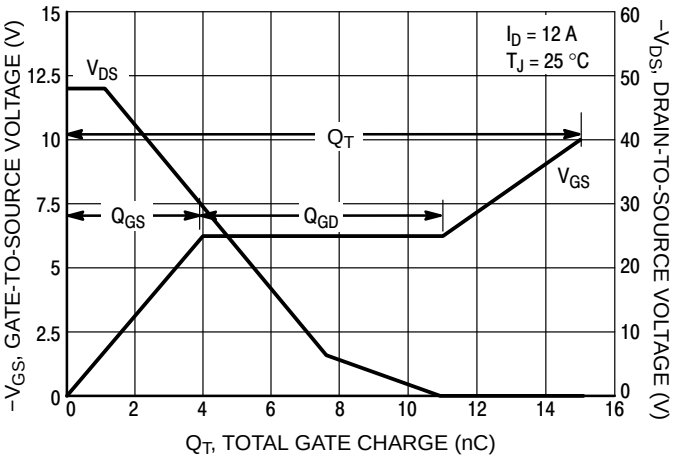


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

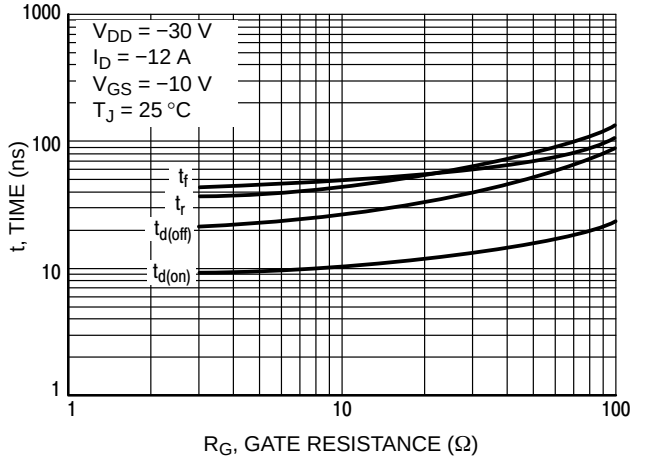


Figure 9. Resistive Switching Time Variation versus Gate Resistance

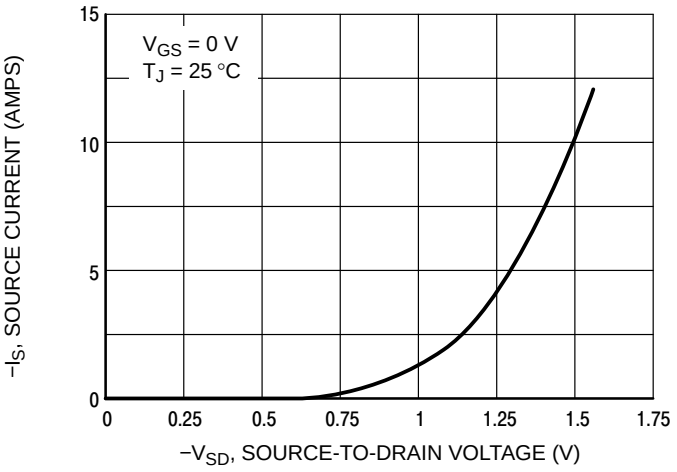


Figure 10. Diode Forward Voltage versus Current

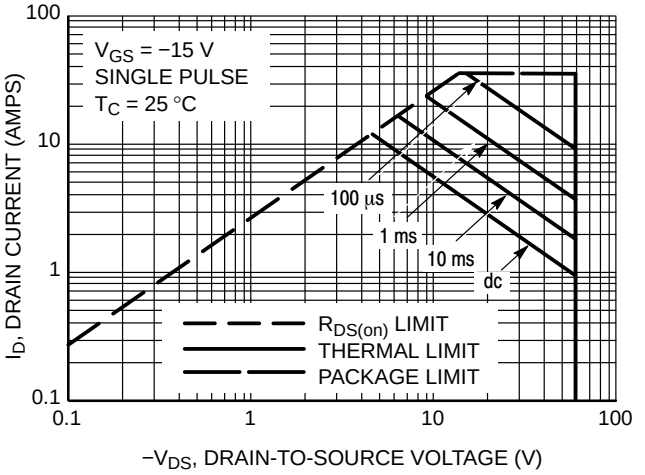


Figure 11. Maximum Rated Forward Biased Safe Operating Area

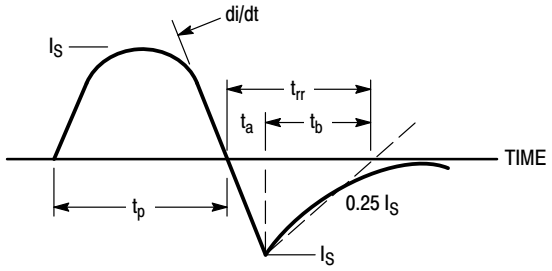


Figure 12. Diode Reverse Recovery Waveform

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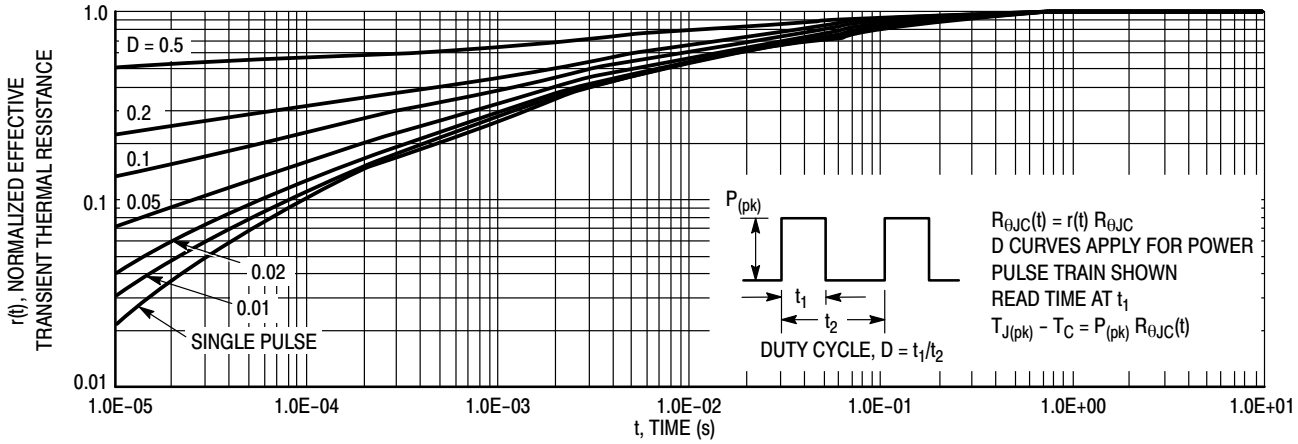


Figure 13. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTD2955T4G	DPAK (Pb-Free)	2500 / Tape & Reel
SVD2955T4G*	DPAK (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

NTD2955G	DPAK (Pb-Free)	75 Units / Rail
NTD2955-1G	IPAK (Pb-Free)	75 Units / Rail
NVD2955T4G*	DPAK (Pb-Free)	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

5. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

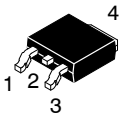
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REVISION HISTORY

Revision	Description of Changes	Date
17	Rebranded the document to **onsemi** format. NTD2955G, NTD2955-1G, NVD2955T4G OPNs marked as Discontinued.	4/21/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

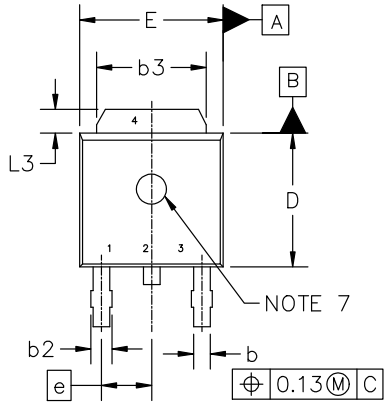
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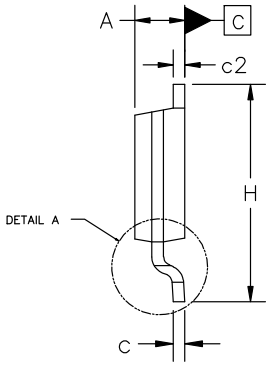
SCALE 1:1

DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE L

DATE 24 AUG 2026

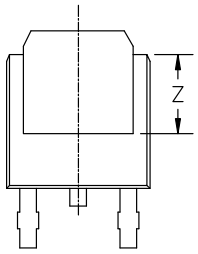


TOP VIEW

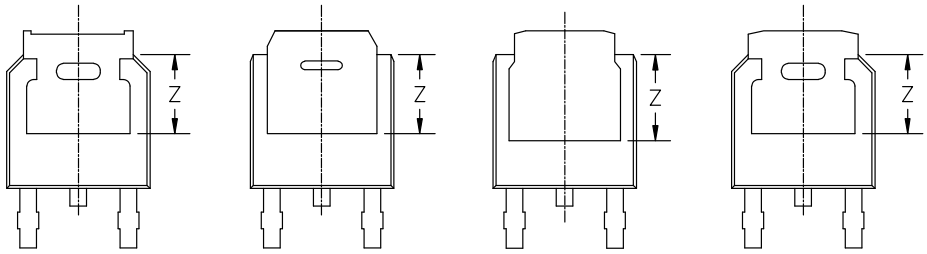


SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	−−−	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	−−−	1.27
L4	−−−	−−−	1.01
Z	3.93	−−−	−−−



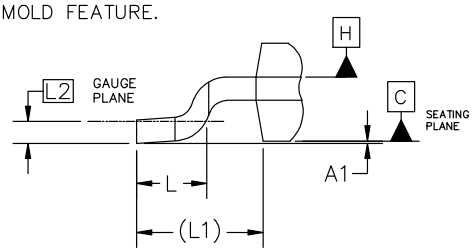
BOTTOM VIEW



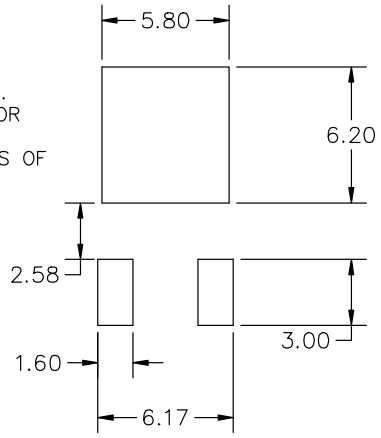
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

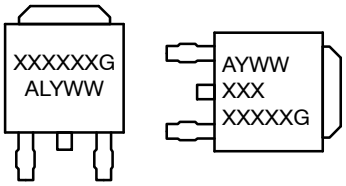
DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK−3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

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DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE L

DATE 24 AUG 2026

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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