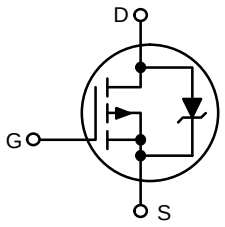
# MOSFET – Power, Single, P-Channel, DPAK

## -60 V, -15.5 A

# NTD20P06L, NTDV20P06L

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX (Note 1) |
|---|---|---|
| −60 V | 130 mΩ @ −5.0 V | −15.5 A |

**P-Channel**



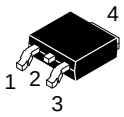

### Features

- Withstands High Energy in Avalanche and Commutation Modes
- Low Gate Charge for Fast Switching
- AEC Q101 Qualified − NTDV20P06L
- These Devices are Pb-Free and are RoHS Compliant

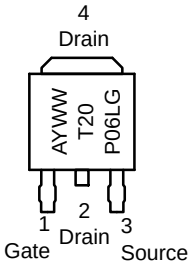
### Applications

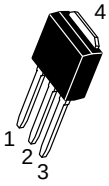
- Bridge Circuits
- Power Supplies, Power Motor Controls
- DC-DC Conversion

### MARKING DIAGRAMS

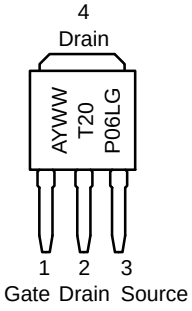



**DPAK**
**CASE 369C**
**STYLE 2**




**IPAK/DPAK**
**CASE 369D**
**STYLE 2**




| | |
|---|---|
| 20P06L | Device Code |
| A | = Assembly Location |
| Y | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

### MAXIMUM RATINGS ($T_J$ = 25 °C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain-to-Source Voltage | | | $V_{DSS}$ | −60 | V |
| Gate-to-Source Voltage | Continuous | | $V_{GS}$ | ±20 | V |
| | Non-Repetitive | $t_p \le 10$ ms | $V_{GSM}$ | ±30 | |
| Continuous Drain Current | Steady State | $T_C$ = 25 °C | $I_D$ | −15.5 | A |
| Power Dissipation | Steady State | $T_C$ = 25 °C | $P_D$ | 65 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | ±50 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 175 | °C |
| Single Pulse Drain-to-Source Avalanche Energy ($V_{DD}$ = 25 V, $V_{GS}$ = 5 V, $I_{PK}$ = 15 A, L = 2.7 mH, $R_G$ = 25 Ω) | | | $E_{AS}$ | 304 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | $T_L$ | 260 | °C |

### THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction-to-Case (Drain) | $R_{\theta JC}$ | 2.3 | °C/W |
| Junction-to-Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 80 | |
| Junction-to-Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 110 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq.)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −60 | −74 | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | −64 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = −60 V | $T_J$ = 25 °C | | | −1.0 | μA |
| | | | $T_J$ = 150 °C | | | −10 | |
| Gate-to-Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −1.0 | −1.5 | −2.0 | V |
| Gate Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 3.1 | | mV/°C |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −5.0 V, $I_D$ = −7.5 A | | | 0.130 | 0.150 | Ω |
| | | $V_{GS}$ = −5.0 V, $I_D$ = −15 A | | | 0.143 | | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = −10 V, $I_D$ = −7.5 A | | | 11 | | S |
| Drain-to-Source On-Voltage | $V_{DS(on)}$ | $V_{GS}$ = −5.0 V, $I_D$ = −7.5 A | $T_J$ = 25 °C | | | −1.2 | V |
| | | | $T_J$ = 150 °C | | | −1.9 | |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = −25 V | | | 740 | 1190 | pF |
| Output Capacitance | $C_{OSS}$ | | | | 207 | 300 | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 66 | 120 | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = −5.0 V, $V_{DS}$ = −48 V, $I_D$ = −18 A | | | 15 | 26 | nC |
| Gate-to-Source Charge | $Q_{GS}$ | | | | 4.0 | | |
| Gate-to-Drain Charge | $Q_{GD}$ | | | | 7.0 | | |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = −5.0 V, $V_{DD}$ = −30 V, $I_D$ = −15 A, $R_G$ = 9.1 Ω | | | 11 | 20 | ns |
| Rise Time | $t_r$ | | | | 90 | 180 | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | | 28 | 50 | |
| Fall Time | $t_f$ | | | | 70 | 135 | |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −15 A | $T_J$ = 25 °C | | 1.5 | 2.5 | V |
| | | | $T_J$ = 150 °C | | 1.3 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $d_{IS}/d_t$ = 100 A/μs, $I_S$ = −12 A | | | 60 | | ns |
| Charge Time | $t_a$ | | | | 39 | | |
| Discharge Time | $t_b$ | | | | 21 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 0.13 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
4. Switching characteristics are independent of operating junction temperatures



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## TYPICAL PERFORMANCE CURVES

($T_J$ = 25 °C unless otherwise noted)

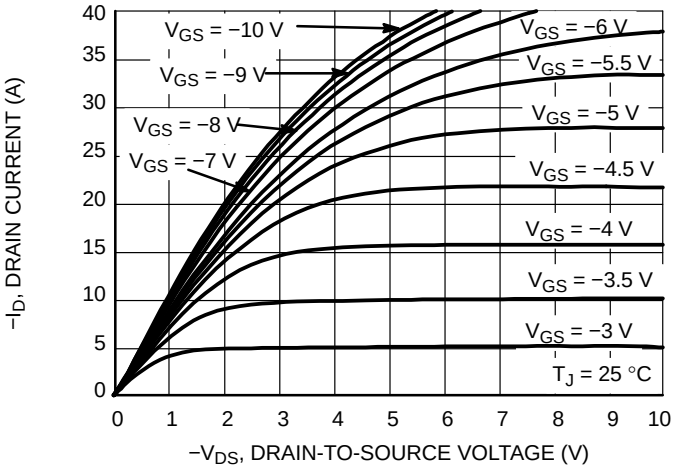



**Figure 1. On-Region Characteristics**

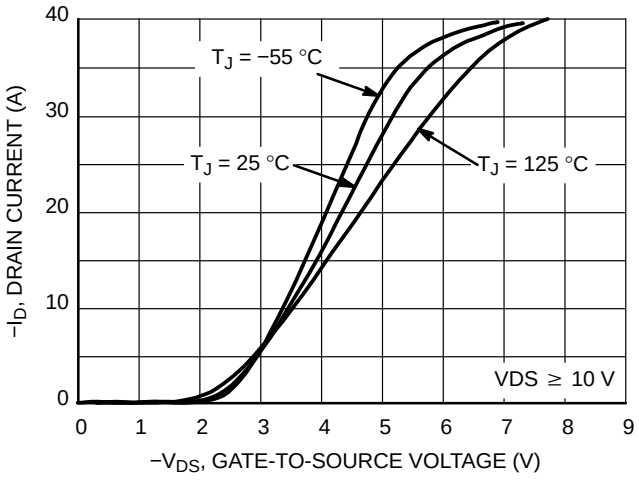



**Figure 2. Transfer Characteristics**

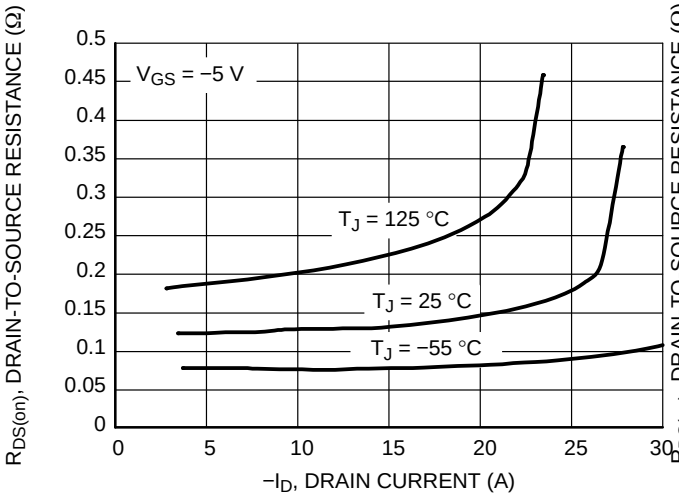



**Figure 3. On-Resistance versus Drain Current and Temperature**

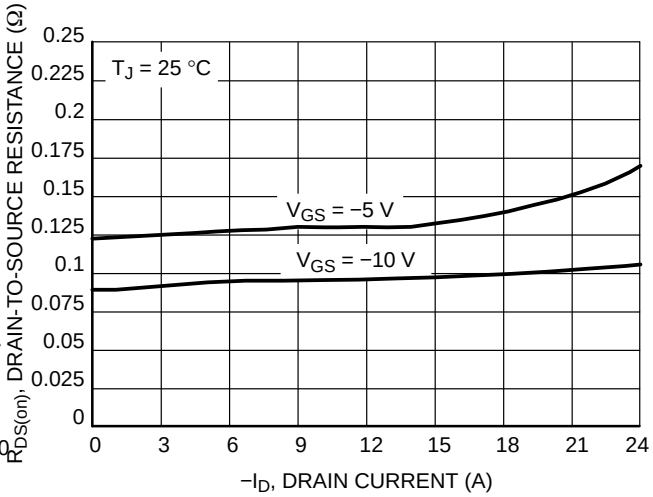



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

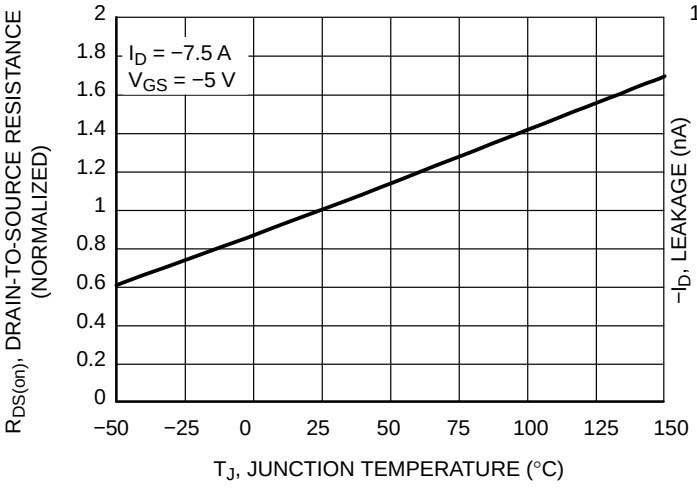



**Figure 5. On-Resistance Variation with Temperature**

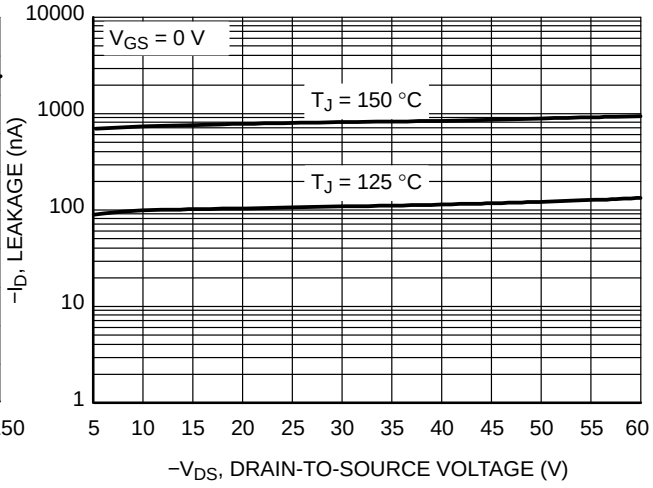



**Figure 6. Drain-to-Source Leakage Current versus Voltage**



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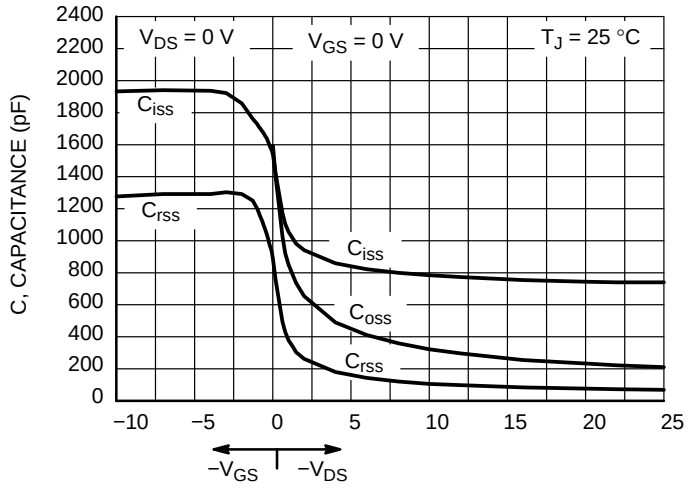



**Figure 7. Capacitance Variation**

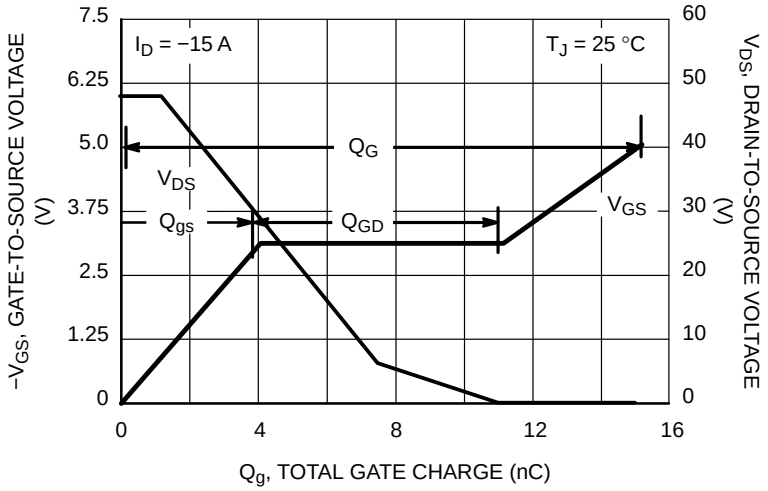



**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**

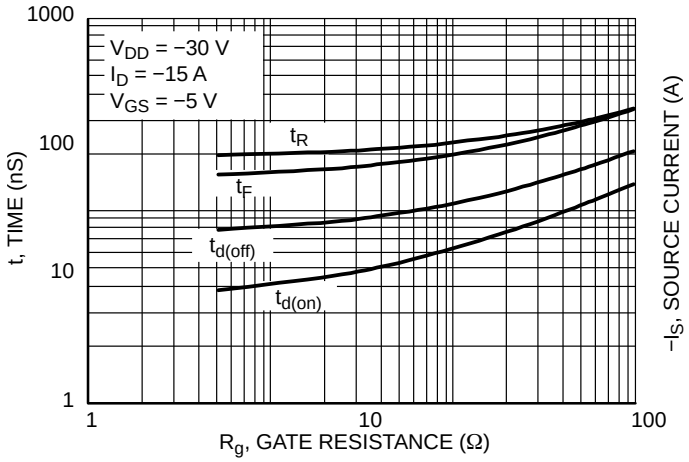



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

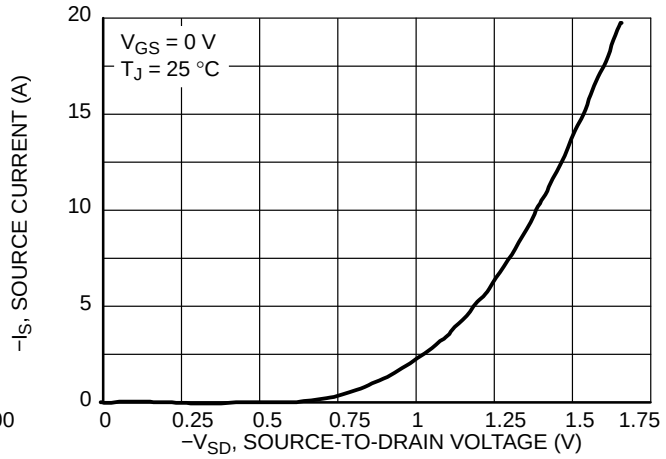



**Figure 10. Diode Forward Voltage versus Current**



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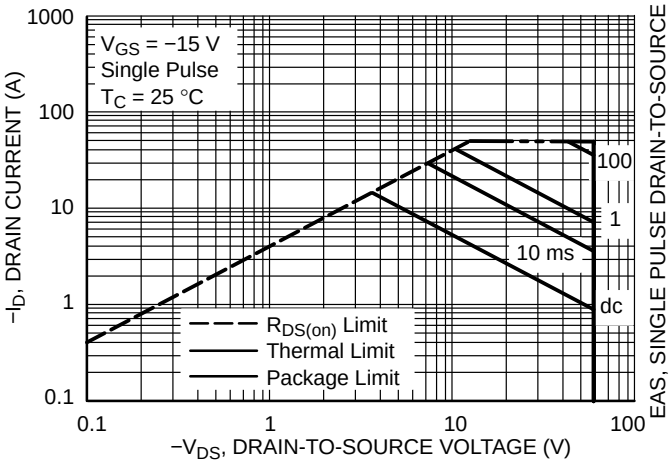



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

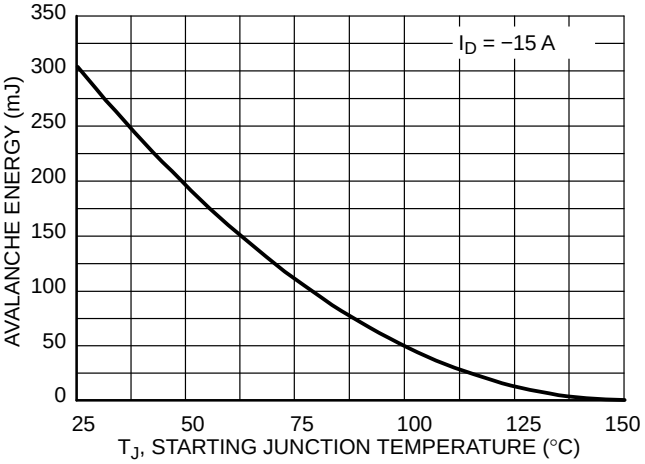



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

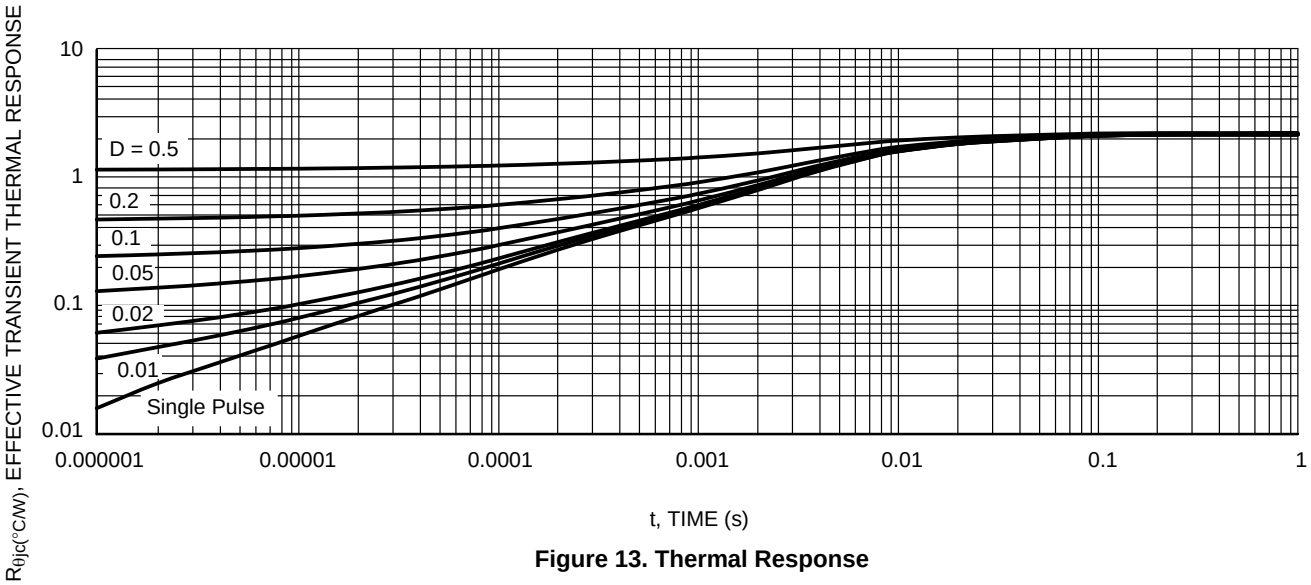



**Figure 13. Thermal Response**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTD20P06LT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NTDV20P06LT4G-VF01 | | 2500 / Tape & Reel |

**DISCONTINUED** (Note 5)

| | | |
|---|---|---|
| NTD20P06LG | DPAK (Pb-Free) | 75 Units / Rail |
| NTDV20P06LT4G | | 2500 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



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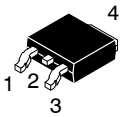
## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 9 | Rebranded the document to **onsemi** format.<br>NTD20P06LG, NTDV20P06LT4G OPNs marked as Discontinued. | 2/16/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



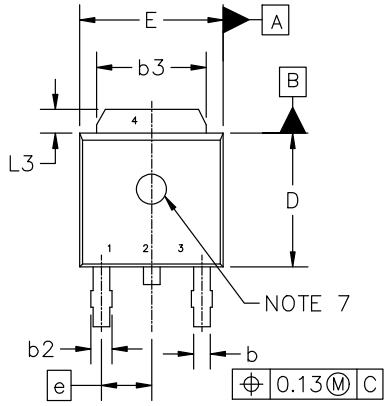
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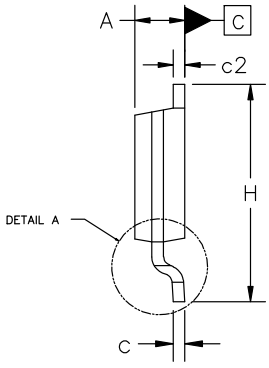

**SCALE 1:1**

**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

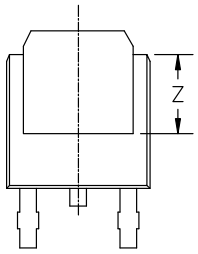



TOP VIEW

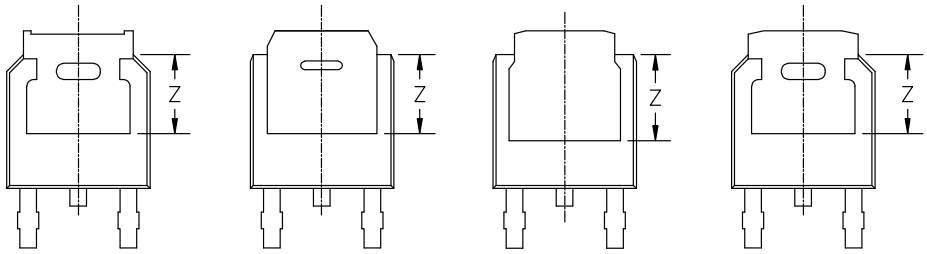



SIDE VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | −−− | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.72 | 0.93 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | −−− | 1.27 |
| L4 | −−− | −−− | 1.01 |
| Z | 3.93 | −−− | −−− |



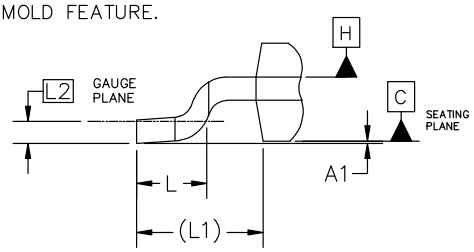

BOTTOM VIEW



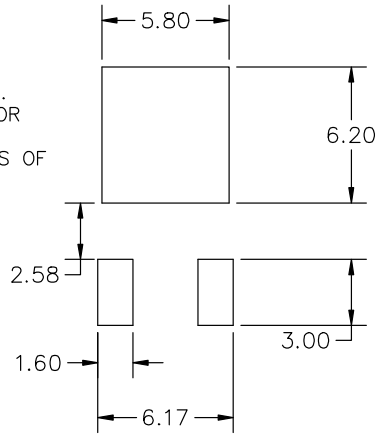

ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.




DETAIL A
ROTATED 90° CW




RECOMMENDED MOUNTING FOOTPRINT*
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

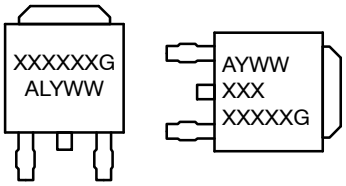
| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON10527D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **DPAK−3 6.10x6.54x2.28, 2.29P** | **PAGE 1 OF 2** |

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**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE




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