+5 Volt Electronic Fuse

NIS5135 Series

The NIS5135 is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It also includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue operation. Two thermal options are available, latching and auto−retry.

Features

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- 68 mΩ Typical
- Internal Charge Pump
- Internal Undervoltage Lockout Circuit
- Internal Overvoltage Clamp
- ESD Ratings: Human Body Model (HBM); 2000 V
  Machine Model (MM); 200 V
- These are Pb−Free Devices and are RoHS Compliant

Typical Applications

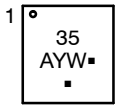
- Mother Board
- Hard Drives
- Fan Drives

3.6 AMP, 5 VOLT ELECTRONIC FUSE



DFN10
CASE 485C

MARKING DIAGRAM



Pin	Function
1–5	SOURCE
6	NC
7	ILIMIT
8	Enable/Fault
9	dv/dt
10	GND
11 (flag)	VCC

35 = Latching Version
35H = Auto−Retry Version
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 10 of this data sheet.

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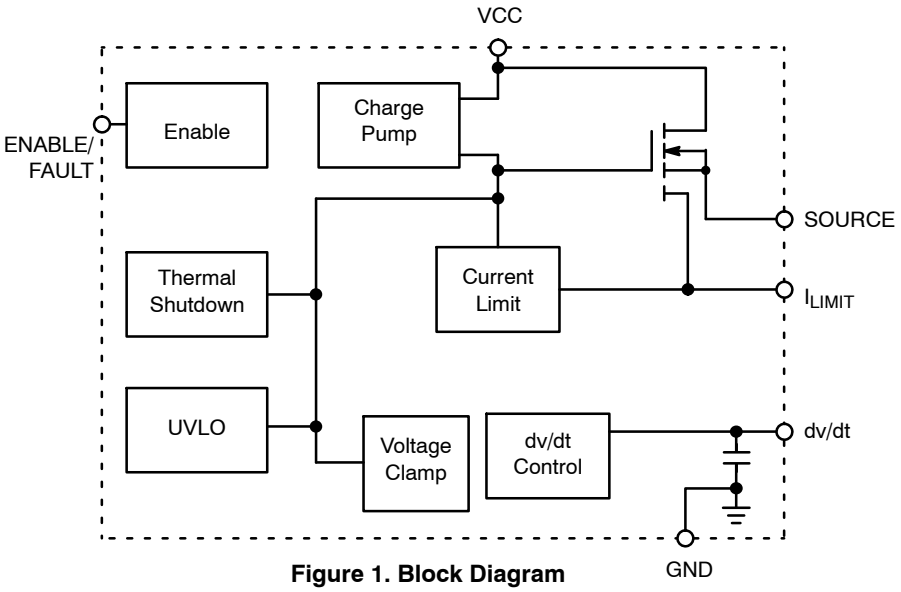


Figure 1. Block Diagram

Table 1. FUNCTIONAL PIN DESCRIPTION

Pin	Function	Description
1–5	Source	This pin is the source of the internal power FET and the output terminal of the fuse.
7	I_{Limit}	A resistor between this pin and the source pin sets the overload and short circuit current limit levels.
8	Enable/Fault	The enable/fault pin is a tri−state, bidirectional interface. It can be used to enable or disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 2 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
10	Ground	Negative input voltage to the device. This is used as the internal reference for the IC.
11 (belly pad)	V_{CC}	Positive input voltage to the device.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady−state (V_{CC} to GND, Note 1) Transient (100 ms)	V_{IN}	−0.6 to 18 −0.6 to 25	V
Thermal Resistance, Junction−to−Air 0.1 in^2 copper (Note 2) 0.5 in^2 copper (Note 2)	θ_{JA}	 227 95	°C/W
Thermal Resistance, Junction−to−Lead (Pin 1)	θ_{JL}	27	°C/W
Thermal Resistance, Junction−to−Case	θ_{JC}	20	°C/W
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_{max}	1.3 10.4	W mW/°C
Operating Temperature Range (Note 3)	T_J	−40 to 150	°C
Nonoperating Temperature Range	T_J	−55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.
2. 1 oz copper, double−sided FR4.
3. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than the maximum ratings for extended periods of time.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 5.0 V, C_L = 70 μF, dv/dt pin open, R_{LIMIT}= 10 Ω, T_J = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (enabling of chip to I_D = 100 mA with 1 A resistive load)	T_{dly}		500		μs
ON Resistance (Note 4) T_J = 140°C (Note 5)	R_{DSon}	54	68 95	82	mΩ
Off State Output Voltage (V_{CC} = 10 V_{dc}, V_{GS} = 0 V_{dc}, R_L = ∞)	V_{off}		50	200	mV
Output Capacitance V_{DS} = 5 V_{DC}, V_{GS} = 0 V_{DC}, R_L = ∞	C_{out}		230		pF
Continuous Current (T_A = 25°C, 0.5 in^2 pad) (Note 5) (T_A = 80°C, minimum copper)	I_D I_D		3.6 1.7		A
THERMAL LATCH					
Shutdown Temperature (Note 5)	T_{SD}	150	175	200	°C
Thermal Hysteresis (Decrease in die temperature for turn on, does not apply to latching parts)	T_{Hyst}		45		°C
UNDER/OVERVOLTAGE PROTECTION					
V_{OUT} Maximum (V_{CC} = 10 V)	$V_{out-clamp}$	5.95	6.65	7.35	V
Undervoltage Lockout (Turn on, Voltage Going High)	V_{UVLO}	3.2	3.6	4.0	V
UVLO Hysteresis	V_{Hyst}	–	0.40	–	V
CURRENT LIMIT					
Kelvin Short Circuit Current Limit (R_{Limit} = 11 Ω, Note 6)	I_{LIM}	2.3	3.1	3.9	A
Kelvin Overload Current Limit (R_{Limit} = 11 Ω, Note 6)	I_{LIM}		3.5		A
dv/dt Circuit					
Output Voltage Ramp Time (Enable to V_{OUT} = 4.7 V)	t_{slew}	0.70	1.4	2.4	ms
Maximum Capacitor Voltage	V_{max}			V_{CC}	V
ENABLE/FAULT					
Logic Level Low (Output Disabled)	V_{in-low}	0.35	0.58	0.81	V
Logic Level Mid (Thermal Fault, Output Disabled)	V_{in-mid}	0.82	1.4	1.95	V
Logic Level High (Output Enabled)	$V_{in-high}$	1.96	2.64	3.30	V
High State Maximum Voltage	V_{in-max}	3.40	4.30	5.2	V
Logic Low Sink Current (V_{enable} = 0 V)	I_{in-low}		−12	−20	μA
Logic High Leakage Current for External Switch (V_{enable} = 3.3 V)	$I_{in-leak}$			1.0	μA
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	Fan			3.0	Units
TOTAL DEVICE					
Bias Current (Operational)	I_{Bias}		1.5	2.0	mA
Bias Current (Shutdown)	I_{Bias}		1.0		mA
Minimum Operating Voltage (Notes 5 and 7)	V_{min}			3.1	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse test: Pulse width 300 μs, duty cycle 2%.
5. Verified by design.
6. Refer to explanation of short circuit and overload conditions in application note AND8140/D.
7. Device will shut down prior to reaching this level based on actual UVLO trip point.

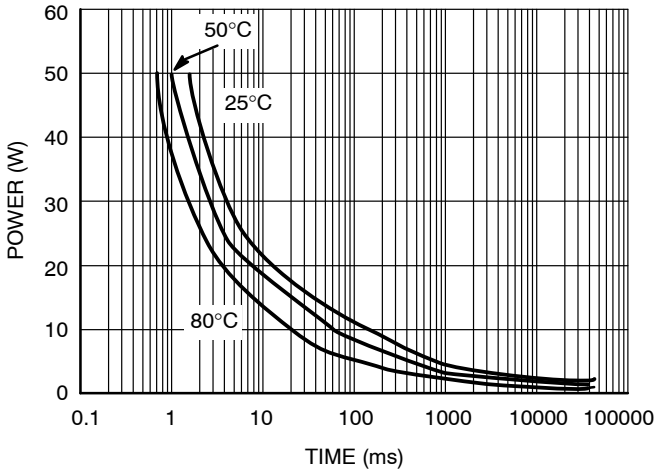


Figure 2. Power Dissipation vs. Thermal Trip Time

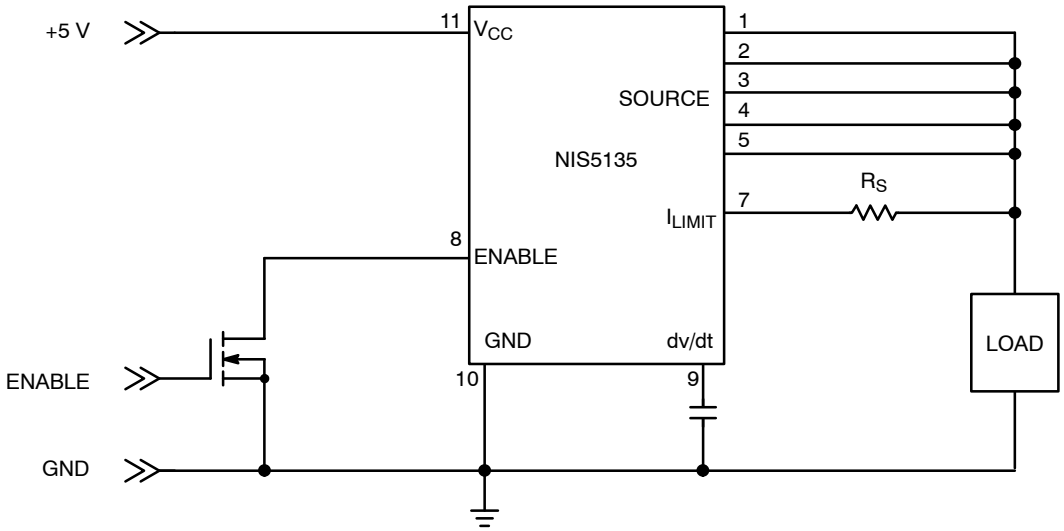


Figure 3. Application Circuit with Direct Current Sensing

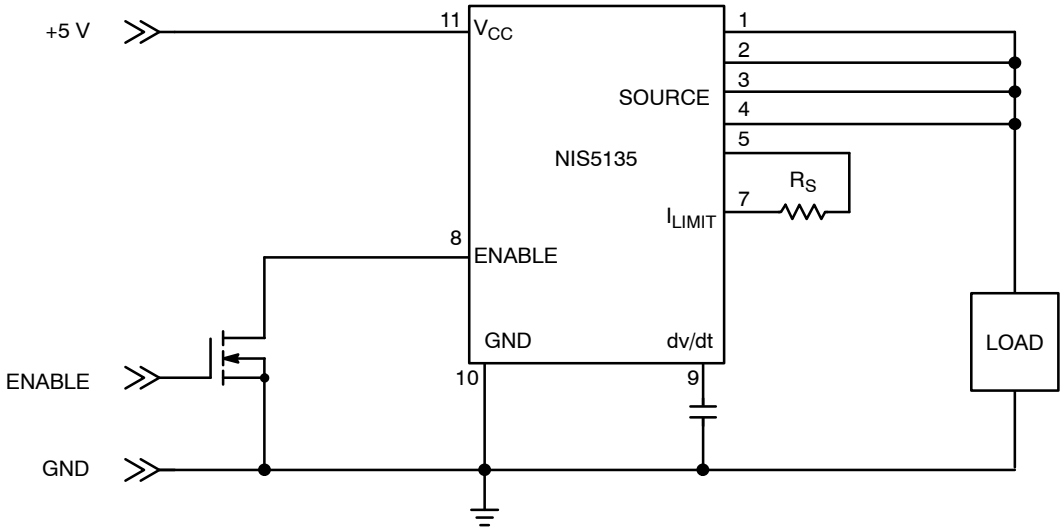


Figure 4. Application Circuit with Kelvin Current Sensing

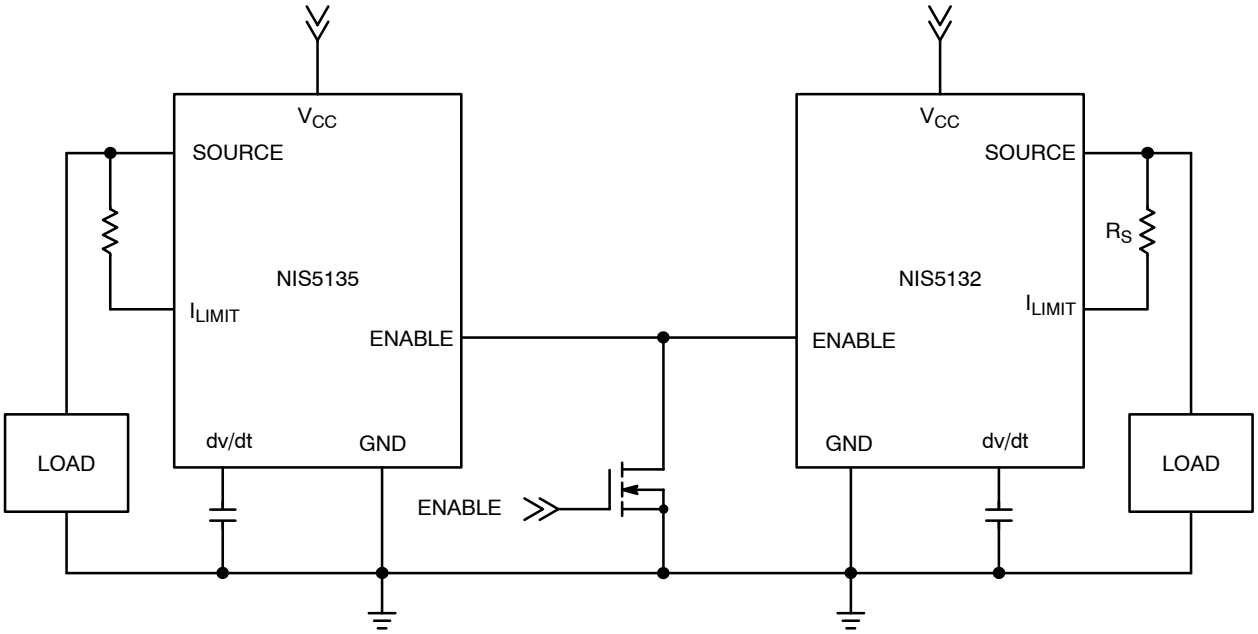


Figure 5. Common Thermal Shutdown

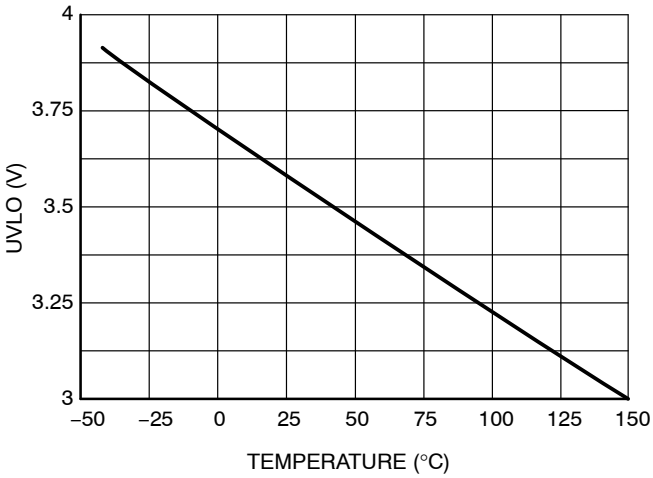


Figure 6. UVLO Turn−On

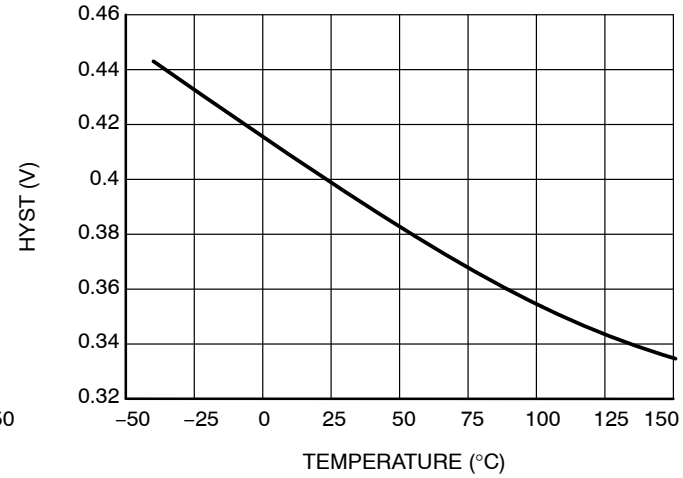


Figure 7. UVLO Hysteresis

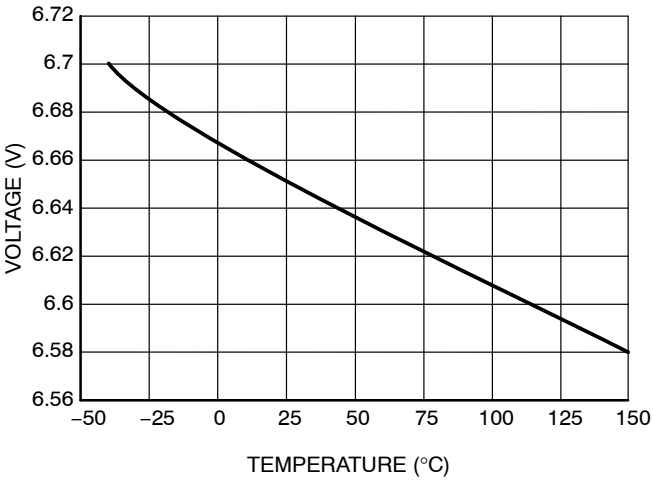


Figure 8. Output Clamping Voltage

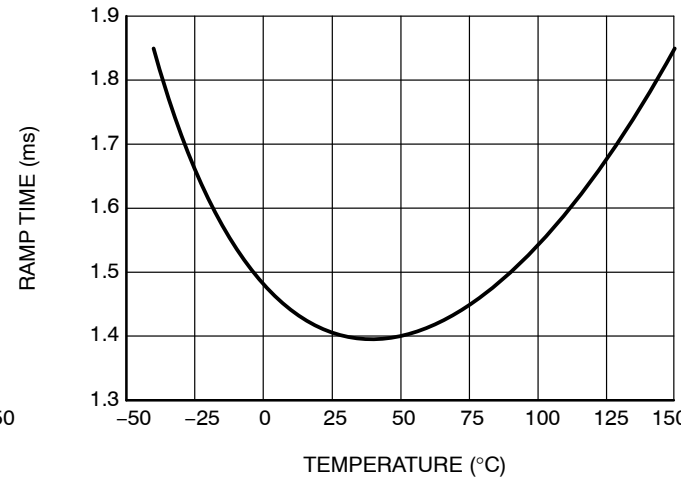


Figure 9. Output Voltage dv/dt Rate

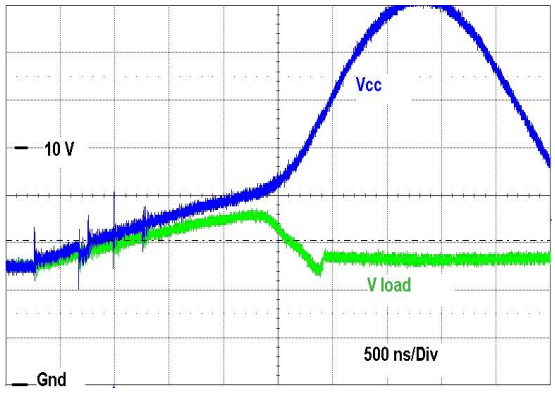


Figure 10. Input Transient Response

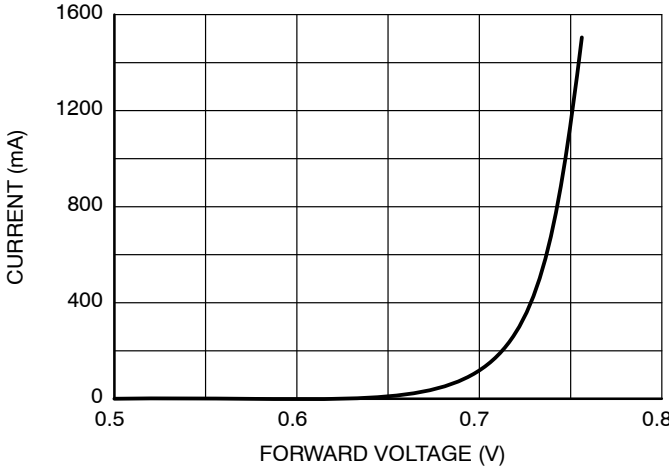


Figure 11. Body Diode Forward Characteristics

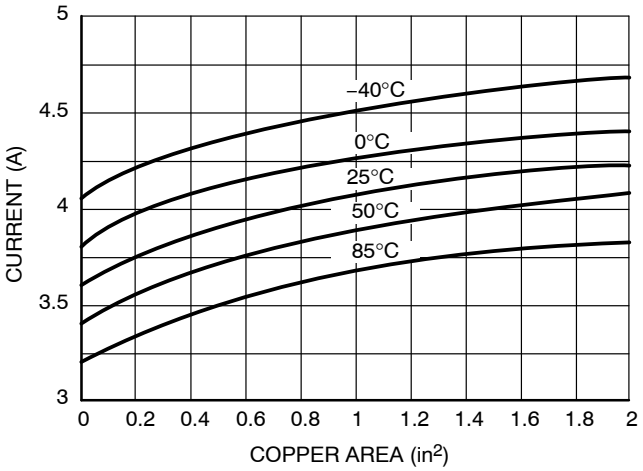


Figure 12. Thermal Limit vs. Copper Area and Ambient Temperature

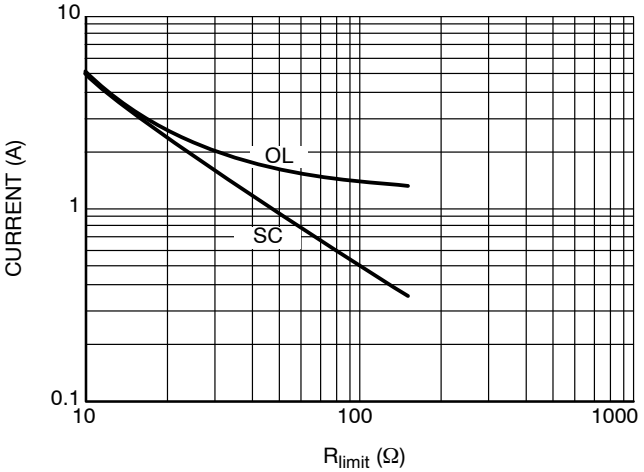


Figure 13. Current Limit vs. R_{sense} for Direct Current Sensing

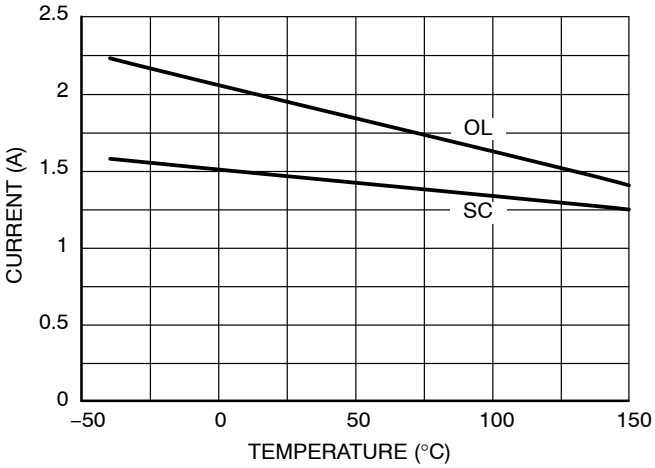


Figure 14. Direct Current Sensing Levels vs. Temperature for 33 Ω Sense Resistor

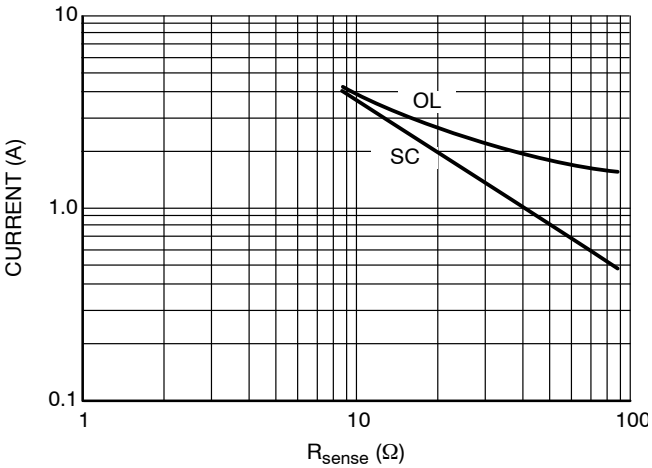


Figure 15. Current Limit vs. R_{sense} for Kelvin Current Sensing

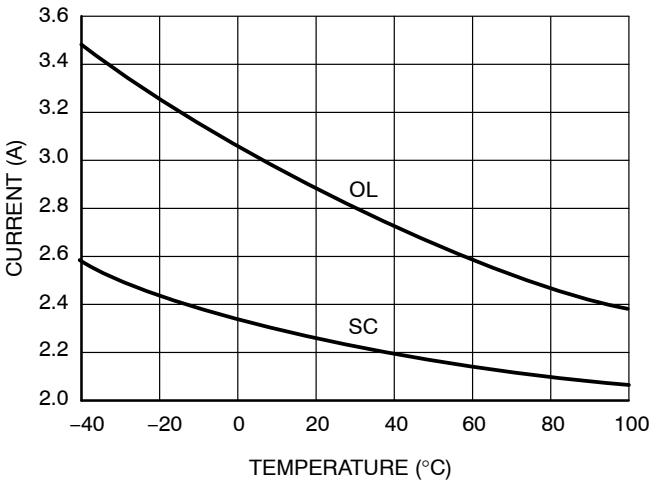


Figure 16. Kelvin Current Sensing Levels vs. Temperature for 18 Ω Sense Resistor

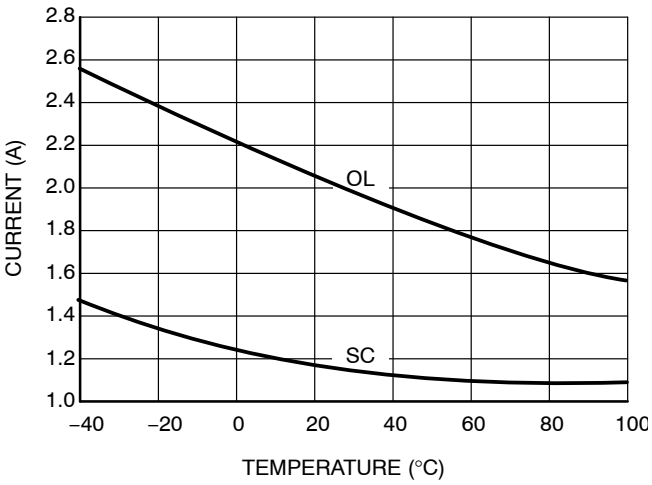


Figure 17. Kelvin Current Sensing Levels vs. Temperature for 39 Ω Sense Resistor

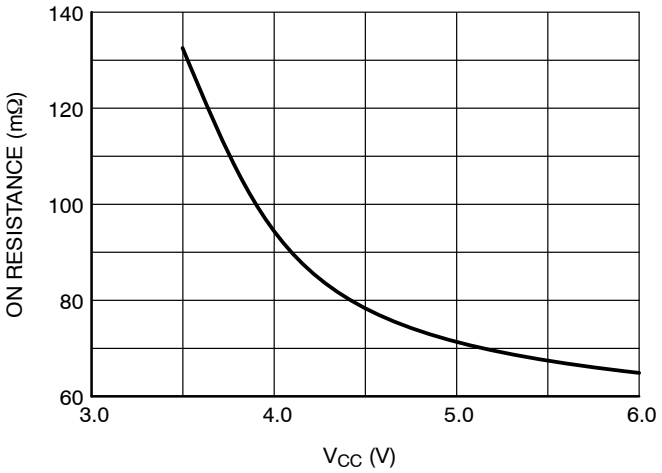


Figure 18. On Resistance vs. V_{CC}

APPLICATION INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dv/dt of the output voltage will be controlled by the internal dv/dt circuit. The output voltage will slew from 0 V to the rated output voltage in 2 ms, unless additional capacitance is added to the dv/dt pin.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage to 6.65 V in the event that the input exceeds that level.

An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

Current Limit

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor as well as increasing the value and decreasing the power rating of the sense resistor. Sense resistors are typically in the tens of ohms range with power ratings of several milliwatts making them very inexpensive chip resistors.

The current limit circuit has two limiting values, one for overload events which are defined as the mode of operation in which the gate is high and the FET is fully enhanced. The short circuit mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level. For a more detailed description of this circuit please refer to application note AND8140.

There are two methods of biasing the current limit circuit for this device. They are shown in the two application figures. Direct current sensing connects the sense resistor between the current limit pin and the load. This method includes the bond wire resistance in the current limit circuit. This resistance has an impact on the current limit levels for a given resistor and may vary slightly depending on the impedance between the sense resistor and the source pins. The on resistance of the device will be slightly lower in this configuration since all five source pins are connected in parallel and therefore, the effective bond wire resistance is one fifth of the resistance for any given pin.

The other method is Kelvin sensing. This method uses one of the source pins as the connection for the current sense resistor. This connection senses the voltage on the die and therefore any bond wire resistance and external impedance on the board have no effect on the current limit levels. In this configuration the on resistance is slightly increased relative to the direct sense method since only for of the source pins are used for power.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds 6.65 V, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

dv/dt Circuit

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 2 ms. This can be modified by adding an external capacitor at the dv/dt pin. This pin includes an internal current source of approximately 85 nA. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

The ramp time from 0 to the nominal output voltage can be determined by the following equation, where *t* is in seconds:

$$t_{0-5} = 30e6 \cdot (50\ pF + C_{ext})$$

$$C_{ext} = \frac{t_{0-5}}{30e6} - 50\ pF$$

Where:
C is in Farads
t is in Seconds

Any time that the unit shuts down due to a fault, enable shut−down, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on.

Enable/Fault

The Enable/Fault Pin is a multi−function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned−on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit.

To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri−state operation, it should not be connected to any type of logic with an internal pullup device.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family (NIS5132 or NIS5135), a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto−retry devices.

For the latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled. For the auto retry devices, both devices will restart as soon as the die temperature of the device in shutdown has been reduced to the lower thermal limit. The thermal options are listed in the ordering table.

Thermal Protection

The NIS5135 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin. Power will automatically be reapplied to the load for auto−retry devices once the die temperature has been reduced by 45°C.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C for extended periods of time.

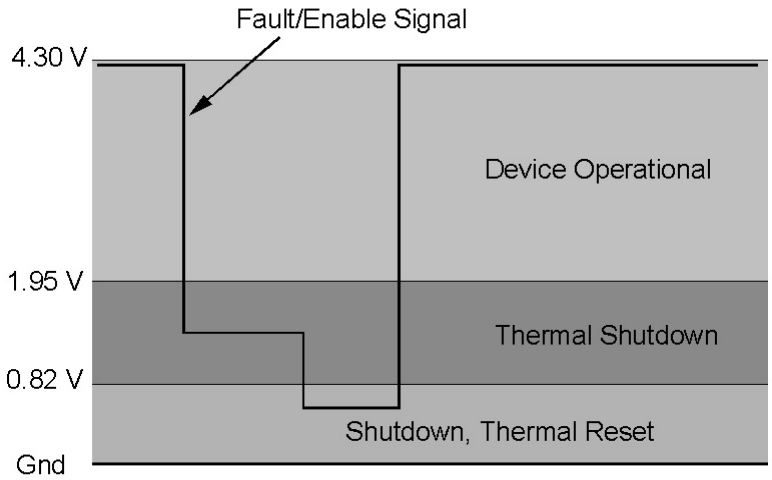


Figure 19. Enable/Fault Signal Levels

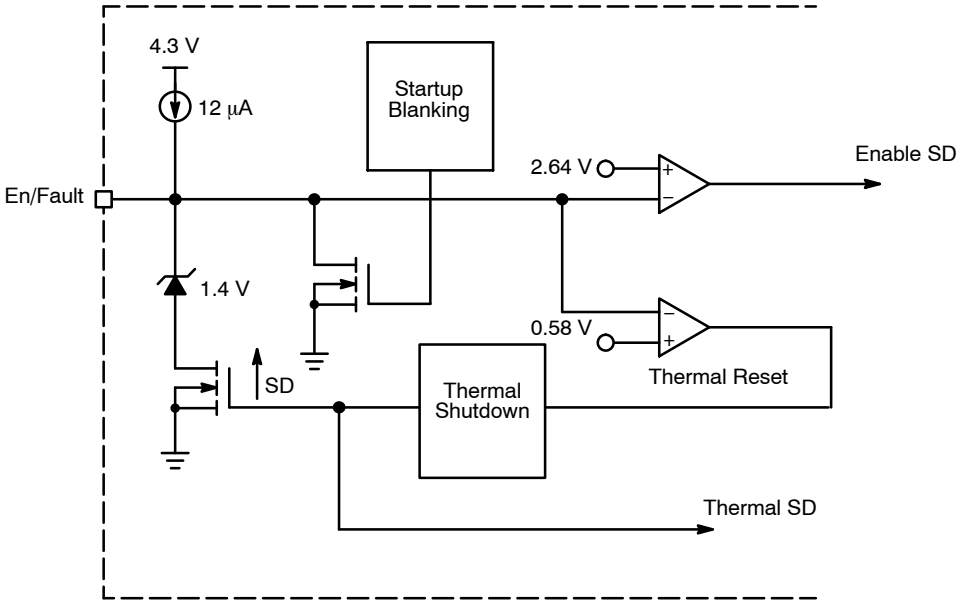


Figure 20. Enable/Fault Simplified Circuit

ORDERING INFORMATION

Device	Features	Package	Shipping†
NIS5135MN1TXG (Note 8)	Thermal Latching	DFN10 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 8)
NIS5135MN2TXG (Note 8)	Thermal Auto−Retry	DFN10 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 8)

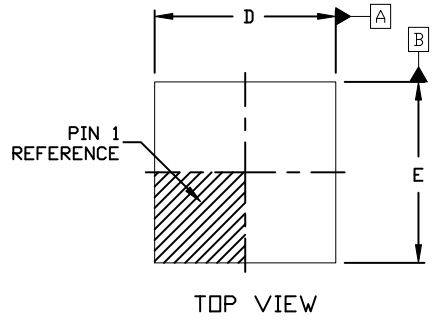
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. Products processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.

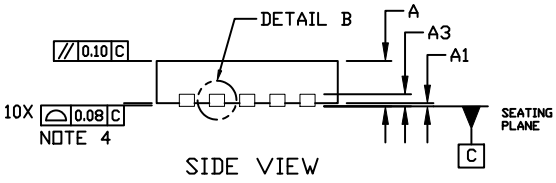
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

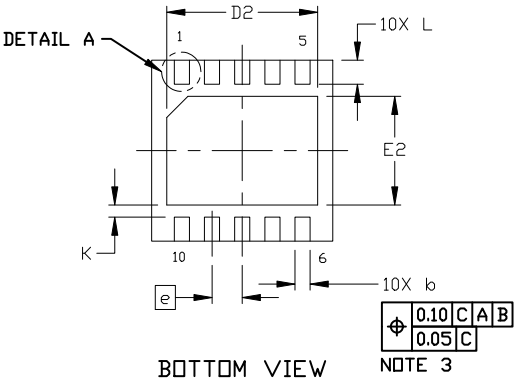
SCALE 2:1



TOP VIEW

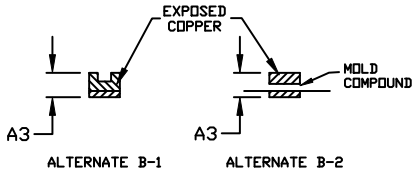


SIDE VIEW

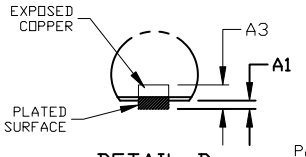


BOTTOM VIEW

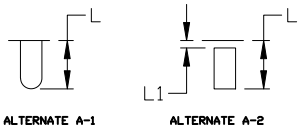
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

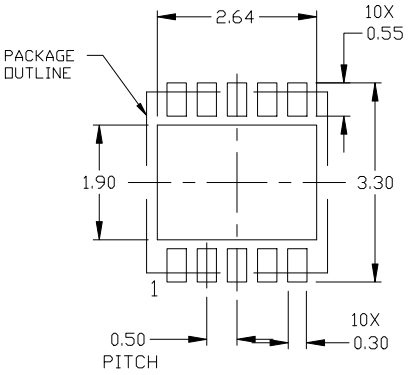


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

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