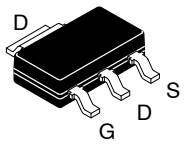
P-Channel Enhancement Mode Field Effect Transistor

NDT2955



SOT−223
CASE 318H−01

General Description

This 60 V P−Channel MOSFET is produced using **onsemi**'s high voltage Trench process. It has been optimized for power management plications.

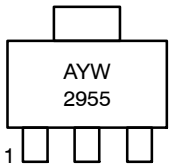
Features

- −2.5 A, −60 V
  - $R_{DS(ON)}$ = 300 mΩ @ V_{GS} = −10 V
  - $R_{DS(ON)}$ = 500 mΩ @ V_{GS} = −4.5 V
- High Density Cell Design for Extremely Low $R_{DS(ON)}$.
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- This is a Pb−Free Device

Applications

- DC/DC Converter
- Power Management

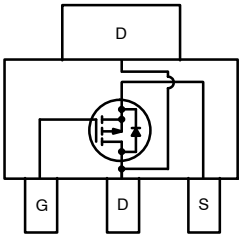
MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
2955 = Specific Device Code

(Note: Microdot may be in either location)

PINOUT DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−Source Voltage	−60	V
V_{GSS}	Gate−Source Voltage	±20	V
I_D	Drain Current − Continuous (Note 1a)	−2.5	A
	− Pulsed	−15	
P_D	Maximum Power Dissipation (Note 1a)	3.0	W
	(Note 1b)	1.3	
	(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	12	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
NDT2955	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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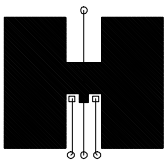
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AVALANCHE RATINGS						
W_{DSS}	Drain–Source Avalanche Energy	Single Pulse, V_{DD} = 30 V, I_D = 2.5 A	–	–	174	mJ
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	–60	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –60 V, V_{GS} = 0 V	–	–	–10	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = –20 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V, V_{DS} = 0 V	–	–	–100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–2	–2.6	–4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	5.7	–	mV/°C
$R_{DS(ON)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –2.5 A	–	95	300	mΩ
		V_{GS} = –4.5 V, I_D = –2 A	–	163	500	
		V_{GS} = –10 V, I_D = –2.5 A, T_J = 125°C	–	153	513	
$I_{D(ON)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–12	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –2.5 A	–	5.5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –30 V, V_{GS} = 0 V, f = 1.0 MHz	–	601	–	pF
C_{oss}	Output Capacitance		–	85	–	pF
C_{rss}	Reverse Transfer Capacitance		–	35	–	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn – On Delay Time	V_{DD} = –30 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω	–	12	21	ns
t_r	Turn – On Rise Time		–	10	20	ns
$t_{d(off)}$	Turn – Off Delay Time		–	19	34	ns
t_f	Turn – Off Fall Time		–	6	12	ns
Q_g	Total Gate Charge	V_{DS} = –30 V, I_D = –2.5 A, V_{GS} = –10 V	–	11	15	nC
Q_{gs}	Gate–Source Charge		–	2.4	–	nC
Q_{gd}	Gate–Drain Charge		–	2.7	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–2.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –2.5 A (Note 2)	–	–0.8	–1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = –2.5 A, d_{iF}/d_t = 100 A/μs	–	25	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	40	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

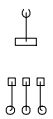
1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 95°C/W when mounted on a 0.066 in^2 pad of 2 oz copper.



c. 110°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

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TYPICAL CHARACTERISTICS

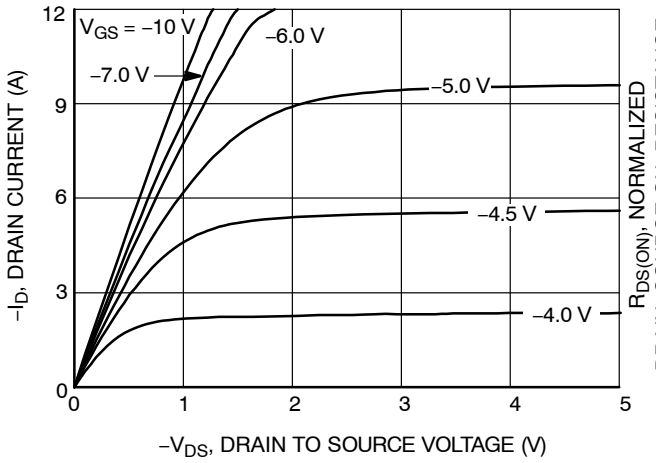

Figure 1. On−Region Characteristics

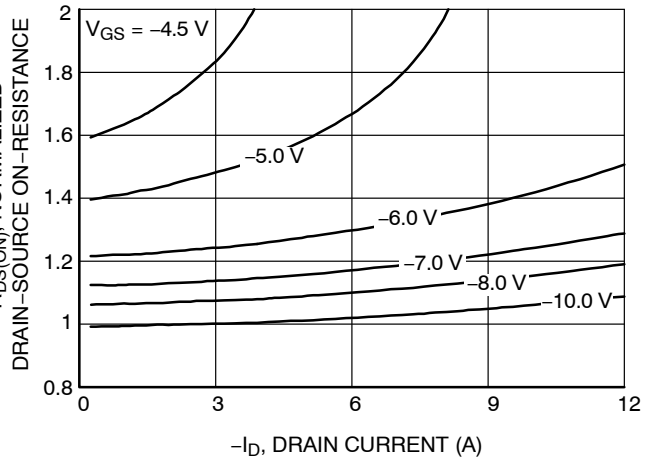

Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

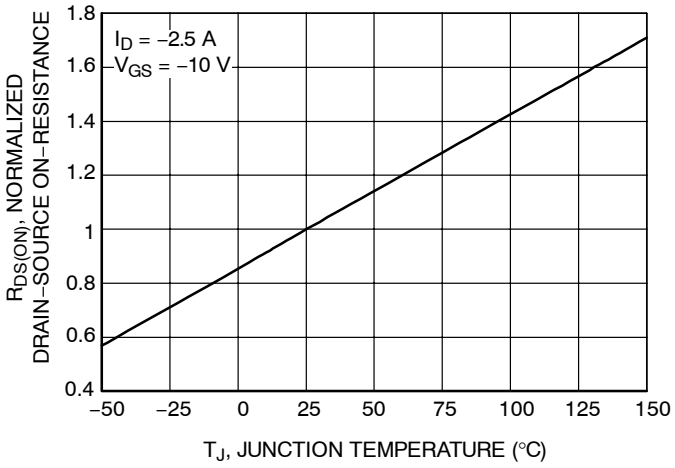

Figure 3. On−Resistance Variation with Temperature

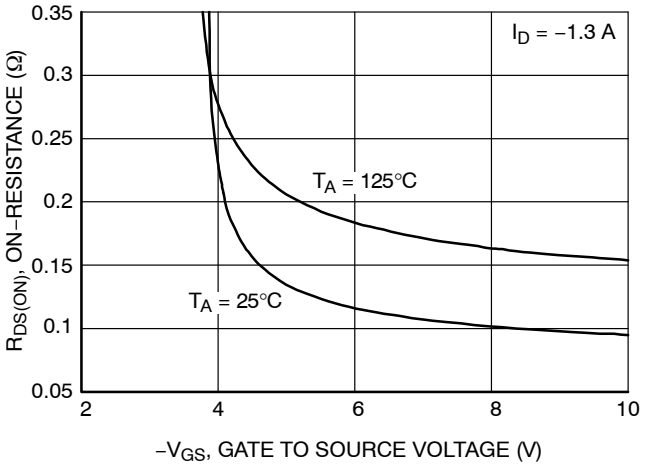

Figure 4. On−Resistance Variation with Gate−to−Source Voltage

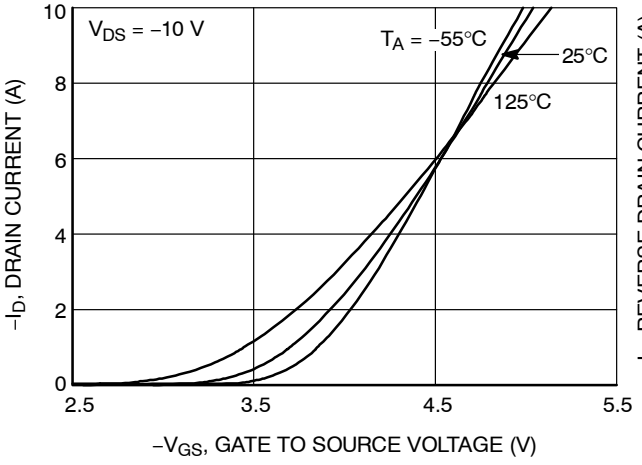

Figure 5. Transfer Characteristics

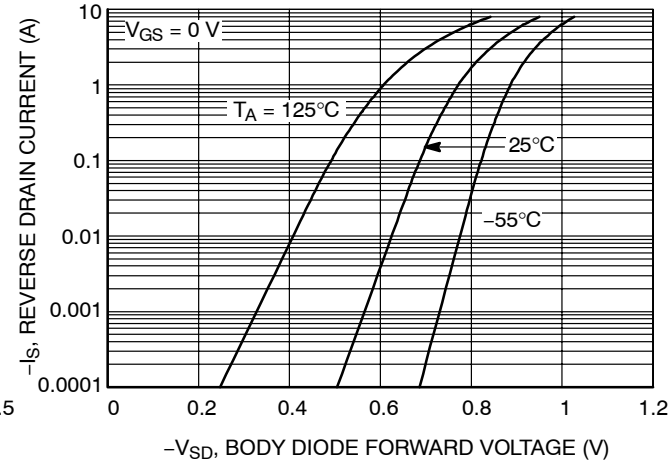

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

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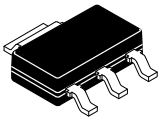
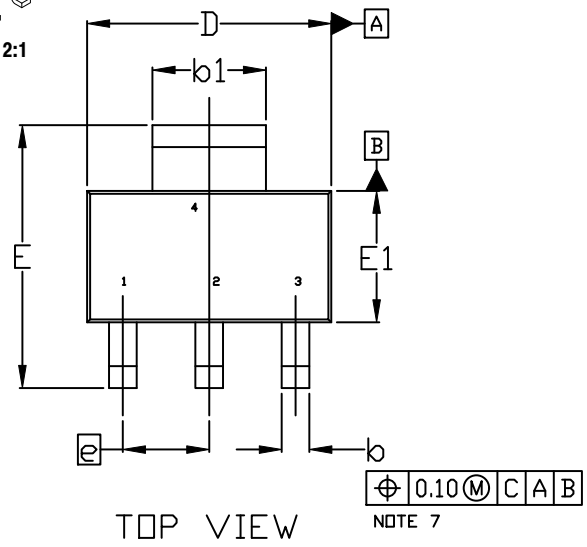
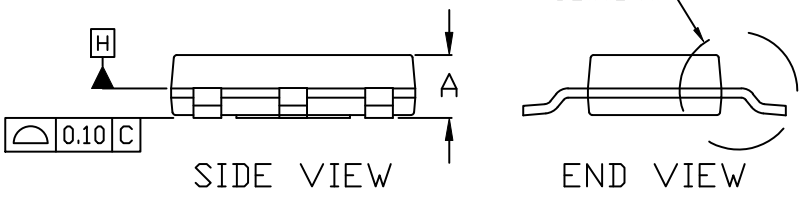


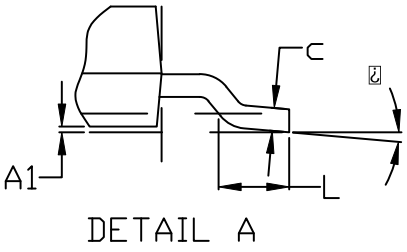
SCALE 2:1

SOT−223
CASE 318H
ISSUE B

DATE 13 MAY 2020

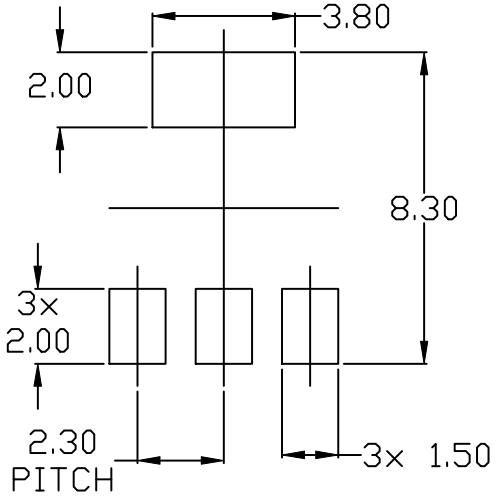






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

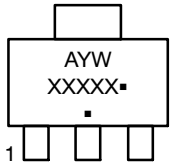
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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