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NCP81178

Secondary Synchronous Rectifier Driver for Forward Converters

The NCP81178 is a secondary−side synchronous rectifier driver designed for isolated power converters, especially actively clamped forward and fly−back, and asymmetric half−bridge converters. The NCP81178 drives two N−channel MOSFETs on the secondary side in a complementary manner. It accepts a PWM input signal derived from the secondary winding or an auxiliary winding on the main power transformer. It can also take a PWM signal from the primary−side controller through a pulse transformer or other isolators.

Features

- N−Channel Synchronous Rectifier MOSFET Driver
- PWM Input Derived from a Winding on the Main Transformer or Directly from a Pulse Transformer
- Internally Generated PWM Threshold Voltage that can be Programmed Externally
- Pre−bias Startup Capability
- Primary Shutdown Detection
- Frequency Detection Window
- Wide VIN/VCC Range: 4.5 V to 14 V
- 6 V/150 mA LDO for VCC Supply
- 4.5 A/3.8 A Sink and 3 A Source Drive Capability
- 12 ns PWM Propagation Time
- 12 ns Rise Time/10 ns Fall Time at C_L = 4700 pF @ V_{CC} = 6 V
- VCC under−voltage lockout
- Will support converter output voltages as high as 28 V
- Pb−Free 10−pin DFN 3 mm x 3 mm Package
- This is a Pb−Free Device

Typical Applications

- High−Efficiency Isolated DC/DC Power Supplies
- Server Power, 48 V Telecom and Data−com Applications

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DFN10
MN SUFFIX
CASE 506AA

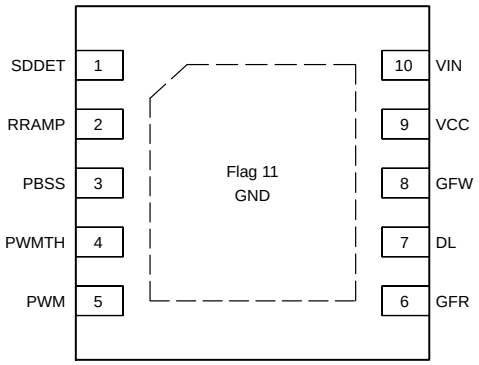
MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81178MNTXG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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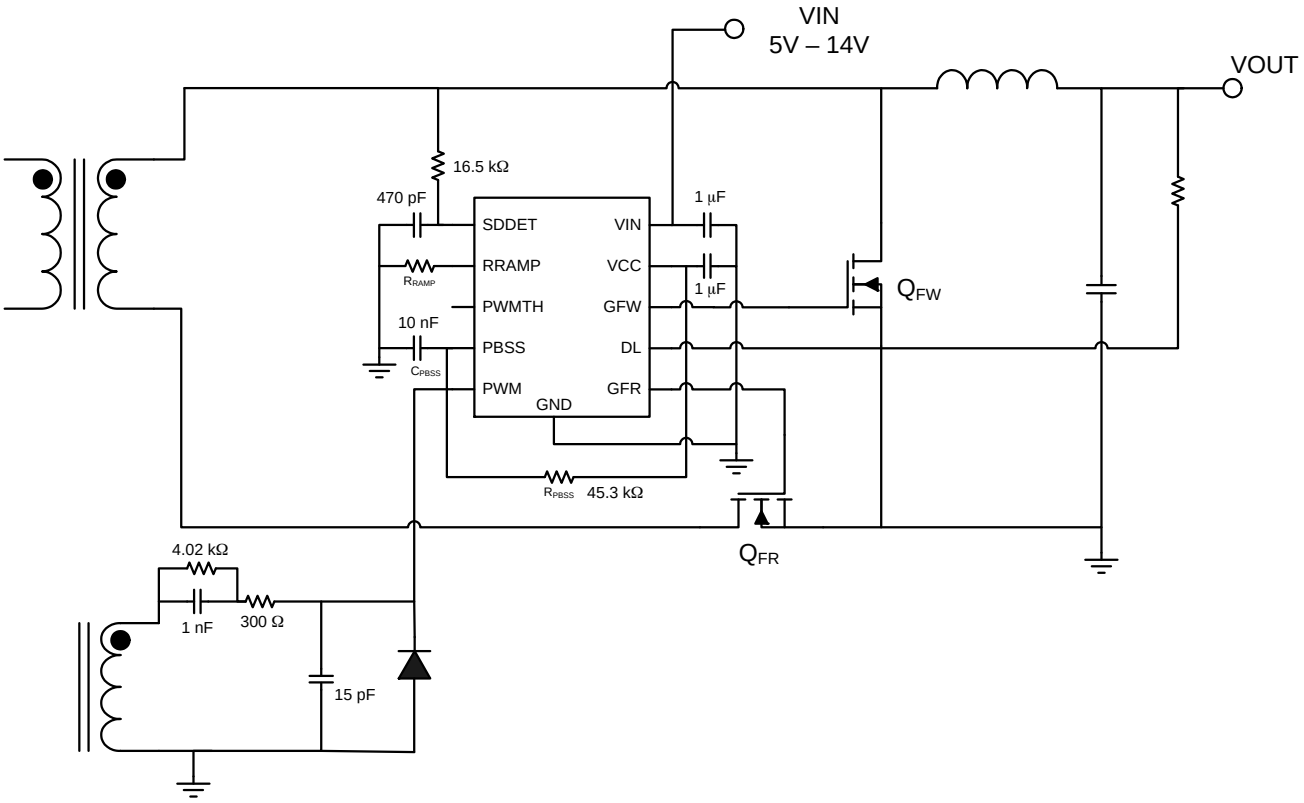


Figure 1. Typical Application Circuit − Secondary Synchronous Rectifier Driver

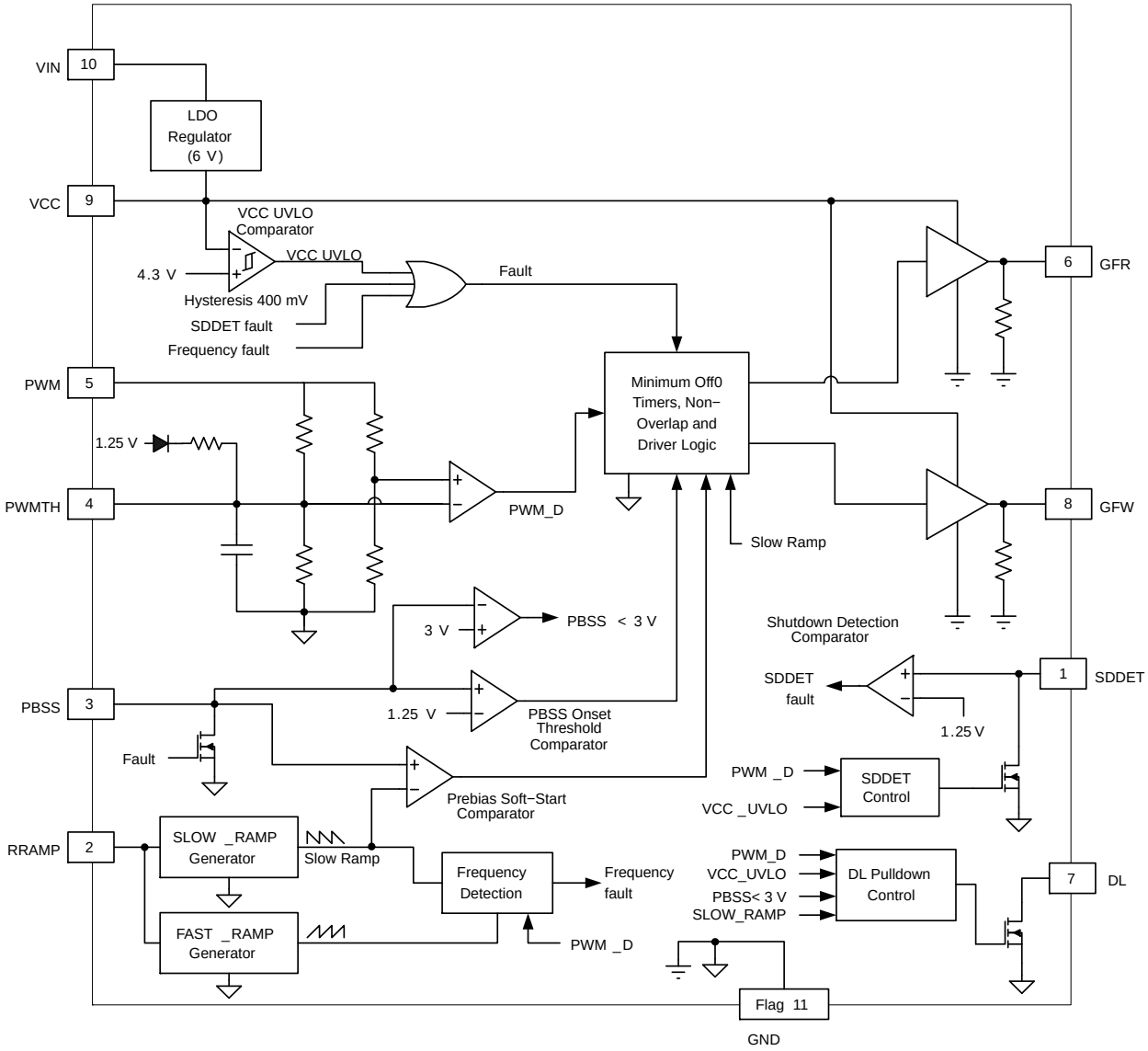


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	SDDET	Primary shutdown detection. When the voltage on this pin exceeds the shutdown threshold, the driver shuts down. If valid PWM pulses resume and VCC is above UVLO threshold, the driver will go through a restart process.
2	RRAMP	Ramp slope setting for the ramp used in pre−bias start control. This pin also sets the upper and lower boundaries of the frequency detection window. Connect a resistor from this pin to GND (see Application Information section for selecting resistor values).
3	PBSS	Pre−bias startup ramp voltage setting pin. Pulling PBSS voltage below the PBSS onset threshold voltage disables both gate drives.
4	PWMTH	PWM threshold voltage.
5	PWM	PWM input
6	GFR	Forward rectifier gate drive
7	DL	Dummy Load function. Discharges the output voltage during startup. To use this function, connect a resistor from this pin to the output voltage.
8	GFW	Freewheeling rectifier gate drive
9	VCC	LDO output. A ceramic capacitor within the range of 0.1 μF and 4.7 μF must be placed between this pin and ground.
10	VIN	LDO input
11	GND	Ground.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Min	Max	Unit
LDO Voltage Range	VCC, VIN	−0.3	16	V
Gate Drive Output Voltage Range (DC)	GFR, GFW	−0.3	16	V
Gate Drive Output Voltage Range (Transient, 100 ns)	GFR, GFW	−5		V
SDDET Input	SDDET	−0.3	32	V
DL Input (DC)	DL	−0.3	32	V
DL Input (Transient, 200 ns)	DL	−1		V
PWM Input	PWM	−1	30	V
PWMTH Input	PWMTH	−1	3	V
PBSS	PBSS	−0.3	VCC + 0.3	V
RRAMP Input	RRAMP	−0.3	3	V
Maximum Junction Temperature	$T_{J(max)}$	−55	150	°C
Storage Temperature Range	TSTG	−65	150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2		kV
Moisture Sensitivity Level	MSL	1		−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}		260 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

THERMAL CHARACTERISTICS (Note 4)

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN10, 3x3 mm (Note 5) Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case	 $R_{\theta JA}$ $R_{\theta JC}$	 55 7.5	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 6)

Rating	Symbol	Min	Typ	Max	Unit
Switching Frequency	Fsw	100		1200	kHz
LDO Input Voltage (Note 7)	VIN	5		14	V
External Supplied DC Source (No DC source on VIN)	VCC	4.5		14	V
External LDO output capacitance	C_{VCC}	0.22	1	4.7	uF
PWM Low	PWM_LO	−0.3		1	V
PWM High	PWM_HI	4		26	V
SDDET & DL	SDDET, DL			30	V
Junction Temperature	T_J	−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
7. LDO Input Voltage must be greater than or equal to 7 V to ensure performance specified in Table 5. Electrical Characteristics.

ELECTRICAL CHARACTERISTICS V_{CC} = 6 V, F_{sw} = 100 kHz to 1.2 MHz, for typical values T_A = 25°C, for min/max values T_A = −40°C to 125°C; unless otherwise noted. (Notes 8, 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LDO AND UVLO						
VCC Voltage Regulation	VIN = 7 V − 14 V, I_{VCC} = 0−150 mA		5.7	6.0	6.3	V
VCC Current Limit			150			mA
VCC UVLO	Positive−going VCC		4.1	4.3	4.5	V
VCC UVLO Hysteresis				400		mV
SHUTDOWN DETECTION (SDDET)						
SDDET Rising Threshold		SDDET_th	1.22	1.26	1.30	V
Internal Discharge Transistor RDS(on)					115	Ω
PWM THRESHOLD (PWMTH)						
PWMTH Rising Hysteresis (Note 11)				50		mV
PWMTH Falling Hysteresis (Note 11)				50		mV
PWM THRESHOLD (PWMTH2)						
PWMTH2 Rising			2.4	3.0	3.6	V
PWMTH2 Hysteresis				1.0		V
PBSS THRESHOLD						
PBSS_onset_th	When GFR and GFW are enabled		1.21	1.25	1.28	V
Internal Discharge Transistor $R_{DS(on)}$					100	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. Refer to the APPLICATION INFORMATION section.
9. Values based on design and/or characterization.
10. 4.7nF driver load capacitance
11. Guaranteed by design and/or characterization. Not production tested.
12. Frequency blanking applied to first valid rising and falling edges of PWM per switching cycle.

ELECTRICAL CHARACTERISTICS V_{CC} = 6 V, F_{sw} = 100 kHz to 1.2 MHz, for typical values T_A = 25°C, for min/max values T_A = −40°C to 125°C; unless otherwise noted. (Notes 8, 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PBSS THRESHOLD						
PBSS Discharge Threshold				200		mV
SLOW_RAMP THRESHOLDS						
Ceiling Threshold Voltage		FRMP_H	3.4	3.5	3.6	V
Bottom Threshold Voltage (Note 11)		FRMP_L	0.46	0.5	0.54	V
FREQUENCY DETECTION WINDOW						
Lower Boundary to Upper Boundary Ratio	RRAMP = 130 kΩ		0.50	0.56	0.62	
Lower Frequency Limit 1	RRAMP = 619 kΩ (100 kHz nominal frequency) (Note 10)		63	70	77	kHz
Upper Frequency Limit 1			117	130	143	kHz
Blanking Time 1 (Note 12)			348	450	552	ns
Lower Frequency Limit 2	RRAMP = 130 kΩ (450 kHz nominal frequency)		284	315	347	kHz
Upper Frequency Limit 2			527	586	645	kHz
Blanking Time 2 (Note 12)			140	200	260	ns
Lower Frequency Limit 3	RRAMP = 47.5 kΩ (1.2 MHz nominal frequency) (Note 11)		756	840	924	kHz
Upper Frequency Limit 3			1404	1560	1716	kHz
Blanking Time 3 (Note 12)			77	100	123	ns
DUMMY LOAD						
Internal Discharge Transistor $R_{DS(on)}$				10	20	Ω
Sink Current Capability	DL = 3 V, T_A = 25°C		0.3			A
DL Disabling PBSS Threshold Voltage		PBSSth2		3.0		V
Number of Ramp Cycles to keep DL On	For each detected PWM pulse			128		Cycles
GATE DRIVER GFR						
GFR Peak Sink Current (Note 11)	GFR = 3 V, V_{CC} = 6 V		3.8			A
GFR Peak Source Current (Note 11)	GFR = 3 V, V_{CC} = 6 V		3			A
GFR Sink Resistance	V_{CC} = 6 V, sink current = 200 mA				0.91	Ω
GFR Source Resistance	V_{CC} = 6 V, source current = 200 mA				0.91	Ω
Rise Time (Note 11)	10% to 90%, Cgate = 4.7 nF, V_{CC} = 6 V			12		ns
Fall Time (Note 11)	90% to 10%, Cgate = 4.7 nF, V_{CC} = 6 V			10		ns
Minimum Off Time, Within PWM Falling Edge Blanking Window	Fsw = 100 kHz (Note 11)			300		ns
	Fsw = 450 kHz		110	150	195	ns
	Fsw = 1.2 MHz (Note 11)			75		ns
Minimum Off Time, Outside of PWM Falling Edge Blanking Window	(Note 11)			75		ns
GATE DRIVER GFW						
GFW Peak Sink Current (Note 11)	GFW = 3 V, V_{CC} = 6 V		4.5			A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Refer to the APPLICATION INFORMATION section.
9. Values based on design and/or characterization.
10. 4.7nF driver load capacitance
11. Guaranteed by design and/or characterization. Not production tested.
12. Frequency blanking applied to first valid rising and falling edges of PWM per switching cycle.

ELECTRICAL CHARACTERISTICS V_{CC} = 6 V, F_{sw} = 100 kHz to 1.2 MHz, for typical values T_A = 25°C, for min/max values T_A = −40°C to 125°C; unless otherwise noted. (Notes 8, 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
GATE DRIVER GFW						
GFW Peak Source Current (Note 11)	GFW = 3 V, V_{CC} = 6 V		3			A
GFW Sink Resistance	V_{CC} = 6 V, sink current = 200 mA				0.91	Ω
GFW Source Resistance	V_{CC} = 6 V, source current = 200 mA				0.91	Ω
Rise Time (Note 11)	10% to 90%, Cgate = 4.7 nF, V_{CC} = 6 V			12		ns
Fall Time (Note 11)	90% to 10%, Cgate = 4.7 nF, V_{CC} = 6 V			8		ns
Minimum Off Time, Within PWM Rising Edge Blanking Window (Note 11)	Fsw = 100 kHz (Note 11)			300		ns
	Fsw = 450 kHz		110	150	195	ns
	Fsw = 1.2 MHz (Note 11)			75		ns
Minimum Off Time, Outside of PWM Rising Edge Blanking Window	(Note 11)			75		ns
MINIMUM DEAD TIMES						
$t_{dt_GFWL_to_GFRH}$, delay time from GFW going low to GFR going high (Note 11)	90% of GFW to 10% of GFR		0	5	10	ns
$t_{dt_GFRL_to_GFWH}$, delay time from GFR going low to GFW going high (Note 11)	90% of GFR to 10% of GFW		0	5	10	ns
PROPAGATION DELAY TIMES						
$t_{pd_pwm_r}$, Propagation delay from PWM going high to GFW going low (Note 11)	PWM crossing PWMTH to GFW falling at 90%		0	12	22	ns
$t_{pd_pwm_f}$, Propagation time from PWM going low to GFR going low (Note 11)	PWM crossing 2 V to GFR falling at 90%		0	21	31	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Refer to the APPLICATION INFORMATION section.
9. Values based on design and/or characterization.
10. 4.7nF driver load capacitance
11. Guaranteed by design and/or characterization. Not production tested.
12. Frequency blanking applied to first valid rising and falling edges of PWM per switching cycle.

APPLICATION INFORMATION

NCP81178 is a secondary−side synchronous rectifier driver designed for isolated power converters, especially actively clamped forward converters. The NCP81178 drives two N−channel MOSFETs on the transformer secondary side in a complementary manner. It accepts a PWM input signal derived from the secondary winding or an auxiliary winding on the main power transformer. The NCP81178 can also operate with a PWM signal from the primary−side controller through a pulse transformer or other isolator.

The PWM threshold voltage on pin PWMTH is internally generated from the PWM input voltage and VCC voltage using a signal conditioning circuit. The PWMTH voltage is used as the PWM rising and falling thresholds. PWMTH is compared with the PWM input voltage to generate an internal PWM signal used to control the gate drive timings.

The NCP81178 driver implements a pre−bias startup feature that allows the converter to start into a pre−biased output voltage.

The NCP81178 implements a shutdown detection function to detect a primary shutdown. When the voltage on SDDET pin exceeds the shutdown threshold, the gate drives are turned off immediately and the NCP81178 will go through a restart process when V_{CC} is above UVLO threshold and valid PWM pulses resume.

The NCP81178 also includes a switching period/frequency window detection function. The detection window boundaries are set with a RRAMP resistor. When the detected switching frequency falls out of this window, the gate drives are turned off immediately and NCP81178 will go through a restart process when VCC is above UVLO threshold and valid PWM pulses resume.

The NCP81178 incorporates key protection features such as V_{CC} under voltage lockout. The PBSS pin can also be used to rapidly enable or disable the driver outputs from an external signal.

PWM Input

The PWM input to the NCP81178 can be transmitted from a primary PWM controller with a pulse transformer. The PWM signal can also be derived from a winding on the main isolation power transformer. In the latter case, a pulse transformer is not needed and the system cost can be reduced. Figure 3 shows a circuit example which uses a voltage shaping circuit to extract the PWM signal from an auxiliary winding on the main transformer.

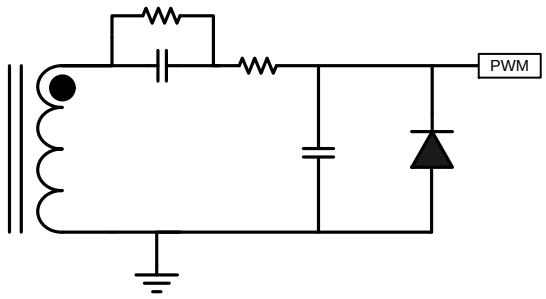


Figure 3. PWM Signal From An Auxiliary Winding

PWM Threshold and Gate Drive Logic

The PWM threshold voltage, PWMTH, is generated internally from the PWM input signal using a voltage conditioning circuit. Figure 4 shows the internal circuitry that generates the PWMTH threshold voltage from the PWM input. There is a resistor divider network that scales down the PWM signal by a 5:1 ratio. This circuit creates a PWM rising threshold at around 0.2 V (equivalent to 1 V without the 5:1 scale factor), while the PWM falling threshold is set to the PWMTH2 falling threshold of 2 V, typical. This approach enables the driver PWM circuit to detect the primary switching actions as early as possible, which is very important for achieving efficient and reliable synchronous rectification on the secondary. Secondly, the PWMTH waveform is kept away from the voltage ringing of the PWM input voltage. Thirdly, the bottom part (i.e. the PWM rising threshold) and the top part (i.e. the PWM falling threshold) of the PWMTH voltage closely follow the PWM input voltage even during extremely fast and large transients which may cause very large swings on PWM input voltage. This ensures the PWM detection logic is always valid for any operating conditions.

This internal PWMTH circuit is optimized to work up to 1.2 MHz switching frequency for a majority of the applications.

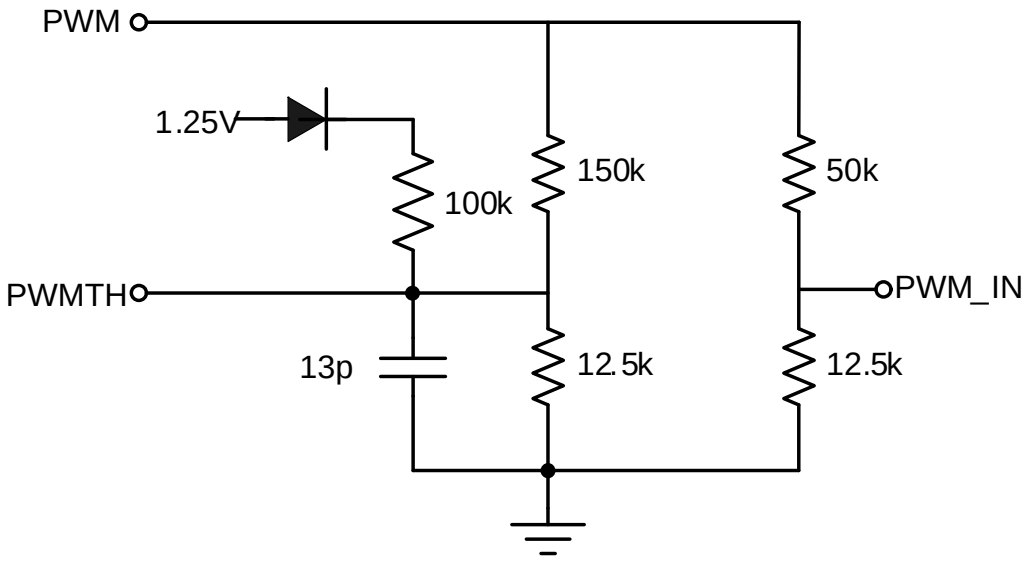


Figure 4. PWM And PWMTH Internal Circuitry

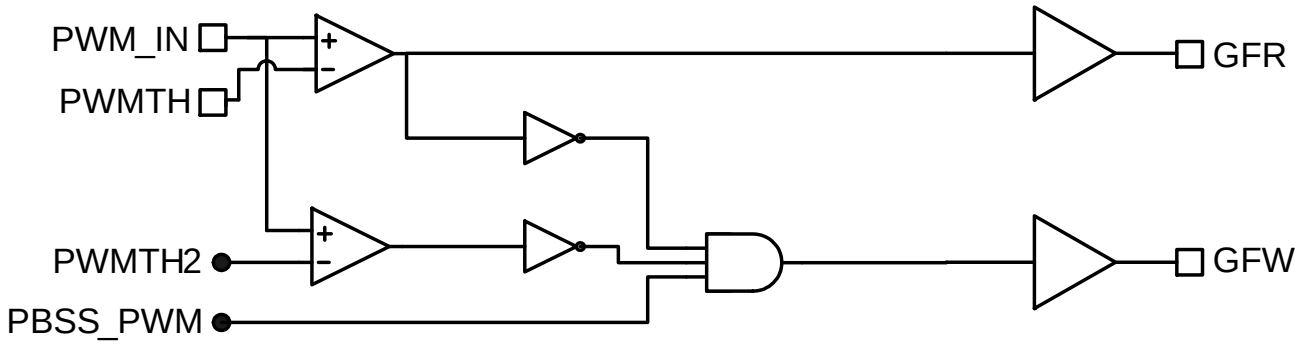


Figure 5. Simplified Driver Logic Block Diagram

As shown in Figure 5, by comparing the PWM input voltage with PWMTH, an internal PWM signal, PWM_D, is obtained to generate the gate drives. The forward rectifier gate drive (GFR) is directly in phase with PWM_D, while the freewheeling rectifier gate drive (GFW) is 180° out of phase with PWM_D and GFR. Refer to Figure 6 for circuit waveforms, PWM logic and gate drive timing diagrams.

To reduce the chance of the gate outputs falsely triggering a frequency fault due to ringing on the PWM signal, the NCP81178 uses blanking windows after there is a change in state of GFR and GFW. After a PWM_D rising edge, a blanking timer is initiated that prevents a frequency detection fault from being declared until the blanking timer expires. The duration of this blanking timer changes with the PWM switching frequency. A similar blanking timer is initiated during the PWM_D falling edge, whose duration timer is also dependent on the PWM switching frequency.

The NCP81178 uses minimum off timers on GFR and GFW, which restrict the shortest time GFR and GFW can be in the low state before changing to a high state. A short off pulse can result in a voltage spike at the pins of GFR and GFW, the magnitude of which depends on the trace inductance between the driver outputs and the gate of the MOSFETs. The minimum off timers help to prevent a voltage spike that can be large enough to damage the output devices on GFR and GFW. The duration of the minimum off timers depends on whether the NCP81178 is in one of the aforementioned blanking timers. When within the blanking timer, the duration of the minimum off timer changes with the PWM switching frequency. At a switching frequency of 100 kHz the typical minimum off timer is 300 ns, while at 1.2 MHz the typical minimum off timer is 75 ns. When outside of the blanking timers, the duration of the minimum off timer is fixed at a typical 75 ns, and does not change with the PWM switching frequency.

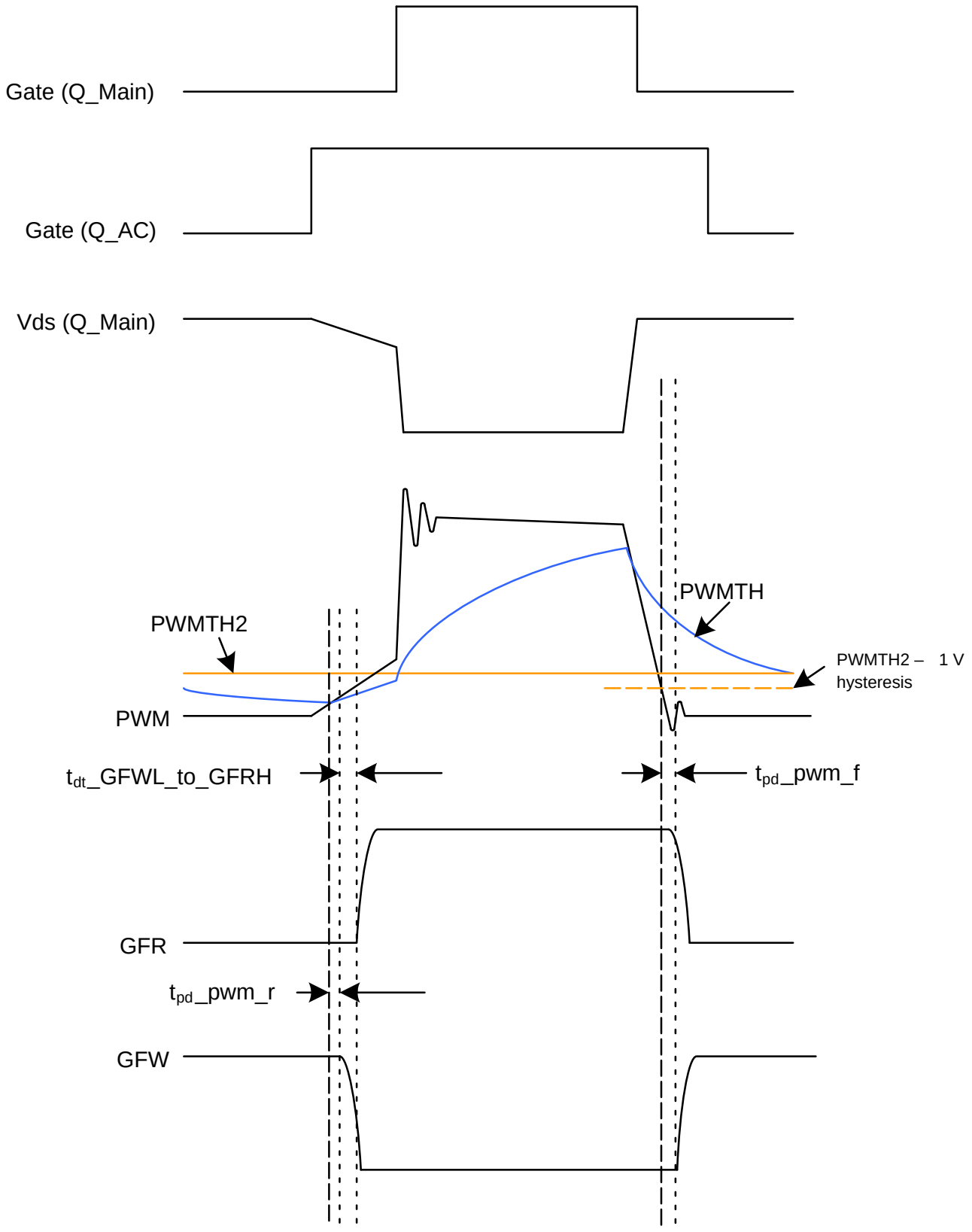


Figure 6. Gate Drive Timing Diagram

Shutdown Detection (SDDET)

The Shutdown Detection function allows the primary−side controller to send a shutdown signal to the secondary−side driver. As shown in the Typical Application Circuit in Figure 1, the SDDET pin is used to detect an increase in volt−seconds in the main transformer. An RC ramp circuit is connected from SDDET to the freewheeling rectifier drain, DFW, or to an auxiliary winding on the main transformer. When the voltage on SDDET exceeds the shutdown detection threshold voltage, GFR and GFW are immediately pulled low and PBSS is discharged. When valid PWM pulses resume and V_{CC} is above UVLO, the NCP81178 will go through a restart process. This is a non−latching shutdown. Using the Shutdown Detection function ensures both gate drives to turn off when there is positive current through the output inductor. Turning off both gate drives when there is negative current through the freewheeling FET could result in excessive voltage transients across the freewheeling FET.

Pre−bias Startup

The NCP81178 implements a pre−bias startup function. A RC circuit (R_{PBSS} and C_{PBSS}) connected to the PBSS pin sets the pre−bias startup ramp voltage to define the transition process from diode rectification mode to synchronous rectification mode. During pre−bias startup, C_{PBSS} is charged by resistor R_{PBSS}, connected from V_{CC} to PBSS.

Initially, when V_{CC} reaches UVLO and the NCP81178 is activated, the PBSS voltage is first discharged and then starts to charge up. When the PBSS voltage is lower than the PBSS onset threshold voltage (PBSS_onset_th), both gate drives are pulled low. Once the PBSS voltage rises above PBSS_onset_th, the GFR output follows the PWM input while at the same time the pre−bias process is initiated and the gate drive pulse width of the freewheeling gate drive gradually increases from 0 to its final steady state value until the secondary rectifier fully enters synchronous rectification mode.

A resistor connected from RRAMP to ground sets the discharge ramp slope for a ramp voltage within the NCP81178. This discharge ramp (SLOW_RAMP) together with the PBSS ramp sets the GFW pulse width in the pre−bias startup transition process. In the pre−bias startup process the rising edge of the GFW pulse gradually expands backward until it meets the falling edge of the GFR pulse. Pulling the PBSS voltage below the PBSS_onset_th voltage disables both gate drives. Refer to Figure 7 for the key timing waveforms for pre−bias start.

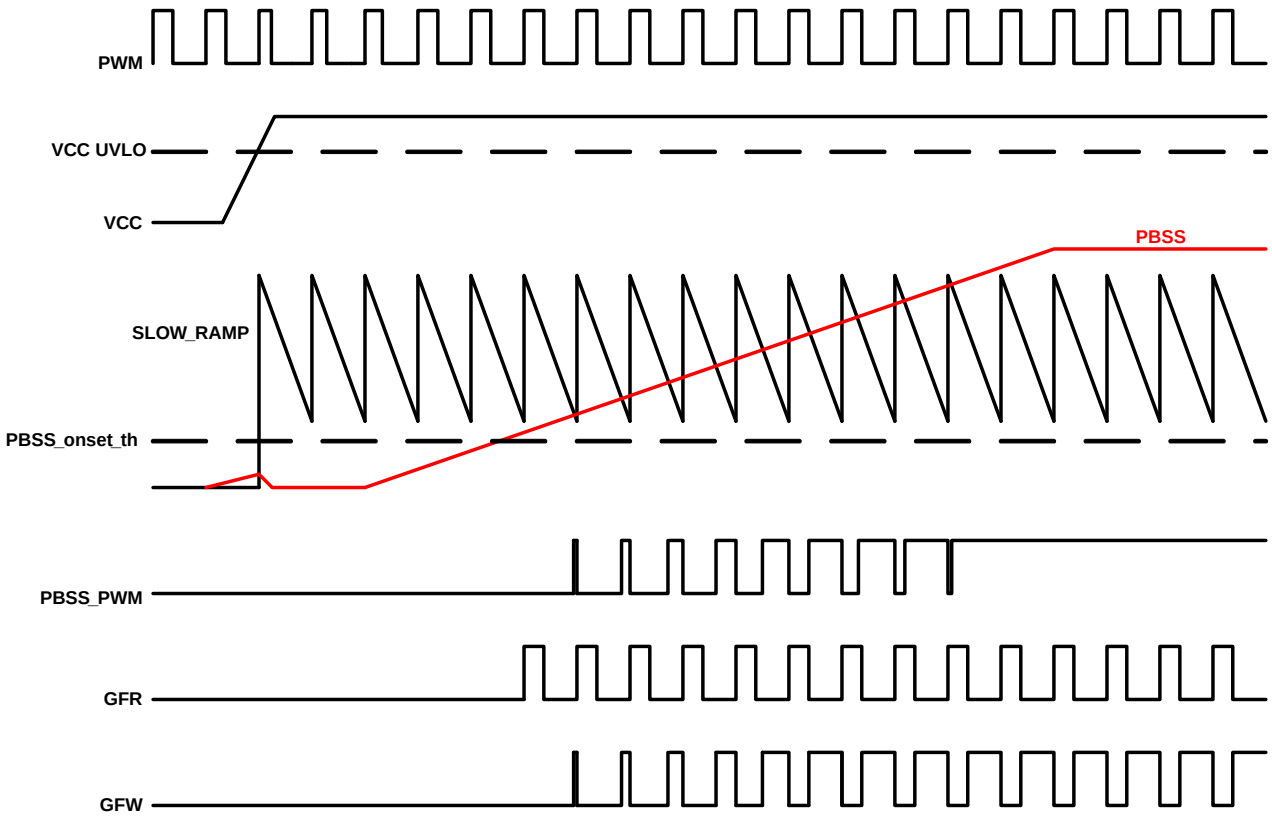


Figure 7. Key Waveforms And Timings For Pre−Bias Start

Switching Period/Frequency Detection

The NCP81178 uses internally−generated ramps to determine if the detected switching frequency differs from the expected switching frequency. The expected switching frequency is programmed by the value of the RRAMP resistor. The RRAMP value set the slopes of both SLOW_RAMP and FAST_RAMP. SLOW_RAMP, see Figure 9, is used to determine if the switching period is longer than 1.3 times the nominal period, while FAST_RAMP, see Figure 10, is used to determine if the switching period is less than 0.7 times the nominal period. If the period is determined to be either greater than 1.3 times or less than 0.7 times the nominal period, a frequency fault will be declared, disabling both gate drives and discharging PBSS. The driver will go through a restart when valid PWM pulses are received and VCC is above UVLO. Figure 8 shows the regions where a frequency fault will occur.

To prevent ringing on PWM from triggering a false frequency fault, the NCP81178 uses blanking windows at the rising and falling edges of PWM. The blanking windows start at the rising and falling edge of the internally−derived PWM signal (PWM_D), and its duration is dependent on the switching frequency set by RRAMP. At a switching frequency of 100 kHz the blanking timer is 450 ns, while at 1.2 MHz the blanking timer is 100 ns. When within a blanking window, GFR and GFW respond normally to PWM_D, but a frequency fault will not be declared regardless of how close together two PWM_D rising edges are.

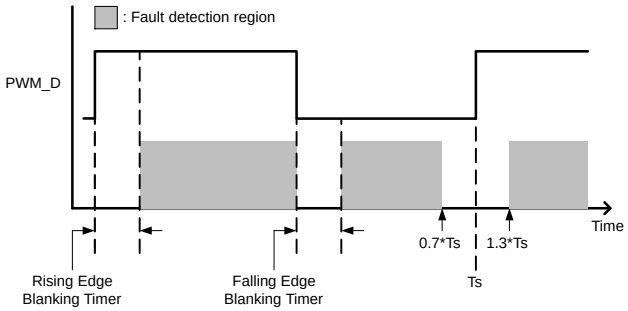


Figure 8. Switching Period/Frequency Detection Region

The RRAMP resistor sets the nominal switching frequency. The value of the RRAMP resistor is determined by the following equation:

For frequencies ≤ 300 kHz:

$$R_{RAMP} = \frac{56065}{f\,(kHz) - 19.7}\ k\Omega$$

For frequencies ≥ 300 kHz:

$$R_{RAMP} = \frac{59095}{f\,(kHz) - 4.55}\ k\Omega$$

In the above equation, f is the target switching frequency, in kHz.

Figure 9 shows how the switching period/frequency detection function detects a switching period longer than 1.3 times a nominal switching period. If SLOW_RAMP is allowed to reach Slow_Freq_Threshold, it indicates that either a missing pulse or a primary shutdown condition is detected and a frequency fault is declared. GFR and GFW are immediately pulled low and the PBSS voltage is discharged. The driver will go through a restart process when valid PWM pulses resume and VCC is above UVLO. The value of the RRAMP resistor sets the slope of SLOW_RAMP. The RRAMP value is chosen such that when SLOW_RAMP is reset to the ceiling voltage at the start of each switching cycle, SLOW_RAMP is not allowed to reach Slow_Freq_Threshold during the valid frequency range.

The missing pulse detection feature is very important to make the pre−bias startup function adaptive. When the isolated DC converter output is pre−biased during startup, before the secondary feedback loop reference voltage rises above the sensed voltage, the primary side PWM controller puts out very narrow PWM pulses, and there are multiple time intervals where the PWM pulses are missing while waiting for the secondary side circuit, including the bias voltage and feedback loop, to come up. During these multiple intervals where the PWM pulses are missing, the PBSS voltage is discharged. This ensures the PBSS voltage starts to charge up until the secondary side circuit has overcome the pre−bias voltage and is ready for a normal startup process without further missing PWM pulses. This ensures the pre−bias function works consistently for wide line and load conditions and pre−bias voltage variation.

Figure 10 shows how a switching period shorter than 0.7 times the nominal switching period is detected. Fast_Freq_threshold represents the voltage on FAST_RAMP that is equivalent to 0.7 times the nominal switching period. The value of the RRAMP resistor sets the slope of FAST_RAMP. If a PWM rising edge is detected before FAST_RAMP has reached Fast_Freq_threshold, a frequency detection fault is triggered. The PBSS voltage is discharged, the gate drives are disabled, and the driver will go through a restart process when valid PWM pulses resume and V_{CC} is above UVLO.

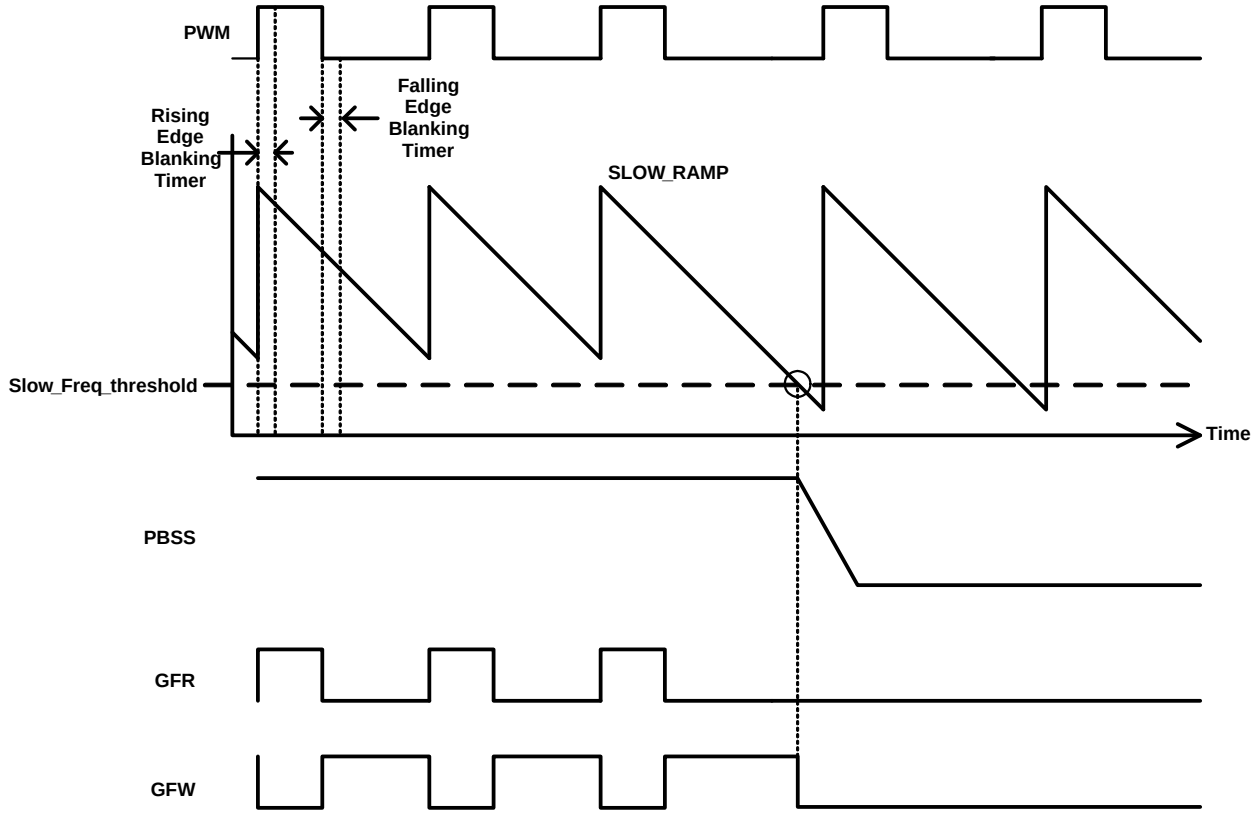


Figure 9. Slow Frequency Detection Leading To A Shutdown

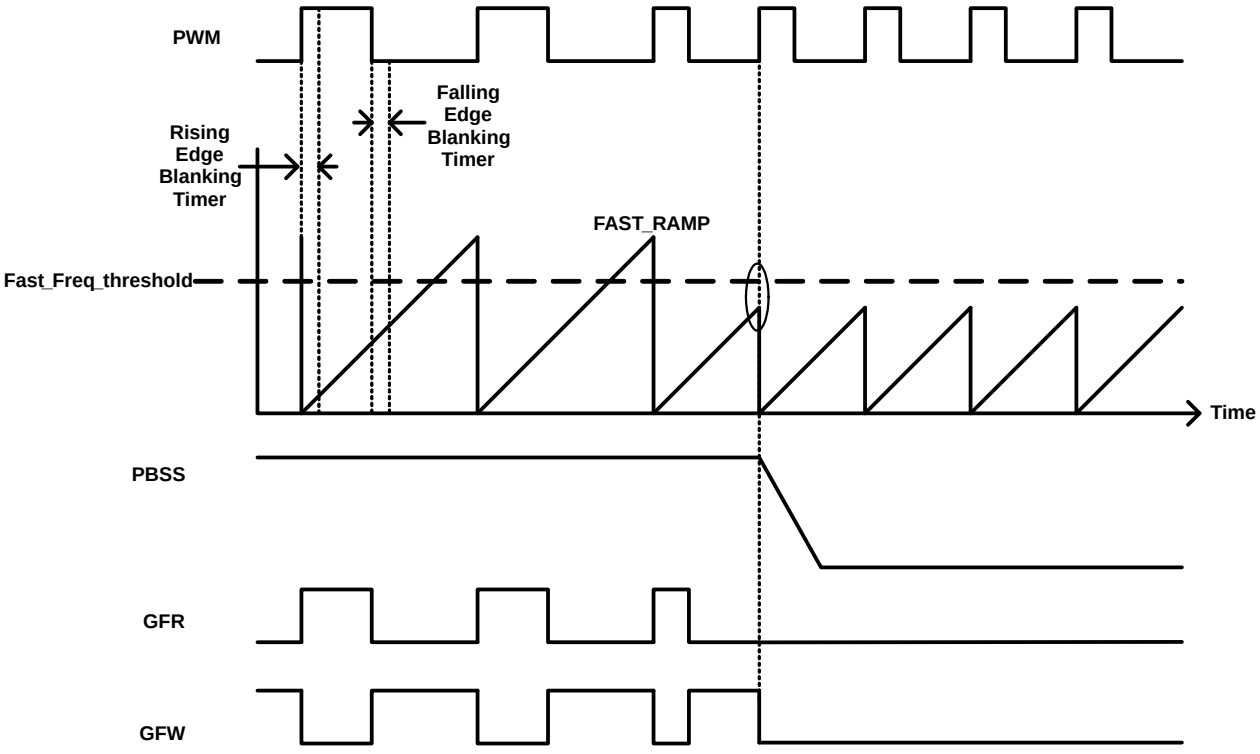


Figure 10. Fast Frequency Detection Leading To A Shutdown

LDO Regulator

The NCP81178 integrates a LDO regulator to generate a regulated V_{CC} voltage from an unregulated or loosely regulated DC voltage on the VIN pin. The regulated voltage on the LDO output VCC pin is nominally 6 V. The LDO regulator supplies the gate drive energy and the IC bias power in the NCP81178. It is capable of delivering at least 150 mA current. To stabilize the feedback loop of the LDO regulator, a ceramic capacitor with a value between 0.22 uF and 4.7 uF is required to be placed between VCC and PGND.

When VCC pin is connected to a DC source with a voltage higher than the LDO regulated output voltage, the LDO regulator is disabled and the NCP81178 is powered from the external DC source.

UVLO

The NCP81178 has an under−voltage lock−out feature on the V_{CC} supply voltage. The driver outputs will be disabled until VCC exceeds the UVLO threshold. There is a hysteresis, typically 400 mV, on this threshold.

Dummy Load Function

During startup, the DL pin will discharge the voltage at the output of the power supply, if DL is connected to the output voltage with a resistor. Once VCC is above the UVLO threshold voltage, the DL pin will start sinking current once:

1. The voltage on PBSS is below 3 V.
2. A valid pulse is detected on PWM.

DL will continue to pull low for 128 SLOW_RAMP cycles after the last valid PWM pulse after PBSS rises above 3 V.

Exposed Pad

The exposed metal pad at the bottom of the package is connected to GND and aids in enhancing the thermal performance of the package.

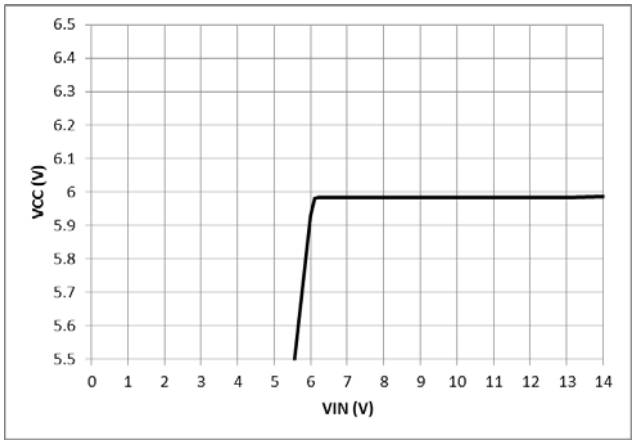


Figure 11. V_{CC} Regulation vs. V_{IN} (T_J = 25°C)

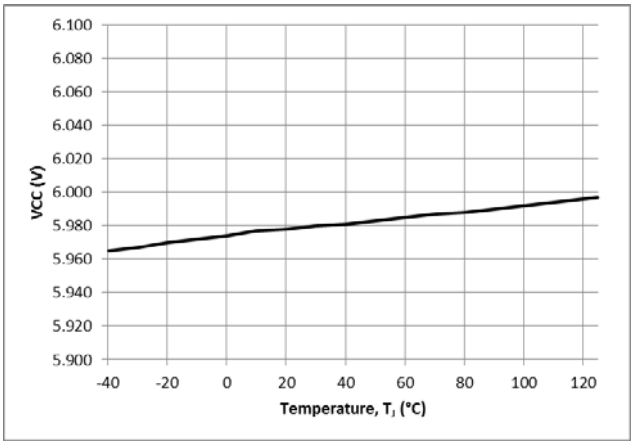


Figure 12. V_{CC} Regulation vs. Temperature (V_{IN} = 10 V)

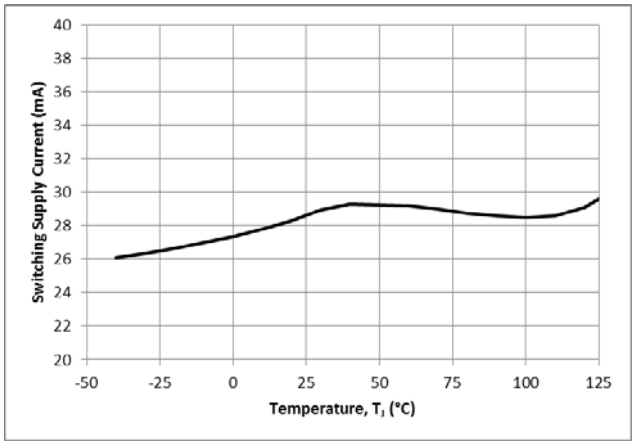


Figure 13. Switching Supply Current vs. Temperature (V_{CC} = 6 V, 4.7 nF Loads, 450 kHz)

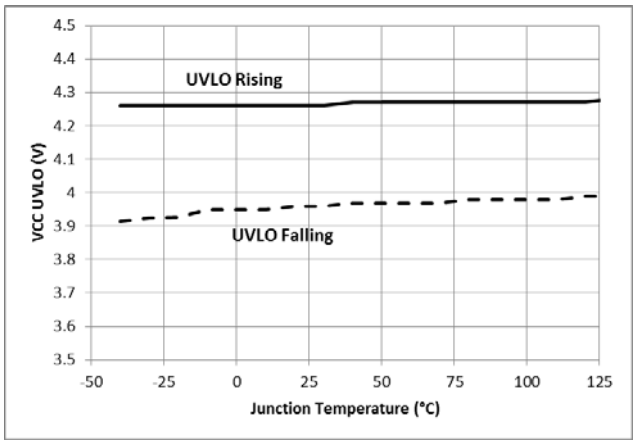


Figure 14. V_{CC} UVLO vs. Temperature

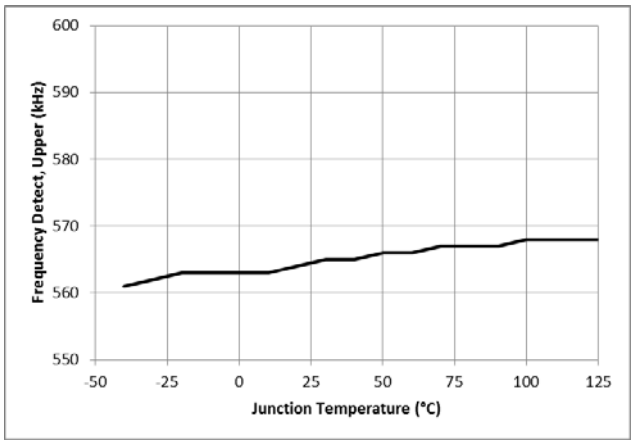


Figure 15. Upper Frequency Detect vs. Temperature (RRAMP = 130 kΩ)

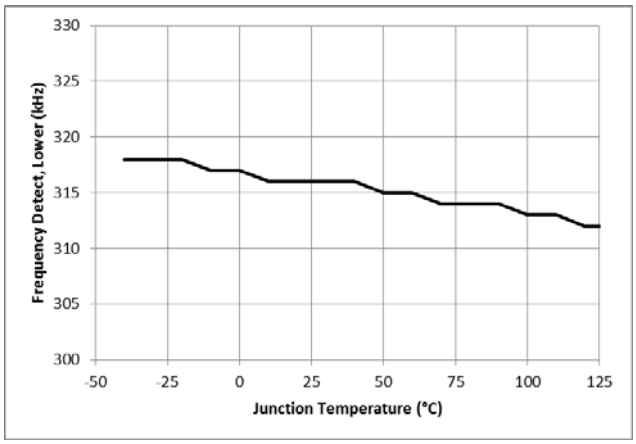


Figure 16. Lower Frequency Detect vs. Temperature (RRAMP = 130 kΩ)

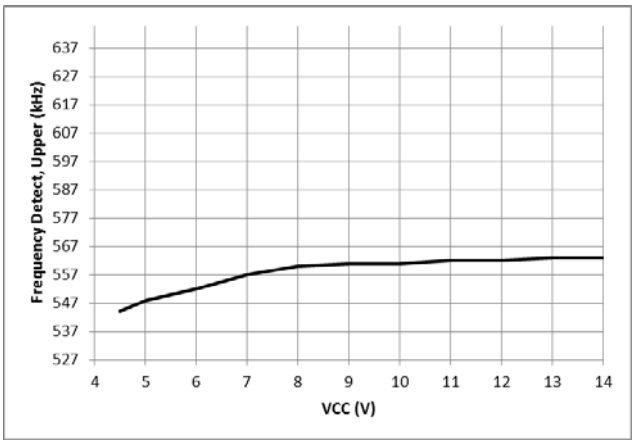


Figure 17. Upper Frequency Detect vs. V_{CC} (T_J = 25°C)

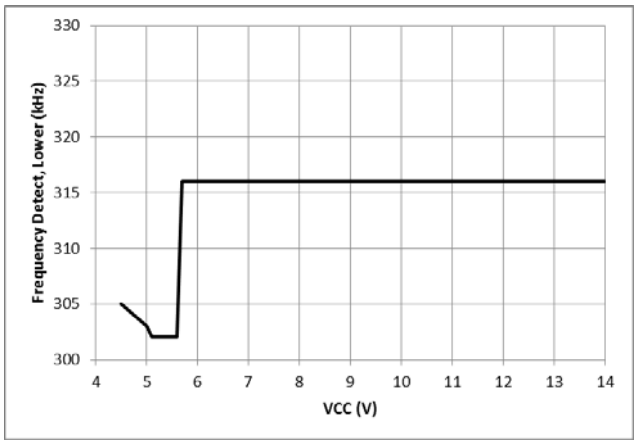
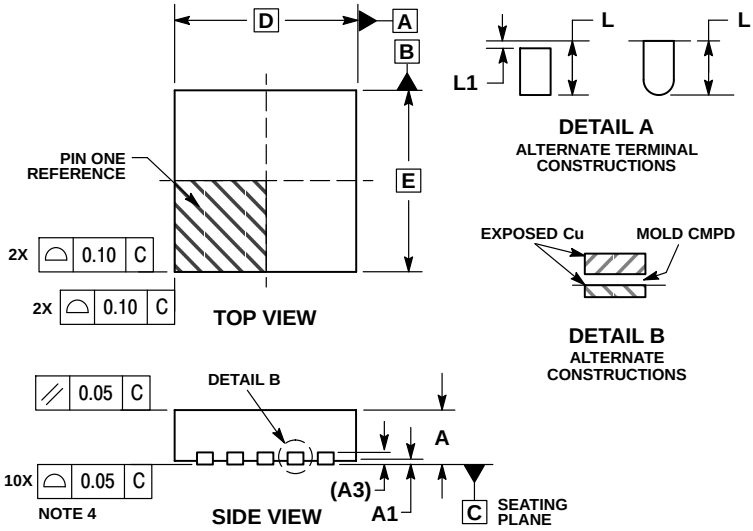


Figure 18. Lower Frequency Detect vs. V_{CC} (T_J = 25°C)

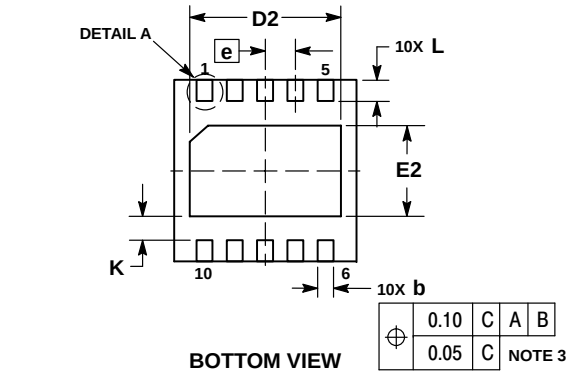
PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P
CASE 506CL
ISSUE O

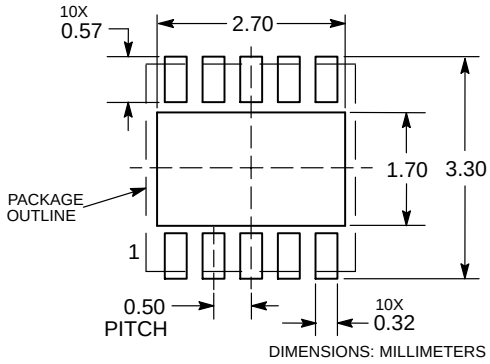


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.40	1.60
e	0.50 BSC	
K	0.25	−−−
L	0.25	0.45
L1	0.00	0.03



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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