LDO Regulator, 100 mA, 18 V, 1 mA IQ, with PG

NCP711

The NCP711 device is based on unique combination of features – very low quiescent current, fast transient response and high input and output voltage ranges. The NCP711 is CMOS LDO regulator designed for up to 18 V input voltage and 100 mA output current. Quiescent current of only 1 μA makes this device ideal solution for battery–powered, always–on systems. Several fixed output voltage versions are available as well as the adjustable version.

The device (version B) implements power good circuit (PG) which indicates that output voltage is in regulation. This signal could be used for power sequencing or as a microcontroller reset.

Internal short circuit and over temperature protections saves the device against overload conditions.

Features

- Operating Input Voltage Range: 2.7 V to 18 V
- Output Voltage: 1.2 V to 17 V
- Capable of Sourcing 140 mA Peak Output Current
- Low Shutdown Current: 100 nA typ.
- Very Low Quiescent Current: 1 μA typ.
- Low Dropout: 215 mV typ. at 100 mA
- Output Voltage Accuracy ±1%
- Power Good Output (Version B)
- Stable with Small 1 μF Ceramic Capacitors
- Built–in Soft Start Circuit to Suppress Inrush Current
- Over–Current and Thermal Shutdown Protections
- Available in Small TSOP–5 and WDFN6 (2x2) Packages
- These Devices are Pb–Free and are RoHS Compliant

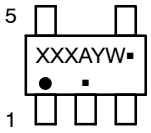
Typical Applications

- Battery Power Tools and Equipment
- Home Automation
- RF Devices
- Metering
- Remote Control Devices
- White Goods

MARKING DIAGRAMS



TSOP–5
CASE 483
SN SUFFIX



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package
(Note: Microdot may be in either location)

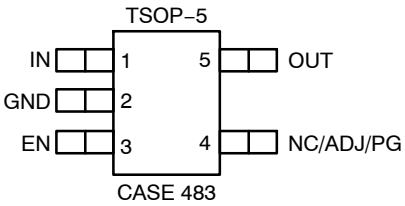


WDFN6 (2x2)
CASE 511BR
MT SUFFIX

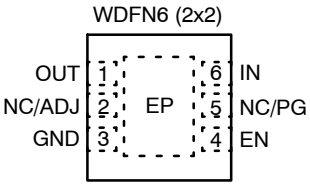


XX = Specific Device Code
M = Date Code

PIN ASSIGNMENTS



CASE 483



CASE511BR
(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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TYPICAL APPLICATION SCHEMATICS

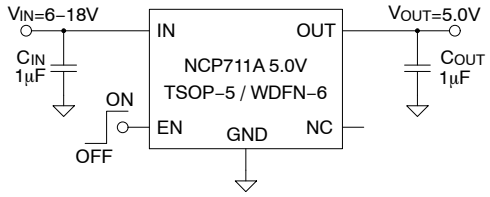

Figure 1. Fixed Output Voltage Application (No PG)

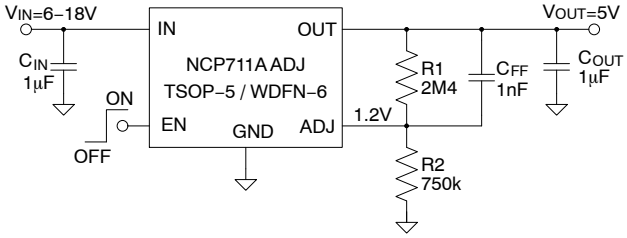

Figure 2. Adjustable Output Voltage Application (No PG)

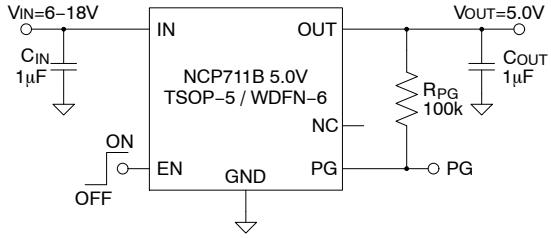

Figure 3. Fixed Output Voltage Application with PG

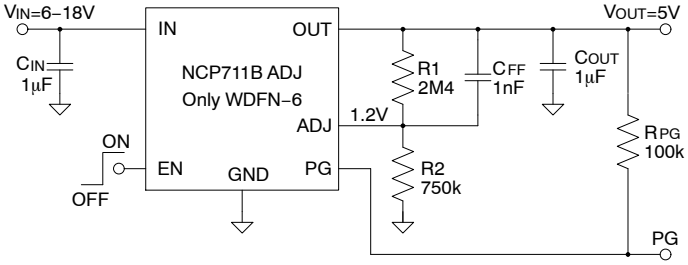

Figure 4. Adjustable Output Voltage Application with PG

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$$

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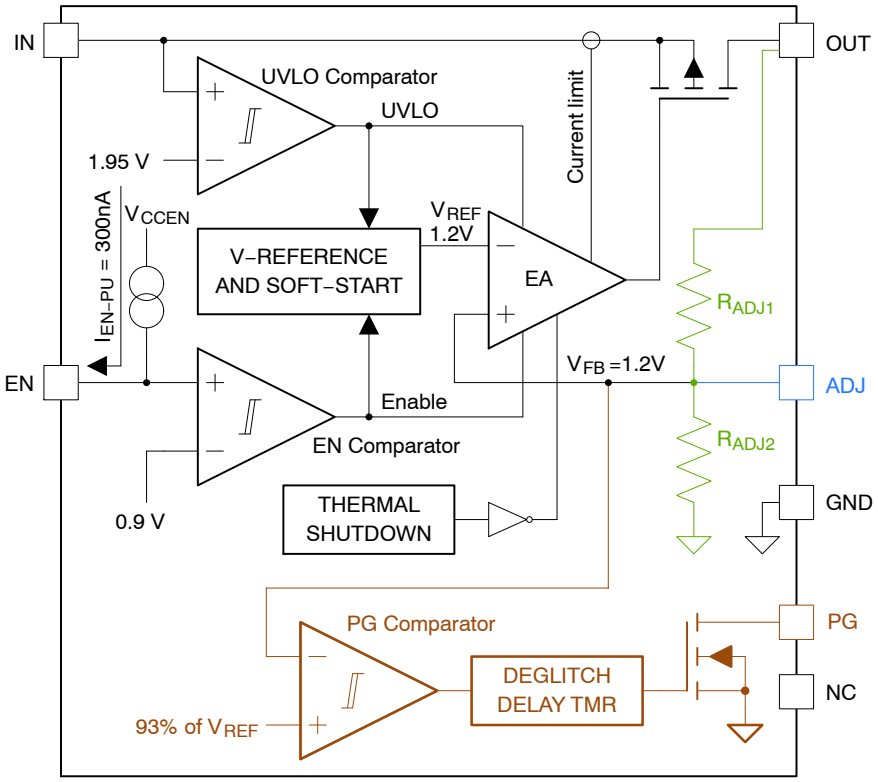
SIMPLIFIED BLOCK DIAGRAMS



Note: Blue objects are valid for ADJ version
Green objects are valid for FIX version
Brown objects are valid for B version (with PG)

Figure 5. Internal Block Diagram

PIN DESCRIPTION

Pin No. TSOP−5	Pin No. WDFN−6	Pin Name	Description
1	6	IN	Power supply input pin.
2	3	GND	Ground pin.
5	1	OUT	LDO output pin.
3	4	EN	Enable input pin (high − enabled, low − disabled). If this pin is connected to IN pin or if it is left unconnected (pull−up resistor is not required) the device is enabled.
4 (Note 1)	2	ADJ	Adjust input pin. Connect it to the output resistor divider or directly to the OUT pin.
4 (Note 1)	5	PG	Power good output pin. Could be left unconnected or could be connected to GND if not needed. High level for power ok, low level for fail.
4 (Note 1)	2, 5	NC	Not internally connected. This pin can be tied to the ground plane to improve thermal dissipation.
NA	EP	EPAD	Connect the exposed pad to GND.

1. Pin function depends on device version.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VIN Voltage (Note 2)	V_{IN}	−0.3 to 22	V
VOUT Voltage	V_{OUT}	*ADJ version & FIX versions $V_{OUT-NOM}$ > 5.0 V:* −0.3 to [(V_{IN} + 0.3) or 22; whichever is lower] *FIX versions $V_{OUT-NOM}$ ≤ 5.0 V:* −0.3 to [(V_{IN} + 0.3) or 6.0; whichever is lower]	V
EN Voltage	V_{EN}	−0.3 to (V_{IN} + 0.3)	V
ADJ Voltage	$V_{FB/ADJ}$	−0.3 to 5.5	V
PG Voltage	V_{PG}	−0.3 to (V_{IN} + 0.3)	V
Output Current	I_{OUT}	Internally limited	mA
PG Current	I_{PG}	3	mA
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101

THERMAL CHARACTERISTICS (Note 4)

Characteristic	Symbol	WDFN6 2x2	TSOP−5	Unit
Thermal Resistance, Junction−to−Air	R_{thJA}	67	178	°C/W
Thermal Resistance, Junction−to−Case (top)	R_{thJCt}	89	93	°C/W
Thermal Resistance, Junction−to−Case (bottom)	R_{thJCb}	11	N/A	°C/W
Thermal Resistance, Junction−to−Board (top)	R_{thJBt}	44	53	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	Psi_{JCt}	4.6	18	°C/W
Thermal Characterization Parameter, Junction−to−Board [FEM]	Psi_{JB}	44	53	°C/W

4. Measured according to JEDEC board specification (board 1S2P, Cu layer thickness 1 oz, Cu area 650 mm^2, no airflow). Detailed description of the board can be found in JESD51−7.

ELECTRICAL CHARACTERISTICS (V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective capacitance − Note 5), T_J = −40°C to 125°C, ADJ tied to OUT, unless otherwise specified) (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Recommended Input Voltage		V_{IN}	2.7	−	18	V
Output Voltage Accuracy	T_J = −40°C to +85°C	V_{OUT}	−1	−	1	%
	T_J = −40°C to +125°C		−1	−	2	
ADJ Reference Voltage	ADJ version only	V_{ADJ}	−	1.2	−	V
ADJ Input Current	V_{ADJ} = 1.2 V	I_{ADJ}	−0.1	0.01	0.1	μA
Line Regulation	V_{IN} = $V_{OUT-NOM}$ + 1 V to 18 V and V_{IN} ≥ 2.7 V	$\Delta V_{O(\Delta VI)}$	−	−	0.2	$\%V_{OUT}$
Load Regulation	I_{OUT} = 0.1 mA to 100 mA	$\Delta V_{O(\Delta IO)}$	−	−	0.4	$\%V_{OUT}$
Quiescent Current (version A)	V_{IN} = $V_{OUT-NOM}$ + 1 V to 18 V, I_{OUT} = 0 mA	I_Q	−	1.3	2.5	μA
Quiescent Current (version B)	V_{IN} = $V_{OUT-NOM}$ + 1 V to 18 V, I_{OUT} = 0 mA		−	1.8	3.0	
Ground Current	I_{OUT} = 100 mA	I_{GND}	−	325	450	μA
Shutdown Current (Note 10)	V_{EN} = 0 V, I_{OUT} = 0 mA, V_{IN} = 18 V	I_{SHDN}	−	0.35	1.5	μA
Output Current Limit	V_{OUT} = $V_{OUT-NOM}$ − 100 mV	I_{OLIM}	140	250	450	mA

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ELECTRICAL CHARACTERISTICS (V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective capacitance – Note 5), T_J = −40°C to 125°C, ADJ tied to OUT, unless otherwise specified) (Note 6) (continued)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Short Circuit Current	V_{OUT} = 0 V		I_{OSC}	140	250	450	mA
Dropout Voltage (Note 7)	I_{OUT} = 100 mA		V_{DO}	–	215	355	mV
Power Supply Ripple Rejection	V_{IN} = $V_{OUT-NOM}$ + 2 V I_{OUT} = 10 mA	10 Hz	PSRR	–	80	–	dB
		10 kHz		–	70	–	
		100 kHz		–	42	–	
		1 MHz		–	48	–	
Output Noise	f = 10 Hz to 100 kHz, $V_{OUT-NOM}$ = 5.0 V		V_N	–	240	–	μV_{RMS}
EN Threshold	V_{EN} rising		V_{EN-TH}	0.7	0.9	1.05	V
EN Hysteresis	V_{EN} falling		V_{EN-HY}	0.01	0.1	0.2	V
EN Internal Pull−up Current	V_{EN} = 1 V, V_{IN} = 5.5 V		I_{EN-PU}	0.01	0.3	1	μA
EN Input Leakage Current	V_{EN} = 18 V, V_{IN} = 18 V		I_{EN-LK}	−1	0.05	1	μA
Start−up time (Note 8)	$V_{OUT-NOM}$ ≤ 3.3 V		t_{START}	100	250	500	μs
	$V_{OUT-NOM}$ > 3.3 V			300	600	1000	
Internal UVLO Threshold	Ramp V_{IN} up until output is turned on		V_{IUL-TH}	1.6	1.95	2.6	V
Internal UVLO Hysteresis	Ramp V_{IN} down until output is turned off		V_{IUL-HY}	0.05	0.2	0.3	V
PG Threshold (Note 9)	V_{OUT} falling		V_{PG-TH}	90	93	96	%
PG Hysteresis (Note 9)	V_{OUT} rising		V_{PG-HY}	0.1	2	4	%
PG Deglitch Time (Note 9)			t_{PG-DG}	75	160	270	μs
PG Delay Time (Note 9)			t_{PG-DLY}	120	320	600	μs
PG Output Low Level Voltage (Note 9)	I_{PG} = 1 mA		V_{PG-OL}	–	0.2	0.4	V
PG Output Leakage Current (Note 9)	V_{PG} = 18 V		I_{PG-LK}	–	0.01	1	μA
Thermal Shutdown Temperature	Temperature rising from T_J = +25°C		T_{SD}	–	165	–	°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
6. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
7. Dropout measured when the output voltage falls 100 mV below the nominal output voltage. Limits are valid for all voltage versions with nominal output voltage higher than or equal to 2.5 V. For lower output voltage versions, the dropout test is not applied because the input voltage during the test would fall below the minimum input voltage 2.7 V.
8. Startup time is the time from EN assertion to point when output voltage is equal to 95% of $V_{OUT-NOM}$.
9. Applicable only to version B (device option with power good output). PG threshold and PG hysteresis are expressed in percentage of nominal output voltage.
10. Shutdown current includes EN Internal Pull−up Current.

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{OUT} = 1.0 μF, ADJ tied to OUT, T_J = 25°C, unless otherwise specified

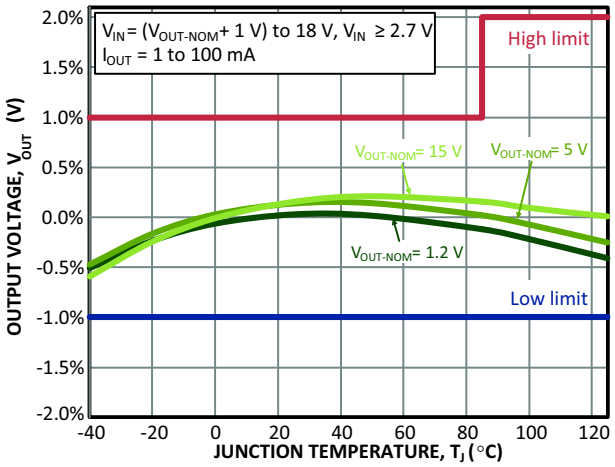

Figure 6. Output Voltage vs. Temperature

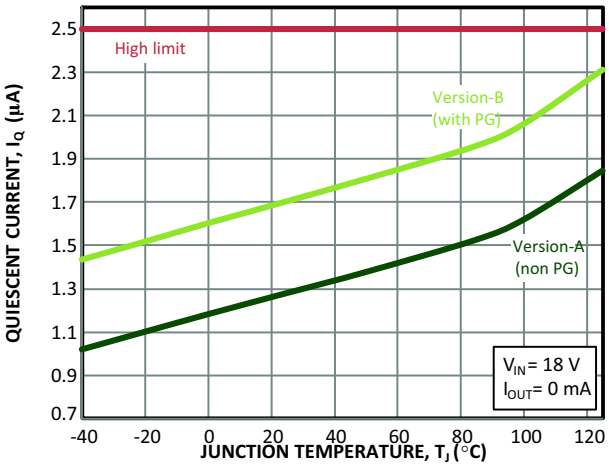

Figure 7. Quiescent Current vs. Temperature

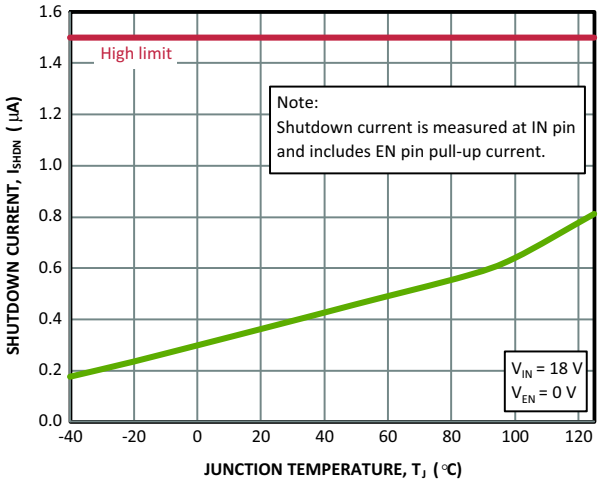

Figure 8. Shutdown Current vs. Temperature

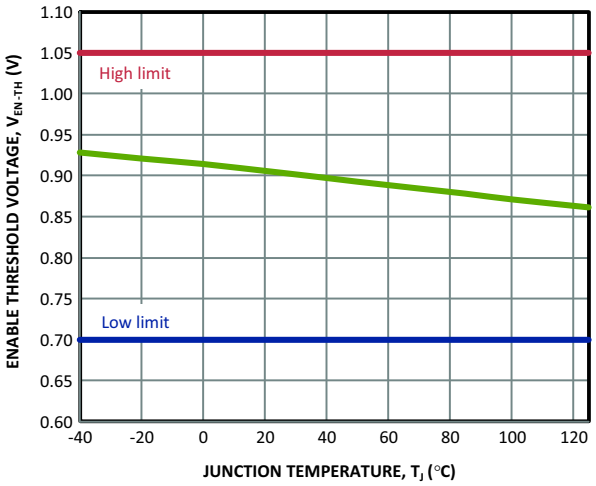

Figure 9. Enable Threshold Voltage vs. Temperature

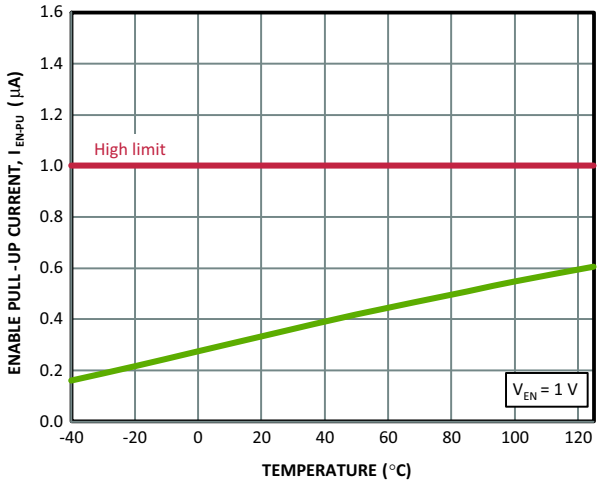

Figure 10. Enable Internal Pull−Up Current vs. Temperature

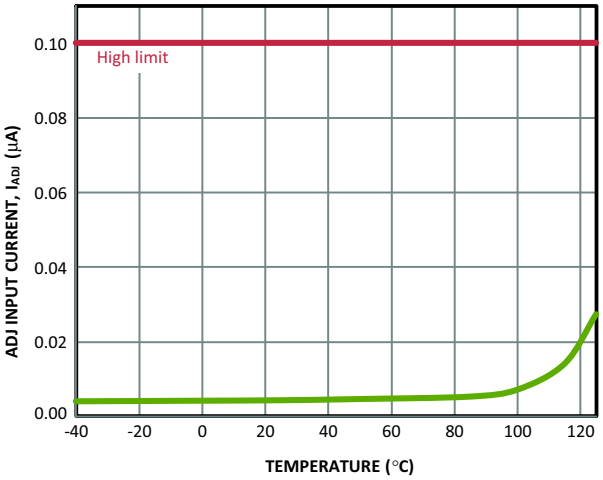

Figure 11. ADJ Input Current vs. Temperature

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{OUT} = 1.0 μF, ADJ tied to OUT, T_J = 25°C, unless otherwise specified

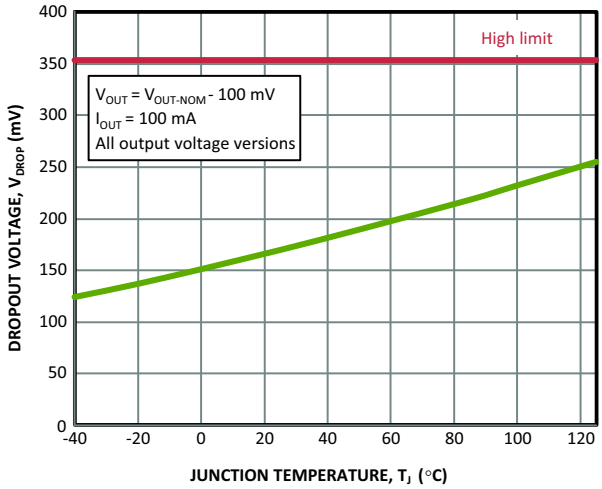

Figure 12. Dropout Voltage vs. Temperature

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{OUT} = 1.0 μF, ADJ tied to OUT, T_J = 25°C, unless otherwise specified

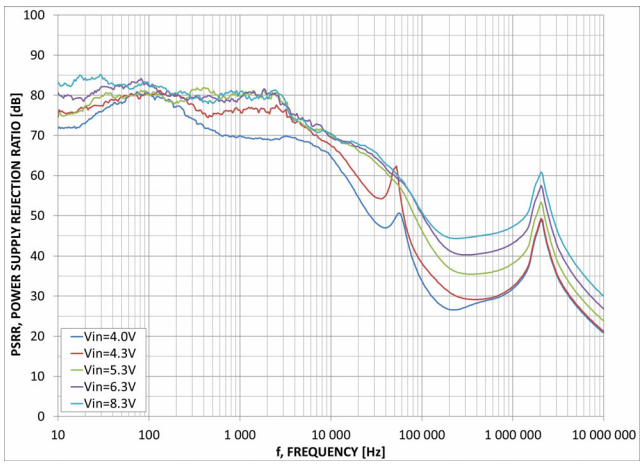

Figure 13. PSRR – FIX–3.3 V, C_{OUT} = 1 μF, I_{OUT} = 100 mA

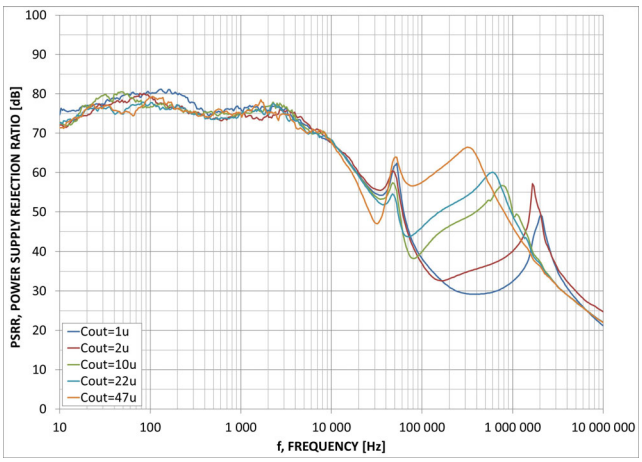

Figure 14. PSRR – FIX–3.3 V, V_{IN} = 4.3 V, I_{OUT} = 100 mA

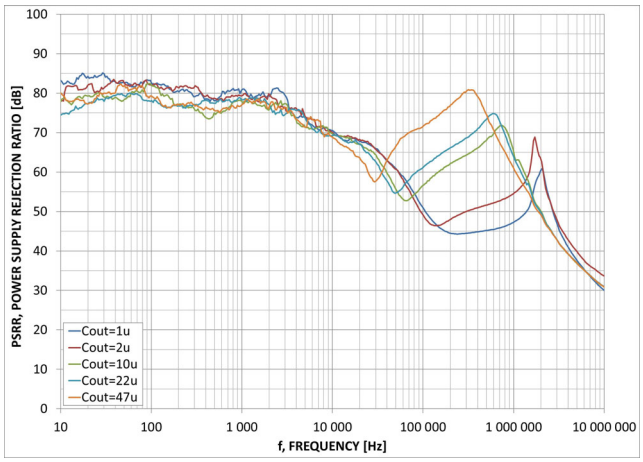

Figure 15. PSRR – FIX–3.3 V, V_{IN} = 8.3 V, I_{OUT} = 100 mA

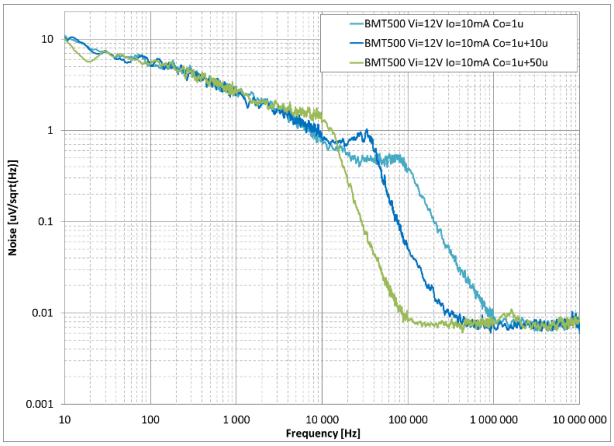

Figure 16. Noise – FIX – 5.0 V, I_{OUT} = 10 mA, Different C_{OUT}

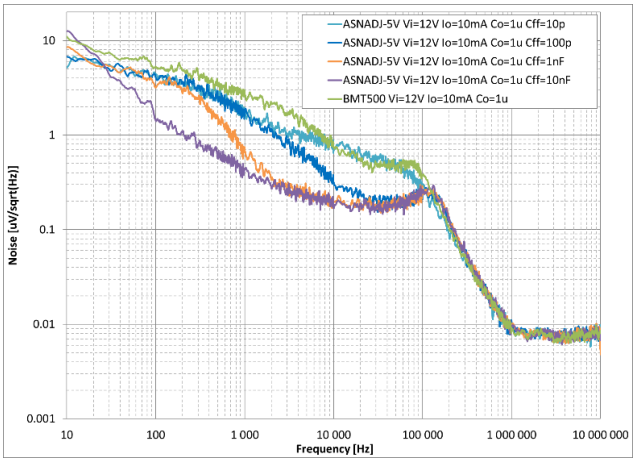

Figure 17. Noise – ADJ–set–5.0 V with Different C_{FF} and FIX – 5.0 V

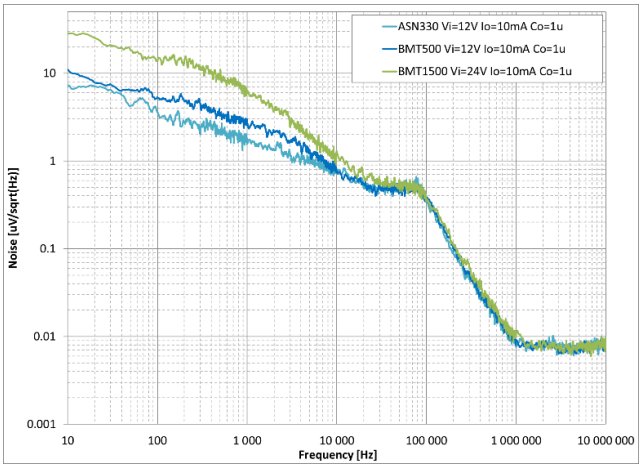

Figure 18. Noise – FIX, I_{OUT} = 10 mA, C_{OUT} = 1 μF, Different V_{OUT}

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ORDERING INFORMATION

Part Number	Marking	Voltage Option ($V_{OUT-NOM}$)	Version	Package	Shipping
NCP711ASNADJT1G	GDA	ADJ	Without PG	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP711ASN300T1G	GDC	3.0 V			
NCP711ASN330T1G	GDD	3.3 V			
NCP711ASN500T1G	GDE	5.0 V			
NCP711BMTADJTBG	PA	ADJ	With PG	WDFN6 2x2 (Pb−Free)	3000 / Tape & Reel
NCP711BMT300TBG	PC	3.0 V			
NCP711BMT330TBG	PD	3.3 V			
NCP711BMT500TBG	PE	5.0 V			

NOTE: To order other package, voltage version or PG / non PG variant, please contact your ON Semiconductor sales representative.

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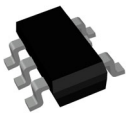
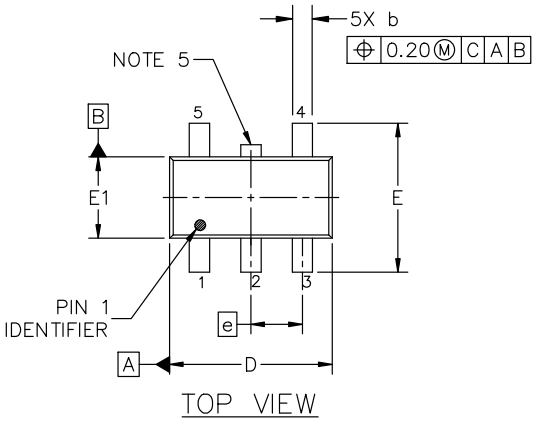
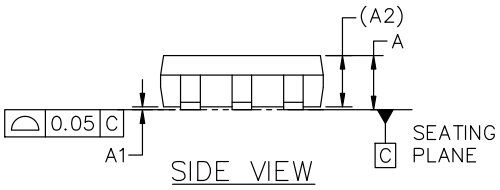


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

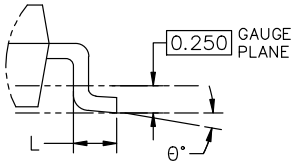
DATE 01 APR 2024



TOP VIEW



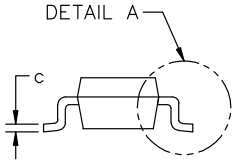
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

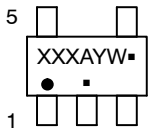
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

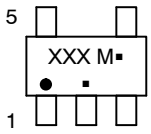
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

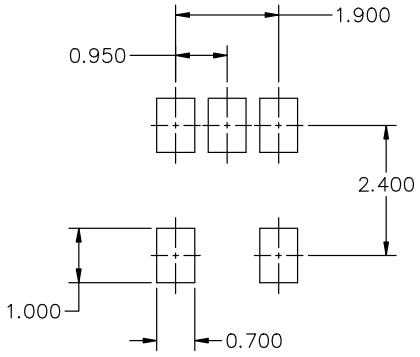
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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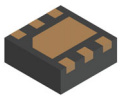
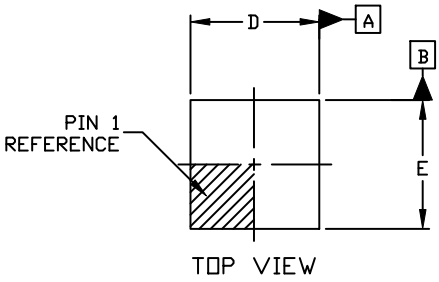
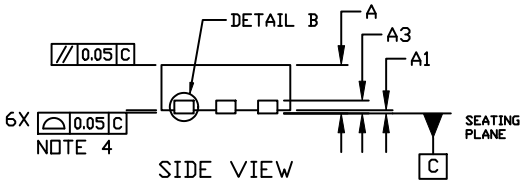
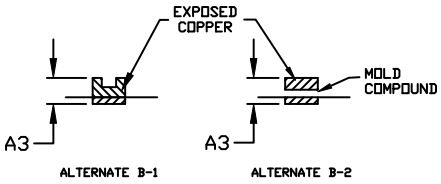


WDFN6 2x2, 0.65P
CASE 511BR
ISSUE C

DATE 01 DEC 2021



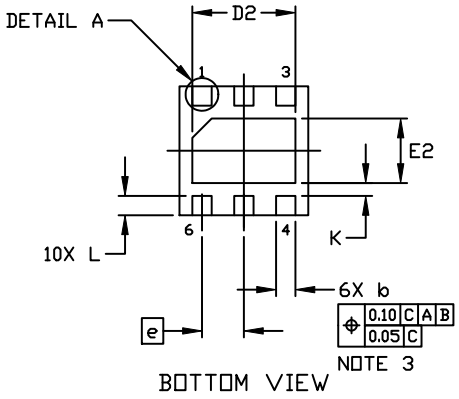


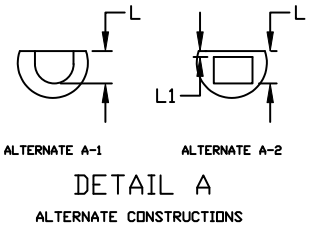


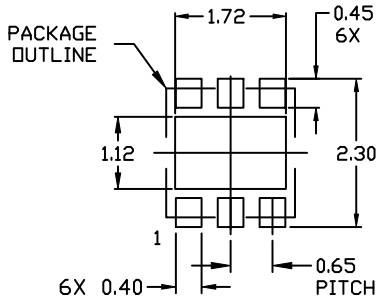
NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e		0.65 BSC	
K		0.20 REF	
L	0.20	0.30	0.40
L1	---	---	0.15







For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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