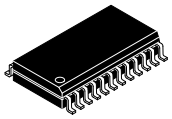
High Performance Combo Controller for ATX Power Supplies

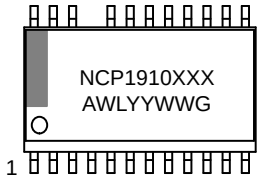
NCP1910



SO-24WB Less Pin 21
DW SUFFIX
CASE 752AB

Housed in a SO-24WB package, the NCP1910 combines a state-of-the-art circuitry aimed to powering next generation of ATX or flat TVs converters. With a 65 or 100 kHz Continuous Conduction Mode Power Factor Controller and a LLC controller hosting a high-voltage driver, the NCP1910 is ready to power 85+ types of offline power supplies. To satisfy stringent efficiency considerations, the PFC circuit implements an adjustable frequency fold back to reduce switching losses as the load is going light. To cope with all the signal sequencing required by the ATX and flat TVs specifications, the controller includes several dedicated pins enabling handshake between the secondary and the primary sides. These signals include a power-good line but also a control pin which turns the controller on and off via an opto coupler. Safety-wise, a second OVP input offers the necessary redundancy in case the main feedback network would drift away. Finally, a fast fault input immediately reacts in presence of an over current condition by triggering an auto-recovery soft-start sequence.

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 35 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 35.

Features

- Fixed-Frequency 65 or 100 kHz CCM Power Factor Controller
- Average Current-Mode Control for Low Line Distortion
- Dynamic Response Enhancer Reduces Bulk Undershoot
- Independent Over Voltage Protection Sensing Pin with Latch-off Capability
- Adjustable Frequency Fold Back Improves Light Load Efficiency
- Adjustable Line Brown-Out Protection with 50 ms Delay to Help Meeting Hold-up Time Specifications
- Programmable Over current Threshold Leads to an Optimized Sensing Resistor
- ±1 A peak Current Drive Capability
- LLC Controller Operates from 25 kHz to 500 kHz
- On Board 600 V High-Voltage Drivers
- 1 A/0.5 A Sink/Source Capability
- Minimum Frequency Precision Down to ±3% Over Temperature Range
- Internally Fixed Dead-Time Value of 300 ns
- Adjustable Soft-Start Sequence
- Fast Fault Input with Soft-Start Trigger for Immediate Auto-recovery Protection
- $\overline{\text{On}}$/Off Control Pin for Secondary-Based Remote Control
- On-Board 5 V Reference Voltage for Precise Thresholds/Hysteresis Adjustments
- Power Good Output Management Signal
- A Version with Dual Ground Pinout (No Skip), B Version with Single Ground and Skip Operation for the LLC Controller
- 20 V Operation
- These are Pb-Free Devices

Typical Applications

- Multi Output ATX Power Supplies (A version)
- Flat TVs Power Supplies (B version)

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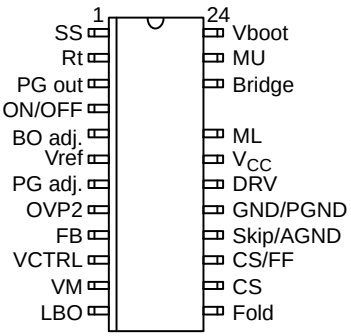

Figure 1. Pin Connections

PIN DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	SS	Soft-Start	A capacitor to ground sets the LLC soft-start duration
2	Rt	The LLC Feedback Pin	A resistive arrangement sets the maximum and minimum switching frequencies with opto coupler-based feedback capabilities.
3	PG out	The Open-Collector Power Good Signal	This pin is low when V_{bulk} is ok, opens when V_{bulk} passes below a level adjusted by PGadj pin.
4	$\overline{on}$/off	Remote Control	When pulled low, the circuit operates: the PFC starts first and once FB is in regulation, the LLC is authorized to work. When left open, the controller is in idle mode.
5	BO adj.	Brown-Out Adjustment	This pin sets the on and off levels for the PFC powering the LLC converter
6	Vref	The 5 V Reference Pin	This pin delivers a stable voltage for threshold adjustments
7	PG adj.	The Power Good Trip Level	From the Vref pin, a dc level sets the trip point for the PFC bulk voltage at which the PG out signal is down.
8	OVP2	Redundant OVP	A fully latched OVP monitoring the PFC bulk independently from FB pin.
9	FB	PFC Feedback	Monitors the boost bulk voltage and regulates it. It also serves as a quick auto-recovery OVP
10	V_{CTRL}	PFC Error Amplifier Output	PFC error amplifier compensation pin
11	V_M	PFC Current Amplifier Output	A resistor to ground sets the maximum power level
12	LBO	PFC Line Input Voltage Sensing	Line feed forward and PFC brown-out
13	Fold	PFC Fold Back	This pin selects the power level at which the frequency starts to reduce gradually.
14	CS	PFC Current Sense	This pin senses the inductor current and also programs the maximum sense voltage excursion
15	CS/FF	Fast-Fault Input	When pulled above 1 V, the LLC stops and re-starts via a full soft-start sequence.
16	Skip/AGND	Skip (B)/AGND (A)	This pin is either used as the analog GND for the signal circuit (A) or for skip operation (B).
17	GND/PGND	GND (B)/PGND (A)	The controller ground for the driving loop (A) or the lump ground pin for all circuits (B)
18	DRV	PFC Drive Signal	The driving signal to the PFC power MOSFET
19	V_{CC}	The Controller Supply	The power supply pin for the controller, 20 V max.
20	ML	Lower-Side MOSFET	Drive signal for the lower side half-bridge MOSFET
22	Bridge	Half-Bridge	This pin connects to the LLC half-bridge
23	MU	Upper-Side MOSFET	Drive signal for the upper side half-bridge MOSFET
24	V_{boot}	Bootstrapped Vcc	The bootstrapped V_{CC} for the floating driver

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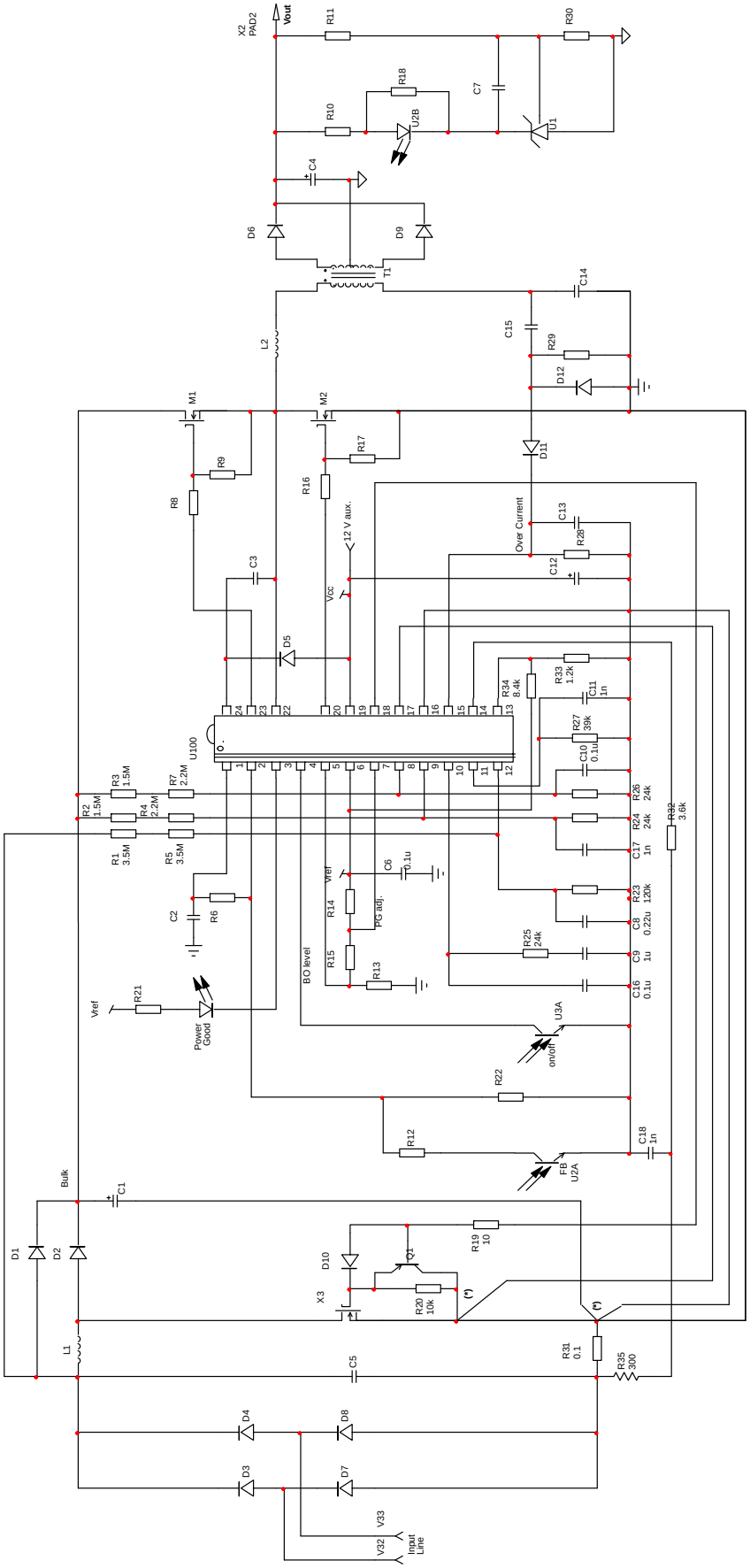

* It is recommended to separate the traces of power ground and analog ground. The power ground (pin 17) for driving loop (PFC DRV and LLC ML) is connected to the PFC MOSFET directly. The analog ground for adjustment components is routed together first and then connected to the analog ground pin (pin 16) and the PFC sense resistor directly.

Figure 2. Typical Application Schematic in A Version

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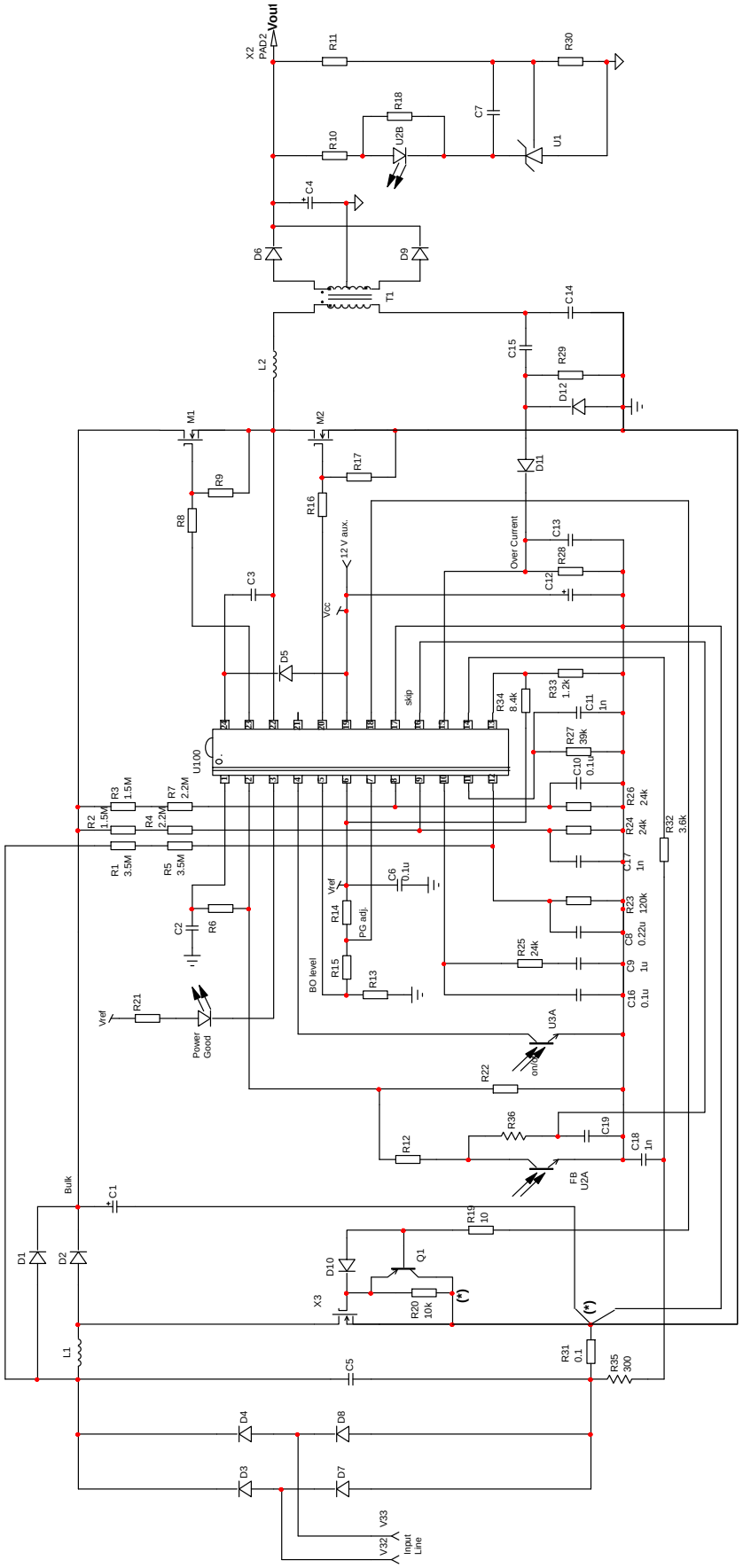

* It is recommended to separate the traces of power ground and analog ground. The analog ground traces for adjustment components are routed together first and then connected to the ground pin (pin 17). The power ground for driving loop (PFC DRV and LLC ML) is connected from ground pin (pin 17) to the PFC sense resistor directly and as short as possible.

Figure 3. Typical Application Schematic in B Version

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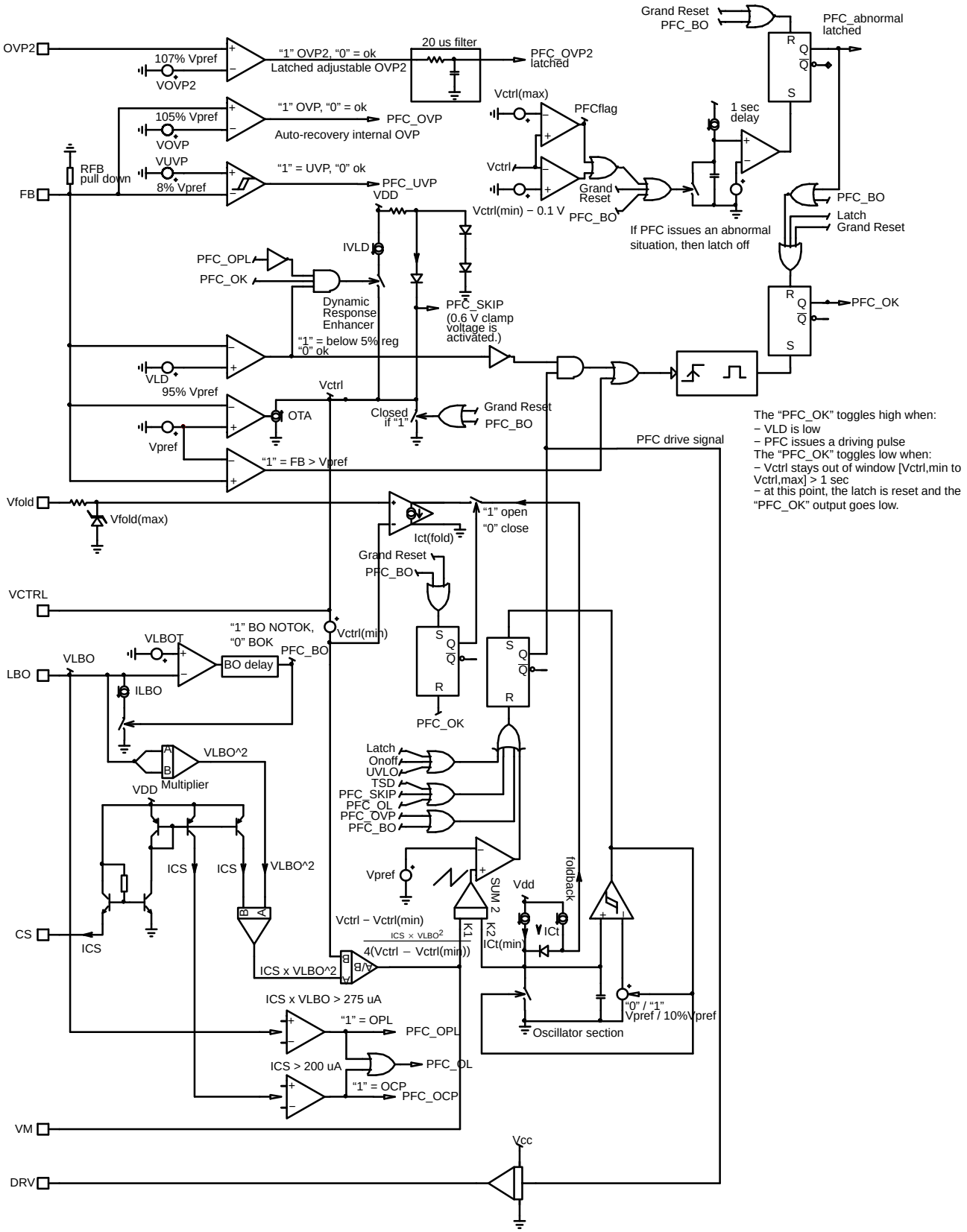

Figure 4. Internal PFC Block Diagram

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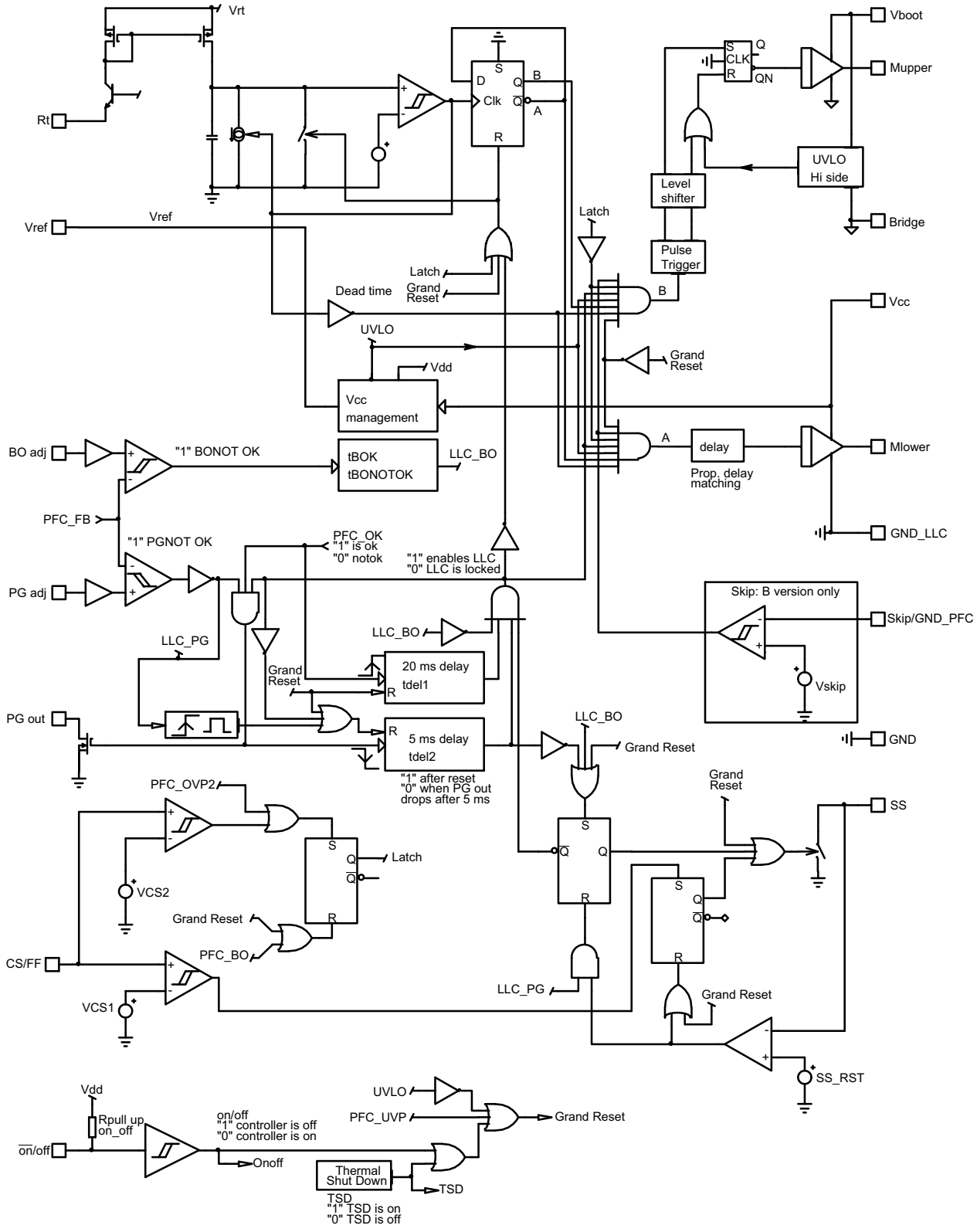

Figure 5. Internal LLC Block Diagram

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MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{Bridge}	Continuous High Voltage Bridge Pin, Pin 22	−1 to 600	V
$V_{BOOT} - V_{Bridge}$	Floating Supply Voltage, Pin 24−22	−0.3 to 20	V
V_{MU}, V_{DRV}	High Side Output Voltage, Pin 23	V_{BRIDGE} − 0.3 to V_{BOOT} + 0.3	V
V_{ML}	Low Side Output Voltage, Pin 18, 20	−0.3 to V_{CC} + 0.3	V
dV_{Bridge}/dt	Allowable Output Slew Rate on the Bridge Pin, Pin 22	50	V/ns
V_{CC}	Power Supply Voltage, Pin 19	20	V
	Pin Voltage, All Pins (except pin 2, 6, 18−24, GND)	−0.3 to 10	V
$R_{\theta JA}$	Thermal Resistance Junction-to-Air 50 mm^2, 1 oz 650 mm^2, 1 oz	 80 65	°C/W
	Storage Temperature Range	−60 to + 150	°C
	ESD Capability, Human Body Model (All pins except V_{CC} and HV)	2	kV
	ESD Capability, Machine Model	200	V
V_{CC}	Power Supply Voltage, Pin 19	20	V
	Pin Voltage, All Pins (except pin 2, 6, 18 ~ 24, GND)	−0.3 to 10	V
V_{Rt}	R_t Pin Voltage	−0.3 to 5	V
V_{ref_out}	V_{ref} Pin Voltage	−0.3 to 7	V
I_{MAX}	Pin Current on Pin 10, 12, and 13	0.5	mA
I_{PGout}	Pin Current on Pin 3	5	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22-A114E
   Machine Model 200 V per JEDEC Standard JESD22-A115-A
2. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25 °C, for min/max values T_J = −40 °C to +125 °C, Max T_J = 150 °C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
COMMON TO BOTH CONTROLLERS						
SUPPLY SECTION						
$V_{CC(on)}$	Turn-On Threshold Level, V_{CC} Going Up	19	9.4	10.4	11.4	V
$V_{CC(min)}$	Minimum Operating Voltage after Turn-On	19	8	9	10	V
$V_{CC(Hys)}$	Hysteresis between $V_{CC(on)}$ and $V_{CC(min)}$	19	1.2	–	–	V
$V_{Boot(on)}$	Startup Voltage on the Floating Section	24, 22	7.8	8.8	9.8	V
$V_{Boot(min)}$	Cutoff Voltage on the Floating Section	24, 22	7	8	9	V
$I_{startup}$	Startup Current, $V_{CC} < V_{CC(on)}$	19	–	–	100	μA
I_{CC1}	PFC Consumption Alone, DRV Pin Unloaded, On/Off Pin Grounded, LLC Off • 65 kHz Version • 100 kHz Version	19	 – –	 5.1 5.3	 6.4 6.54	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. In normal operation, when the power supply is un-plugged, the bulk voltage goes down. At a first crossed level, the PG pin opens. Later, when the bulk crosses a second level, the LLC turns off. There is no timing link between these events, except the bulk capacitor discharge slope. However, if for an unknown reason the PFC is disabled (fault, short-circuit), the PG pin immediately opens and if sufficient voltage is still present on the bulk (e.g. in high line condition), the LLC will be disabled after a typical time of 5 ms.
4. Guaranteed by design.

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ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25 °C, for min/max values T_J = −40 °C to +125 °C, Max T_J = 150 °C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
COMMON TO BOTH CONTROLLERS						
SUPPLY SECTION						
I_{CC2}	PFC Consumption Alone, DRV Pin Loaded by 1 nF, On/Off Pin Grounded, LLC Off • 65 kHz Version • 100 kHz Version	19	 – –	 5.9 6.4	 7.4 7.9	mA
I_{CC4}	IC Consumption, Both PFC & LLC DRV Pin Unloaded, R_t = 70 kΩ (LLC F_{SW} = 25 kHz) • 65 kHz Version • 100 kHz Version	19	 – –	 5.9 6.0	 7.2 7.3	mA
I_{CC5}	IC Consumption, Both PFC & LLC DRV Pin Loaded by 1 nF, R_t = 70 kΩ (LLC F_{SW} = 25 kHz) • 65 kHz Version • 100 kHz Version	19	 – –	 6.9 7.4	 8.6 9.1	mA
I_{CC6}	IC Consumption in Fault Mode from V_{boot} (Drivers Disabled, $V_{boot} > V_{boot(min)}$)	19	–	64	300	μA
I_{CC7}	IC Consumption in OFF Mode from V_{CC} ($\overline{On}$/Off Pin is Open)	19	–	–	950	μA
REFERENCE VOLTAGE						
$V_{ref-out}$	Reference Voltage for External Threshold Setting @ I_{out} = 5 mA	6	4.75	5	5.25	V
$V_{ref-out}$	Reference Voltage for External Threshold Setting @ I_{out} = 5 mA − T_J = 25 °C	6	4.9	5	5.1	V
$V_{refLineReg}$	Vcc Rejection Capability, I_{out} = 5 mA − ΔV_{CC} = 1 V − T_J = 25 °C	6	–	0.01	5	mV
$V_{refLoadReg}$	Reference Variation with Load Changes, 1 mA < I_{ref} < 5 mA − T_J = 25 °C	6	–	1.6	7	mV
$I_{ref-out}$	Maximum Output Current Capability	6	5	–	–	mA
NOTE: Maximum capacitance directly connected to V_{REF} pin must be under 100 nF.						
DELAY						
t_{DEL1}	Turn-On LLC Delay after PFC OK Signal is Asserted	–	10	20	30	ms
t_{DEL2}	Turn-Off LLC after Power Good Pin Goes Low (Note 3)	–	2	5	8	ms
PROTECTIONS						
$R_{Pull-up}$	$\overline{On}$/Off Pin Pull-Up Resistor	4	–	5	–	kΩ
$t_{on/off}$	Propagation Delay from On to Off (ML & MU are Off) (Note 4)	4	–	–	1	μs
V_{on}	Low Level Input Voltage on $\overline{On}$/Off Pin (NCP1910 is Enabled)	4	–	–	1	V
V_{off}	High Level Input Voltage on $\overline{On}$/Off Pin (NCP1910 is Disabled)	4	3	–	–	V
V_{op}	Open Voltage on $\overline{On}$/Off Pin	4	–	7	–	V
I_{PG}	Maximum Power Good Pin Sink Current Capability	3	5	–	–	mA
V_{PG}	Power Good Saturation Voltage for I_{PG} = 5 mA	3	–	–	350	mV
I_{PGadj}	Input Bias Current, PGadj Pin	7	–	10	–	nA
V_{PGadjH}	PG Comparator Hysteresis	7	–	100	–	mV
TSD	Temperature Shutdown (Note 4)	–	140	–	–	°C
TSDhyste	Temperature Hysteresis Shutdown	–	–	30	–	°C

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ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25 °C, for min/max values T_J = −40 °C to +125 °C, Max T_J = 150 °C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
POWER FACTOR CORRECTION						
GATE DRIVE SECTION						
R_{POH}	Source Resistance @ I_{DRV} = −100 mA	18	–	9	20	Ω
R_{POL}	Sink Resistance @ I_{DRV} = 100 mA	18	–	6.6	18	Ω
t_{Pr}	Gate Drive Voltage Rise Time from 1.5 V to 10.5 V (C_L = 1 nF)	18	–	60	–	ns
t_{Pf}	Gate Drive Voltage Fall Time from 10.5 V to 1.5 V (C_L = 1 nF)	18	–	40	–	ns
REGULATION BLOCK						
V_{PREF}	PFC Voltage Reference	–	2.425	2.5	2.575	V
I_{EA}	Error Amplifier Current Capability	10	–	±30	–	μA
G_{EA}	Error Amplifier Gain	–	100	200	300	μS
I_B	Bias Current @ V_{FB} = V_{PREF}	9	0	–	0.3	μA
V_{CTRL} $V_{CTRL(max)}$ $V_{CTRL(min)}$ ΔV_{CTRL}	 Maximum Control Voltage @ V_{FB} = 2 V Minimum Control Voltage @ V_{FB} = 3 V $\Delta V_{CTRL} = V_{CTRL(max)} - V_{CTRL(min)}$	 10 10 10	 – – 2.7	 3.6 0.6 3	 – – 3.3	V
$V_{OUT}L$ / V_{PREF}	Ratio (V_{OUT} Low Detect Threshold / V_{PREF}) (Note 4)	–	94	95	96	%
$H_{OUT}L$ / V_{PREF}	Ratio (V_{OUT} Low Detect Hysteresis / V_{PREF})	–	–	0.5	–	%
I_{VLD} + I_{EA}	Source Current when (V_{OUT} Low Detect) is Activated	10	190	230	260	μA
CURRENT SENSE						
V_S	Current Sense Pin Offset Voltage, (I_{CS} = 100 μA)	14	–	10	–	mV
$I_{CS(OCP)}$	Over-Current Protection Threshold	14	185	200	215	μA
POWER LIMIT						
I_{CS}x V_{LBO}	Over Power Limitation Threshold	–	215	275	335	μVA
$I_{CS(OPL1)}$ $I_{CS(OPL2)}$	Over-Power Current Threshold (V_{LBO} = 1.8 V, V_M = 0 V) Over-Power Current Threshold (V_{LBO} = 3.6 V, V_M = 0 V)	–	119 56	153 75	187 99	μA
PULSE WIDTH MODULATION						
F_{PSW}	PFC Switching Frequency • 65 kHz Version • 100 kHz Version	18	 58 90	 65 100	 72 110	kHz
$F_{PSW(fold)}$	Minimum Switching Frequency (V_{fold} = 1.5 V, V_{CTRL} = $V_{CTRL(min)}$ + 0.1 V) • 65 kHz Version • 100 kHz Version	18	 34 33	 39 40	 43 46	kHz
DC_{Pmax}	Maximum PFC Duty Cycle	18	–	97	–	%
DC_{Pmin}	Minimum PFC Duty Cycle	18	–	–	0	%
$V_{CTRL(fold)}$	V_{CTRL} Pin Voltage to Start Frequency Foldback (V_{fold} = 1.5 V)	10	1.8	2	2.2	V
$V_{CTRL(foldend)}$	V_{CTRL} Pin Voltage as Frequency Foldback Reducing to the Minimum (F_{PSW} = $F_{PSW(fold)}$, V_{fold} = 1.5 V)	10	1.4	1.6	1.8	V
$V_{fold(max)}$	Maximum Internal Fold Voltage (Note 4)	–	1.97	2	2.03	V
LINE BROWN-OUT DETECTION						
V_{LBOT}	Line Brown-Out Voltage Threshold	12	0.96	1.00	1.04	V
I_{LBOH}	Line Brown-Out Hysteresis Current Source	12	6	7	8	μA

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ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25 °C, for min/max values T_J = −40 °C to +125 °C, Max T_J = 150 °C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
POWER FACTOR CORRECTION						
LINE BROWN-OUT DETECTION						
$t_{LBO(blank)}$	Line Brown-Out Blanking Time	−	25	50	75	ms
$t_{LBO(window)}$	Line Brown-Out Monitoring Window (Note 4)	−	25	50	75	ms
$V_{LBO(clamp)}$	LBO Pin Clamped Voltage if $V_{BO} < V_{LBOT}$ during $t_{LBO(BLANK)}$ (I_{LBO} = 100 μA)	12	−	980	−	mV
V_{LBOH}	Hysteresis ($V_{LBOT} - V_{LBO(clamp)}$) (Note 4)	12	10	35	60	mV
$I_{LBO(clamp)}$	Current Capability of LBO	12	100	−	−	μA
$V_{LBO(PNP)}$	LBO Pin Voltage when Clamped by the PNP Transistor (I_{LBO} = 100 μA)	12	0.4	0.7	0.9	V
$V_{LBO(PD)}$	Pull Down V_{LBO} Threshold	12	1.8	2	2.2	V
$t_{LBO(Pdlimit)}$	Pull Down V_{LBO} Time Limitation	−	4.5	5	6.1	ms
$t_{PFCflag}$	Time Delay to Confirm that V_{CTRL} is the Maximum to Pull Down V_{LBO}	−	2.5	5	7.5	ms
$t_{LBO(Pdblank)}$	Pull Down V_{LBO} Blanking Time	−	55	77	90	ms
CURRENT MODULATION						
I_{M1}	Multiplier Output Current ($V_{CTRL} = V_{CTRL(max)} - 0.2$ V, V_{LBO} = 3.6 V, I_{CS} = 50 μA)	11	46	58	72	μA
I_{M2}	Multiplier Output Current ($V_{CTRL} = V_{CTRL(max)} - 0.2$ V, V_{LBO} = 1.2 V, I_{CS} = 150 μA)	11	15	19	24.5	
OVER-VOLTAGE PROTECTION						
V_{OVP1}	Internal Auto Recovery Over Voltage Threshold	9	2.536	2.615	2.694	V
V_{OVP1H}	Hysteresis of Internal Auto Recovery Over Voltage Threshold (Note 4)	9	−	44	60	mV
t_{OVP1}	Propagation Delay (V_{FB} = 108% V_{PREF}) to Drive Low	9, 18	−	500	−	ns
V_{OVP2}	External Latched Over Voltage Threshold	8	2.595	2.675	2.755	V
K_{OVPH}	The Difference between V_{OVP2} and V_{OVP1} over V_{PREF} ($(V_{OVP2} - V_{OVP1})/V_{PREF}$)	−	−	2	−	%
$t_{DELOVP2}$	External Latched OVP Integrating Filter Time Constant	−	−	20	−	μs
$I_{b,OVP2}$	Input Bias Current, OVP2	8	−	10	−	nA
UNDER-VOLTAGE PROTECTION						
$V_{UVP(on)}/V_{PREF}$	UVP Activate Threshold Ratio	9	4	8	12	%
$V_{UVP(off)}/V_{PREF}$	UVP Deactivate Threshold Ratio	9	6	12	18	%
$V_{UVP(H)}$	UVP Lockout Hysteresis	9	−	4	−	%
t_{UVP}	Propagation Delay (V_{FB} < 8 % V_{PREF}) to Drive Low	9−18	−	7	−	μs
PFC ABNORMAL						
$t_{PFCabnormal}$	PFC Abnormal Delay Time ($V_{CTRL} = V_{CTRL(max)}$ or $V_{CTRL} = V_{CTRL(min)} - 0.1$ V)	−	1	1.5	2.1	sec
LLC CONTROL SECTION						
OSCILLATOR						
$F_{Lsw,min}$	Minimum Switching Frequency, Rt = 70 kΩ on R_t Pin	2	24.25	25	25.75	kHz

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4. Guaranteed by design.

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ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25 °C, for min/max values T_J = −40 °C to +125 °C, Max T_J = 150 °C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
LLC CONTROL SECTION						
OSCILLATOR						
F_{Lsw}	Switching Frequency, DT_L = 300 ns, Rt = 7 kΩ on R_t Pin	2	208	245	282	kHz
$F_{Lsw,max}$	Maximum Switching Frequency, DT_L = 300 ns, Rt = 3.5 kΩ on R_t Pin	2	424	500	575	kHz
DC_L	Operating Duty-Cycle Symmetry	23, 20	48	50	52	%
V_{refRt}	Reference Voltage for Oscillator Charging Current Generation	2	3.33	3.5	3.67	V
R_{SS}	Discharge Switch Resistance	1	–	70	–	Ω
SS_{RST}	Soft-Start Reset Voltage	1	–	200	–	mV
V_{Skip}	Skip Cycle Threshold, B Version Only	16	350	400	450	mV
$V_{skip,hyste}$	Hysteresis Level on Skip Cycle Comparator, B Version Only	16	–	50	–	mV
DRIVE OUTPUT						
T_{Lr}	Output Voltage Rise-Time @ C_L = 1 nF, 10−90% of Output Signal	23, 20	–	40	–	ns
T_{Lf}	Output Voltage Fall-Time @ C_L = 1 nF, 10−90% of Output Signal	23, 20	–	20	–	ns
R_{LOH}	Source Resistance	23, 20	–	12	26	Ω
R_{LOL}	Sink Resistance	23, 20	–	5	11	Ω
DT_L	Dead Time, Measured between 50% of the Rise and Fall Edge	23, 20	268	327	386	ns
$I_{HV,leak}$	Leakage Current on High Voltage Pins to GND (600 Vdc)	22, 23, 24	–	–	5	μA
PROTECTIONS						
I_{BOadj}	Input Bias Current, BOadj Pin	5	–	15	–	nA
V_{BOadjH}	BO Comparator Hysteresis	5	–	100	–	mV
t_{BOK}	BO Comparator Integrating Filter Time Constant from High to Low	5	–	150	–	μs
$t_{BONOTOK}$	BO Comparator Integrating Filter Time Constant from Low to High	5	–	20	–	μs
V_{CS1}	Current-Sense Pin Level that Resets the Soft-Start Capacitor	15	0.95	1	1.05	V
V_{CS2}	Current-Sense Pin Level that Permanently Latches Off the Circuit	15	1.42	1.5	1.58	V
t_{CS}	Propagation Delay from VCS1/2 Activation to Respective Action	15	–	–	500	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. In normal operation, when the power supply is un-plugged, the bulk voltage goes down. At a first crossed level, the PG pin opens. Later, when the bulk crosses a second level, the LLC turns off. There is no timing link between these events, except the bulk capacitor discharge slope. However, if for an unknown reason the PFC is disabled (fault, short-circuit), the PG pin immediately opens and if sufficient voltage is still present on the bulk (e.g. in high line condition), the LLC will be disabled after a typical time of 5 ms.
4. Guaranteed by design.

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TYPICAL CHARACTERISTICS

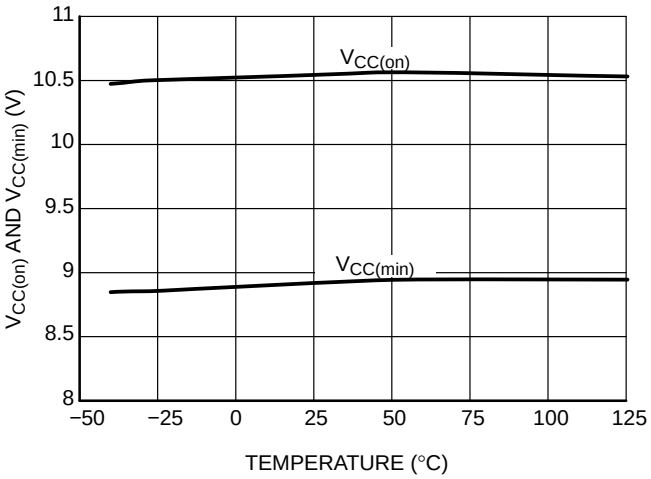

Figure 6. $V_{CC(on)}$ and $V_{CC(min)}$ vs. Temperature

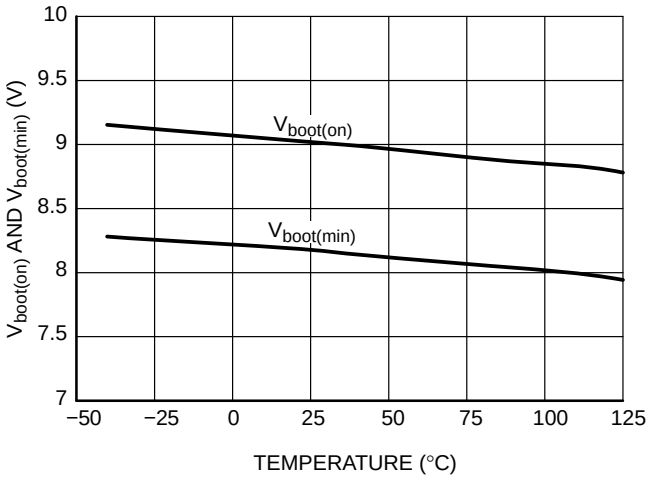

Figure 7. $V_{boot(on)}$ and $V_{boot(min)}$ vs. Temperature

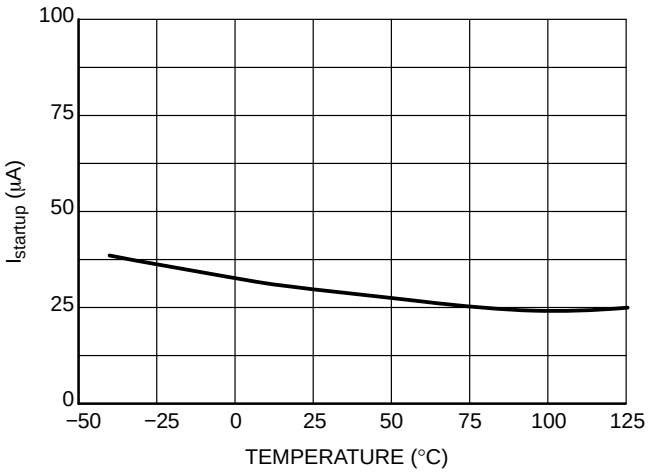

Figure 8. $I_{startup}$ vs. Temperature

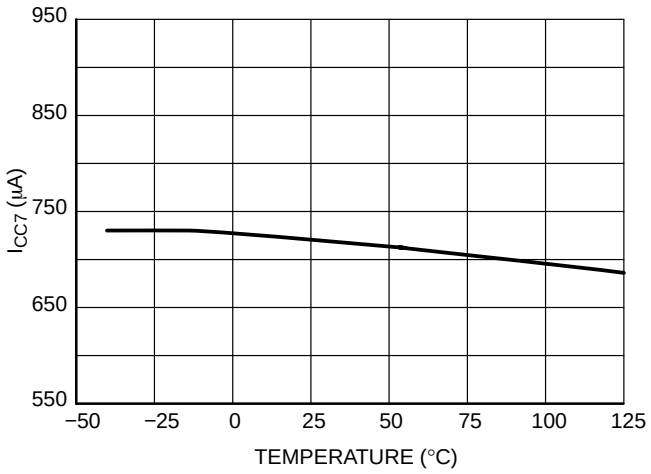

Figure 9. I_{CC7} vs. Temperature

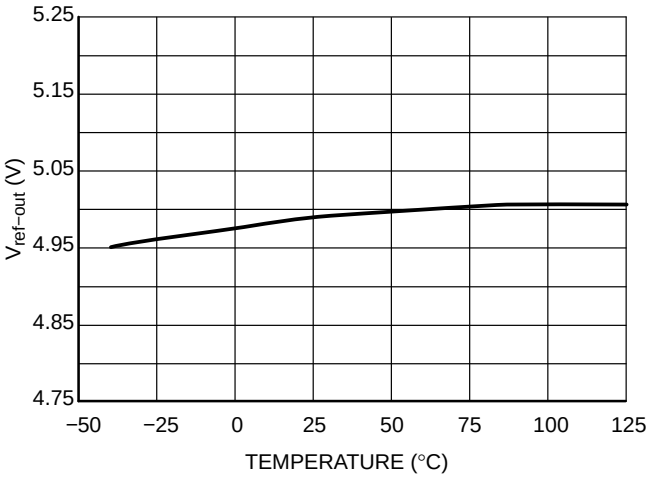

Figure 10. $V_{ref\text{-}out}$ vs. Temperature

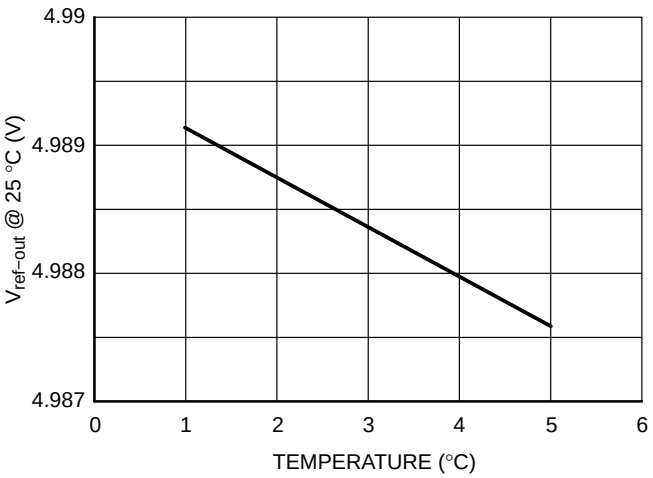

Figure 11. $V_{ref\text{-}out}$ @ 25 °C vs. $I_{ref\text{-}out}$

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TYPICAL CHARACTERISTICS

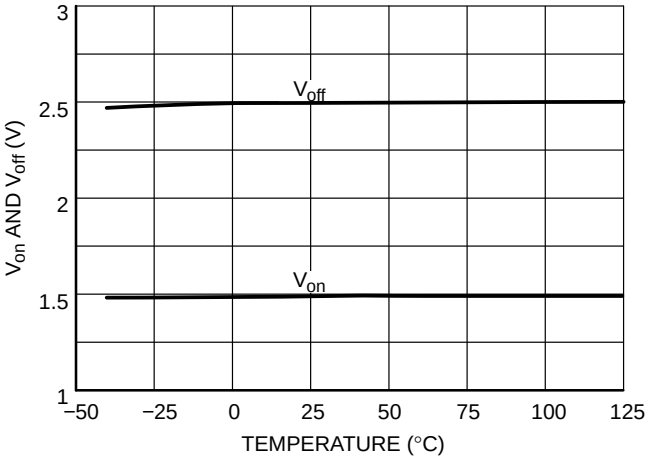

Figure 12. V_{on} and V_{off} vs. Temperature

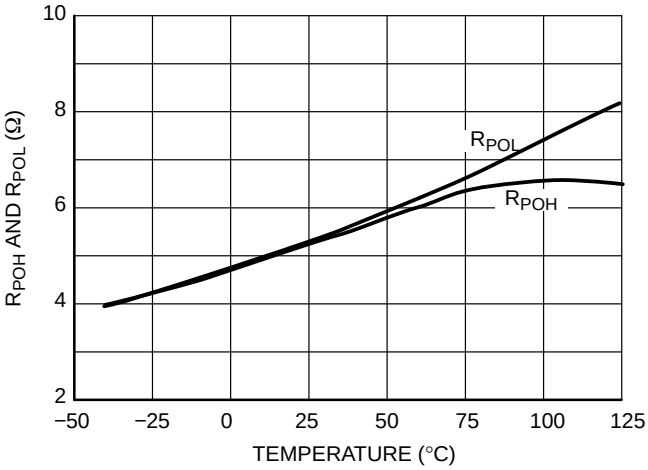

Figure 13. R_{POH} and R_{POL} vs. Temperature

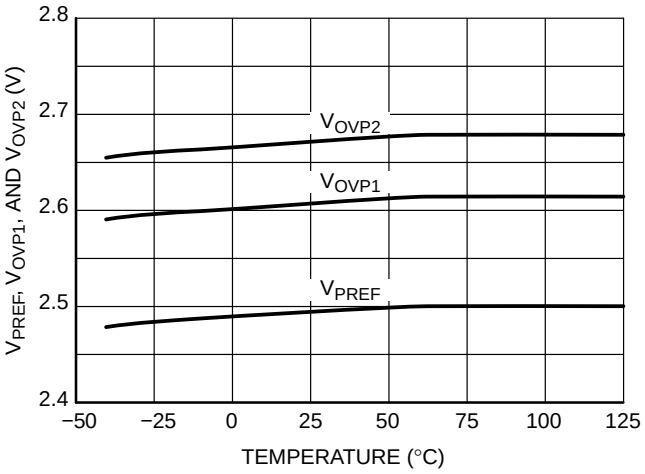

Figure 14. V_{PREF}, V_{OVP1}, and V_{OVP2} vs. Temperature

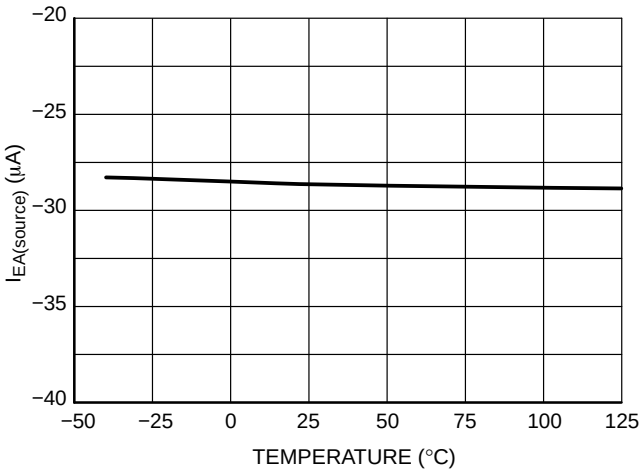

Figure 15. $I_{EA(source)}$ vs. Temperature

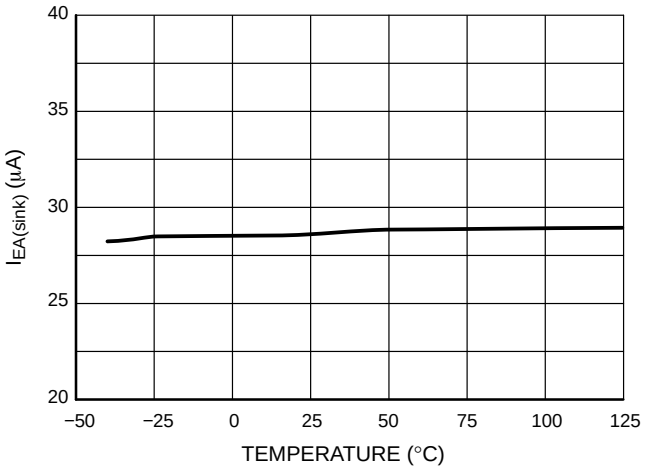

Figure 16. $I_{EA(sink)}$ vs. Temperature

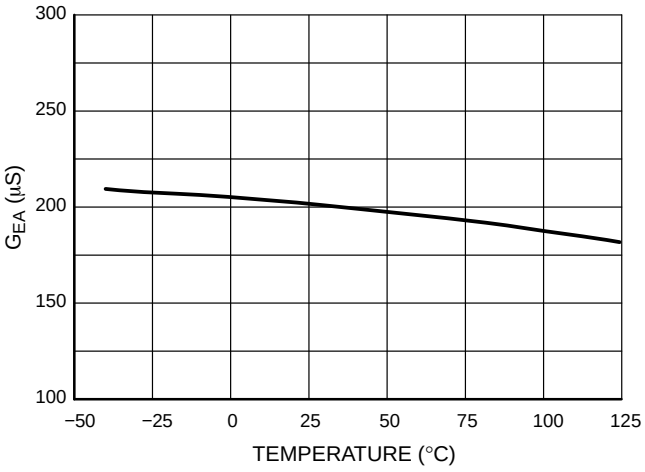

Figure 17. G_{EA} vs. Temperature

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TYPICAL CHARACTERISTICS

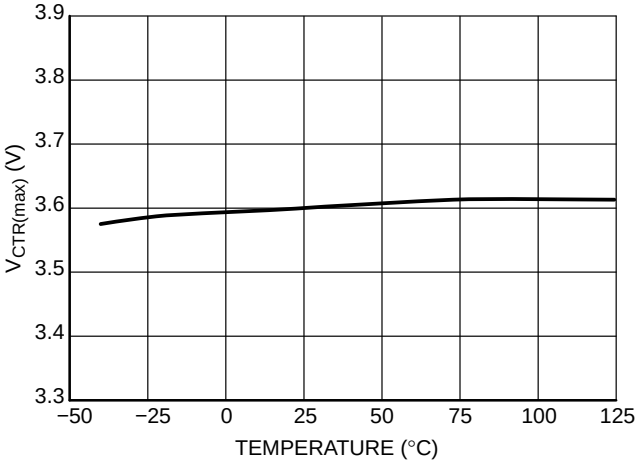

Figure 18. $V_{CTRL(max)}$ vs. Temperature

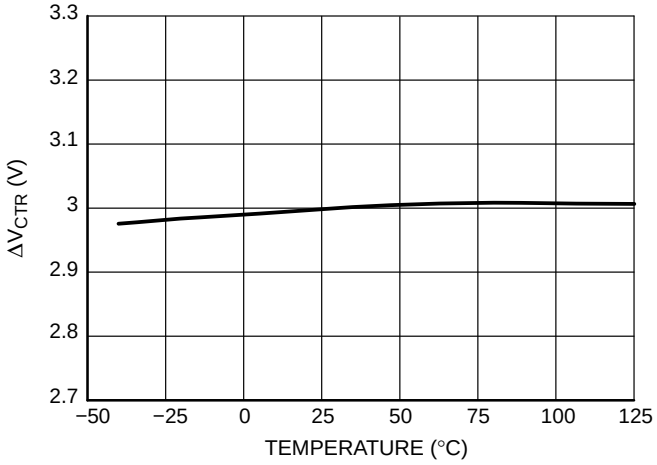

Figure 19. ΔV_{CTRL} vs. Temperature

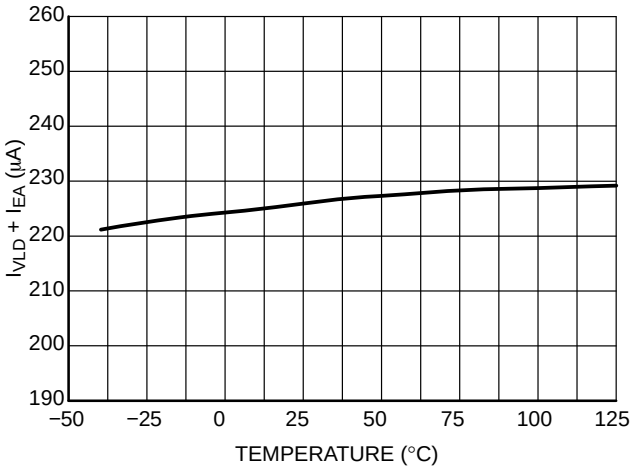

Figure 20. I_{VLD}+I_{EA} vs. Temperature

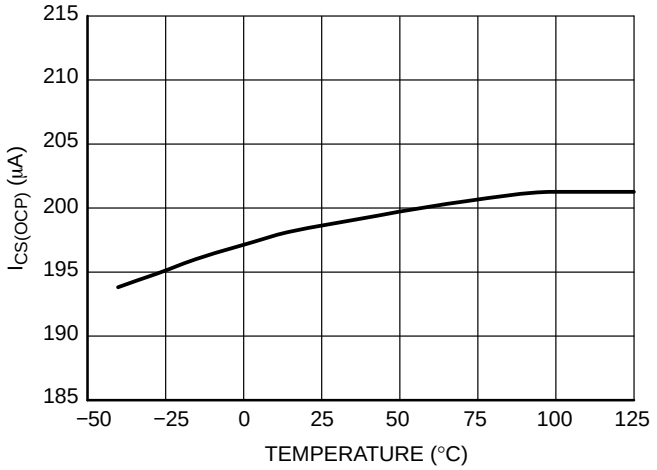

Figure 21. $I_{CS(OCP)}$ vs. Temperature

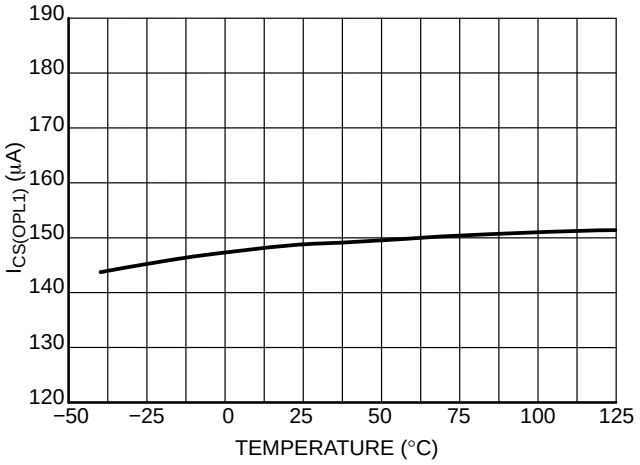

Figure 22. $I_{CS(OPL1)}$ vs. Temperature

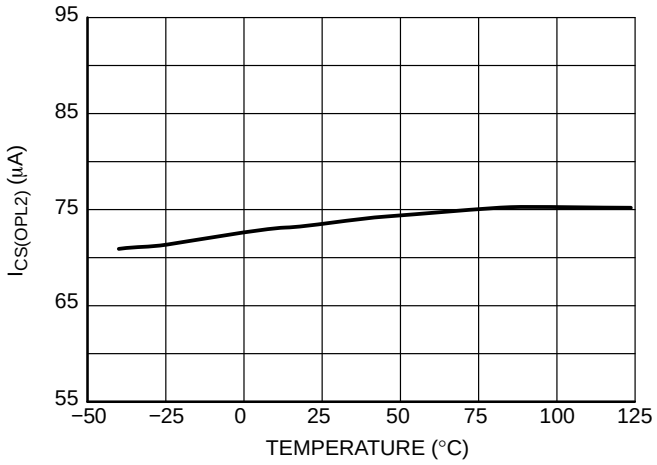

Figure 23. $I_{CS(OPL2)}$ vs. Temperature

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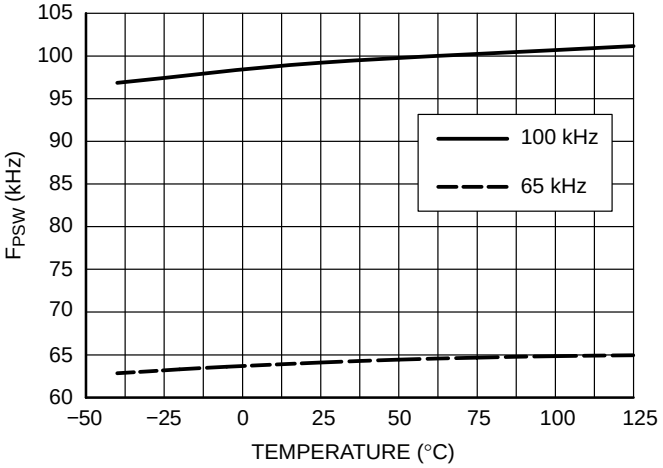

Figure 24. F_{PSW} vs. Temperature

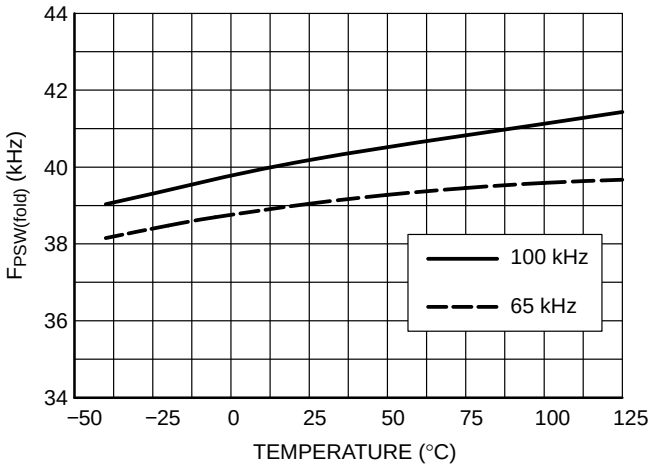

Figure 25. $F_{PSW(fold)}$ vs. Temperature

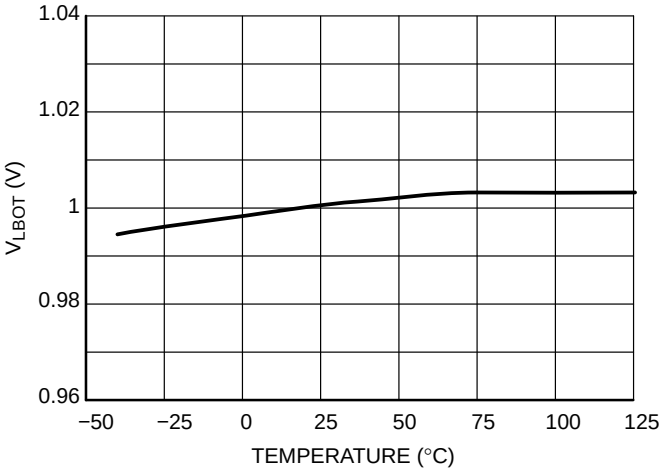

Figure 26. V_{LBOT} vs. Temperature

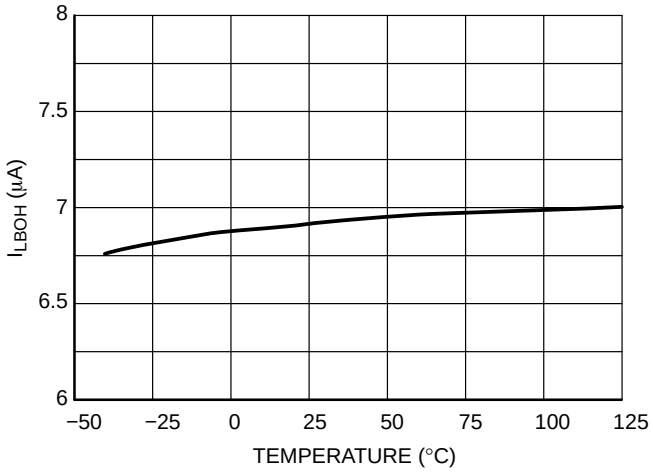

Figure 27. I_{LBOH} vs. Temperature

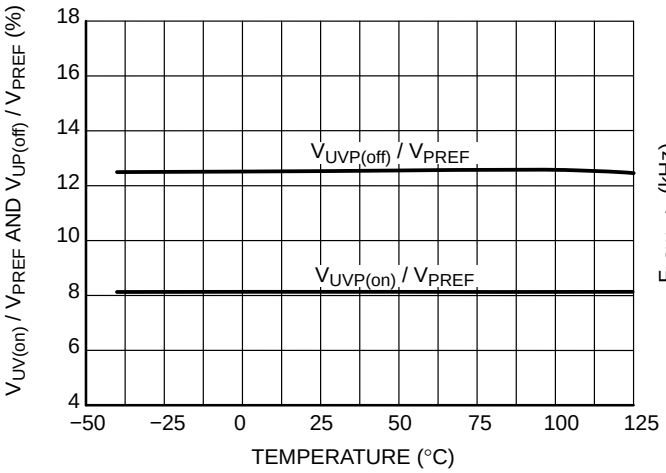

Figure 28. $V_{UVP(on)}/V_{PREF}$ and $V_{UVP(off)}/V_{PREF}$ vs. Temperature

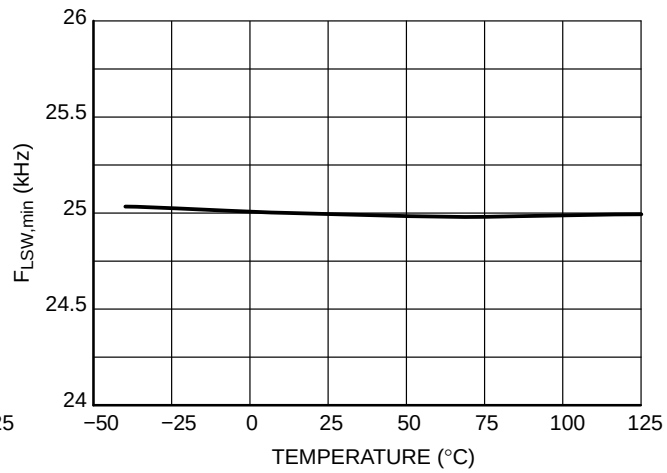

Figure 29. $F_{Lsw,min}$ vs. Temperature

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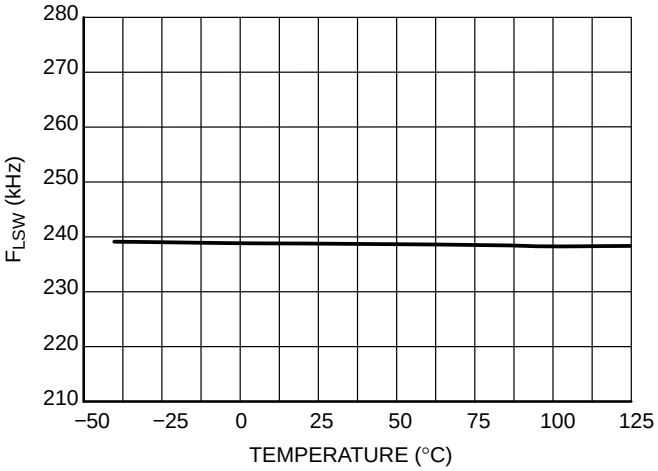

Figure 30. F_{Lsw} vs. Temperature

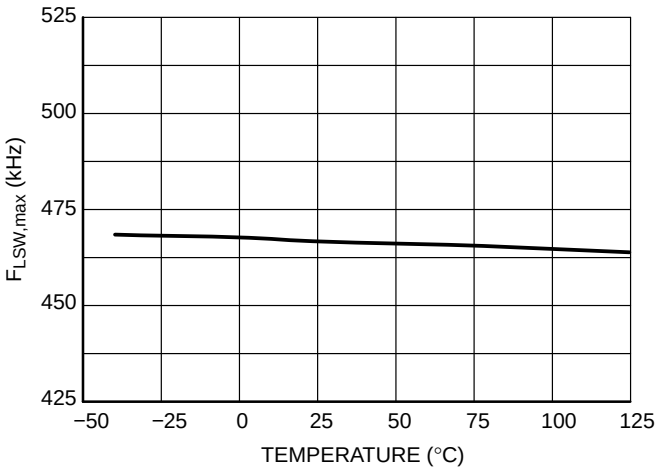

Figure 31. $F_{Lsw,max}$ vs. Temperature

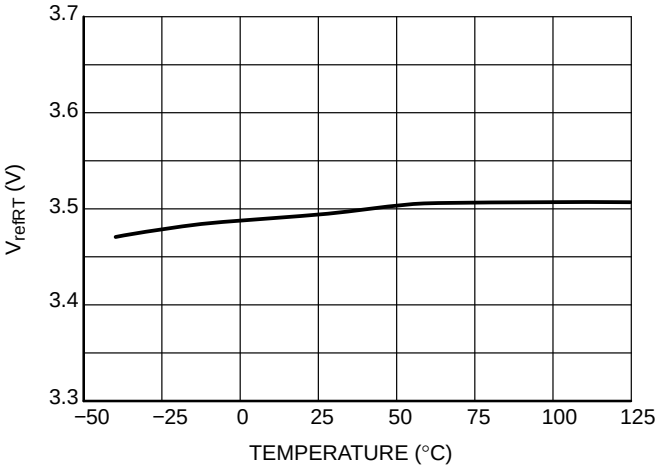

Figure 32. V_{refRt} vs. Temperature

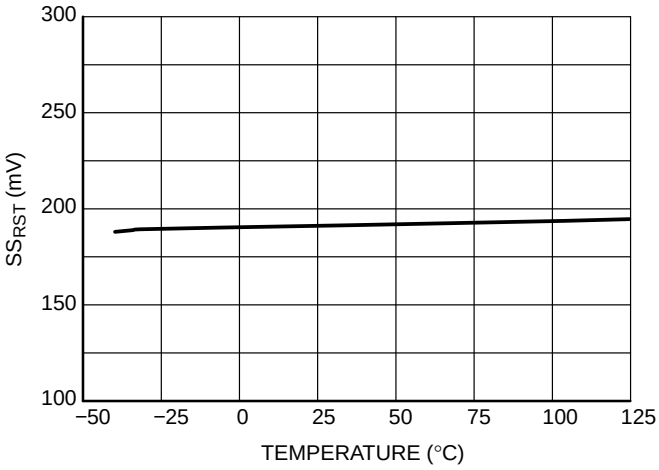

Figure 33. SS_{RST} vs. Temperature

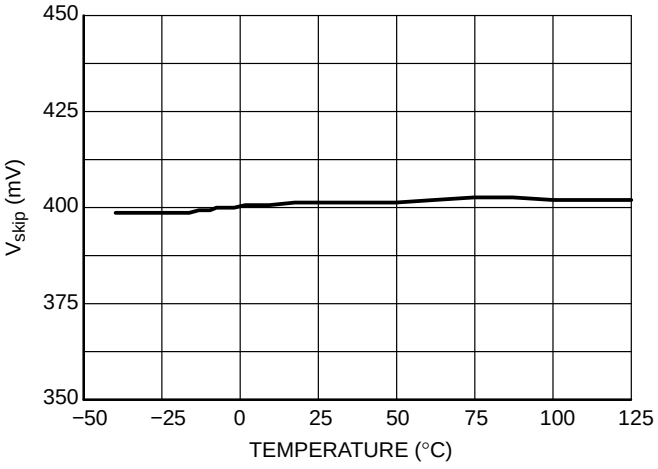

Figure 34. V_{skip} vs. Temperature

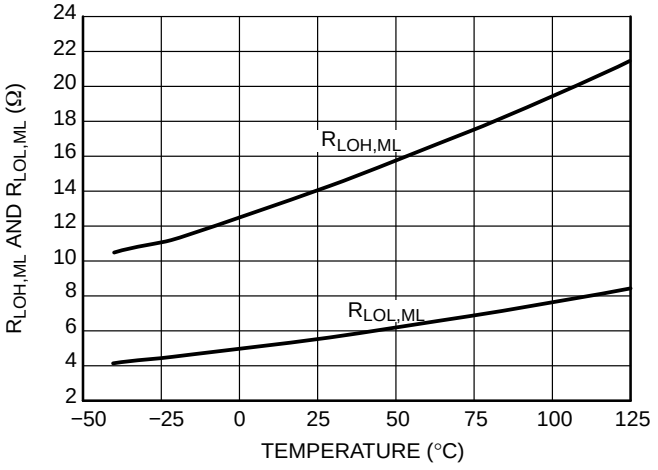

Figure 35. $R_{LOH,ML}$ and $R_{LOL,ML}$ vs. Temperature

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TYPICAL CHARACTERISTICS

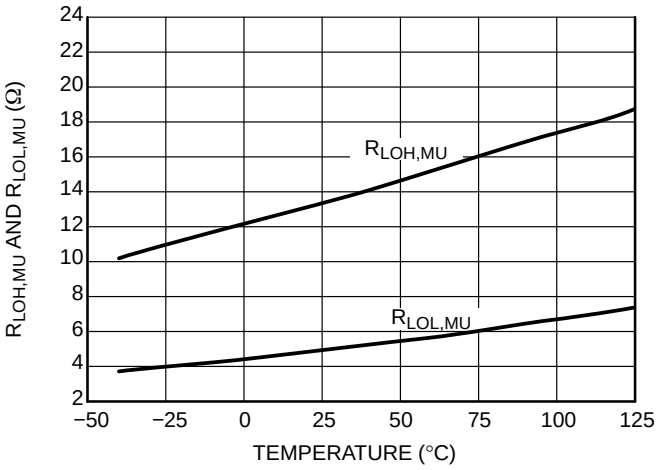

Figure 36. $R_{LOH,MU}$ and $R_{LOL,MU}$ vs. Temperature

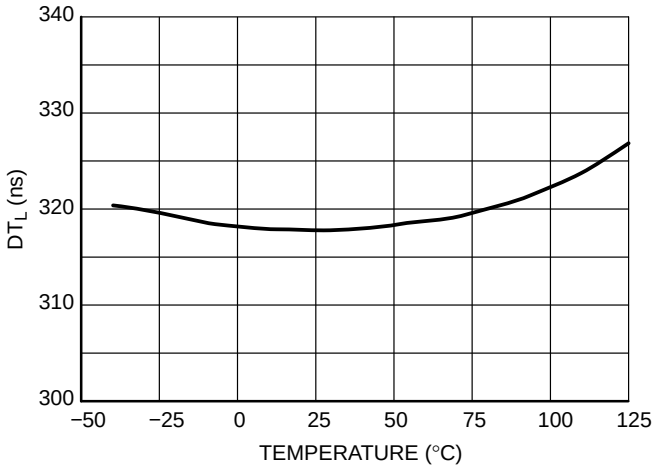

Figure 37. DT_L vs. Temperature

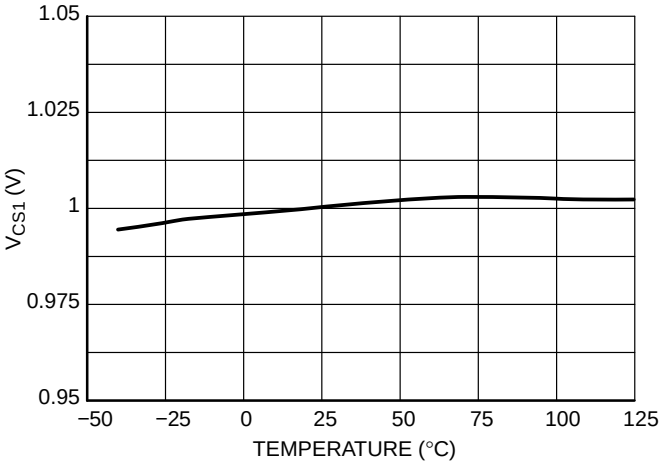

Figure 38. V_{CS1} vs. Temperature

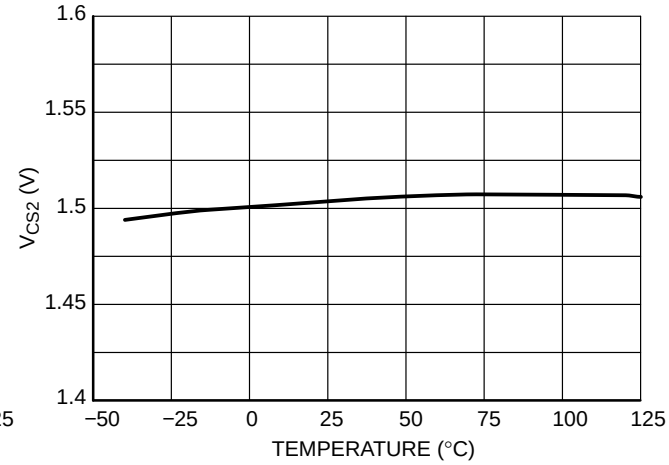

Figure 39. V_{CS2} vs. Temperature

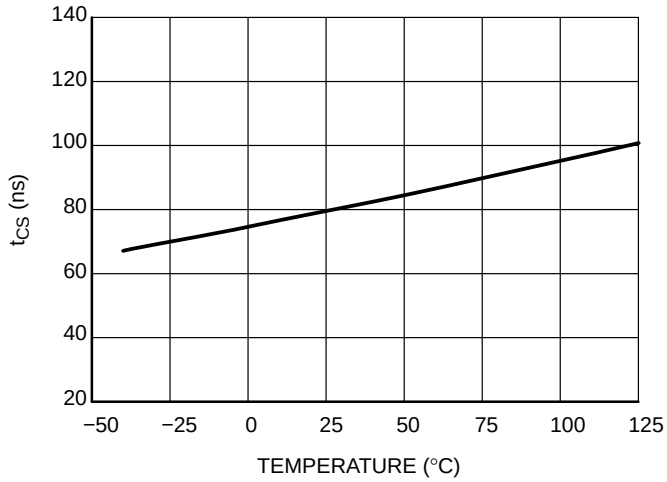

Figure 40. t_{CS} vs. Temperature

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APPLICATION INFORMATION

The NCP1910 represents a new generation of control circuit, associating two individual cores performing the functions of Continuous Conduction Mode (CCM) Power Factor Correction (PFC) and LLC resonant control. These cores interact together and implement handshake functions in normal operating conditions but also when a fault appears. Based on the ON Semiconductor proprietary high-voltage technology, the LLC section can drive the high-side MOSFET of the LLC half-bridge without the need of a gate-drive transformer.

Power Factor Correction

- **Compactness and Flexibility**: the NCP1910 requires a minimum of external components to perform a CCM PFC operation. In particular, the circuit scheme simplifies the PFC stage design. In addition, the circuit offers some functions like the line brown-out detection or true power limiting capability that enable the optimization of the PFC design.
- **Low Consumption and Shutdown Capability**: the NCP1910 is optimized to consume a small current in all operation modes. The consumed current is particularly reduced during the start-up phase and in shutdown mode so that the power losses are minimized when the circuit is disabled. This feature helps meet stringent stand-by low power specifications. Grounding the Feed-back pin can force the circuit to enter standby but the on/off pin can also serve this purpose.
- **Maximum Current Limit**: the circuit permanently senses the inductor current and immediately turns off the power switch if it is higher than the set current limit. The NCP1910 also prevents any turn on of the power switch as long as the inductor current is not below its maximum permissible level. This feature protects the MOSFET from possible excessive stress that could result from the switching of a current higher than the one the power switch is dimensioned for. In particular, this scheme effectively protects the PFC stage during the start-up phase when large in-rush currents charge the bulk capacitor.
- **Under-Voltage Protection for Open Loop Protection**: the circuit detects when the feed-back voltage goes below than about 8% of the regulation level. In this case, the circuit turns off and its consumption drops to a very low value. This feature protects the PFC stage from starting operation in case of low ac line conditions or in case of a failure in the feed-back network (i.e. bad connection). In case the UVP circuitry is activated, the Power Good signal is disabled and the LLC circuit stops immediately.
- **Fast Transient Response**: given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over or under-shoots because of abrupt load or input voltage variations (e.g. at start up). If the bulk voltage is too far from the regulation level:
  - **Over-Voltage Protection**: NCP1910 turns off the power switch as soon as V_{bulk} exceeds the OVP threshold (105% of the regulation level). This is an auto-recovery function.
  - **Dynamic Response Enhancer**: NCP1910 drastically speeds up the regulation loop by its internal 200 μA current source, activated when the bulk voltage drops below 95% of its regulation level.
- **Line Brown-Out Detection**: the circuit detects low ac line conditions and disables the PFC stage in this case. This protection mainly protects the power switch from the excessive stress that could damage it in such conditions.
- **Over-Power Limitation**: the NCP1910 computes the maximum permissible current in dependence of the average input voltage measured by the brown-out block. It is the second OCP with a threshold that is line dependent. When the circuit detects an excessive power transfer, it resets the driver output immediately.
- **Redundant Over-Voltage Protection**: As a redundant safety feature, the NCP1910 offers a second latched OVP whose input is available on OVP2 pin. If the voltage on this pin is above the maximum allowable voltage, the PFC and the LCC are latched off.
- **PFC Abnormal Protection**: When PFC faces an abnormal situation so that the bulk voltage is under regulation longer than the allowable timing, the PFC and LLC are latched off.
- **Frequency Foldback**: in light output loading conditions, the user has the ability to program a point on the V_{CTRL} pin where the oscillator frequency is gradually reduced. This helps to maintain an adequate efficiency on the PFC power stage alone.
- **Soft-Start**: to offer a clean start-up sequence and limit both the stress on the power MOSFET and the bulk voltage overshoot, a 30 μA current source charges the compensation network installed on V_{CTRL} pin and makes V_{CTRL} raise gradually.
- **Output Stage Totem Pole**: the NCP1910 incorporates a ±1.0 A gate driver to efficiently drive TO220 or TO247 power MOSFETs.

LLC Controller

- **Wide Frequency Operation**: the part can operate to a frequency up to 500 kHz by connecting a resistive network from R_t pin to ground. One resistor sets the maximum switching frequency whereas a second resistor set the minimum frequency.
- **On Board Dead Time**: to eliminate the shoot-through on the half-bridge leg, a dead time is included in the controller (see DT_L parameter).
- **Soft-Start**: a dedicated pin discharges a capacitor to ground upon start-up to offer a smooth output voltage ramp up. The start-up frequency is the maximum set by

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the resistor connected between R_t pin and SS pin. The capacitor connected from R_t pin to ground fixes the soft start duration. In fault mode, when the voltage on CS/FF pin exceeds a typical value of 1 V, the soft-start pin is immediately discharged and a re-start at high frequency occurs.

- **Skip Cycle Operation**: to avoid any frequency runaway in light conditions but also to improve the standby power consumption, the NCP1910B welcomes a skip input (Skip pin) which permanently observes the opto-coupler collector. If this pin senses a low voltage, it cuts the LLC output pulses until the collector goes up again. The NCP1910A does not offer the skip capability and routes the analog ground on pin 16 instead.
- **High-Soltage Drivers**: capitalizing on ON Semiconductor technology, the LLC controller includes a high-voltage section allowing a direct connection to the high-voltage rail. The MOSFET leg can therefore be directly driven without using a gate-drive transformer.
- **Fault Protection**: as explained in the above lines, the CS/FF pin combines a two-level protection circuit. If the level crosses the first level (1 V), the LLC converter immediately increases its switching frequency to the maximum set by the external resistive divider connected on R_t pin. This is an auto-recovery protection mode. In case the fault is more severe, the signal on the CS/FF pin crosses the second threshold (1.5 V) and latches off the whole combo controller. Reset occurs via an UVLO detection on V_{CC}, a reset on the on/off pin or a brown-out detection on the PFC stage. This latter confirms that the user has unplugged and re-plugged the power supply.

Combo Management

- **Start-Up Delay**: the PFC start-up sequence often generates an output overshoot followed by damped oscillations. To make sure the PFC output voltage is fully stabilized before starting the LLC converter, a 20 ms delay is inserted after the internal PFC_ok signal is asserted. This delay is always reset when the combo is started from a V_{CC} ULVO, line brown-out condition or via the on/off pin.
- **Power Good Signal**: the power good signal (PG) is intended to instruct the downstream circuitry installed on the isolated secondary side that the combo is working. Once the PFC has started, an internal “PFC_OK” signal is asserted. 20 ms later, the PG pin is brought low. This signal can now disappear in two cases: the bulk voltage decreases to an abnormal level, programmed by a reference voltage imposed on PG_{adj} pin. This level is usually above the LLC turn-off voltage, programmed by BO_{adj} pin. Therefore, in a normal turn-off sequence, PG first drops and signals the secondary side that it must be prepared for shutdown. The second event that can drop the PG signal is when the PFC experiences a fault: broken feedback path, severe overload. In this case, the PG signal is immediately asserted high and a 5 ms timer starts. Once this timer is elapsed, the LLC converter can be safely halted.
- **Latched Event**: in the event of a severe operating condition, the PFC can be latched (OVP2 pin) and/or the LLC controller also (CS/FF pin). In either case, the whole combo controller is locked and can only be reset via a V_{CC} UVLO, line brown-out or a level transition on pin on/off.
- **Thermal Shutdown**: an internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 140 °C typically. The circuit resumes operation once the temperature drops below about 110 °C (30 °C hysteresis).

Principle of NCP1910 Scheme

PFC Section

A CCM PFC boost converter is shown in Figure 41. The input voltage is a rectified 50 Hz or 60 Hz sinusoidal signal. The MOSFET is switching at a high frequency (typically 65 kHz in NCP1910) so that the inductor current I_L basically consists of high and low-frequency components.

Filter capacitor C_{in} is an essential and very small value capacitor in order to eliminate the high-frequency component of the inductor I_L. This filter capacitor cannot be too bulky because it can pollute the power factor by distorting the rectified sinusoidal input voltage.

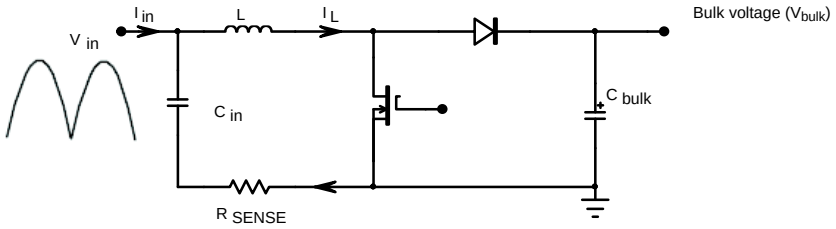

Figure 41. CCM PFC Boost Converter

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PFC Methodology

The NCP1910 uses a proprietary PFC methodology particularly designed for CCM operation. The PFC methodology is described in this section.

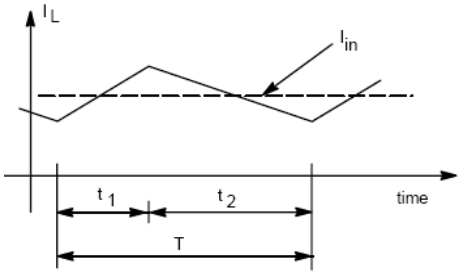

Figure 42. Inductor Current in CCM

As shown in Figure 42, the inductor current I_L in a switching period T includes a charging phase for duration t_1 and a discharging phase for duration t_2. The voltage conversion ratio is obtained in Equation 1.

$$\frac{V_{bulk}}{V_{in}} = \frac{t_1 + t_2}{t_2} = \frac{T}{T - t_1} \qquad \text{(eq. 1)}$$

$$V_{in} = \frac{T - t_1}{T} V_{bulk}$$

Where:

- V_{bulk} is the output voltage of PFC stage,
- V_{in} is the rectified input voltage,
- T is the switching period,
- t_1 is the MOSFET on time, and
- t_2 is the MOSFET off time.

The input filter capacitor C_{in} and the front-ended EMI filter absorbs the high-frequency component of inductor current I_L. It makes the input current I_{in} a low-frequency signal only of the inductor current.

$$I_{in} = I_{L-50} \qquad \text{(eq. 2)}$$

Where:

- I_{in} is the input AC current.
- I_L is the inductor current.
- I_{L-50} supposes a 50 Hz operation. The suffix 50 means it is with a 50 Hz bandwidth of the original I_L.

From Equations 1 and 2, the input impedance Z_{in} is formulated.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{T - t_1}{T} \frac{V_{bulk}}{I_{L-50}} \qquad \text{(eq. 3)}$$

where: Z_{in} is input impedance.

Power factor is corrected when the input impedance Z_{in} in Equation 3 is constant or varies slowly in the 50 or 60 Hz bandwidth.

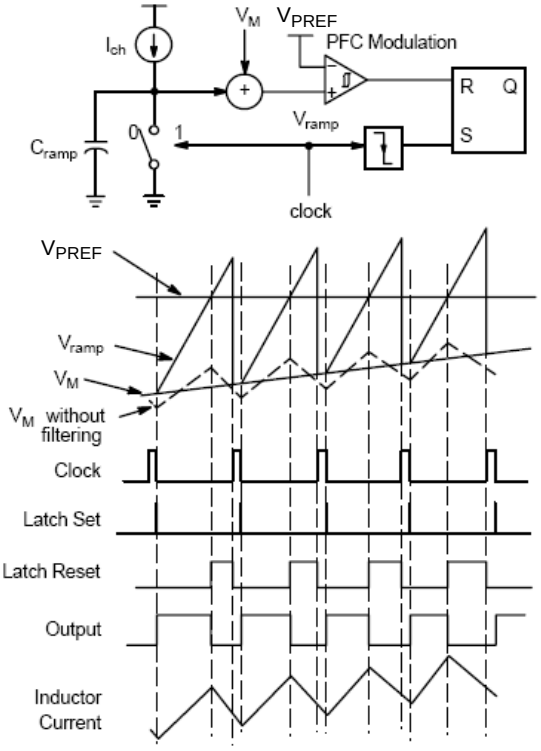

Figure 43. PFC Duty Modulation and Timing Diagram

The PFC modulation and timing diagram is shown in Figure 43. The MOSFET on time t_1 is generated by the intersection of reference voltage V_{PREF} and ramp voltage V_{ramp}. A relationship in Equation 4 is obtained.

$$V_{ramp} = V_M + \frac{I_{ch} t_1}{C_{ramp}} = V_{PREF} \qquad \text{(eq. 4)}$$

Where:

- V_{ramp} is the internal ramp voltage, the positive input of the PFC modulation comparator,
- V_M is the multiplier voltage appearing on V_M pin,
- I_{ch} is the internal charging current,
- C_{ramp} is the internal ramp capacitor, and
- V_{PREF} is the internal reference voltage, the negative input of the PFC modulation comparator.

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I_{ch}, C_{ramp}, and V_{PREF} also act as the ramp signal of switching frequency. Hence the charging current I_{ch} is specially designed as in Equation 5. The multiplier voltage V_M is therefore expressed in terms of t_1 in Equation 6.

$$I_{ch} = \frac{C_{ramp} V_{PREF}}{T} \quad \text{(eq. 5)}$$

$$V_M = V_{PREF} - \frac{t_1}{C_{ramp}} \frac{C_{ramp} V_{PREF}}{T} = V_{PREF} \frac{T - t_1}{T} \quad \text{(eq. 6)}$$

From Equation 3 and Equation 6, the input impedance Z_{in} is re-formulated in Equation 7.

$$Z_{in} = \frac{V_M}{V_{PREF}} \frac{V_{bulk}}{I_{L-50}} \quad \text{(eq. 7)}$$

Because V_{PREF} and V_{bulk} are roughly constant versus time, the multiplier voltage V_M is designed to be proportional to the I_{L-50} in order to have a constant Z_{in} for PFC purpose. It is illustrated in Figure 44.

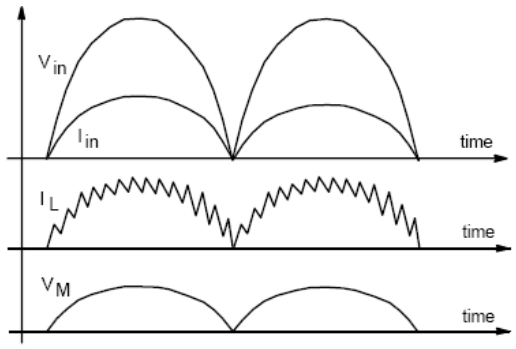

Figure 44. Multiplier Voltage Timing Diagram

It can be seen in the timing diagram in Figure 43 that V_M originally consists of a switching frequency ripple coming from the inductor current I_L. The duty ratio can be inaccurately generated due to this ripple. This modulation is the so-called “peak current mode”. Hence, an external capacitor C_M connected to the multiplier voltage V_M pin is essential to bypass the high-frequency component of V_M. The modulation becomes the so-called “average current mode” with a better accuracy for PFC.

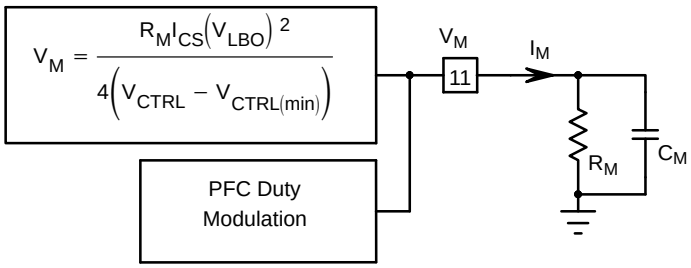

Figure 45. The Multiplier Voltage Pin Configuration

The multiplier voltage V_M is generated according to Equation 8.

$$V_M = \frac{R_M I_{CS} (V_{LBO})^2}{4(V_{CTRL} - V_{CTRL(min)})} \quad \text{(eq. 8)}$$

Where:

- R_M is the external multiplier resistor connected to V_M pin, which is constant.
- V_{LBO} is the input voltage signal appearing on the LBO pin, which is proportional to the rms input voltage,
- I_{CS} is the sense current proportional to the inductor current I_L as described in Equation 13.
- V_{CTRL} is the control voltage signal, the output voltage of Operational Trans-conductance Amplifier (OTA), as described in Equation 17.
- $V_{CTRL(min)}$ is not only the minimum operating voltage of V_{CTRL} but also the offset voltage for the PFC current modulation.

R_M directly limits the maximum input power capability. Also, due to the V_{in}^2 feed-forward feature, where the V_{LBO} is squared, the transfer function and the power delivery is independent from the ac line level. The relationship between V_{CTRL} and power delivery will be depicted later on.

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Line Brown-Out Protection

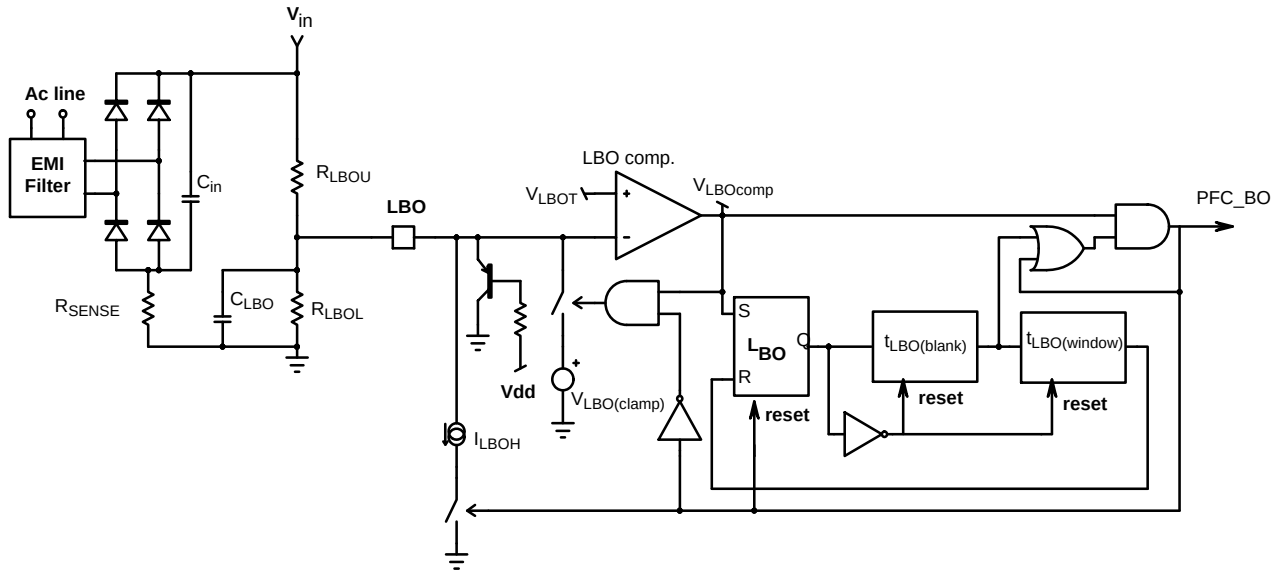

Figure 46. The Line Brown-Out Configuration

As shown in Figure 46, the Line Brown-Out pin (represented LBO pin) as receives a portion of the input voltage (V_{in}). As V_{in} is a rectified sinusoid, a capacitor must integrate the ac line ripple so that a voltage proportional to the average value of V_{in} is applied to the brown-out pin.

The main function of the LBO block is to detect too low input voltage conditions. A 7 μA current source lowers the LBO pin voltage when a brown-out condition is detected. This is for hysteresis purpose as required by this function.

In nominal operation, the voltage applied to LBO pin must be above the internal reference voltage, V_{LBOT} (1 V typically). In this case, the output of the LBO comparator $V_{LBOcomp}$ is low.

Conversely, if V_{LBO} goes below 1 V, $V_{LBOcomp}$ turns high and a 980 mV voltage source, $V_{LBO(clamp)}$, is connected to the LBO pin to maintain the pin level near 1 V. Then a 50 ms blanking delay, $t_{LBO(blank)}$, is activated during which no fault is detected. The main goal of the 50 ms lag is to help meet the hold-up requirements. In case of a short mains interruption, no fault is detected and hence, both PFC and LLC keep operating. In addition, LBO pin being kept at 980 mV, there is almost no extra delay between the line recovery and the occurrence of a proper voltage applied to LBO pin, that otherwise would exist because of the large capacitor typically placed between LBO pin and ground to filter the input voltage ripple. As a result, the NCP1910 effectively “blanks” any mains interruption that is shorter than 25 ms (minimum guaranteed value of the 50 ms timer).

At the end of this blanking delay ($t_{LBO(blank)}$), another timer is activated that sets a 50 ms window during which a fault can be detected. This is the role of the $t_{LBO(window)}$ in Figure 46:

- If $V_{LBOcomp}$ is high during the second 50 ms delay ($t_{LBO(window)}$), a line brown-out condition is confirmed and PFC_BO signal is asserted high.
- If $V_{LBOcomp}$ remains low for the duration of the $t_{LBO(window)}$, no fault is detected.

When the PFC_BO signal is high:

- The PFC driver is disabled, and the V_{CTRL} pin is grounded to recover operation with a soft-start when the fault has gone.
- The $V_{LBO(clamp)}$ voltage source is removed from LBO pin.
- The I_{LBOH} current source (7 μA typically) is enabled that lowers the LBO pin voltage for hysteresis purpose.

At startup, a pnp transistor ensures that the LBO pin voltage remains below when: V_{CC} < UVLO or ON/OFF pin is released open or UVP or Thermal Shutdown. This is to guarantee that the circuit starts operation in the right state, which is “PFC_BO” high. When the NCP1910 is ready to work, the pnp transistor turns off and the circuit enables the I_{LBOH}.

Also, I_{LBOH} is enabled whenever the part is in off mode, but at startup, I_{LBOH} is disabled until V_{CC} reaches $V_{CC(on)}$.

Line Brown-Out Network Calculation

If the line brown-out network is connected to the voltage after bridge diode, the monitored voltage can be very different depending on the phase:

- Before operation, the PFC stage is off and the input bridge acts as a peak detector. As a consequence, the input voltage is approximately flat and nearly equates the ac

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line amplitude: $<V_{in}> = \sqrt{2}\,V_{ac,rms}$, where $V_{ac,rms}$ is the rms voltage of the line. As depicted in previous section, the I_{LBOH} turns on before PFC operates for the purpose of adjustable line brown-out hysteresis; hence, the average voltage applied to LBO pin is:

$$V_{LBO} = \sqrt{2}\,V_{ac,rms}\frac{R_{LBOL}}{R_{LBOU} + R_{LBOL}} - I_{LBOH} \cdot \frac{R_{LBOU} \cdot R_{LBOL}}{R_{LBOU} + R_{LBOL}}$$

If $R_{LBOL} << R_{LBOU}$,

$$V_{LBO} \simeq \sqrt{2}\,V_{ac,rms}\frac{R_{LBOL}}{R_{LBOU} + R_{LBOL}} - I_{LBOH}R_{LBOL} \quad \text{(eq. 9)}$$

- After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the average voltage becomes $<V_{in}> = (2/\pi)\sqrt{2}\,V_{ac,rms}$, which decays $2/\pi$ of the peak value of rms input voltage. Hence, the average voltage applied to LBO pin is: $<V_{LBO}> = (2/\pi)\sqrt{2}\,V_{ac,rms}\,R_{LBOL}/(R_{LBOU} + R_{LBOL})$. And because of the ripple on the LBO pin, the minimum value of V_{LBO} is around:

$$V_{LBO} = \frac{2}{\pi}\sqrt{2}\,V_{ac,rms}\frac{R_{LBOL}}{R_{LBOU} + R_{LBOL}} \times \left(1 - \frac{f_{LBO}}{3f_{line}}\right) \quad \text{(eq. 10)}$$

Where:

- f_{LBO} is the sensing network pole frequency.

$$f_{LBO} = \frac{R_{LBOU} + R_{LBOL}}{2\pi R_{LBOU}R_{LBOL}C_{LBO}}$$

- f_{line} is the line frequency.
- R_{LBOL} is low side resistor of the dividing resistors between LBO pin and ground.
- R_{LBOU} is upper side resistor of the dividing resistors between V_{in} and LBO pin.

The term $1 - \frac{f_{LBO}}{3f_{line}}$ of Equation 10 enables to take into account the LBO pin voltage ripple (first approximation).

If as a rule of the thumb, we will assume that $f_{LBO} = \frac{f_{line}}{10}$.

Re-arranging the Equation 9 and 10, the network connected to LBO pin can be calculated with the following equations:

$$R_{LBOL} = \left(\frac{1}{1 - \frac{f_{LBO}}{3f_{line}}} \cdot \frac{\pi}{2} \cdot \frac{V_{ac,on}}{V_{ac,off}} - 1\right) \cdot \frac{V_{LBOT}}{I_{LBOH}} \quad \text{(eq. 11)}$$

$$\cong \left(\frac{1}{0.967} \cdot \frac{\pi}{2} \cdot \frac{V_{ac,on}}{V_{ac,off}} - 1\right) \cdot \frac{V_{LBOT}}{I_{LBOH}}$$

$$R_{LBOU} = \left(\frac{\sqrt{2} \cdot V_{ac,on}}{I_{LBOH}R_{LBOL} + V_{LBOT}} - 1\right)R_{LBOL} \quad \text{(eq. 12)}$$

Where:

- $V_{ac,on}$ is the rms ac voltage to starts PFC operating.
- $V_{ac,off}$ the rms ac voltage for line brown-out detection.

PFC Current Sense

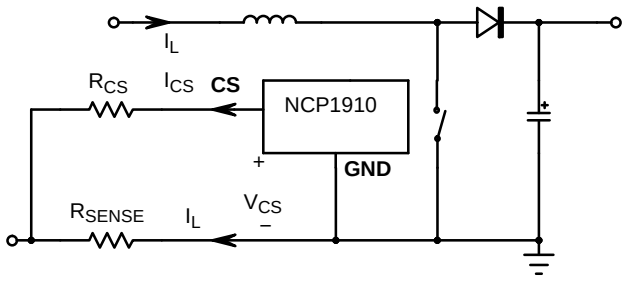

Figure 47. PFC Current Sensing Configuration

The device senses the inductor current I_L by the current sense scheme in Figure 47. The device maintains the voltage at CS pin to be zero voltage, i.e. $V_{CS} = 0$ V, so that

$$I_{CS} = \frac{R_{SENSE}}{R_{CS}}I_L \quad \text{(eq. 13)}$$

Where:

- R_{SENSE} is the sense resistor to sense I_L.
- R_{CS} is the offset resistor between CS pin and R_{SENSE}.

This scheme has the advantage of the minimum number of components for current sensing. The sense current I_{CS} represents the inductor current I_L and will be used in the PFC duty modulation to generate the multiplier voltage V_M, Over-Power Limitation (OPL), and Over-Current Protection. Equation 13 would insist in the fact that it provides the flexibility in the R_{SENSE} choice and that it allows to detect in-rush currents.

PFC Over-Current Protection (OCP)

PFC Over-current Protection is reached when I_{CS} is larger than $I_{S(OCP)}$ (200 μA typical). The offset voltage of the CS pin is typical 10 mV and it is neglected in the calculation. Hence, the maximum OCP inductor current threshold $I_{L(OCP)}$ is obtained in Equation 14.

$$I_{L(OCP)} = \frac{R_{CS}I_{S(OCP)}}{R_{SENSE}} = \frac{R_{CS}}{R_{SENSE}} \times 200\ \mu A \quad \text{(eq. 14)}$$

When over-current protection threshold is reached, the PFC drive goes low. The device automatically resumes operation when the inductor current goes below the threshold.

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PFC Over-Power Limitation (OPL)

This is a second OCP with a threshold that is line dependent. Sense current I_{CS} represents the inductor current I_L and hence represents the input current approximately. Input voltage signal V_{LBO} represents the rms input voltage. The product ($I_{CS} \times V_{LBO}$) represents an approximated input power ($I_L \times V_{ac}$). It is illustrated in Figure 48.

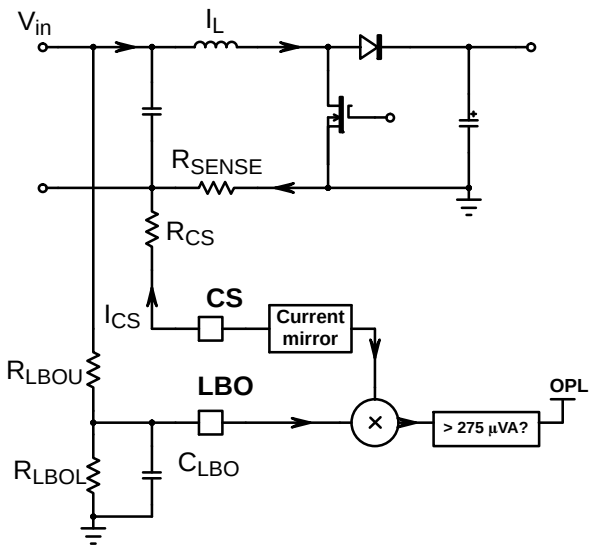

Figure 48. PFC Over-Power Limitation Configuration

When the product ($I_{CS} \times V_{LBO}$) is greater than a permissible level 275 μVA, the device turns off the PFC driver so that the input power is limited. The OPL is automatically deactivated when the product ($I_{CS} \times V_{LBO}$) is lower than the 275 μVA level. This 275 μVA level corresponds to the approximated input power ($I_L \times Vac$) to be smaller than the particular expression in Equation 15.

$$I_{CS} V_{LBO} < 275\ \mu VA$$

$$\left(I_L \frac{R_{SENSE}}{R_{CS}}\right) \times \left(\frac{2\sqrt{2} K_{LBO}}{\pi} \cdot V_{ac}\right) < 275\ \mu VA \quad \text{(eq. 15)}$$

$$I_L \cdot V_{ac} < \frac{R_{CS} \cdot \pi}{R_{SENSE} \cdot K_{LBO}} \cdot 97\ \mu VA$$

Where

$$K_{LBO} = \frac{R_{LBOL}}{R_{LBOU} + R_{LBOL}}$$

PFC Reference Section

The internal reference voltage (V_{PREF}) is trimmed to be ±2% accurate over the temperature range (the typical value is 2.5 V). V_{PREF} is the reference used for the regulation of PFC section.

PFC Feedback and Compensation

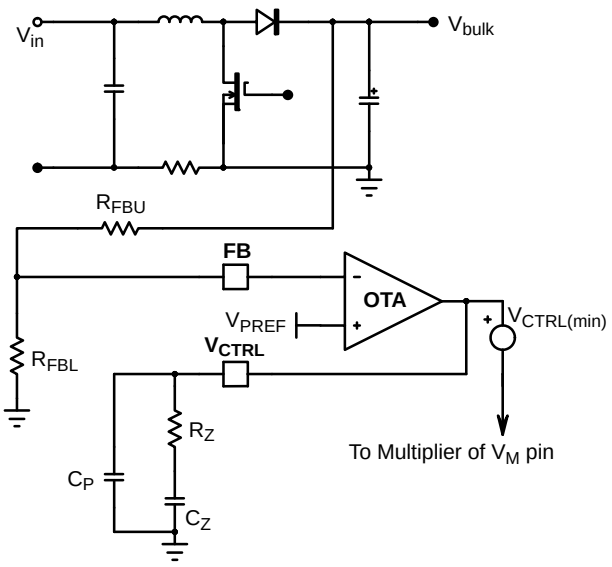

Figure 49. V_{CTRL} Type-2 Compensation

The output voltage V_{bulk} of the PFC circuits is sensed at FB pin via the resistor divider (R_{FBL} and R_{FBU}) as shown in Figure 49. V_{bulk} is regulated as described in Equation 16.

$$V_{bulk} = V_{PREF} \frac{R_{FBU} + R_{FBL}}{R_{FBL}} \quad \text{(eq. 16)}$$

The feedback signal V_{FB} represents the output voltage V_{bulk} and will be used in the output voltage regulation, Over-Voltage Protection (OVP), fast transient response, and Under-Voltage Protection (UVP)

The Operational Trans-conductance Amplifier (OTA) constructs a control voltage, V_{CTRL}, depending on the output power and hence V_{bulk}. The operating range of V_{CTRL} is from $V_{CTRL(min)}$ to $V_{CTRL(max)}$. The signal used for PFC duty modulation is after decreasing a offset voltage, $V_{CTRL(min)}$, i.e. $V_{CTRL} - V_{CTRL(min)}$.

This control voltage V_{CTRL} is a roughly constant voltage that comes from the PFC output voltage V_{bulk} that is a slowly varying signal. The bandwidth of V_{CTRL} can be additionally limited by inserting the external type-2 compensation components (that are R_Z, C_Z, and C_P as shown in Figure 49). It is recommended to limit cross over frequency of open loop system below 20 Hz typically if the input ac voltage is 50 Hz to achieve power factor correction purpose.

The transformer of V_{bulk} to V_{CTRL} is as described in Equation 16 if $C_Z >> C_P$. G_{EA} is the error amplifier gain.

$$\frac{V_{CTRL}}{V_{bulk}} = \frac{R_{FBL} \cdot G_{EA} R_Z}{R_{FBL} + R_{FBU}} \cdot \frac{1 + sR_ZC_Z}{sR_ZC_Z(1 + sR_ZC_P)} \quad \text{(eq. 17)}$$

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PFC Power Analysis and V_{in}^2 Feed-Forward

From Equation 7 through 13, the input impedance Z_{in} is re-formulated in Equation 18.

$$Z_{in} = \frac{2R_M R_{SENSE} \cdot K_{LBO}^{\ 2} \cdot V_{ac}^{\ 2} \cdot V_{bulk} I_L}{\pi^{\ 2} R_{CS} \cdot \left(V_{CTRL} - V_{CTRL(min)}\right) \cdot V_{PREF} I_{L-50}} \quad \text{(eq. 18)}$$

When I_L is equal to I_{L-50}, Equation 18 is re-formulated in Equation 19.

$$Z_{in} = \frac{2R_M R_{SENSE} \cdot K_{LBO}^{\ 2} \cdot V_{ac}^{\ 2} \cdot V_{bulk}}{\pi^{\ 2} R_{CS} \cdot \left(V_{CTRL} - V_{CTRL(min)}\right) \cdot V_{PREF}} \quad \text{(eq. 19)}$$

The multiplier capacitor C_M is the one to filter the high-frequency component of the multiplier voltage V_M. The high-frequency component is basically coming from the inductor current I_L. On the other hand, the input filter capacitor C_{in} similarly removes the high-frequency component of inductor current I_L. If the capacitors C_M and C_{in} match with each other in terms of filtering capability, I_L becomes I_{L-50}. Input impedance Z_{in} is roughly constant over the bandwidth of 50 or 60 Hz and power factor is corrected.

Input and output power (P_{in} and P_{out}) are derived in Equations 20 and 21 when the circuit efficiency η is obtained or assumed. The variable V_{ac} stands for the rms input voltage.

$$P_{in} = \frac{V_{ac}^{\ 2}}{Z_{in}} = \frac{\pi^{\ 2} \cdot R_{CS} \cdot \left(V_{CTRL} - V_{CTRL(min)}\right) \cdot V_{PREF}}{2R_M R_{SENSE} K_{LBO}^{\ 2} \cdot V_{bulk}}$$

$$\propto \frac{\left(V_{CTRL} - V_{CTRL(min)}\right)}{V_{bulk}} \quad \text{(eq. 20)}$$

$$P_{in} = \eta P_{in} = \eta \frac{\pi^2 \cdot R_{CS} \cdot \left(V_{CTRL} - V_{CTRL(min)}\right) \cdot V_{PREF}}{2R_M R_{SENSE} K_{LBO}^{\ 2} \cdot V_{bulk}}$$

$$\propto \frac{\left(V_{CTRL} - V_{CTRL(min)}\right)}{V_{bulk}} \quad \text{(eq. 21)}$$

Because of the V_{in}^2 feed-forward, the power delivery is independent from input voltage. Hence the transfer function of power stage is independent from input voltage, which easies the compensation loop design.

PFC Frequency Foldback

NCP1910 implements frequency foldback feature on PFC section to improve the efficiency at light load. Thanks to V_{in}^2 feed-forward feature, the output power is proportional to the (V_{CTRL} − $V_{CTRL(min)}$). The PFC frequency foldback is hence done by comparing (V_{CTRL} − $V_{CTRL(min)}$) with V_{fold}, the voltage on Fold pin.

The simplified block diagram of PFC frequency foldback feature is depicted in Figure 50.

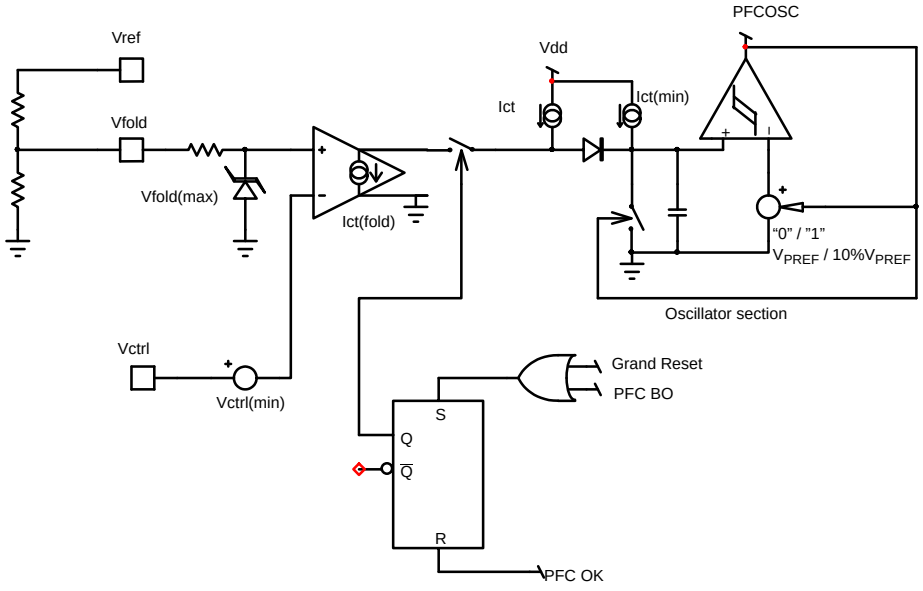

Figure 50. The PFC Frequency Foldback Block

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Where:

- $I_{Ct(min)}$ limits the minimum operating frequency.
- I_{Ct} and $I_{Ct(min)}$ provide the charging current for oscillator and hence control the nominal operating frequency.
- V_{fold} determines the power level at which the frequency foldback starts.
- $I_{Ct(fold)}$ steals the I_{Ct} and hence reduces the operating frequency according to the error information between V_{fold} and (V_{CTRL} − $V_{CTRL(min)}$).
- The transient slope of frequency foldback vs. V_{CTRL} is fixed inside.
- $V_{fold(max)}$ is to limit the maximum power level of frequency foldback, which is around 2 V typically.

The frequency foldback is disabled at start-up, i.e. before the PFCok signal in Figure 50 is asserted high.

The user can adjust the power level at which the frequency foldback starts by adjust the resistor divider between V_{REF} pin and fold pin. Also, the frequency foldback can be disabled by grounding fold pin.

The relationship between operating frequency and V_{CTRL} is depicted in Figure 51.

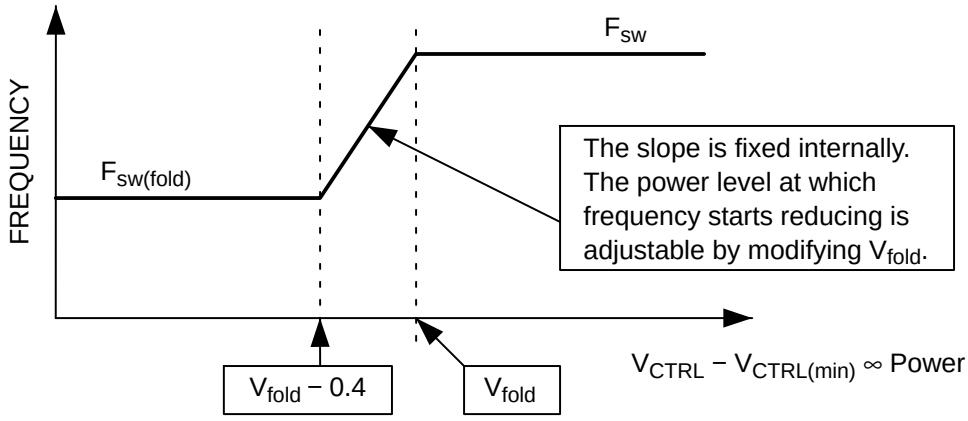

Figure 51. The Relationship between Frequency and V_{CTRL}

PFC Power Boost

As depicted in previous section, thanks to the V_{in}^2 feed-forward, the power delivery is independent from input voltage. It brings benefit of good power factor and a direct control on the frequency foldback. However, in some special case such as when the ac input voltage drops sharply from high line to low line, the power will be limited because the filter on LBO pin slows down the reaction speed to follow up the change on input voltage. In the end, the bulk voltage might drop too low and stop the LLC converter.

Hence, NCP1910 builds a so-called PFC power boost function inside. The idea is to pull down LBO pin to 2 V typically, $V_{LBO(PD)}$, when

- V_{LBO} is above 2 V, $V_{LBO(PD)}$, i.e. the input is at high line, and
- V_{CTRL} is at maximum for more than timer defined by $t_{PFCflag}$, and,
- V_{bulk} is under 95% of nominal output, i.e. VLD is triggered.

The maximum pulling-down duration is defined by $t_{LBO(PDlimit)}$, which is 5 ms typically. A blanking timer, $t_{LBO(PDblank)}$, is to avoid this power boost function reacting too soon, which is about 77 ms typically. The PFC power boost function is inhibited at start-up until bulk voltage is above 95% of nominal output.

PFC Skip Mode

In order to ensure a proper regulation in no load conditions, the circuit skips cycles when V_{CTRL} is at its minimum level. V_{CTRL} is maintained between about 0.6 V and 3.6 V due to the internal active clamps. A skip sequence occurs as long as the 0.6 V clamp circuitry is triggered and switching operations is recovered when the clamp is inactive.

Fast Transient Response

Given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over or under-shoots because of abrupt load or input voltage variations (such as start-up duration). As shown in Figure 52, if the output voltage is out of regulation, NCP1910 has 2 functions to maintain the output voltage regulation.

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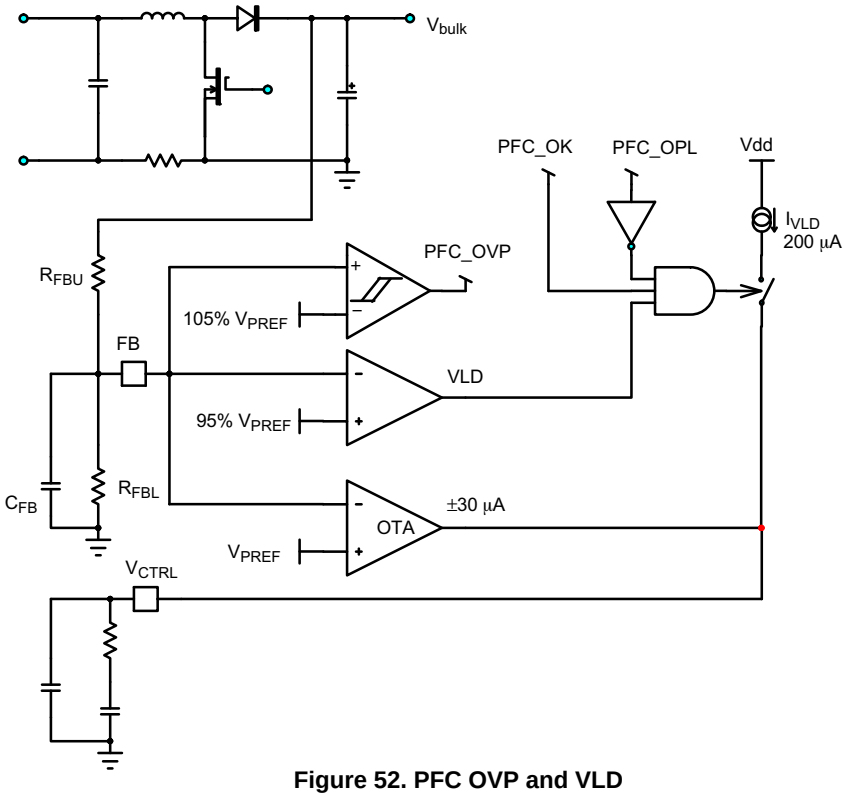

Figure 52. PFC OVP and VLD

- **Over-Voltage Protection (OVP)**: When V_{FB} is higher than 105% of V_{PREF} (i.e. V_{bulk} > 105% of nominal bulk voltage), the PFC driver output goes low for protection. The circuit automatically resumes operation when V_{FB} becomes lower than 103.2% of V_{PREF}, i.e. around 44 mV hysteresis in the OVP comparator. If the nominal V_{bulk} is set at 390 V, then the maximum bulk voltage is 105% of 390 V = 410 V. Hence a cost and size effective bulk capacitor of lower voltage rating is suitable for this application,
- **Voltage-Low Detection (VLD)**: NCP1910 drastically speeds up the regulation loop by its internal 200 μA enhanced current source when the bulk voltage is below 95% of its regulation level. Under normal condition, the maximum sink and source of output current capability of OTA is around 30 μA. Due to the "V_{out} Low Detect" block (VLD), when the V_{FB} is below 95% V_{PREF}, an extra 200 μA current source (I_{VLD} in Figure 52) will raise V_{CTRL} rapidly. Hence prevent the PFC output from dropping too low and improve the transient response performance. The relationship between current flowing in/out V_{CTRL} pin and V_{FB} is as shown in Figure 53.

It is recommended to add a typical 100 pF capacitor C_{FB} decoupling capacitor next to feedback pin to prevent from noise impact.

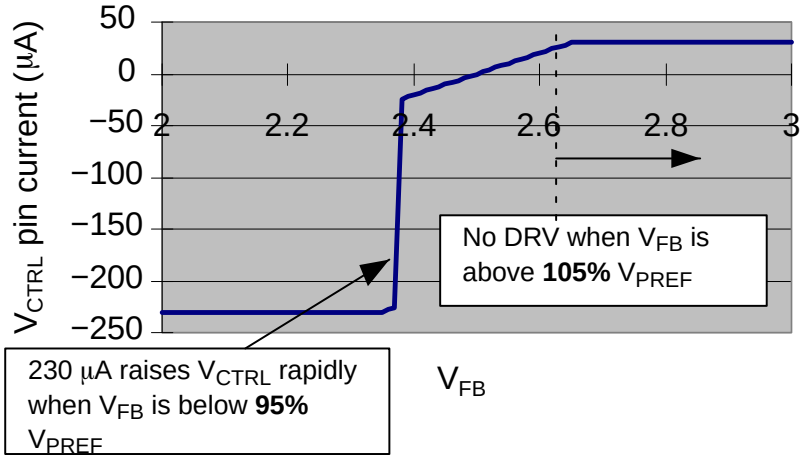

Figure 53. V_{FB} vs. Current Flowing In/Out From V_{CTRL} Pin

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PFCok Signal

The PFC provides a “PFCok” signal to:

- enable the dynamic response enhancer (I_{VLD}) if V_{bulk} is below 95%, finish of the PFC soft-start,
- enable the PFC frequency foldback,
- enable the timer (t_{DEL1}), which is to start the LLC-HB converter,
- enable the timer (t_{DEL2}), which is to stop LLC-HB converter once “PFCok” is asserted low or V_{bulk} is lower than PG level after LLC-HB has started.

This “PFCok” signal is high when the PFC stage is in normal operation, i.e. its output is above 95% of normal output, and low otherwise.

Refer to Figure 54. “PFCok” signal is low when

- the PFC stage start-up, or
- any latch off signal arrives, or
- line brown-out activates.

“PFCok” signal is high when

- DRV starts operating and the PFC stage is above 95% of target, i.e. the VLD comparator output is high, or
- the PFC stage is above 100% target, i.e. PFC_{REG} comparator output is high.

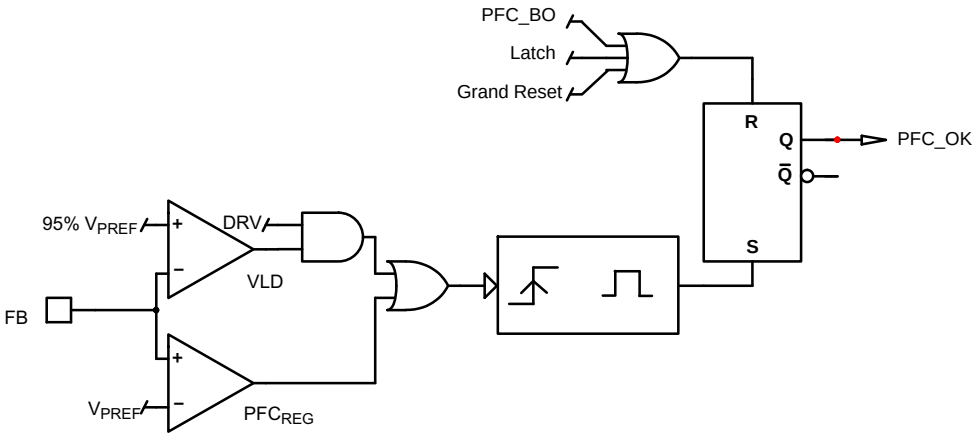

Figure 54. PFCok Signal Block Diagram

PFC Soft-Start

Refer to Figure 52 and 54. The device provides no PFC driver output when the V_{CTRL} is lower than $V_{CTRL(min)}$. V_{CTRL} is pulled low by:

- V_{CC} Under-Voltage Lockout, or
- Off Signal from On/Off Pin, or
- Thermal Shut-Down (TSD), or
- Line Brown-Out, or
- PFC Under-Voltage Protection

At one of these situations, NCP1910 grounds the V_{CTRL} pin and turns off the 200 μA current source in regulation block.

When the IC turns on again:

- V_{CTRL} will be pulled low and PFC DRV output keeps off until V_{CTRL} is below $V_{CTRL(min)}$ to make PFC starts with lowest duty cycle.
- The 200 μA current source block keeps off. Only the Operating Transconductance Amplifier (OTA) raises the V_{CTRL} slowly.

This is to obtain a slow increasing duty cycle and hence reduce the voltage and current stress on the MOSFET. A soft-start operation is obtained.

PFC Under-Voltage Protection (UVP) for Open Loop Protection

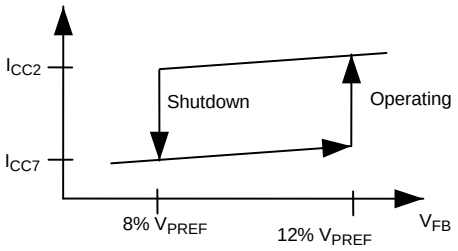

Figure 55. PFC Under-Voltage Protection

As shown in Figure 55, when V_{FB} is less than 8% of V_{PREF}, the device is shut down. The device automatically starts operation when the output voltage goes above 12% of V_{PREF}. In normal situation of boost converter configuration, the bulk voltage V_{bulk} is always greater than the input voltage V_{in} and the feedback signal V_{FB} has to be always greater than 8% and 12% of V_{PREF} to enable NCP1910 to operate.

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The main purpose of this Under-Voltage Protection function is to protect the power stage from damage at feedback loop abnormal, such as V_{FB} is grounded or the feedback resistor R_{FBU} is open.

Redundant Over-Voltage Protection (OVP2 pin)

Except the Over-Voltage Protection in FB pin, NCP1910 also reserve one dedicated pin, OVP2 pin, for the redundant over voltage protection on bulk voltage. The purpose of this feature is to protect the power components from damage in case of any drift on the feedback resistor. As shown in Figure 56, the OVP2 has 3 differences compared to the OVP in FB pin:

- The protection mode provided by OVP2 pin is latch-off. When OVP2 is triggered, the NCP1910 stays at latch off mode, i.e. both PFC and LLC stop.
- A 20 μs filter is built-in after the OVP2 comparator for better noise immunity.
- The reference voltage for this OVP2 comparator is 107% of V_{PREF}.

The resistance value of R_{OVPU} and R_{OVPL} could be the same as R_{FBU} and R_{FBL} depending on the requirement of OVP2 level. In this case, the level of the OVP in FB pin would be 105% of normal bulk voltage and OVP2 will be 107% of normal bulk voltage. Or if one would need a higher level for the OVP2, then it is flexible to change the value.

If someone doesn't need this OVP2 feature, then OVP2 function could be disable by grounding the OVP2 pin.

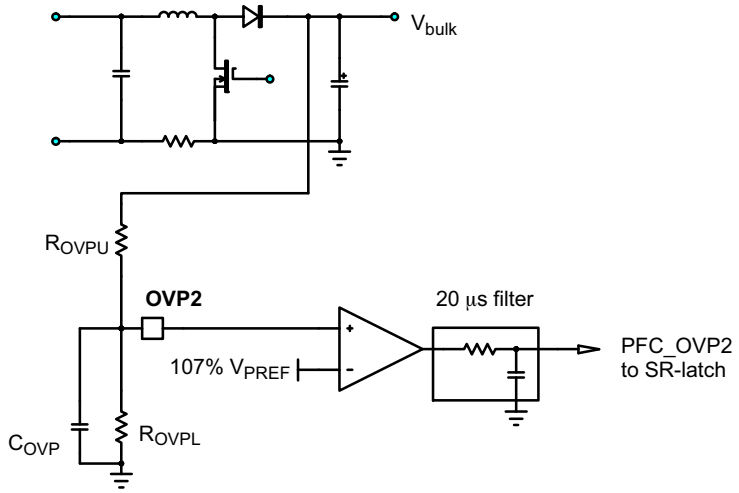

Figure 56. PFC 2nd Over-Voltage Protection

PFC Abnormal

The PFC abnormal is detected by sensing V_{CTRL} level. When V_{CTRL} stays at $V_{CTRL(max)}$, or lower than $V_{CTRL(min)}$ − 0.1 V, for more than $t_{PFCabnormal}$, PFC turns off first. After t_{DEL2}, LLC shuts down. It is latches off protection.

The main purpose of this feature is to avoid LLC from operating without correct operation of PFC stage.

LLC Section

Current Controlled Oscillator (CCO)

The current controlled oscillator features a high-speed circuitry allowing operation from 50 kHz up to 1 MHz. However, as a D-flip-flop that creates division-by-two internally provides two outputs (A and B in Figure 57), the final effective signal on LLC driver outputs (ML and MU) switches between 25 kHz and 500 kHz. The CCO is configured in such a way that if the current that flows out from the R_t pin increases, the switching frequency also goes up.

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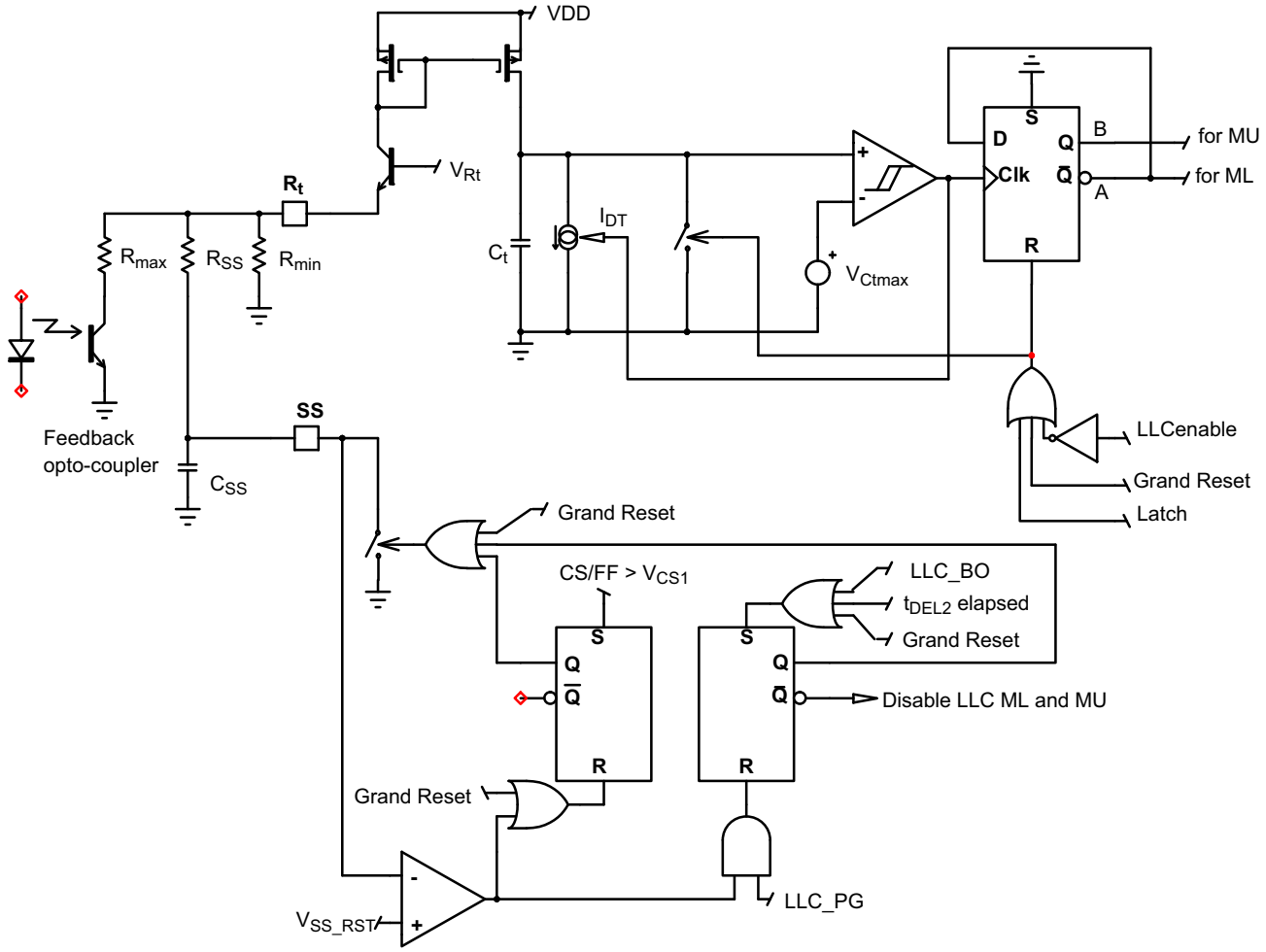

Figure 57. The Current Controlled Oscillator Architecture and Configuration

The internal timing capacitor C_t is charged by current which is proportional to the current flowing out from the R_t pin. The discharging current i_{DT} is applied when voltage on this capacitor reaches V_{Ctmax}. The output drivers are disabled during discharge period so the dead time length is given by the discharge current sink capability. Discharge sink is disabled when voltage on the timing capacitor reaches zero and charging cycle starts again. C_t is grounded to disable the oscillator when either of "turn-off LLC" signals arrives.

For the resonant applications, it is necessary to adjust minimum operating frequency with high accuracy. The designer also needs to limit maximum operating and startup frequency. All these parameters can be adjusted by using external components connected to the R_t pin as shown in Figure 57.

The following approximate relationships hold for the minimum, maximum and startup frequency respectively:

- The minimum switching frequency is given by the R_{min} resistor value. This frequency is reached if there is no feedback action and soft start period has already elapsed.

$$R_{min} = \frac{490 \times 10^6 V_{Rt}}{F_{min}} \quad \text{(eq. 22)}$$

- The maximum switching frequency excursion is limited by the R_{max} selection. Note that the maximum frequency is influenced by the opto-coupler saturation voltage value.

$$R_{max} = \frac{490 \times 10^6 V_{Rt}}{F_{max} - F_{min}} \quad \text{(eq. 23)}$$

- Resistor R_{SS} together with capacitor C_{SS} prepares the soft start period for the resonant converter.

$$R_{SS} = \frac{490 \times 10^6 V_{Rt}}{F_{SS} - F_{min}} \quad \text{(eq. 24)}$$

Where:

- $V_{Rt} = 3.5$ V
- F_{min} is the minimal frequency
- F_{max} is the maximal frequency
- F_{SS} is the maximal soft start switching frequency

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LLC Power Good Signal and Brown-Out (PG_{adj}, PG_{out} and BO_{adj} Pin)

As shown in Figure 22, the NCP1910 provides the Brown-Out circuitry (BO) that offer a way to protect the resonant converter from operating at too low V_{bulk}. In the mean time, NCP1910 provides a Power Good signal (PG_{out}) to inform the isolated secondary side that the NCP1910 is in order of match.

Once the PFC has started and raises V_{bulk} above 95% of its regulated voltage, an internal "PFC_OK" signal is asserted. 20 ms later (t_{DEL1}), the PG_{out} pin is brought low.

The PG_{out} signal can now disappear, which will release PG_{out} pin open, in two cases:

- V_{bulk} decreases to the level, programmed by a reference voltage imposed on PG_{adj} pin. This level is usually above the LLC turn-off voltage, programmed by BO_{adj} pin. Therefore, in a normal turn-off sequence, PG first drops and informs the secondary side that it must be prepared for shutdown.
- The second event that can drop the PG signal is when the PFC experiences a fault: broken feedback path (PFC UVP), PFC abnormal, or input line brown-out. In either case, the internal PFCok signal will drop and then assert the PG_{out} signal high, and starts a 5 ms timer (t_{DEL2}). Once this timer is elapsed, the LLC converter can be safely halted.

The definition of start-up, shut-off and these 2 delay timers (t_{DEL1} and t_{DEL2}) will be depicted later in "combo management section".

There are the other 2 delay timers are built-in after the brown-out comparator:

- t_{BOK} is the delay timer after V_{bulk} is rising above the BO level.
- $t_{BONOTOK}$ is the delay timer after V_{bulk} is falling down the BO level.

NCP1910 gets the information of V_{bulk} from the PFC FB pin, which minimizes the losses of the high voltage sensing circuit. As depicted in Figure 22, 3 resistors (R_1, R_2, and R_3) among V_{REF}, PG_{adj}, BO_{adj} pin, and ground determine the levels of PG_{out} signal and LLC brown-out as the following formulas:

$$V_{PG} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \cdot V_{REF} = V_{bulk,PG} \cdot \frac{R_{FBL}}{R_{FBU} + R_{FBL}} = V_{bulk,PG} \cdot \frac{V_{PREF}}{V_{bulk,nom}} \quad \text{(eq. 25)}$$

$$V_{BO} = \frac{R_3}{R_1 + R_2 + R_3} \cdot V_{REF} = V_{bulk,BO} \cdot \frac{R_{FBL}}{R_{FBU} + R_{FBL}} = V_{bulk,BO} \cdot \frac{V_{PREF}}{V_{bulk,nom}} \quad \text{(eq. 26)}$$

Where:

- V_{PG} is the voltage on PG_{adj} pin
- V_{BO} is the voltage on BO_{adj} pin
- V_{REF} is the reference voltage (5 V typically).
- V_{PREF} is the internal reference voltage for PFC feedback OTA (2.5 V typically)
- $V_{bulk,PG}$ is the bulk voltage when PG_{out} pin is released open.
- $V_{bulk,BO}$ is the bulk voltage when brown-out function of LLC activates.
- $V_{bulk,nom}$ is the normal bulk voltage, e.g. 390 V.

Divide Equation 25 by 26, we can get the relationship between R_2 and R_3 in Equation 27:

$$\frac{R_2}{R_3} = \frac{V_{bulk,PG}}{V_{bulk,BO}} - 1 \quad \text{(eq. 27)}$$

Hence, by given $V_{bulk,PG}$ and $V_{bulk,BO}$, and choose the value R_3 as the 1st step, we can get the R_2 by Equation 27 and R_1 by Equation 26.

For example, $V_{bulk,nom}$ is 390 V, $V_{bulk,PG}$ is 340 V, and $V_{bulk,BO}$ is 330 V. Choose 10 kΩ resistor as R_3. Then R2 is 303 Ω. Choose 300 Ω as it is the closet standard resistor. Then we can get the R_1 is 13.3 kΩ.

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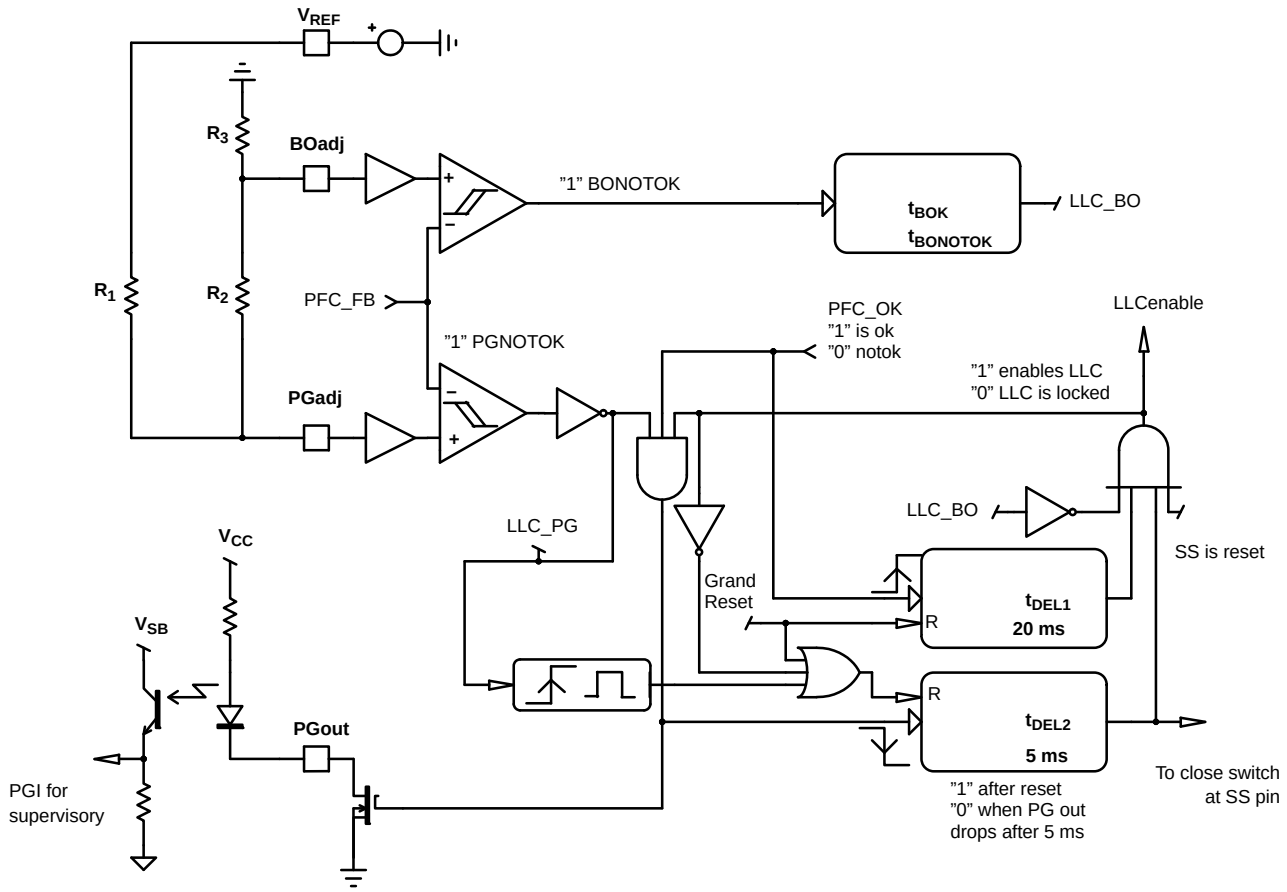

Figure 58. The PG and BO Block Diagram for LLC

LLC Fast Fault Input (CS/FF Pin)

As shown in Figure 59, the NCP1910 offers a dedicated input (CS/FF pin) to detect the primary over-current conditions and protect the power stage from damage.

Once the voltage on the CS/FF pin exceeds the threshold of V_{CS1} (1 V typically), the internal switch at SS pin will be closed to discharge C_{SS} until V_{SS} is below V_{SS_RST} (150 mV typically). Hence the switching frequency of LLC (ML and MU) is shifted up to keep the primary current under acceptable level.

In case of heavy overload, like transformer short circuit, the primary current grows very fast and thus could reach danger level. The NCP1910 therefore features additional comparator V_{CS2} (1.5 V typically) at the CS/FF pin to permanently latch the device (both PFC and LLC) and protect against destruction.

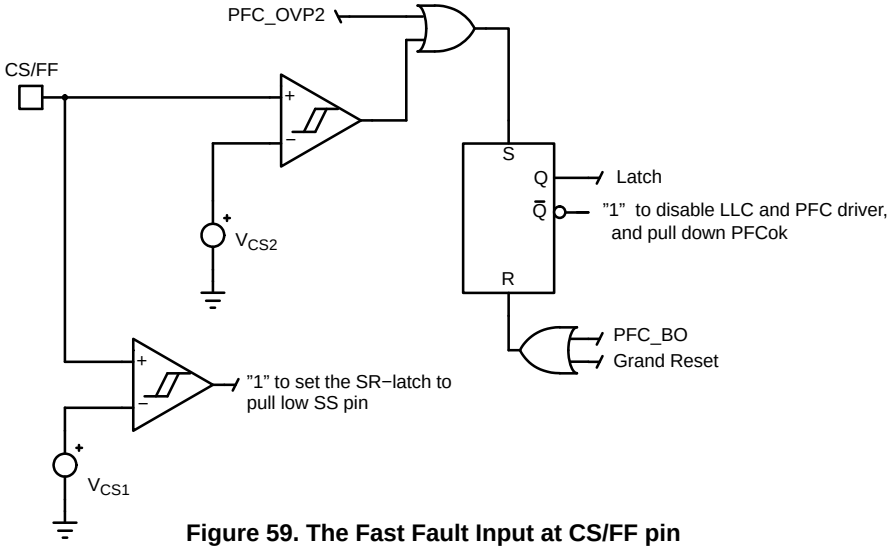

Figure 59. The Fast Fault Input at CS/FF pin

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LLC Soft-Start (SS Pin)

In resonant converter, a soft-start is needed to avoid suddenly applying the full current into the resonating circuit. NCP1910 reserves SS pin to fully discharge soft-start capacitor before re-start and in case of fault conditions:

- LLC brown-out actives,
- t_{DEL2} is elapsed, where t_{DEL2} timer could be activated by line brown-out or power good comparator,
- CS/FF pin is above V_{CS1}, the fast fault input for LLC,
- V_{CC} UVLO,
- PFC UVP,
- Off signal from on/off pin, or
- Thermal Shut-Down (TSD)

When the switch inside SS pin is activated to discharge the soft-start capacitor, it keeps close until V_{SS} is below V_{SS_RST} (150 mV typically). It ensures the full discharge of soft-start capacitor before re-start, and hence the fresh soft-start is confirmed.

Once the LLC part starts operation, the internal switch at SS pin is released open and the empty soft-start capacitor withdraws current from R_t pin through soft-start resistor, R_{SS}. This current charges up and soft-start capacitor and increases the operating frequency of LLC. As the soft-start capacitor is charged, the LLC driver output frequency smoothly decreases down to F_{min}. Of course, practically, the feedback loop is supposed to take over the CCO lead as soon as the output voltage has reached the target.

LLC Skip (Skip Pin, B Version Only)

To avoid any frequency runaway in light conditions but also to improve the standby power consumption, the NCP1910B welcomes a skip mode operation (Skip pin) which permanently observes the opto-coupler collector as depicted in Figure 60. If skip pin senses a low voltage, it cuts the LLC output pulses (ML and MU pins) until the collector goes up again.

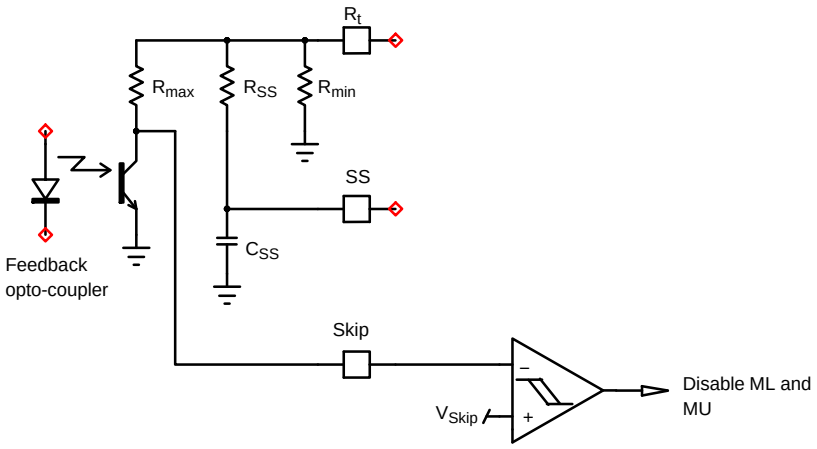

Figure 60. The LLC Skip Mode Configuration

LLC High-Voltage Driver

The NCP1910 includes a high-voltage driver allowing a direct connection to the upper side MOSFET of LLC converter. This device also incorporates an upper UVLO circuitry that makes sure enough gate voltage is available for the upper side MOSFET. The bias of the floating driver section is provided by C_{boot} capacitor between V_{boot} pin and HB pin that is refilled by external booststrap diode. The floating portion can go up to 600 Vdc and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front-end stage.

Combo Management Section

Start-Up and Stop Delay of LLC and PGout Signal (t_{DEL1} and t_{DEL2})

To ensure the proper operation of LLC, LLC cannot start if the PFC is not ready.

As depicted in the “PFCok signal” section, the internal PFCok signal is asserted high when V_{bulk} is above 95% of normal bulk voltage. After PFCok signal is high, a timer (t_{DEL1}) starts to ensure PFC stage is fully stable before LLC starts. When t_{DEL1} is elapsed, PG_{out} pin is grounded and LLC starts its driver outputs (ML and MU pins).

In case of shutdown by unplugging ac input or line brown out situation, PG_{out} signal is released open. And then another timer (t_{DEL2}) starts. Once the t_{DEL2} is elapsed, LLC stops its drivers (ML and MU pins).

Figure 61 depicts the start-up and stop delay of LLC and PG_{out}.

Once the PFC is ready (PFCok is asserted high), t_{DEL1} (20 ms typically) is started. Once this delay is elapsed:

- PG_{out} pin is asserted low
- LLC drivers (ML and MU pins) can start to operate.

As shutdown by unplug ac input, V_{bulk} decreases:

- When it reaches the PG signal, which is adjusted by PG_{adj} pin, PG_{out} pin is released open.

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- If V_{bulk} reaches the LLC stop level (BO level adjusted by BO_{adj} pin), the LLC stops; or if V_{bulk} drops slowly, e.g. light load, LLC drivers (ML and MU pins) will stop 5 ms after PG_{out} pin is released (t_{DEL2}).

As shutdown by line brown-out situation, PFCok signal will be pulled down:

- PG_{out} pin is released open once this internal PFCok signal is low.
- LLC drivers (ML and MU pins) will stop 5 ms after PG_{out} pin is released open (t_{DEL2}).

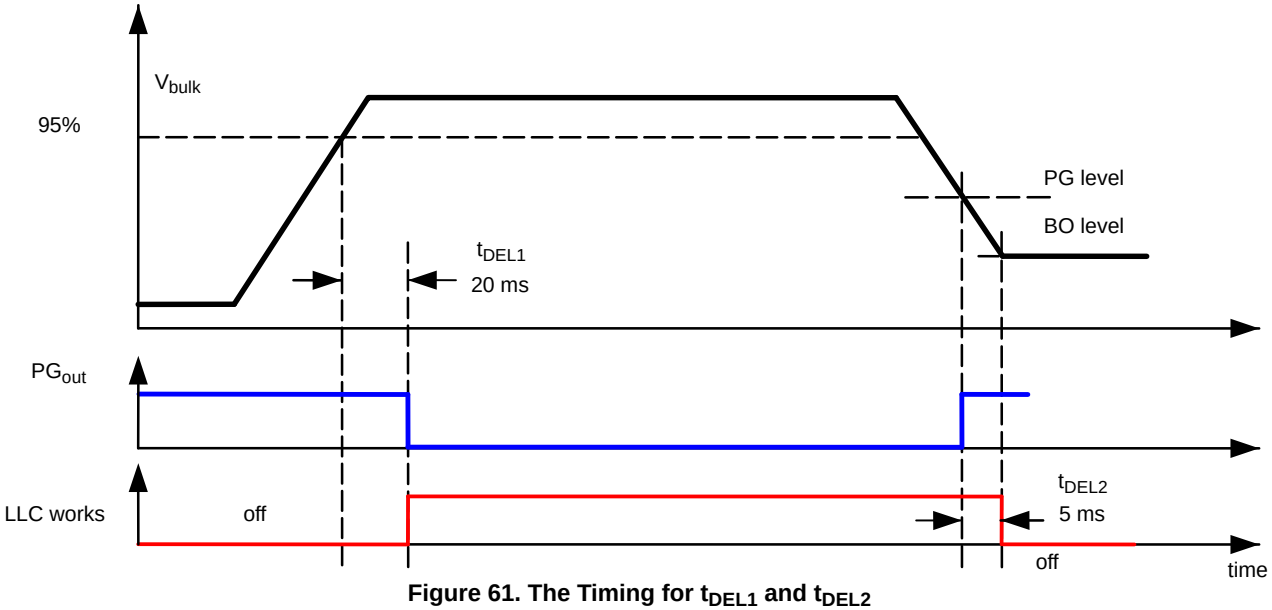

Figure 61. The Timing for t_{DEL1} and t_{DEL2}

Remote On/Off (On/Off Pin)

NCP1910 reserves one dedicated pin for remote control feature at on/off pin:

- When the on/off pin is pulled below 1 V, the PFC starts operation. 20 ms after V_{bulk} is above 95% of target level, LLC starts.
- When the on/off pin is above 3 V, the device stops both PFC and LLC immediately and keeps low consumption. Figure 62 depicts the relationship between the operation mode and on/off pin.

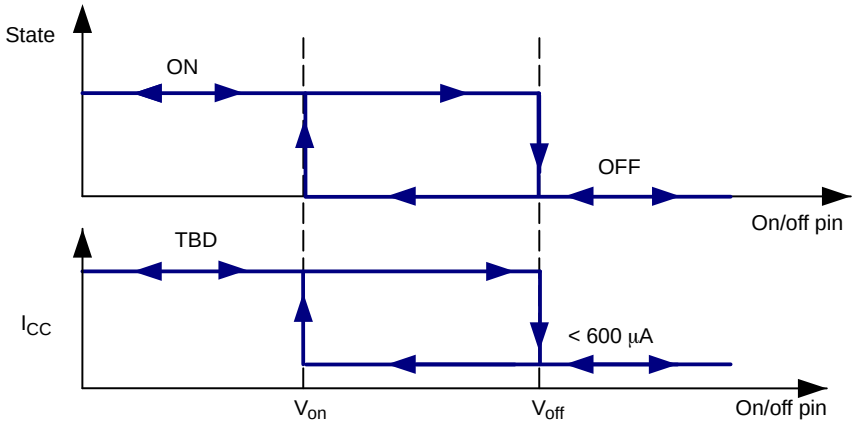

Figure 62. Remote on/off (on/off Pin)

V_{CC} Under-Voltage LockOut (UVLO)

The device incorporates an Under-Voltage Lockout block to prevent the circuit from operating when V_{CC} is too low in order to ensure a proper operation. An UVLO comparator monitors V_{CC} pin voltage to allow the NCP1910 to operate when V_{CC} exceeds $V_{CC(on)}$. The comparator incorporates some hysteresis ($V_{CC(Hys)}$) to prevent erratic operation as the V_{CC} crosses the threshold. When V_{CC} goes below the UVLO comparator lower threshold ($V_{CC(min)}$), the circuit turns off. It is illustrated in Figure 63. After startup, the operating range is between 9 V and 20 V.

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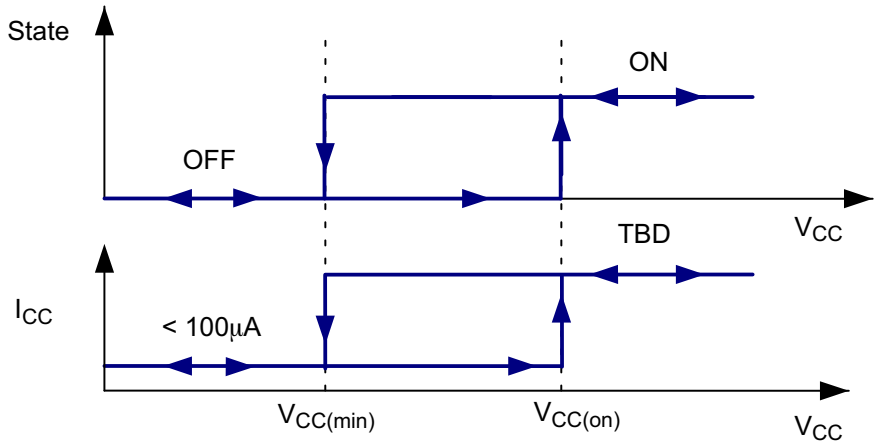

Figure 63. V_{CC} Under-Voltage LockOut (UVLO)

Bias the Controller

It is recommended to add a typical 1 nF to 100 nF decoupling capacitor next to the V_{CC} pin for proper operation. The hysteresis between $V_{CC(on)}$ and $V_{CC(min)}$ is small because the NCP1910 is supposed to be biased by external power source. Therefore it is recommended to make a low-voltage source to bias NCP1910, e.g. the standby power supply.

Thermal Shutdown

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds TSD level. The output stage is then enabled once the temperature drops below typically 110 °C (i.e. TSD − TSD_{hyste}). The thermal shutdown is provided to prevent possible device failures that could result from an accidental over-heating.

5 V Reference

The V_{REF} pin provides an accurate (±2% typically) 5 V reference voltage. The Power-Good and Brown-Out of LLC converter, and the frequency foldback level (fold pin) of PFC can hence can get an accurate reference voltage by resistor dividers.

Latched Protections and Reset

As depicated in the above sections, there are 3 fault modes that latch off both PFC and LLC:

- PFC abnormal
- PFC OVP2
- LLC CS/FF pin is above V_{CS2}

To release from the latch-off mode, NCP1910 offers 3 ways:

- Recycle V_{CC} so that V_{CC} is below $V_{CC(min)}$ and back to above $V_{CC(on)}$ again.
- Recycle the remote on/off function, which toggles on/off pin high and low again.
- Recycle the line brown-out function, which could be done by unplug and re-plug the ac input.

ORDERING INFORMATION

Device	Version	Marking	Package	Shipping†
NCP1910B65DWR2G	65 kHz − B	NCP1910B65	SOIC-24 WB Less Pin 21 (Pb-Free)	1000 / Tape & Reel

DISCONTINUED (Note 5)

NCP1910A65DWR2G	65 kHz − A	NCP1910A65	SOIC-24 WB Less Pin 21 (Pb-Free)	1000 / Tape & Reel
NCP1910A100DWR2G	100 kHz − A	NCP1910A10	SOIC-24 WB Less Pin 21 (Pb-Free)	1000 / Tape & Reel
NCP1910B100DWR2G	100 kHz − B	NCP1910B10	SOIC-24 WB Less Pin 21 (Pb-Free)	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranded the document to **onsemi** format. NCP1910A65DWR2G, NCP1910A100DWR2G, NCP1910B100DWR2G OPNs marked as Discontinued. JP version discontinued due to low usage and minimal marketing benefit.	3/27/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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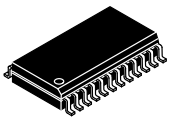
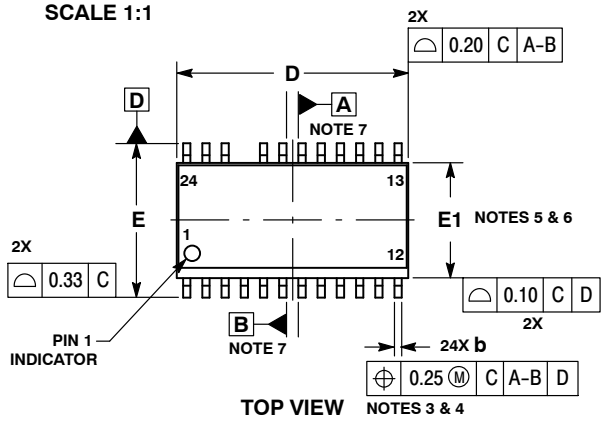
SOIC−24 WB LESS PIN 21
CASE 752AB
ISSUE O

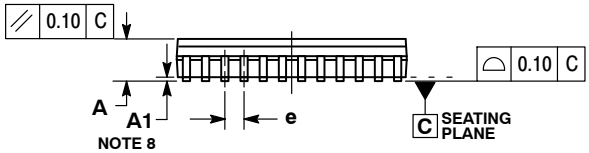
DATE 17 AUG 2010



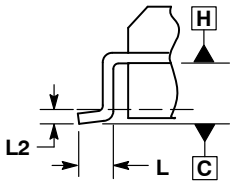
SCALE 1:1



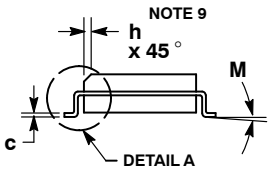
TOP VIEW



SIDE VIEW



DETAIL A

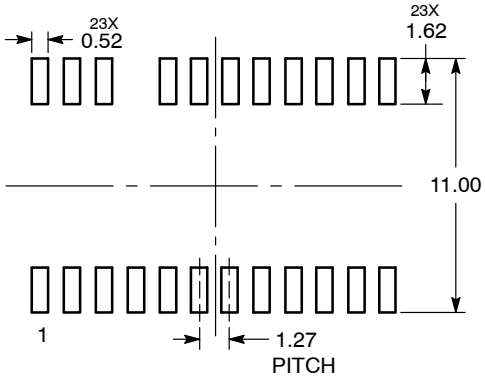


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
6. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, PROTRUSIONS, TIE BAR BURRS, OR GATE BURRS BUT INCLUSIVE OF ANY MOLD MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
9. THIS CHAMFER IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED IN THE INDICATED AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.29
b	0.31	0.51
J	0.20	0.33
D	15.40 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
h	0.25	0.75
L	0.40	1.27
L2	0.25 BSC	
M	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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DESCRIPTION:	**SOIC−24 WB LESS PIN 21**	**PAGE 1 OF 1**

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