Low Power Offline PWM Current Mode Controller with Brown-Out Protection

NCP1256



TSOP−6
CASE 318G
STYLE 13

The NCP1256 includes everything to build cost−effective switch mode power supplies ranging from a few watts up to several tens of watts. Housed in a tiny TSOP−6 package, the part can be supplied up to 30 V. It hosts a jittered 65 or 100 kHz switching circuitry operated in peak current mode control. When the power in the secondary side starts decreasing, the controller automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while freezing the peak current.

NCP1256 comes with several protection features such as a timer−based auto−recovery short circuit protection, lossless OPP, and an easily adjustable Brown Out (BO) pin. Two inputs are provided to latch off the part in a practical way, for instance with OVP and OTP events. Several options exists to chose latch or auto−recovery for these events.

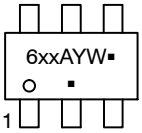
Features

- Fixed−frequency 65 kHz or 100 kHz Current−mode Control Operation
- Adjustable Over Power Protection (OPP) Circuit, Disabled at Low Line
- Adjustable Brown Out Level
- Frequency Foldback down to 26 kHz and Skip−cycle in Light Load Conditions
- Internally−fixed Slope Compensation Ramp
- Internally−fixed 4 ms Soft−start
- 70 ms Timer−based Auto−recovery Short−circuit Protection
- Frequency Jittering in Normal and Frequency Foldback Modes
- Double Hiccup Auto−recovery Short−circuit Protection
- Pre−short Ready for Latched OCP Option
- Latched/Auto−Recovery OVP Protection on V_{cc}
- Latched Inputs for Improved Robustness (OVP and OTP implementations)
- Auto−Recovery ac Line OVP Protection (E Version)
- +500 mA/ −500 mA Source/Sink Drive Capability
- EPS 2.0 Compliant
- These are Pb−Free Devices

Typical Applications

- Ac−dc Adapters for Portable Devices, Computers, Tablets etc.
- Auxiliary Power Supplies

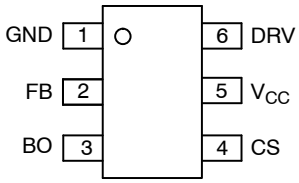
MARKING DIAGRAM



6xx	= Specific Device Code
x	= A, E or 2
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in on page 23 of this data sheet.

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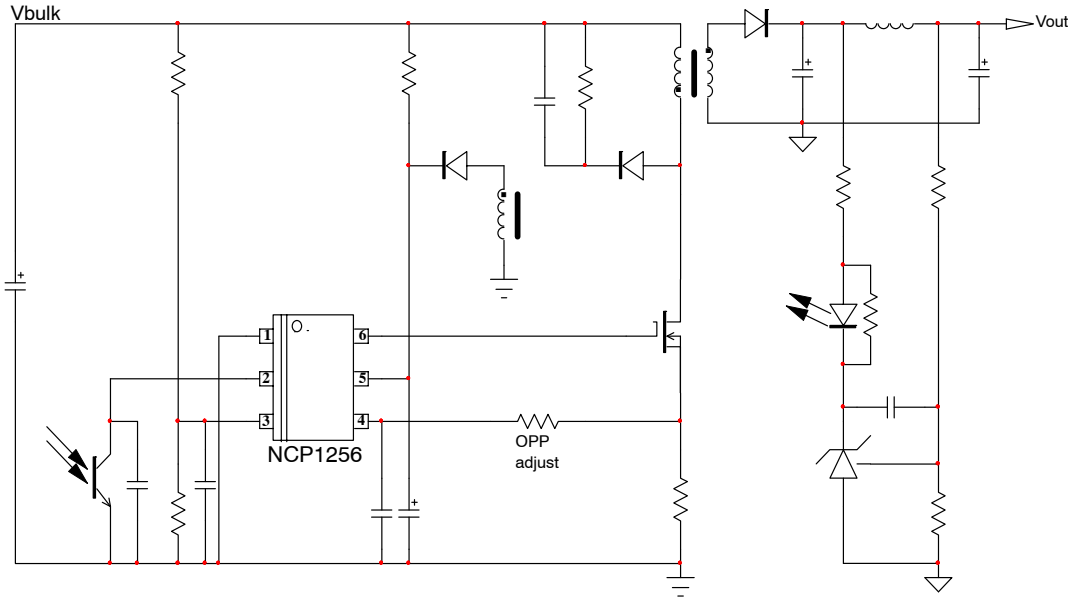

Figure 1. Typical Application Example – Latched OVP on V_{cc}

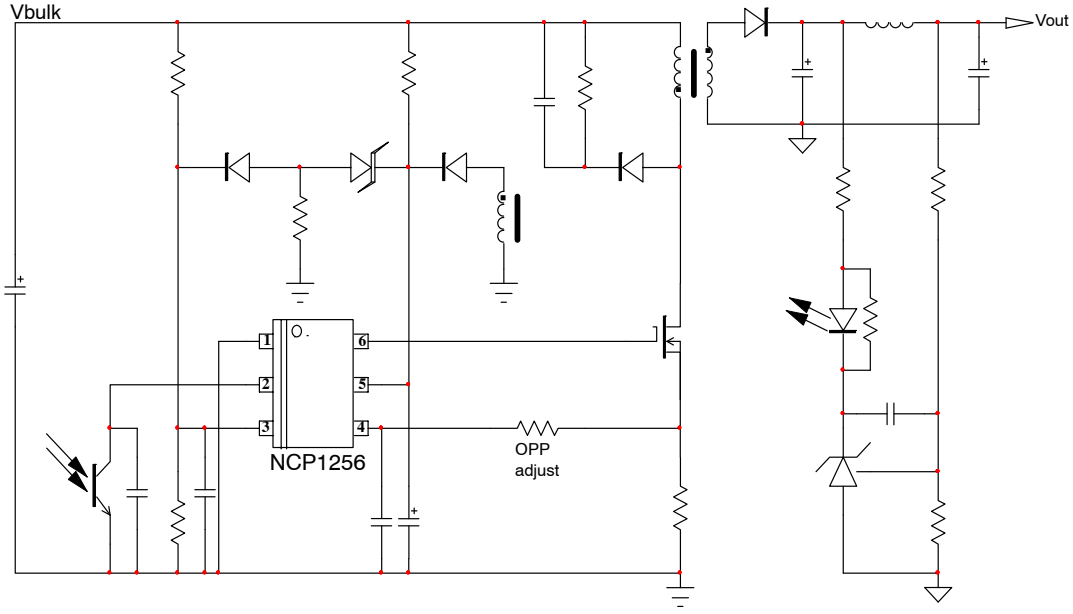

Figure 2. Typical Application Example – OVP is Latched on BO

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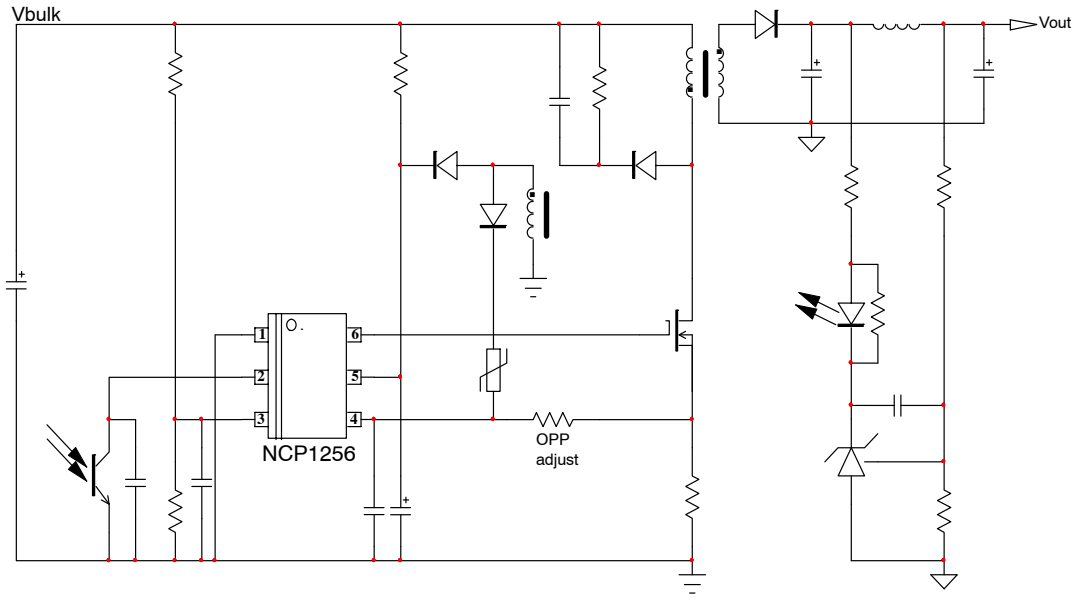

Figure 3. Typical Application Example – OVP is Latched on V_{cc}, OTP Latched on CS

Table 1. PIN DESCRIPTIONS

Pin No	Pin Name	Function	Pin Description
1	GND	–	The controller ground.
2	FB	Feedback pin	Hooking an optocoupler collector to this pin will allow regulation.
3	BO/OVP	Adjust the BO level Latch input	A voltage below the programmed level stops the controller. When above, the controller can start. When the pin is brought above 4.5 V for four consecutive clock cycles, the part latches off. With the E version, an auto−recovery ac line OVP is available through this pin.
4	CS	Current sense + OPP adjustment Latch input	This pin monitors the primary peak current but also offers a means to introduce over power compensation. When the pin is brought above 1.5 V during the off time, the part permanently latches off.
5	V_{cc}	Supplies the controller – protects the IC	This pin is connected to an external auxiliary voltage. An OVP comparator monitors this pin and offers a means to latch the converter in fault conditions.
6	DRV	Driver output	The driver's output to an external MOSFET gate.

Table 2. OPTIONS

Controller	Frequency	OCP	OVP on BO	OVP/OTP CS	OVP V_{cc}
NCP1256ASN65T1G	65 kHz	Latched	Latched	Latched	Latched
NCP1256BSN65T1G	65 kHz	Auto−recovery	Latched	Latched	Latched
NCP1256ASN100T1G	100 kHz	Latched	Latched	Latched	Latched
NCP1256BSN100T1G	100 kHz	Auto−recovery	Latched	Latched	Latched
NCP1256ESN65T1G	65 kHz	Auto−recovery	Auto−recovery	Auto−recovery	Auto−recovery

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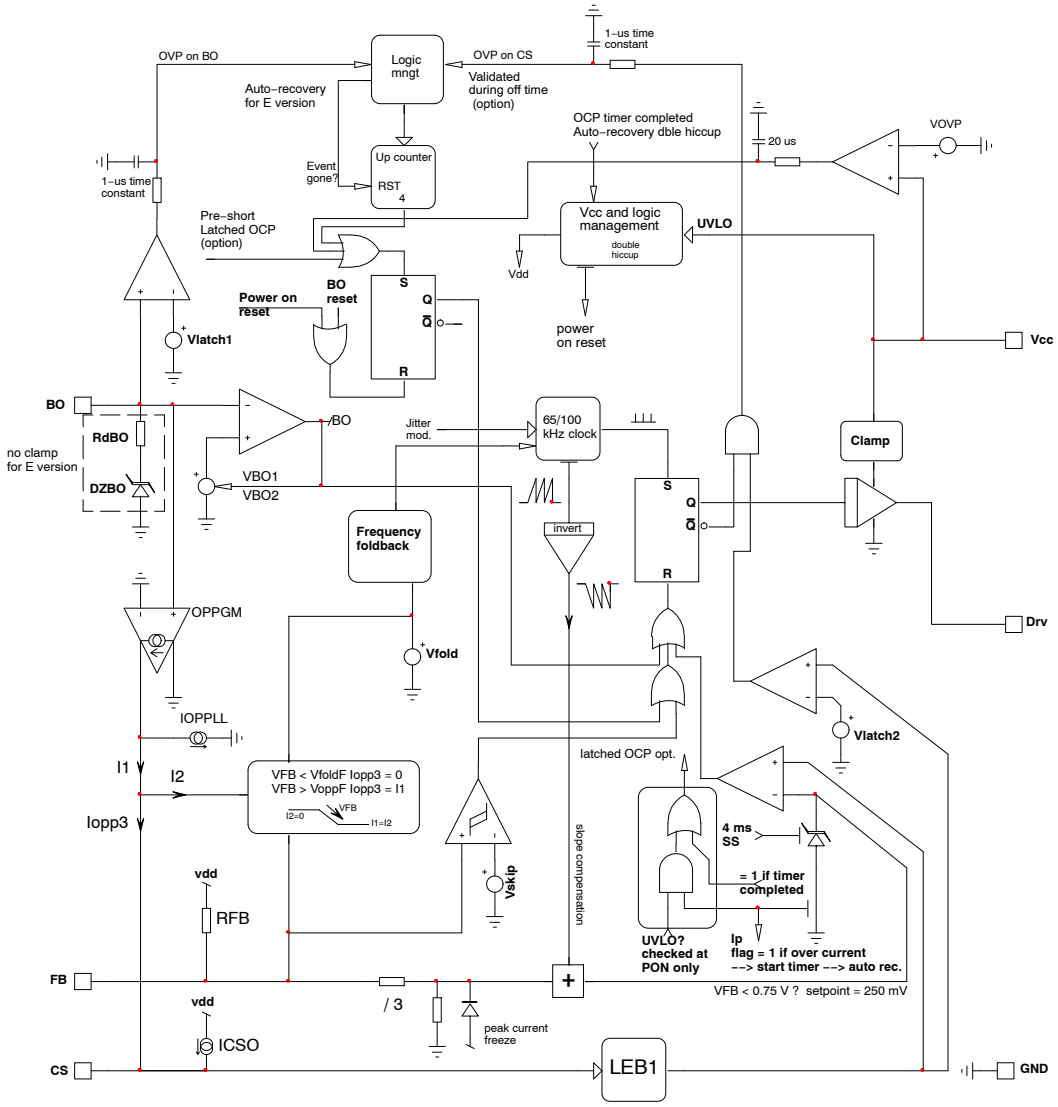

Figure 4. Internal Block Diagram

Table 3. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{cc}	Power Supply voltage, V_{cc} pin, continuous voltage	−0.3 to 28	V
	Maximum voltage on low power pins CS, FB and BO	−0.3 to 10	V
V_{DRV}	Maximum voltage on DRV pin	−0.3 to V_{cc}+0.3	V
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	360	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
HBM	Human Body Model ESD Capability per JEDEC JESD22−A114F	4	kV
MM	Machine Model ESD Capability per JEDEC JESD22−A115C	200	V
CDM	Charged−Device Model ESD Capability per JEDEC JESD22−C101E	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 4. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
VCC_{ON}	V_{CC} increasing level at which driving pulses are authorized	5	16	18	20	V
$VCC_{(min)}$	V_{CC} decreasing level at which driving pulses are stopped	5	8.3	8.9	9.5	V
VCC_{HYST}	Hysteresis Vcc_{ON}−$Vcc_{(min)}$	5	8.4	–	9.25	V
VCC_{reset}	Latched state reset voltage	5	8.1	$V_{CC(min)}$−2 50 mV	8.8	V
ICC_1	Start−up current	5	5		7.5	μA
ICC_2	Internal IC consumption with V_{FB} = 3.2 V and C_L = 0 F_{SW} = 65 kHz F_{SW} = 100 kHz	5	 – –	 1.30 1.35	 – –	mA
ICC_3	Internal IC consumption with V_{FB} = 3.2 V and C_L = 1 nF F_{SW} = 65 kHz F_{SW} = 100 kHz	5	 – –	 1.8 2.5	 – –	mA
I_{dis}	Natural part consumption in hiccup mode − non switching	5	–	350	–	μA
ICC_{stby}	Static consumption between two skip cycles	5	–	420	–	μA
ICC_{noload}	Internal IC consumption while in skip mode (V_{cc} = 14 V, driving a typical 7−A/600−V MOSFET, includes opto current) (Note 1)	5	–	440	–	μA
DRIVE SECTION						
T_r	Output voltage rise−time @ CL = 1 nF, 10−90% of output signal	6	–	40	–	ns
T_f	Output voltage fall−time @ CL = 1 nF, 10−90% of output signal	6	–	30	–	ns
R_{OH}	Source resistance	6	–	13	–	Ω
R_{OL}	Sink resistance	6	–	6	–	Ω
I_{source}	Peak source current, V_{GS} = 0 V (Note 2)	6	–	500	–	mA
I_{sink}	Peak sink current, V_{GS} = 12 V (Note 2)	6	–	500	–	mA
V_{DRVlow}	DRV pin level at V_{CC} close to $VCC_{(min)}$ with a 33−kΩ resistor to GND	6	8	–	–	V
$V_{DRVhigh}$	DRV pin level at V_{CC}= V_{OVP}−0.2 V − DRV unloaded	6	10	12	14	V
CURRENT COMPARATOR						
V_{Limit}	Maximum internal current setpoint − no OPP	4	0.744	0.8	0.856	V
V_{foldI}	Default internal voltage set point for frequency foldback trip point ≈ 63% of V_{limit}	4	–	500	–	mV
$V_{freezeI}$	Internal peak current setpoint freeze (≈31% of V_{limit})	4	–	250	–	mV
T_{DEL}	Propagation delay from current detection to gate off−state	4	–	40	60	ns
T_{LEB1}	Leading Edge Blanking Duration − first OCP path	4	–	300	–	ns
T_{SS}	Internal soft−start duration activated upon startup, auto−recovery	–	–	4	–	ms
I_{CSO}	Internal pull−up source for pin opening safety test	4	–	1	–	μA
I_{OPP1}	Voltage on V_{FB} < V_{foldF}, percentage of applied OPP current	4	–	0	–	%
I_{OPP2}	Voltage on V_{FB} > V_{foldF} + 0.7 V, percentage of applied OPP current	4	–	100	–	%
I_{OPP3}	Voltage on pin 3 = 2.65 V (265 V rms in) AND V_{FB} > V_{foldF}	4	170	185	210	μA
$I_{OPP3clp}$	Voltage on pin 3 > 2.65 V − clamped OPP current	4	–	185	–	μA
I_{OPPLL}	OPP current delivered from CS pin for V_{pin3} = V_{BOon}	4	–	–	6	μA
$OPPg_m$	Internal OTA for OPP current generation from BO −40°C to +125°C +25°C to +125°C	4	 101 103	 115 115	 125 125	μS

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Table 4. ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
INTERNAL OSCILLATOR						
$f_{OSC,nom}$	Oscillation Frequency 65 kHz version 100 kHz version	–	 61 93	 65 100	 70 107	kHz
D_{max}	Maximum duty ratio	–	77	80	83	%
f_{jitter}	Frequency jittering in percentage of f_{OSC}	–	–	±5	–	%
f_{swing}	Swing frequency over the whole frequency range	–	–	240	–	Hz
FEEDBACK SECTION						
R_{up}	Internal pull−up resistor	2	–	30	–	kΩ
R_{eq}	Equivalent ac resistance from FB to gnd	2	19	23	26	kΩ
I_{ratio}	Pin 2 to current setpoint division ratio	–	–	3	–	
$V_{freezeF}$	Feedback voltage below which the peak current is frozen	2	–	0.75	–	V
FREQUENCY FOLDBACK						
V_{foldF}	Frequency foldback level on the feedback pin − ≈63% of maximum peak current	–	–	1.5	–	V
F_{trans}	Minimum operating frequency	–	22	26	30	kHz
$V_{fold,end}$	End of frequency foldback feedback level, $F_{sw} = F_{trans}$		–	1.2	–	V
V_{skip}	Skip−cycle level voltage on the feedback pin	–	–	0.6	–	V
Skip hysteresis	Hysteresis on the skip comparator (Note 3)	–	–	45	–	mV
INTERNAL SLOPE COMPENSATION						
S_{65}	Compensation ramp slope, F_{sw} = 65 kHz	–	–	30	–	mV/μs
S_{100}	Compensation ramp slope, F_{sw} = 100 kHz	–	–	50	–	mV/μs
PROTECTIONS						
V_{latch1}	Latching level input, brown−out input	3	4.3	4.5	4.7	V
V_{latch2}	Latching level, current sense input, off time only	4	1.45	1.5	1.55	V
$T_{latch-count}$	Number of clock cycles before latch confirmation from pin 3&4	–	–	4	–	
$T_{latch-del}$	OVP detection time constant	–		1	–	μs
Timer	Internal auto−recovery fault timer duration	–	50	70	90	ms
V_{OVP}	Latched over voltage protection on the V_{cc} rail	6	25.3	26	26.8	V
T_{OVP}−del	Delay before OVP confirmation on V_{cc}	6	–	25	–	μs
I_{BO}	Brown−Out input bias current, $V_{BO} < D_{ZBO}$	3	–	0.02	–	μA
V_{BOon}	Turn−on voltage	3	0.76	0.8	0.87	V
V_{BOoff}	Turn−off voltage	3	0.66	0.7	0.74	V
T_{BO}	De−bouncing filter on BO comparator	3	–	50	–	μs
R_{dBO}	Dynamic Zener diode resistance (all versions except E)	3	–	1	–	kΩ
D_{ZBO}	Active Zener diode clamping BO signal (all versions except E)	3	3.1	3.3	3.5	V
D_{ZBO}	Active Zener diode clamping BO signal (all versions except E)	3	3.1	3.3	3.5	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. For information only, collected on a typical 45−W adapter.
2. Guaranteed by design
3. Not tested in production.

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TYPICAL CHARACTERISTICS

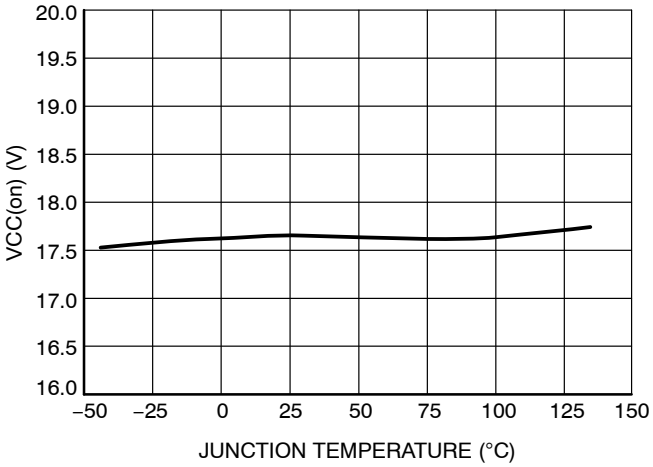

Figure 5. VCC(on) vs. Junction Temperature

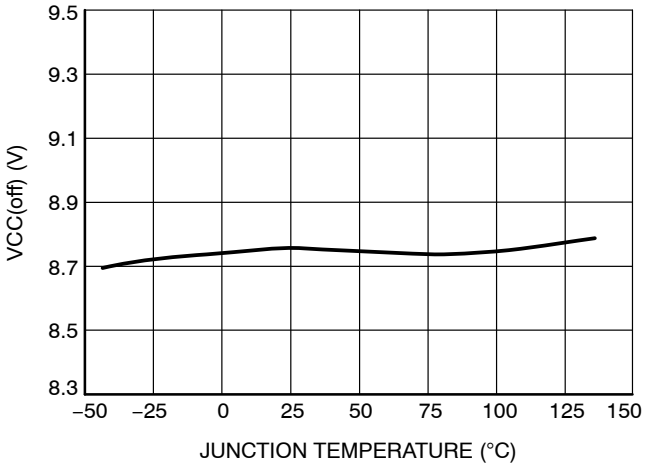

Figure 6. VCC(off) vs. Junction Temperature

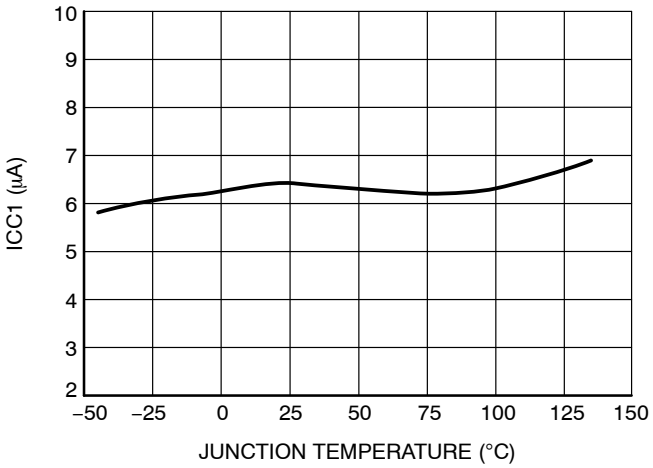

Figure 7. ICC1 vs. Junction Temperature

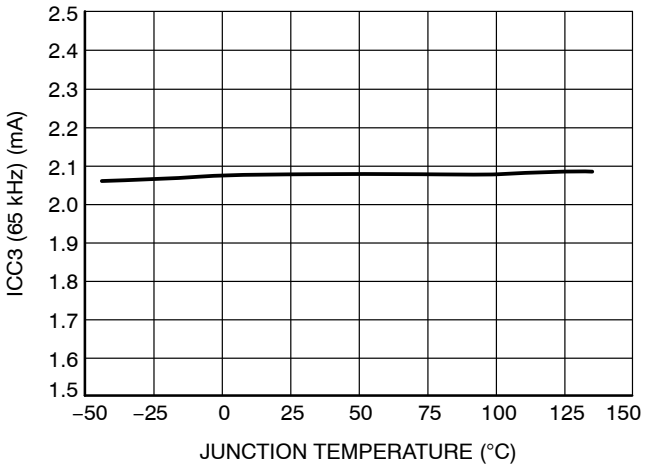

Figure 8. ICC3 vs. Junction Temperature

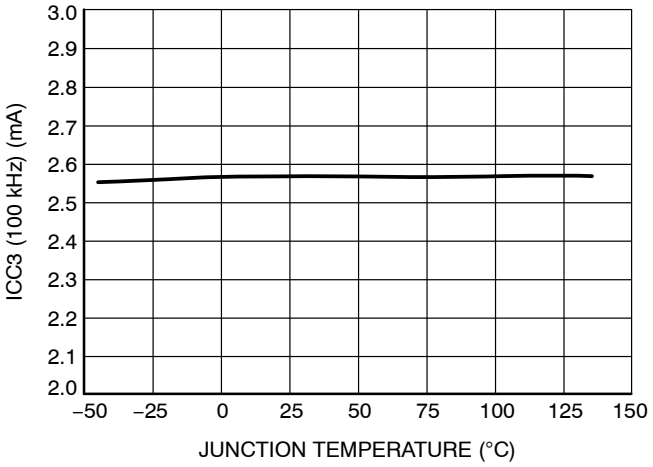

Figure 9. ICC3 vs. Junction Temperature

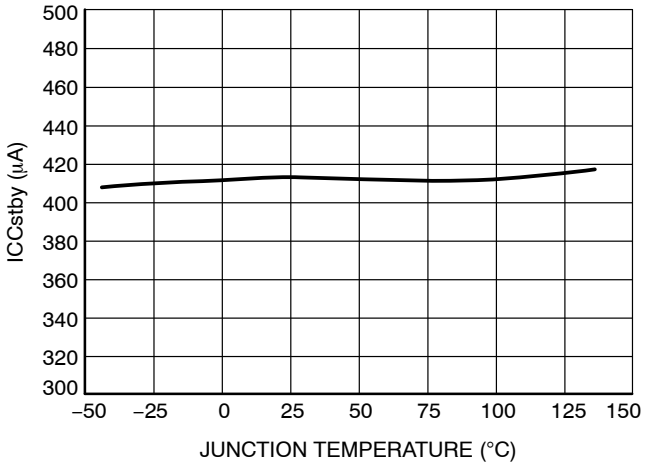

Figure 10. ICCstby vs. Junction Temperature

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TYPICAL CHARACTERISTICS

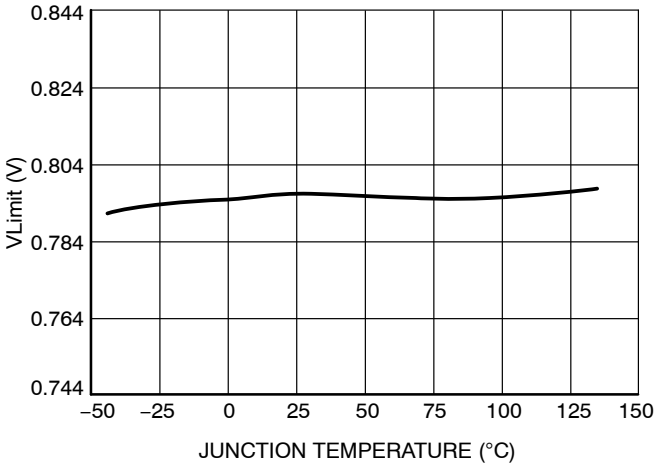

Figure 11. VLimit vs. Junction Temperature

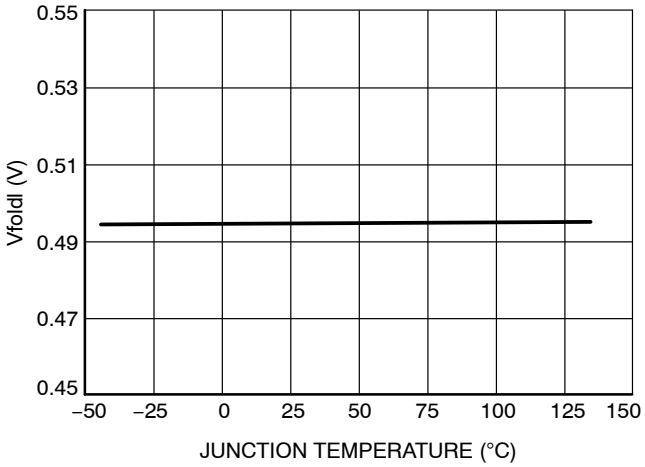

Figure 12. Vfoldl vs. Junction Temperature

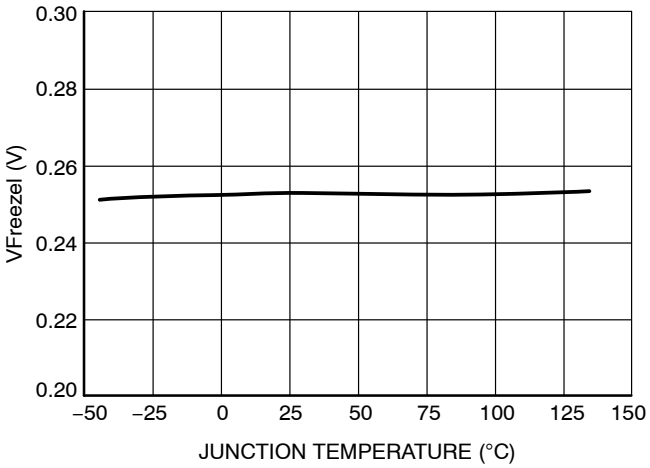

Figure 13. VFreezel vs. Junction Temperature

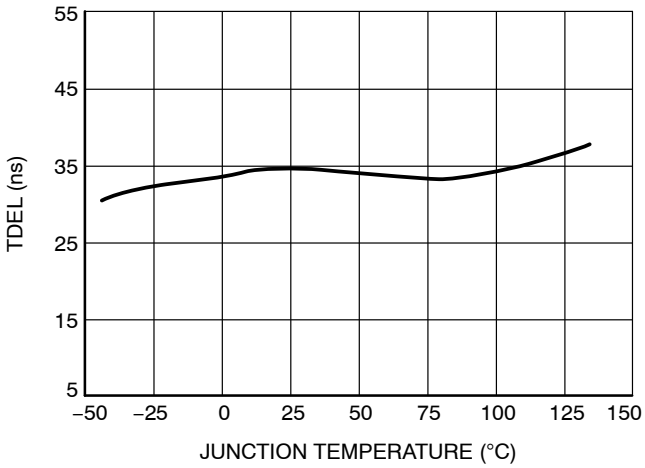

Figure 14. TDEL vs. Junction Temperature

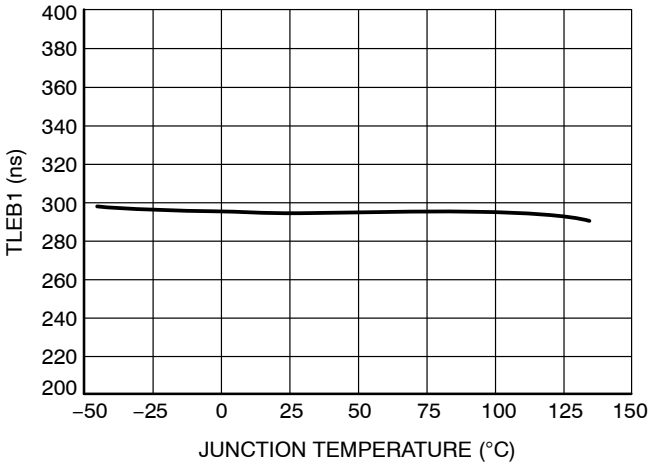

Figure 15. TLEB1 vs. Junction Temperature

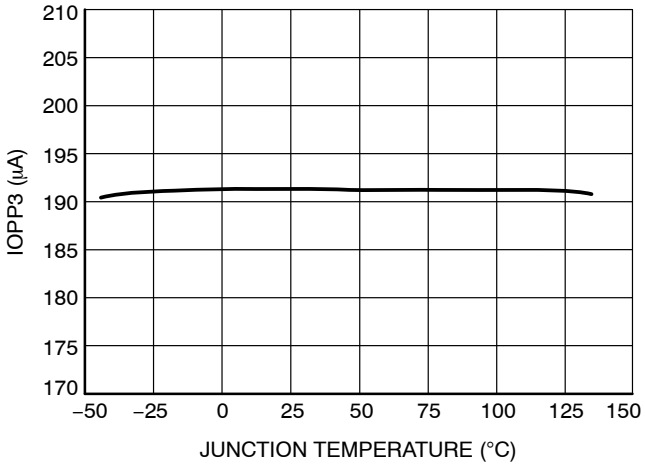

Figure 16. IOPP3 vs. Junction Temperature

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TYPICAL CHARACTERISTICS

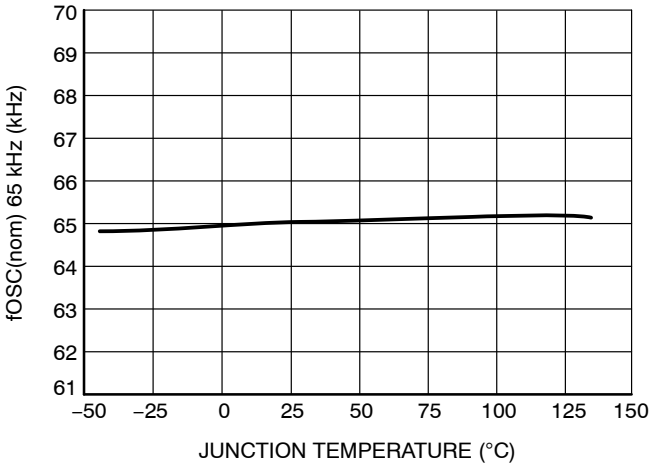

Figure 17. fOSC(nom) vs. Junction Temperature

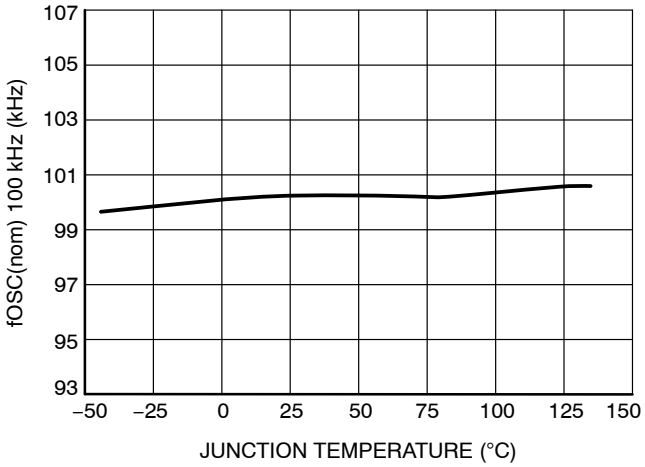

Figure 18. fOSC(nom) vs. Junction Temperature

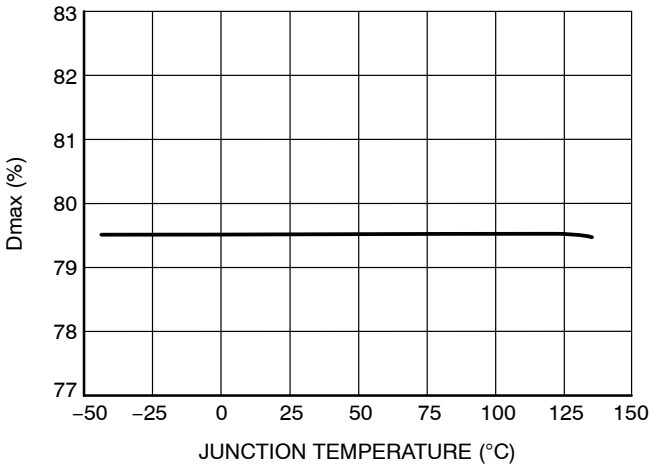

Figure 19. Dmax vs. Junction Temperature

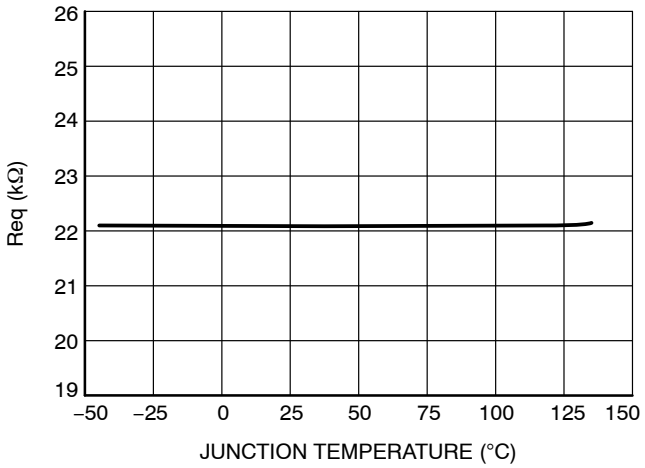

Figure 20. Req vs. Junction Temperature

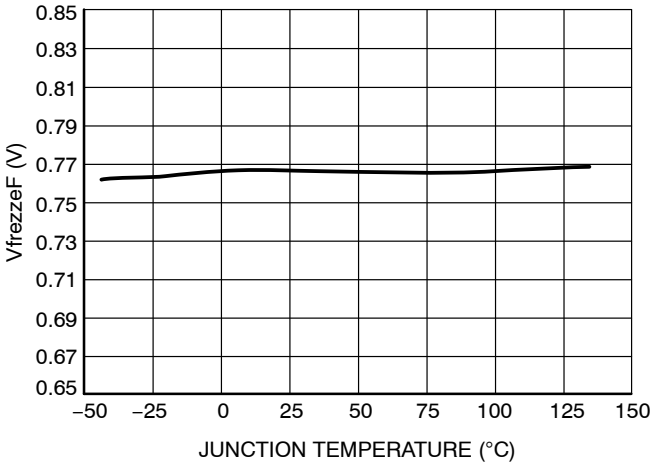

Figure 21. VfreezeF vs. Junction Temperature

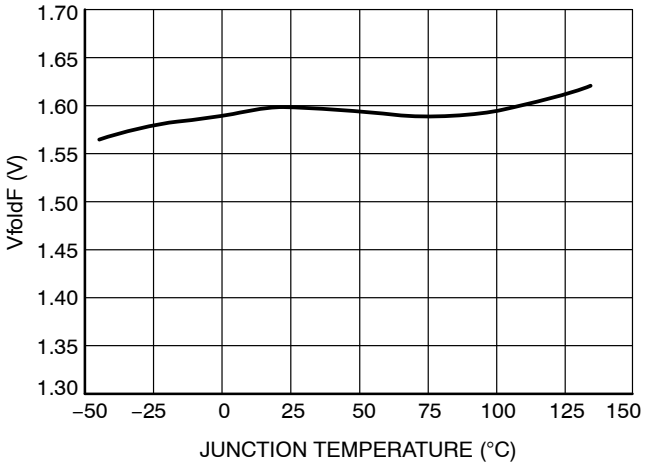

Figure 22. VfoldF vs. Junction Temperature

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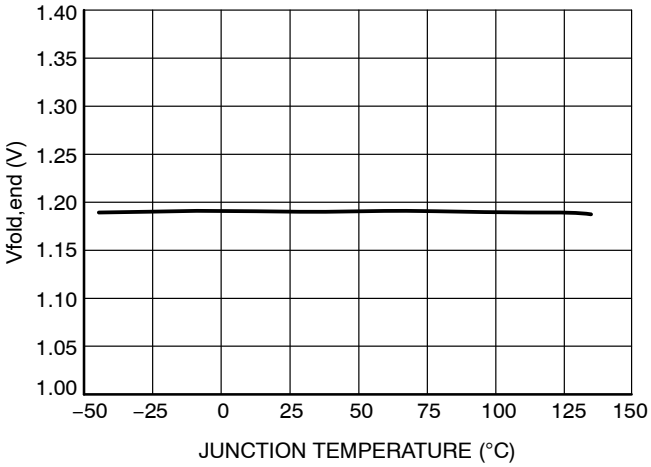

Figure 23. Vfold,end vs. Junction Temperature

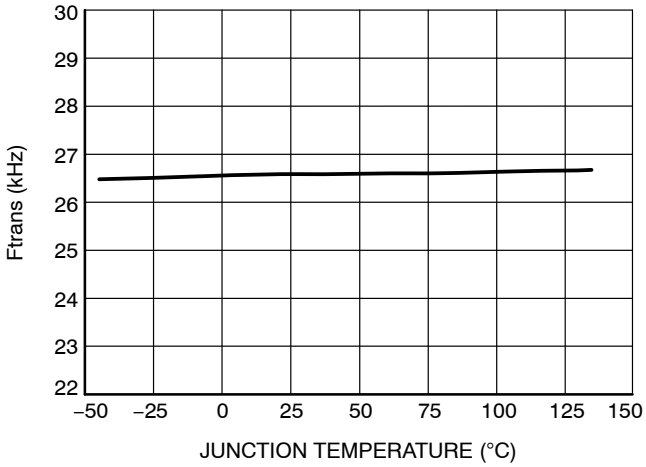

Figure 24. Ftrans vs. Junction Temperature

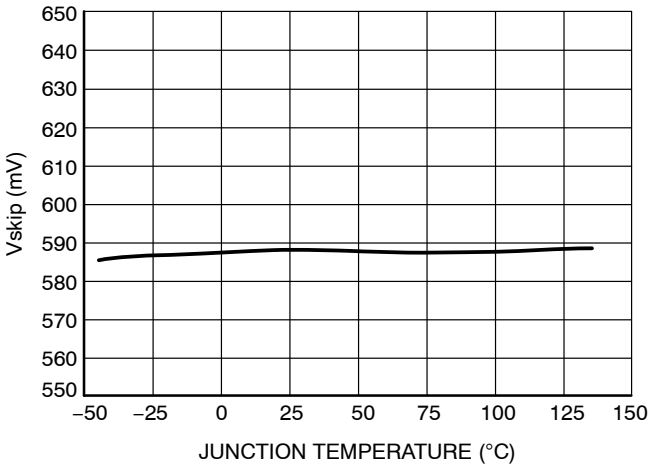

Figure 25. Vskip vs. Junction Temperature

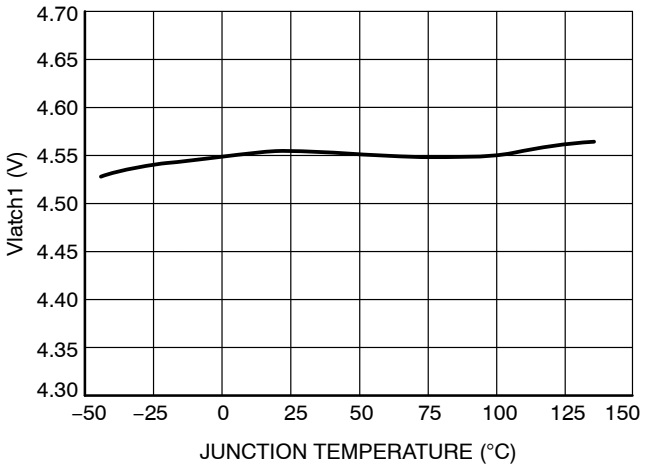

Figure 26. Vlatch1 vs. Junction Temperature

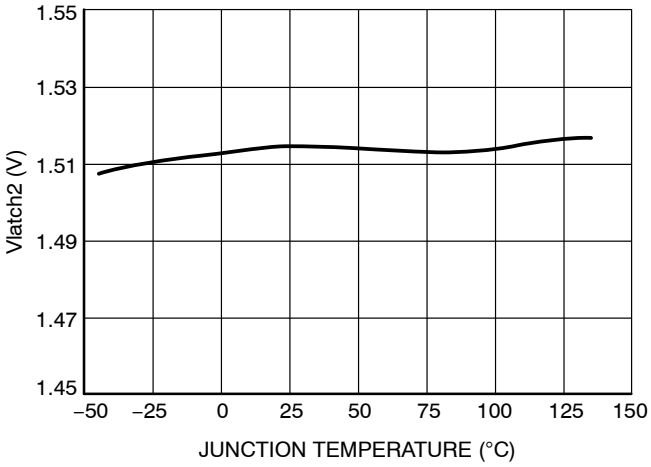

Figure 27. Vlatch2 vs. Junction Temperature

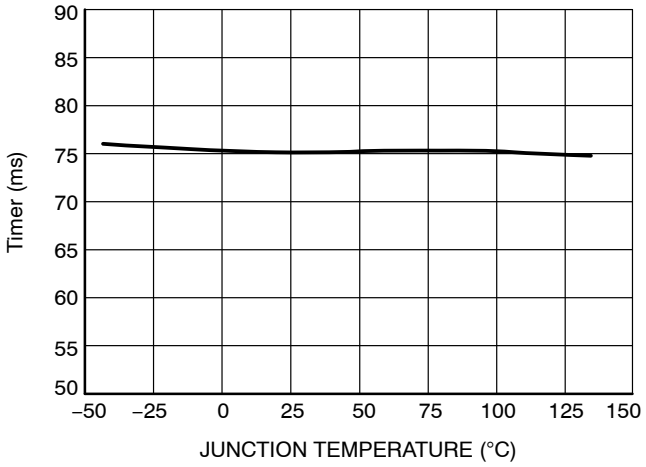

Figure 28. Timer vs. Junction Temperature

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TYPICAL CHARACTERISTICS

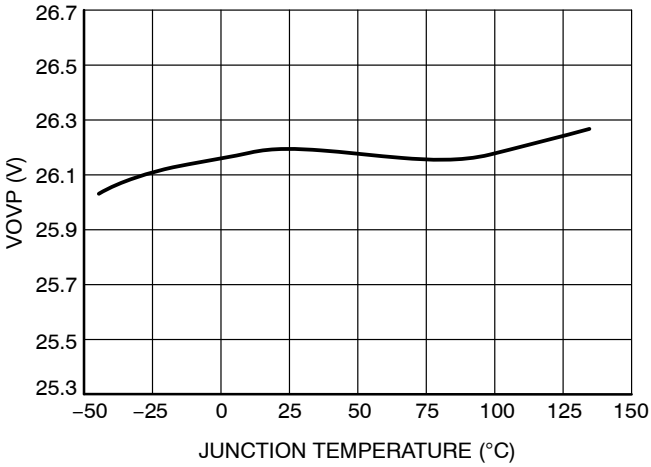

Figure 29. VOVP vs. Junction Temperature

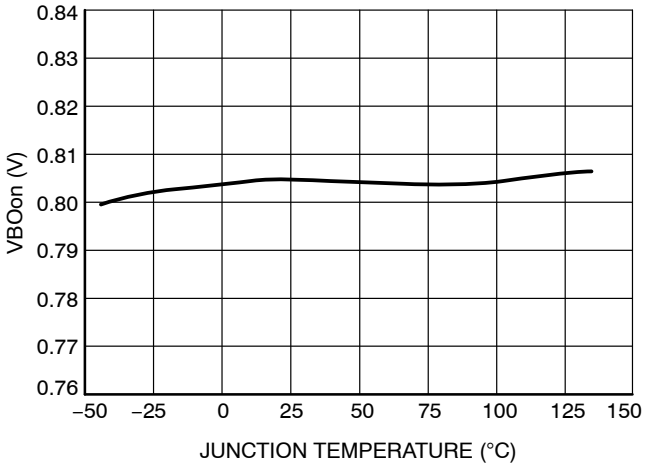

Figure 30. VBOon vs. Junction Temperature

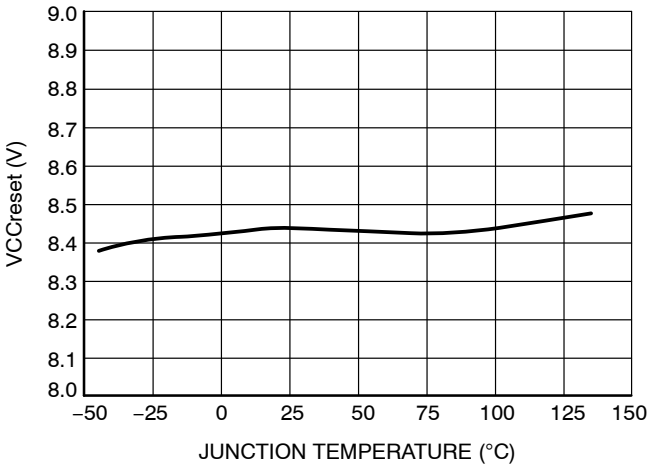

Figure 31. VCCreset vs. Junction Temperature

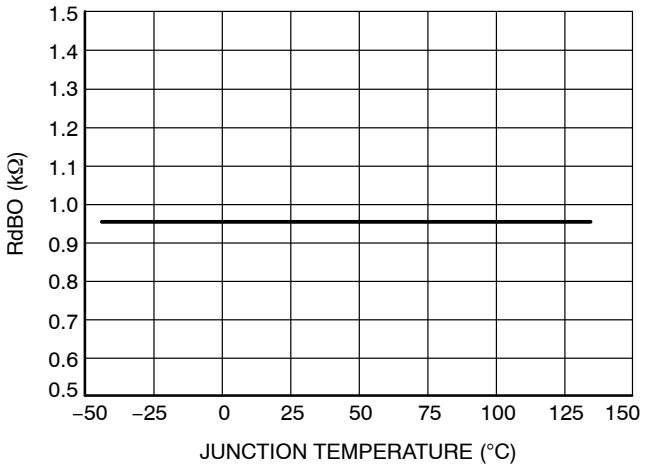

Figure 32. RdBO vs. Junction Temperature

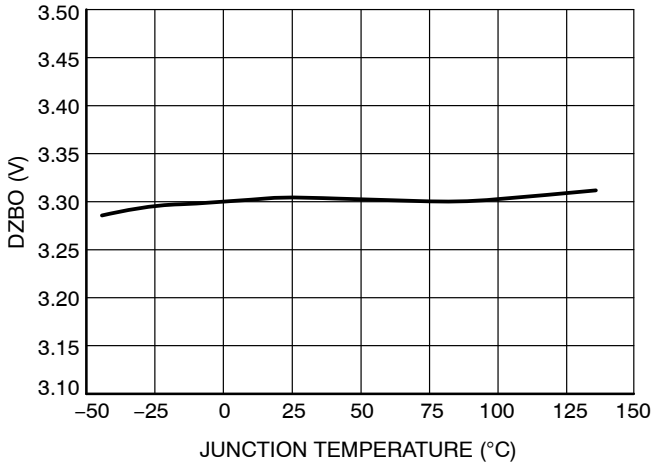

Figure 33. DZBO vs. Junction Temperature

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APPLICATION INFORMATION

NCP1256 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count and cost effectiveness are key design parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. NCP1256 brings all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a non−dissipative OPP, a brown−out protection and two independent latch inputs for OVP/OTP implementations. All these features are packed in a tiny TSOP−6 package.

- **Current−mode operation with internal slope compensation:** implementing peak current mode control at a fixed 65 kHz or 100 kHz frequency, the NCP1256 includes an internal slope compensation signal whose level will cover most of offline design cases. Additional ramp can be added via a simple scheme around the feedback or current sense pin as described below.
- **Brown−out protection:** a portion of the input mains (or the rectified bulk rail) is brought to pin 3 via a resistive network. When the voltage on this pin is too low, the part stops pulsing. No re−start attempt is made until the controller senses that the voltage is back within its normal range. When the brown−out comparator senses the voltage is acceptable, it sends a general reset to the controller (latched states are released) and authorizes re−start. Please note that a re−start is always synchronized with a VCC_{ON} transition event for a clean start−up sequence. If V_{cc} is naturally above VCC_{ON} when the BO circuit recovers, re−start is immediate.
- **Internal OPP:** the part internally buffers the brown out voltage and transforms it into a current, sourced out of the CS pin. By inserting a resistance between the sense resistor and the CS pin, the designer has the ability to build an offset and precisely adjust the OPP level he needs. Please note that the OPP current starts from 0 when the BO voltage is 0.8 V, a low−line condition. It helps pass maximum power at the lowest input voltage despite a strong compensation at high line. OPP is also disabled in frequency foldback mode for a better light−load efficiency.
- **Low startup current:** reaching a low no−load standby power always represents a difficult exercise when the controller draws a significant amount of current during start−up. Thanks to its proprietary architecture, the NCP1256 is guaranteed to draw less than 10 μA maximum (guaranteed at a 125°C T_J), easing the design of low standby power adapters.
- **EMI jittering:** an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering is kept in frequency foldback mode (light load conditions).
- **Frequency foldback capability:** a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of 1.5 V, it starts reducing switching frequency. When the feedback level reaches 1.2 V, the frequency hits its lower stop at 26 kHz. When the feedback pin goes further down and reaches 0.75 V, the peak current setpoint is internally frozen at 31% of the maximum limit. Below this point, if power continues to drop, the feedback pins passes below 0.6 V and the controller enters classical skip−cycle mode.
- **Internal soft−start:** a soft−start precludes the main power switch from being stressed upon start up and it reduces output voltage overshoots. In this controller, the soft−start is internally fixed to 4 ms. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- **OVP inputs:** the NCP1256 welcomes two inputs. One is located in the brown out input whose upper dynamic range is less than 3 V at a 375 V dc input. If an external event lifts the BO pin above 4.5 V for four consecutive clock cycles, the part permanently latches off. Noise immunity is strengthened by reducing the BO pin resistance when the voltage on the pin exceeds 3.3 V (beyond the OPP dynamic range). In the E version, the clamp is removed and the fault is fully auto−recovery for an efficient ac line OVP. The second OVP input is placed in the current sense pin and is only observed during the off−time duration. If during the off time the current sense pin is lifted above 1.5 V typically four consecutive clock cycles, the part latches off. By connecting an NTC via a diode to the auxiliary winding, a cheap and accurate OTP can be implemented. Regardless of the trip mode (BO or CS), when latched, V_{cc} hiccups between both UVLO levels while all drive pulses are off. Reset occurs when a) the BO voltage drops below $V_{BO(off)}$ during a going−down V_{cc} cycle or b) V_{cc} passes below the reset voltage VCC_{reset} which is $V_{CC(min)}$−250 mV. When either event is detected, the IC goes through a new fresh start−up sequence.
- **V_{cc} OVP:** an OVP protects the circuit against V_{cc} runaways. The fault must be present at least 20 μs to be validated. This OVP is latched, except on E version where it is auto−recovery.
- **Short−circuit protection:** short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the auxiliary winding

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level does not properly collapse in presence of an output short). In this controller, every time the internal 0.8−V maximum peak current limit is activated (or less when OPP is used), an error flag is asserted and a time period starts, thanks to the programmable timer. When the timer has elapsed, the controller enters a double−hiccup auto−recovery mode or is fully latched depending on the selected option.

Please note that with the latched OCP option, the part becomes sensitive to the UVLO event only at the first power−on sequence. Any UVLO event is ignored afterwards (normal auto−recovery operation). This is to pass the pre−short test at power up:

1. if the internal error flag is armed (short circuit) AND a UVLO event is sensed, the part is immediately latched. UVLO sensing is ignored after the first sucessful start−up sequence.
2. if an UVLO signal is detected but the error flag is not asserted, double−hiccup auto−recovery occurs and the part tries to resume operations.
3. if the error flag is asserted without UVLO, the part classically permanently latches off.

Start−up Sequence

The NCP1256 start−up voltage is purposely made high to permit large energy storage in a small V_{cc} capacitor value. This helps operate with a small start−up current which, together with a small V_{cc} capacitor, will not hamper the start−up time. To further reduce the standby power, the controller start−up current is purposely kept low, below 10 μA. Start−up resistors can therefore be connected to the bulk capacitor or directly to the mains input voltage if you wish to save a few more mW.

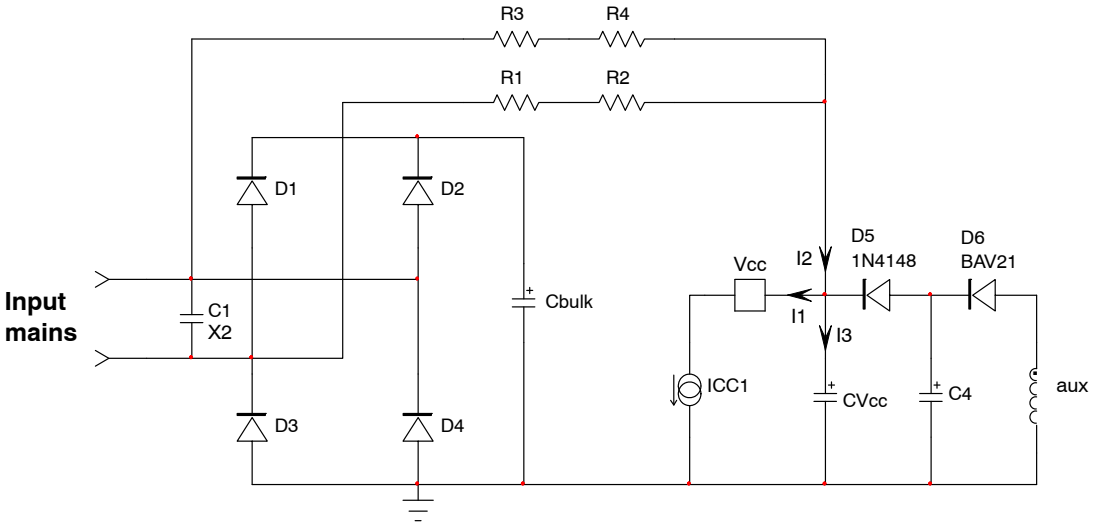

Figure 34. The startup resistor can be connected to the input mains for further power dissipation reduction

Figure 34 shows a typical recommended configuration where start−up resistors connect together to the mains input. This technique offers the benefit of freely discharging the X2 capacitor usually part of the EMI filter. The calculation of these resistors depends on several parameters. Assuming a 0.47−μF X2 capacitor, the safety standard recommends a time constant less than 1 s maximum when a resistor is connected in parallel to provide a discharge path. This sets the upper limit for the sum of discharge resistors connected to the controller V_{cc}:

$$R_{startup} < \frac{1}{0.47\ \mu} < 2.1\ M\Omega \qquad \text{(eq. 1)}$$

The first step starts with the calculation of the needed V_{cc} capacitor which will supply the controller until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 and 20 ms. Considering that we need at least an energy reservoir for a t_1 time of 10 ms, the V_{cc} capacitor must be larger than:

$$CV_{CC} \geq \frac{I_{CC}t_1}{VCC_{on} - VCC_{min}} \geq \frac{1.5\ m \times 10\ m}{9} \geq 1.6\ \mu F \qquad \text{(eq. 2)}$$

Let us select a 2.2−μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for t_1. Experiments across temperature range are important as capacitance and ESR of this V_{cc} capacitor can be affected. The V_{cc} capacitor being known, we can now evaluate the charging current we need to bring the V_{cc} voltage from 0 to the IC VCC_{on} voltage, 18 V typical. This current has to be selected to ensure start−up at the lowest mains (85 V rms) to be less than 3 s (2.5 s for design margin):

$$I_{charge} \geq \frac{VCC_{on}C_{V_{CC}}}{2.5} \geq \frac{18 \times 2.2\ \mu}{2.5} \geq 16\ \mu A \qquad \text{(eq. 3)}$$

If we account for the 10−μA current that will flow inside the controller (I_1 in Figure 34), then the total charging current delivered by the start−up resistor must be 26 μA, rounded to 30 μA. If we connect the start−up network to both

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mains inputs (two half−wave connections then), half of the average current I_1 is defined by:

$$\frac{I_1}{2} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{R_{startup}} \quad \text{(eq. 4)}$$

To make sure this current is always greater than 15 μA (half of the necessary 30−μA current), the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{I_{CV_{cc},min}} \leq \frac{\frac{85 \times 1.414}{\pi} - 18}{15\ \mu} \leq 1.3M\Omega \quad \text{(eq. 5)}$$

We could thus connect two resistors of 1.3 MΩ (total 2.6 MΩ) across the line to a) power the IC at start up b) ensure X2 discharge when the user unplugs the adapter.

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time at start up can be shorter (or longer!) and it can lead to a reduction of the V_{cc} capacitor. This brings a decrease in the charging current and an increase of the start−up resistor, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the two 1 MΩ resistors as suggested by Equation 5, the dissipated power per resistance at high line amounts to:

$$P_{R_{startup,max}} \approx \frac{V_{ac,peak}^2}{4R_{start-up}} = \frac{\left(230 \times \sqrt{2}\right)^2}{4 \times 1Meg} = \frac{105k}{4Meg} = 26mW \quad \text{(eq. 6)}$$

or a total of 52 mW.

Now that the first V_{cc} capacitor has been selected, we must ensure that the self−supply does not disappear in no−load conditions. In this mode, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the V_{cc} capacitor. If this ripple is too large, chances exist to touch the $VCC_{(min)}$ and reset the controller into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 34 elegantly solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the V_{cc} pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the controller without affecting the start−up time and standby power.

Brown−Out Protection

Brown−out (BO) is a means to protect the converter against an erratic behavior that can occur at the lowest input voltage level. By safely stopping the output pulses when the mains is below a predetermined value, the converter prevents thermal runaway, greatly improving its robustness. Brown−out protection is another way to avoid an erratic hiccup mode when too low an input voltage limits the power delivery. Some applications, such as printer power supplies, forbid this kind of operations and impose a clean stop. In that case, brown−out detection/protection is the way to go. Figure 35 shows a simplified version of what is implemented in the controller.

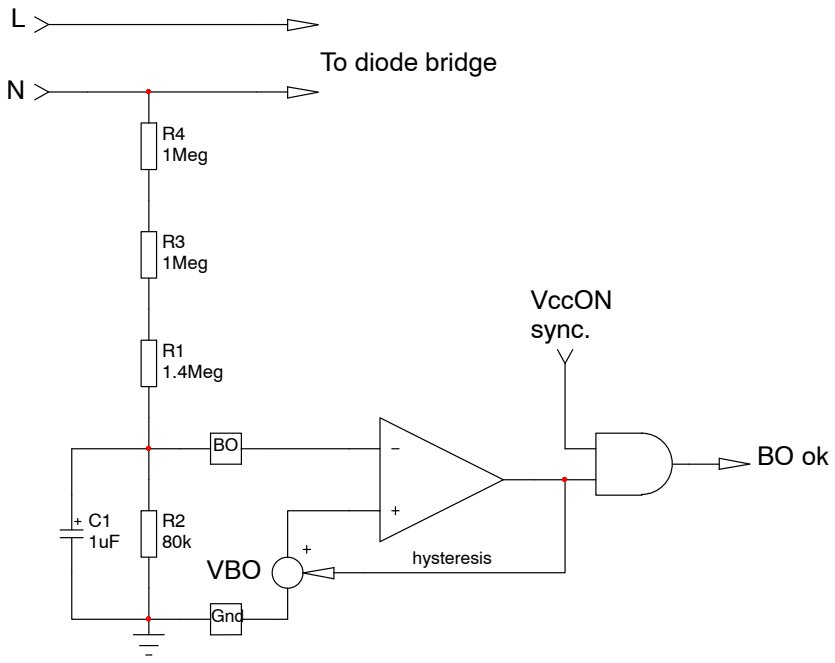

Figure 35. A simple comparator monitors the input voltage via a single pin. When this voltage is too low, the pulses are stopped and the V_{cc} hiccups

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To ensure a clean re−start, the BO information is only validated when V_{cc} reaches VCC_{ON}. This ensures a fully−charged V_{cc} capacitor when the controller pulses again (fresh start up). An asynchronous BO−related re−start could induce aborted start−up sequences if the V_{cc} capacitor would be too close to the UVLO threshold.

From the above schematic, the calculation of the resistor is straightforward. We have connected the resistor to the input line and thus observe a single−wave signal peaking to $V_{in,peak}$. The average voltage seen on top of R_4 in Figure 35 is:

$$V_{in,avg} = \frac{V_{in,peak}}{\pi} \qquad \text{(eq. 7)}$$

Then, choose a bridge current compatible with the power consumption you can accept. If we chose 10 μA, the pull−down resistor R_2 calculation is straightforward:

$$R_2 = \frac{V_{BOon}}{I_{bridge}} = \frac{0.8}{10\ \mu} = 80\ k\Omega \qquad \text{(eq. 8)}$$

Now suppose we want a typical turn−on voltage $V_{turn-on}$ of 80 V rms. From the two above equations, we can calculate the value of the upper resistive string:

$$R_{upper} = \frac{\left(\frac{V_{turn-on}\sqrt{2}}{\pi}\right) - V_{BOon}}{I_{bridge}} = \frac{\frac{80 \times 1.414}{3.14} - 0.8}{10\ \mu} = 3.5M\Omega \qquad \text{(eq. 9)}$$

The hysteresis on the internal reference source is 140 mV typically. The ratio of the two voltages is 1.14. With the upper resistive network, the turn−off voltage can then easily be derived:

$$V_{turn-off} = \frac{V_{turn-on}}{1.14} = \frac{80}{1.14} \approx 70\ V \qquad \text{(eq. 10)}$$

A 1−μF capacitor is necessary to filter out the input ripple. Reducing its value, hence allowing more ripple, can help fine−tune the hysteresis, if necessary. A simulation has been run with an upper−side resistor of 3.7 MΩ, a lower−side resistor of 80 kΩ and a 1 μF filtering capacitor. The measured turn−on voltage is 80 V rms and the turn−off voltage is around 70 V rms.

Please check the demonstration board schematic in which the BO sensing is done in a slightly different way, capitalizing on the X2 discharge resistors. Be aware that BO test has to be carried without oscilloscope probes or any leakage path that could affect the high−impedance sensing.

When the controller senses a BO event, all pulses are immediately cut. The IC internal consumption brings V_{cc} down towards UVLO. When this level is reached, the controller goes back into low−consumption mode and lifts V_{cc} up again. At VCC_{ON}, a check on the BO comparator is made: if the input level is correct, the part re−starts, if still too low, the part consumption brings V_{cc} down again. As a result, V_{cc} operates in hiccup mode during a BO event.

The below figure describes the typical waveforms obtained at start−up and in operation. Please note the synchronization of the BO validation with the VCC_{ON} point. This ensures a clean start−up sequence with a fully charged V_{cc} capacitor.

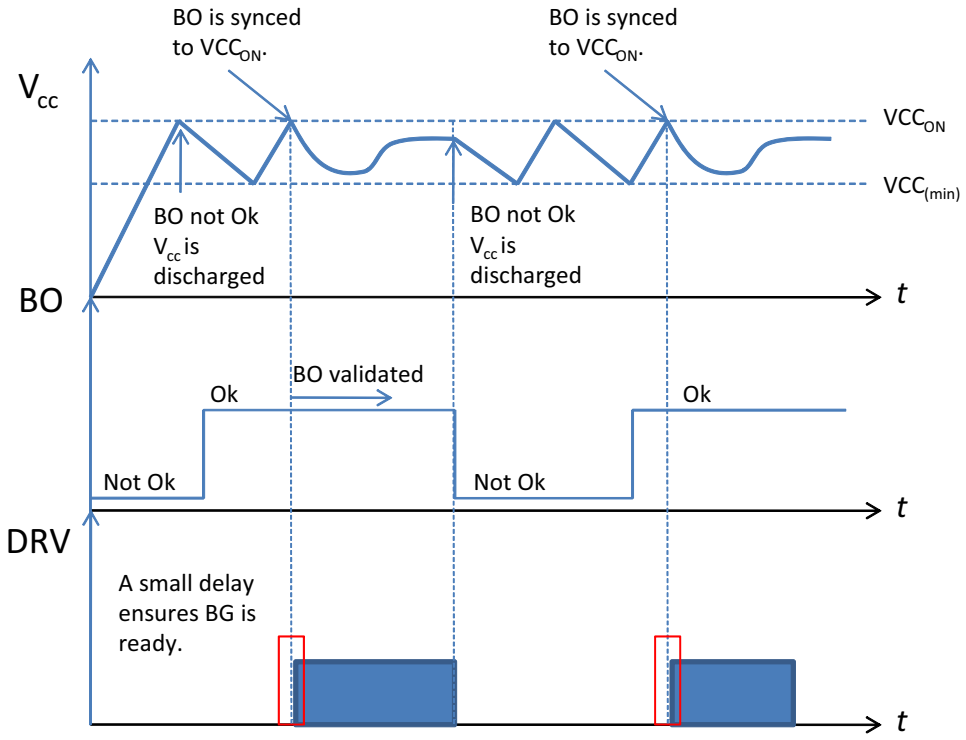

Figure 36. the brown−out recovery is always synchronized to the V_{cc} signal: when it reaches VCC_{ON}, the driver delivers the output pulses.

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Please note that the IC will restart immediately if the BO comparator sends the green light while V_{cc} is above VCC_{ON}. In that case, as V_{cc} is already high, there is no need to go through a fresh start−up sequence and the part can switch again.

Over Power Protection

Over Power Protection (OPP) is a known means to limit the output power excursion at high mains. Several elements such as propagation delays and operating mode explain why a converter operated at high line delivers more power than at low line. NCP1256 senses the input voltage via a resistive network primarily used for brown−out protection. This line image is transformed into a current information further applied to the current sense pin (CS). A resistor placed in series from the sense resistor to the CS pin will create an offset voltage proportional to the input voltage variation. An added current sink will ensure a 0 OPP current at low line, leaving the converter power capability intact in the lowest operating voltage. Figure 37 presents the internal simplified architecture of this OPP circuitry.

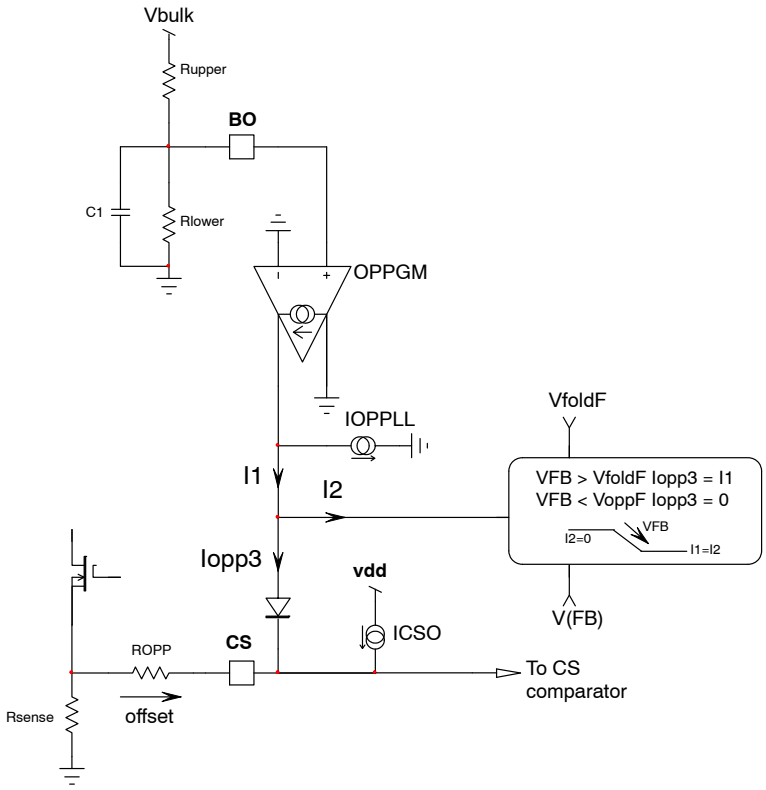

Figure 37. Over Power Protection is provided via the bulk voltage image present on Brown−Out pin

We assume the brown−out network is tweaked so that a 80−V rms input voltage brings 0.8 V on the BO pin. This is the voltage at which the adapter will start working. The voltage will be transformed into a current by the OPPGM block. Its transconductance is 115 µS, leading to a generated current of 92 µA at a 0.8 V bias. However, there is an internal fixed current sink IOPPLL calibrated so that the net current flowing into R_{OPP} is 0 at this low−voltage input. It ensures an almost non−compensated converter at low line. Now, assume a 265 V input voltage, the BO level will be 2.65 V and will generate an offset current of 185 µA as stated in the specs. In our design, as an example, say we need to reduce the maximum peak current setpoint by 250 mV to reduce the maximum power at the 265 V input. In that case, we will need to generate a 250 mV offset across R_{OPP}. With a 185 µA current, R_{OPP} should be equal to 230 m / 185 u = 1.35 kΩ. A small 100−220 pF capacitor closely connected between the CS and GND pins will form an effective noise filter and will nicely improve the converter immunity to noise. Please note that the OPP current is clamped for a BO pin voltage greater than 2.65 V. Should you lift the pin above this voltage, there will be no increase of the OPP current and the current absorbed by the pin will increase as you approach the OVP level.

The offset voltage can affect the standby power performance by reducing the peak current setpoint in light−load conditions. For this reason, it is desirable to smoothly cancel its action as soon as frequency folback occurs. A typical curve variation is shown in Figure 38. At low power, below the frequency folback starting point, 100% of the OPP current is internally absorbed and no offset is created through the CS pin. When feedback increases again and reaches the frequency foldback point, as the frequency goes up, OPP starts to build up and reaches its full value at V_{foldF} + 0.7 V.

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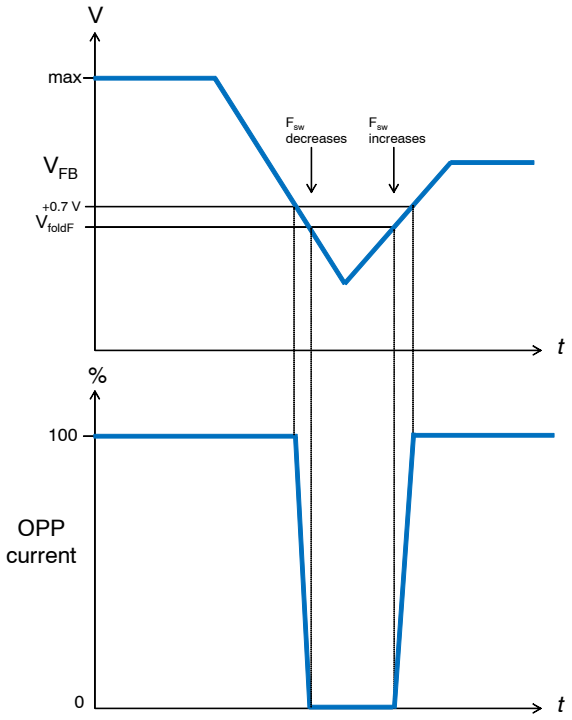

Figure 38. The OPP current is applied when the feedback voltage exceeds the folback point. It is 0 below it

Latch on Brown−Out Input

It is possible to latch the controller if an external event brings the BO input above V_{latch1} for four consecutive clock cycles. The simplified internal circuitry appear in Figure 39 where OVP is triggered from the secondary side via a dedicated optocoupler. To improve the controller noise immunity, a circuit made of an active Zener diode and a series resistor reduce the pin impedance as the voltage starts to increase above 3.3 V. More current is thus needed to actually trigger the internal latch. The example shows how an external event (an OVP in the secondary side for instance) can trip the latch. R_5 ensures enough bias circulates in the optocoupler while D_2 isolates the circuit from the high−impedance BO bridge. As the voltage on the BO pin starts increasing beyond 3.3 V, more current is drawn on the optocoupler (R_{dBO} is 1 kΩ typically) and when the BO voltage touches the 4.5−V trip point, the circuit latches off after 4 consecutive clock cycles. If the OVP assertion disappears before the counter counts to 4, a counter reset occurs.

A primary−side version of the above circuit can be implemented with the help of a single Zener diode as shown in Figure 40. The Zener will lift the BO pin when the feedback loop is lost and will latch the part immediately.

In latch−off mode, the V_{cc} keeps hiccupping for ever between VCC_{ON} and $VCC_{(min)}$ while the drive output is cut. To reset the latch, either cycle the input voltage so that the BO pin passes below V_{BOoff} or unplug the adapter until the controller V_{cc} goes below VCC_{reset}. In either case, the controller will resume via a fresh start−up sequence.

With the E version, the current clamp is removed and the fault is auto−recovery for ac line OVP implementation. You can design in two different ways:

1. You select the ac line OVP and then have a corresponding BO on: assume you design the sensing network to have 4.5 V for 320 Vrms, then, the BO on is 320 x 0.8/4.5 = 57 Vrms.
2. You select the BO on voltage and have a corresponding ac line OVP: assume a turn on voltage of 60 Vrms, then the ac line OVP voltage is set to 60 x 4.5/0.8 = 337 Vrms.

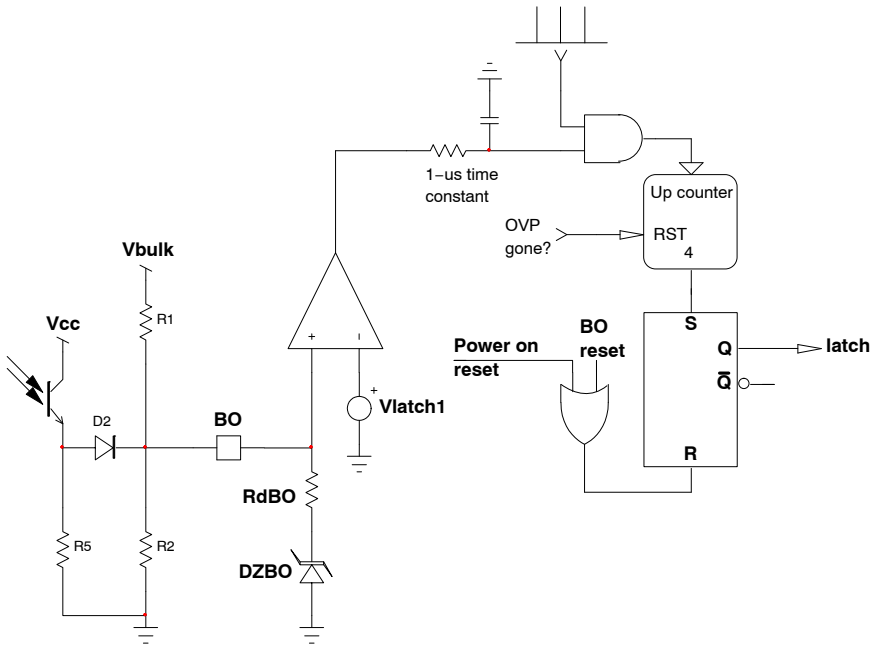

Figure 39. The circuit can easily be latched via a dedicated optocoupler observing the secondary side voltage

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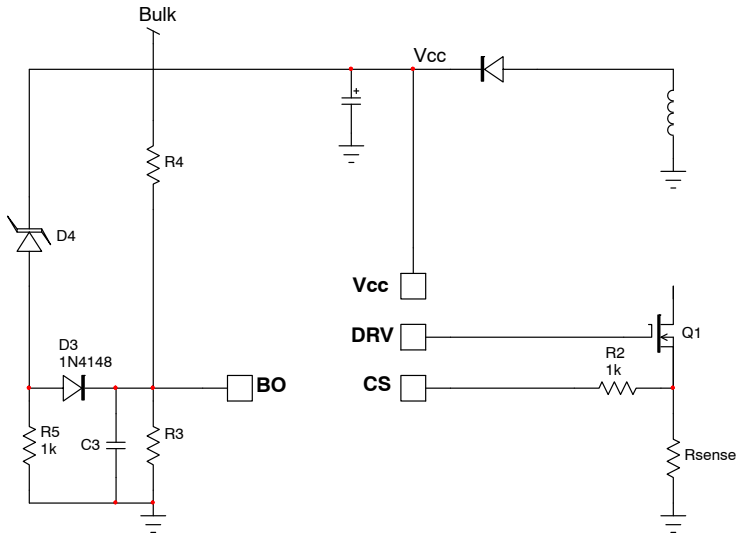

Figure 40. A simple Zener diode (D_4) can also be wired on the BO pin, latching off the part in case V_{cc} runs away (if the secondary−side LED is shorted for instance). Make sure R_3, R_4, R_5 D_3, D_4 and C_3 are closely located to the controller

Auto−Recovery Short−Circuit Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. The flag is raised at the first maximum peak current event. If the flag is asserted longer than its programmed value (70 ms typical), the driving pulses are stopped and V_{cc} falls down as the auxiliary pulses are missing. V_{cc} fall out is ensured by the part natural consumption in this mode which is around 400 μA. To ensure V_{cc} hiccup and thus autorecovery, the start−up current must always be less than these 400 μA otherwise recovery will be lost. Timer reset occurs when 8 successive resets coming from the feedback back into regulation. When the V_{cc} level crosses $VCC_{(min)}$, the controller consumption is down to a few μA and the V_{cc} slowly builds up again thanks to the resistive starting network. When V_{cc} reaches VCC_{ON}, the controller purposely ignores the re−start and waits for another V_{cc} cycle: this is the so−called double hiccup. By lowering the duty ratio in fault condition, it naturally reduces the average input power and the rms current in the output cable. Illustration of such principle appears in Figure 41. Please note that soft−start is activated upon re−start attempt.

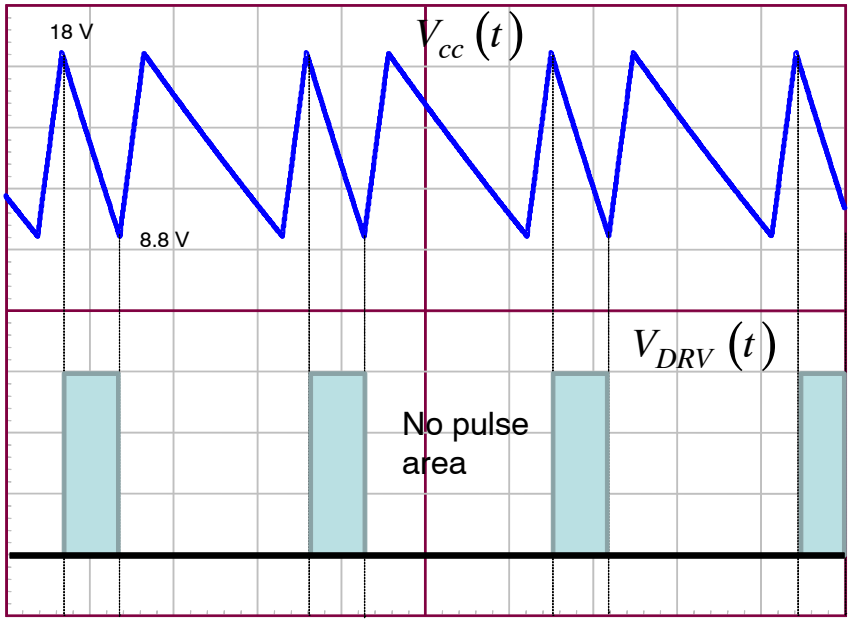

Figure 41. An auto−recovery hiccup mode is entered in case a faulty event longer than 70 ms is acknowledged by the controller

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The double hiccup is operating regardless of the brown−out level. However, when the internal comparator toggles indicating that the controller recovers from a brown−out situation (the input line was ok, then too low and back again to normal), the double hiccup is interrupted and the controller re−starts to the next available V_{cc} peak. Figure 42 displays the resulting waveform: the controller is protecting the converter against an overload. The mains suddenly went down, and then back again at a normal level. Right at this moment, the double hiccup logic receives a reset signal and ignores the next hiccup to immediately initiate a re−start signal.

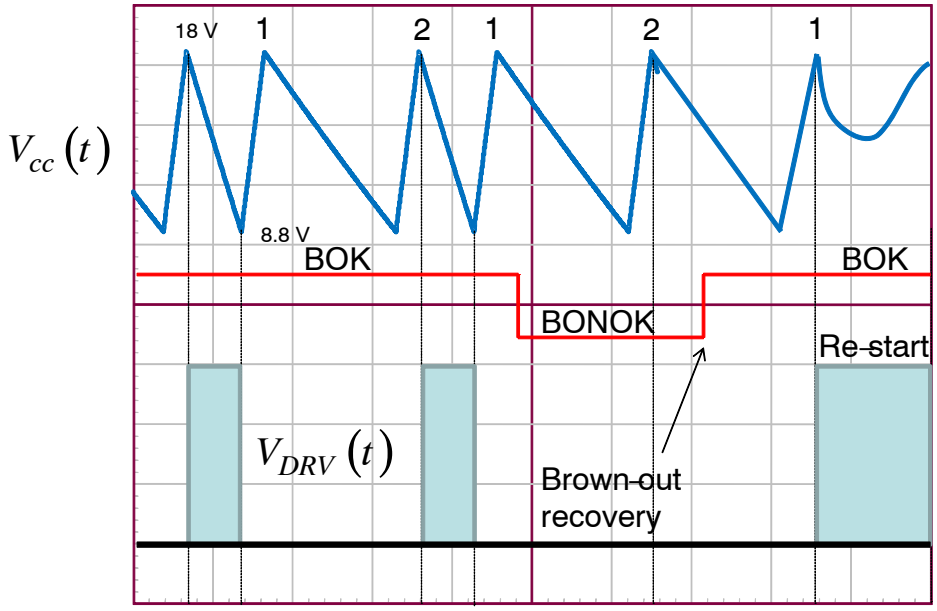

Figure 42. The hiccup latch is reset when a brown−out transition is detected to shorten the re−start time

Latched Short Circuit Protection with Pre Short

In some applications, the controller must be fully latched in case of an output short circuit presence. In that case, you would select options A in the controller list. When the error flag is asserted, meaning the controller is asked to deliver its full peak current, upon timer completion, the controller latches off: all pulses are immediately stopped and V_{cc} hiccups between the two levels, VCC_{ON} and $VCC_{(min)}$. However, in presence of a small V_{cc} capacitor, it can very well be the case where the stored energy does not give enough time to let the timer elapse before V_{cc} touches UVLO. When this happens, the latch is not acknowledged since the timer countdown has been prematurely aborted. To avoid this problem, NCP1256 (with latched−OCP option) combines the error flag assertion together with the UVLO flag to confirm a pre−short situation: upon start up, as maximum power is asked to increase V_{out}, the error flag is temporarily raised until regulation is met. If during the time the flag is raised an UVLO event is detected, the part latches off immediately. When latched, V_{cc} hiccups between the two levels, VCC_{ON} and $VCC_{(min)}$ until a reset occurs (Brown−out event or V_{cc} cycled down below VCC_{reset}). In normal operation, if a UVLO event is detected for any reason while the error flag is not asserted, the controller will naturally resume operations in a double hiccup mode. Details of this behavior are given in Figure 43.

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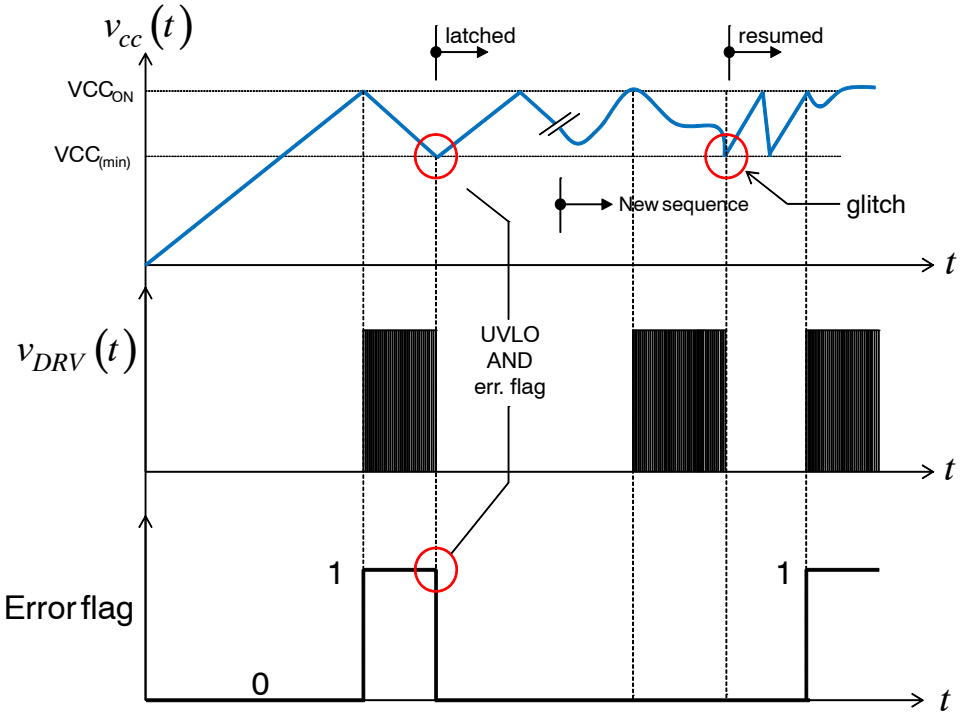

Figure 43. In case a UVLO event is sensed while the error flag is asserted, full latch occurs

UVLO latch is made available solely during the start−up sequence. When the power supply starts−up, the loop is open and asks for maximum peak current. The internal fault flag is armed and the fault timer counts down. If an UVLO event occurs during this time, the part immediately latches off. If no UVLO occurs, once the output voltage has reached regulation, the internal error flag is released and the latch authorizing UVLO detections is reset: any new UVLO events will simply be ignored. In the latched−OCP version, UVLO test is available at the first power up, when recovering from a brown−out episode or while the part operates in hiccup mode.

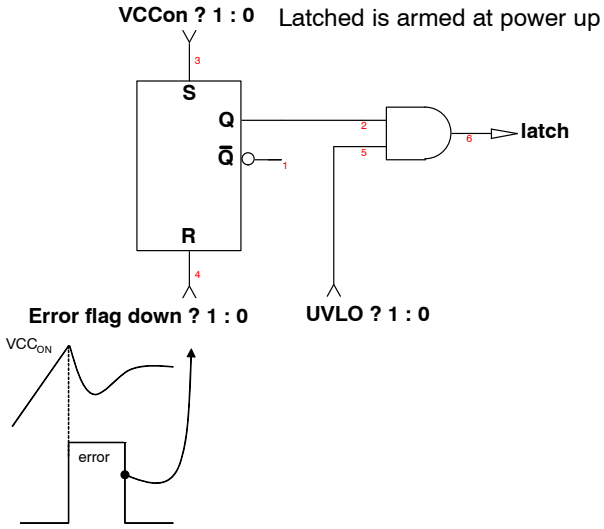

Figure 44. In case a UVLO event is sensed while the error flag is asserted, full latch occurs. UVLO observation disappears if regulation is successful after the first start−up sequence.

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Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change in the traditional fixed−frequency type of operation. This controller implements a switching frequency foldback when the feedback voltage passes below a certain level, V_{fold}, set at 1.5 V. At this point, the oscillator turns into a Voltage−Controlled Oscillator (VCO) and reduces switching frequency down to a feedback voltage of 1.2 V where switching frequency is 26 kHz typically. Below 1.2 V, the frequency is fixed and cannot go further down. The peak current setpoint is free to follow the feedback voltage from 2.4 V (full power) down to 0.75 V. At 0.75 V, as both frequency and peak current are frozen (250 mV or ≈31% of the maximum 0.8 V setpoint) the only way to further reduce the transmitted power is to enter skip cycle and chop the switching pattern. This is what happens when the feedback voltage drops below 0.6 V typically. Figure 45 depicts the adopted scheme for the part.

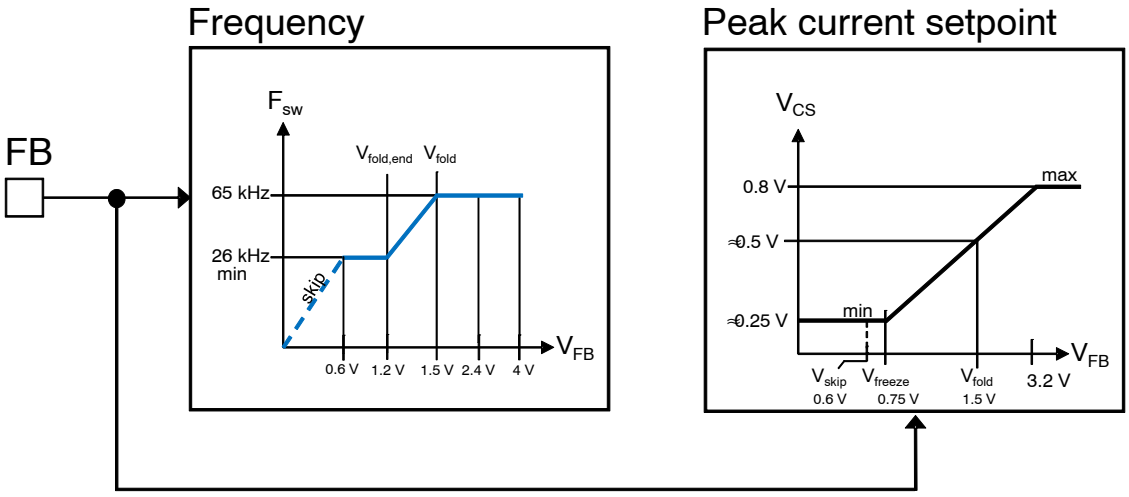

Figure 45. By observing the voltage on the feedback pin, the controller reduces its switching frequency for an improved performance at light load

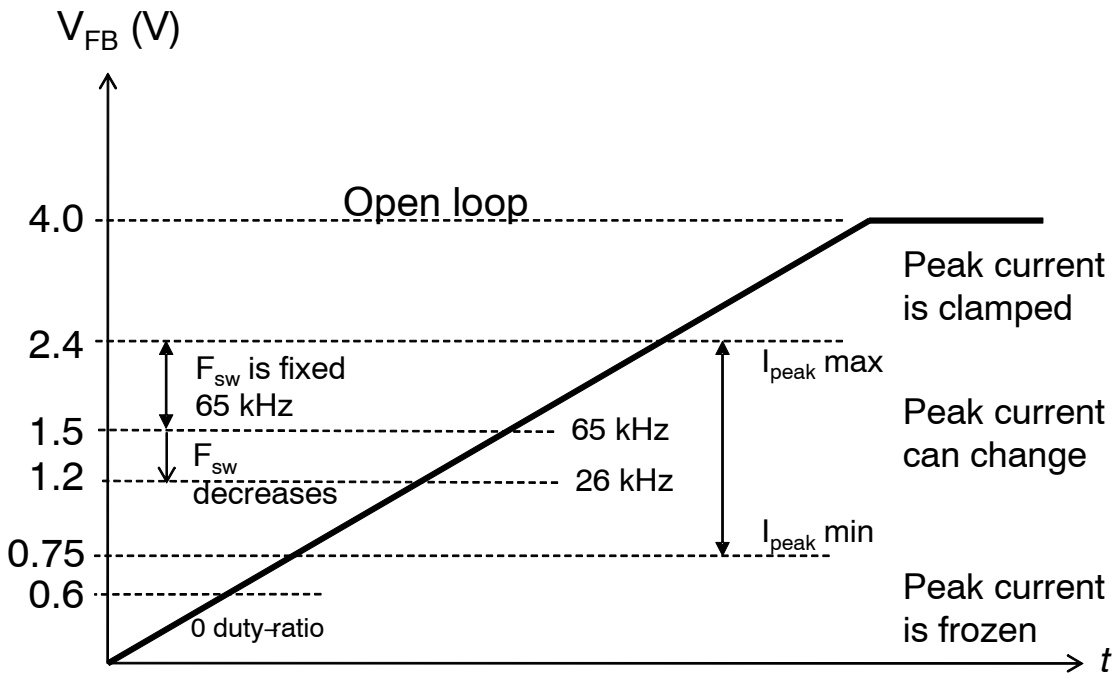

Figure 46. Another look at the relationship between feeback and current setpoint while in frequency reduction mode.

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Slope Compensation

Slope compensation is a known means to fight sub−harmonic oscillations in peak−current mode controlled power converters (flyback in our case). By adding an artificial ramp to the current sense information or subtracting it from the feedback voltage, you implement slope compensation. How much compensation do you need? The simplest way is to consider the primary−side inductor downslope and apply 50% of its value for slope compensation. For instance, assume a 65 kHz/19 V output flyback converter whose transformer turns ratio 1:*N* is 1:0.25. The primary inductor is 600 μH. As such, assuming a 1 V forward drop of the output rectifier, the downslope is evaluated to

$$S_{off} = \frac{V_{out} + V_f}{NL_p} = \frac{19 + 1}{0.25 \times 600\mu} = 133\text{kA/s or } 133\text{mA/}\mu\text{s} \quad \text{(eq. 11)}$$

If we have a 0.33−Ω sense resistor, then the current downslope turns into a voltage downslope whose value is simply

$$S'_{off} = S_{off}R_{sense} = 133\text{ k} \times 0.33 \approx 44\text{ mV/}\mu\text{s} \quad \text{(eq. 12)}$$

50% of this value is 22 mV/μs. The internal slope compensation level is typically 30 mV/μs (for the 65 kHz version) so it will nicely compensate this design example. What if my converter is under−compensated? You can still add compensation ramp via a simple *RC* arrangement showed in Figure 47. Please look at AND8029 available from www.onsemi.com regarding calculation details of this configuration.

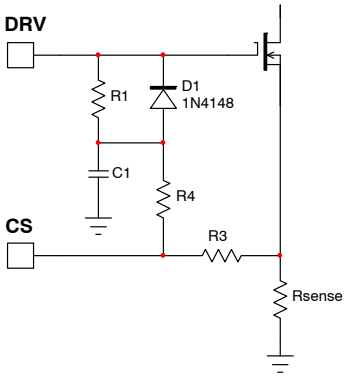

Figure 47. An easy means to add more slope compensation is by using an extra *RC* network building a ramp from the drive signal

Latching off the Controller

The part offers a dedicated latch input via the BO pin but also through the CS pin. However, latch through the CS pin is only possible if a fault voltage is applied during the off time. If we would apply the voltage during the on time, let's say by connecting a Zener diode from the auxiliary V_{cc} to the CS pin, then peak current reduction would occur as the Zener conducts and a kind of primary−regulated converter would be built. We could not latch off the part. Now, if we use the dynamic voltage present on the auxiliary winding during the off time only, we do not bias the CS pin during the on time and operations are not disturbed. In Figure 48 example, it is possible to realize overtemperature protection without using a single active element. As the auxiliary voltage is positive during the off−time duration, we can use this voltage and scale it down on the CS pin via a dedicated NTC. The series diode blocks when the auxiliary jumps negative at turn on. We recommend using a fast diode with a small junction capacitance. A BAV21 perfectly fits the bill. As temperature increases, the CS pin bias goes up during the off time, cycle by cycle. When it reaches the latch level of typically 1.5 V more than 4 consecutive clock cycles, the part fully latches off.

When latched, V_{cc} hiccups between the two levels, VCC_{ON} and $VCC_{(min)}$ until a reset occurs (Brown−out event or V_{cc} cycled down below VCC_{reset}).

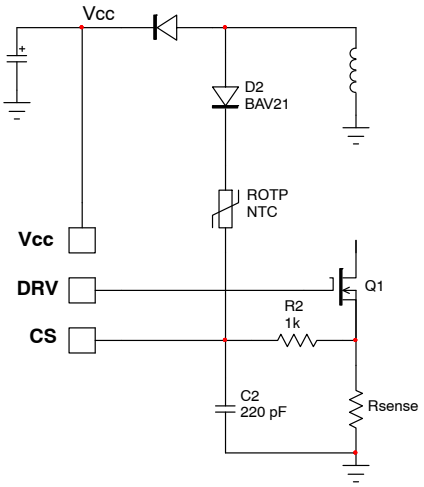

Figure 48. A simple NTC wired between the auxiliary winding and the CS pin is enough to implement a precise overtemperature protection

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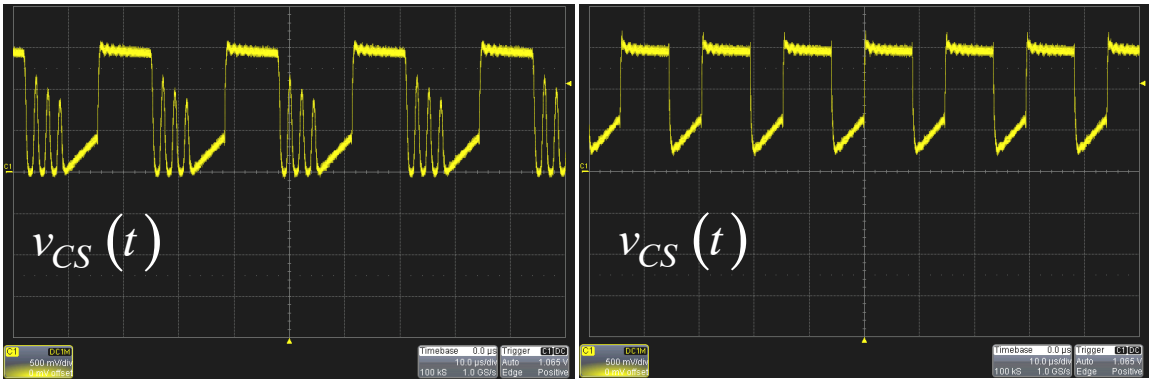

Figure 49. Typical waveforms on the CS pin with a controller almos latching off (off voltage close to 1.5 V in these shots). Left condition is light−load DCM while the right one is operating in CCM at nominal load.

A more comprehensive circuits allows a combined action from an overtemperature event and an overvoltage on the auxiliary V_{cc} (or directly via the auxiliary plateau).

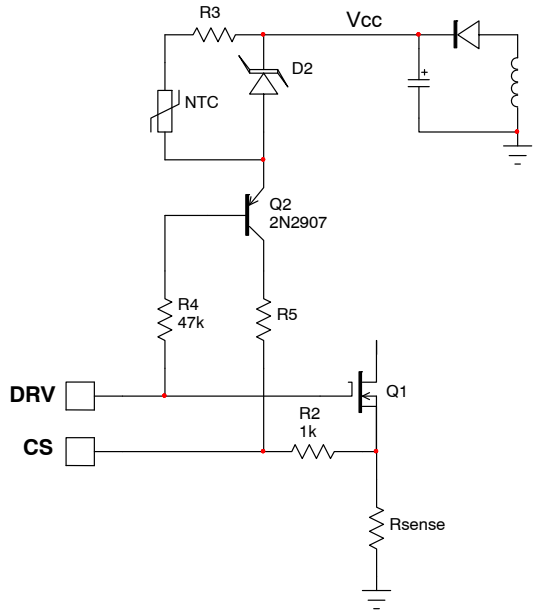

Figure 50. Adding a small PNP bipolar transistor helps combine both faulty events (OTP and OVP) on the CS pin input.

Latching off with the V_{cc} pin

The NCP1256 hosts a dedicated comparator on the V_{cc} pin. When the voltage on this pin exceeds 26 V typically for more than 20 μs, a signal is sent to the internal latch and the controller immediately stops the driving pulses while remaining in a lockout state. The part can be reset by cycling down its V_{cc}, for instance by pulling off the power plug but also if a brown−out recovery is sensed by the controller. This technique offers a simple and cheap means to protect the converter against optocoupler failures.

ORDERING INFORMATION

Controller	Marking	Frequency	OCP	OVP on BO	OVP/OTP CS	OVP V_{cc}
NCP1256ASN65T1G	6AA	65 kHz	Latched	Latched	Latched	Latched
NCP1256BSN65T1G	62A	65 kHz	Auto−recovery	Latched	Latched	Latched
NCP1256ASN100T1G	6A2	100 kHz	Latched	Latched	Latched	Latched
NCP1256BSN100T1G	622	100 kHz	Auto−recovery	Latched	Latched	Latched
NCP1256ESN65T1G	6EA	65 kHz	Auto−recovery	Auto−recovery	Auto−recovery	Auto−recovery

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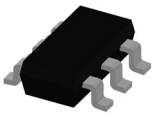

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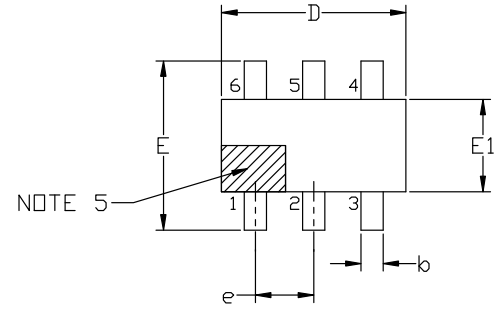
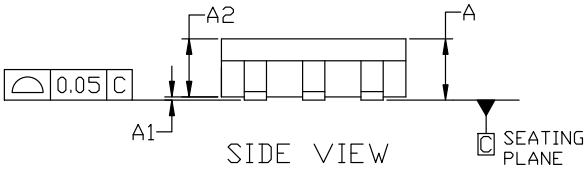
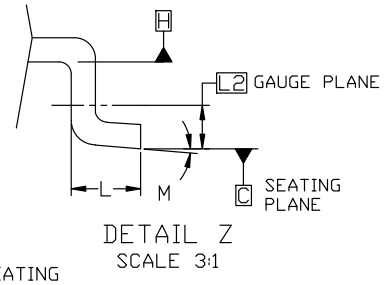
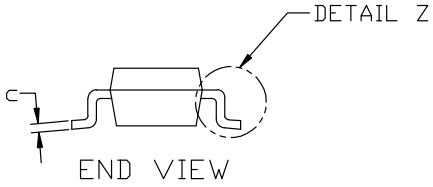


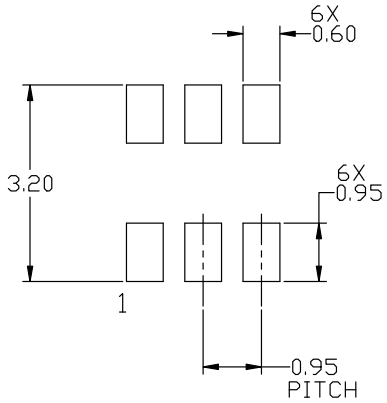






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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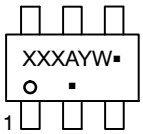
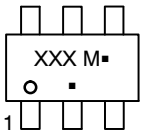
GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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