mWSaver® Integrated Power Switcher with 800 V SJ MOSFET for Offline SMPS

NCP11184, NCP11185, NCP11187

NCP1118x integrates a peak current mode PWM controller employing mWSaver technology and a highly robust 800 V SJ MOSFET providing especially enhanced performance in flyback converters. The mWSaver technology reduces switching frequency and operating current of the controller at light−load condition, which helps avoid acoustic−noise problems and even meet international power conservation standards, such as Energy Star®.

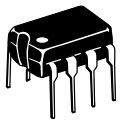
Additionally, NCP1118x includes a high−voltage startup circuit, frequency−hopping function, slope compensation, constant output power limit, and highly reliable and various protections, which allows easy design, less BOM counts, smaller PCB size and designing cost−effective off−line power supply. The protections feature a protection of a feedback pin open−loop, current−sense resistor short, brown−out and line over−voltage using an line voltage sensing pin, which operate with auto−recovery operation.

Features

- Integrated 800 V Super Junction MOSFET
- Built−in High Voltage Start−up, Soft−Start, and Slope Compensation
- mWSaver Technology Provides Industry's Best−in−Class Standby Power
- Switching Frequency Option: 65/100/130 kHz
- Proprietary Asynchronous Frequency Hopping Technique for Low EMI
- Programmable Constant Output Power Limit for Entire Input Voltage Range
- Precise Brown−out Protection and Line Over−voltage Protection (LOVP) with Hysteresis
- Current Sense Short Protection (CSSP) and Abnormal Over−Current Protection (AOCP)
- Thermal Shutdown (TSD) with Hysteresis
- All Protections Operated by Auto−recovery: VCC Under−voltage Lockout (UVLO), Feedback Open−Loop Protection (OLP), VCC Over−Voltage Protection (OVP)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

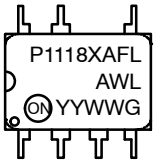
Typical Applications

- Industrial Auxiliary Power Supplies, E−metering SMPS
- Power Supplies for White Good Applications and Consumer Electronics



PDIP−7
(PDIP−8 LESS PIN 6)
CASE 626A

MARKING DIAGRAM



PDIP−7

X	= MOSFET Option
A	= Trimming Version
F	= Frequency Version
L	= Lead Forming Version
A	= Plant Code
WL	= Wafer Lot
YY	= Year of Production
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 22 of this data sheet.

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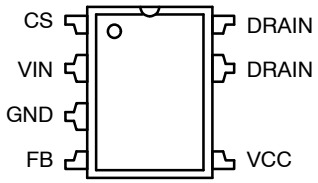
PRODUCTS INFORMATION & INDICATIVE MAXIMUM OUTPUT POWER

Part Number	Package	Switching Frequency	$R_{DS(ON)}$ (Ω) (Note 1)	Output Power Table (W) (Note 2)	
				Open Frame	
				85 ~ 265 V_{AC}	230 V_{AC}
NCP11184A065PG	PDIP7	65 kHz	2.25	35	45
NCP11185A065PG			1.3	40	55
NCP11187A065PG			0.87	50	65
NCP11184A100PG		100 kHz	2.25	33	40
NCP11187A100PG			0.87	45	60
NCP11184A130PG		130 kHz	2.25	30	36
NCP11185A130PG			1.3	37	52

1. Maximum value at T_J = 25°C.
2. Estimated maximum output power rating at T_A = 50°C not exceeding T_C of 110°C assuming DRAIN pin surrounding with a thermal relief pad 150 mm^2 in single layer PCB with 1oz. The actual output power could be varied depending on particular designs.

PIN CONFIGURATION



(Top View)
PDIP−7

Figure 1. Pin Configuration of PDIP

PIN FUNCTION DESCRIPTION

PIN #	Name	Description
1	CS	Sensing the drain current using a resistor. The sensed voltage is used for peak current mode control and cycle−by−cycle current limit. This pin also connects to a source of the integrated MOSFET
2	VIN	Detecting line input voltage. The sensed line input voltage is used for brown−out protection with hysteresis. Besides, constant output power limit is controlled with the sensed voltage. It is recommended to add a low−pass filter with this pin in parallel to reject high frequency noise and line ripple on the bulk capacitor. Pulling this pin up triggers auto−restart protection
3	GND	Ground of the controller
4	FB	Control compensation. The PWM duty cycle is determined in response of comparing the signal on this pin and the sensed drain signal on the CS pin. Typically, an opto−coupler and capacitor are connected to this pin
5	VCC	Power supply for the internal circuit operations
6, 7	DRAIN	This pin connects to an internal high voltage startup circuit and a drain of the integrated MOSFET. Typically, this pin is directly connected to one of terminals of the transformer. At initial startup or restart mode, operating voltage is powered through this pin

TYPICAL APPLICATION

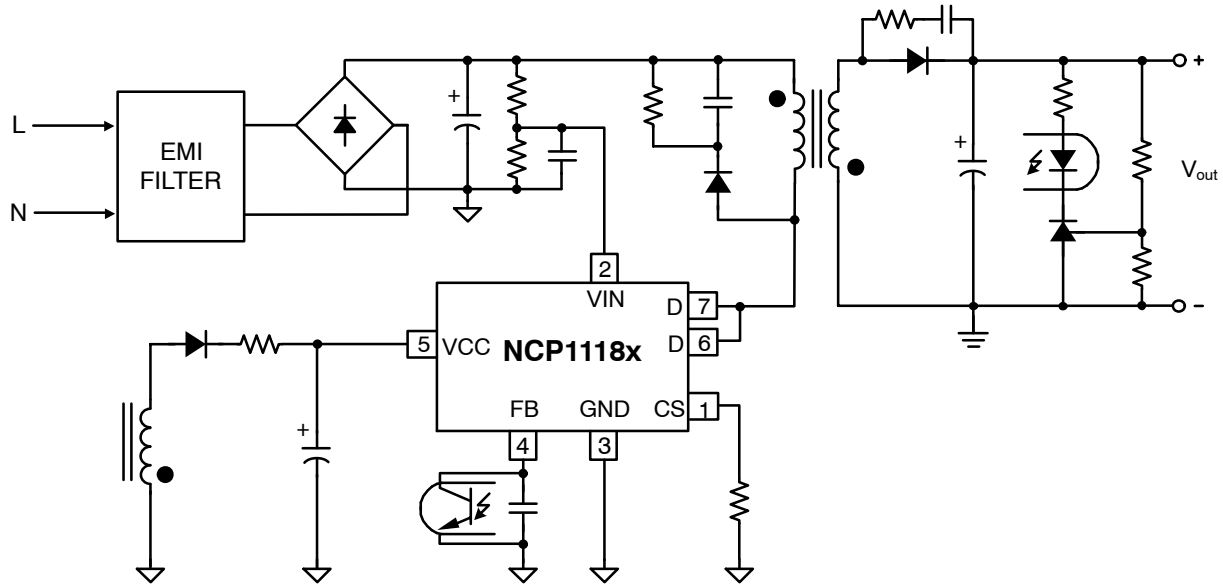


Figure 2. Typical Application (Detecting DC Voltage on Bulk−capacitor)

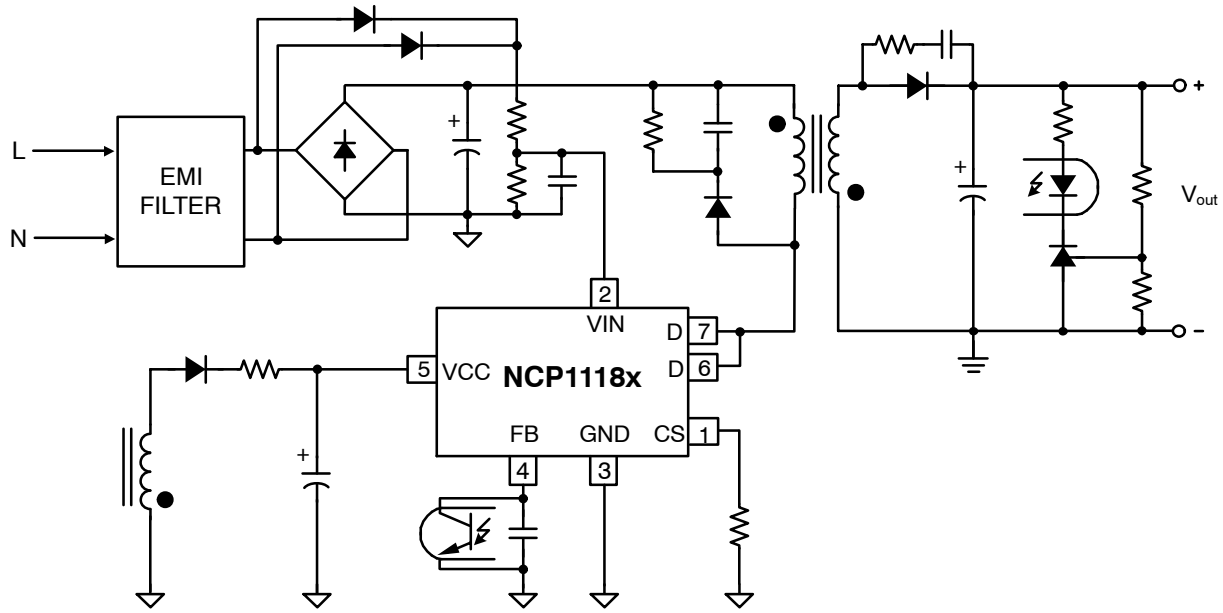


Figure 3. Typical Application (Detecting AC Input Voltage)

BLOCK DIAGRAM

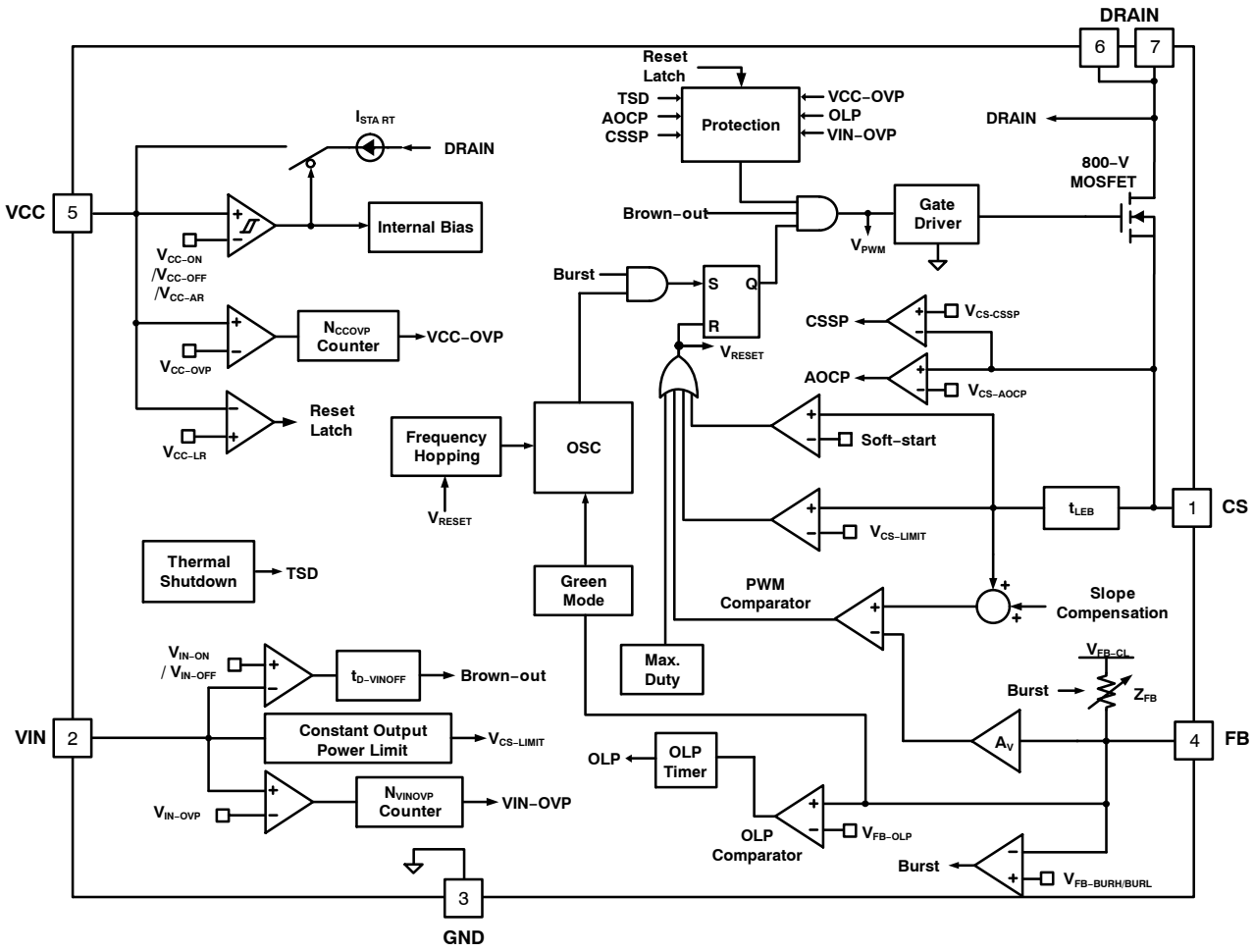


Figure 4. Simplified Internal Circuit Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
VCC Supply Voltage	V_{CC}	−0.3 to 30	V
FB Pin Input Voltage	V_{FB}	−0.3 to 5.5	V
CS Pin Input Voltage	V_{CS}	−0.3 to 5.5	V
VIN Pin Input Voltage	V_{VIN}	−0.5 to 5.5	V
DRAIN Pin Input Voltage	V_{DRAIN}	−0.3 to 800	V
Pulsed Drain Current (Note 3) NCP11184 NCP11185 NCP11187	I_{DM}	 4.2 5.4 6.8	A
Power Dissipation	P_D	1.25	W
Junction Temperature (Note 4)	T_J	−40 to +150	°C
Storage Temperature	T_{STG}	−40 to +150	°C
Lead Temperature, Wave Soldering or IT, 10 seconds	T_L	260	°C
ESD Capability HBM, JESD22−A114 All Pins Except DRAIN Pin DRAIN Pin NCP11184 / 5 NCP11187		 4.0 1.5 2.0	kV
ESD Capability CDM, JESD22−C101		1.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Repetitive rating. Pulse width is limited by maximum junction temperature. T_A = 25°C.
4. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction−to−Ambience Thermal Impedance PDIP−7 (Note 5) PDIP−7 (Note 6)	$R_{\theta JA}$	 100 70	°C/W
Junction−to−Case (Top−side) Thermal Impedance PDIP−7 (Note 6)	$R_{\theta JC}$	 11	°C/W

5. JEDEC recommended environment in JESD51−2 and test board with minimum land pad in JESD51−3.
6. Estimated in soldering a copper thermal relief pad with 200 mm^2 (0.31 sq. inch) and 2 oz. to the drain pin.

ELECTRICAL CHARACTERISTICS (T_J = −40°C to +125°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
MOSFET SECTION						
Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, V_{CS} = 0 V, I_{DRAIN} = 1 mA, T_J = 25°C	BV_{DSS}	800	–	–	V
Off−state Drain−to−Source Leakage Current	$V_{CC} \geq V_{CC-OVP}$, V_{CS} = 0 V, V_{DRAIN} = 800 V T_J = 25°C T_J =125°C	I_{DSS}	 – –	 2.05 4.57	 25 250	µA
Static Drain−to−Source On Resistance (Note 7)	V_{CC} = 15 V, T_J = 25°C NCP11184, I_{DRAIN} = 0.3 A NCP11185, I_{DRAIN} = 0.4 A NCP11187, I_{DRAIN} = 0.6 A	$R_{DS(ON)}$	 – – –	 1.87 1.05 0.70	 2.25 1.3 0.87	Ω
Static Drain−to−Source On Resistance (Note 7)	V_{VCC} = 15 V, T_J = 125°C NCP11184, I_{DRAIN} = 0.3 A NCP11185, I_{DRAIN} = 0.4 A NCP11187, I_{DRAIN} = 0.6 A	$R_{DS(ON)}$	 – – –	 3.74 2.10 1.40	 4.5 2.6 1.74	Ω
Effective Output Capacitance Time−related	V_{DS} = 0 to 400 V, V_{GS} = 0 V NCP11184 NCP11185 NCP11187	$C_{OSS(tr)}$	 – – –	 65 97 151	 – – –	pF
Effective Output Capacitance Energy−related	V_{DS} = 0 to 400 V, V_{GS} = 0 V NCP11184 NCP11185 NCP11187	$C_{OSS(er)}$	 – – –	 14 20 30	 – – –	pF
Fall Time (Note 8)	V_{CC} = 15 V, V_{DS} = 400 V, falling 90→10% NCP11184 NCP11185 NCP11187	t_f	 – – –	 22 24 20	 – – –	ns
Rise Time (Note 8)	V_{CC} = 15 V, V_{DS} = 400 V, rising 10→90% NCP11184 NCP11185 NCP11187	t_r	 – – –	 25 16 20	 – – –	ns
HV STARTUP SECTION						
VCC Threshold Voltage Switching Startup Current from I_{START1} to I_{START2}		V_{CC-SSC}	1.0	2.1	3.0	V
Startup Charging Current	V_{DRAIN} > 40 V, V_{CC} = 0 V	I_{START1}	0.2	0.5	0.8	mA
Startup Charging Current	V_{DRAIN} > 40 V, V_{CC} = V_{CC-ON} − 0.5 V	I_{START2}	2.7	4.5	6.3	mA
Minimum Required Drain Voltage for Startup (Note 9)		V_{D-STR}	25	–	–	V
VCC SUPPLY SECTION						
VCC Turn−on Threshold Voltage		V_{CC-ON}	14	16	18	V
VCC Turn−off Threshold Voltage		V_{CC-OFF}	6.8	7.8	8.8	V
Operating Current before V_{CC-ON}	V_{CC} = V_{CC-ON} − 0.5 V	$I_{CC-INIT}$	–	30	–	µA
Operating Supply Current	V_{CC} = 15 V, V_{FB} = 4.5 V, Open DRAIN pin, 65−kHz Version NCP11184 NCP11185 NCP11187 100−kHz Version NCP11184 NCP11187 130−kHz Version NCP11184 NCP11185	I_{CC-OP1}	 – – – – – – –	 1.6 2.0 2.6 1.9 3.3 2.2 3.0	 – – – – – – –	mA
Operating Supply Current without Switching	V_{CC} = 15 V, V_{FB} = 0 V	I_{CC-OP2}	–	500	–	µA

ELECTRICAL CHARACTERISTICS (T_J = −40°C to +125°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VCC SUPPLY SECTION						
Soft−start Time	$V_{FB} = V_{FB-CL}$ 65/130 kHz Version 100 kHz Version	t_{SS}	 4.0 5.2	 5.5 7.15	 7.0 9.1	ms
V_{CC} Threshold Voltage Switching Operating Current after Protection Mode		V_{CC-SOP}	9	10.2	11.4	V
Operating Current after Protection	V_{CC-AR} + 0.2 V	I_{CC-OP3}	60	100	140	μA
Protection Reset V_{CC} Threshold Voltage		V_{CC-AR}	6.4	7.4	8.4	V
OSCILLATOR SECTION						
Switching Frequency	V_{FB} = 4.5 V (V_{FB-OLP}), T_J = 25°C 65 kHz Version 100 kHz Version 130 kHz Version	f_{OSC}	 62 95 124	 65 100 130	 68 105 136	kHz
Frequency Variation vs. Temperature Deviation (Note 9)	V_{FB} = 4.5 V $T_A = T_J$ = −40 to 125°C	f_{DT}	−	−	7.5	%
Frequency Modulation Range	V_{FB} = 4.5 V (V_{FB-OLP}) 65 kHz Version 100 kHz Version 130 kHz Version	f_M	 ±5.1 ±7.8 ±10.5	 ±6 ±9.2 ±12.5	 ±6.9 ±10.6 ±14.5	kHz
Hopping Period	T_J = 25°C	t_{HOP}	7	14.5	22	ms
PWM CONTROL SECTION						
Feedback(FB) Voltage Attenuation (Note 9)	V_{FB} = 2~2.2 V	A_V	1/4.5	1/4.0	1/3.5	−
FB Impedance	V_{FB} = 4 V	Z_{FB}	10.4	15.65	20.9	kΩ
FB Clamp Voltage	FB Pin Open	V_{FB-CL}	4.75	5.1	5.4	V
Maximum Duty Cycle		D_{MAX}	70	80	90	%
Current Limit Threshold Voltage	V_{IN} = 1 V V_{IN} = 3 V	$V_{CS-LIMIT}$	0.77 0.64	0.83 0.70	0.89 0.76	V
Current Limit Delay Time	T_J = 25°C	t_{CLD}	−	330	450	ns
Leading Edge Blanking Time (Note 9)	Steady State	t_{LEB}	255	305	355	ns
Slope Compensation Generation Delay Time (Note 9)	65 kHz Version 100 kHz Version 130 kHz Version	t_{D-SE}	− − −	6 4 2.99	− − −	μs
Slope Compensation (Note 9)	Normalized to CS Signal 65 kHz Version 100 kHz Version 130 kHz Version	S_E	 − − −	 30 46 60	 − − −	mV/μs
GREEN/BURST MODE SECTION						
Green−mode Start Threshold Voltage	T_J = 25°C	V_{FB-SG}	−	3.0	−	V
Green−mode End Threshold Voltage	T_J = 25°C	V_{FB-EG}	−	2.4	−	V
Green−mode Start Frequency	$V_{FB} = V_{FB-SG}$ 65 kHz Version 100 kHz Version 130 kHz Version	f_{OSC-SG}	 − − −	 58.5 90 117	 − − −	kHz
Green−mode End Frequency	$V_{FB} = V_{FB-EG}$ 65 kHz Version 100 kHz Version 130 kHz Version	f_{OSC-EG}	 − − −	 25.6 28 29	 − − −	kHz
Burst−mode Start Threshold Voltage		$V_{FB-BURL}$	1.3	1.6	1.9	V
Burst−mode End Voltage		$V_{FB-BURH}$	1.5	1.8	2.1	V

ELECTRICAL CHARACTERISTICS (T_J = −40°C to +125°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
GREEN/BURST MODE SECTION						
Burst−mode Hysteresis Voltage	$V_{FB-BURH} - V_{FB-BURL}$	$V_{BUR-HYS}$	−	0.2	−	V
Frequency Before Burst−mode	$V_{FB} = V_{FB-BURL}$	$f_{OSC-BUR}$	20	23	26	kHz
FB Impedance in Burst−mode	$V_{FB} < V_{FB-BURL}$, $V_{CC} > V_{CC-ZFB}$	Z_{FB-BUR}	55	70	85	kΩ
FB Impedance Switching Time from Z_{FB-BUR} to Z_{FB}	T_J = 25°C	t_{ZFB}	3.6	6.2	8.8	ms
V_{CC} Threshold Voltage to Force Z_{FB} Reset	$V_{FB} < V_{FB-BURL}$, V_{CC} Decrease	V_{CC-ZFB}	9	10	11	V
PROTECTION SECTION						
V_{CC} Over−Voltage Protection (OVP)		V_{CC-OVP}	24.5	26	27.5	V
V_{CC} OVP Debounce Counting Number	65 kHz Version 100/130 kHz Version	N_{VCCOVP}	5 11	6 12	− −	pulse
Brown−in Threshold Voltage	V_{CC}= V_{CC-ON} during HV start−up	V_{IN-ON}	0.85	0.9	0.95	V
Brown−out Threshold Voltage		V_{IN-OFF}	0.66	0.70	0.74	V
Brown−out Debounce Time	$V_{FB} = V_{FB-CL}$, T_J = 25°C 65/130 kHz Version 100 kHz Version	$t_{D-VINOFF}$	 45.0 58.5	 62.5 81.2	 70.0 91.0	ms
V_{IN} Over−voltage Protection (OVP) Threshold Voltage		V_{IN-OVP}	3.65	3.85	4.05	V
V_{IN} OVP Release Hysteresis		$V_{IN-OVPHYS}$	−	0.2	−	V
V_{IN} OVP Debounce Counting Number	65 kHz Version 100/130 kHz Version	N_{VINOVP}	5 11	6 12	− −	pulse
FB Open−loop Protection (OLP) Threshold Voltage		V_{FB-OLP}	4.1	4.5	4.9	V
FB OLP Debounce Time	$V_{FB} = V_{FB-CL}$, T_J = 25°C 65/130 kHz Version 100 kHz Version	t_{D-OLP}	 47 58	 60 75	 73 92	ms
Abnormal Over−current Protection (AOCP) Threshold Voltage	Default: Enable after t_{SS}	$V_{CS-AOCP}$	1.15	1.25	1.35	V
Abnormal Over−current Blanking Time (Note 9)		$t_{ON-AOCP}$	75	110	145	ns
AOCP Debounce Counting Number	Counting GATE Pulses	N_{AOCP}	−	3	−	Pulses
Current Sensing Short Protection (CSSP) Threshold Voltage	V_{IN} = 1 V V_{IN} = 3 V	$V_{CS-CSSP}$	70 145	95 175	120 205	mV
PWM On−time to Trigger CSSP	65 kHz Version 100kHz Version 130kHz Version	$t_{ON-CSSP}$	4.05 2.35 1.6	4.6 3.0 2.0	5.15 3.62 2.4	μs
CSSP Debounce Counting Number	Counting GATE Pulses	N_{CSSP}	−	2	−	Pulses
Thermal Shutdown (TSD) Junction Temperature (Note 9)		T_{SD}	130	140	150	°C
TSD Release Hysteresis (Note 9)		T_{SD-HYS}	−	50	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. The parameter, although guaranteed, is fully tested in wafer test process.
8. Evaluated in a typical flyback converter with T_A = 25°C.
9. This parameter is not tested in production, but verified by design or characterization.

TYPICAL CHARACTERISTICS

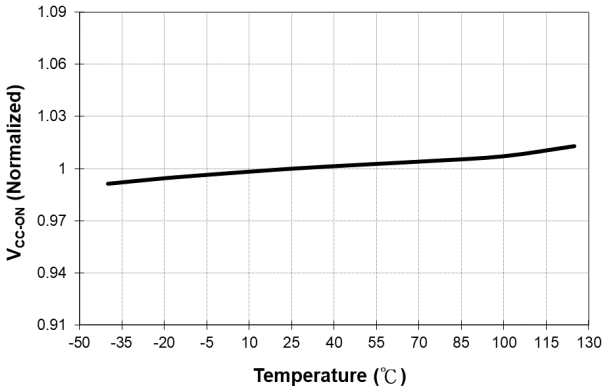


Figure 5. V_{CC-ON} vs. T_J

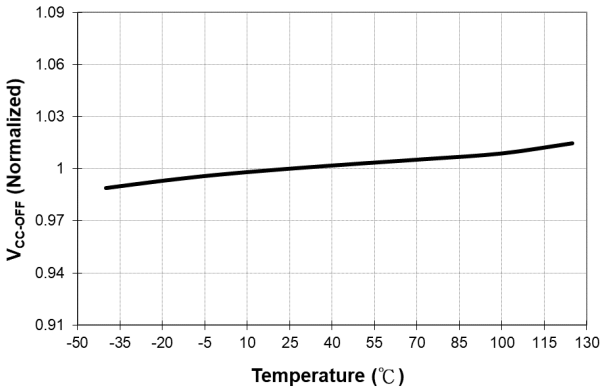


Figure 6. V_{CC-OFF} vs. T_J

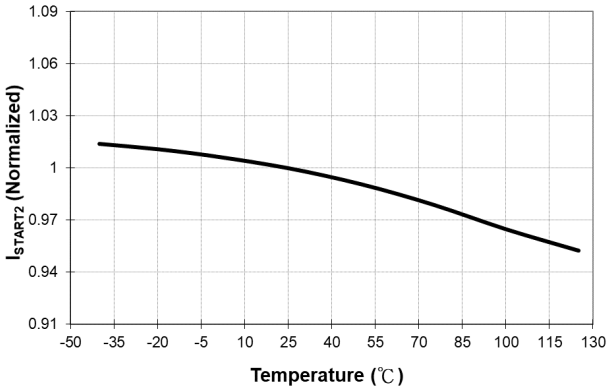


Figure 7. I_{START2} vs. T_J

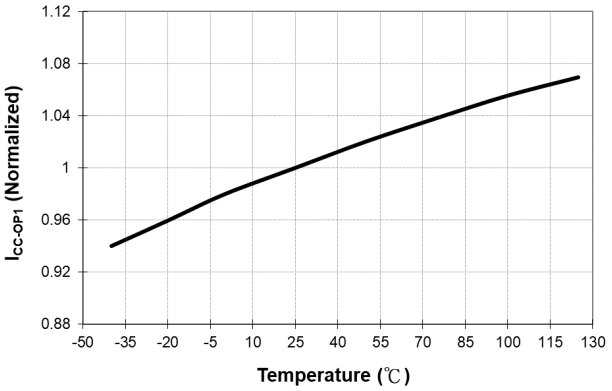


Figure 8. I_{CC-OP1} vs. T_J

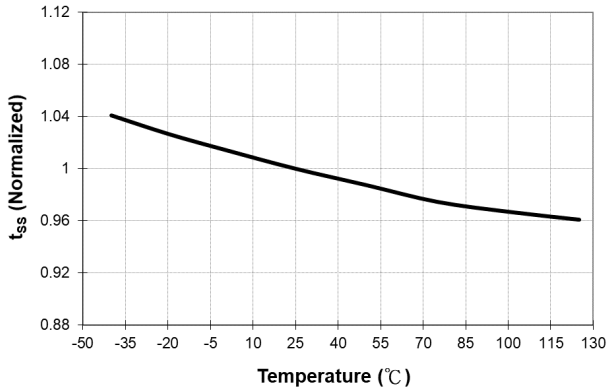


Figure 9. t_{SS} vs. T_J

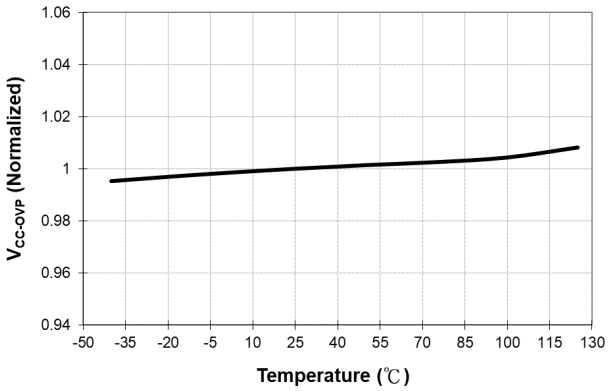


Figure 10. V_{CC-OVP} vs. T_J

TYPICAL CHARACTERISTICS (Continued)

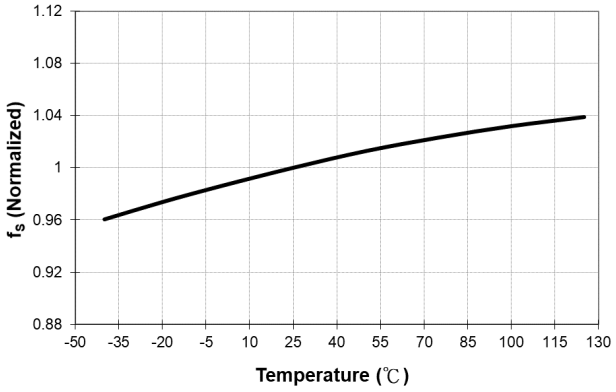


Figure 11. f_S vs. T_J

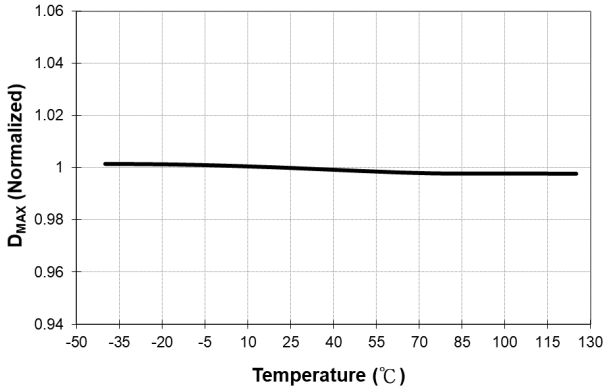


Figure 12. D_{MAX} vs. T_J

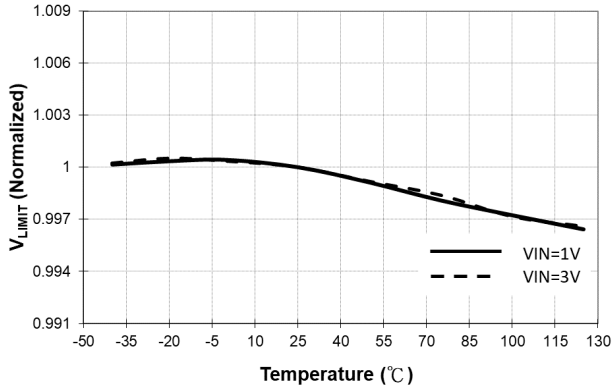


Figure 13. V_{LIMIT} vs. T_J

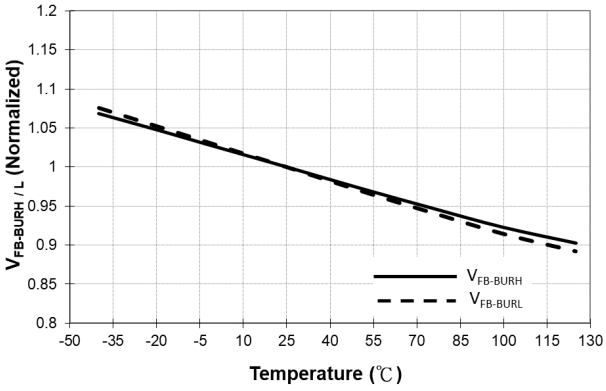


Figure 14. $V_{FB-BURH/L}$ vs. T_J

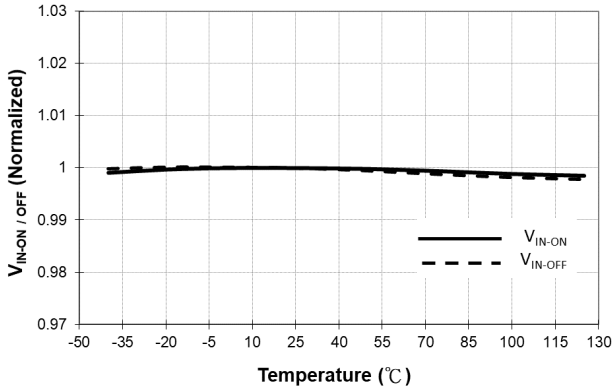


Figure 15. $V_{IN-ON/OFF}$ vs. T_J

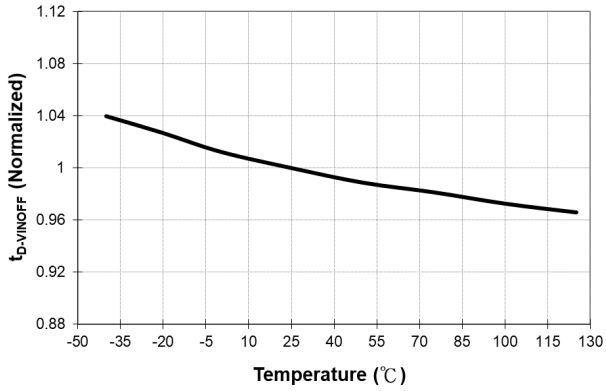


Figure 16. $t_{D-VINOFF}$ vs. T_J

TYPICAL CHARACTERISTICS (Continued)

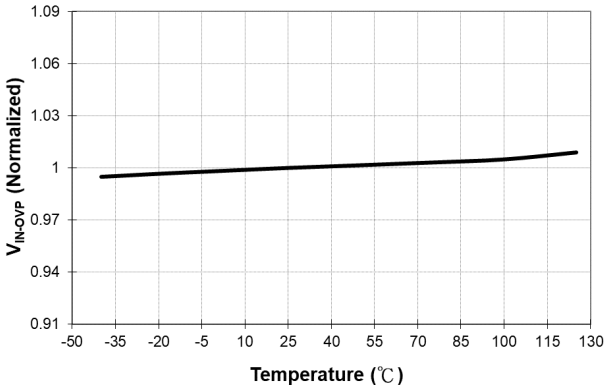


Figure 17. V_{IN-OVP} vs. T_J

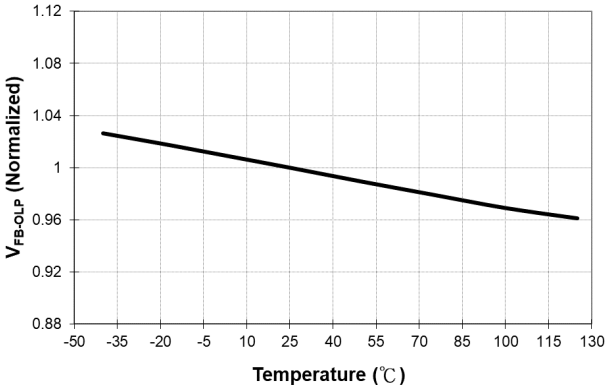


Figure 18. V_{FB-OLP} vs. T_J

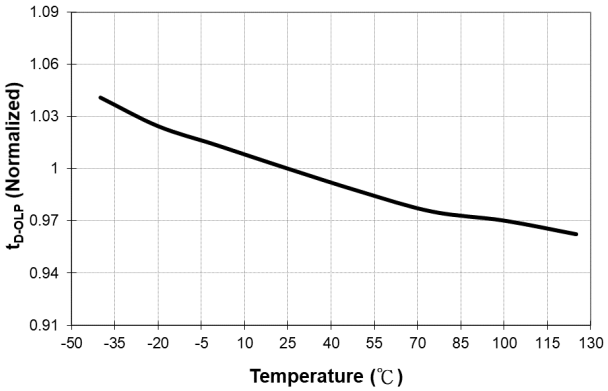


Figure 19. t_{D-OLP} vs. T_J

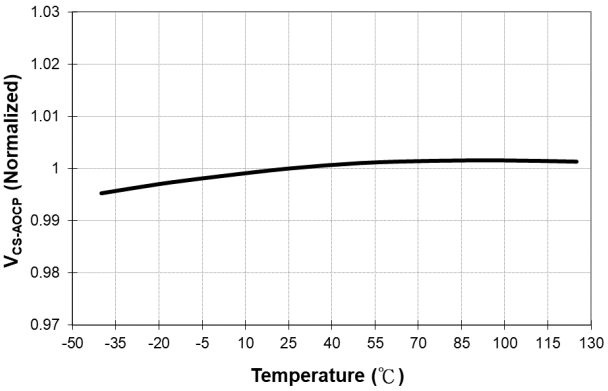


Figure 20. $V_{CS-AOCP}$ vs. T_J

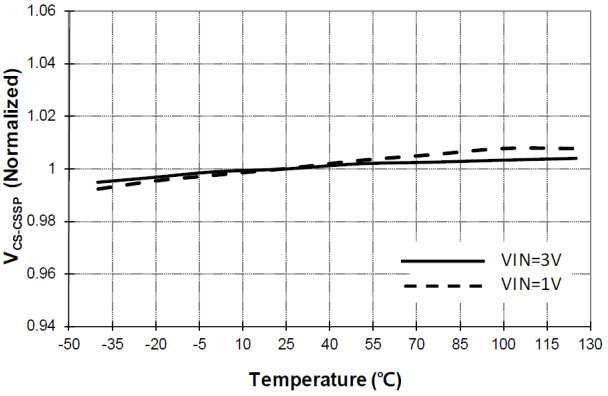


Figure 21. $V_{CS-CSSP}$ vs. T_J

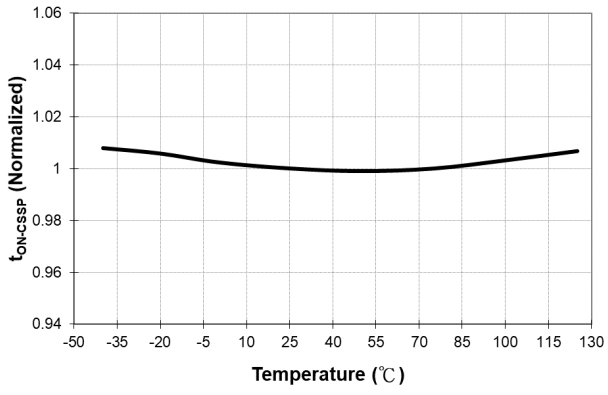


Figure 22. $t_{ON-CSSP}$ vs. T_J

TYPICAL CHARACTERISTICS (Continued)

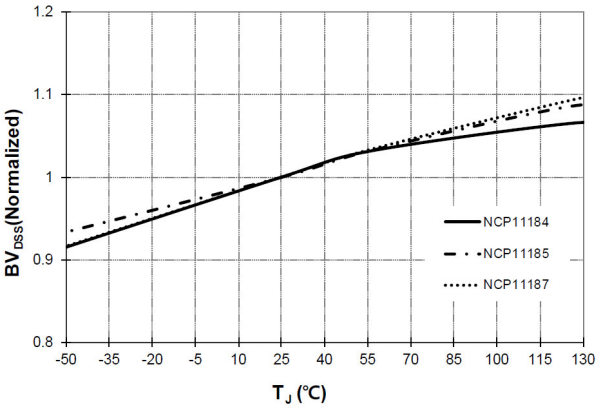


Figure 23. Normalized BV_{DSS} vs. T_J

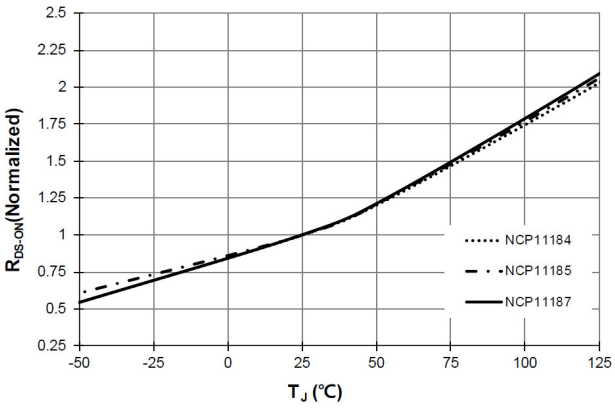


Figure 24. $R_{DS(ON)}$ vs. T_J

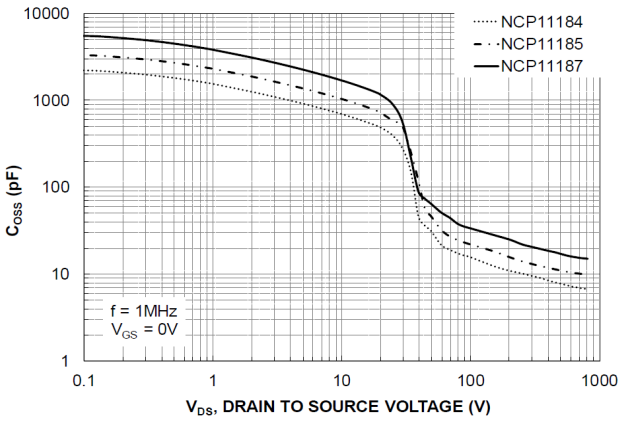


Figure 25. Output Capacitance vs. V_{DS}

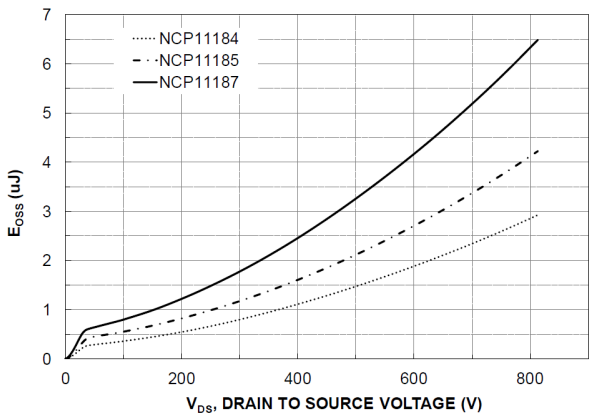


Figure 26. Energy Loss in C_{OSS} vs. V_{DS}

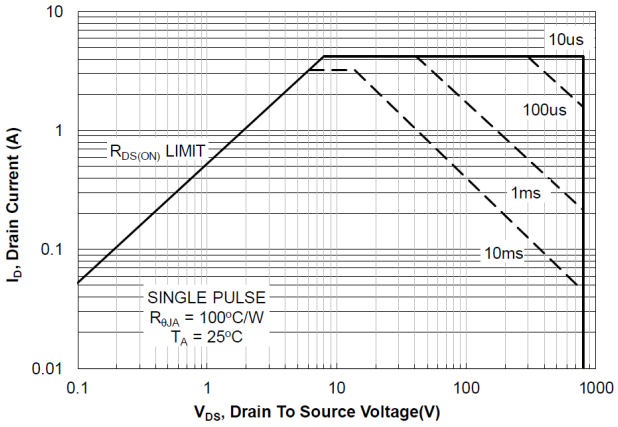


Figure 27. Safe Operating Area, NCP11184

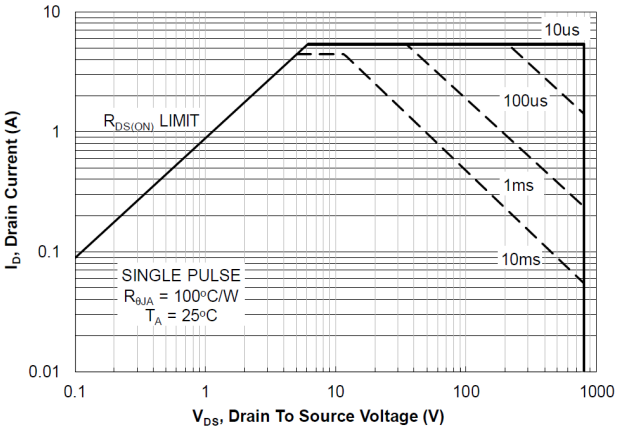


Figure 28. Safe Operating Area, NCP11185

TYPICAL CHARACTERISTICS (Continued)

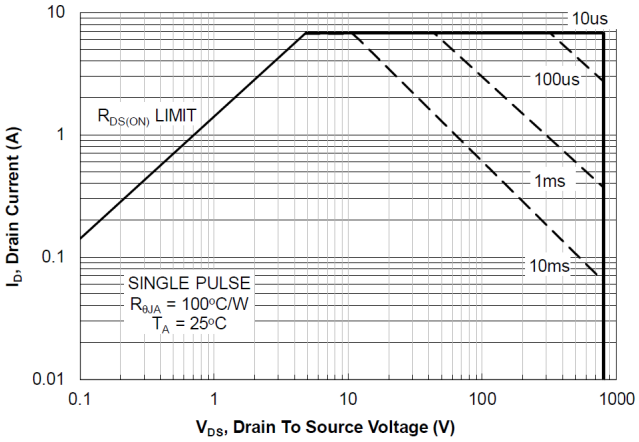


Figure 29. Safe Operating Area, NCP11187

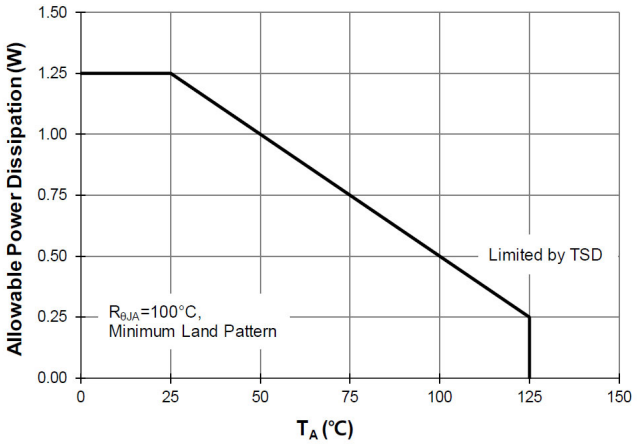


Figure 30. Allowable Power Dissipation vs. T_A

FUNCTIONAL DESCRIPTION

Startup & Soft−Start

At startup, an internal high−voltage(HV) startup circuit connecting the DRAIN pin supplies a constant startup current to internal circuits while charging the rest of current the external capacitor C_{VCC} as shown in Figure 31. While V_{CC} is lower than V_{CC-SSC}, the startup charging current is as small as ISTART1 to avoid NCP1118x damage when V_{CC} is shorted to the ground. Whereas, once V_{CC} exceeds V_{CC-SSC}, the startup charging current becomes I_{START2}, which allows being fast startup.

After V_{CC} reaches V_{CC-ON}, the HV startup circuit is deactivated and NCP1118x begins soft−startup with increasing step−wise drain currents of the MOSFET to minimize an inrush current and reduce an output voltage overshoot during internal soft−start time t_{SS}. Meanwhile, during this time, NCP1118x operates by the only supply current from C_{VCC} until the auxiliary winding of main transformer provides sufficient operating current. Selecting sufficient C_{VCC} is required. Otherwise, V_{CC} could be decreased to V_{CC-OFF} and V_{CC} under−voltage lockout protection is triggered.

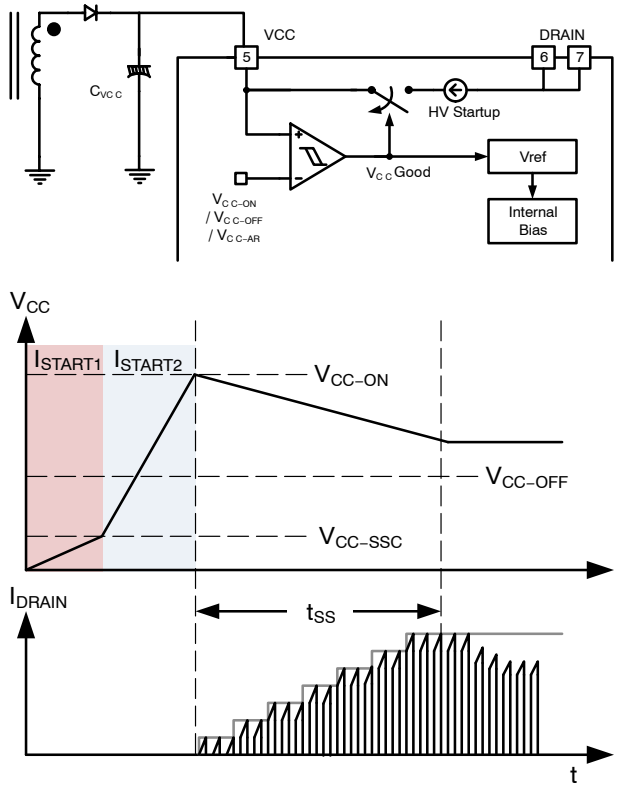


Figure 31. HV Startup Circuit and Soft Start

Auto Restart Operation

NCP1118x offers auto restart mode for the protections like feedback open−loop protection (OLP), VCC over−voltage protection (VCC OVP), and thermal shutdown (TSD) by over−temperature. Once one of the protections is triggered, the IC stops switching operation immediately and V_{CC} starts decreasing by the internal operating current I_{DD-OP2}. Then, after V_{CC} decreases lower than V_{CC-SOP}, V_{CC} is discharged by I_{DD-OP3}. As soon as V_{CC} decreases to V_{CC-AR}, all of protections is reset and the IC restart up, which secure a long enough restart time after a protection.

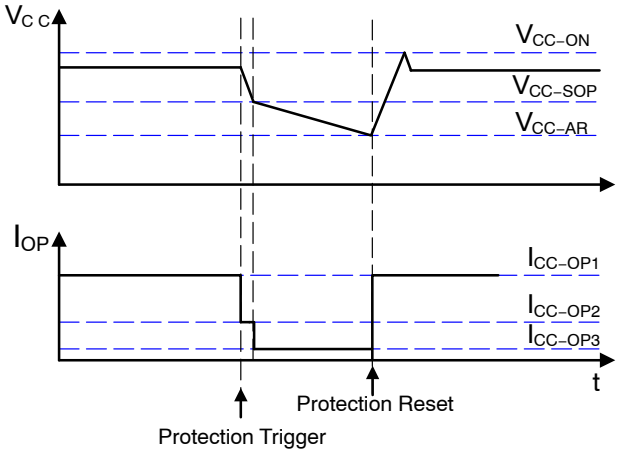


Figure 32. V_{CC} Behavior in Auto Restart Mode

Latch Operation

Protections with latch mode are available in latch−version products optionally. When any protections is triggered in the product, the switching is stopped immediately and V_{CC} decreases. Once V_{CC} touches V_{CC-AR}, the internal HV startup circuit restarts to supply operating current. However, no switching operation will be taken place until V_{CC} decreases to V_{CC-LR} and a protection is reset. In addition, V_{CC} is discharged by I_{DD-OP4} in this V_{CC} range. In the end, this latch−protection reset can happen only when an input voltage is disconnected and the HV startup circuit cannot supply an operating current any longer. Next reconnection of an input voltage can make IC restart.

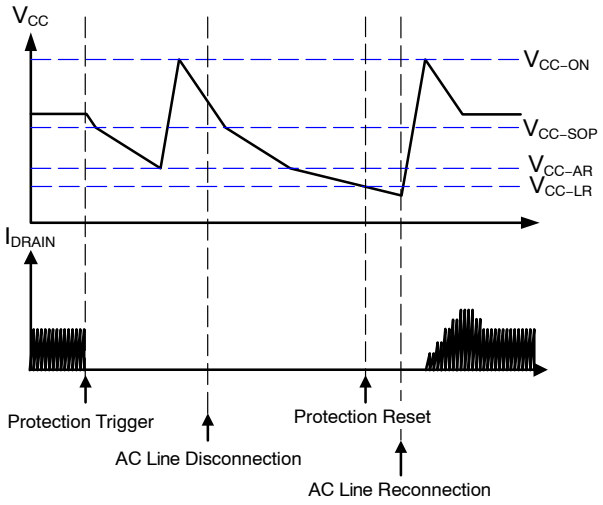


Figure 33. VCC Behavior in Latch Mode

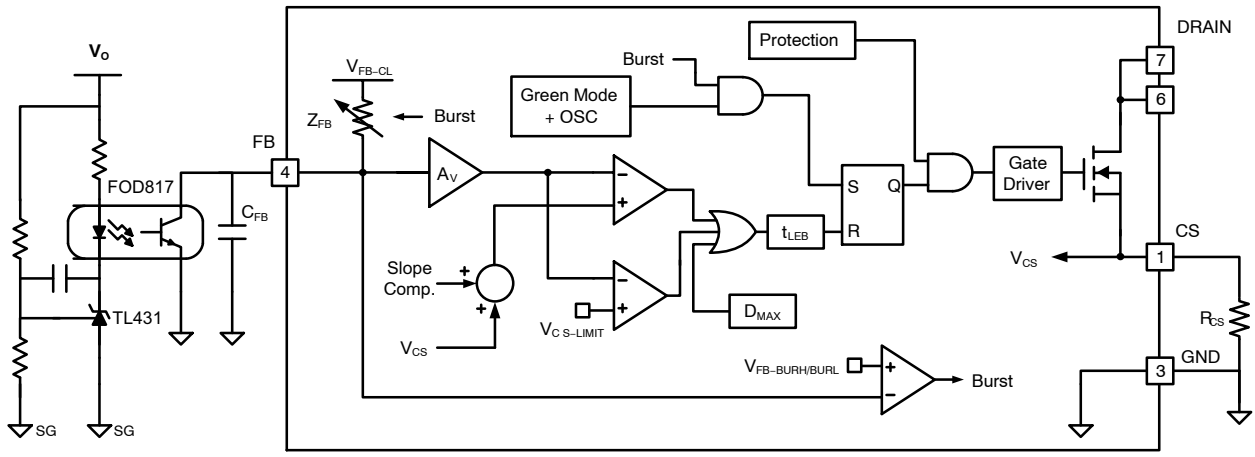


Figure 34. PWM Control Block

PWM Control Operation

NPC1118x employs peak−current mode pulse width modulation (PWM) control method to regulate output voltage. As shown in Figure 34, an opto−coupler and shunt regulator are typically used for the feedback network, which controls a feedback voltage V_{FB}. A sensing resistor is connected to CS pin and used to detect a drain current when the integrated MOSFET turns on.

Meanwhile, V_{FB} is attenuated by the internal amplifier with a gain of A_V, that becomes $(A_V \times (V_{FB} - V_F))$ where V_F is forward voltage drop of an series−connected diode at FB pin inside node. Simply comparing the attenuated voltage from the feedback voltage V_{FB} with a sensed drain current V_{CS} makes it possible to control the switching duty cycle. When V_{CS} reaches the attenuated voltage, the PWM comparator generates turn−off signal to the MOSFET immediately. In case, an output voltage V_O increase makes a current of the photo−diode increase, which leads V_{FB} to decrease and duty cycle is reduced as well. Accordingly, an output power transferred to the secondary side is limited.

In addition, whenever the integrated MOSFET turns on, a leading edge current occurs on the sense resistor R_{CS}, which could lead premature termination of the gate turn−on signal. To avoid it, a leading−edge blanking time t_{LEB} is employed. During the t_{LEB}, PWM comparator output is blocked so that turn−on signal to the gate can be maintained.

Frequency Hopping

Asynchronous frequency−hopping function built−in the oscillator generates consistent jittering in switching frequency. This frequency jittering prevents switching noises from being concentrated in its switching frequency band and distributes them to alleviate quasi−peak noises. The frequency is varied with period of t_{HOP} and amplitude of double of f_M as can be seen in Figure 35.

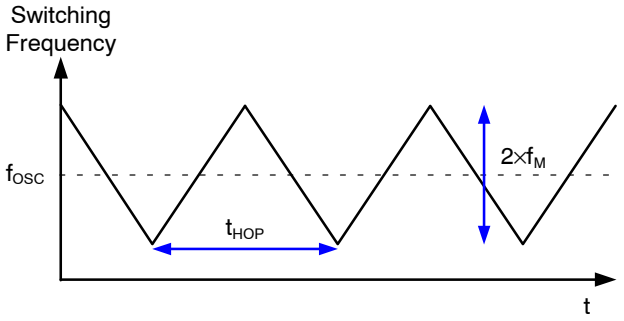


Figure 35. Frequency Hoping

Slope Compensation

A slope compensation is employed to prevent sub−harmonic oscillator and improve stability. A sawtooth signal is generated and added V_{CS} after pulse width of PWM signal exceeds t_{D-SE} which is around 40% of duty cycle to an switching frequency f_{OSC}. The amount of signals is compared with the internal feedback signal, which determines PWM on time.

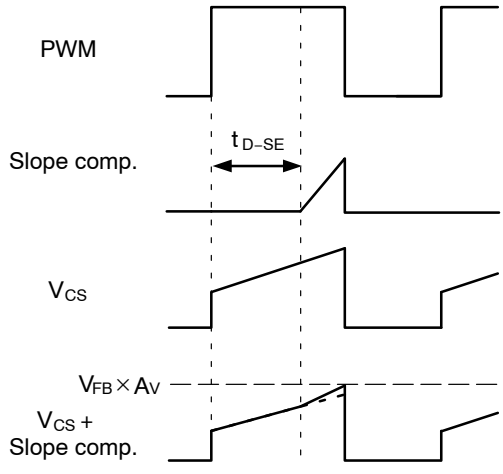


Figure 36. Slope Compensation

Slope of the sawtooth signal and t_{D-SE} are 30 mV/μs & 6 μs for 65 kHz of f_{OSC}, 46 mV/μs & 3.9 μs for 100 kHz of f_{OSC} and 60 mV/μs & 3 μs for 130 kHz of f_{OSC}. The delay time t_{D-SE} is 6 μs for 65−kHz version, 3.9 μs for 100−kHz version, and 3 μs for 130−kHz version, respectively.

Constant Over−power Limit

For constant output power limit at the entire input voltage range, a peak current limit threshold level V_{LIMIT} is controlled by the voltage of VIN pin V_{IN}. As can be seen in Figure 37, V_{LIMIT} is decreased as V_{IN} increases and maximum output power is limited automatically.

VIN pin is typically connected to the rectified AC line input voltage through the resistors divider.

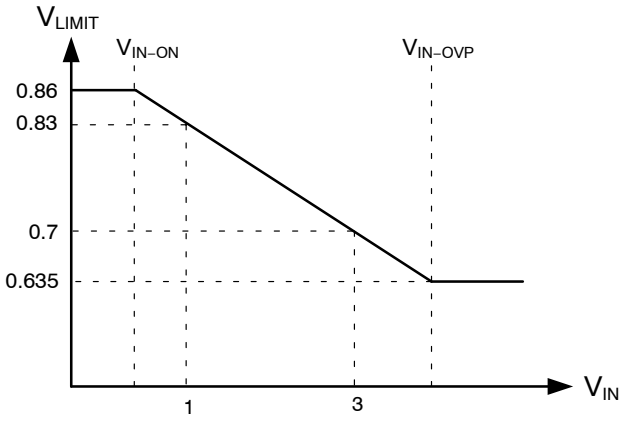


Figure 37. V_{IN} vs. V_{LIMIT}

Green−mode & Burst−mode Operation

To improve efficiency while reducing power dissipation, the proprietary green−mode function reduces switching frequency as load is decreased and forces PWM operation to stop at light load condition. The switching frequency depends on V_{FB} as illustrated in Figure 38.

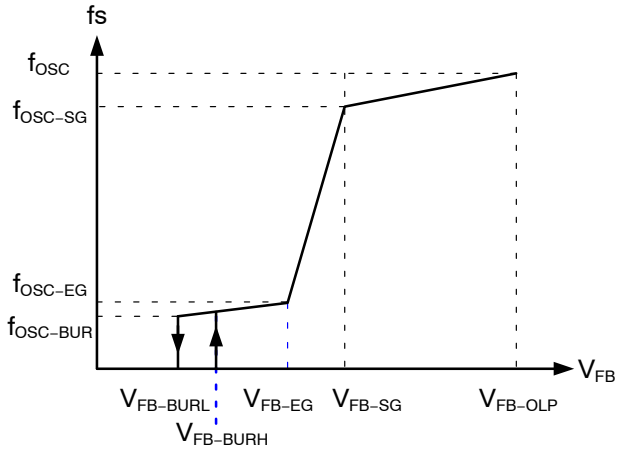


Figure 38. PWM Frequency vs. V_{FB}

After V_{FB} is lower than V_{FB-SG}, the switching frequency is steeply decreased from the green−mode start frequency f_{OSC-SG} to the green−mode end frequency f_{OSC-EG} until V_{FB} touches the green−mode end level V_{FB-EG}. When V_{FB} is lower than the burst−mode start level $V_{FB-BURL}$, the PWM controller is halted and starts entering the burst−mode operation. In this mode, the most of internal circuits are disabled so that internal operating current consumption is drastically decreased, thereby standby power figure can be improved as well. Meanwhile, all of internal circuits is enabled and the PWM switching is resumed as soon as V_{FB} is higher than the burst−mode end level $V_{FB-BURH}$.

Feedback Impedance Switching in Burst−mode

To minimize power consumption in no−load condition especially, a method to switch FB−pin impedance Z_{FB} in burst−mode is implemented. Figure 39 illustrates Z_{FB} variation depending on V_{FB}. By increasing Z_{FB}, amount of current consumed by the feedback network including the opto−coupler can be reduced. When V_{FB} touches $V_{FB-BURL}$, Z_{FB} is switched from 15 kΩ to Z_{FB-BUR} of typical 70 kΩ immediately. Whereas, when V_{FB} increases and gets higher than $V_{FB-BURH}$, Z_{FB} decreases stepwise and is back to normal Z_{FB} of 15 kΩ.

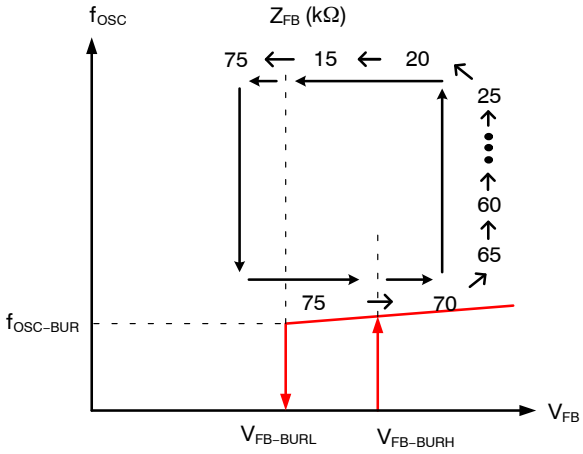


Figure 39. Z_{FB} Switching

Meanwhile, when V_{CC} decreases to V_{CC-ZFB} while Z_{FB} switches to Z_{FB-BUR}, the Z_{FB} of 70 kΩ is forced to back to normal Z_{FB} to prevent $V_{CC-UVLO}$ by touching V_{CC-OFF}.

VCC Over−Voltage Protection (V_{CC-OVP})

To prevent damage from over−voltage to V_{CC} pin, VCC over−voltage protection (OVP) is included. Once V_{CC} is over the over−voltage protection voltage V_{CC-OVP}, which lasts for fixed time duration corresponding to the V_{CC} OVP debounce counting number N_{VCCOVP}, the PWM will be disabled immediately. This protection can be reset only when V_{CC} is lower than V_{CC-AR} in the auto−restart mode.

FB Open Loop Protection (OLP)

When the output voltage drops below a regulation voltage or FB pin is open circuit, FB Voltage V_{FB} will settle V_{FB-OLP}, because a shunt regulator such as NCP431 no longer draws the opto−coupler current down. This is regarded as FB OL situation. If it lasts longer than t_{D-OLP}, FB OLP is triggered and PWM operation is stopped immediately. This protection can be reset when V_{CC} is below than V_{CC-OFF}.

Abnormal Over−current Protection (AOCP)

The AOCP stops PWM switching to prevent any damage of NCP1118x from excessive drain current caused by either of the secondary−side rectifier diode or the transformer is shorted. It has blanking time $t_{ON-AOCP}$ and doubouncing counting number N_{AOCP} to prevent AOCP activation prematurely from a leading edge current at an instance of turn−on of the main MOSFET in normal operation. When extreme current flows above the abnormal over−current threshold level $V_{CS-AOCP}$, which lasts over $t_{ON-AOCP}$ in abnormal conditions, the main MOSFET turns off immediately and the internal counter counts up the number of occurrence. Once this situation occurs the number of N_{AOCP} consecutively, then AOCP is triggered and PWM switching stops immediately until V_{CC} decreases to V_{CC-LR}.

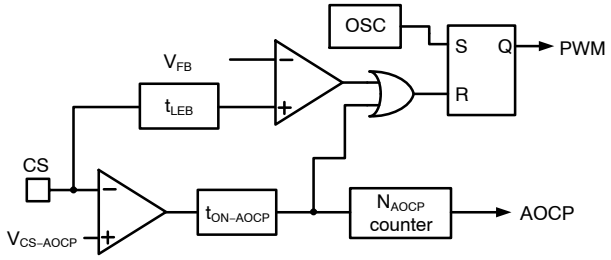


Figure 40. AOCP Logic

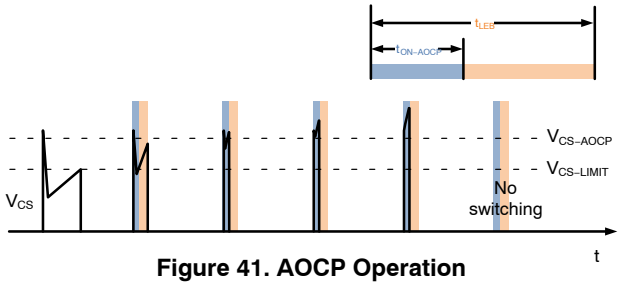


Figure 41. AOCP Operation

Current−Sense Short Protection

When CS pin is shorted to GND pin due to soldering defect or some dust, a drain current− cannot be sensed properly. It causes excessive drain current and ends up the switcher damage. If PWM on−time is longer than $t_{ON-CSSP}$ while V_{CS} is less than $V_{CS-CSSP}$, the CSSP circuit regards as a situation of CS pin short and turns off PWM switching immediately. If this state persists consecutively NCSSP times, then PWM switching operation stops permanently. This protection cannot be reset until unplugging the input voltage. Meanwhile, $V_{CS-CSSP}$ is varied depending on VIN level to avoid abnormal detection of CSSP at low input voltage. N_{CSSP} is different in either of startup or normal operation as well.

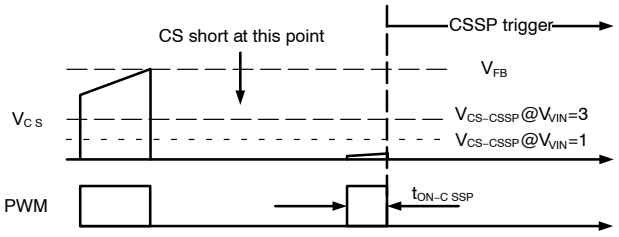


Figure 42. CSSP Waveform

Brown−out/Line Over−voltage Protection (Line OVP)

Brown−out and Line−OVP are performed by detecting line input voltage through VIN pin. VIN pin is typically connected to a resistive divider. They can connect to either of the ac rectifier or dc−link capacitor as can be seen in Figure 2 and Figure 3.

As for Brown−in operation, if a sensed V_{IN} is above V_{IN-ON} and V_{CC} is higher than V_{CC-ON}, then NCP1118x starts up and operates. Whereas, Brown−out is triggered when V_{IN} is kept less than V_{IN-OFF} for a debounce time $t_{D-VINOFF}$, the PWM switching stop. The protection is not released until V_{IN} is higher than V_{IN-ON}.

Meanwhile, when V_{IN} is higher than V_{IN-OVP} and the number of PWM switching last longer than Line−OVP debouncing counting number N_{VINOVP}, Line−OVP is triggered and PWM switching stops. Whereas, this protection can be released and allows NCP1118x to restart with soft−start when V_{IN} decreases by $V_{IN-OVPHYS}$ lower and V_{CC} is higher than V_{CC-ON}.

An ac input voltage for brown−out and Line−OVP can be simply set up by equations shown in Figure 43. Since it, a brown−in level is naturally determined by V_{IN-ON}. Additionally, it is recommended to add a capacitor of tens nano−farad to decouple switching noise and sense a voltage stably.

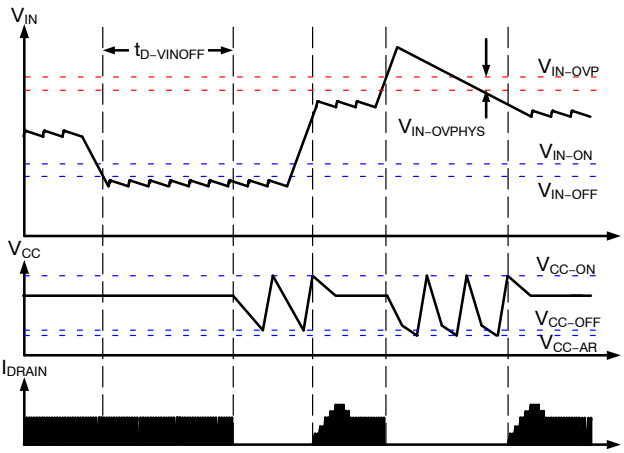


Figure 43. Brown−in/out & Line−OVP

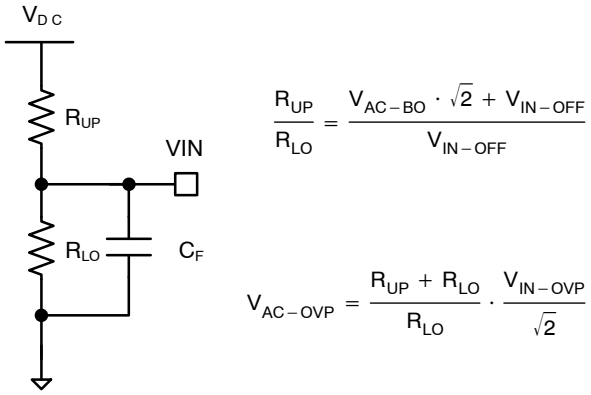


Figure 44. Line Voltage Detection

Thermal Shutdown (TSD)

TSD limits total power dissipation of NCP1118x by detecting temperature. When the junction temperature T_J exceeds T_{SD}, this switcher shuts down immediately. It can be recovery when T_J reduces by below $T_{TSD-HYS}$. During this TSD status, HV startup circuit performs on and off repeatedly.

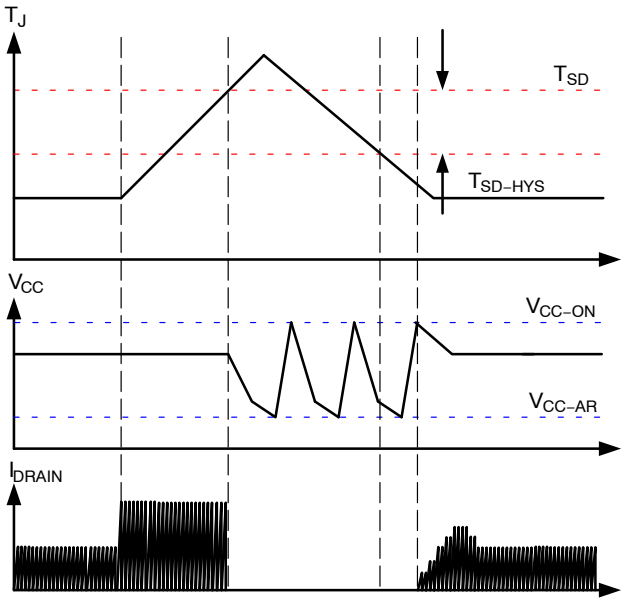


Figure 45. Thermal Shutdown

PCB LAYOUT RECOMMENDATIONS

This section introduces some PCB design tips for designers to minimize EMI (Electromagnetic Interference) and make robust switched mode power supplies using NCP1118x.

- High−frequency switching current/voltage makes PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD (Electro Static Discharge) tests.
- To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should connect to bulk capacitor as close as possible.
- As indicated by 1 in Figure 46, the high−frequency current loop is formed by beginning of the bridge rectifier, bulk capacitor, a power transformer to return to bulk capacitor. The area enclosed by this current loop should be designed as small as possible to reduce conduction and radiation noise. Keep the traces short, direct, and wide. High−voltage traces related the drain of MOSFET and RCD snubber should be kept far away from control circuits to prevent noise interference affecting low voltage signal paths at the control part.
- As indicated by 2, the ground of control circuits should be connected first, then to other circuitry.
- Place C_{VCC} as close to VCC pin of the NCP1118x as possible for good decoupling. It is recommended to use a few of micro−farad capacitor and 100 nF ceramic capacitor for high frequency noise decoupling as well. C_{VIN} pin and C_{FB} pin capacitor are also recommended to place as close as possible to VIN and FB pin.

There are some suggestions for grounding connection.

- GND: There are two kinds of GND in power conversion board and should be separated for avoiding interference and better performance.
- Generally, lightning surge could pass through stray capacitance of the transformer from the primary side to the secondary side or vice−versa. Regard with that, some points should be taken into account when designing PCB, such as placing control circuit parts, EMI filters and an Y−capacitor.
- 3 could be a point−discharger route to bypass the static electricity energy. It is suggested to map out this discharge route and not to place any low voltage components on the route.
- Should a Y−cap be required between primary and secondary, connect this Y−cap to the positive terminal of bulk capacitor. If this Y−cap is connected to primary GND, it should be connected to the negative terminal of bulk capacitor (GND) directly. Point discharge of this Y−cap helps for ESD; however, the creepage between these two pointed ends should be at least 5 mm according to safety requirements.
- Thermal Considerations:
  Power MOSFET dissipates heats during switching operation. If chip temperature exceeds TSD, thermal shutdown would be triggered and NCP1118x stops operating to protect itself from damage. The path of lowest thermal impedance from NCP1118x chip to externals is from DRAIN pin. It is recommended to increase area of connected copper to DRAIN pin as much as possible.

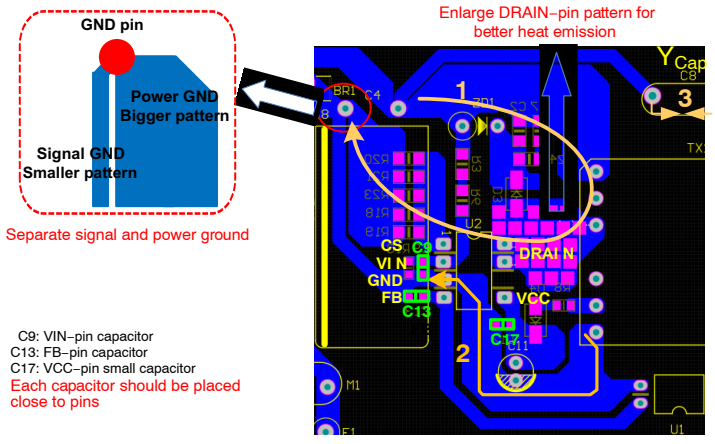


Figure 46. Layout Considerations

DESIGN EXAMPLE

This is a design example of 45 W isolated flyback converter using NCP1118765. For further detail information, go to the webpage of NCP1118x.

EVB No: NCP11187A65F45GEVB

Devices	Applications	Topology	Output Power
NCP11187A65	White Goods and Industrial Power Supplies	Isolated Flyback	45 W
Input Voltage	**Output Spec.**	**Efficiency**	**Standby Power**
85–265 Vac	12 V/3.5 A & 16 V/0.2 A	> 88% @ Full−load	< 50 mW @ 230 Vac
Package Temperature	**Operating Temperature**	**Cooling Method**	**Board Size**
90°C @ T_A = 50°C	0~50°C	Natural Convection In Open Frame	145 x 60 x 30 mm 2.83 W/inch^3

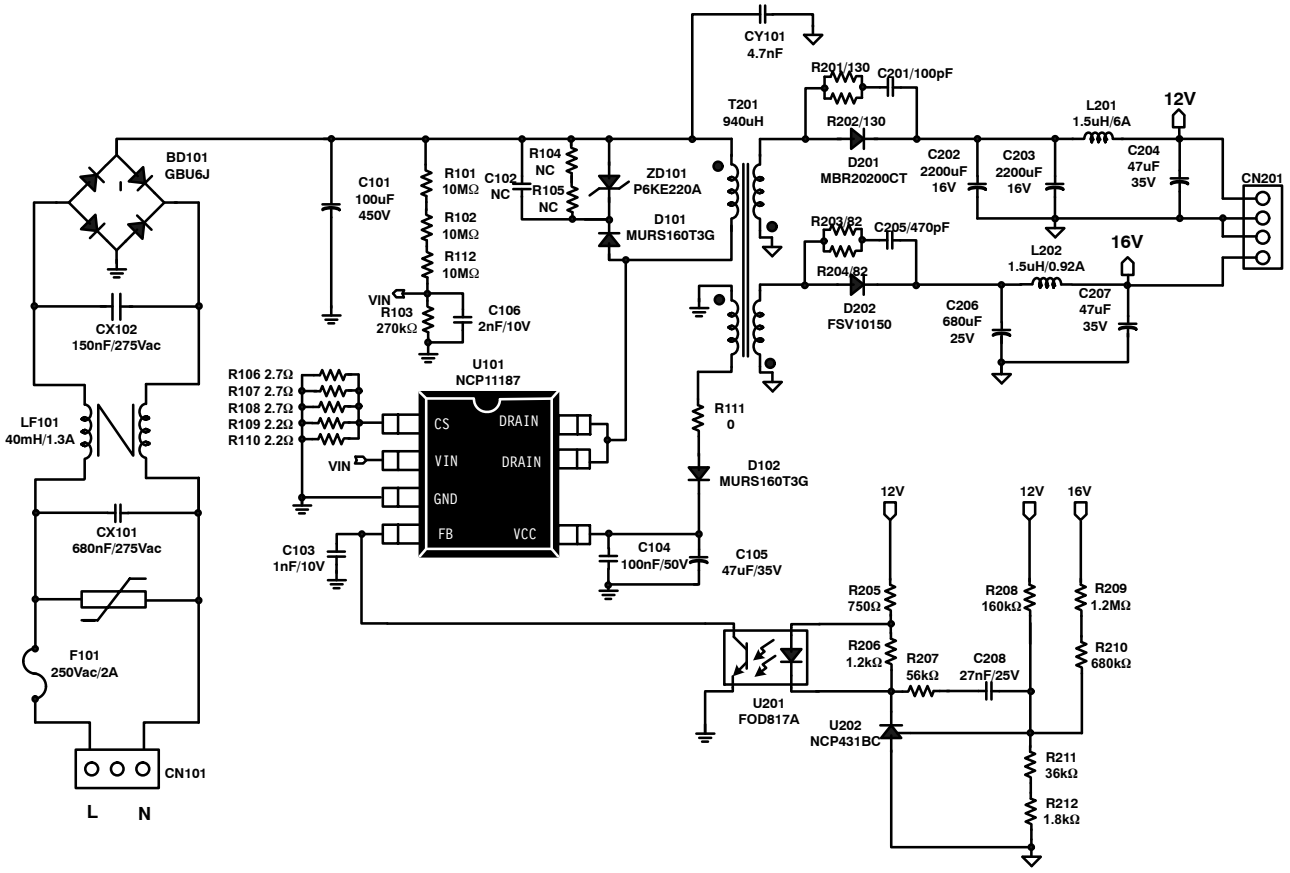


Figure 47. NCP11187 EVB Schematic

REFERENCES

For more specific designs, refer to the links below:

- AN−4148 Audible Noise Reduction Technique for FPS Applications
  https://www.onsemi.com/pub/Collateral/AN−4148.pdf
- AN−4137 Design Guidelines for Off−line Flyback Converters Using Power Switch
  https://www.onsemi.com/pub/Collateral/AN−4137.pdf
- AN−4140 Transformer Design Consideration for Offline Flyback Converters Using Power Switch
  https://www.onsemi.com/pub/Collateral/AN−4140.pdf
- NCP1118x Family Simplis Behavior Model
- NCP1118x Family Excel−based Design Tool

ORDERING INFORMATION

ORDERING INFORMATION

Device	$R_{DS(ON)}$ (Ω)	f_{OSC} (kHz)	Package	Shipping
NCP11184A065PG	2.25	65	PDIP−7 (Pb−Free)	50 Units / Rail
NCP11185A065PG	1.3	65		
NCP11187A065PG	0.87	65		
NCP11184A100PG	2.25	100		
NCP11187A100PG	0.87	100		
NCP11184A130PG	2.25	130		
NCP11185A130PG	1.3	130		

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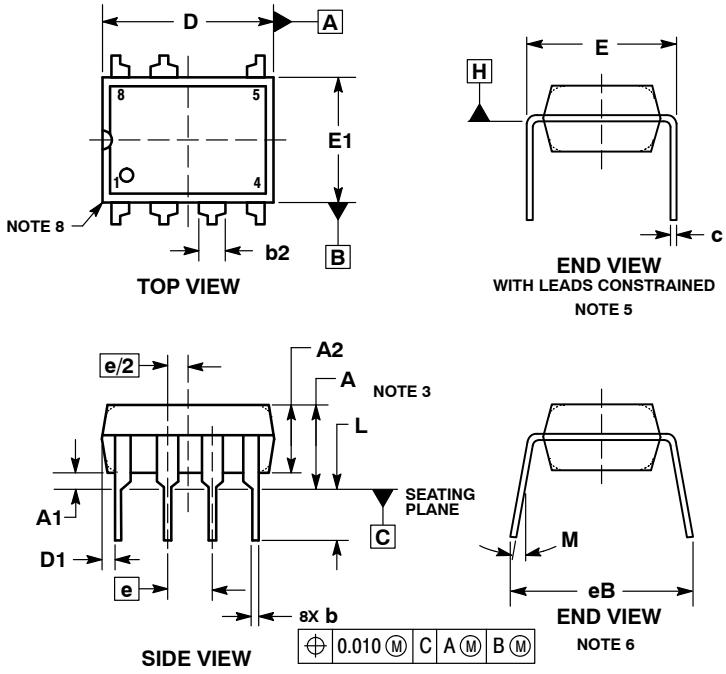
PACKAGE DIMENSIONS

PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

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