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NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055

Monolithic High Voltage Gated Oscillator Power Switching Regulator

The NCP1050 through NCP1055 are monolithic high voltage regulators that enable end product equipment to be compliant with low standby power requirements. This device series combines the required converter functions allowing a simple and economical power system solution for office automation, consumer, and industrial products. These devices are designed to operate directly from a rectified AC line source. In flyback converter applications they are capable of providing an output power that ranges from 6.0 W to 40 W with a fixed AC input of 100 V, 115 V, or 230 V, and 3.0 W to 20 W with a variable AC input that ranges from 85 V to 265 V.

This device series features an active startup regulator circuit that eliminates the need for an auxiliary bias winding on the converter transformer, fault detector and a programmable timer for converter overload protection, unique gated oscillator configuration for extremely fast loop response with double pulse suppression, power switch current limiting, input undervoltage lockout with hysteresis, thermal shutdown, and auto restart fault detection. These devices are available in economical 8–pin dual–in–line and 4–pin SOT–223 packages.

Features

- Startup Circuit Eliminates the Need for Transformer Auxiliary Bias Winding
- Optional Auxiliary Bias Winding Override for Lowest Standby Power Applications
- Converter Output Overload and Open Loop Protection
- Auto Restart Fault Protection
- IC Thermal Fault Protection
- Unique, Dual Edge, Gated Oscillator Configuration for Extremely Fast Loop Response
- Oscillator Frequency Dithering with Controlled Slew Rate Driver for Reduced EMI
- Low Power Consumption Allowing European Blue Angel Compliance
- On–Chip 700 V Power Switch Circuit and Active Startup Circuit
- Rectified AC Line Source Operation from 85 V to 265 V
- Input Undervoltage Lockout with Hysteresis
- Oscillator Frequency Options of 44 kHz, 100 kHz, 136 kHz
- These are Pb–Free and Halide–Free Devices

Typical Applications

- AC–DC Converters
- Wall Adapters
- Portable Electronic Chargers
- Low Power Standby and Keep–Alive Supplies

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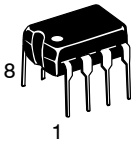
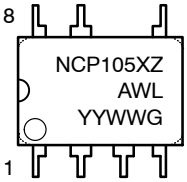
MARKING DIAGRAMS



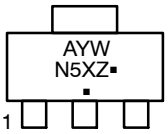
PDIP–8
P SUFFIX
CASE 626A



Pin: 1. V_{CC}
2. Control Input
3, 7–8. Ground
4. No Connection
5. Power Switch Drain



SOT–223
ST SUFFIX
CASE 318E



Pin: 1. V_{CC}
2. Control Input
3. Power Switch Drain
4. Ground

X = Current Limit (0, 1, 2, 3, 4, 5)
Z = Oscillator Frequency
A = 44 kHz, B = 100 kHz, C = 136 kHz
A = Assembly Location
WL, = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 22 of this data sheet.

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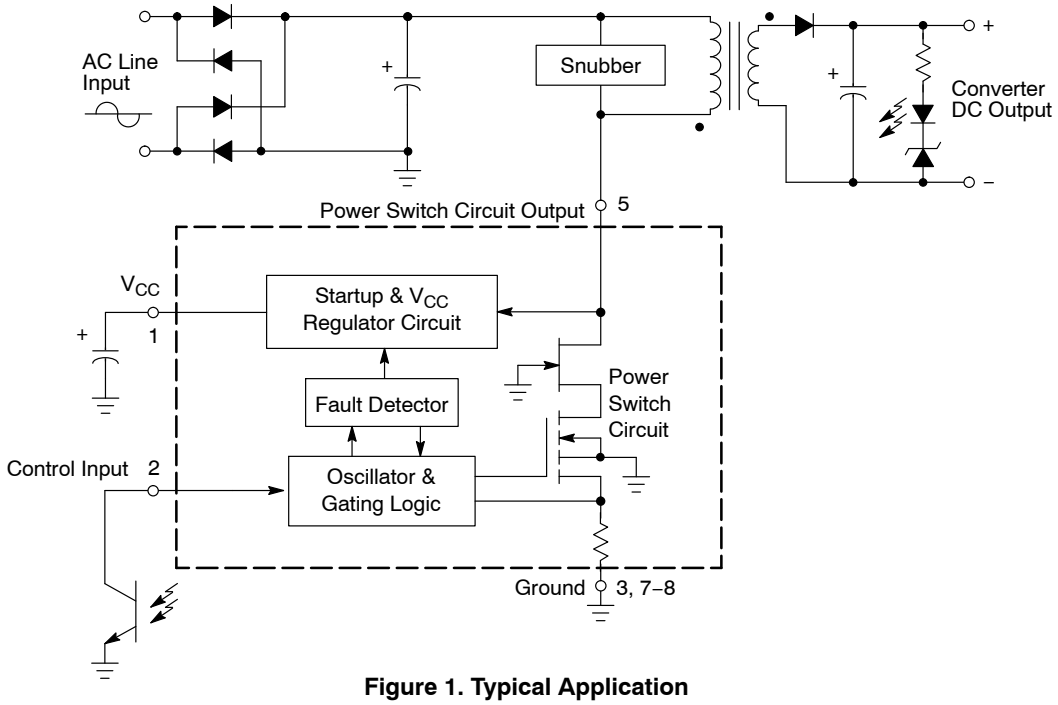


Figure 1. Typical Application

Pin Function Description

Pin (SOT−223)	Pin (PDIP−8)	Function	Description
1	1	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 5. When V_{CC} reaches V_{CC}(on), the Startup Circuit turns off and the output is allowed to begin switching with 1.0 V hysteresis on the V_{CC} pin. The capacitance connected to this pin programs fault timing and frequency modulation rate.
2	2	Control Input	The Power Switch Circuit is turned off when a current greater than approximately 50 μA is drawn out of or applied to this pin. A 10 V clamp is built onto the chip to protect the device from ESD damage or overvoltage conditions.
4	3, 7, 8	Ground	This pin is the control circuit and Power Switch Circuit ground. It is part of the integrated circuit lead frame.
–	4	No Connection	
3	5	Power Switch Drain	This pin is designed to directly drive the converter transformer primary, and internally connects to Power Switch and Startup Circuit.

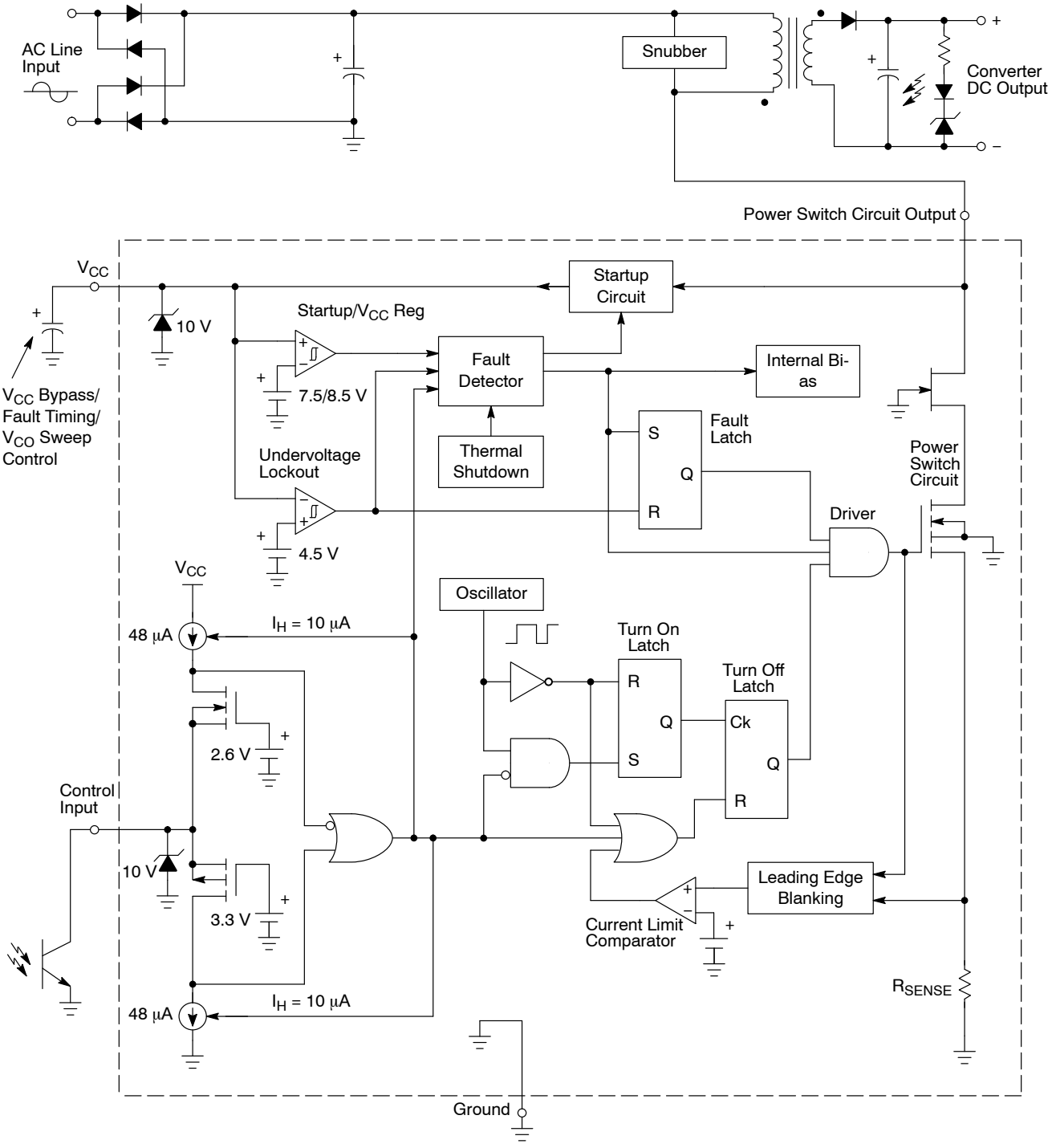


Figure 2. Representative Block Diagram

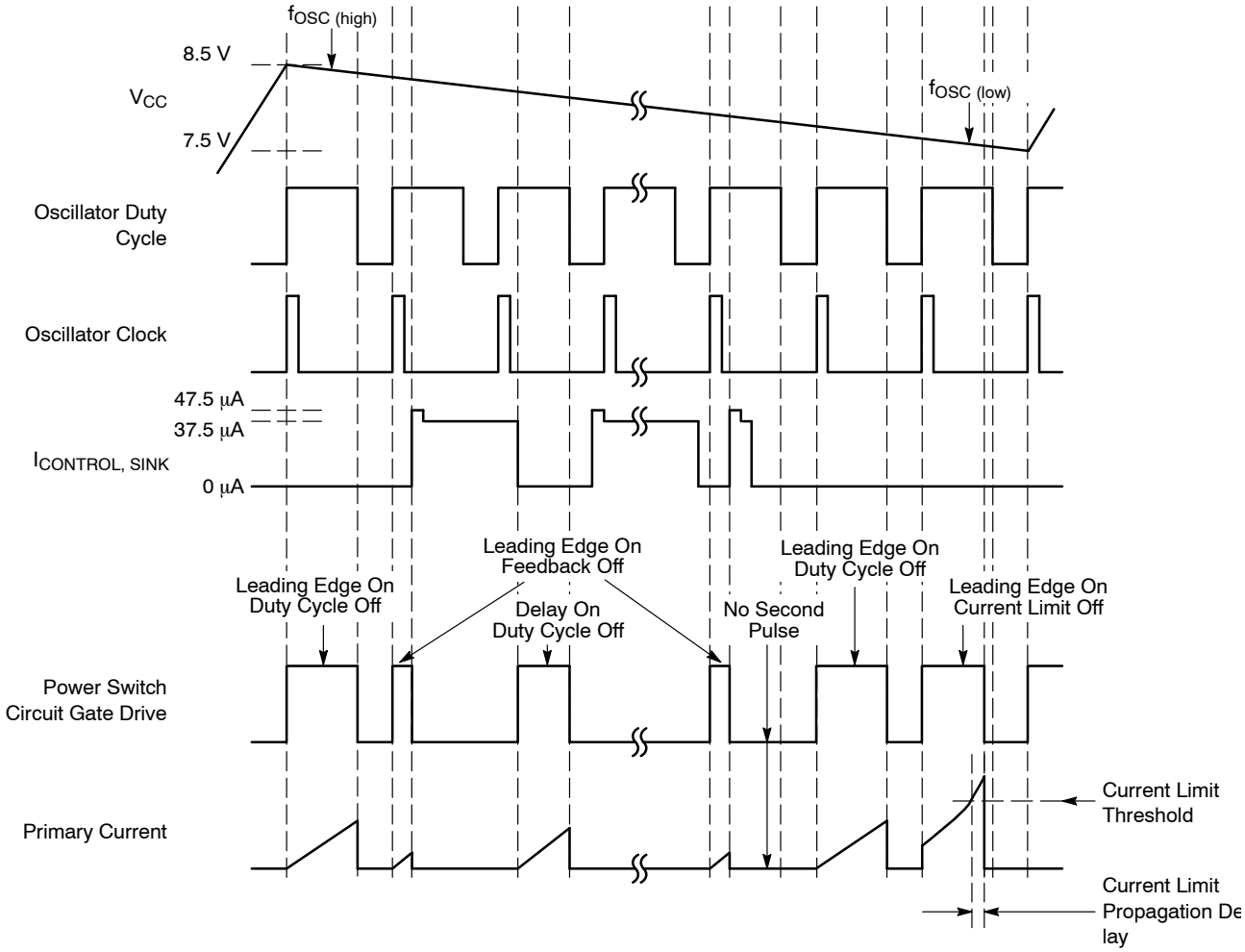


Figure 3. Timing Diagram for Gated Oscillator with Dual Edge PWM

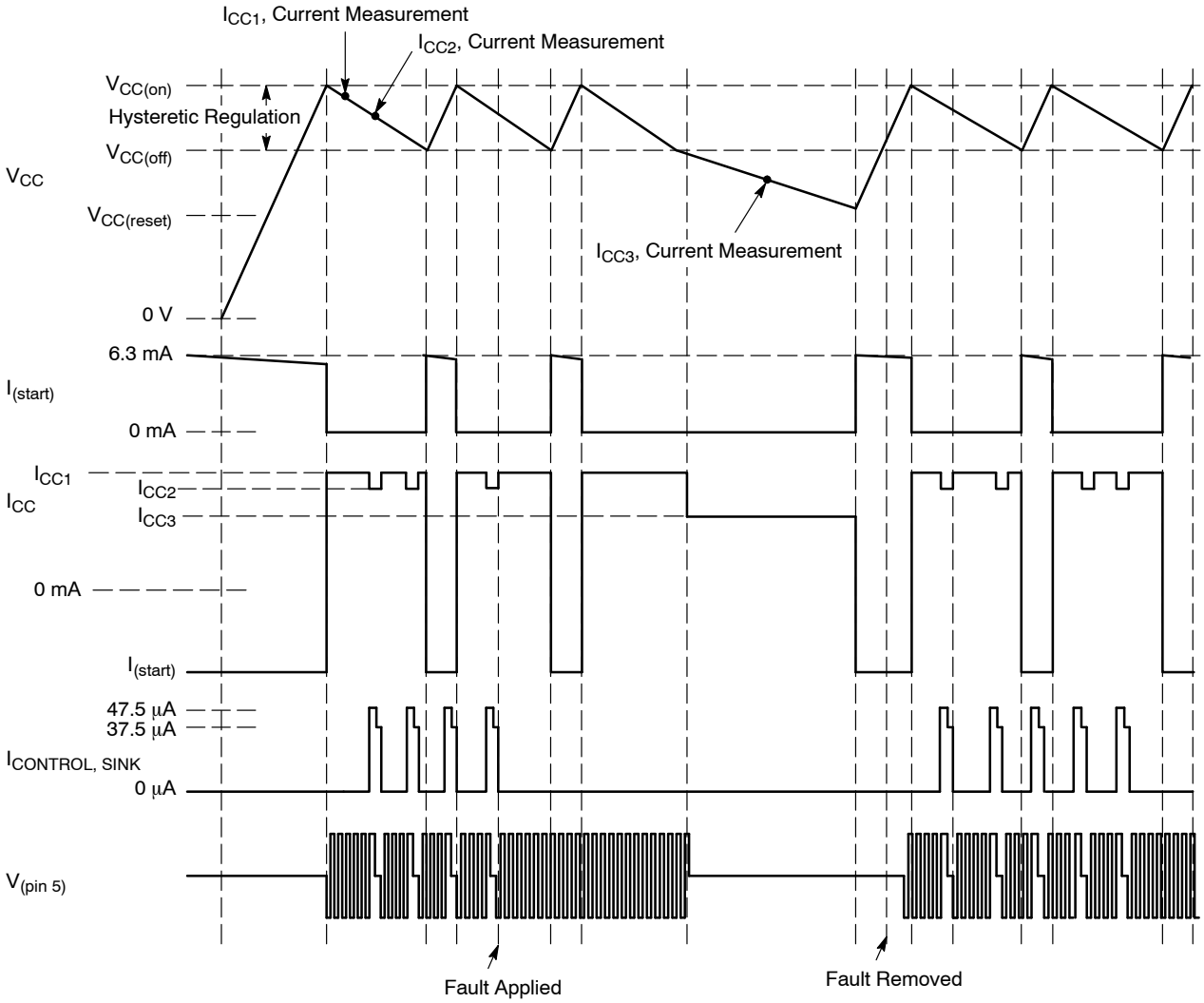


Figure 4. Non−Latching Fault Condition Timing Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch and Startup Circuit Drain Voltage Range Drain Current Peak During Transformer Saturation	 V_{DS} $I_{DS(pk)}$	 −0.3 to 700 2.0 x I_{lim} Max	 V A
Power Supply/V_{CC} Bypass and Control Input Voltage Range Current	 V_{IR} I_{max}	 −0.3 to 10 100	 V mA
Thermal Characteristics P Suffix, Plastic Package Case 626A−01 Junction−to−Lead Junction−to−Air, 2.0 Oz. Printed Circuit Copper Clad 0.36 Sq. Inch 1.0 Sq. Inch ST Suffix, Plastic Package Case 318E−04 Junction−to−Lead Junction−to−Air, 2.0 Oz. Printed Circuit Copper Clad 0.36 Sq. Inch 1.0 Sq. Inch	 $R_{\theta JL}$ $R_{\theta JA}$ $R_{\theta JL}$ $R_{\theta JA}$ 	 9.0 77 60 14 74 55	°C/W
Operating Junction Temperature	T_J	−40 to +150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1−3: Human Body Model 2000 V per JEDEC JESD22−A114−F.
   Machine Model Method 400 V per JEDEC JESD22−A115−A.
   Pin 5: Human Body Model 1000 V per JEDEC JESD22−A114−F.
   Machine Model Method 400 V per JEDEC JESD22−A115−A.
   Pin 5 is connected to the power switch and start−up circuits, and is rated only to the max voltage of the part, or 700 V.
   Charged Device Model (CDM) 1000 V per JEDEC Standard JESD22−C101E.
2. This device contains Latch−up protection and exceeds ±100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, for typical values T_J = 25°C, for min/max values, T_J is the operating junction temperature range that applies (Note 3), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{CC} = 7.5 V) T_J = 25°C: 44 kHz Version 100 kHz Version 136 kHz Version T_J = T_{low} to T_{high} 44 kHz Version 100 kHz Version 136 kHz Version	$f_{OSC(low)}$	 38 87 119 37 84 113	 42.5 97 132 – – –	 47 107 145 47 107 145	kHz
Frequency (V_{CC} = 8.5 V) T_J = 25°C: 44 kHz Version 100 kHz Version 136 kHz Version T_J = T_{low} to T_{high} 44 kHz Version 100 kHz Version 136 kHz Version	$f_{OSC(high)}$	 41 93 126 39 90 120	 45.5 103 140 – – –	 50 113 154 50 113 154	kHz
Frequency Sweep (V_{CC} = 7.5 V to 8.5 V, T_J = 25°C)	$\%f_{OSC}$	–	5.0	–	%
Maximum Duty Cycle	$D_{(max)}$	74	77	80	%
CONTROL INPUT					
Lower Window Input Current Threshold Switching Enabled, Sink Current Increasing Switching Disabled, Sink Current Decreasing Upper Window Input Current Threshold Switching Enabled, Source Current Increasing Switching Disabled, Source Current Decreasing	 $I_{off(low)}$ $I_{on(low)}$ $I_{off(high)}$ $I_{on(high)}$	 –58 –50 37 25	 –47.5 –37.5 47.5 37.5	 –37 –25 58 50	μA
Control Window Input Voltage Lower (I_{sink} = 25 μA) Upper (I_{source} = 25 μA)	 V_{low} V_{high}	 1.1 4.2	 1.35 4.6	 1.6 5.0	V

3. Tested junction temperature range for the NCP105X series:
   T_{low} = –40°C T_{high} = +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, for typical values T_J = 25°C, for min/max values, T_J is the operating junction temperature range that applies (Note 4), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER SWITCH CIRCUIT					
Power Switch Circuit On−State Resistance NCP1050, NCP1051, NCP1052 (I_D = 50 mA) T_J = 25°C T_J = 125°C NCP1053, NCP1054, NCP1055 (I_D = 100 mA) T_J = 25°C T_J = 125°C	$R_{DS(on)}$	 – – – –	 22 42 10 23	 30 55 15 28	Ω
Power Switch Circuit & Startup Breakdown Voltage ($I_{D(off)}$ = 100 μA, T_A = 25°C)	$V_{(BR)DS}$	700	–	–	V
Power Switch Circuit & Startup Circuit Off−State Leakage Current (V_{DS} = 650 V) T_J = 25°C T_J = 125°C	$I_{DS(off)}$	 – –	 25 15	 40 80	μA
Switching Characteristics (R_L = 50 Ω, V_{DS} set for I_D = 0.7 I_{lim}) Turn−on Time (90% to 10%) Turn−off Time (10% to 90%)	 t_{on} t_{off}	 – –	 20 10	 – –	ns
CURRENT LIMIT AND THERMAL PROTECTION					
Current Limit Threshold (T_J = 25°C) (Note 7) NCP1050 NCP1051 NCP1052 NCP1053 NCP1054 NCP1055	I_{lim}	 93 186 279 372 493 632	 100 200 300 400 530 680	 107 214 321 428 567 728	mA
Conversion Power Deviation (T_J = 25°C) (Note 8)	I^2f_{OSC}	–	0	10	$\%A^2Hz$
Propagation Delay, Current Limit Threshold to Power Switch Circuit Output NCP1050, NCP1051, NCP1052 NCP1053, NCP1054, NCP1055	t_{PLH}	 – –	 135 160	 – –	ns
Thermal Protection (V_{CC} = 8.6 V) (Note 4, 5, 6) Shutdown (Junction Temperature Increasing) Hysteresis (Junction Temperature Decreasing)	 T_{sd} T_H	 140 –	 160 75	 – –	°C
STARTUP CONTROL					
Startup/V_{CC} Regulation Startup Threshold/V_{CC} Regulation Peak (V_{CC} Increasing) Minimum Operating/V_{CC} Valley Voltage After Turn−On Hysteresis	 $V_{CC(on)}$ $V_{CC(off)}$ V_H	 8.0 7.0 –	 8.5 7.5 1.0	 9.0 8.0 –	V
Undervoltage Lockout Threshold Voltage, V_{CC} Decreasing	$V_{CC(reset)}$	4.0	4.5	5.0	V
Startup Circuit Output Current (Power Switch Circuit Output = 40 V) V_{CC} = 0 V T_J = 25°C T_J = −40 to 125°C V_{CC} = $V_{CC(on)}$ − 0.2 V T_J = 25°C T_J = −40 to 125°C	I_{start}	 5.4 4.5 4.6 3.5	 6.3 – 5.6 –	 7.2 8.0 6.6 7.0	mA
Minimum Start−up Drain Voltage (I_{start} = 0.5 mA, V_{CC} = $V_{CC(on)}$ − 0.2 V)	$V_{start(min)}$	–	13.4	20	V
Output Fault Condition Auto Restart (V_{CC} Capacitor = 10 μF, Power Switch Circuit Output = 40 V) Average Switching Duty Cycle Frequency	 D_{rst} f_{rst}	 – –	 6.0 3.5	 – –	 % Hz

4. Tested junction temperature range for the NCP105X series:
   T_{low} = −40°C T_{high} = +125°C
5. Maximum package power dissipation limits must be observed.
6. Guaranteed by design only.
7. Adjust di/dt to reach I_{lim} in 4.0 μsec.
8. Consult factory for additional options including test and trim for output power accuracy.

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, for typical values T_J = 25°C, for min/max values, T_J is the operating junction temperature range that applies (Note 9), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE					
Power Supply Current After UVLO Turn−On (Note 10)					mA
Power Switch Circuit Enabled	I_{CC1}				
NCP1050, NCP1051, NCP1052					
44 kHz Version		0.35	0.45	0.55	
100 kHz Version		0.40	0.50	0.60	
136 kHz Version		0.40	0.525	0.65	
NCP1053, NCP1054, NCP1055					
44 kHz Version		0.40	0.50	0.60	
100 kHz Version		0.45	0.575	0.70	
136 kHz Version		0.50	0.65	0.80	
Power Switch Circuit Disabled					
Non−Fault Condition	I_{CC2}	0.35	0.45	0.55	
Fault Condition	I_{CC3}	0.10	0.175	0.25	

9. Tested junction temperature range for the NCP105X series:
   T_{low} = −40°C T_{high} = +125°C
10. See Non−Latching Fault Condition Timing Diagram in Figure 4.

TYPICAL CHARACTERISTICS

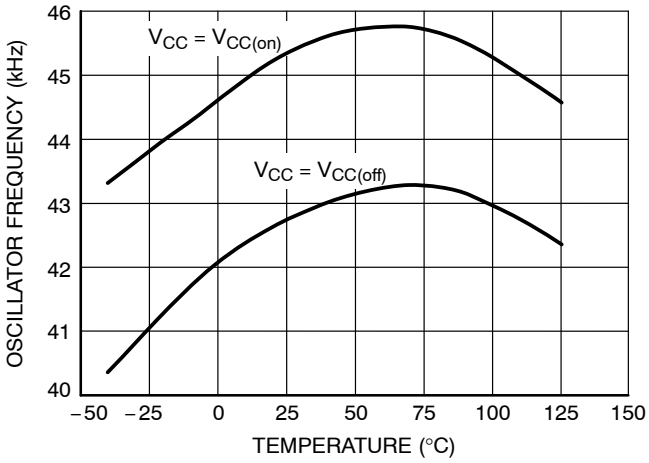


Figure 5. Oscillator Frequency (44 kHz Version) versus Temperature

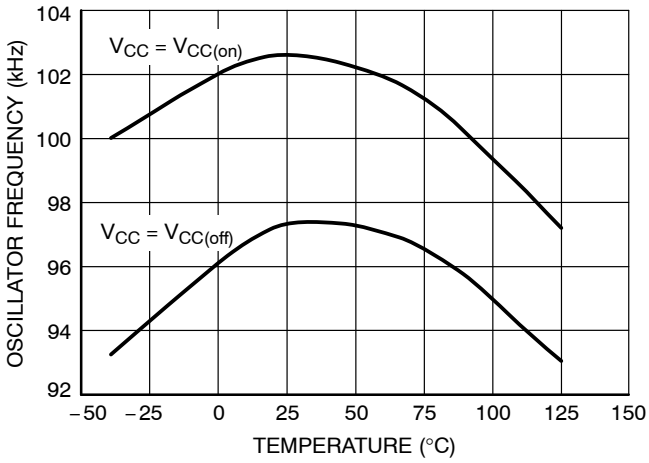


Figure 6. Oscillator Frequency (100 kHz Version) versus Temperature

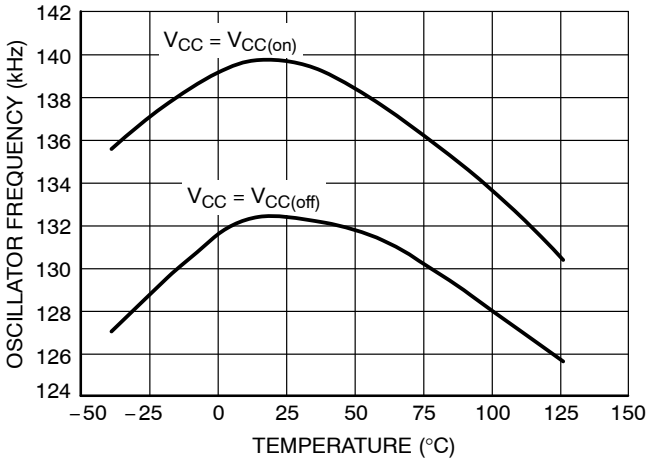


Figure 7. Oscillator Frequency (136 kHz Version) versus Temperature

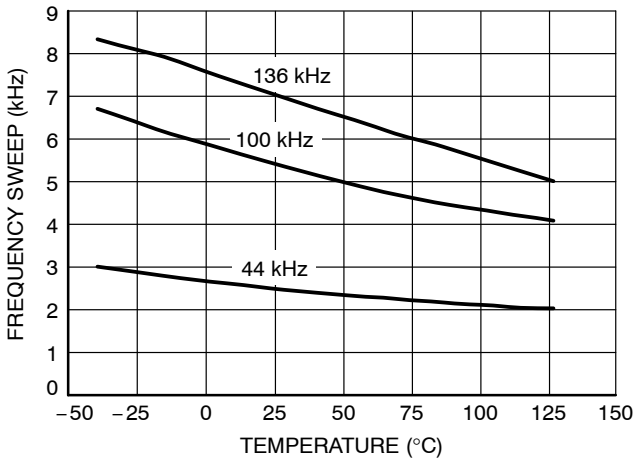


Figure 8. Frequency Sweep versus Temperature

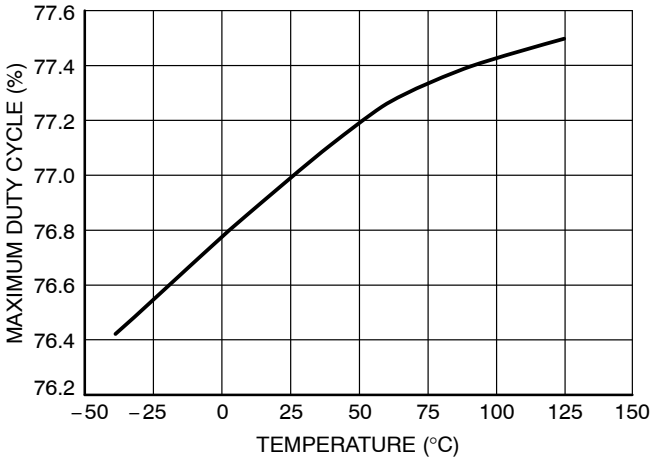


Figure 9. Maximum Duty Cycle versus Temperature

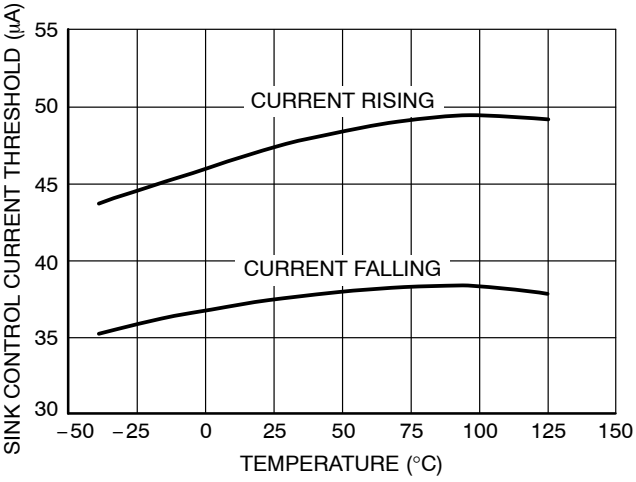


Figure 10. Lower Window Control Input Current Thresholds versus Temperature

TYPICAL CHARACTERISTICS

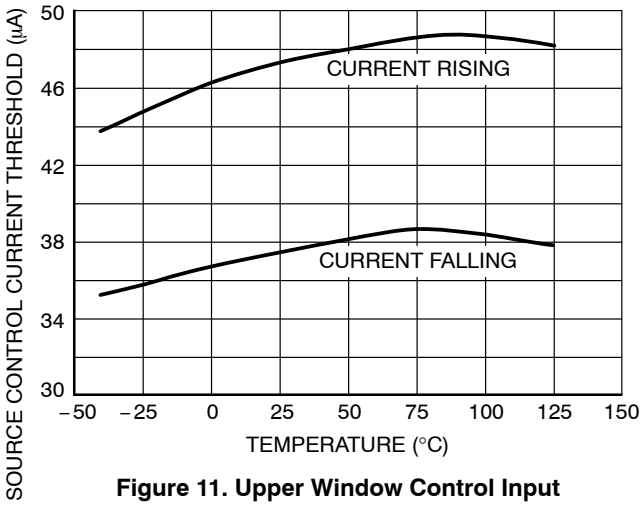


Figure 11. Upper Window Control Input Current Thresholds versus Temperature

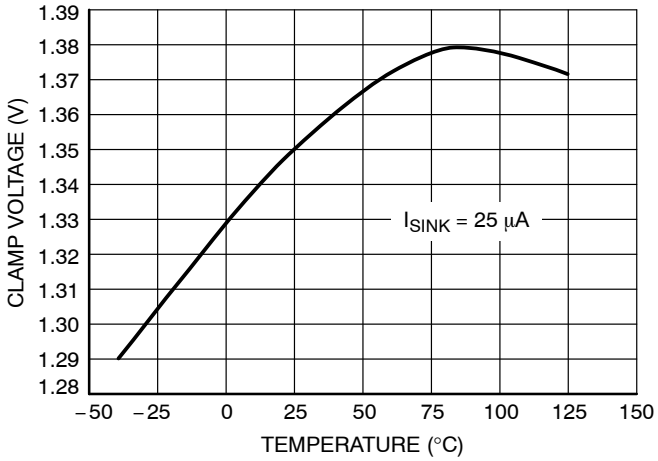


Figure 12. Control Input Lower Window Clamp Voltage versus Temperature

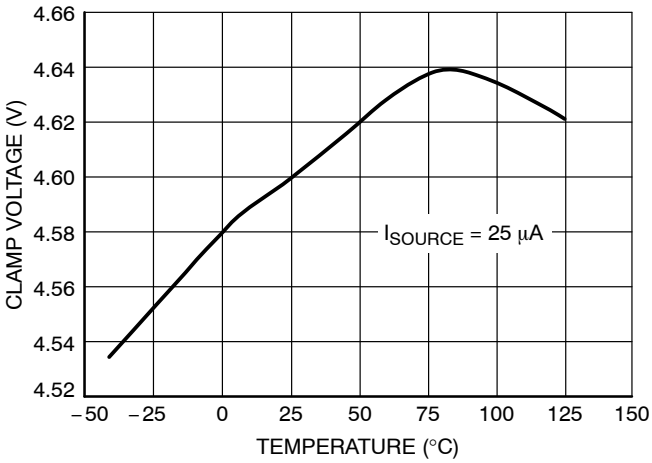


Figure 13. Control Input Upper Window Clamp Voltage versus Temperature

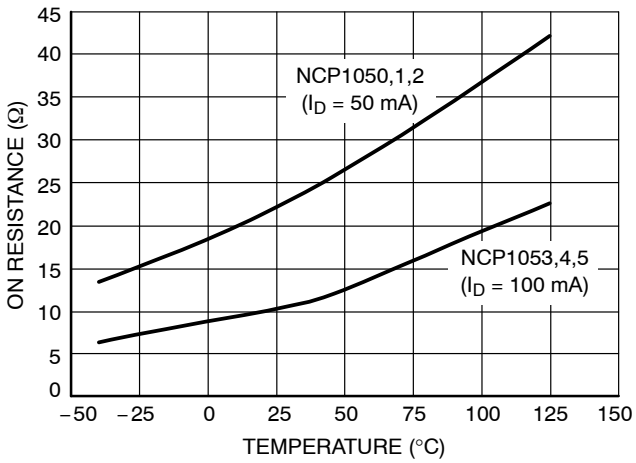


Figure 14. On Resistance versus Temperature

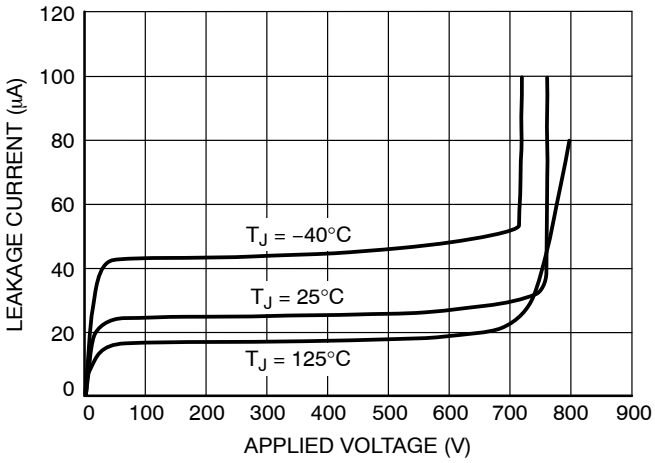


Figure 15. Power Switch and Startup Circuit Leakage Current versus Voltage

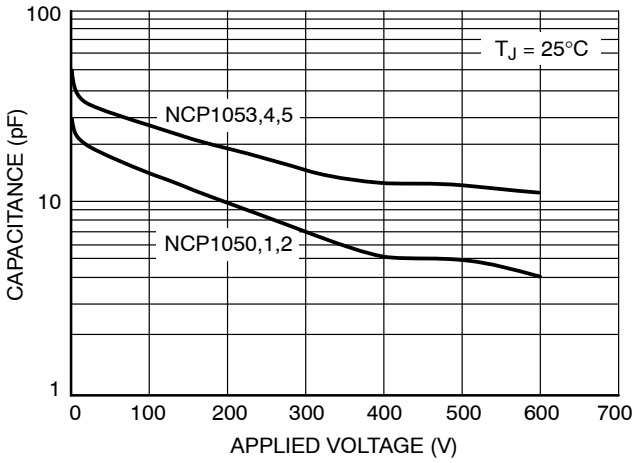


Figure 16. Power Switch and Startup Circuit Output Capacitance versus Applied Voltage

TYPICAL CHARACTERISTICS

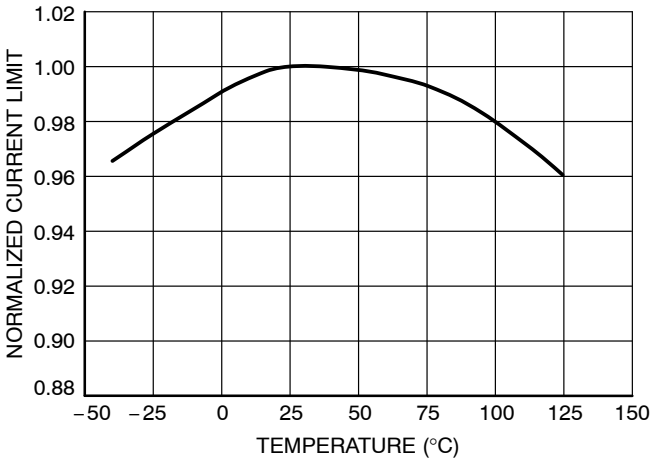


Figure 17. Normalized Peak Current Limit versus Temperature

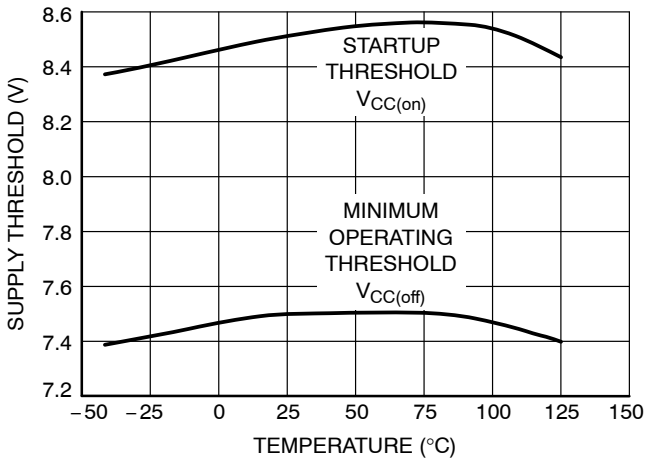


Figure 18. Supply Voltage Thresholds versus Temperature

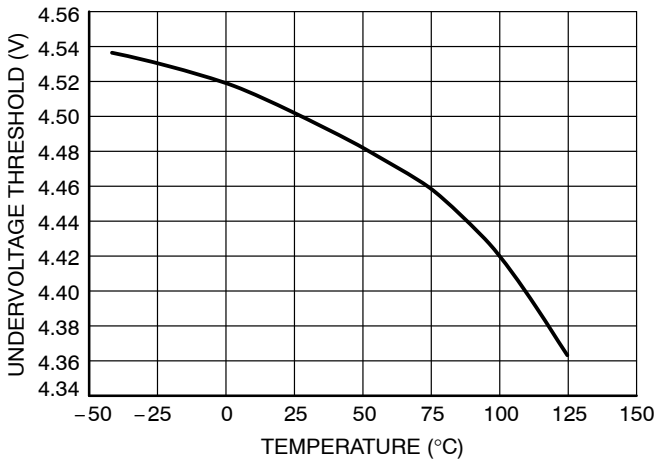


Figure 19. Undervoltage Lockout Threshold versus Temperature

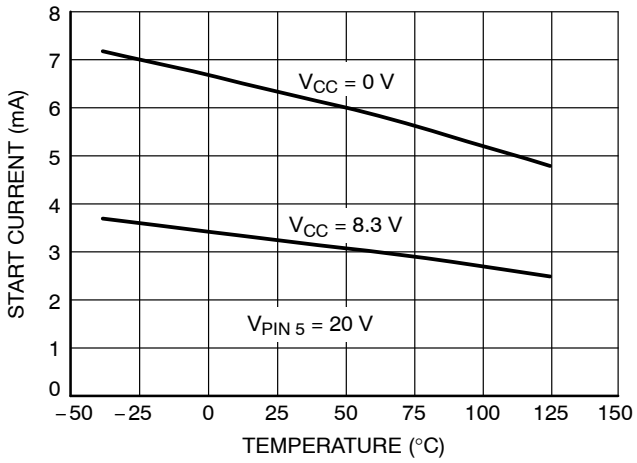


Figure 20. Start Current versus Temperature

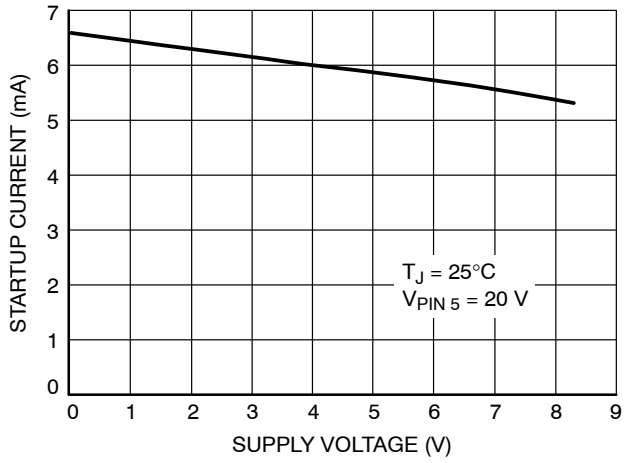


Figure 21. Startup Current versus Supply Voltage

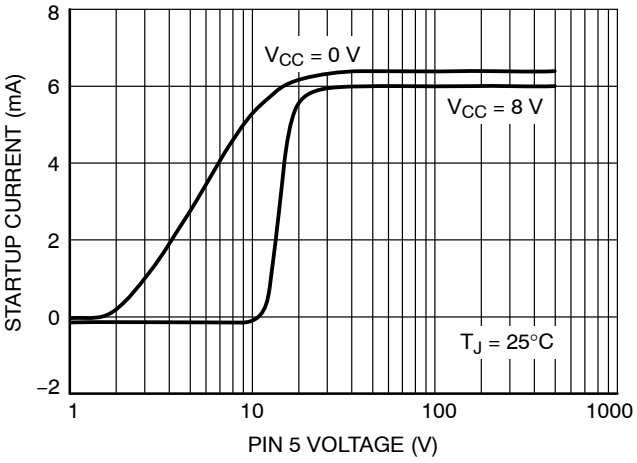


Figure 22. Startup Current versus Pin 5 Voltage

TYPICAL CHARACTERISTICS

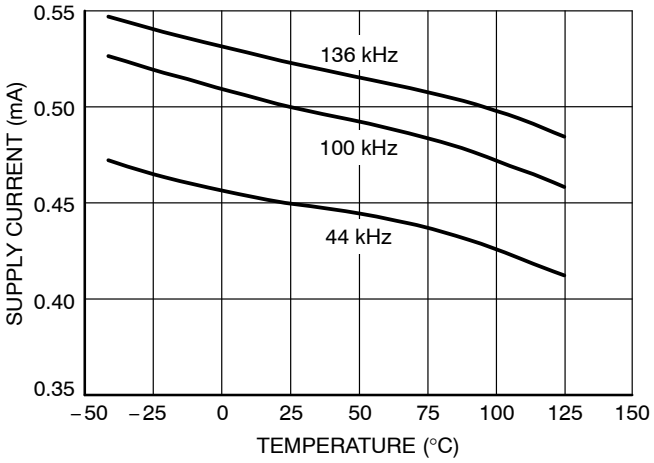


Figure 23. Supply Current versus Temperature (NCP1050/1/2)

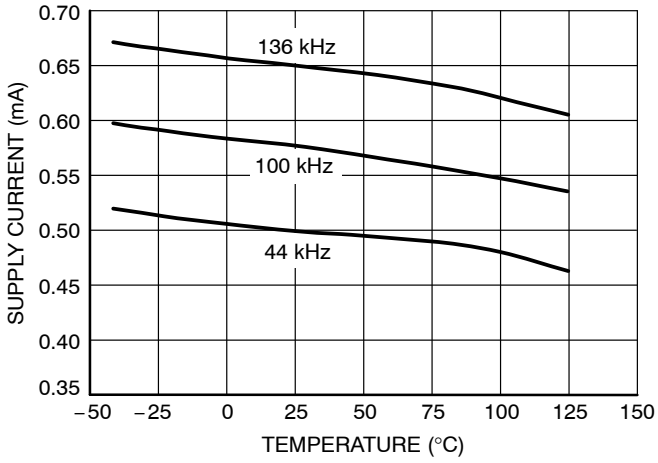


Figure 24. Supply Current versus Temperature (NCP1053/4/5)

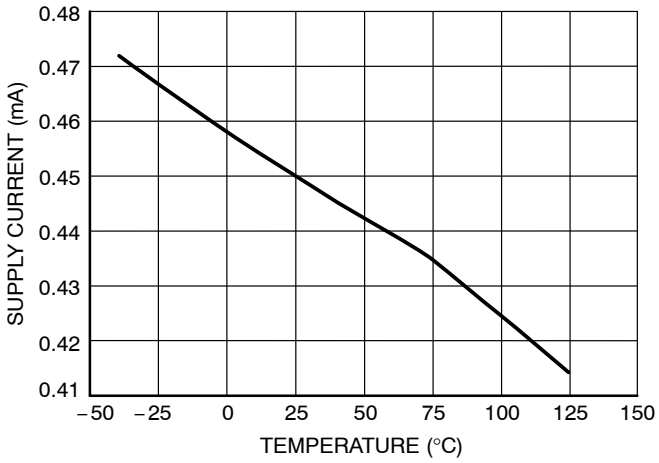


Figure 25. Supply Current When Switching Disable versus Temperature

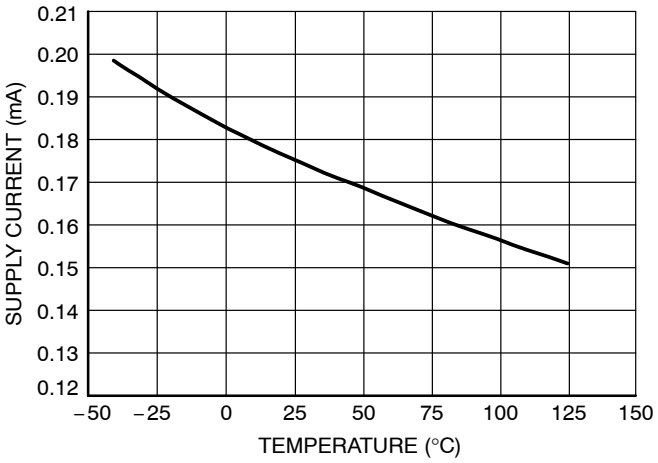


Figure 26. Supply Current in Fault Condition versus Temperature

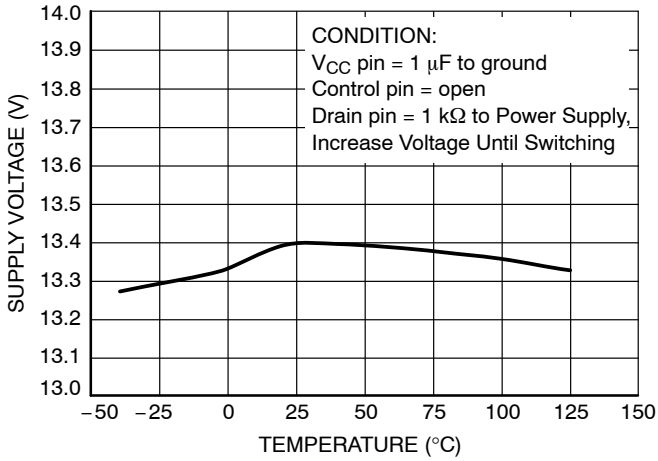


Figure 27. Supply Voltage versus Temperature

OPERATING DESCRIPTION

Introduction

The NCP105X series represents a new higher level of integration by providing on a single monolithic chip all of the active power, control, logic, and protection circuitry required to implement a high voltage flyback converter and compliance with very low standby power requirements for modern consumer electronic power supplies. This device series is designed for direct operation from a rectified 240 VAC line source and requires minimal external components for a complete cost sensitive converter solution. Potential markets include cellular phone chargers, standby power supplies for personal computers, secondary bias supplies for microprocessor keep−alive supplies and IR detectors. A description of each of the functional blocks is given below, and the representative block diagram is shown in Figure 2.

This device series features an active startup regulator circuit that eliminates the need for an auxiliary bias winding on the converter transformer, fault logic with a programmable timer for converter overload protection, unique gated oscillator configuration for extremely fast loop response with double pulse suppression, oscillator frequency dithering with a controlled slew rate driver for reduced EMI, cycle−by−cycle current limiting, input undervoltage lockout with hysteresis, thermal shutdown, and auto restart or latched off fault detect device options. These devices are available in economical 8−pin PDIP and 4−pin SOT−223 packages.

Oscillator

The Oscillator is a unique fixed−frequency, duty−cycle−controlled oscillator. It charges and discharges an on chip timing capacitor to generate a precise square wave signal used to pulse width modulate the Power Switch Circuit. During the discharge of the timing capacitor, the Oscillator duty cycle output holds one input of the Driver low. This action keeps the Power Switch Circuit off, thus limiting the maximum duty cycle.

A frequency modulation feature is incorporated into the IC in order to aide in EMI reduction. Figure 3 illustrates this frequency modulation feature. The power supply voltage, V_{CC}, acts as the input to the built−in voltage controlled oscillator. As the V_{CC} voltage is swept across its nominal operating range of 7.5 to 8.5 V, the oscillator frequency is swept across its corresponding range.

The center oscillator frequency is internally programmed for 44 kHz, 100 kHz, or 136 kHz operation with a controlled charge to discharge current ratio that yields a maximum Power Switch duty cycle of 77%. The Oscillator temperature characteristics are shown in Figures 5 through 9. Contact an ON Semiconductor sales representative for further information regarding frequency options.

Control Input

The Control Input pin circuit has parallel source follower input stages with voltage clamps set at 1.35 and 4.6 V. Current sources clamp the input current through the followers at approximately 47.5 μA with 10 μA hysteresis. When a source or sink current in excess of this value is applied to this input, a logic signal generated internally changes state to block power switch conduction. Since the output of the Control Input sense is sampled continuously during t_{on} (77% duty cycle), it is possible to turn the Power Switch Circuit on or off at any time within t_{on}. Because it does not have to wait for the next cycle (rising edge of the clock signal) to switch on, and because it does not have to wait for current limit to turn off, the circuit has a very fast transient response as shown in Figure 3.

In a typical converter application the control input current is drawn by an optocoupler. The collector of the optocoupler is connected to the Control Input pin and the emitter is connected to ground. The optocoupler LED is mounted in series with a shunt regulator (typically a TL431) at the DC output of the converter. When the power supply output is greater than the reference voltage (shunt regulator voltage plus optocoupler diode voltage drop), the optocoupler turns on, pulling down on the Control Input. The control input logic is configured for line input sensing as well.

Turn On Latch

The Oscillator output is typically a 77% positive duty cycle square waveform. This waveform is inverted and applied to the reset input of the turn−on latch to prevent any power switch conduction during the guaranteed off time. This square wave is also gated by the output of the control section and applied to the set input of the same latch. Because of this gating action, the power switch can be activated when the control input is not asserted and the oscillator output is high.

The use of this unique gated Turn On Latch over an ordinary Gated Oscillator allows a faster load transient response. The power switch is allowed to turn on immediately, within the maximum duty cycle time period, when the control input signals a necessary change in state.

Turn Off Latch

A Turn Off Latch feature has been incorporated into this device series to protect the power switch circuit from excessive current, and to reduce the possibility of output overshoot in reaction to a sudden load removal. If the Power Switch current reaches the specified maximum current limit, the Current Limit Comparator resets the Turn Off Latch and turns the Power Switch Circuit off. The turn off latch is also reset when the Oscillator output signal goes low or the Control Input is asserted, thus terminating output MOSFET conduction. Because of this response to control input signals, it provides a very fast transient response and very tight load regulation. The turn off latch has an edge triggered set input which ensures that the switch can only be activated once during any oscillator period. This is commonly referred to as double pulse suppression.

Current Limit Comparator and Power Switch Circuit

The Power Switch Circuit is constructed with a SENSEFET™ in order to monitor the drain current. A portion of the current flowing through the circuit goes into a sense element, R_{sense}. The current limit comparator detects if the voltage across R_{sense} exceeds the reference level that is present at its inverting input. If this level is exceeded, the comparator quickly resets the Turn Off Latch, thus protecting the Power Switch Circuit.

A Leading Edge Blanking circuit was placed in the current sensing signal path to prevent a premature reset of the Turn Off Latch. A potential premature reset signal is generated each time the Power Switch Circuit is driven into conduction and appears as a narrow voltage spike across current sense resistor R_{sense}. The spike is due to the Power Switch Circuit gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior that masks the current signal until the Power Switch Circuit turn−on transition is completed. The current limit propagation delay time is typically 135 to 165 nanoseconds. This time is measured from when an overcurrent appears at the Power Switch Circuit drain, to the beginning of turn−off. Care must be taken during transformer saturation so that the maximum device current limit rating is not exceeded.

The high voltage Power Switch Circuit is monolithically integrated with the control logic circuitry and is designed to directly drive the converter transformer. Because the characteristics of the power switch circuit are well known, the gate drive has been tailored to control switching transitions to help limit electromagnetic interference (EMI). The Power Switch Circuit is capable of switching 700 V with an associated drain current that ranges nominally from 0.10 to 0.68 Amps.

Startup Circuit

Rectified AC line voltage is applied to the Startup Circuit on Pin 5, through the primary winding. The circuit is self−biasing and acts as a constant current source, gated by control logic. Upon application of the AC line voltage, this circuit routes current into the supply capacitor typically connected to Pin 1. During normal operation, this capacitor is hysteretically regulated from 7.5 to 8.5 V by monitoring the supply voltage with a comparator and controlling the startup current source accordingly. This Dynamic Self−Supply (DSS) functionality offers a great deal of applications flexibility as well. The startup circuit is rated at a maximum 700 V (maximum power dissipation limits must be observed).

Undervoltage Lockout

An Undervoltage Lockout (UVLO) comparator is included to guarantee that the integrated circuit has sufficient voltage to be fully functional. The UVLO comparator monitors the supply capacitor input voltage at Pin 1 and disables the Power Switch Circuit whenever the capacitor voltage drops below the undervoltage lockout threshold. When this level is crossed, the controller enters a new startup phase by turning the current source on. The supply voltage will then have to exceed the startup threshold in order to turn off the startup current source. Startup and normal operation of the converter are shown in Figure 3.

Fault Detector

The NCP105X series has integrated Fault Detector circuitry for detecting application fault conditions such as open loop, overload or a short circuited output. A timer is generated by driving the supply capacitor with a known current and hysteretically regulating the supply voltage between set thresholds. The timer period starts when the supply voltage reaches the nominal upper threshold of 8.5 V and stops when the drain current of the integrated circuit draws the supply capacitor voltage down to the undervoltage lockout threshold of 7.5 V.

If, during this timer period, no feedback has been applied to the control input, the fault detect logic is set to indicate an abnormal condition. This may occur, for example, when the optocoupler fails or the output of the application is overloaded or completely shorted. In this case, the part will stop switching, go into a low power mode, and begin to draw down the supply capacitor to the reset threshold voltage of 4.5 V. At that time, the startup circuit will turn on again to drive the supply to the turn on threshold. Then the part will begin the cycle again, effectively sampling the control input to determine if the fault condition has been removed. This mode is commonly referred to as burst mode operation and is shown is Figure 4.

Proper selection of the supply capacitor allows successful startup with monotonically increasing output voltage, without falsely sensing a fault condition. Figure 4 shows successful startup and the evolution of the signals involved in the presence of a fault.

Thermal Shutdown

The internal Thermal Shutdown block protects the device in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, one input of the Driver is held low to disable the Power Switch Circuit. The Power Switch is allowed to resume operation when the junction temperature falls below 85°C. The thermal shutdown feature is provided to prevent catastrophic device failures from accidental overheating. It is not intended to be used as a substitute for proper heatsinking.

APPLICATIONS

Two application examples have been provided in this document, and they are described in detail in this section. Figure 28 shows a Universal Input, 6 Watt Converter Application as well as a 5.5 Watt Charger Application using the NCP1053 @ 100 kHz. The Charger consists of the additional components Q1, C13, and R7 through R10, as shown. These were constructed and tested using the printed circuit board layout shown in Figure 40. The board consists of a fiberglass epoxy material (FR4) with a single side of two ounce per square foot (70 μm thick) copper foil. Test data from the two applications is given in Figures 29 through 39.

Both applications generate a well−regulated output voltage over a wide range of line input voltage and load current values. The charger application transitions to a constant current output if the load current is increased beyond a preset range. This can be very effective for battery charger application for portable products such as cellular telephones, personal digital assistants, and pagers. Using the NCP105X series in applications such as these offers a wide range of flexibility for the system designer.

The NCP105X application offers a low cost alternative to other applications. It uses a Dynamic Self−Supply (DSS) function to generate its own operating supply voltage such that an auxiliary transformer winding is not needed. (It also offers the flexibility to override this function with an auxiliary winding if ultra−low standby power is the designer's main concern.) This product also provides for automatic output overload, short circuit, and open loop protection by entering a programmable duty cycle burst mode of operation. This eliminates the need for expensive devices overrated for power dissipation or maximum current, or for redundant feedback loops.

The application shown in Figure 28 can be broken down into sections for the purpose of operating description. Components C1, L1 and C6 provide EMI filtering for the design, although this is very dependent upon board layout, component type, etc. D1 through D4 along with C2 provide the AC to bulk DC rectification. The NCP1053 drives the primary side of the transformer, and the capacitor, C5, is an integral part of the Dynamic Self−Supply. R1, C3, and D5 comprise an RCD snubber and R2 and C4 comprise a ringing damper both acting together to protect the IC from voltage transients greater than 700 volts and reduce radiated noise from the converter. Diode D6 along with C7−9, L2, C11, and C12 rectify the transformer secondary and filter the output to provide a tightly regulated DC output. IC3 is a shunt regulator that samples the output voltage by virtue of R5 and R6 to provide drive to the optocoupler, IC2, Light Emitting Diode (LED). C10 is used to compensate the shunt regulator. When the application is configured as a Charger, Q1 delivers additional drive to the optocoupler LED when in constant current operation by sampling the output current through R7 and R8.

Component Selection Guidelines

Choose snubber components R1, C3, and D5 such that the voltage on pin 5 is limited to the range from 0 to 700 volts. These components protect the IC from substrate injection if the voltage was to go below zero volts, and from avalanche if the voltage was to go above 700 volts, at the cost of slightly reduced efficiency. For lower power design, a simple RC snubber as shown, or connected to ground, can be sufficient. Ensure that these component values are chosen based upon the worst−case transformer leakage inductance and worst−case applied voltage. Choose R2 and C4 for best performance radiated switching noise.

Capacitor C5 serves multiple purposes. It is used along with the internal startup circuitry to provide power to the IC in lieu of a separate auxiliary winding. It also serves to provide timing for the oscillator frequency sweep for limiting the conducted EMI emissions. The value of C5 will also determine the response during an output fault (overload or short circuit) or open loop condition as shown in Figure 4, along with the total output capacitance.

Resistors R5 and R6 will determine the regulated output voltage along with the reference voltage chosen with IC3.

The base to emitter voltage drop of Q1 along with the value of R7 will set the fixed current limit value of the Charger application. R9 is used to limit the base current of Q1. Component R8 can be selected to keep the current limit fixed with very low values of output voltage or to provide current limit foldback with results as shown in Figures 29 and 33. A relatively large value of R8 allows for enough output voltage to effectively drive the optocoupler LED for fixed current limit. A low value of R8, along with resistor R10, provides for a low average output power using the fault protection feature when the output voltage is very low. C13 provides for output voltage stability when the Charger application is in current limit.

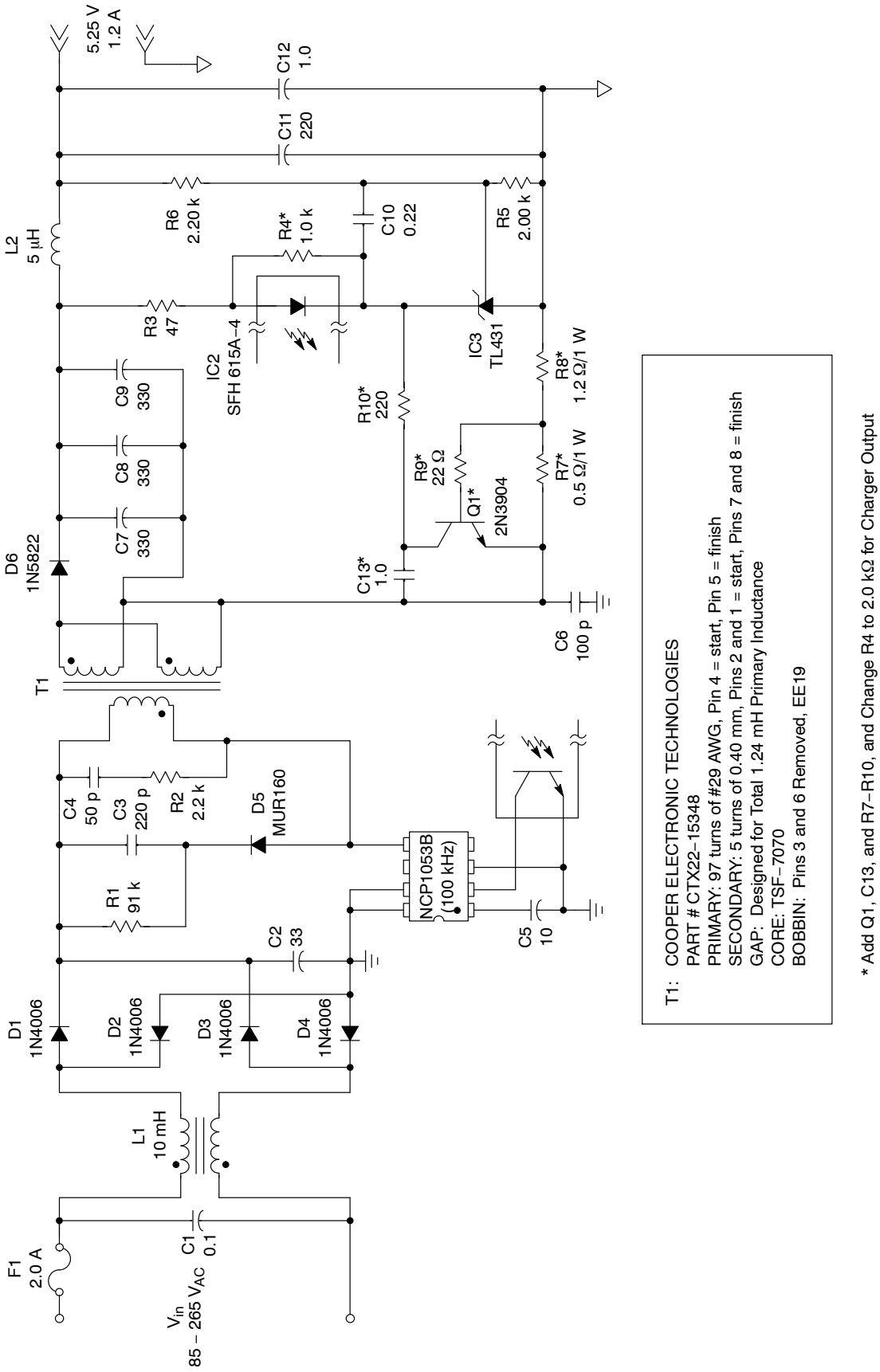


Figure 28. Universal Input 6/5 Watt Converter/Charger Application

Test	Conditions	Converter Results	Charger Results
Line Regulation	V_{in} = 85 – 265 V_{AC}; I_{out} = 120 mA I_{out} = 600 mA I_{out} = 1.2 A	2 mV 1 mV 2 mV	
	V_{in} = 85 – 265 V_{AC}; I_{out} = 100 mA I_{out} = 500 mA I_{out} = 1.00 A		11 mV 24 mV 41 mV
Load Regulation	V_{in} = 85 V_{AC}; I_{out} = 120 mA – 1.2 A V_{in} = 110 V_{AC}; I_{out} = 120 mA – 1.2 A V_{in} = 230 V_{AC}; I_{out} = 120 mA – 1.2 A V_{in} = 265 V_{AC}; I_{out} = 120 mA – 1.2 A	12 mV 13 mV 12 mV 13 mV	
	V_{in} = 85 V_{AC}; I_{out} = 100 mA – 1.00 A V_{in} = 110 V_{AC}; I_{out} = 100 mA – 1.00 A V_{in} = 230 V_{AC}; I_{out} = 100 mA – 1.00 A V_{in} = 265 V_{AC}; I_{out} = 100 mA – 1.00 A		58 mV 65 mV 71 mV 67 mV
Output Ripple	V_{in} = 110 V_{AC}; I_{out} = 1.2 A V_{in} = 230 V_{AC}; I_{out} = 1.2 A	86 mV_{p-p} 127 mV_{p-p}	
	V_{in} = 110 V_{AC}; I_{out} = 1.00 A V_{in} = 230 V_{AC}; I_{out} = 1.00 A		80 mV_{p-p} 155 mV_{p-p}
Efficiency	V_{in} = 110 V_{AC}; I_{out} = 1.2 A V_{in} = 230 V_{AC}; I_{out} = 1.2 A	72.4% 69.6%	
	V_{in} = 110 V_{AC}; R_8 = 1.2 Ω, I_{out} = 1.00 A V_{in} = 230 V_{AC}; R_8 = 1.2 Ω, I_{out} = 1.00 A		54.6% 53.6%
	V_{in} = 110 V_{AC}; R_8 = 0 Ω, I_{out} = 1.00 A V_{in} = 230 V_{AC}; R_8 = 0 Ω, I_{out} = 1.00 A		66.1% 63.3%
No Load Input Power	V_{in} = 110 V_{AC}; I_{out} = 0 A V_{in} = 230 V_{AC}; I_{out} = 0 A	100 mW 200 mW	100 mW 200 mW
Standby Output Power	V_{in} = 110 V_{AC}; P_{in} = 1 W V_{in} = 230 V_{AC}; P_{in} = 1 W	680 mW 630 mW	640 mW 540 mW
Short Circuit Load Input Power	V_{in} = 110 V_{AC}; V_{out} = 0 V (Shorted) V_{in} = 230 V_{AC}; V_{out} = 0 V (Shorted)	400 mW 550 mW	
	V_{in} = 110 V_{AC}; R_8 = 1.2 Ω, V_{out} = 0 V (Shorted) V_{in} = 230 V_{AC}; R_8 = 1.2 Ω, V_{out} = 0 V (Shorted)		750 mW 900 mW
	V_{in} = 110 V_{AC}; R_8 = 0 Ω, V_{out} = 0 V (Shorted) V_{in} = 230 V_{AC}; R_8 = 0 Ω, V_{out} = 0 V (Shorted)		700 mW 850 mW

Figure 29. Converter and Charger Test Data Summary

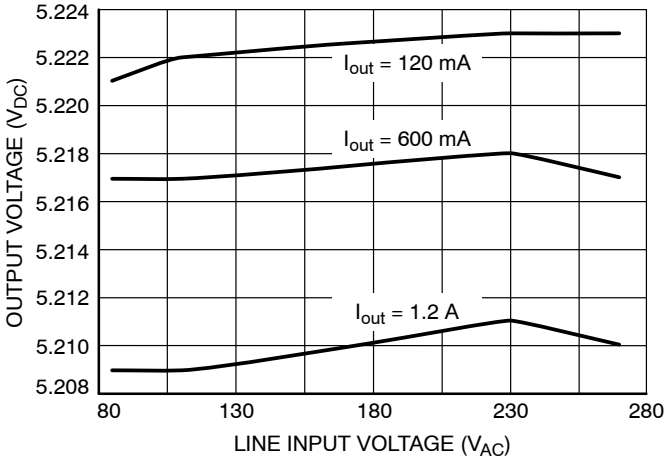


Figure 30. Converter Line Regulation

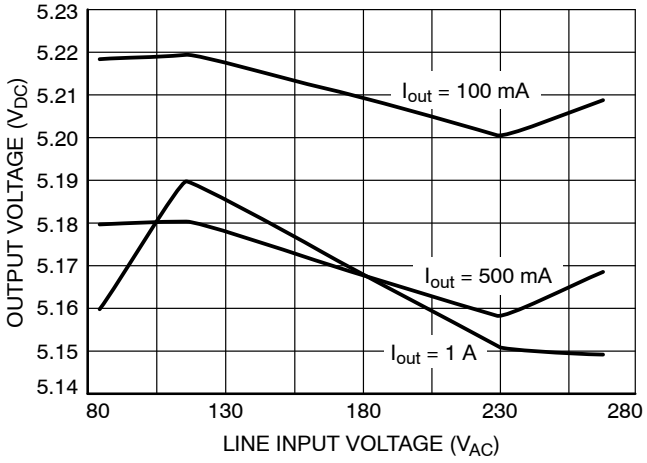


Figure 31. Charger Line Regulation

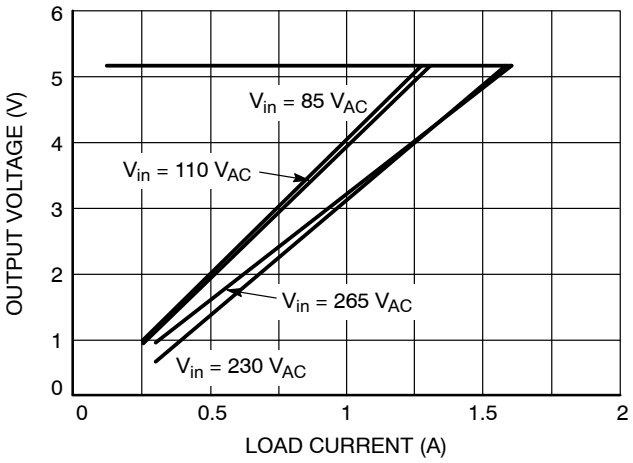


Figure 32. Converter Load Regulation

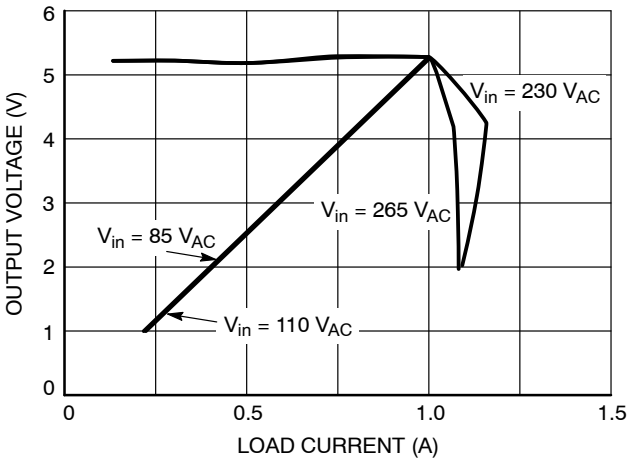


Figure 33. Charger Load Regulation

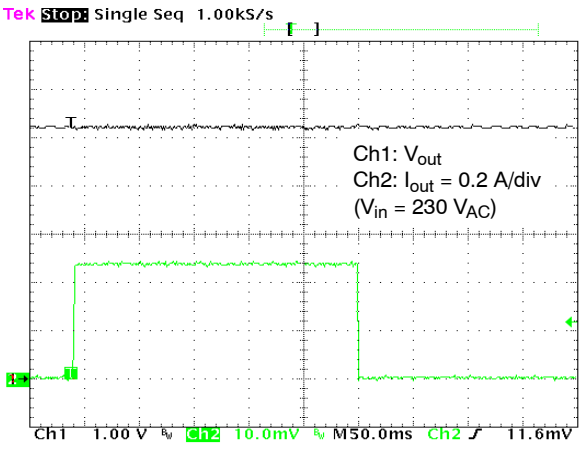


Figure 34. Converter Load Transient Response

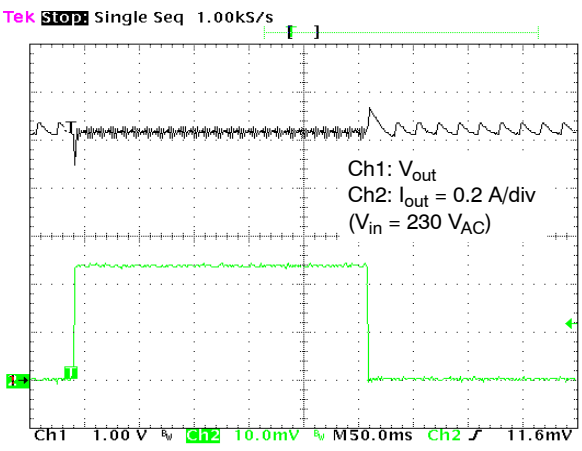


Figure 35. Charger Load Transient Response

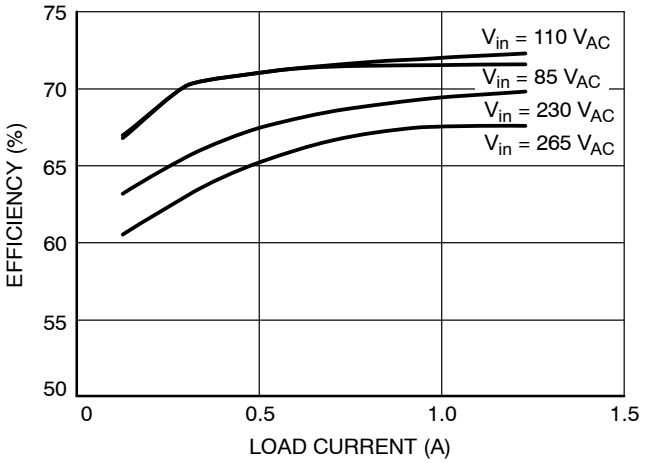


Figure 36. Converter Efficiency

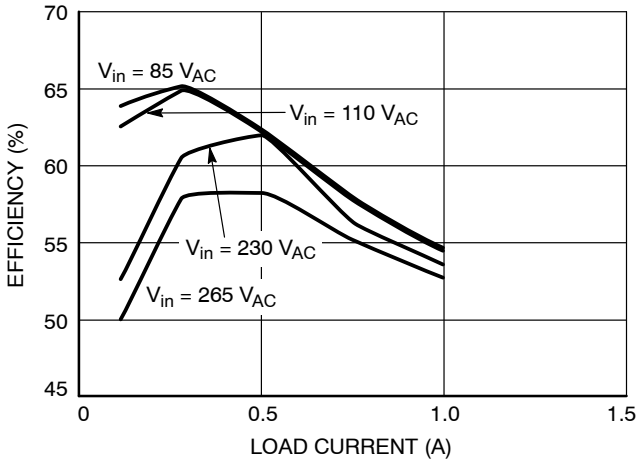


Figure 37. Charger Efficiency

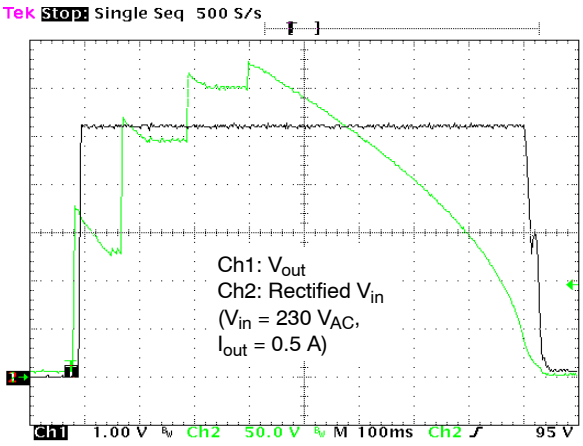


Figure 38. Converter On/Off Line Transient Response

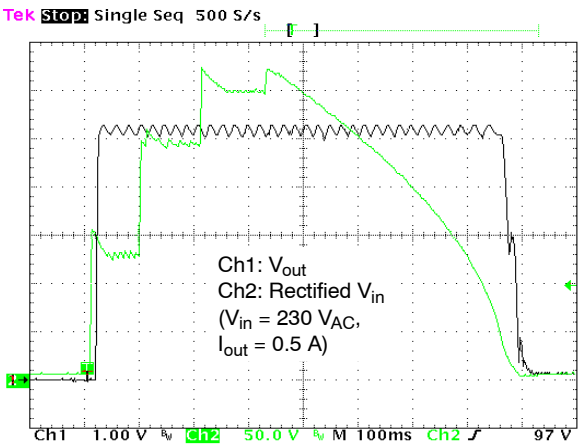
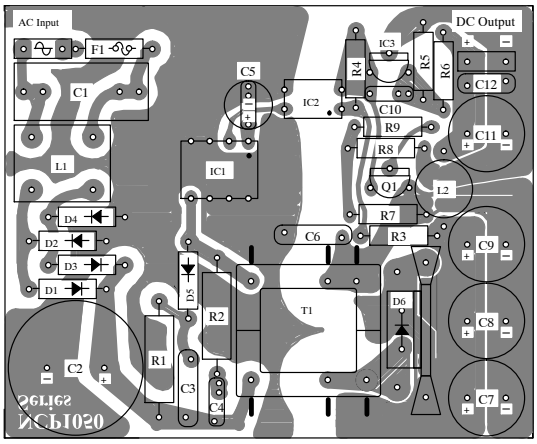
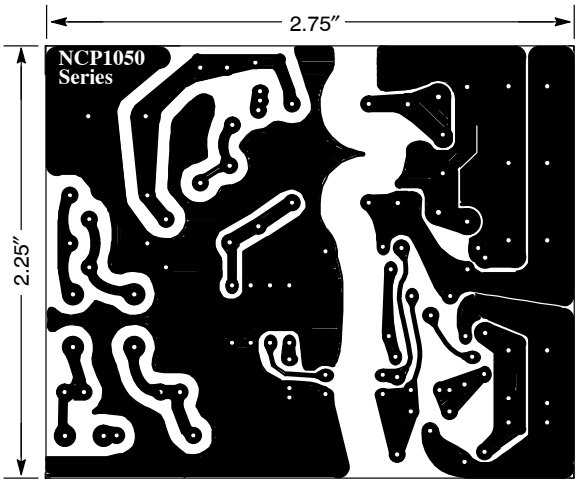


Figure 39. Charger On/Off Line Transient Response

BOARD GRAPHICS



Top View



Bottom View

Figure 40. Printed Circuit Board and Component Layout

DEVICE ORDERING INFORMATION (Note 11)

Device	$R_{DS(on)}$ (Ω)	I_{pk} (mA)	Package	Shipping†
NCP1050P44G	30	100	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1050P100G	30	100	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1050P136G	30	100	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1050ST44T3G	30	100	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1050ST100T3G	30	100	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1050ST136T3G	30	100	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1051P44G	30	200	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1051P100G	30	200	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1051P136G	30	200	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1051ST44T3G	30	200	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1051ST100T3G	30	200	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1051ST136T3G	30	200	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1052P44G	30	300	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1052P100G	30	300	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1052P136G	30	300	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1052ST44T3G	30	300	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1052ST100T3G	30	300	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1052ST136T3G	30	300	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1053P44G	15	400	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1053P100G	15	400	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1053P136G	15	400	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1053ST44T3G	15	400	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1053ST100T3G	15	400	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1053ST136T3G	15	400	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

11. Consult factory for additional optocoupler fail−safe latching, frequency, current limit and line input options.

DEVICE ORDERING INFORMATION (Note 11)

Device	$R_{DS(on)}$ (Ω)	I_{pk} (mA)	Package	Shipping†
NCP1054P44G	15	530	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1054P100G	15	530	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1054P136G	15	530	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1054ST44T3G	15	530	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1054ST100T3G	15	530	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1054ST136T3G	15	530	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1055P44G	15	680	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1055P100G	15	680	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1055P136G	15	680	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1055ST44T3G	15	680	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1055ST100T3G	15	680	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCP1055ST136T3G	15	680	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

11. Consult factory for additional optocoupler fail−safe latching, frequency, current limit and line input options.



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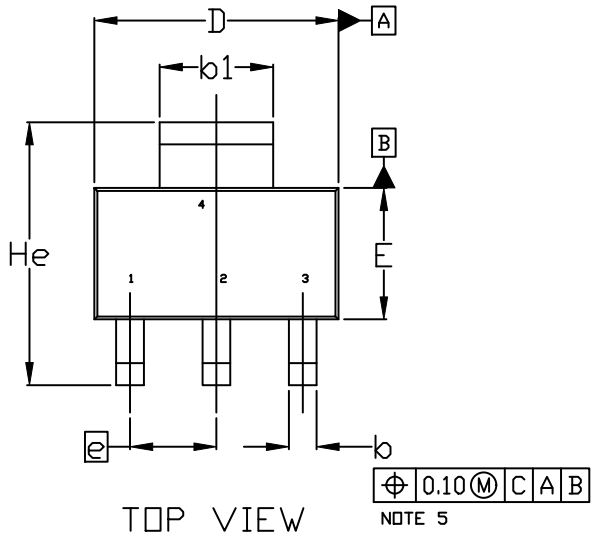
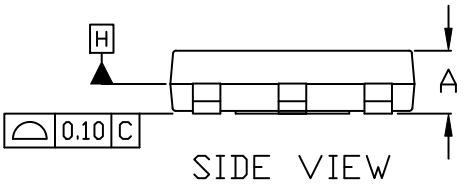
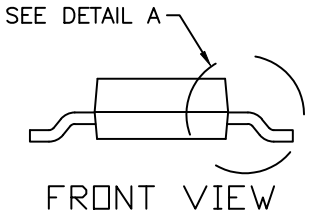
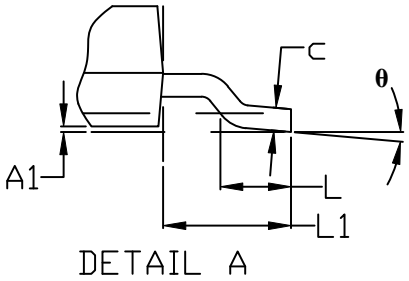
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



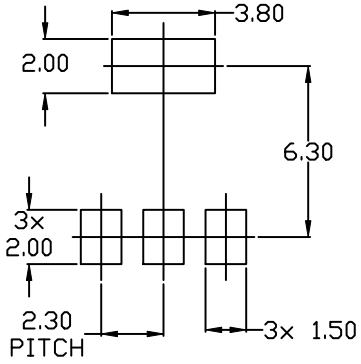






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

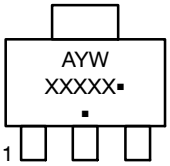
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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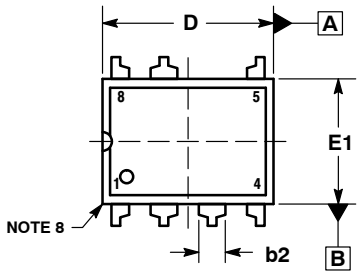
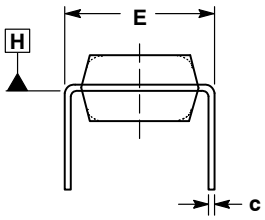
PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C

DATE 22 APR 2015

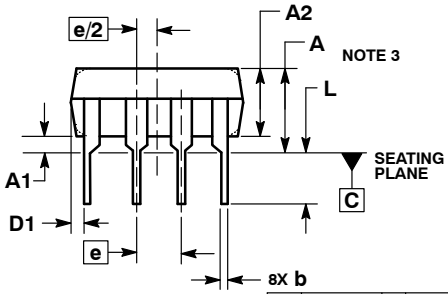
SCALE 1:1



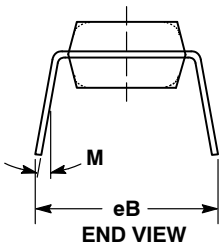
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

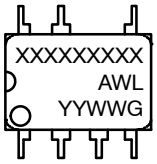


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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