LNK520
LinkSwitch Family

Energy Efficient, CV or CV/CC Switcher for Very Low Cost Chargers and Adapters

Product Highlights

Cost Effective Linear/RCC Replacement

- Lowest cost and component count, constant voltage (CV) or constant voltage/constant current (CV/CC) solutions
- Optimized for bias winding feedback
- Up to 75% lighter power supply reduces shipping cost
- Primary based CV/CC solution eliminates 10 to 20 secondary components for low system cost
- Fully integrated auto-restart for short circuit and open loop fault protection – saves external component costs
- 42 kHz operation with optimized switching characteristics for significantly reduced EMI

Much Higher Performance Over Linear/RCC

- Universal input range allows worldwide operation
- Up to 70% reduction in power dissipation – reduces enclosure size significantly
- CV/CC output characteristic without secondary feedback
- System level thermal and current limit protection
- Meets all single point failure requirements with only one additional bias capacitor
- Controlled current in CC region provides inherent soft-start
- Optional opto feedback improves output voltage accuracy

EcoSmart ™ – Extremely Energy Efficient

- Consumes <300 mW at 265 VAC input with no load
- Meets California Energy Commission (CEC), Energy Star, and EU requirements
- No current sense resistors – maximizes efficiency

Applications

- Linear transformer replacement in all ≤3 W applications
- Chargers for cell phones, cordless phones, PDAs, digital cameras, MP3/portable audio devices, shavers, etc.
- Home appliances, white goods and consumer electronics
- Constant output current LED lighting applications
- TV standby and other auxiliary supplies

Description

LinkSwitch™ is specifically designed to replace low power linear transformer/RCC chargers and adapters at equal or lower system cost with much higher performance and energy efficiency. LNK520 is equivalent to LNK500 but optimized for use with bias winding feedback and has improved switching characteristics for significantly reduced EMI. In addition, if bias and output windings are magnetically well coupled, output voltage load regulation can be improved. With efficiency of up to 75% and <300 mW no-load consumption, a LinkSwitch solution can save the end user enough energy over a linear design to completely pay for the full power supply cost in less than one year. LinkSwitch integrates a 700 V power MOSFET, PWM control, high voltage start-up, current limit, and thermal shutdown circuitry, onto a monolithic IC.

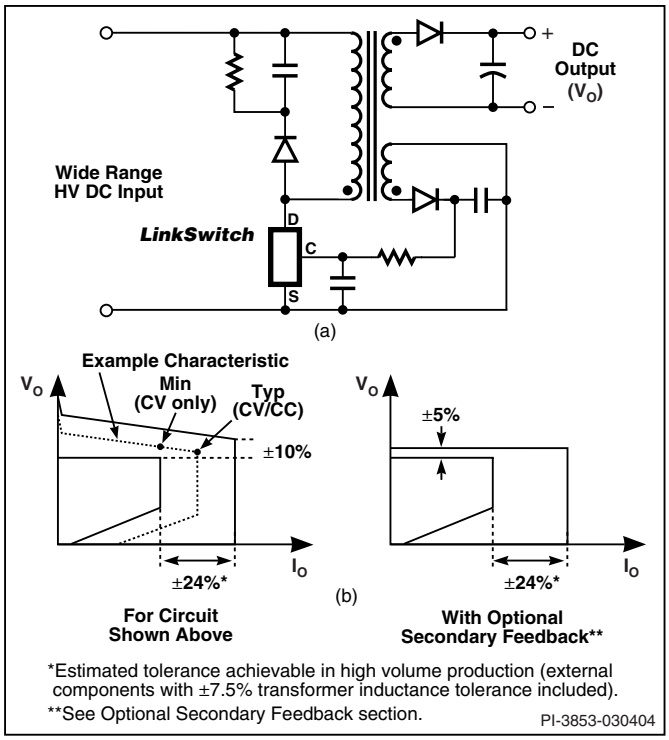


Figure 1. (a) Typical Application – not a Simplified Circuit and (b) Output Characteristic Tolerance Envelopes.

Output Power Table[1]

PRODUCT[4]	230 VAC ±15%		85-265 VAC		No-Load Input Power
	Min[2]	Typ[2]	Min[2]	Typ[2]	
LNK520 P or G	3.3 W	4 W	2.4 W	3 W	<300 mW
	4.2 W	5.5 W	2.9 W	3.5 W	<500 mW[3]

Table 1. Notes: 1. Output power for designs in an enclosed adapter measured at 50 °C ambient. 2. See Figure 1 (b) for Min (CV only designs) and Typ (CV/CC charger designs) power points identified on output characteristic. 3. Uses higher reflected voltage transformer designs for increased power capability – see Key Application Considerations section. 4. For lead-free package options, see Part Ordering Information.

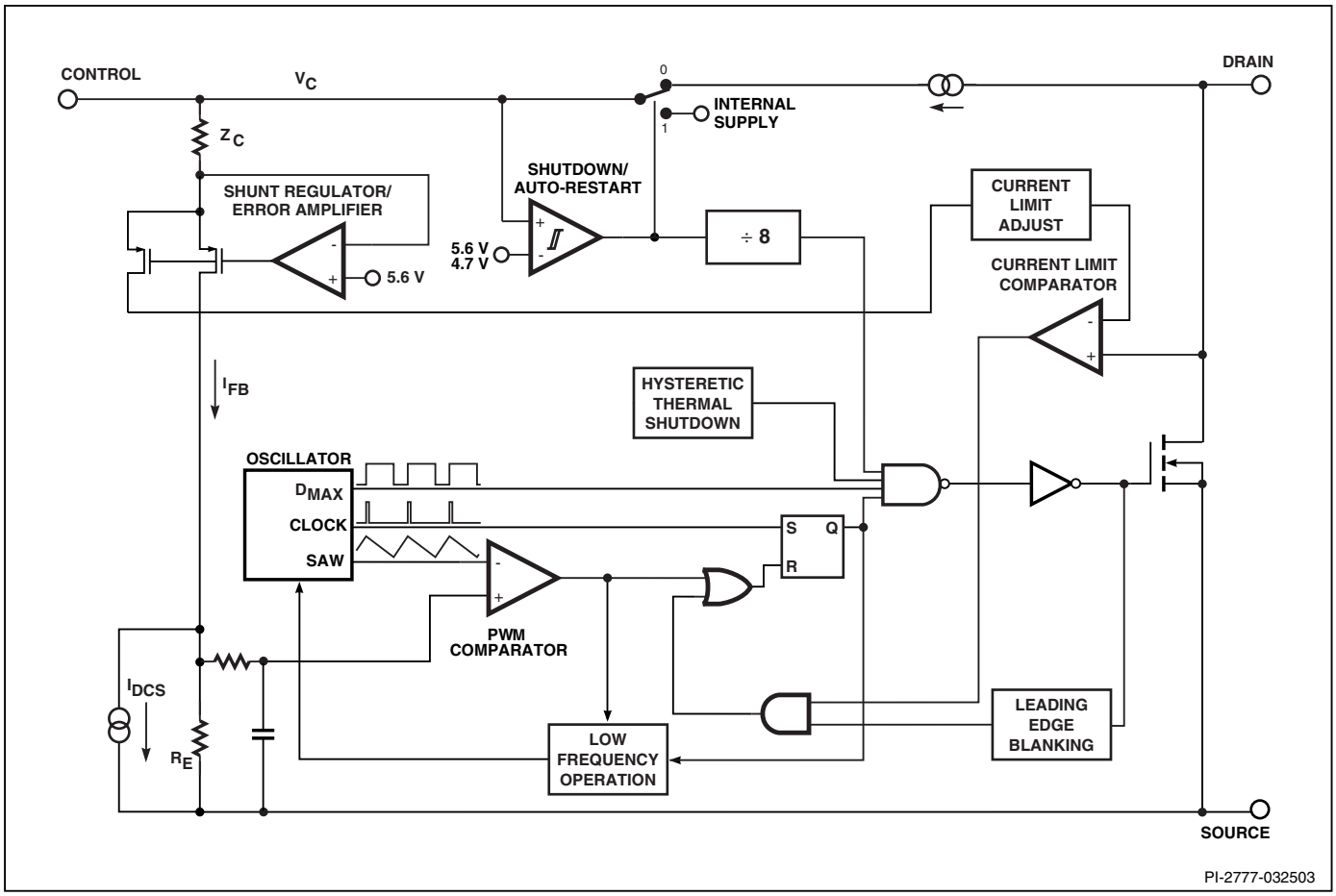


Figure 2. Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. Provides internal operating current for start-up. Internal current limit sense point for drain current.

CONTROL (C) Pin:
Error amplifier and feedback current input pin for duty cycle and current limit control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the connection point for the supply bypass and auto-restart/compensation capacitor.

SOURCE (S) Pin:
Output MOSFET source connection for high voltage power return. Primary side control circuit common and reference point.

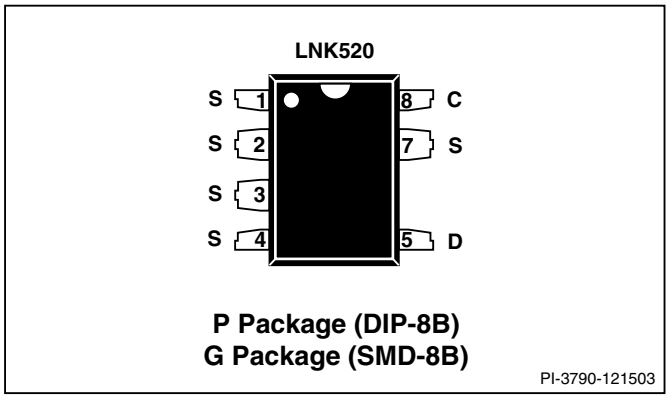


Figure 3. Pin Configuration.

LinkSwitch Functional Description

The duty cycle, current limit and operating frequency relationships with CONTROL pin current are shown in Figure 4. Figure 5 shows a typical power supply schematic outline which is used below to describe the LinkSwitch operation.

Power Up

During power up, as V_{IN} is first applied (Figure 5), the CONTROL pin capacitor C1 is charged through a switched high voltage current source connected internally between the DRAIN and CONTROL pins (see Figure 2). When the CONTROL pin voltage reaches approximately 5.6 V relative to the SOURCE pin, the high voltage current source is turned off, the internal control circuitry is activated and the high voltage internal MOSFET starts to switch. At this point, the charge stored on C1 is used to supply the internal consumption of the chip.

Constant Current (CC) Operation

As the output voltage, and therefore the reflected voltage across the transformer bias winding ramp up, the feedback CONTROL current I_C flowing through R1 increases. As shown in Figure 4, the internal current limit increases with I_C and reaches I_{LIM} when I_C is equal to I_{DCT}. The internal current limit vs. I_C characteristic is designed to provide an approximately constant power supply output current as the power supply output voltage rises.

Constant Voltage (CV) Operation

When I_C exceeds I_{DCS}, typically 2 mA (Figure 4), the maximum duty cycle is reduced. At a value of I_C that depends on power supply input voltage, the duty cycle control limits LinkSwitch peak current below the internal current limit value. At this point the power supply transitions from CC to CV operation. With minimum input voltage in a typical universal input design, this transition occurs at approximately 30% duty cycle. Resistor R1 (Figure 5) is therefore initially selected to conduct a value of I_C approximately equal to I_{DCT} when V_{OUT} is at the desired value at the minimum power supply input voltage. The final choice of R1 is made when the rest of the circuit design is complete. When the duty cycle drops below approximately 4%, the frequency is reduced, which reduces energy consumption under light load conditions.

Auto-Restart Operation

When a fault condition, such as an output short circuit or open loop, prevents flow of an external current into the CONTROL pin, the capacitor C1 discharges towards 4.7 V. At 4.7 V, auto-restart is activated, which turns the MOSFET off and puts the control circuitry in a low current fault protection mode. In auto-restart, LinkSwitch periodically restarts the power supply so that normal power supply operation can be restored when the fault is removed.

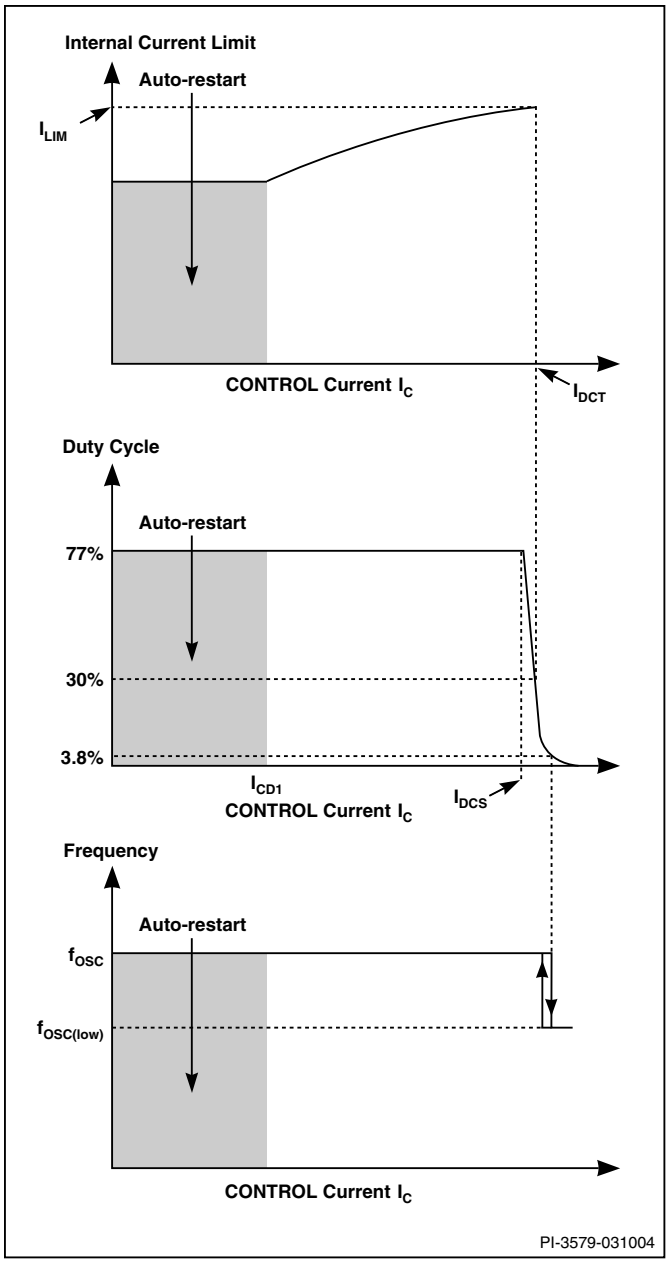


Figure 4. CONTROL Characteristics.

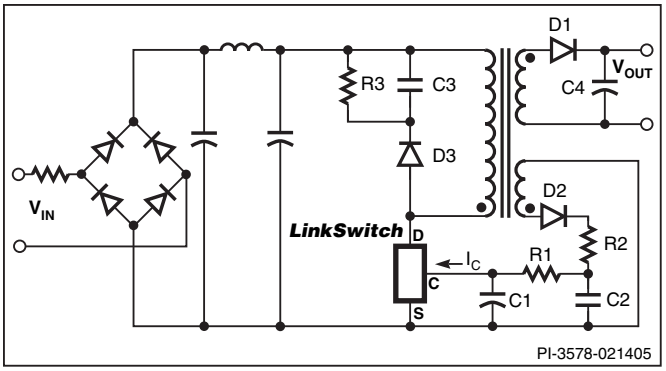


Figure 5. Power Supply Schematic outline.

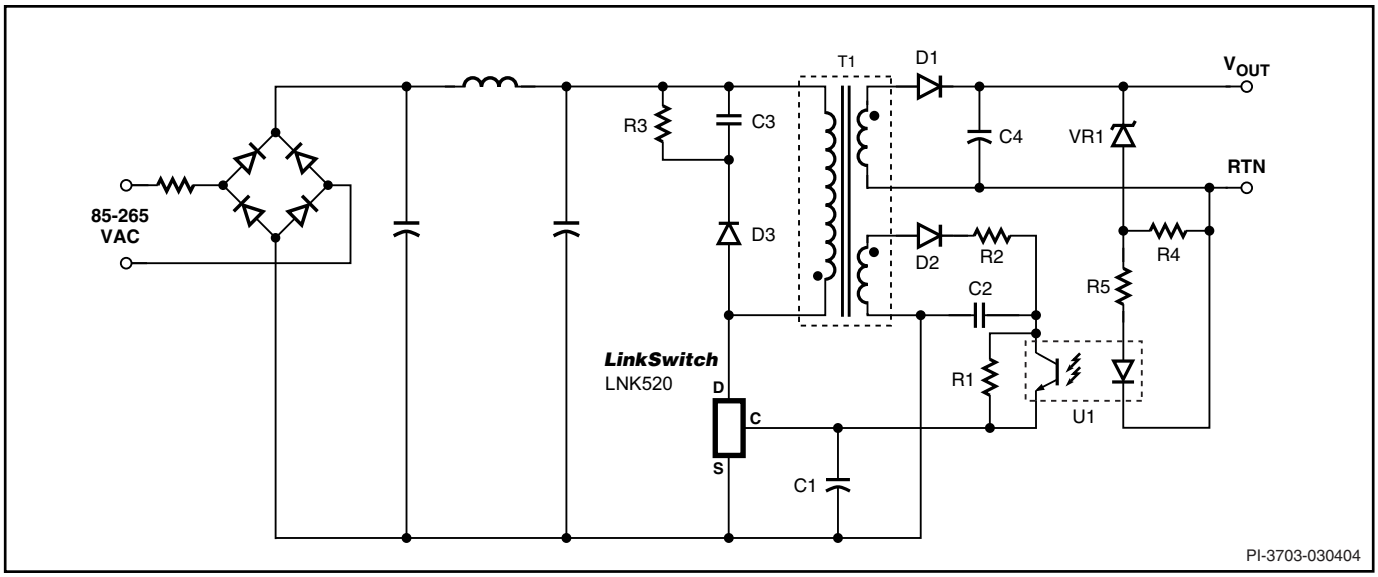


Figure 6. Power Supply Schematic Outline with Optocoupler Feedback, Providing Tight CV Regulation.

The characteristics described above provide an approximate CV/CC power supply output without the need for secondary side voltage or current feedback. The output voltage regulation is influenced by how well the voltage across C2 tracks the reflected output voltage. This tracking is influenced by the coupling between transformer output and bias windings. Tight coupling improves CV regulation and requires only a low value for resistor R2. Poor coupling degrades CV regulation and requires a higher value for R2 to filter leakage inductance spikes on the bias winding voltage waveform. This circuitry, used with standard transformer construction techniques, provides much better output load regulation than a linear transformer, making this an ideal power supply solution in many low power applications. If even tighter load regulation is required, an optocoupler configuration can be used while still employing the constant output current characteristics provided by LinkSwitch.

Optional Secondary Feedback

Figure 6 shows a typical power supply schematic outline using LinkSwitch with optocoupler feedback to improve output voltage regulation. On the primary side, the schematic only differs from Figure 5 by the addition of optocoupler U1 transistor in parallel to R1.

On the secondary side, the addition of voltage sense circuit components R4, VR1 and U1 LED provide the voltage feedback signal. In the example shown, a simple Zener (VR1) reference is used though more accurate references may be employed for improved output voltage tolerancing and to provide cable drop compensation, if required. Resistor R4 provides biasing for VR1. The regulated output voltage is equal to the sum of the VR1 Zener voltage plus the forward voltage drop of the U1 LED. Resistor R5 is an optional low value resistor to limit U1 LED peak current due to output ripple. Manufacturer's specifications for U1 current and VR1 slope resistance should be consulted to determine whether R5 is required.

When the power supply operates in the constant current (CC) region, for example at start up and when charging a battery, the output voltage is below the voltage feedback threshold defined by U1 and VR1 and the optocoupler is fully off. In this region, the circuit behaves exactly as previously described with reference to Figure 5 where the voltage across C2 and therefore the current flowing through R1 increases with increasing output voltage and the LinkSwitch internal current limit is adjusted to provide an approximate CC output characteristic.

When the output reaches the voltage feedback threshold set by U1 and VR1, the optocoupler turns on. Any further increase in the power supply output voltage results in the U1 transistor current increasing. The resulting increase in the LinkSwitch CONTROL current reduces the duty cycle according to Figure 4 and therefore, maintains the output voltage regulation.

Figure 7 shows the influence of optocoupler feedback on the output characteristic. The envelope defined by the dashed lines represent the worst-case power supply DC output voltage and current tolerances (unit-to-unit and over the input voltage range) if an optocoupler is not used. A typical example of an inherent (without optocoupler) output characteristic is shown dotted. This is the characteristic that would result if U1, R4, R5 and VR1 were removed. The optocoupler feedback results in the characteristic shown by the solid line. The load variation arrow in Figure 7 represents the locus of the output characteristic normally seen during a battery charging cycle. The two characteristics are identical as the output voltage rises but then separate as shown when the voltage feedback threshold is reached. This is the characteristic seen if the voltage feedback threshold is above the output voltage at the inherent CC to CV transition point also indicated in Figure 7.

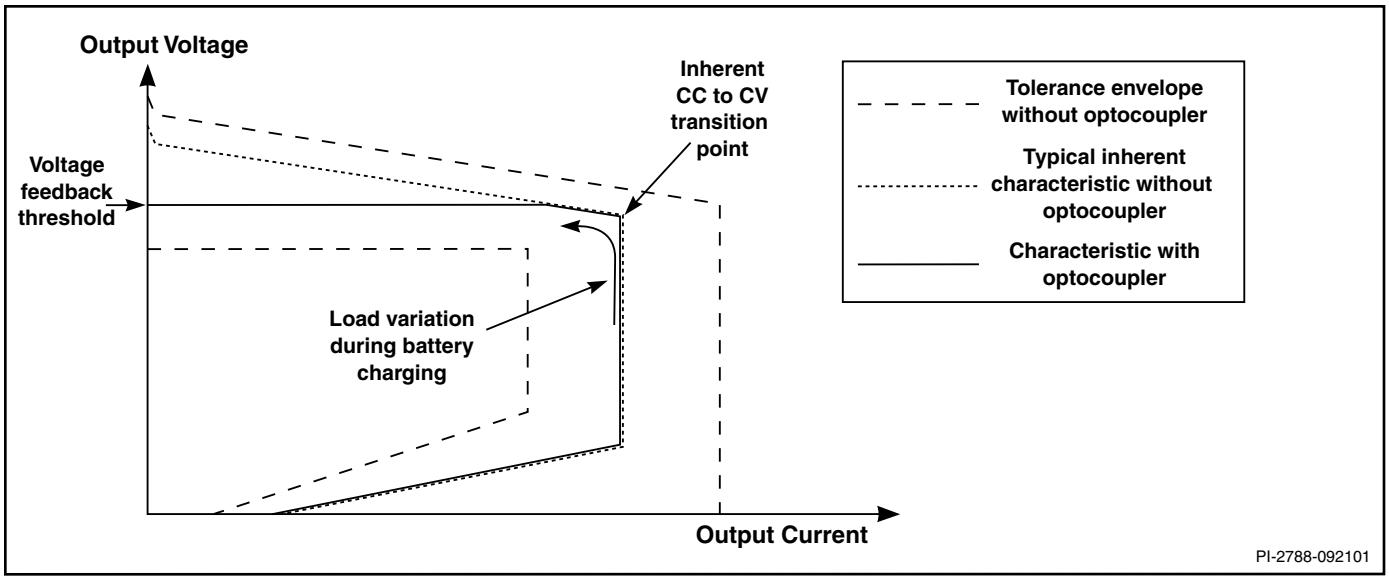


Figure 7. Influence of the Optocoupler on the Power Supply Output Characteristic.

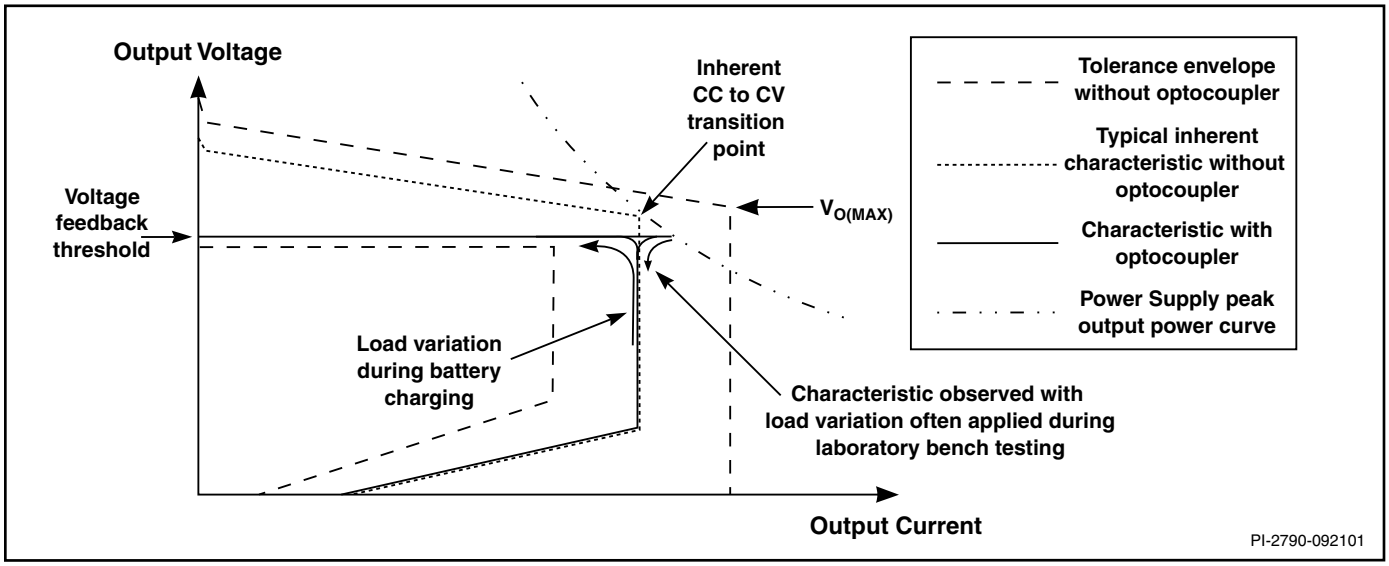


Figure 8. Output Characteristic with Optocoupler Regulation (Reduced Voltage Feedback Threshold).

Figure 8 shows a case where the voltage feedback threshold is set below the voltage at the inherent CC to CV transition point. In this case, as the output voltage rises, the secondary feedback circuit takes control before the inherent CC to CV transition occurs. In an actual battery charging application, this simply limits the output voltage to a lower value. However, in laboratory bench tests, it is often more convenient to test the power supply output characteristic starting from a low output current and gradually increasing the load. In this case, the optocoupler feedback regulates the output voltage until the peak output power curve is reached as shown in Figure 8. Under these conditions, the output current will continue to rise until the peak power point is reached and the optocoupler turns off. Once the optocoupler is off, the CONTROL pin feedback current is determined only by R1 and the output current therefore folds back to the inherent CC characteristic as shown. Since this type of load transition does not normally occur in a battery charger, the output current never overshoots the inherent constant current value in the actual application.

In some applications it may be necessary to avoid any output current overshoot, independent of the direction of load variation. To achieve this goal, the minimum voltage feedback threshold should be set at $V_{O(MAX)}$. This will ensure that the voltage at the CC to CV transition point of the inherent characteristic will always occur below the voltage feedback threshold. However, the output voltage tolerance is then increased, since the inherent CV characteristic tolerance below $V_{O(MAX)}$ is added to the tolerance of the optocoupler feedback circuit.

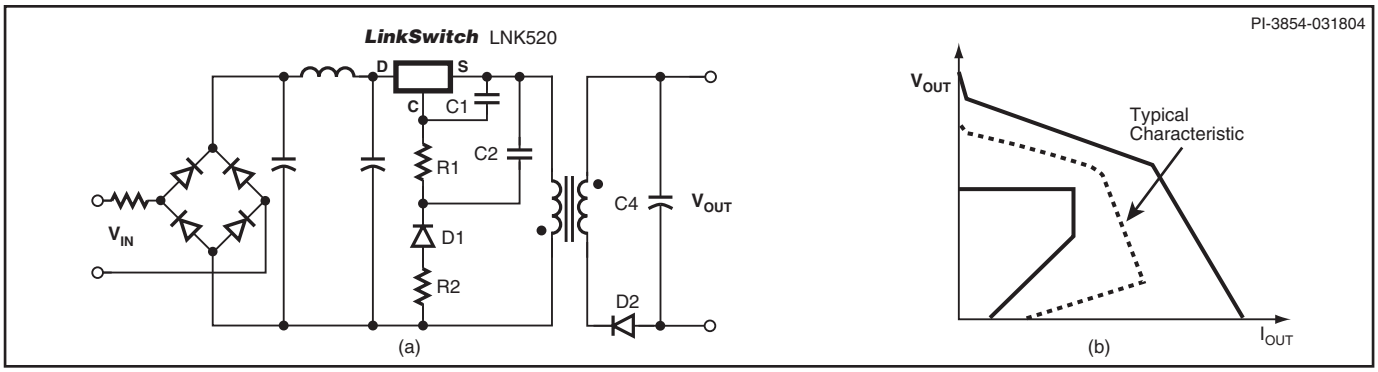


Figure 9. High-side Configuration Using LNK520: (a) Schematic Outline; (b) Typical Output Characteristic Envelope.

The LNK520 can also be used in the high-side configuration as shown in Figure 9(a). This configuration provides a very low component count solution with an approximate CV/CC power supply output characteristic. A typical output characteristic envelope is shown in Figure 9(b).

This configuration is ideal for very low cost charger and adapter applications where output CC tolerance is loose or unspecified. Typical applications include low cost chargers and adapters where direct replacement for a linear transformer is required. In applications with a high voltage DC input voltage, the circuit is further simplified with the removal of input rectifiers, EMI filter choke and input capacitors. Typical applications of this type include auxiliary supplies in domestic appliances and industrial applications.

In the high-side configuration, the CONTROL pin receives feedback current through R1 generated by the voltage across C2. To a first order, this voltage is proportional to V_{OUT} since V_{OUT} is reflected to the primary and appears across C2 during the off time of the LNK520 switching cycle. The output CV regulation is therefore determined by how well the voltage across C2 tracks the output voltage. This tracking is influenced by the value of the transformer leakage inductance, which introduces an error. This error, which is partially filtered by R2 and C2, causes a slope in the output CV regulation characteristic. The LNK520 is optimized for use with a bias winding where tracking of feedback voltage and output voltage is typically better than it is in the high-side configuration of Figure 9 (a). As a consequence, the increased leakage error in the high-side configuration causes the output current to increase with falling output voltage, as indicated by the output CC characteristic envelope in Figure 9 (b).

In this high-side configuration, the SOURCE pins and circuit board traces form a switching node. Extra care should be taken to optimize EMI performance. The LNK520 internal MOSFET switching characteristics have been designed to significantly reduce EMI, particularly in the radiated spectrum (>30 MHz). However, the SOURCE trace area should be minimized and EMI filter components should be distanced from the SOURCE node whenever possible. In embedded applications where a high voltage DC input voltage is available, system level EMI filtering is typically located away from the power supply and circuit board layout is less critical.

Applications Example

The circuit shown in Figure 10 shows a typical implementation of an approximate constant voltage / constant current (CV/CC) charger using LinkSwitch in the low-side configuration. This design delivers 2.75 W with nominal peak power point voltage of 5.5 V and a current of 500 mA (Figure 11). Efficiency is greater than 65% over an input range of 85 VAC to 265 VAC.

The bridge rectifier, D1-D4, rectifies the AC input. The rectified AC is smoothed by C1 and C2, with inductor L1 forming a pi-filter to filter differential mode conducted EMI. Resistor RF1 is a fusible, flameproof type providing protection from primary-side short circuits and line surges and provides additional differential EMI filtering. The switching frequency of 42 kHz allows such a simple EMI filter to be used without the need for a Y capacitor while still meeting international EMI standards.

When power is applied, high voltage DC appears at the DRAIN pin of LinkSwitch (U1). The CONTROL pin capacitor C5 is then charged through a switched high voltage current source connected internally between the DRAIN and CONTROL pins. When the CONTROL pin reaches approximately 5.6 V relative to the SOURCE pin, the internal current source is turned off. The internal control circuitry is activated and the high voltage MOSFET starts to switch, using the energy in C5 to power the IC.

The secondary of the transformer is rectified and filtered by D7 and C6 to provide the DC output to the load. LinkSwitch dramatically simplifies the secondary side by controlling both the constant voltage and constant current regions entirely from the primary side. This is achieved by monitoring the primary-side bias voltage.

Diode D5, C4, R1 and R2 form the primary clamp network. This limits the peak DRAIN voltage due to leakage inductance. Resistor R2 allows the use of a slow, low cost rectifier diode by limiting the reverse current through D5 when U1 turns on. The selection of a slow diode improves radiated EMI and also improves CV regulation, especially at no-load.

The output during CV operation is equal to the primary-side bias voltage multiplied by the turns ratio. The bias voltage, in turn, is the sum of the CONTROL pin voltage (approximately

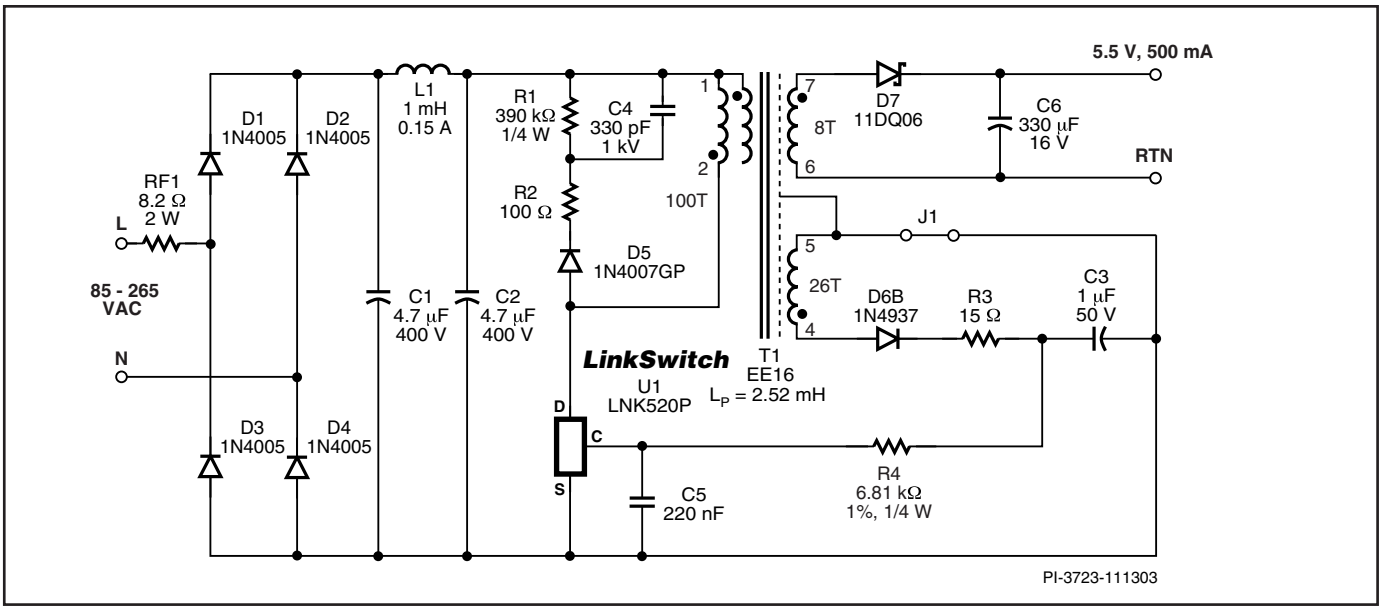


Figure 10. 2.75 W Constant Voltage/Constant Current (CV/CC) Charger Using LinkSwitch.

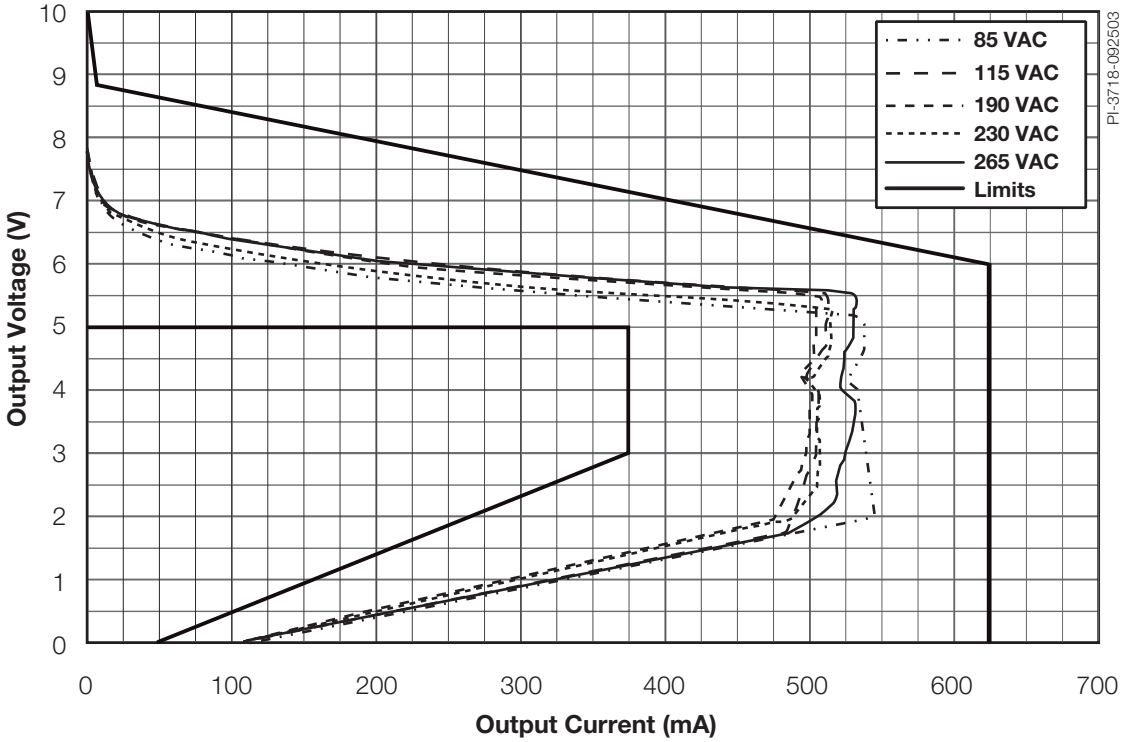


Figure 11. Measured Output Characteristic of the Circuit in Figure 10.

5.7 V), the voltage across the bias feedback resistor R4 and the forward voltage of D6B. Resistor R3 can be neglected as proportionally the voltage drop across this resistance is small. In CV operation, the voltage across R4 is equal to the CONTROL pin current, I_{DCT} (2.15 mA) multiplied by the value of R4.

As the output load is decreased, the output and therefore bias voltage increase resulting in increased current into the CONTROL pin. As the current into the CONTROL pin exceeds I_{DCS} (~2 mA), the duty cycle begins to reduce, maintaining regulation of the output, reaching 30% at a CONTROL pin current of 2.15 mA.

Under light or no-load conditions, when the duty cycle reaches approximately 4%, the switching frequency is reduced from 44 kHz to 29 kHz to lower light and no-load input power.

As the output load is increased, the peak power point (defined by $0.5 \cdot L_P \cdot I_{LIM}^2 \cdot f$) is exceeded. The output voltage and therefore primary-side bias voltage reduce. The reduction in the bias voltage results in a proportional reduction of CONTROL pin current, which lowers the internal LinkSwitch current limit (current limit control).

Constant current (CC) operation controls secondary-side output current by reducing the primary-side current limit. The current limit reduction characteristic has been optimized to maintain an approximate constant output current as the output voltage and therefore, bias voltage is reduced.

If the load is increased further and the CONTROL pin current falls below approximately 0.8 mA, the CONTROL pin capacitor C5 will discharge and LinkSwitch will enter auto-restart operation.

Current limit control removes the need for any secondary-side current sensing components (sense resistor, transistor, optocoupler and associated components). Removing the secondary sense circuit dramatically improves efficiency, giving the associated benefit of reduced enclosure size.

Key Application Considerations

Design Output Power

Table 1 (front page) shows the maximum continuous output power that can be obtained under the following conditions:

1. The minimum DC input bus voltage is 90 V or higher. This corresponds to a filter capacitor of 3 μF/W for universal input and 1 μF/W for 230 VAC or 115 VAC input with doubler input stage.
2. Design is a discontinuous mode flyback converter with nominal primary inductance value and a V_{OR} in the range 40 V to 80 V. Continuous mode designs can result in loop instability and are therefore not recommended.
3. A secondary output of 5 V with a Schottky rectifier diode.
4. Assumed efficiency of 65%.
5. The part is board mounted with SOURCE pins soldered to sufficient area of copper to keep the die temperature at or below 100 °C.
6. An output cable with a total resistance of 0.2 Ω.

In addition to the thermal environment (sealed enclosure, ventilated, open frame, etc.), the maximum power capability of LinkSwitch in a given application depends on transformer core size, efficiency, primary inductance tolerance, minimum specified input voltage, input storage capacitance, output voltage, output diode forward drop, etc., and can be different from the values shown in Table 1.

Transformer Design

To provide an approximately CV/CC output, the transformer should be designed to be discontinuous; all the energy stored in the transformer is transferred to the secondary during the MOSFET off time. Energy transfer in discontinuous mode is independent of line voltage.

The peak power point prior to entering constant current operation is defined by the maximum power transferred by the transformer. The power transferred is given by the expression $P = 0.5 \cdot L_P \cdot I^2 \cdot f$, where L_P is the primary inductance, I^2 is the primary peak current squared and f is the switching frequency.

To simplify analysis, the data sheet parameter table specifies an I^2f coefficient. This is the product of current limit squared and switching frequency normalized to the feedback parameter I_{DCT}. This provides a single term that specifies the variation of the peak power point in the power supply due to LinkSwitch.

As primary inductance tolerance is part of the expression that determines the peak output power point (start of the CC characteristic) this parameter should be well controlled. For an estimated overall constant current tolerance of ±24%, the primary inductance tolerance should be ±7.5% or better. This is achievable using standard low cost, center leg gapping techniques where the gap size is typically 0.08 mm or larger. Smaller gap sizes are possible but require non-standard, tighter ferrite A_L tolerances.

Other gapping techniques such as film gapping allow tighter tolerances (±7% or better) with associated improvements in the tolerance of the peak power point. Please consult your transformer vendor for guidance.

Core gaps should be uniform. Uneven core gapping, especially with small gap sizes, may cause variation in the primary inductance with flux density (partial saturation) and make the constant current region non-linear. To verify uniform gapping, it is recommended that the primary current wave-shape be examined while feeding the supply from a DC source. The gradient is defined as di/dt = V/L and should remain constant throughout the MOSFET on time. Any change in gradient of the current ramp is an indication of uneven gapping.

Measurements made using a LCR bridge should not be solely relied upon; typically these instruments only measure at currents of a few milliamps. This is insufficient to generate high enough flux densities in the core to show uneven gapping.

For a typical EE16 or EE13 core using center leg gapping, a 0.08 mm gap allows a primary inductance tolerance of ±10% to be maintained in standard high volume production. This allows the EE13 to be used in designs up to 2.75 W with less than 300 mW no-load consumption. Using outer leg film gapping reduces inductance tolerance to ±7% or better, allowing designs up to 3 W. Using the larger EE16 allows for a 3 W output with center leg gapping. The EE13 core size may be attractive in designs were space is limited or if there is a cost advantage over the EE16.

The transformer turns ratio should be selected to give a V_{OR} (output voltage reflected through secondary to primary turns ratio) of 40 V to 80 V. Higher V_{OR} increases the output power capability of LinkSwitch but also increases no-load power consumption. This allows even higher values to be used in designs where no-load power is not a concern. However care should be taken to ensure that the maximum temperature rise of the device is acceptable at the upper limit of the output characteristic when used in a charger application. In all cases, discontinuous mode operation should be maintained and note that the linearity of the CC region of the power supply output characteristic is influenced by the bias voltage. If this is an important aspect of the application, the output characteristic should be checked before finalizing the design.

Output Characteristic Variation

Both the device tolerance and external circuit govern the overall tolerance of the LinkSwitch power supply output characteristic. Estimated peak power point tolerances for a LNK520, 2.75 W design are ±10% for voltage and ±24% for current limit for overall variation in high volume manufacturing. This includes device and transformer tolerances (±7.5% assumed) and line variation. Lower power designs may have poorer constant current linearity.

As the output load reduces from the peak power point, the output voltage will tend to rise due to tracking errors compared to the load terminals. Sources of these errors include the output cable drop, output diode forward voltage and leakage inductance, which is the dominant cause. As the load reduces, the primary operating peak current reduces, together with the leakage inductance energy, which reduces the peak charging of the clamp capacitor.

At very light or no-load, typically less than 2 mA of output current, the output voltage rises due to leakage inductance peak charging of the secondary. This voltage rise can be reduced with a small preload with little change to no-load power consumption. The output voltage load variation can be improved across the whole load range by adding an optocoupler and secondary reference (Figure 6). The secondary reference is designed to only provide feedback above the normal peak power point voltage to maintain the correct constant current characteristic.

Component Selection

The schematic shown in Figure 10 outlines the key components needed for a LinkSwitch supply.

Clamp diode – D5

Diode D5 can be an ultra-fast (t_{rr} < 50 ns), a fast (t_{rr} < 250 ns) or standard recovery diode with a voltage rating of 600 V or higher. A standard recovery diode is recommended as it improves the CV characteristic, but should be a glass-passivated type (1N400xGP) to ensure a defined reverse recovery time.

Clamp Capacitor – C4

Capacitor C4 should be in the range of 100 pF to 1000 pF, 500 V capacitor. A low cost ceramic disc is recommended. The tolerance of this part has a very minor effect on the output characteristic so any of the standard ±5%, ±10% or ±20% tolerances are acceptable. 330 pF is a good initial value, iterated with R1.

Clamp Resistor – R1

The value of R1 is selected to be the highest value that still provides adequate margin to the DRAIN BV_{DSS} rating at high line. As a general rule, the value of C4 should be minimized and R1 maximized.

CONTROL Pin Capacitor – C5

Capacitor C5 is used during start-up to power LinkSwitch and sets the auto-restart frequency. For designs that have a battery load, this component should have a value of 0.22 µF and for resistive loads a value of 1 µF. This ensures there is sufficient time during start-up for the output voltage to reach regulation. Any capacitor type is acceptable with a voltage rating of 10 V or above.

Bias Capacitor – C3

Capacitor C3 should be a 1 µF, 50 V electrolytic type. The voltage rating is consistent with the 20 V to 30 V seen across the bias winding. Lower values give poorer regulation.

Feedback Resistor – R4

The value of R4 is selected to give a feedback current into the CONTROL pin of approximately 2.15 mA at the peak output power point of the supply. The actual value depends on the bias voltage, typically in the range 20 V to 35 V, selected during design. Higher values for the bias voltage will increase no-load power consumption. Any 1%, 0.25 W resistor is suitable.

Output Diode – D7

PN fast, PN ultra-fast or Schottky diodes can be used depending on the efficiency target for the supply, Schottky diodes giving higher efficiency than PN diodes. The diode voltage rating should be sufficient to withstand the output voltage plus the input voltage transformed through the turns ratio (a typical V_{OR} of 50 V requires a diode PIV of 50 V). Slow recovery diodes are not recommended (1N400X types).

Output Capacitor – C6

Capacitor C6 should be selected such that its voltage and ripple current specifications are not exceeded. Selecting a capacitor with low equivalent series resistance (ESR) will reduce peak-peak output ripple and improve overall supply operating efficiency.

LinkSwitch Layout considerations

Primary Side Connections
The copper area connected to SOURCE should be maximized to minimize temperature rise of the LinkSwitch device.

The CONTROL pin capacitor C5 should be located as close as possible to the SOURCE and CONTROL pins.

To minimize EMI coupling from the switching DRAIN node on the primary to both the secondary and AC input, the LinkSwitch should be positioned away from the secondary of the transformer and AC input.

The length and copper area of all PCB traces connecting to the switching DRAIN node should be kept to an absolute minimum to limit EMI radiation.

Y Capacitor
If a Y capacitor is required, it should be connected close to the transformer secondary output return pin(s) and the primary bulk capacitor positive terminal. Such placement will maximize the EMI benefit of the Y capacitor and avoid problems in common-mode surge testing.

Quick Design Checklist

As with any power supply design, all LinkSwitch designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. Performing the following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 675 V at highest input voltage and peak output power.

2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output power, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. LinkSwitch has a minimum leading edge blanking time of 200 ns to prevent premature termination of the on-cycle. Verify that the leading edge current spike event is below current limit at the end of the 200 ns blanking period.

3. Thermal check – At peak output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for LinkSwitch, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch as specified in the data sheet. Under low line, peak power, a maximum LinkSwitch SOURCE pin temperature of 100 °C is recommended to allow for these variations.

4. Centered output characteristic – Using a transformer with nominal primary inductance and at an input voltage midway between low and high line, verify that the peak power point occurs at ~4% above the desired nominal output current, with the correct output voltage. If this does not occur, then the design should be refined (increase L_P) to ensure the overall tolerance limits are met.

Selecting Between LNK500 and LNK520

The LNK500 and LNK520 differ in the circuit location of the LinkSwitch device. The LNK500 is designed for high-side operation and the LNK520 is designed for low-side operation. The LNK520 can, however, be used in the high-side configuration in certain applications. Refer to Figure 9 and supporting description. Table 2 summarizes the considerations for selecting which device to use.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations Web site: www.power.com.

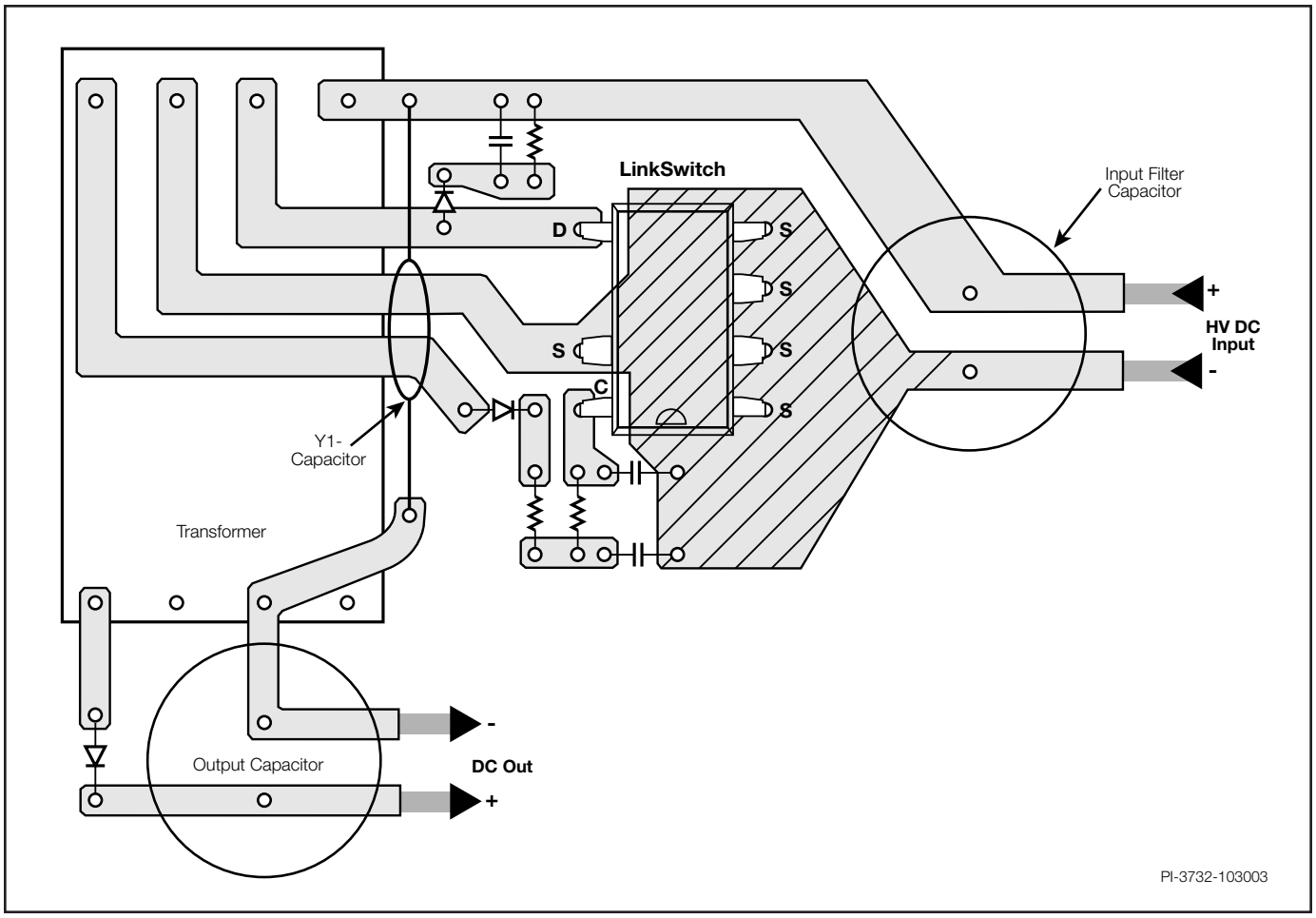


Figure 12. Recommended Circuit Board Layout for LinkSwitch using LNK520.

Family	LNK500	LNK520
Considerations	• Lowest cost CV/CC implementation • Source is connected to the switching node – simple circuit configuration & low component count • Fast switching speeds minimize losses for best efficiency • Source PCB copper heatsink connected to switching node – size should be minimized to limit noise • No bias winding required – simplest circuit configuration • Perfect for linear replacement in applications where additional system EMI shielding or filtering exists	• Very low cost CV/CC implementation • Source connected to quiet low-side primary return - easy layout & low noise (low-side configuration only) • Optimized switching speed – reduces radiated EMI by up to 5 dB (Figure 13) • Source PCB copper heatsink connected to primary return – area can be maximized for higher power without noise (low-side configuration only) • Bias winding required – allows higher V_{OR}, increasing power capability (low-side configuration only) • Perfect for systems where no additional filtering or shielding exists
Summary	The LNK500 is recommended for cost sensitive applications in larger systems with existing EMI filtering (e.g. white goods).	The LNK520 is recommended for both stand-alone charger and adapter applications, and larger systems where EMI reduction is required (e.g. emergency lighting).

Table 2. Comparison of LNK500 and LNK520.

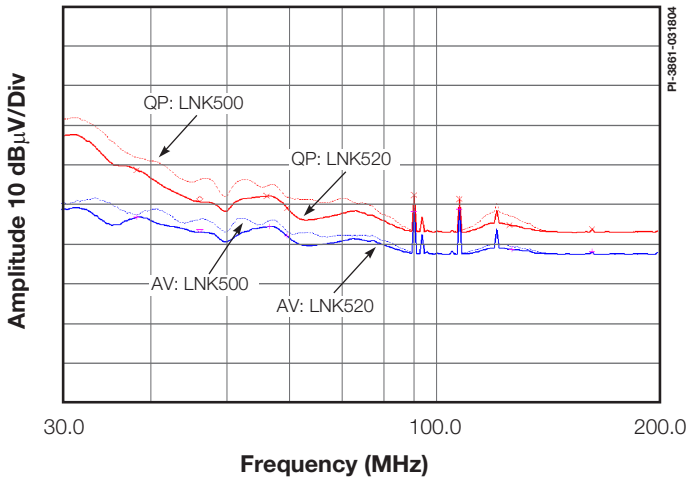


Figure 13. Comparison of LNK520 and LNK500 Showing an Approximate 5 dBµV Reduction in Radiated EMI.

ABSOLUTE MAXIMUM RATINGS(1,4)

DRAIN Voltage ..... -0.3 V to 700 V
DRAIN Peak Current ..... 400 mA
CONTROL Voltage ..... -0.3 V to 9 V
CONTROL Current (not to exceed 9 V) ..... 100 mA
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature(2) ..... -40 °C to 150 °C
Lead Temperature(3) ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

THERMAL IMPEDANCE

Thermal Impedance: P or G Package:
(θ_{JA}) ..... 70 °C/W(2); 60 °C/W(3)
(θ_{JC})(1) ..... 11 °C/W

Notes:
1. Measured on pin 2 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 14 (Unless Otherwise Specified)	Min	Typ	Max	Units
CONTROL FUNCTIONS						
Switching Frequency	f_{OSC}	$I_C = I_{DCT}$, T_J = 25 °C	34.5	42	49.5	kHz
Low Switching Frequency	$f_{OSC(LOW)}$	Duty Cycle = DC_{LF} T_J = 25 °C	24	30	36	kHz
Duty Cycle at Low Switching Frequency	DC_{LF}	Frequency Switching from f_{OSC} to $f_{OSC(LOW)}$, T_J = 25 °C	2.7	4.1	5.5	%
Low Frequency Duty Cycle Range	$DC_{(RANGE)}$	Frequency = $f_{OSC(LOW)}$, T_J = 25 °C	2.0	3.5	5.0	%
Maximum Duty Cycle	DC_{MAX}	I_C = 1.5 mA	74	77	80	%
PWM Gain	DC_{REG}	$I_C = I_{DCT}$, T_J = 25 °C	-0.37	-0.27	-0.17	%/µA
CONTROL Pin Current at 30% Duty Cycle	I_{DCT}	T_J = 25 °C See Figure 4	2.06	2.15	2.25	mA
CONTROL Pin Voltage	$V_{C(IDCT)}$	$I_C = I_{DCT}$	5.5	5.75	6	V
Dynamic Impedance	Z_C	$I_C = I_{DCT}$, T_J = 25 °C	60	90	120	Ω

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 14 (Unless Otherwise Specified)		Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	$I_{C(CH)}$	T_J = 25 °C	V_C = 0 V	-4.5	-3.25	-2	mA
			V_C = 5.15 V	-2.5	-1.8	-1.0	
Control/Supply/ Discharge Current	I_{CD1}	T_J = 25 °C	Output MOSFET Enabled	0.68	0.75	0.82	mA
	I_{CD2}	T_J = 25 °C	Output MOSFET Disabled	0.5	0.6	0.7	
Auto-Restart Threshold Voltage	$V_{C(AR)}$				5.6		V
Auto-Restart Hysteresis Voltage	$V_{C(AR)hyst}$				0.9		V
Auto-Restart Duty Cycle	$DC_{(AR)}$	Short Circuit Applied at Power Supply Output			8		%
Auto-Restart Frequency	$f_{(AR)}$	S2 Open C1 = 0.22 µF (See Figure 14)			300		Hz
CIRCUIT PROTECTION							
Self-Protection Current Limit	I_{LIM}	T_J = 25 °C di/dt = 90 mA/µs See Note B		228	254	280	mA
I^2f Coefficient	I^2f	T_J = 25 °C di/dt = 90 mA/µs See Notes B, C		2412	2710	3008	A^2Hz
Current Limit at Auto-Restart	$I_{LIM(AR)}$	$I_C = I_{CD1}$, T_J = 25 °C			165		mA
Power Up Reset Threshold Voltage	$V_{C(RESET)}$			1.5	2.75	4.0	V
Leading Edge Blanking Time	t_{LEB}	$I_C = I_{DCT}$, T_J = 25 °C		200	300		ns
Current Limit Delay	$t_{iL(D)}$	T_J = 25 °C			100		ns
Thermal Shutdown Temperature		$I_C = I_{DCT}$		125	135		°C
Thermal Shutdown Hysteresis					70		°C

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 14 (Unless Otherwise Specified)		Min	Typ	Max	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 25 mA	T_J = 25 °C		28	32	Ω
			T_J = 100 °C		42	48	
OFF-State Drain Leakage Current	I_{DSS}	V_C = 6.2 V V_D = 560 V, T_A = 125 °C				50	µA
Breakdown Voltage	BV_{DSS}	See Note D V_C = 6.2 V, T_A = 25 °C		700			V
DRAIN Supply Voltage		See Note E		36	50		V

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. I_C is increased gradually to obtain maximum current limit at di/dt of 90 mA/µs. Increasing I_C further would terminate the cycle through duty cycle control.

C. This parameter is normalized to I_{DCT} to correlate to power supply output current (it is multiplied by I_{DCT}(nominal)/I_{DCT}).

D. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

E. It is possible to start up and operate LinkSwitch at DRAIN voltages well below 36 V. However, the CONTROL pin charging current is reduced, which affects start-up time, auto-restart frequency, and auto-restart duty cycle. Refer to the characteristic graph on CONTROL pin charge current (I_C) vs. DRAIN voltage (Figure 16) for low voltage operation characteristics.

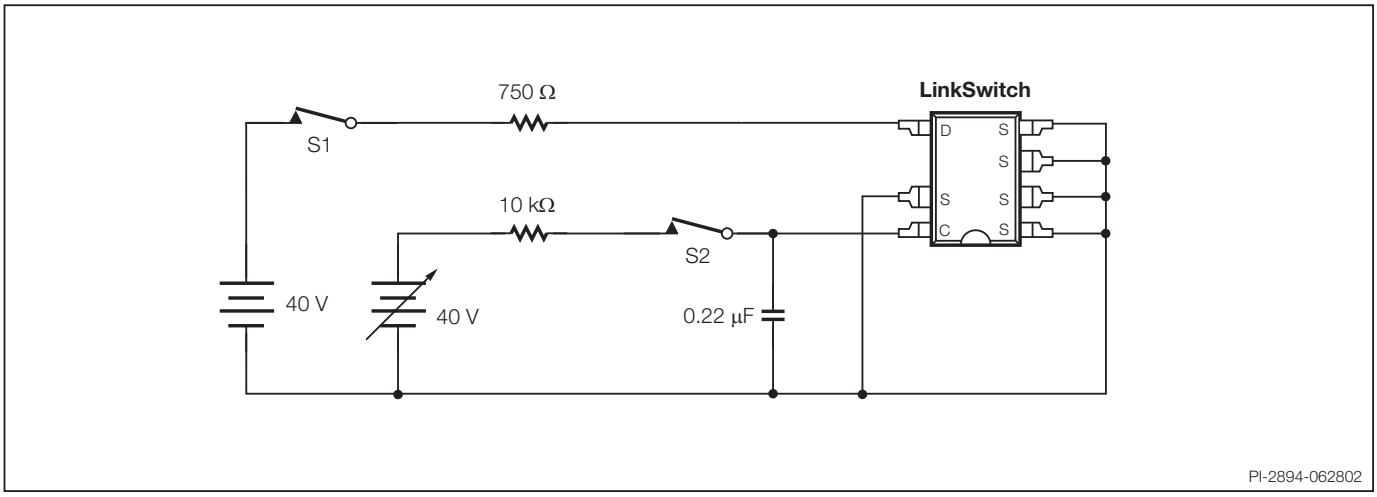


Figure 14. LinkSwitch General Test Circuit.

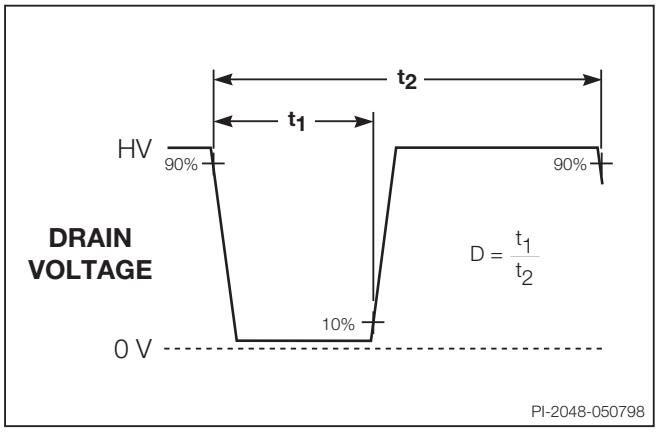


Figure 15. Duty Cycle Measurement.

Typical Performance Characteristics

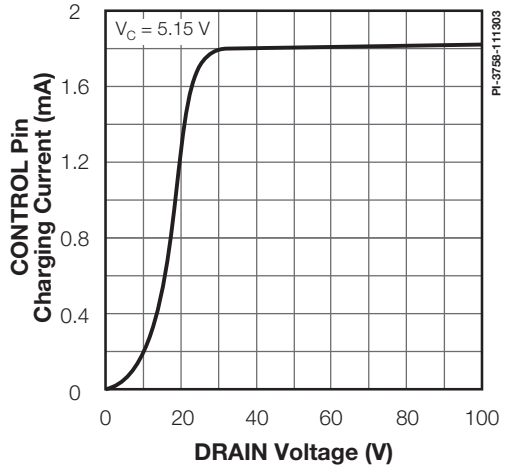


Figure 16. I_C vs. DRAIN Voltage.

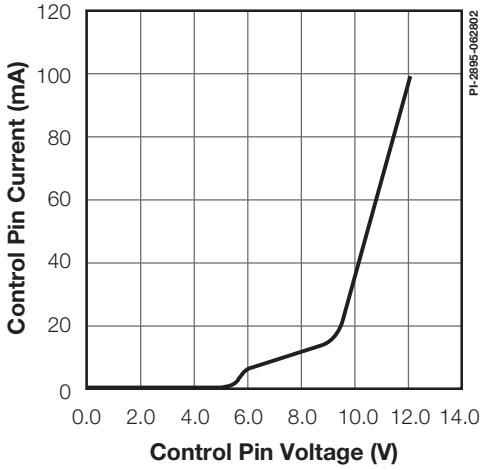


Figure 17. CONTROL Pin I-V Characteristic.

Typical Performance Characteristics (cont.)

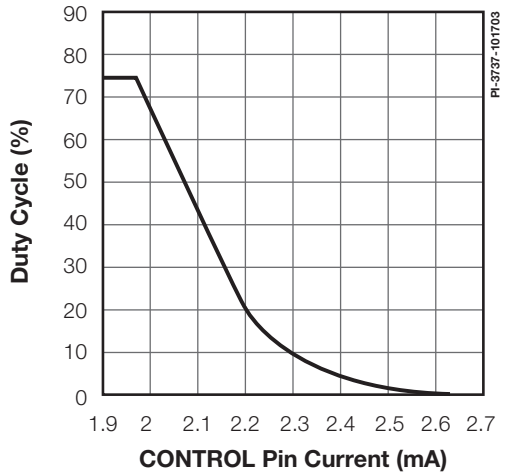


Figure 18. Duty Cycle vs. CONTROL Pin Current.

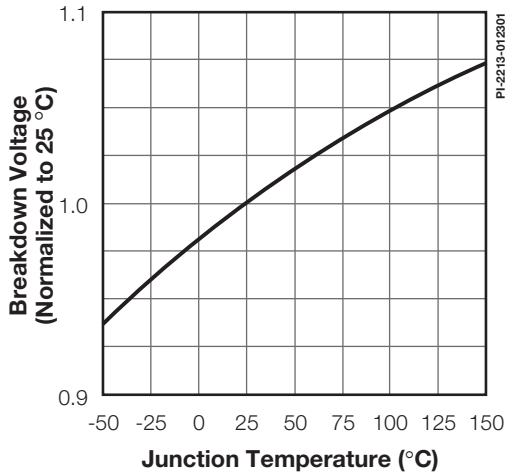


Figure 19. Breakdown Voltage vs. Temperature.

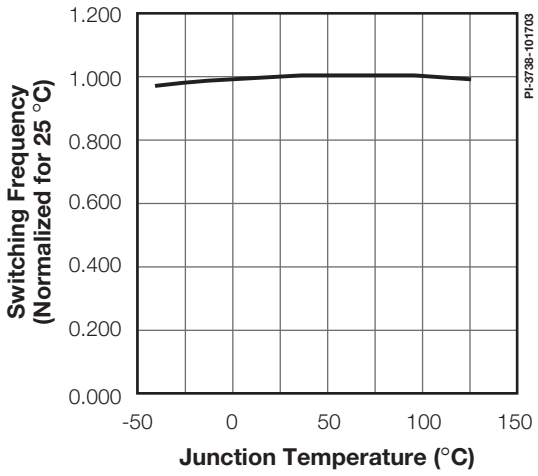


Figure 20. Switching Frequency vs. Temperature.

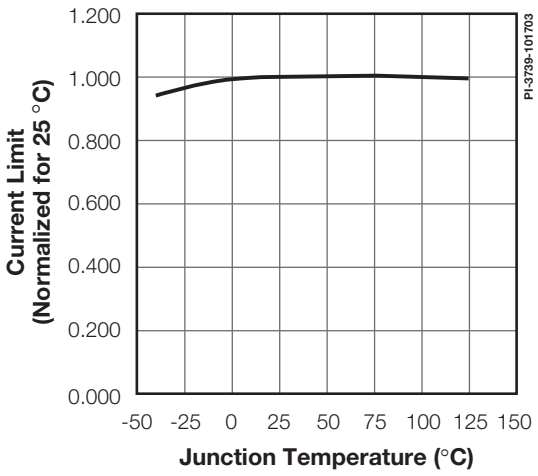


Figure 21. Current Limit vs. Temperature.

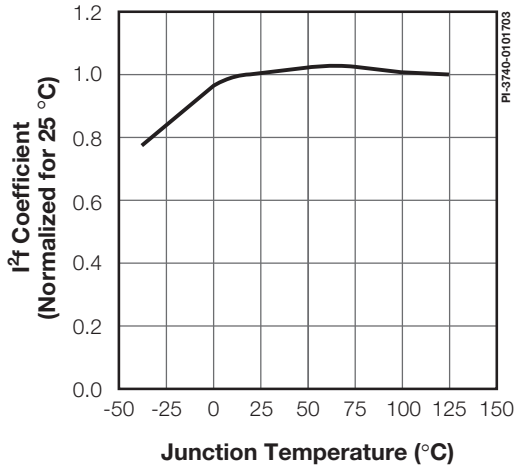


Figure 22. I^2f Coefficient vs. Temperature.

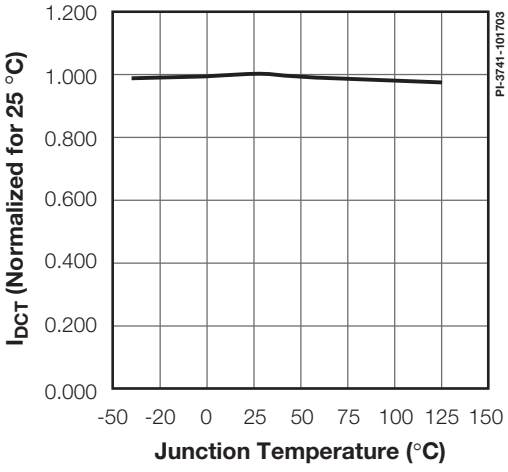


Figure 23. I_{DCT} vs. Temperature.

Typical Performance Characteristics (cont.)

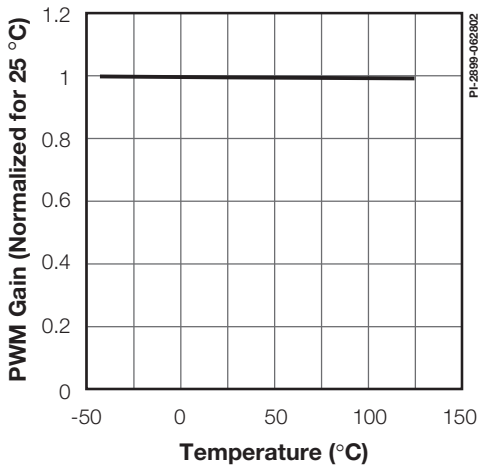


Figure 24. PWM Gain vs. Temperature.

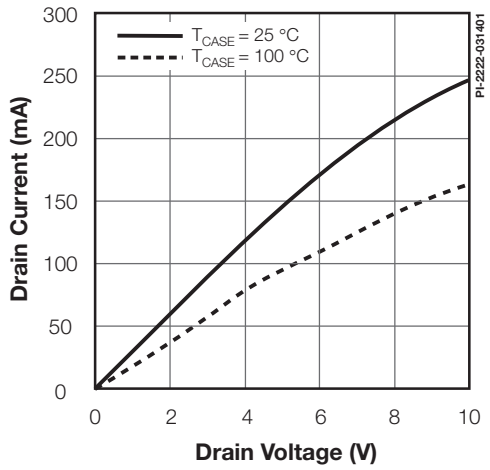
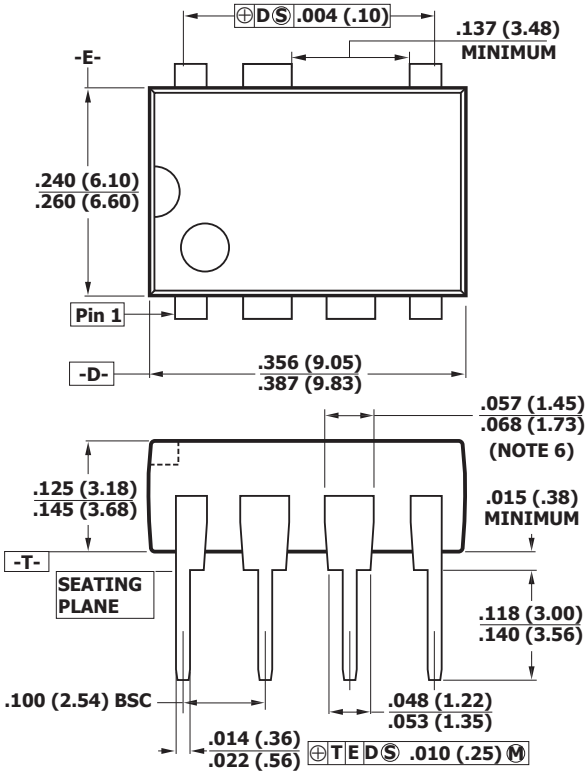


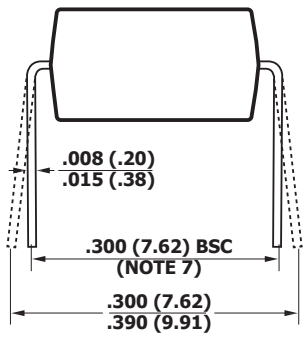
Figure 25. Output Characteristics (DRAIN Current vs. DRAIN Voltage.

PDIP-8B (P Package)



Notes:

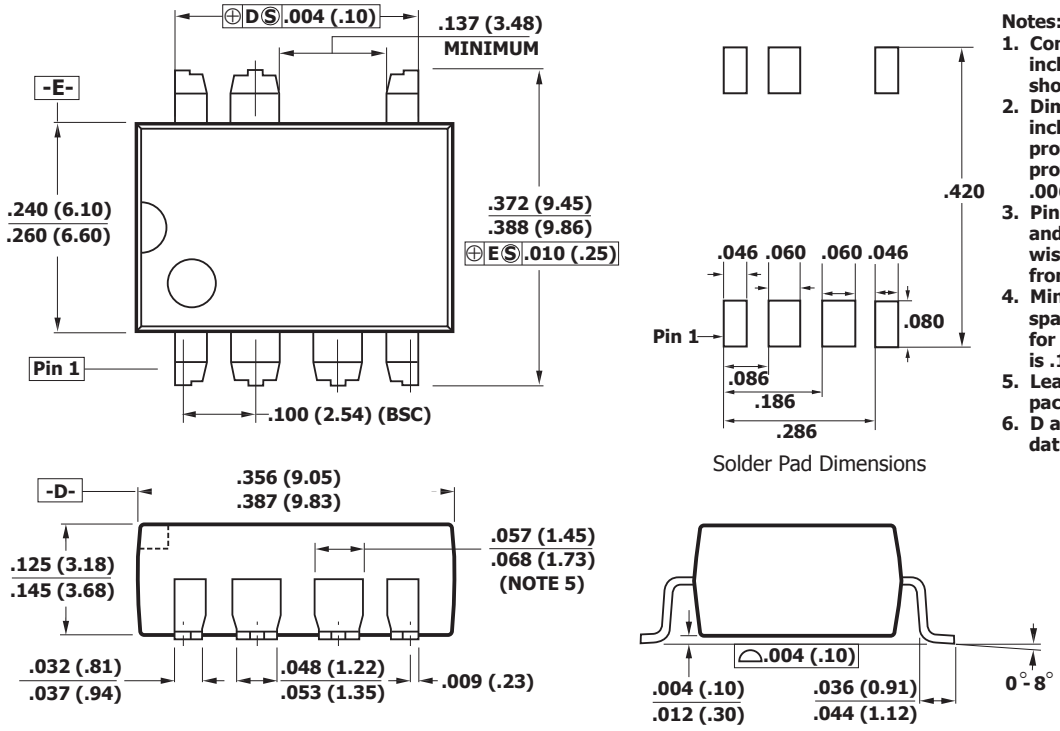
1. **Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.**
2. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
4. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 6 is omitted.**
5. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
6. **Lead width measured at package body.**
7. **Lead spacing measured with the leads constrained to be perpendicular to plane T.**



P08B

PI-2551-081716

SMD-8B (G Package)



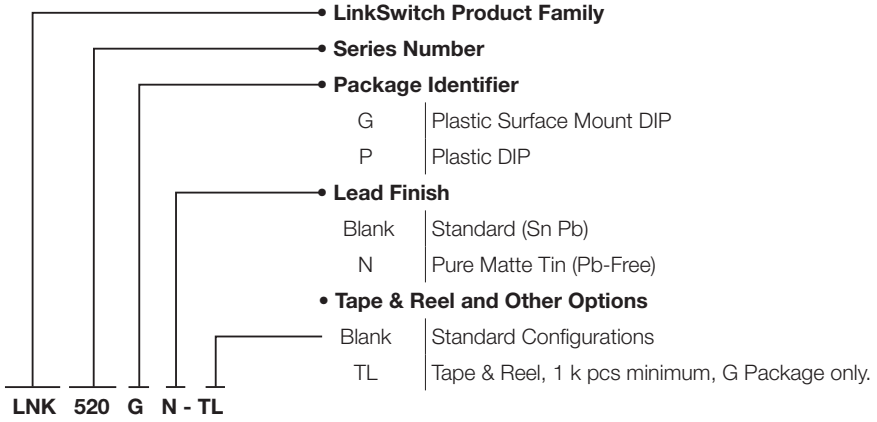
Notes:

1. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
2. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
3. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 6 is omitted.**
4. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
5. **Lead width measured at package body.**
6. **D and E are referenced datums on the package body.**

G08B

PI-2546-081716

Part Ordering Information



Revision	Notes	Date
C	Released Final Data Sheet.	3/04
D	Added lead-free ordering information.	12/04
E	Minor descriptive change and formatting correction.	2/05
F	Updated PDIP-8B (P Package) and SMD-8B (G Package) per PCN-16232.	09/16

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