LNK574/576
LinkZero-LP

Zero No-Load or Zero Standby Consumption
with up to 1 mW Output Load

Product Highlights

Lowest System Cost with Zero Standby (1 mW Output Power)

- Automatically enters low consumption power-down mode when load drops below ~0.2% of full load for LNK576 and ~0.6% for LNK574
- Detects load reconnection and automatically restarts regulation
- Simple upgrade to existing LinkSwitch-LP designs
- Very accurate IC parameter tolerances improve system manufacturing yield
- Suitable for low-cost clampless designs
- Frequency jittering greatly reduces EMI filter cost
- Extended package creepage improves system field reliability

Advanced Protection/Safety Features

- Accurate hysteretic thermal shutdown protection – automatic recovery reduces field returns
- Universal input range allows worldwide operation
- Auto-restart reduces delivered power by >85% during short-circuit and open-loop fault conditions
- Simple ON/OFF control, no loop compensation needed
- High bandwidth provides excellent transient load response with no overshoot

EcoSmart™– Energy Efficient

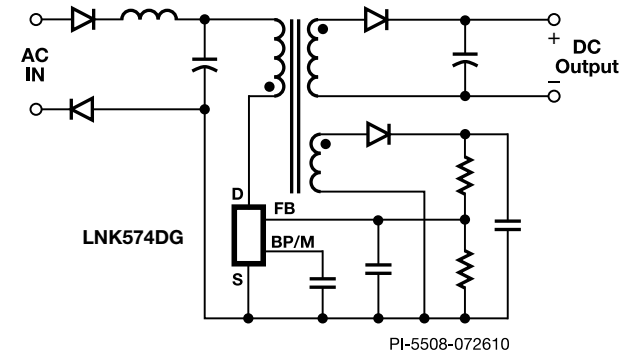
- No-load or standby (1 mW output power) consumption as low as <5 mW at 230 VAC input (Note 1)
- Easily meets all global energy efficiency regulations with no added components
- ON/OFF control provides constant efficiency to very light loads

Applications

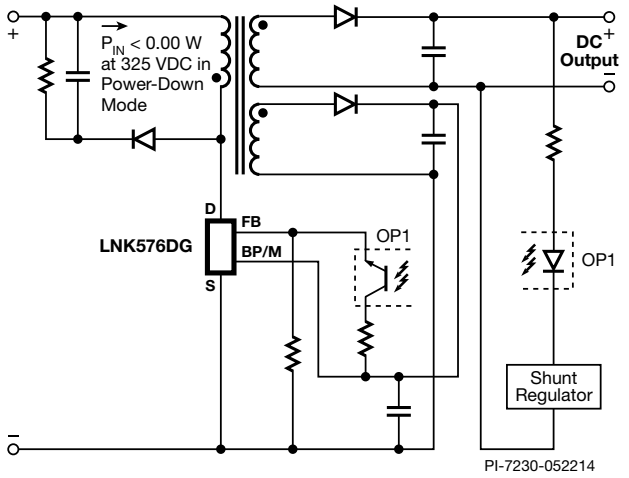
- Chargers for cell/cordless phones, PDAs, power tools, MP3/portable audio devices, shavers, etc.
- Standby power supply for TV, video displays, and appliances

Description

The LinkZero™-LP controller incorporates new technology which enables the device to automatically enter into and wake up from no-load mode or with 1 mW load while taking less than 5 mW from the AC power. IEC 62301 specifies measurements of standby power to a minimum accuracy of 10 mW, and so LinkZero-LP's consumption of substantially less than 5 mW at 230 VAC rounds to zero based on the IEC definition. This low power level is also immeasurable on most power meters. The accurately specified FEEDBACK (FB) pin voltage reference enables universal input primary-side regulated power supplies with accurate constant voltage from 5% to full load. The start-up and operating power are derived directly from the DRAIN pin which eliminates start-up circuitry. The internal oscillator frequency is jittered to significantly reduce both quasi-peak and average EMI, minimizing filter cost.



(a) Typical Application Schematic for LNK574DG.



(b) Typical Application Schematic for LNK576DG.

Figure 1. Typical Applications – Zero No-Load Charger (a) and Zero Standby Power Supply (b).

Output Power Table[1]

Product[4]	230 VAC ±15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
LNK574DG	3 W	3 W	3 W	3 W
LNK576DG	6 W	9 W	5 W	8 W

Table 1. Output Power Table.

Notes:
1. IEC 62301 Clause 4.5 rounds standby power use below 5 mW to zero.
2. Typical continuous power in a non-ventilated enclosed adapter measured at +50 °C ambient.
3. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient.
4. Packages: D: SO-8C.

This Product is Covered by Patents and/or Pending Patent Applications.

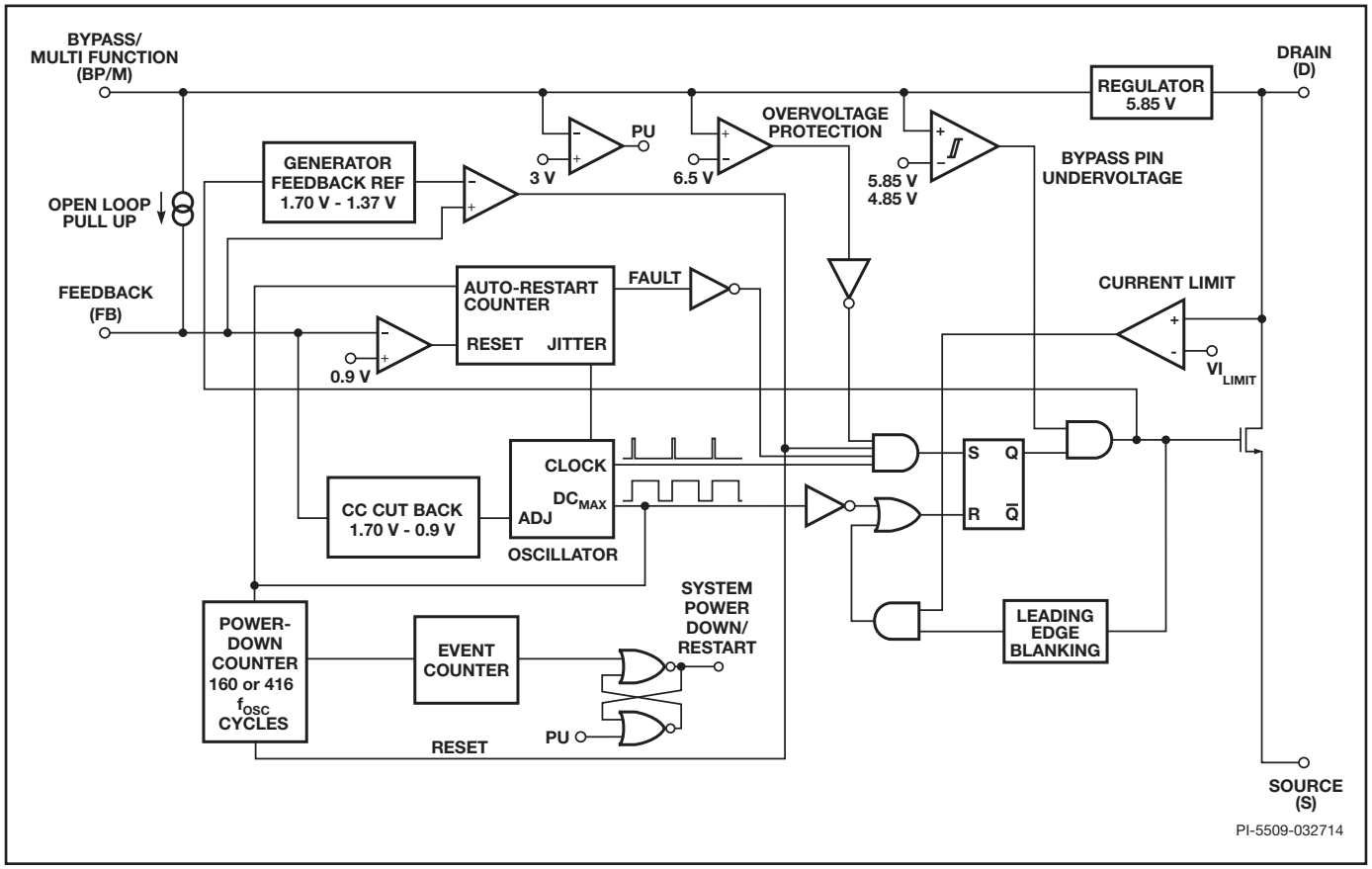


Figure 2 Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
The power MOSFET drain connection provides internal operating current for both startup and steady-state operation.

BYPASS/MULTI-FUNCTIONAL PROGRAMMABLE (BP/M) Pin:
An external bypass capacitor for the internally generated 5.85 V supply is connected to this pin. The value of capacitor establishes the power-down period. The minimum value of capacitor is 0.1 μF. An overvoltage protection disables the switching if the current into the pin exceeds 6.5 mA (I_{SD}).

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is disabled when a voltage greater than an internal V_{FB} reference voltage is applied to the FEEDBACK pin.

The V_{FB} reference voltage is internally adjusted from 1.70 V at full load to 1.37 V at no-load in CV mode, and 1.70 V to 0.9 V in CC mode. Below 0.9 V the part enters auto-restart operation.

SOURCE (S) Pin:
This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

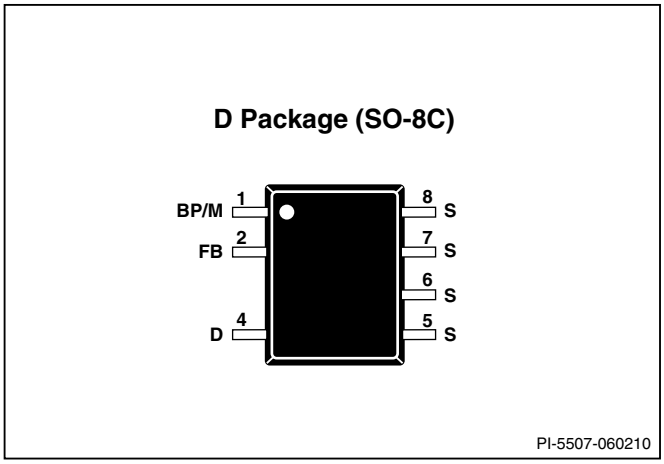


Figure 3. Pin Configuration.

LinkZero-LP Functional Description

LinkZero-LP comprises a 700 V power MOSFET switch with a power supply controller on the same die. Unlike conventional PWM (pulse width modulation) controllers, it uses a simple ON/OFF control to regulate the output voltage. The controller consists of an oscillator, feedback (sense), 5.85 V regulator, BYPASS pin under/overvoltage protection, over-temperature protection, frequency jittering, current limit, leading edge blanking, BYPASS pin clamp during operation in power-down and bypass modes. The controller includes a proprietary power- down mode that automatically reduces standby consumption to levels that are immeasurable on most power meters.

Power-Down Mode
The device enters into power-down mode (where MOSFET switching is disabled) when the total load (power supply output plus bias winding loads) has reduced to ~0.6% for LNK574 or ~0.2% for LNK576 of full load. The internal controller detects this condition by sensing when 160 or 416 cycles have been skipped twice with only one active switching cycle in between the two sets of 160 for LNK574 or 416 for LNK576 skipped switching cycles. During the power-down period the BYPASS pin capacitor will discharge from 5.85 V down to about 3 V at which point the LinkZero-LP will wake up and charge the BYPASS pin back up to 5.85 V. The wake up frequency is determined by the user through the choice of the BYPASS pin capacitor value (see Figure 22 for reference). Once the BYPASS pin has recharged to 5.85 V, LinkZero-LP senses if the load condition has changed or not, if not the LinkZero-LP will enter into a new power-down cycle or otherwise resumes normal operation (See Applications Example section for more details of power-down mode operation).

Oscillator
The typical oscillator frequency is internally set to an average of 100 kHz. An internal circuit senses the on-time of the MOSFET switch and adjusts the oscillator frequency so that at large duty cycle (low-line voltage) the frequency is about 100 kHz and at small duty cycle (high-line voltage) the oscillator frequency is about 78 kHz. This internal frequency adjustment is used to make the peak power point constant over line voltage. Two signals are generated from the oscillator: the maximum duty cycle signal (DC_{MAX}) and the clock signal that indicates the beginning of a switching cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 6% of the switching frequency, to minimize EMI. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter, which is proportional to the oscillator frequency, should be measured with the oscilloscope triggered at the falling edge of the drain voltage waveform. The oscillator frequency is linearly reduced when the FEEDBACK pin voltage is lowered from 1.70 V down to 1.37 V.

Feedback Input Circuit CV Mode
The feedback input circuit reference is set at 1.70 V at full load and gradually reduces down to 1.37 V at no-load. When the FEEDBACK pin voltage reaches a V_{FB} reference voltage (1.70 V to 1.37 V) depending on the load, a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the FEEDBACK pin voltage during the remainder of the cycle are ignored.

Feedback Input CC Mode
When the FEEDBACK pin voltage at full load falls below 1.70 V, the oscillator frequency linearly reduces to typically 43% at the auto-restart threshold voltage of 0.9 V. This function limits the power supply output power at output voltages below the rated voltage regulation threshold V_R.

5.85 V Regulator
The BYPASS pin voltage is regulated by drawing a current from the DRAIN whenever the MOSFET is off if needed to charge up the BYPASS pin to a typical voltage of 5.85 V. When the MOSFET is on, LinkZero-LP runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows LinkZero-LP to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage.

6.5 V Shunt Regulator and 8.5 V Clamp
In addition, there is a shunt regulator that helps maintain the BYPASS pin at 6.5 V when current is provided to the BYPASS pin externally. This facilitates powering the device externally through a resistor from the bias winding or power supply output in non-isolated designs, to decrease device dissipation and increase power supply efficiency.

The 6.5 V shunt regulator is only active in normal operation, and when in power-down mode a clamp at a higher voltage (typical 8.5 V) will clamp the BYPASS pin.

BYPASS Pin Undervoltage Protection
The BYPASS pin undervoltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.85 V. Once the BYPASS pin voltage drops below 4.85 V, it must rise back to 5.85 V to enable (turn on) the power MOSFET.

BYPASS Pin Overvoltage Protection
If the BYPASS pin gets pulled above 6.5 V (BP_{SHUNT})and the current into the shunt exceeds 6.5 mA a latch will be set and the power MOSFET will stop switching. To reset the latch the BYPASS pin has to be pulled down to below 1.5 V.

Over-Temperature Protection
The thermal shutdown circuit senses the die temperature. The threshold is set at 142 °C typical with a 70 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 70 °C, at which point the MOSFET is re-enabled.

Current Limit
The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remaining of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction.

Auto-Restart
In the event of a fault condition such as output short-circuit, LinkZero-LP enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FEEDBACK pin voltage exceeds the FEEDBACK pin auto-restart threshold voltage ($V_{FB(AR)}$ typical 0.9 V). If the FEEDBACK pin voltage drops below $V_{FB(AR)}$ for more than 145 ms to 170 ms depending on the line voltage, the power MOSFET switching is disabled. The auto-restart alternately enables and disables the switching of the power MOSFET at a duty cycle of typically 12% until the fault condition is removed.

A resistor lower than 50 kΩ in value should always be connected from FEEDBACK pin to SOURCE pin. For resistor values >50 kΩ, device operation is not guaranteed. If for any reason the FEEDBACK pin is floated, the IC will stop switching.

Open-Loop Condition on the FEEDBACK Pin

When an open-loop condition on the FEEDBACK pin is detected, an internal pull up current source pulls the FEEDBACK pin up to above 1.70 V and LinkZero-LP stops switching after 160 clock cycles for LNK574 or 416 clock cycles for LNK576.

Applications Example

The circuit shown in Figure 4 is a typical isolated zero no-load 6 V, 350 mA, constant voltage, and constant current (CV/CC) output power supply using LinkZero-LP.

AC input differential filtering is accomplished by the π filter formed by C1, C2 and L1. The proprietary frequency jitter feature of the LinkZero-LP eliminates the need for any Y capacitor or common-mode inductor. Wire-wound resistor RF1 is a fusible, flame proof resistor which is used as a fuse as well as to limit inrush current. Wire-wound types are recommended for designs that operate ≥132 VAC to withstand the instantaneous power when AC is first applied as C1 and C2 charge.

The power supply utilizes simplified bias winding voltage feedback, enabled by the LinkZero-LP ON/OFF control. The voltage across C5 is determined by the FEEDBACK pin reference voltage and the resistor divider formed by R3 and R4. Capacitor C4 provides high frequency filtering on the FEEDBACK pin to avoid switching cycle pulse bunching. The FEEDBACK pin reference voltage, which varies with load, is set to 1.37 V at no-load and gradually increases to 1.70 V at full load to provide cable drop compensation. In the constant voltage (CV) region, the LinkZero-LP device enables/disables switching cycles to maintain the FEEDBACK pin reference voltage. Diode D6 and low cost ceramic capacitor C5 provide rectification and filtering of the primary feedback winding waveform. At increased loads, beyond the maximum power threshold, the IC transitions into the constant current (CC) region. In this region, the FEEDBACK pin voltage begins to reduce as the power supply output voltage falls. In order to maintain a constant output current, the internal oscillator frequency is reduced in this region until it reaches typically 48% of the starting frequency. When the FEEDBACK pin voltage drops below the auto-restart threshold (typically 0.9 V on the FEEDBACK pin), the power supply enters the auto-restart mode. In this mode, the power supply will turn off for 1.2 s and then turn back on for 170 ms. The auto-restart function reduces the average output current during an output short-circuit condition.

The LinkZero-LP device is self biased through the DRAIN pin. However, to improve efficiency at high-line, an external bias may be added using optional components diode D5 and resistor R2. The power-down (PD) mode duty cycle and the no-load power consumption is determined by the BYPASS pin capacitor C3. No-load power consumption can be reduced by a capacitor with higher value. Higher C3 capacitor values will tend to increase the output ripple in PD mode – See LinkZero-LP Design Considerations section below.

A clampless primary circuit is achieved due to the very accurate tolerance current limit trimming techniques used in manufacturing the LinkZero-LP, plus the transformer construction techniques used. The peak drain voltage is therefore limited to typically less than 550 V at 265 VAC, providing significant margin to the 700 V minimum drain voltage specification (BV_{DSS}).

Output rectification and filtering is achieved with output rectifier D7 and filter capacitor C7. Due to the auto-restart feature, the average short-circuit output current is significantly less than 1 A, allowing low current rating and low cost rectifier D7 to be used. Output circuitry is designed to handle a continuous short-circuit on the power supply output. Although not necessary in this design, a preload resistor may be used at the output of the supply to reduce output voltage at no-load.

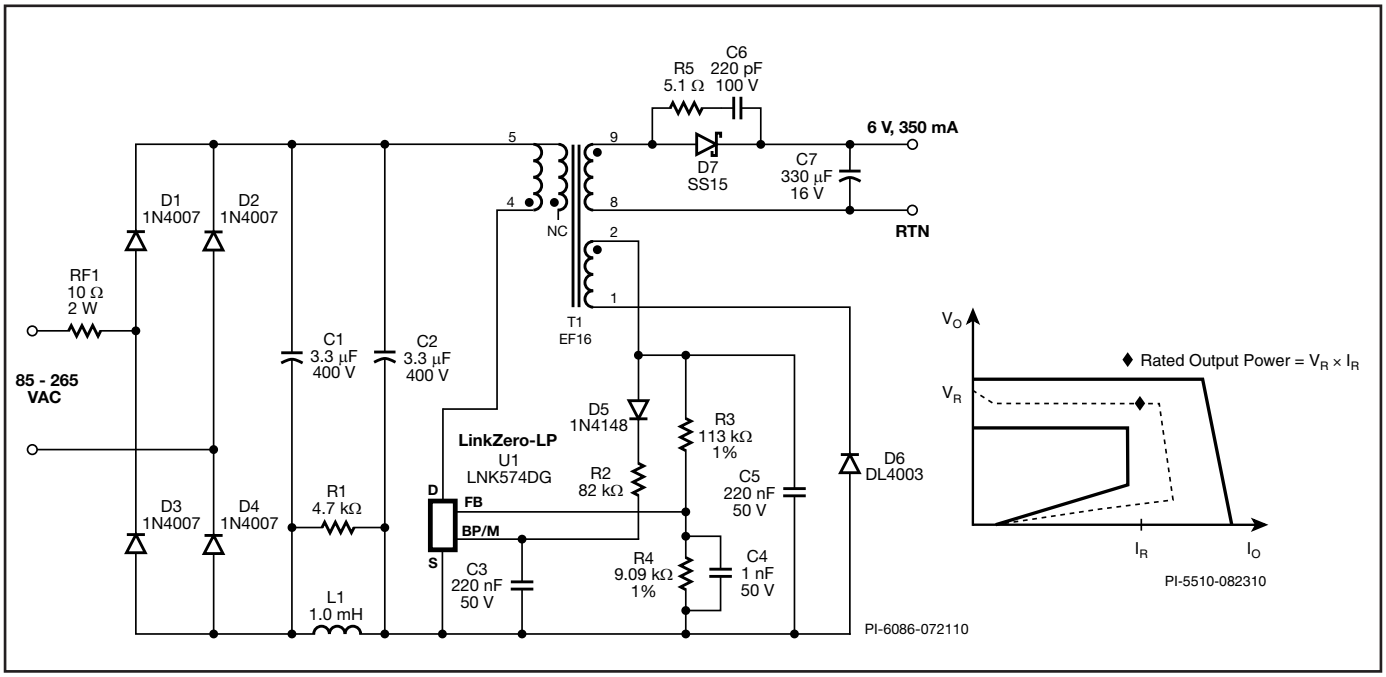


Figure 4. Schematic of 2.1 W, 6 V, 350 mA, 0.00 W Adapter/Charger.

LinkZero-LP Power-Down (PD) Mode Design Considerations

The LinkZero-LP goes into PD mode when the output power supply load is reduced enough that 160 for LNK574 or 416 for LNK576 consecutive switching cycles are skipped twice with only one active switching cycle in between the two sets of 160 for LNK574 or 416 for LNK576 skipped switching cycles. This corresponds to ~0.6% for LNK574 or ~0.2% for LNK576 of the full load power capability of the LinkZero-LP.

Even when the power supply output load is completely removed, any preload resistor on the output and the components connected to the bias winding still represent a load on the transformer. The feedback circuitry connected to the bias winding should therefore be designed to represent <0.6% for LNK574 or <0.2% for LNK576 of the power supply full load. Otherwise LinkZero-LP will not be able to detect a no-load condition on the output and will not enter PD mode thereby disabling the benefit of zero no-load input power.

In the case of the design of Figure 4, the power supply full load output power is 2.1 W (6 V, 350 mA). The bias winding load should therefore be designed to be <<0.6% of this (<12.6 mW). In the example of Figure 4, the average no-load voltage across bias winding capacitor C5 is approximately 20 V. The loading of R3, R4 and R2 (if used) should therefore be chosen to present <12.6 mW load with this bias voltage. In the case shown, the R2 path consumes ~3.3 mW and R3 and R4 also consumes ~3.3 mW. So the total consumption of 6.6 mW meets the criteria necessary to ensure the power supply will enter PD mode when the power supply load is removed. Adjusting the power consumption of the circuitry connected to the bias winding can therefore be used to adjust the power supply output power threshold at which the LinkZero-LP goes into PD mode.

It can be seen therefore that, if desired, PD mode can be avoided altogether simply by adding a preload resistor on the output of the power supply or increasing the load on the bias winding to >0.6% (plus margin) of the power supply maximum power capability for LNK574 or >0.2% for LNK576.

When the LinkZero-LP is in PD mode, the time taken for the BYPASS pin voltage to discharge to $V_{BPPDRESET}$ (~3 V) determines the duration of the PD off-time. The duration of the PD off-time also determines the ripple on the output voltage.

If components D5 and R2 are not used in Figure 4, this time is determined purely by the choice of C3. If however D5 and R2 are used to provide an external BYPASS pin supply, then a combination of the energy stored in C5 and C3 determine the PD off-time before the BYPASS pin voltage reaches the $V_{BP(PU)}$ (~3 V).

In either case, C5 is completely discharged through R3 and R4 during the PD off-time (D5 prevents the BYPASS capacitor C3 being discharged through this path). C5 is therefore kept as small as possible to reduce the power supply no-load input power consumption associated with recharging this capacitor at the start of the next PD on-time. The minimum value of C5 is determined by the time constant set up with the feedback resistors R3 and R4 to avoid excessive cycle by cycle ripple on C5 influencing the output voltage regulation. The typical choice for C5 is between 100 nF and 330 nF.

When D5 and R2 are used, the minimum value of bias winding capacitor C5 is again governed by voltage regulation performance so the value of BYPASS pin capacitor C3 is typically reduced to reduce PD off-time period if required. A minimum C3 value of 47 nF is recommended.

PCB Layout Considerations

LinkZero-LP Layout Considerations

Layout
See Figure 5 for a recommended circuit board layout for LinkZero-LP (U1).

Single Point Grounding
Use a single point ground (Kelvin) connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitor (C_{BP}), FEEDBACK Pin Noise Filter Capacitor (C_{FB}) and Feedback Resistors
To minimize loop area, these two capacitors should be physically located as near as possible to the BYPASS and SOURCE pins, and FEEDBACK pin and SOURCE pins respectively. Also note that to minimize noise pickup, feedback resistors R_{FB1} and R_{FB2} are placed close to the FEEDBACK pin.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and LinkZero-LP should be kept as small as possible.

Primary Clamp Circuit
An external clamp may be used to limit peak voltage on the DRAIN pin at turn off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and LinkZero-LP (U1).

Thermal Considerations
The copper area underneath the LinkZero-LP (U1) acts not only as a single point ground, but also as a heat sink. As it is connected to the quiet source node, this area should be maximized for good heat sinking of U1. The same applies to the cathode of the output diode.

Y Capacitor
The placement of the Y-type capacitor (if used) should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common-mode surge currents away from U1. Note: If an input π EMI filter is used, the inductor in the π filter should be placed between the negative terminals on the input filter capacitors.

Output Diode (D_O)
For best performance, the area of the loop connecting the secondary winding, the output diode (D_O) and the output filter capacitor (C_O) should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heat sinking. A larger area is preferred at the electrically "quiet" cathode terminal. A large anode area can increase high frequency conducted and radiated EMI. Resistor R_S and C_S represent the secondary side RC snubber.

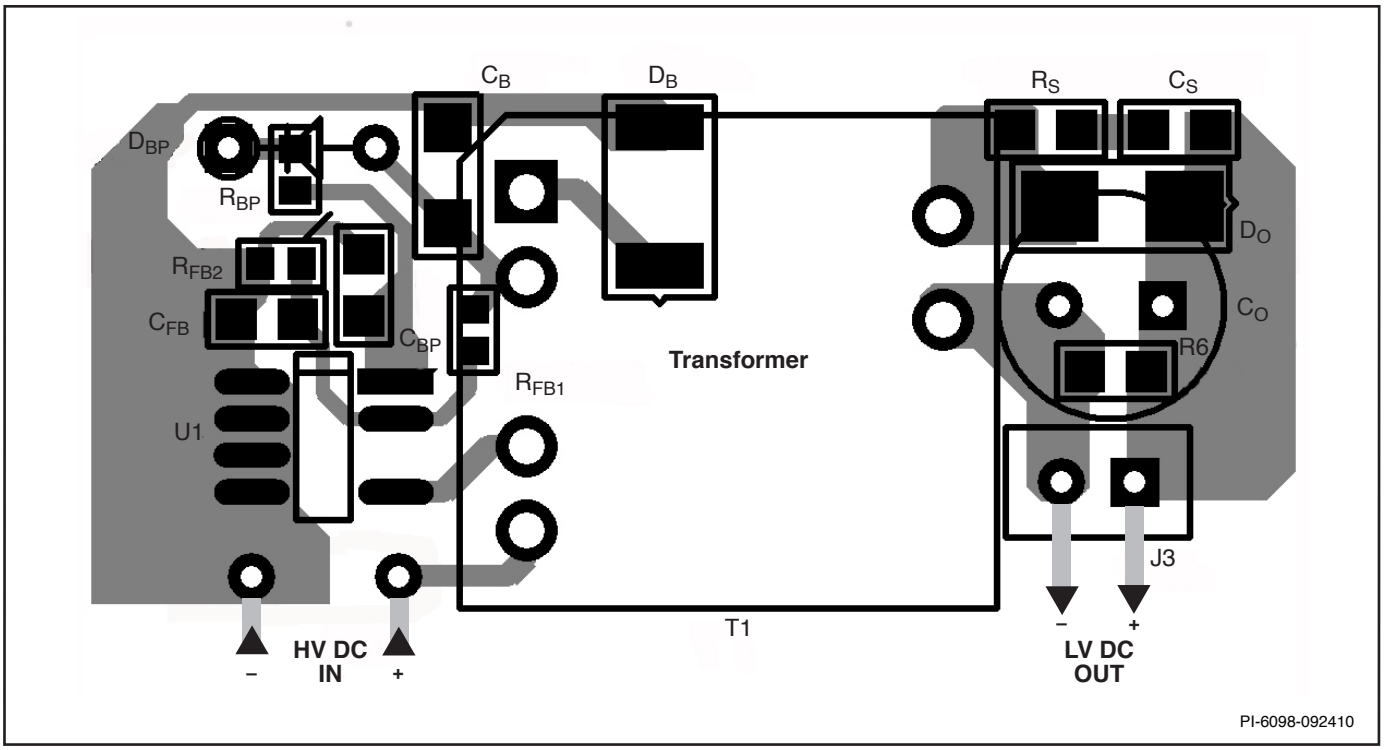


Figure 5. PCB Layout of a 2.1 W, 6 V, 350 mA Charger.

Quick Design Checklist

As with any power supply design, all LinkZero-LP designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 660 V at the highest input voltage and peak (overload) output power. This margin to the 700 V BV_{DSS} specification gives margin for design variation, especially in clampless designs.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading-edge current spikes at startup. Repeat under steady state conditions and verify that the leading-edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for LinkZero-LP, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkZero-LP as specified in the data sheet. Under low-line and maximum power, maximum LinkZero-LP source pin temperature of 100 °C is recommended to allow for these variations.
4. Negative drain voltages – Clampless designs may allow the drain voltage to ring below source and cause reverse currents to flow from source to drain. Verify that any such current remains within the envelope shown in Figure 9.

Absolute Maximum Ratings[1,6]

DRAIN Voltage .....-0.3 V to 700 V
Peak DRAIN Current LNK574 ..... 200 (375) mA[2]
LNK576 ..... 440 (825) mA[2]
Peak Negative Pulsed Drain Current ..... -100 mA[3]
Feedback Voltage ..... -0.3 V to 9 V
Feedback Current .....100 mA
BYPASS Pin Voltage ..... -0.3 V to 9 V
BYPASS Pin Voltage in Power-Down Mode.....-0.3 V to 11 V[7]
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature.....-40 °C to 150 °C[4]
Lead Temperature ..... 260 °C[5]

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Higher peak DRAIN current allowed while DRAIN source voltage does not exceed 400 V.
3. Duration not to exceed 2 μs.
4. Normally limited by internal circuitry.
5. 1/16 in. from case for 5 seconds.
6. Maximum ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum ratings for extended periods of time may affect product reliability.
7. Maximum current into pin is 300 μA.

Thermal Resistance

Thermal Resistance: D Package:
(θ_{JA}) .....100 °C/W[2]; 80 °C/W[3]
(θ_{JC}) .....30 °C/W[1]

Notes:
1. Measured on the SOURCE pin close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm²), 2 oz. copper clad.
3. Soldered to 1 sq. in. (645 mm²), 2 oz. copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
Output Frequency	f_{OSC}	T_J = 25 °C V_{FB} = 1.70 V, See Note C	93	100	107	kHz
Frequency Jitter		Peak-Peak Jitter Compared to Average Frequency, T_J = 25 °C		±3		%
Ratio of Output Frequency at Auto-Restart to f_{osc}	$\frac{f_{OSC(AR)}}{f_{OSC}}$	T_J = 25 °C V_{FB} = $V_{FB(AR)}$ See Note B		43		%
Maximum Duty Cycle	DC_{MAX}		60	63		%
FEEDBACK Pin Voltage at no Skipped Cycles	V_{FB}		1.63	1.70	1.77	V
FEEDBACK Pin Voltage at 99.4% Skipped Cycles	$V_{FB(NL)}$			1.37		V
FEEDBACK Pin Voltage at Auto-Restart	$V_{FB(AR)}$		0.8	0.9	1.05	V
Minimum Switch ON-Time	$t_{ON(MIN)}$			700		ns

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
DRAIN Supply Current	I_{S1}	Feedback Voltage > V_{FB} (MOSFET not Switching)		150	200	260	µA
	I_{S2}	0.9 V ≤ V_{FB} ≤ 1.70 V (MOSFET Switching)	LNK574	200	260	310	
			LNK576	230	285	340	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C	LNK574	-5.5	-3.8	-1.8	mA
			LNK576	-7.0	-5.3	-3.3	
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C	LNK574	-3.8	-2.5	-1.0	
			LNK576	-4.8	-3.5	-2.0	
BYPASS Pin Voltage	V_{BP}			5.60	5.85	6.10	V
BYPASS Pin Voltage Hysteresis	$V_{BP(H)}$			0.8	1.0	1.2	V
BYPASS Pin Shunt Voltage	BP_{SHUNT}			6.1	6.5	6.9	V
Circuit Protection							
Current Limit	I_{LIMIT}	di/dt = 40 mA/µs T_J = 25 °C	LNK574	126	136	146	mA
		di/dt = 100 mA/µs T_J = 25 °C	LNK576	325	350	375	
Power Coefficient	I^2f	di/dt = 40 mA/µs T_J = 25 °C	LNK574	1665	1850	2091	A^2Hz
		di/dt = 100 mA/µs T_J = 25 °C	LNK576	10562	12250	14062	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C		220	265		ns
BYPASS Pin Shutdown Threshold Current	I_{SD}	V_{BP} = BP_{SHUNT} See Note E		5.0	6.5	8.0	mA
Thermal Shutdown Temperature	T_{SD}	See Note B		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note B			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Power-Down (PD) Mode							
Off-State Drain Leakage in Power-Down Mode	$I_{DSS(PD)}$	T_J = 25 °C V_{DRAIN} = 325 V See Figure 25			6.5	9	µA
BYPASS Pin Overvoltage Protection in Power-Down Mode	$V_{BP(PDP)}$	I_{BP} = 300 µA T_J ≤ 100 °C		7.25	8.5	10.9	V
BYPASS Pin Power-Up Reset Threshold (in Power-Down Mode or at Power Supply Start-Up)	$V_{BP(PU)}$			1.5	3	4	V
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK574 I_D = 13 mA	T_J = 25 °C		48	55	Ω
			T_J = 100 °C		76	88	
		LNK576 I_D = 33 mA	T_J = 25 °C		19	22	
			T_J = 100 °C		30	35	
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, T_J = 25 °C		700			V
DRAIN Supply Voltage				50			V
Auto-Restart ON-Time	t_{AR}	V_{IN} = 85 VAC T_J = 25 °C See Note C			145		ms
Auto-Restart Duty Cycle					1.0		s
Output Enable Delay	t_{EN}	See Figure 8				14	µs

NOTES:

A. I_{DSS} is the worse case off-state leakage specification at 80% of BV_{DSS} and maximum operating junction temperature.

B. This parameter is derived from characterization.

C. Output frequency specification applies to low-line input voltage in the final application. The controller is designed to reduce output frequency by approximately 20% at high-line input voltages to balance low-line and high-line maximum output power.

D. The auto-restart on-time/off-time is increased by 20% at high-line input 265 VAC.

E. LinkZero-LP shuts down if current into BYPASS pin reaches I_{SD} at BP_{SHUNT} voltage.

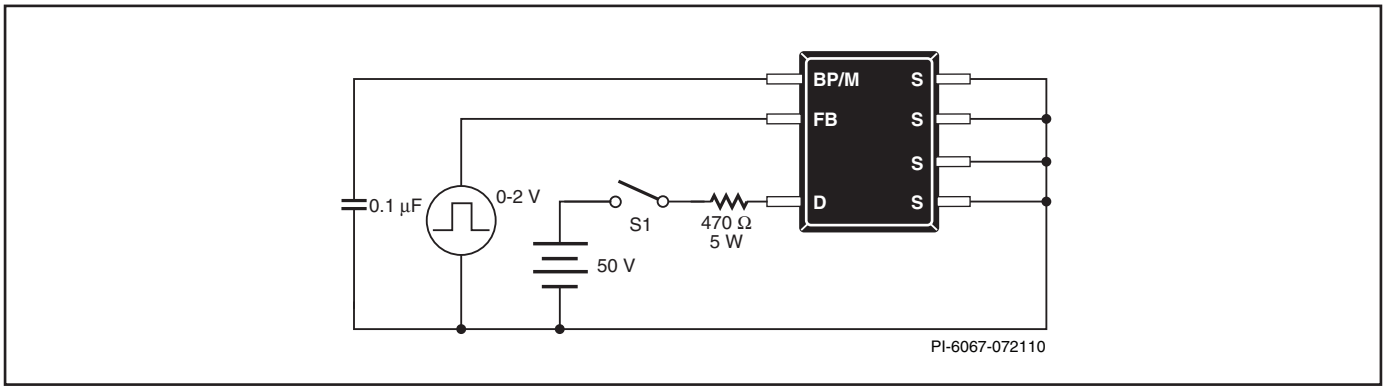


Figure 6. General Test Circuit.

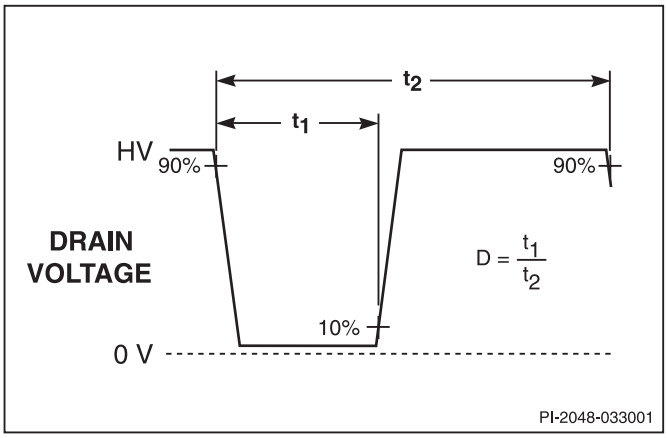


Figure 7. Duty Cycle Measurement.

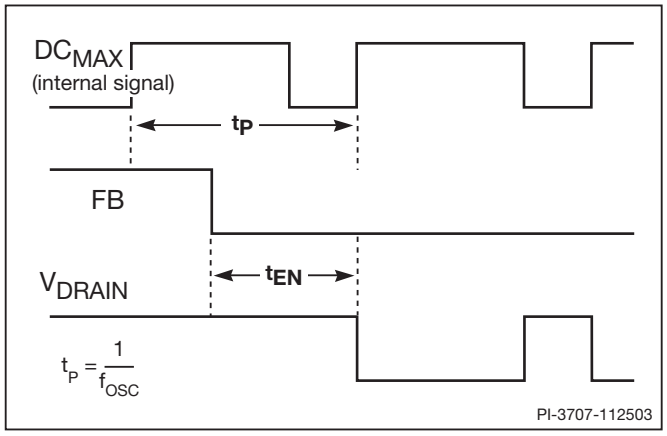


Figure 8. Output Enable Timing.

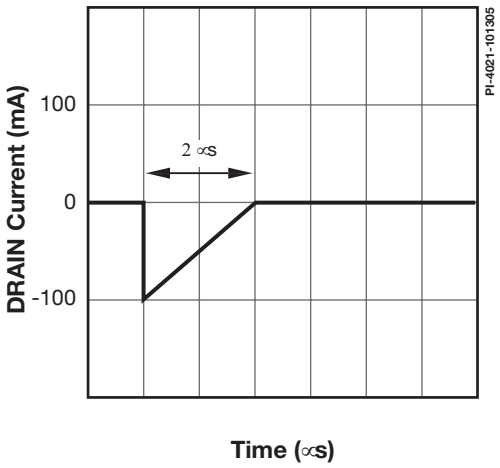


Figure 9. Peak Negative Pulsed DRAIN Current Waveform.

Typical Performance Characteristics

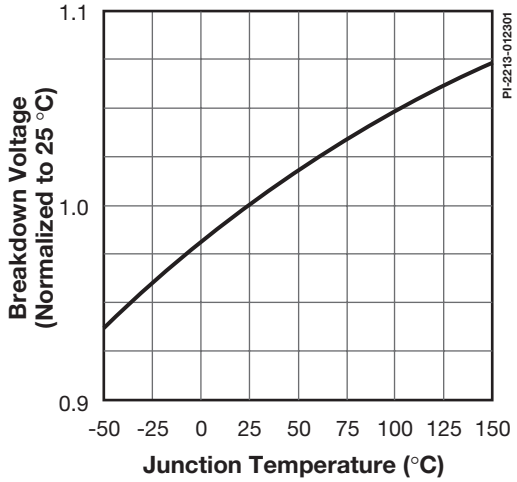


Figure 10. Breakdown vs. Temperature.

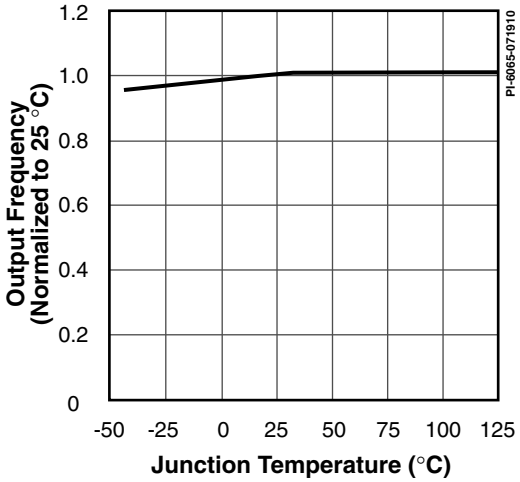


Figure 11. Frequency vs. Temperature.

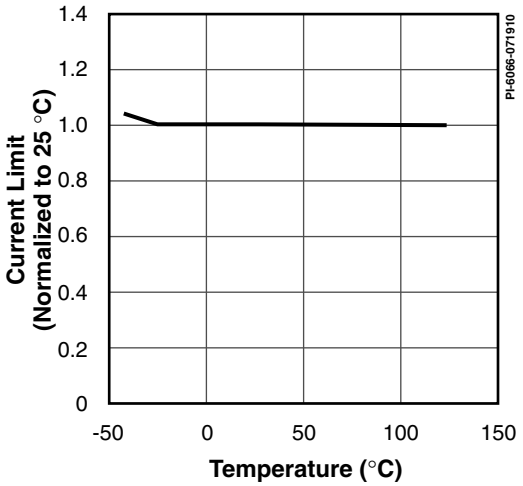


Figure 12. Current Limit vs. Temperature.

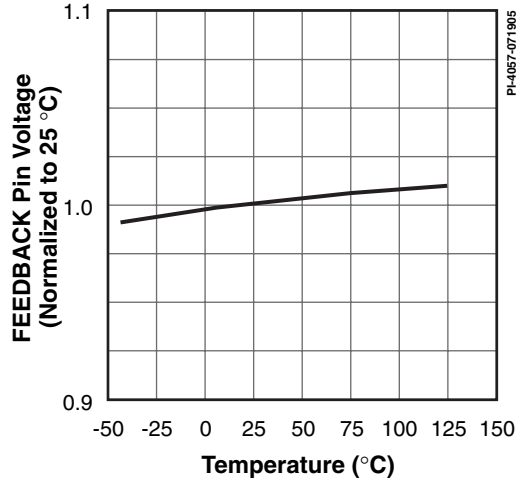


Figure 13. FEEDBACK Pin Voltage vs. Temperature.

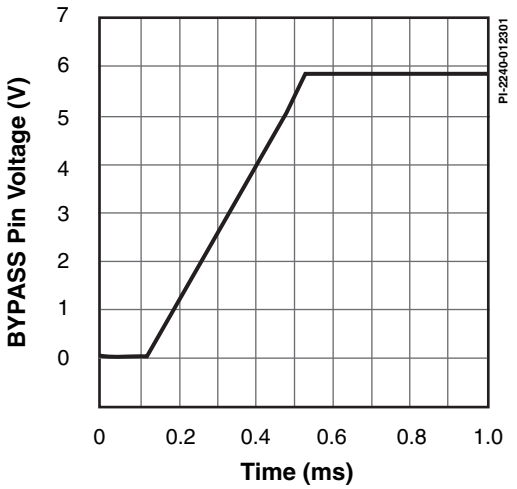


Figure 14. BYPASS Pin Start-up Waveform (C_{BP} = 0.22 µF).

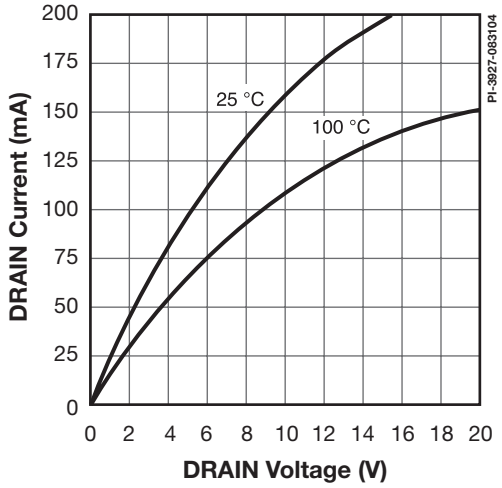


Figure 15. Output Characteristics for LNK574.

Typical Performance Characteristics (cont.)

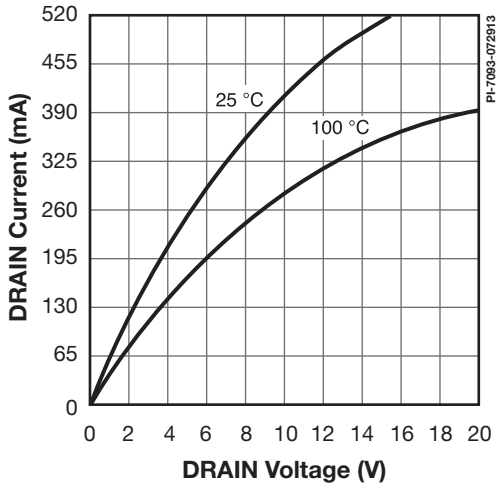


Figure 16. Output Characteristics for LNK576.

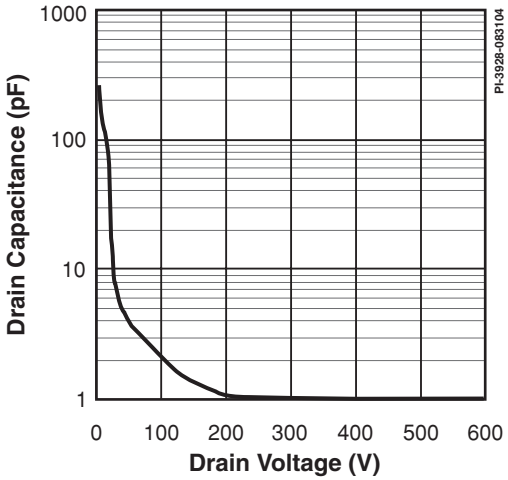


Figure 17. C_{DSS} vs. Drain Voltage for LNK574.

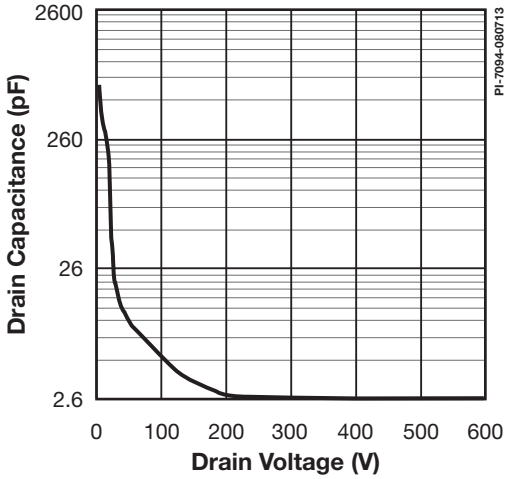


Figure 18. C_{DSS} vs. Drain Voltage for LNK576.

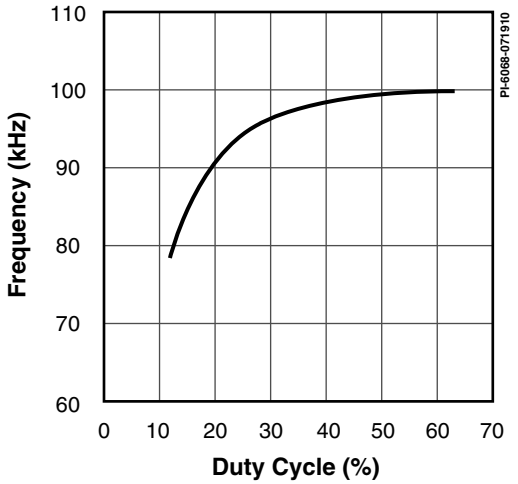


Figure 19. Frequency Reduction vs. Duty Cycle (Line Voltage).

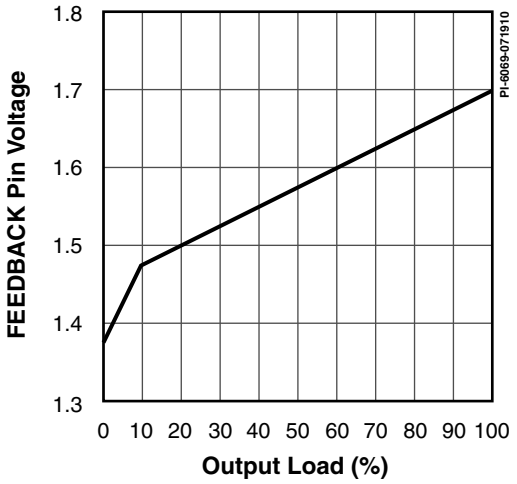


Figure 20. FEEDBACK Pin Regulation Voltage Threshold vs. Output Load in CV Mode.

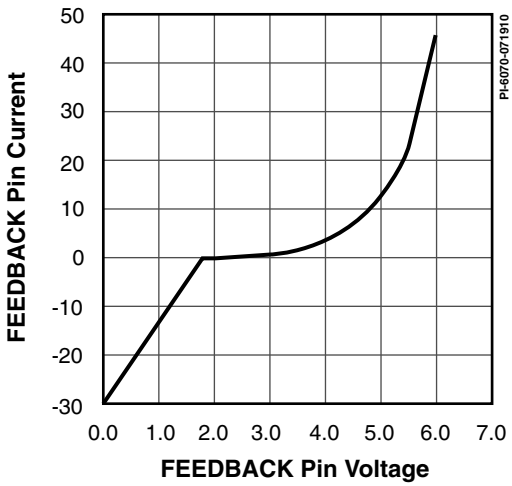


Figure 21. FEEDBACK Pin Input Characteristics.

Typical Performance Characteristics (cont.)

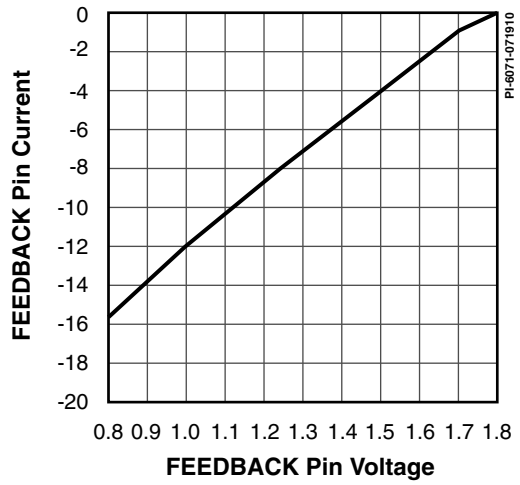


Figure 22. FEEDBACK Pin Input Characteristics in CC Mode (1.7 V to 0.9 V).

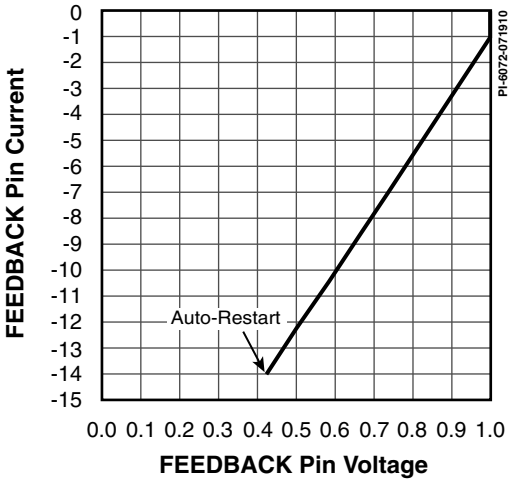


Figure 23. Frequency Cut Back in CC Mode Normalized to 1.

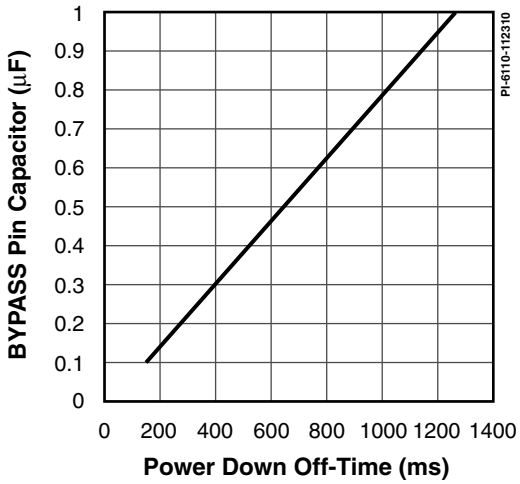


Figure 24. Power-Down Off-Time vs. BYPASS Pin Capacitor. V_{BP} Start at 5.85 V (Temperature = 25 °C)

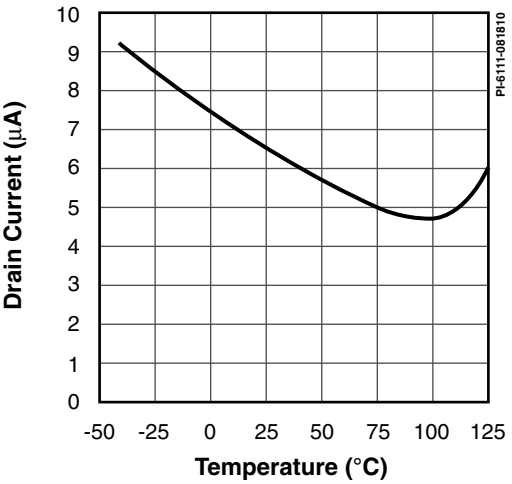
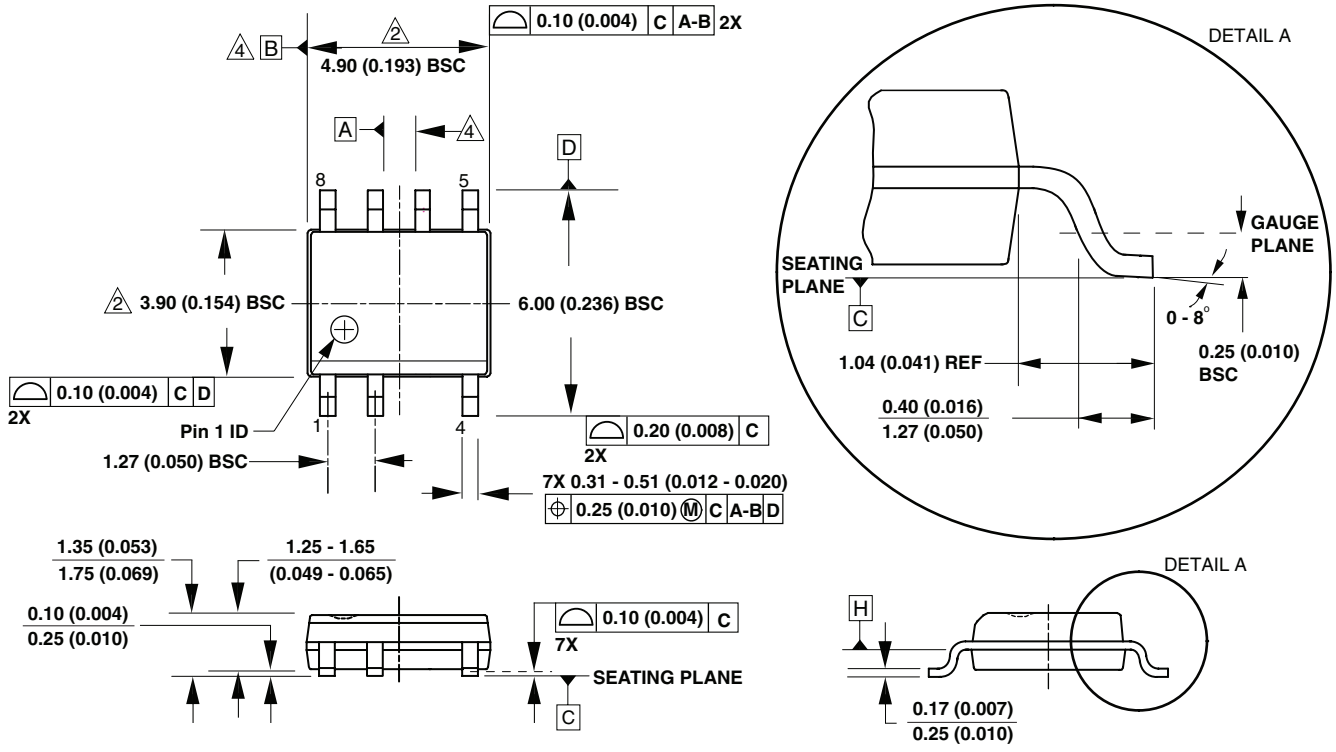
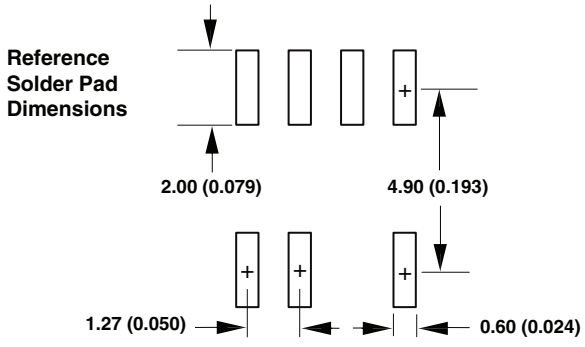


Figure 25. Typical Drain Current vs. Temperature in Power-Down Mode.

SO-8C





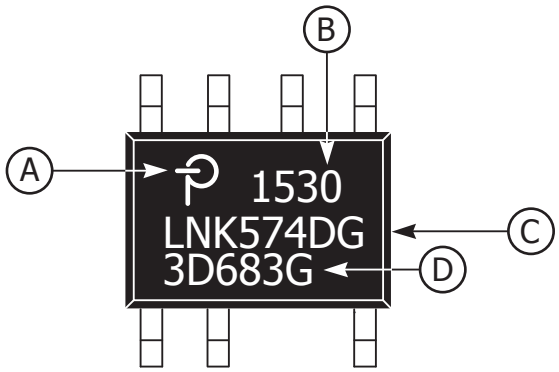
Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-040207

SO-8C PACKAGE MARKING



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-6583-060915

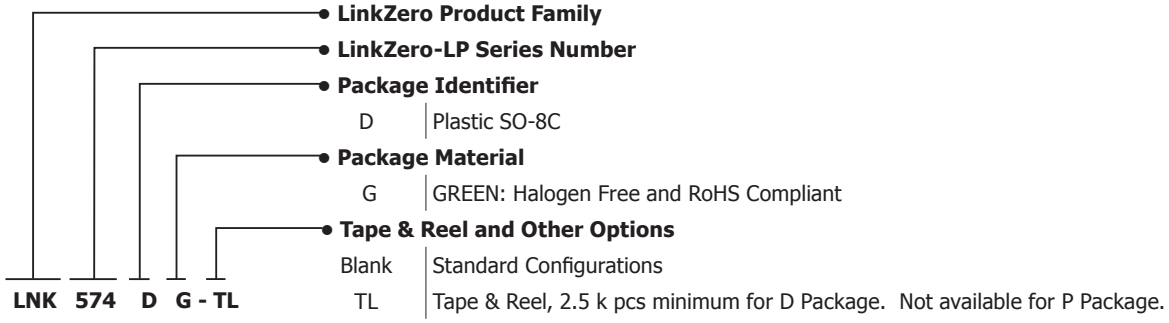
MSL Table

Part Number	MSL Rating
LNK574DG	1
LNK576DG	1

ESD and Latch-Up

Test	Conditions	Results
Latch-up at 125 °C	EIA/JESD78	> ±100 mA or > 1.5 V (max) on all pins
Human Body Model ESD	EIA/JESD22-A114-A	Passes ±2000 V on all pins
Machine Model ESD	EIA/JESD22-A115-A	Passes ±200 V on all pins

Part Ordering Information



Notes

Revision	Notes	Date
A	Internal release.	10/12/10
B	Updated text and parameter tables.	12/07/10
B	Corrected Figure 2.	11/14/12
C	Added LNK576 parts.	05/15/14
D	Updated with new Brand Style. Added Package Marking, ESD and MSL tables.	11/15

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