LNK584-586
LinkZero-AX

Zero Standby Consumption Integrated Off-Line Switcher

Product Highlights

Lowest System Cost with Zero Standby Consumption

- Simple system configuration provides zero consumption standby/power-down with user controlled wake up
- Very tight IC parameter tolerances improves system manufacturing yield
- Suitable for low-cost clampless designs
- Frequency jittering greatly reduces EMI filter cost
- Extended package creepage improves system field reliability

Advanced Protection/Safety Features

- Hysteretic thermal shutdown protection – automatic recovery reduces field returns
- Universal input range allows worldwide operation
- Auto-restart reduces delivered power by >85% during short-circuit and open-loop fault conditions
- Simple ON/OFF control, no loop compensation needed
- High bandwidth provides fast turn on with no overshoot

EcoSmart™– Energy Efficient

- Standby/power-down consumption less than 3 mW at 325 VDC input (Note 1)
- Easily meets all global energy efficiency regulations with no added components
- ON/OFF control provides constant efficiency to very light loads

Applications

- Ultra low consumption isolated or non-isolated standby and auxiliary supplies

Description

LinkZero™-AX combines extremely low standby/power-down energy use with the industry's lowest component count standby supply solution. Below 3 mW at 230 VAC in power-down (PD) mode meets IEC 62301 definition of zero power consumption and is immeasurable on most power meters. LinkZero-AX is set into power-down mode using an external signal to pull the FEEDBACK pin high for 2.5 ms. Such an external signal can be generated by a system micro controller or infrared controller. In power-down mode the BYPASS pin remains regulated allowing the LinkZero-AX to be woken up with a reset pulse to pull the BYPASS pin below a reset threshold (1.5 V). Ultra low system consumption is therefore achieved without needing to disconnect the input voltage with a relay.

LinkZero-AX is designed to be used in isolated or non-isolated converters. In either, the tightly specified FEEDBACK (FB) pin voltage reference enables universal input primary side regulated power supplies that cost effectively replace unregulated linear transformer and other switched mode supplies. The start-up and operating power are derived directly from the DRAIN pin. The internal oscillator frequency is jittered to significantly reduce both quasi-peak and average EMI, minimizing filter cost.

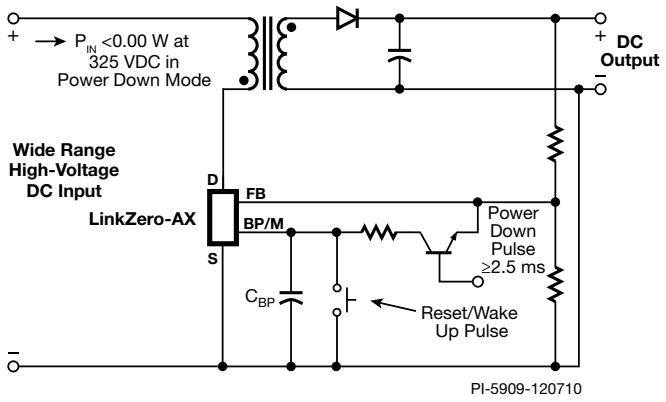


Figure 1. Typical Application Schematic.

Output Power Table

Product[3]	230 VAC ±15%	85-265 VAC
	Open Frame[2]	**Open Frame[2]**
LNK584DG	3 W	3 W
LNK584GG	3 W	3 W
LNK585DG	4.5 W	4 W
LNK585GG	5 W	4.5 W
LNK586DG	6 W	5 W
LNK586GG	6.5 W	5.5 W

Table 1. Output Power Table.

Notes:
1. IEC 62301 Clause 4.5 rounds standby power use below 5 mW to zero.
2. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient.
3. Packages: D: SO-8C, G: SMD-8C.

This Product is Covered by Patents and/or Pending Patent Applications.

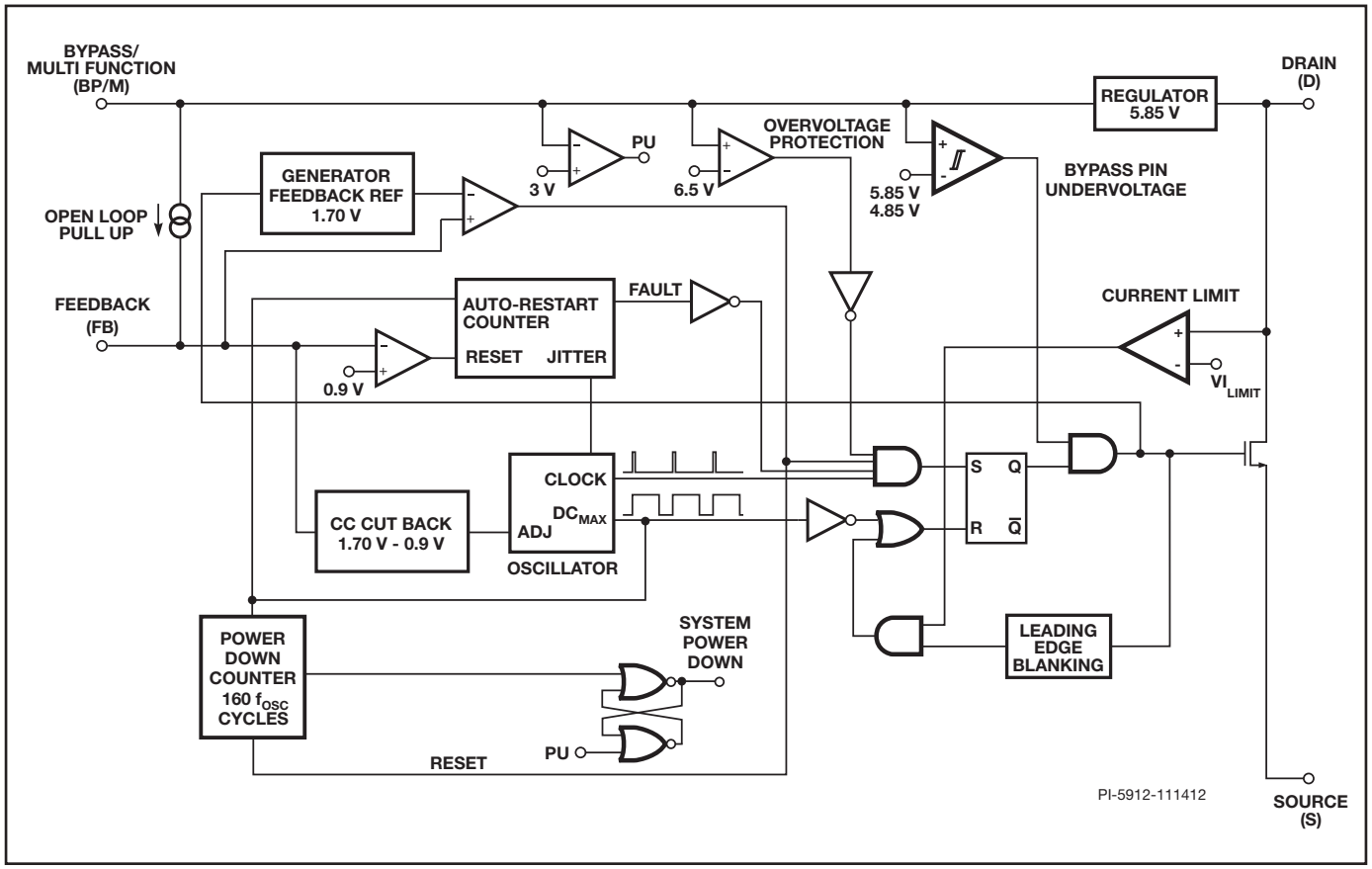


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
The power MOSFET drain connection provides internal operating current for both start-up, steady-state and power-down mode operation.

BYPASS/MULTI-FUNCTIONAL (BP/M) Pin:
An external bypass capacitor, 0.1 μF or greater for the internally generated 5.85 V supply is connected to this pin. The minimum value of capacitor is 0.1 μF for internal circuit operation. Higher values may be required to enter power-down mode (see LinkZero-AX Power-Down (PD) Mode Design Considerations). An overvoltage protection disables MOSFET switching if the current into the pin exceeds 6.5 mA (I_{SD}).

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is disabled when a voltage greater than an internal V_{FB} reference voltage is applied to this pin. The V_{FB} reference voltage is internally set to 1.70 V. LinkZero-AX goes into auto-restart mode when the FEEDBACK pin voltage has come down to 0.9 V.

SOURCE (S) Pin:
This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

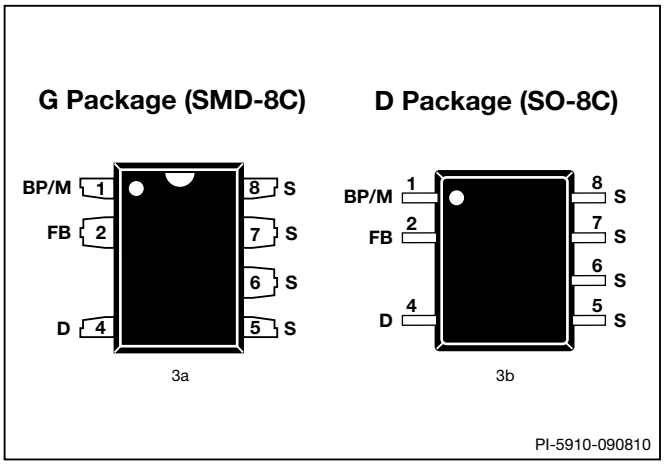


Figure 3. Pin Configuration.

LinkZero-AX Functional Description

LinkZero-AX comprises a 700 V power MOSFET switch with a power supply controller on the same die. Unlike conventional PWM (pulse width modulation) controllers, it uses a simple ON/OFF control to regulate the output voltage. The controller consists of an oscillator, feedback (sense and logic) controller, 5.85 V regulator, BYPASS pin undervoltage protection, over-temperature protection, frequency jittering, current limit protection, and leading edge blanking. The controller includes a proprietary power-down mode that automatically reduces standby consumption to levels that are immeasurable on most power meters.

Power-Down Mode
The internal controller will go into power-down mode when 160 switching cycles are skipped. This can occur due to the FEEDBACK pin being pulled high using an external power-down pulse signal or due to a light load condition where the total loading on the transformer (output plus feedback circuit loads) has reduced to ~0.6% of full load. The device then operates in an ultra low consumption power-down mode where switching is disabled completely. The controller wakes up (or is reset) when the BYPASS pin is pulled below 1.5 V and then released to be recharged through the internal drain connected 5.85 V regulator block (see Figure 2). When the BYPASS capacitor recharges to the V_{BP} BYPASS pin threshold, the device starts switching and operates normally. If the FEEDBACK pin is pulled high such that 160 cycles are again skipped, the device returns to power-down mode operation as described above. In applications with dynamic loads it may not be desirable to go into power-down mode under light or no-load conditions. Techniques to ensure this is avoided are discussed in the LinkZero-AX power-down Mode Design Considerations section.

Oscillator
The typical oscillator frequency is internally set to an average of 100 kHz. An internal circuit senses the duty cycle of the MOSFET switch conduction-time and adjusts the oscillator frequency so that during long conduction intervals (low-line voltage) the frequency is about 100 kHz and at short conduction intervals (high-line voltage) the oscillator frequency is about 78 kHz. This internal frequency adjustment is used to make the peak power point constant over line voltage. Two signals are generated from the oscillator: the maximum duty cycle signal (DC_{MAX}) and the clock signal that indicates the beginning of a switching cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 6% of the switching frequency, to minimize EMI. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak measurements. The frequency jitter, which is proportional to the oscillator frequency, should be measured with the oscilloscope triggered at the falling edge of the DRAIN voltage waveform. The oscillator frequency is gradually reduced when the FEEDBACK pin voltage is lowered below 1.70 V.

Feedback Input Circuit CV Mode
The feedback input circuit reference is set at 1.70 V. When the FEEDBACK pin voltage reaches a V_{FB} reference voltage (1.70 V), a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the FEEDBACK pin voltage during the remainder of the cycle are ignored.

Output Power Limiting
When the FEEDBACK pin voltage at full load falls below 1.70 V, the oscillator frequency linearly reduces to typically 60% at the auto-restart threshold voltage of 0.9 V. This function limits the power supply output current and power.

5.85 V Regulator
The BYPASS pin voltage is regulated by drawing a current from the DRAIN whenever the MOSFET is off if needed to charge up the BYPASS pin to a typical voltage of 5.85 V. When the MOSFET is on, LinkZero-AX runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows LinkZero-AX to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 μF is sufficient for both high frequency decoupling and energy storage.

6.5 V Shunt Regulator and 8.5 V Clamp
In addition, there is a shunt regulator that helps maintain the BYPASS pin at 6.5 V when current is provided to the BYPASS pin externally. This facilitates powering the device externally through a resistor from the bias winding or power supply output in non-isolated designs, to decrease device dissipation and increase power supply efficiency.

The 6.5 V shunt regulator is only active in normal operation, and when in power-down mode a clamp at a higher voltage (typical 8.5 V) will clamp the BYPASS pin.

BYPASS Pin Undervoltage Protection
The BYPASS pin undervoltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.85 V. Once the BYPASS pin voltage drops below 4.85 V, it must rise back to 5.85 V to enable (turn on) the power MOSFET.

BYPASS Pin Overvoltage Protection
If the BYPASS pin gets pulled above 6.5 V and the current into the shunt exceeds 6.5 mA a latch will be set and the power MOSFET will stop switching. To reset the latch the BYPASS pin has to be pulled down to below 1.5 V.

Over-Temperature Protection
The thermal shutdown circuit senses the die temperature. The threshold is set at 142 °C typical with a 70 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 70 °C, at which point the MOSFET is re-enabled.

Current Limit
The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction.

Auto Restart
In the event of a fault condition such as output short-circuit, LinkZero-AX enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FEEDBACK pin voltage exceeds the FEEDBACK pin auto-restart threshold voltage ($V_{FB(AR)}$ typical 0.9 V). If the FEEDBACK pin voltage drops below $V_{FB(AR)}$ for more than 145 ms to 170 ms depending on the line voltage, the power MOSFET switching is disabled. The auto-restart alternately enables and disables the switching of the power MOSFET at a duty cycle of typically 12% until the fault condition is removed.

Open-Loop Condition on the FEEDBACK Pin

When an open-loop condition on the FEEDBACK pin is detected, an internal current source pulls up the FEEDBACK pin to above the V_{FB} (1.70 V), the part stops switching and after 160 clock cycles goes into latched power-down mode.

Applications Example

The circuit shown in Figure 4 is a typical non-isolated 5 V, 300 mA output auxiliary power supply using LinkZero-AX. Isolated configurations are also fully compatible with the LinkZero-AX where the FEEDBACK pin receives a signal from a primary feedback/bias winding or through an optocoupler. The circuit of Figure 4 is typical of auxiliary supplies in white goods where isolation is often not required. AC input differential filtering is accomplished by the π filter formed by C1, C2 and L3. The proprietary frequency jitter feature of the LinkZero-AX eliminates the need for any Y capacitor or common-mode inductor. Wire-wound resistor RF1 is a fusible, flame proof resistor which is used as a fuse as well as to limit inrush current. Wire wound types are recommended for designs that operate >132 VAC to withstand the instantaneous power dissipated when AC is first applied.

The output voltage is directly sensed through feedback resistors R3 and R9, and regulated by LinkZero-AX (U1) via the FEEDBACK pin. Capacitor C7 provides high frequency filtering on the FEEDBACK pin to filter noise and to avoid switching cycle pulse bunching. The controller in U1 receives feedback from the output through feedback resistors R9 and R3. Based on that feedback, it enables or disables the switching of its integrated MOSFET to maintain output regulation. Switching cycles are skipped once the FEEDBACK pin threshold voltage (1.70 V) is exceeded. When the voltage on the FEEDBACK pin falls below the disable threshold (1.70 V), switching cycles are re-enabled. By adjusting the ratio of enabled to disabled switching cycles the output voltage is regulated. At increased loads, beyond the output peak power point, where all switching cycles are enabled, the FEEDBACK pin voltage begins to reduce as the power supply output voltage falls. Under this condition the switching frequency is also reduced to limit the maximum output overload power. When the FEEDBACK pin voltage drops below the auto-restart threshold (typically 0.9 V on the FEEDBACK pin), the power supply enters the auto-restart mode. In this mode, the power supply will turn off for approximately 1.2 s and then turn back on for approximately 145 ms. The auto-restart function reduces the average output current during an output short-circuit condition.

The LinkZero-AX device is self biased through the DRAIN pin. An optional external bias, can be derived either from a third winding or from an output voltage rail in non-isolated designs. By providing an external supply current in excess of I_{S2} (310 µA for the LNK584) the internal 5.85 V regulator circuit is disabled providing a simple way to reduce device temperature and improve efficiency, especially at high-line.

A clampless primary circuit is achieved due to the very tight tolerance current limit device, plus the transformer construction techniques used. The peak drain voltage is therefore limited to typically less than 550 V at 265 VAC, providing significant margin to the 700 V minimum drain voltage specification (BV_{DSS}).

Output rectification and filtering is achieved with output rectifier D6 and filter capacitor C6. Due to the auto-restart feature, the average

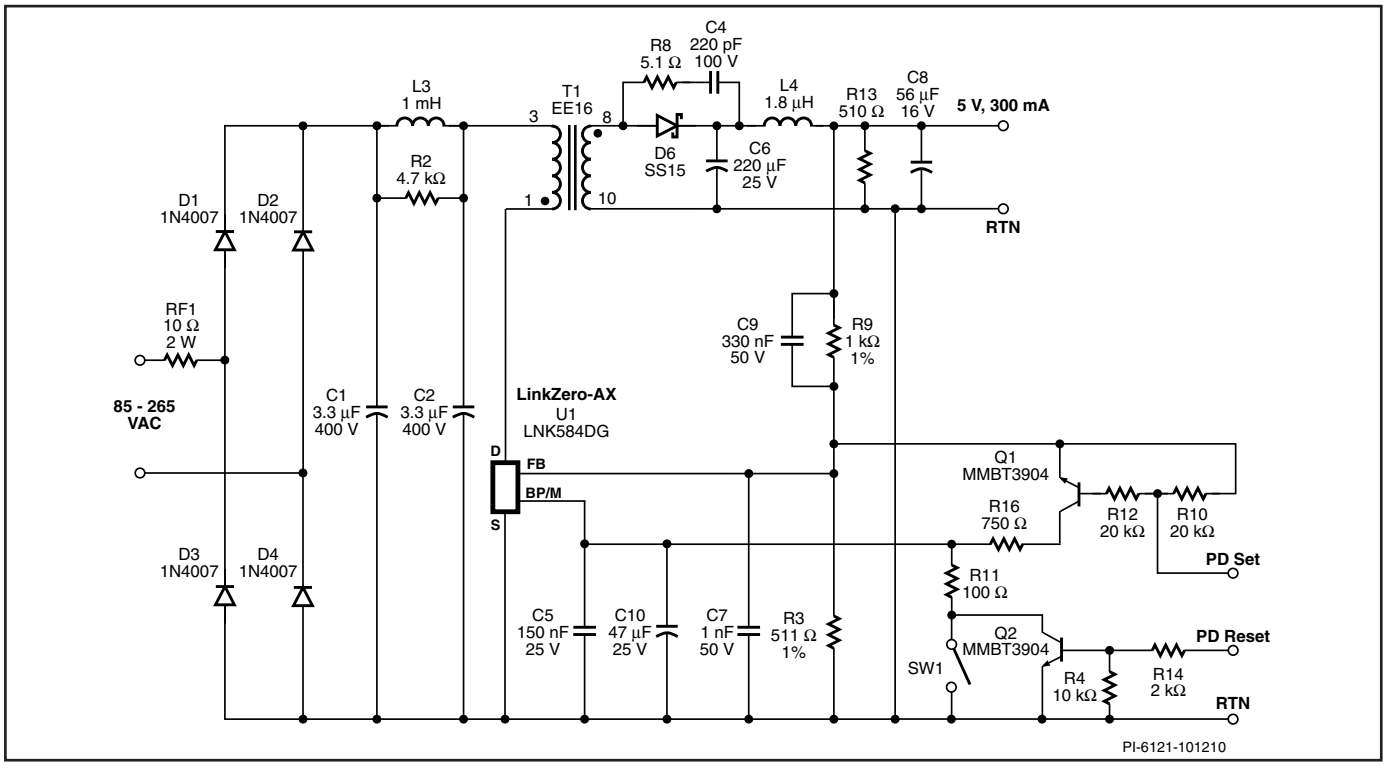


Figure 4. Schematic of Non-Isolated 1.5 W, 5 V, 300 mA, 0.00 W Standby Consumption Power Supply.

short-circuit output current is significantly less than 1 A, allowing low current rating and low cost rectifier D6 to be used. Output circuitry is designed to handle a continuous short-circuit on the power supply output. In this design a preload resistor R13 is used at the output of the supply to prevent automatic triggering of the power-down mode when the load is removed.

LinkZero-AX Power-Down (PD) Mode Design Considerations

LinkZero-AX goes into power-down mode when 160 consecutive switching cycles have been skipped. This condition occurs when the output load is low or the FEEDBACK pin is pulled high (for example through Q1 and R16 in Figure 4). The value of the BYPASS pin capacitor must be high enough to sustain enough current through R16 for more than the period of 160 switching cycles to successfully trigger the power-down mode. At low-line input voltage (90 VAC) the 160 switching cycle period is ~1.6 ms as the internal oscillator frequency is 100 kHz. However as the input line voltage increases, the internal oscillator frequency is gradually reduced to keep the maximum output power relatively constant. At high-line (265 VAC) therefore, the internal oscillator frequency can be as low as 78 kHz (see parameter table Note C). Therefore to provide sufficient margin to ensure power-down mode is triggered it is recommended that the power-down pulse (see Figure 1) is 2.5 ms (200 switching cycles at 80 kHz). LinkZero-AX stops switching once the power-down mode is triggered. The IC does not resume switching until the BYPASS pin is pulled below 1.5 V using the reset/wake up pulse (see Figure 1) and then allowed to recharge back up to 5.85 V through the drain connected 5.85 V regulator block. Transistor Q2 or mechanical switch SW1 can be used for resetting the power-down mode either electronically or mechanically.

It is important to design the power supply to ensure that load transients and other external events do not unintentionally trigger power-down mode by causing 160 consecutive switching cycles to be skipped. It is recommended that a preload resistor is added to draw ~2% of the full load current (12 mA at 5 V in a 3 W power supply). Although this reduces full load efficiency slightly, it has no influence on the power consumption during power-down mode since the power supply output is fully discharged under this condition. Low value feedback resistors may also be used as a preload too. Recommended value of the feedback resistors is such that they should draw ~1% of full load current. Finally a capacitor in parallel to the high side feedback resistor can be used to increase the speed of the loop (C9 in Figure 4).

These recommendations apply for full load to zero load transients. For applications with more limited load range, the preload and the capacitor in parallel to the high side feedback resistor may not be necessary.

Layout Considerations

LinkZero-AX Layout Considerations

Layout
See Figure 5 for a recommended circuit board layout for LinkZero-AX (U1).

Single Point Grounding
Use a single point ground (Kelvin) connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitor (C_{BP}), FEEDBACK Pin Noise Filter Capacitor (C_{FB}) and Feedback Resistors
To minimize loop area, these two capacitors should be physically located as near as possible to the BYPASS and SOURCE pins, and FEEDBACK pin and source pins respectively. Also note that to minimize noise pickup, feedback resistors R_{FB1} and R_{FB2} are placed close to the FEEDBACK pin.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and LinkZero-AX should be kept as small as possible.

Primary Clamp Circuit
An external clamp may be used to limit peak voltage on the DRAIN pin at turn off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and LinkZero-AX (U1).

Thermal Considerations
The copper area underneath the LinkZero-AX (U1) acts not only as a single point ground, but also as a heat sink. As it is connected to the quiet source node, this area should be maximized for good heat sinking of U1. The same applies to the cathode of the output diode.

Y Capacitor
The placement of the Y-type capacitor (if used) should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common-mode surge currents away from U1. Note: If an input π EMI filter is used, the inductor in the π filter should be placed between the negative terminals on the input filter capacitors.

Output Diode (D_O)
For best performance, the area of the loop connecting the secondary winding, the output diode (D_O) and the output filter capacitor (C_O) should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heat sinking. A larger area is preferred at the electrically "quiet" cathode terminal. A large anode area can increase high frequency conducted and radiated EMI. Resistor R_S and C_S represent the secondary side RC snubber.

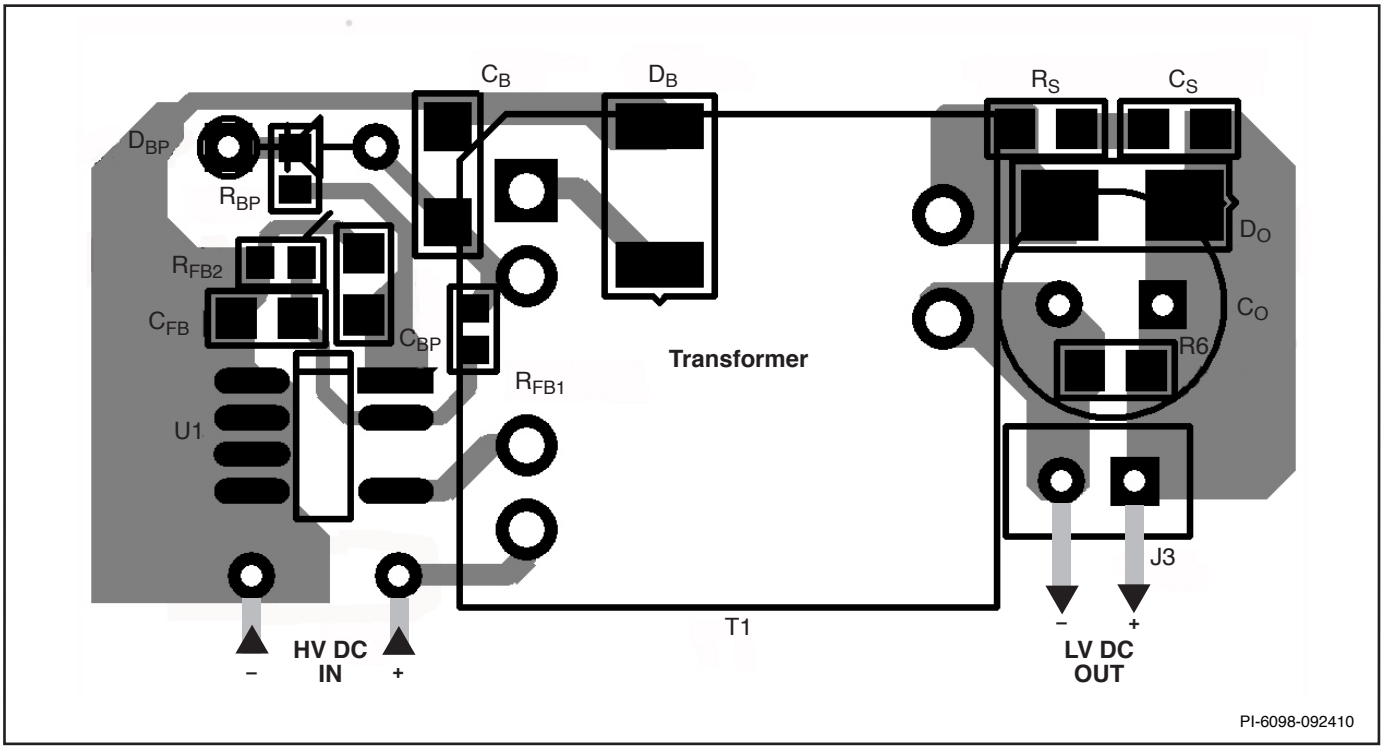


Figure 5. PCB Layout of a 2.1 W, 6 V, 350 mA Charger.

Quick Design Checklist

As with any power supply design, all LinkZero-AX designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 660 V at the highest input voltage and peak (overload) output power. This margin to the 700 V BV_{DSS} specification gives margin for design variation, especially in clampless designs.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading-edge current spikes at start-up. Repeat under steady state conditions and verify that the leading-edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for LinkZero-AX, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkZero-AX as specified in the data sheet. Under low-line and maximum power, maximum LinkZero-AX source pin temperature of 100 °C is recommended to allow for these variations.

Absolute Maximum Ratings[1,6]

DRAIN Voltage .....-0.3 V to 700 V
Peak DRAIN Current[2]: LNK584 .....200 (375) mA
LNK585 .....370 (680) mA
LNK586 .....440 (825) mA
Peak Negative Pulsed Drain Current[3].....-100 mA
Feedback Voltage ..... -0.3 V to 9 V
Feedback Current .....100 mA
BYPASS Pin Voltage ..... -0.3 V to 9 V
BYPASS Pin Voltage in Power-Down Mode[7].....-0.3 V to 11 V
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature[4] .....-40 °C to 150 °C
Lead Temperature[5] .....260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Higher peak DRAIN current allowed while DRAIN source voltage does not exceed 400 V.
3. Duration not to exceed 2 μs.
4. Normally limited by internal circuitry.
5. 1/16 in. from case for 5 seconds.
6. Maximum ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum ratings for extended periods of time may affect product reliability.
7. Maximum current into pin is 300 μA.

Thermal Resistance

Thermal Resistance: D Package:
(θ_{JA}) .....100 °C/W[2]; 80 °C/W[3]
(θ_{JC}) .....30 °C/W[1]
G Package:
(θ_{JA}) .....70 °C/W[2]; 60 °C/W[3]
(θ_{JC}) .....11 °C/W[1]

Notes:
1. Measured on the SOURCE pin close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm²), 2 oz. copper clad.
3. Soldered to 1 sq. in. (645 mm²), 2 oz. copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency	f_{OSC}	T_J = 25 °C V_{FB} = 1.70 V, See Note B		93	100	107	kHz
Frequency Jitter		Peak-Peak Jitter Compared to Average Frequency, T_J = 25 °C			±3		%
Ratio of Output Frequency at Auto-Restart to f_{osc}	$\frac{f_{OSC(AR)}}{f_{OSC}}$	T_J = 25 °C $V_{FB} = V_{FB(AR)}$			60		%
Maximum Duty Cycle	DC_{MAX}			60	63		%
FEEDBACK Pin Voltage	V_{FB}			1.63	1.70	1.77	V
FEEDBACK Pin Voltage at Auto-Restart	$V_{FB(AR)}$			0.8	0.9	1.05	V
Minimum Switch ON-Time	$t_{ON(MIN)}$				700		ns
DRAIN Supply Current	I_{S1}	Feedback Voltage > V_{FB} (MOSFET not Switching)			200	260	μA
	I_{S2}	0.9 V ≤ V_{FB} ≤ 1.70 V (MOSFET Switching)	LNK584		260	310	μA
			LNK585		275	330	
			LNK586		285	340	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C	LNK584	-5.5	-3.8	-1.8	mA
			LNK585-586	-7.0	-5.3	-3.3	
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C	LNK584	-3.8	-2.5	-1.0	
			LNK585-586	-4.8	-3.5	-2.0	
BYPASS Pin Voltage	V_{BP}			5.60	5.85	6.10	V
BYPASS Pin Voltage Hysteresis	$V_{BP(H)}$			0.8	1.0	1.2	V
BYPASS Pin Shunt Voltage	BP_{SHUNT}			6.1	6.5	6.9	V
BYPASS Pin Supply Current	I_{BPSC}	See Note D		84			µA
Circuit Protection							
Current Limit	I_{LIMIT}	di/dt = 40 mA/µs T_J = 25 °C	LNK584	126	136	146	mA
		di/dt = 75 mA/µs T_J = 25 °C	LNK585	232	250	268	
		di/dt = 90 mA/µs T_J = 25 °C	LNK586	279	300	321	
Power Coefficient	I^2f	di/dt = 40 mA/µs T_J = 25 °C	LNK584	1665	1850	2091	A^2Hz
		di/dt = 75 mA/µs T_J = 25 °C	LNK585	5625	6250	7063	
		di/dt = 90 mA/µs T_J = 25 °C	LNK586	8100	9000	10170	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C		220	265		ns
BYPASS Pin Shutdown Threshold Current	I_{SD}	V_{BP} = BP_{SHUNT} See Note F		5.0	6.5	8.0	mA
Thermal Shutdown Temperature	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C
Power-Down (PD) Mode							
OFF-State Drain Leakage in Power-Down Mode	$I_{DSS(PD)}$	T_J = 25 °C, V_{DRAIN} = 325 V See Figure 21			6.5	9	µA
BYPASS Pin Overvoltage Protection in Power-Down Mode	$V_{BP(PDP)}$	I_{BP} = 300 µA -5 °C ≤ T_J ≤ 100 °C		7.0	8.5	10.9	V
BYPASS Pin Power-Up Reset Threshold (in Power-Down Mode or at Power Supply Start-up)	$V_{BP(PU)}$			1.5	3	4	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Power-Down (PD) Mode (cont.)							
BYPASS Pin Voltage in Power-Down Mode	$V_{BP(PD)}$	I_{BP} = 500 µA			4		V
BYPASS Pin Power-Down to Power-Up Threshold Delta	$V_{BP(PD)}$ - $V_{BP(PU)}$			0.5			V
BYPASS Pin Supply Current in Power-Down Mode	$I_{BPSC(PD)}$	V_{BP} = $V_{BP(PD)}$ See Note E		500			µA
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK584 I_D = 13 mA	T_J = 25 °C		48	55	Ω
			T_J = 100 °C		76	88	
		LNK585 I_D = 26 mA	T_J = 25 °C		24	28	
			T_J = 100 °C		38	44	
		LNK586 I_D = 33 mA	T_J = 25 °C		19	22	
			T_J = 100 °C		30	35	
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, T_J = 25 °C		700			V
DRAIN Supply Voltage				50			V
Auto-Restart ON-Time	t_{AR}	V_{IN} = 85 VAC, T_J = 25 °C, See Note C			145		ms
Auto-Restart Duty Cycle					11		%
Output Enable Delay	t_{EN}	See Figure 8				14	µs

NOTES:

A. This parameter is derived from characterization.

B. Output frequency specification applies to low-line input voltage in the final application. The controller is designed to reduce output frequency by approximately 20% at high-line input voltages to balance low-line and high-line maximum output power.

C. The auto-restart on-time/off-time is increased by 20% from low to high-line voltage input (85 VAC to 265 VAC).

D. I_{BPSC} is the current that can be supplied from the BYPASS pin at 5.85 V when in normal switching mode of operation to power an optional external circuit. The current will be supplied from the Drain via the internal BYPASS pin voltage regulator. When calculating the power consumption the I_{BPSC} (84 µA max) and the drain voltage has to be taken into account. More current can be sourced during power-down mode – see Note E.

$I_{BPSC(PD)}$ is the current that can be supplied from the BYPASS pin at 4 V when in power-down mode to power an optional external circuit. The current will be supplied from the Drain via the internal BYPASS pin voltage regulator. Lower current is available during normal operation – see Note D. If the external circuit requires current in excess of $I_{BP(PD)}$ in power-down mode, it must be supplied from an external source such as a bias winding. The $I_{BP(PD)}$ current adds to power supply power consumption during power-down mode – for example at 230 VAC (325 VDC rectified DC rail voltage) the power consumption with be 325 × $I_{BP(PD)}$.

E. LinkZero-AX shuts down if the current into the BYPASS pin reaches I_{SD} at the BP_{SHUNT} voltage.

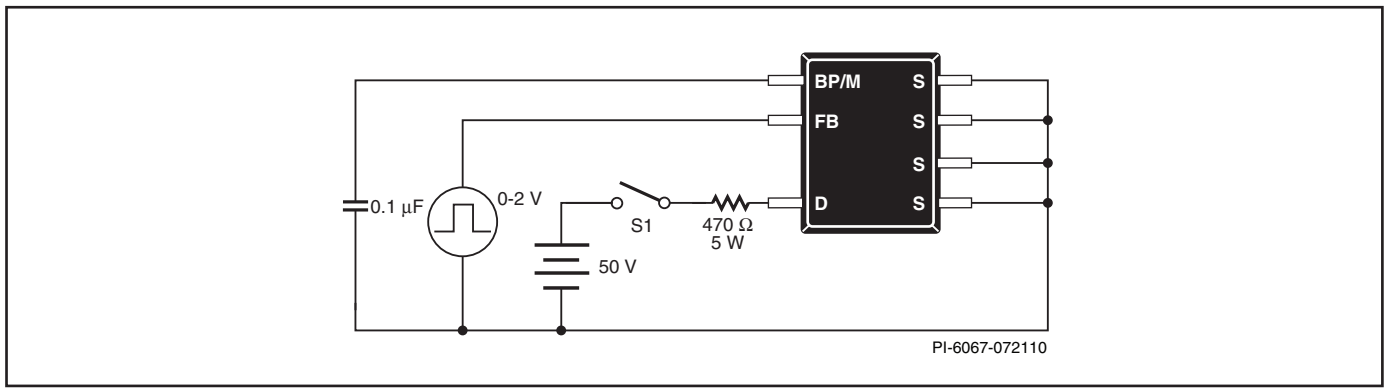


Figure 6. General Test Circuit.

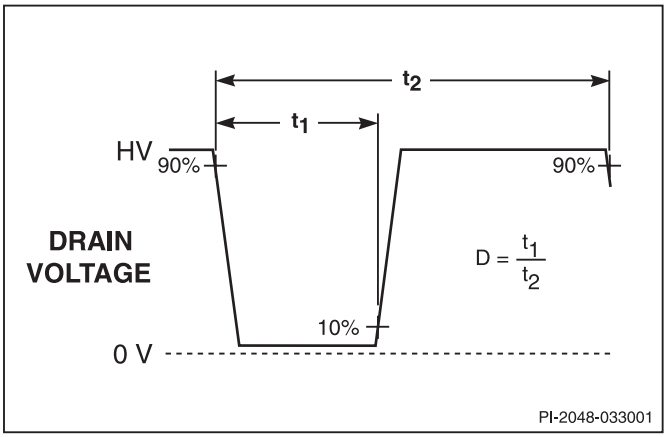


Figure 7. Duty Cycle Measurement.

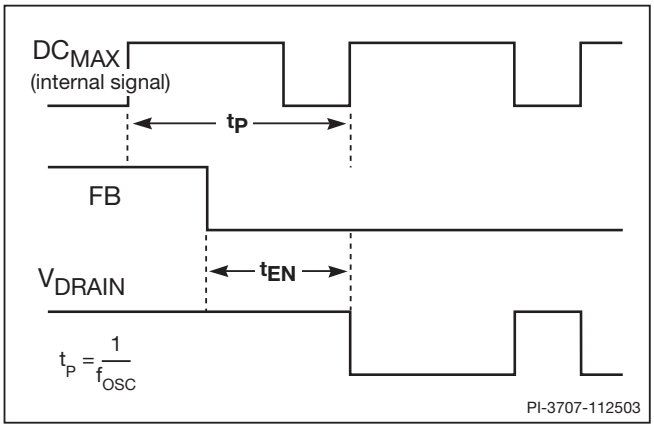


Figure 8. Output Enable Timing.

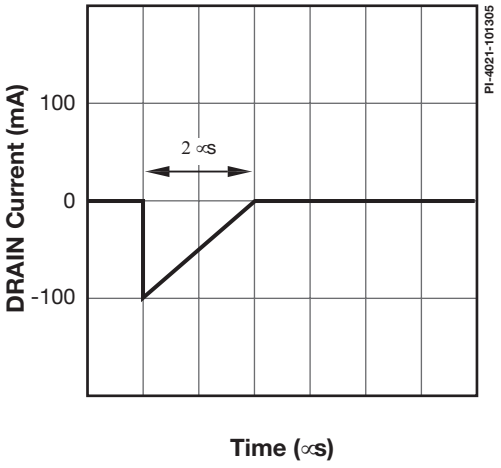


Figure 9. Peak Negative Pulsed DRAIN Current Waveform.

Typical Performance Characteristics

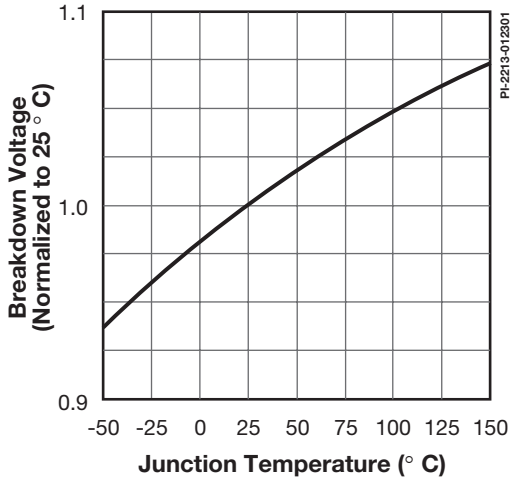


Figure 10. Breakdown vs. Temperature.

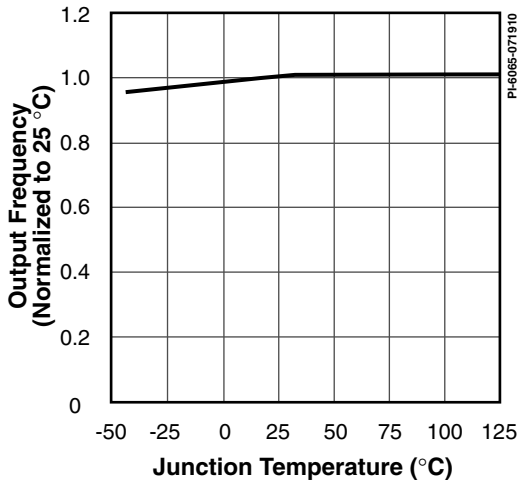


Figure 11. Frequency vs. Temperature.

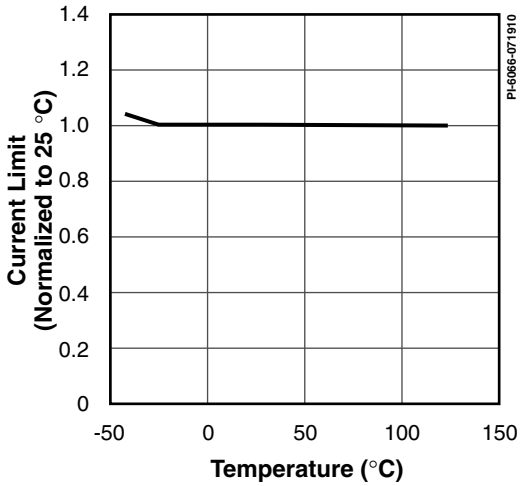


Figure 12. Current Limit vs. Temperature.

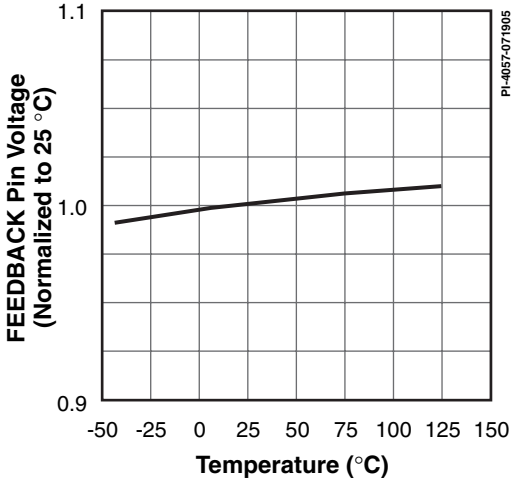


Figure 13. FEEDBACK Pin Voltage vs. Temperature.

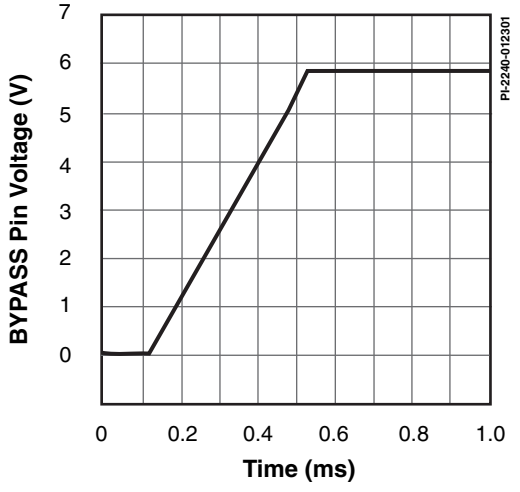


Figure 14. BYPASS Pin Start-up Waveform (C_{BP} = 0.22 μF).

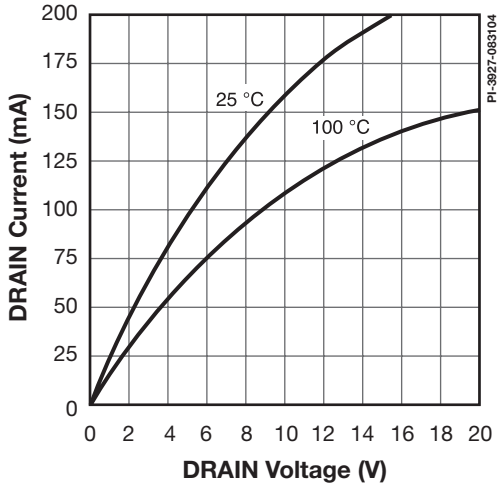


Figure 15. Output Characteristics.

Typical Performance Characteristics (cont.)

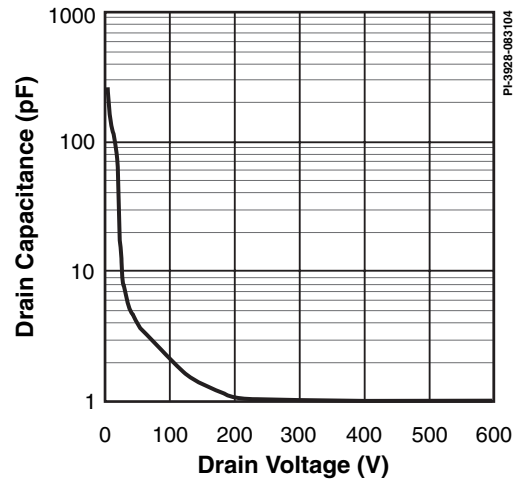


Figure 16. C_{DSS} vs. Drain Voltage.

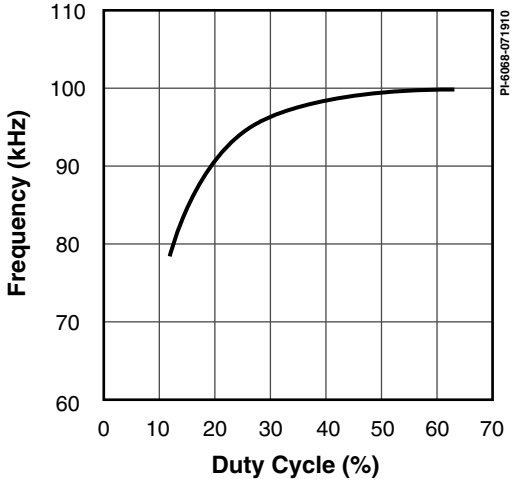


Figure 17. Frequency Reduction vs. Duty Cycle (Line Voltage).

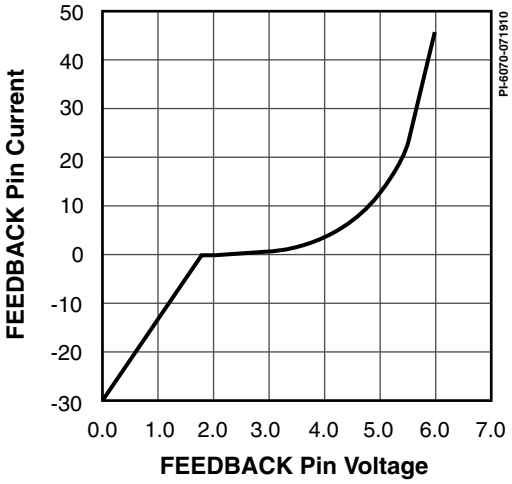


Figure 18. FEEDBACK Pin Input Characteristics.

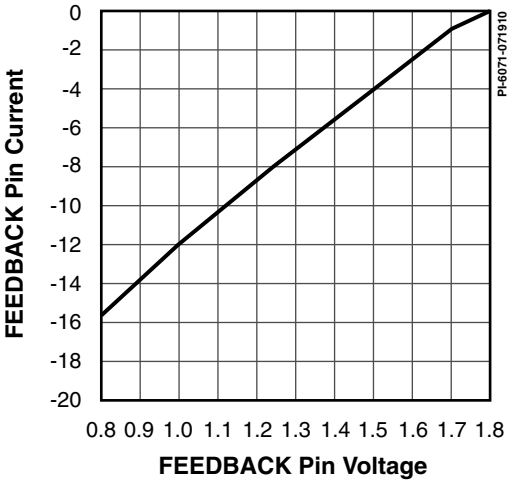


Figure 19. FEEDBACK Pin Input Characteristics During Output Power Limiting (1.70 V to 0.9 V).

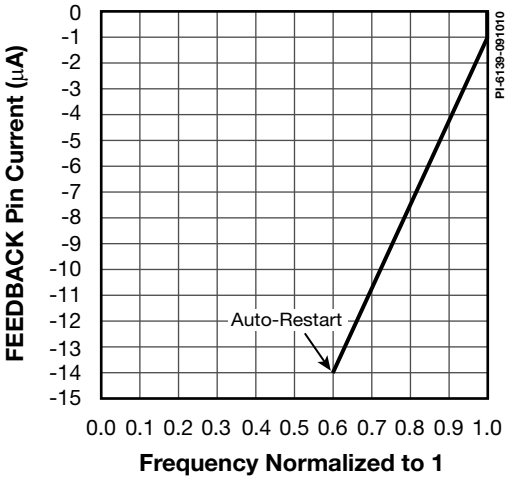


Figure 20. Frequency Cut Back During Output Power Limiting.

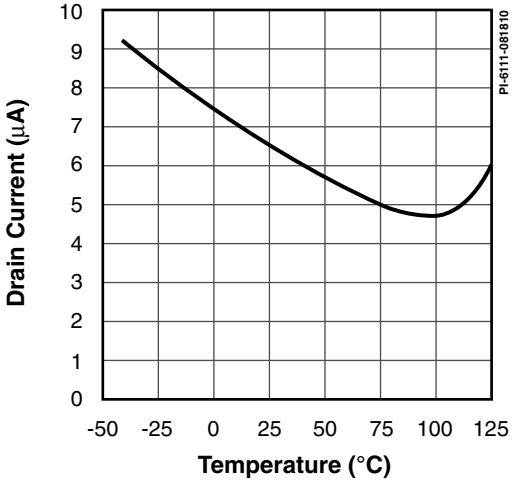
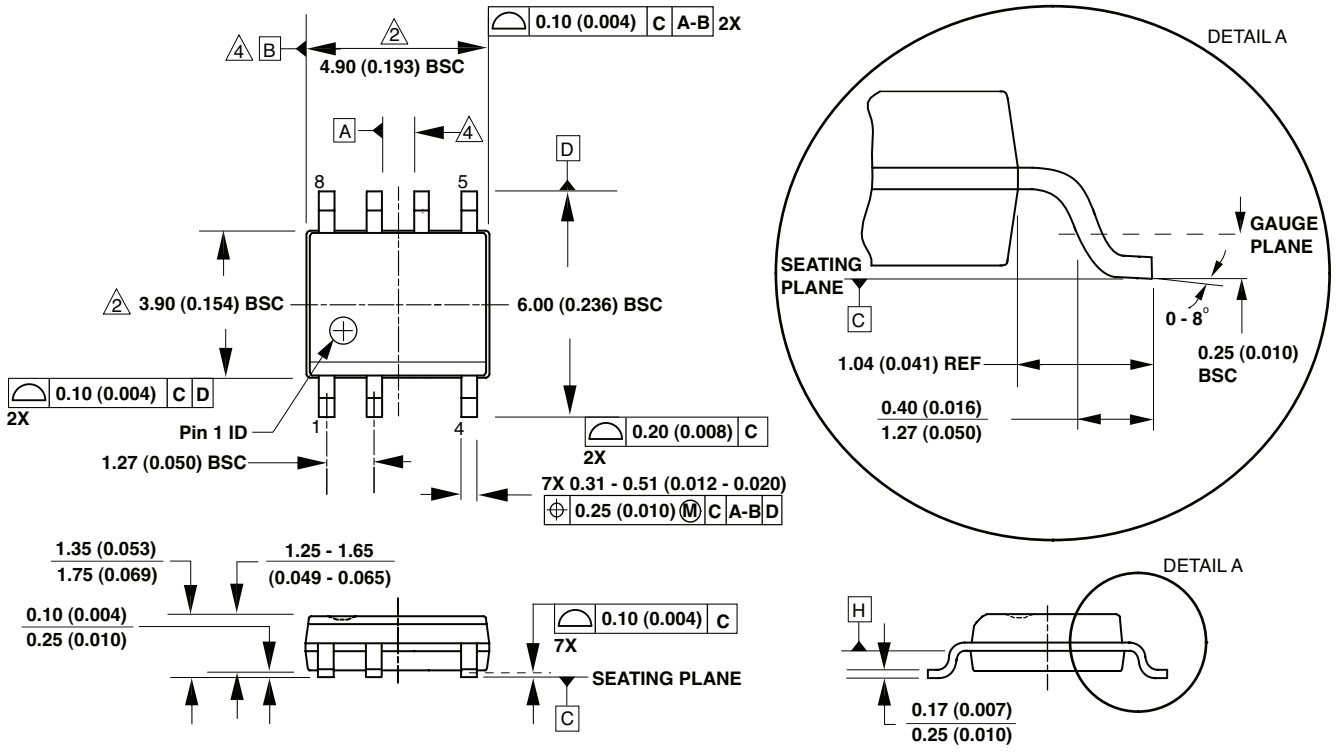


Figure 21. Typical Drain Current vs. Temperature in Power-Down Mode.

SO-8C (D Package)



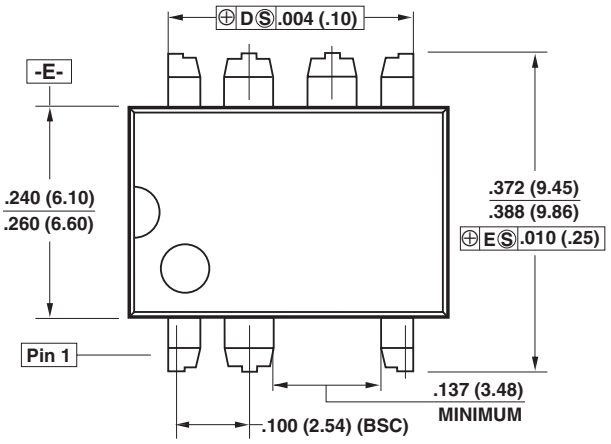
Notes:

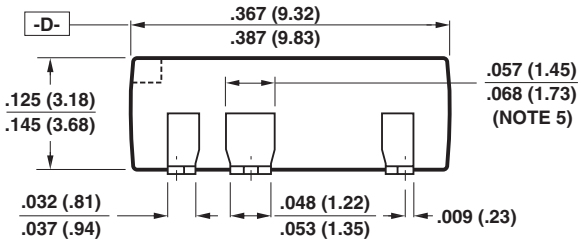
1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

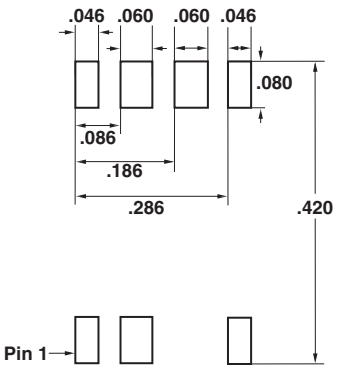
D07C

PI-4526-040110

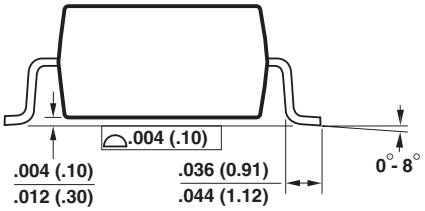
SMD-8C (G Package)







Solder Pad Dimensions



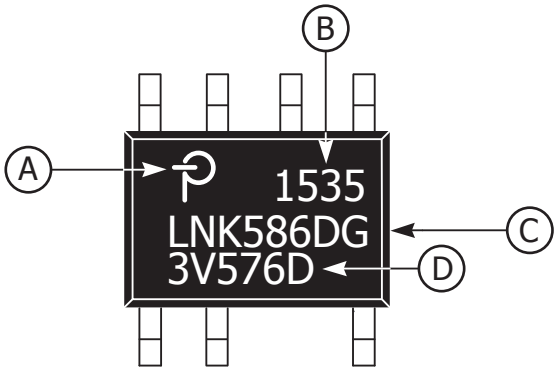
Notes:

1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
3. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 3 is omitted.
4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
5. Lead width measured at package body.
6. D and E are referenced datums on the package body.

G08C

PI-4015-101507

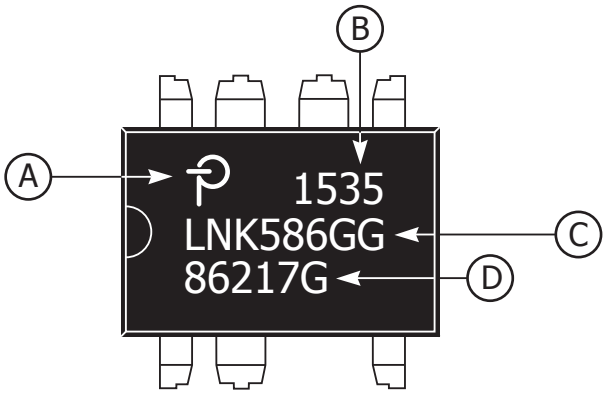
SO-8C PACKAGE MARKING



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-6623-040615

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D. Lot Identification Code

PI-6624-040615

MSL Table

Part Number	MSL Rating
LNK584DG LNK585DG LNK586DG	1
LNK584GG LNK585GG LNK586GG	4

ESD and Latch-Up

Test	Conditions	Results
Latch-up at 125 °C	JESD78C	> ±100 mA or > 1.5 V (max) on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	Passes ±2000 V on all pins
Machine Model ESD	JESD22-A115C	Passes ±200 V on all pins

Part Ordering Information



Notes

Revision	Notes	Date
A	Initial release.	10/10
B	Added LNK585 and LNK586.	05/11
B	Corrected Figure 2.	11/14/12
C	Updated with new Brand Style. Added Package Marking, ESD and MSL tables.	11/15

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