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ISL9203R5220

Li-ion/Li Polymer Battery Charger

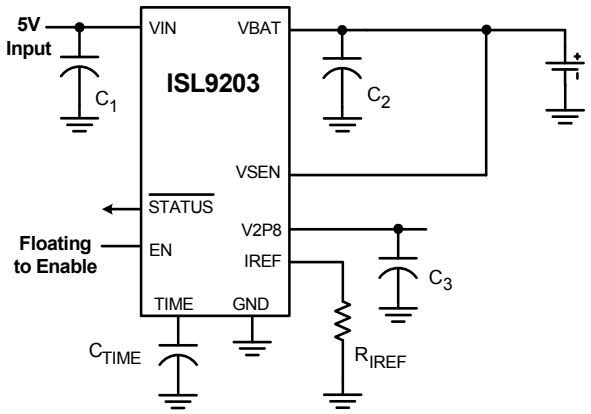
FN9242
Rev 1.00
January 3, 2006

The ISL9203R5220 is an integrated single-cell Li-ion or Li-polymer battery charger capable of operating with an input voltage as low as 2.4V. This charger is designed to work with various types of AC adapters.

The ISL9203R5220 operates as a linear charger when the AC adapter is a voltage source. The battery is charged in a CC/CV (constant current/constant voltage) profile. The charge current is programmable with an external resistor up to 1.5A. The ISL9203R5220 can also work with a current-limited adapter to minimize the thermal dissipation, in which case the ISL9203R5220 combines the benefits of both a linear charger and a pulse charger.

The ISL9203R5220 features charge current thermal foldback to guarantee safe operation when the printed circuit board is space limited for thermal dissipation. Additional features include preconditioning of an over-discharged battery and thermally enhanced DFN package.

Typical Application Circuit



Features

- Complete Charger for Single-Cell Li-ion Batteries
- Very Low Thermal Dissipation
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- 1% Voltage Accuracy
- Programmable Current Limit up to 1.5A
- Charge Current Thermal Foldback
- Accepts Multiple Types of Adapters
- Guaranteed operation down to VIN = 2.65V after start up
- Ambient Temperature Range: -20°C to 70°C
- Thermally-Enhanced DFN Packages
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Handheld Devices including Medical Handhelds
- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Self-Charging Battery Packs
- Stand-Alone Chargers
- USB Bus-Powered Chargers

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

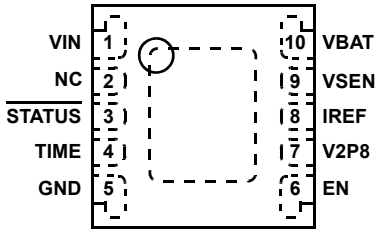
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG DWG. #
ISL9203CRZR5220	03CZ	-20 to 70	10 Ld 3x3 DFN	L10.3x3
ISL9203CRZ-TR5220	10 Ld 3x3 DFN Tape and Reel			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL9203R5220
(3x3 DFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . -0.3 to 7V
Output Pin Voltage (BAT, VSEN, V2P8). . . . . -0.3 to 5.5V
Signal Input Voltage (TIME, IREF). . . . . -0.3 to 3.2V
Output Pin Voltage (STATUS) . . . . . -0.3 to 7V
Charge Current 1.6A
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . .4500V
Machine Model (Per EIAJ ED-4701 Method C-111). 200V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x3 DFN Package	46	4

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Recommended Operating Conditions

Ambient Temperature Range. . . . . -20°C to 70°C
Supply Voltage, VIN. . . . . 4.3V to 6.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising VIN Threshold			3.0	3.4	4.0	V
Falling VIN Threshold			2.3	2.4	2.65	V
STANDBY CURRENT						
VBAT Pin Sink Current	$I_{STANDBY}$	VIN floating or EN = LOW	-	-	3.0	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN pulled low	-	30	250	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN floating	-	1	2	mA
VOLTAGE REGULATION						
Output Voltage	V_{CH}		4.158	4.20	4.242	V
Dropout Voltage		VBAT = 3.7V, Charge current = 1A	-	320	550	mV
CHARGE CURRENT						
Constant Charge Current (Note 3)	I_{CHARGE}	R_{IREF} = 80kΩ, V_{BAT} = 3.7V	0.9	1.0	1.1	A
Constant Charge Current	I_{CHARGE}	R_{IREF} = 1.21MΩ, V_{BAT} = 3.7V	33	66	100	mA
Trickle Charge Current	$I_{TRICKLE}$	R_{IREF} = 80kΩ, V_{BAT} = 2.0V	85	110	135	mA
Trickle Charge Current	$I_{TRICKLE}$	R_{IREF} = 1.21MΩ, V_{BAT} = 2.0V	2	7	15	mA
End-of-Charge Threshold	I_{MIN}	R_{IREF} = 80kΩ	85	110	135	mA
End-of-Charge Threshold	I_{MIN}	R_{IREF} = 1.21MΩ	2	-	30	mA
RECHARGE THRESHOLD						
Recharge Voltage Threshold	V_{RECHRG}		3.85	4.00	4.10	V
TRICKLE CHARGE THRESHOLD						
Trickle Charge Threshold Voltage	V_{MIN}		2.7	2.8	3.0	V

Electrical Specifications Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V2P8 PIN VOLTAGE						
V2P8 Pin Voltage	V_{V2P8}		2.7	2.9	3.1	V
TEMPERATURE MONITORING						
Charge Current Foldback Threshold (Note 4)	T_{FOLD}		-	100	-	°C
Current Foldback Gain (Note 5)	G_{FOLD}		-	100	-	mA/°C
OSCILLATOR						
Oscillation Period	T_{OSC}	C_{TIME} = 15nF	2.4	3.0	3.6	ms
LOGIC OUTPUTS						
STATUS Logic Low Sink Current		Pin Voltage = 0.8V	5	-	-	mA
STATUS Leakage Current		$V_{VIN} = V_{STATUS}$ = 5V	-	-	1	µA
EN Input Logic High			2.0	-	3.3	V
EN Input Logic Low			-	-	0.8	V
EN Pin Current When Driven Low			-	-	100	µA

NOTES:

3. The accuracy includes all errors except the programming resistance tolerance. The actual charge current may be affected by the thermal foldback function if the thermal dissipation capability is not enough or by the on resistance of the power MOSFET if the charger input voltage is too close to the output voltage.
4. Guaranteed by design and characterization to be typically 100°C ±15%
5. Guaranteed by design and characterization.

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, $R_{IREF} = R_{IMIN}$ = 80kΩ, V_{BAT} = 3.7V, unless otherwise noted.

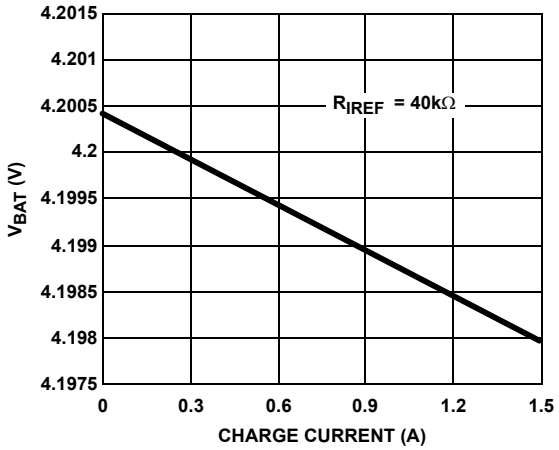


FIGURE 1. CHARGER OUTPUT VOLTAGE vs CHARGE CURRENT

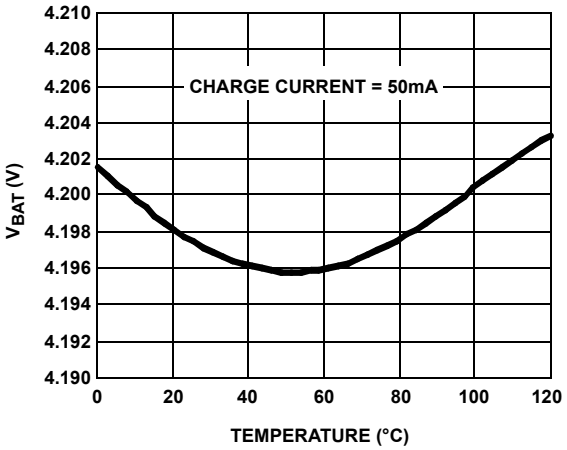


FIGURE 2. CHARGER OUTPUT VOLTAGE vs TEMPERATURE

Typical Operating Performance The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, unless otherwise noted. **(Continued)**

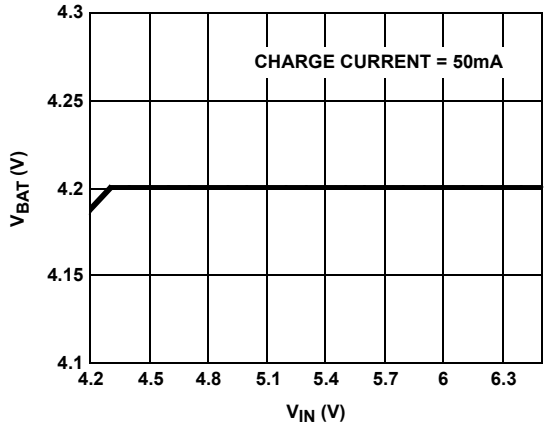


FIGURE 3. CHARGER OUTPUT VOLTAGE vs INPUT VOLTAGE CHARGE CURRENT IS 50mA

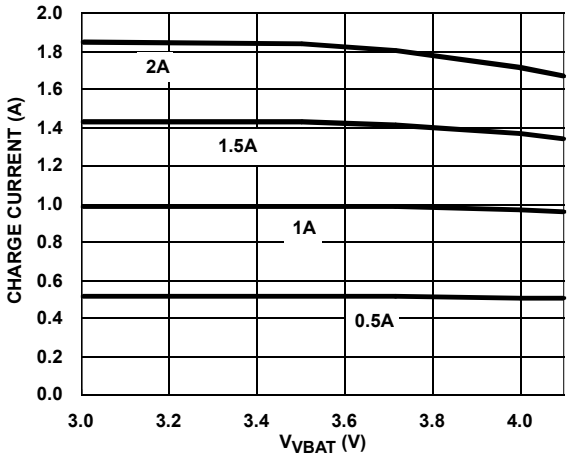


FIGURE 4. CHARGE CURRENT vs OUTPUT VOLTAGE

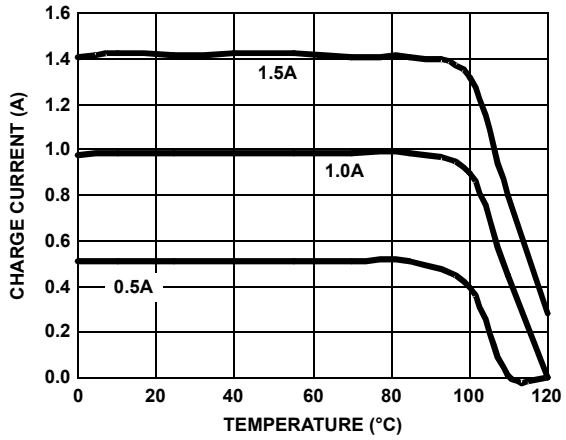


FIGURE 5. CHARGE CURRENT vs AMBIENT TEMPERATURE

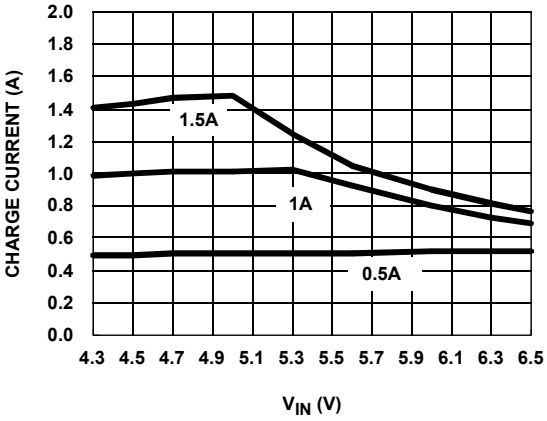


FIGURE 6. CHARGE CURRENT vs INPUT VOLTAGE

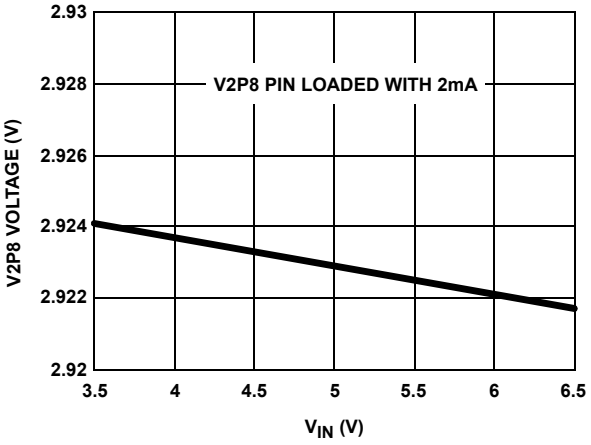


FIGURE 7. V2P8 OUTPUT vs INPUT VOLTAGE

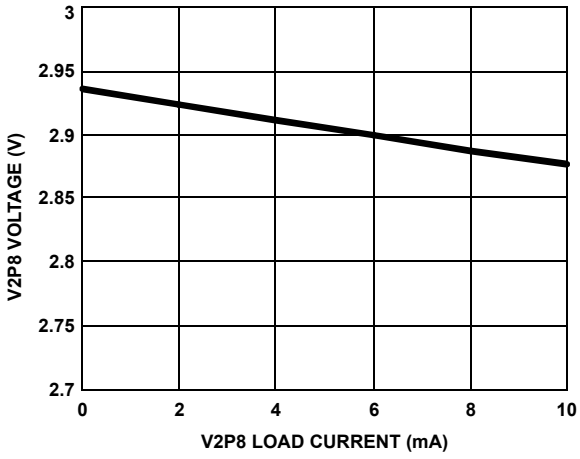


FIGURE 8. V2P8 OUTPUT vs ITS LOAD CURRENT

Typical Operating Performance The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, $R_{IREF} = R_{IMIN}$ = 80kΩ, V_{BAT} = 3.7V, unless otherwise noted. **(Continued)**

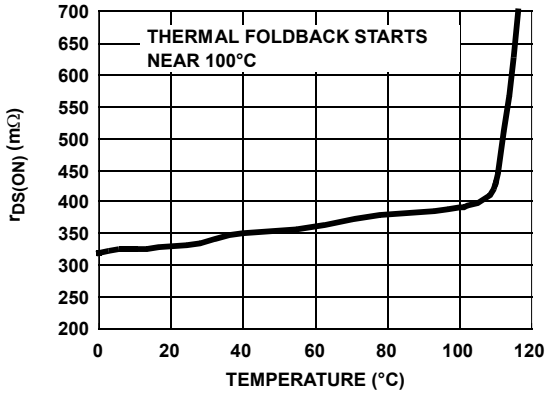


FIGURE 9. $r_{DS(ON)}$ vs TEMPERATURE AT 3.7V OUTPUT

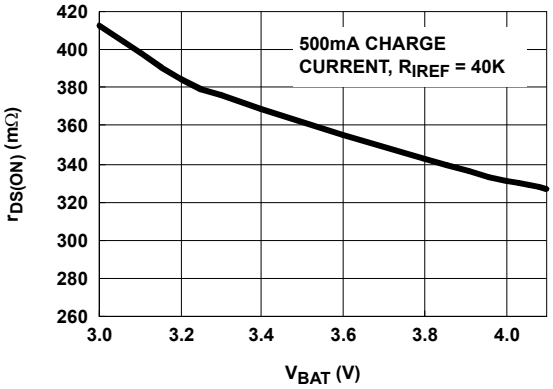


FIGURE 10. $r_{DS(ON)}$ vs OUTPUT VOLTAGE USING CURRENT LIMITED ADAPTERS

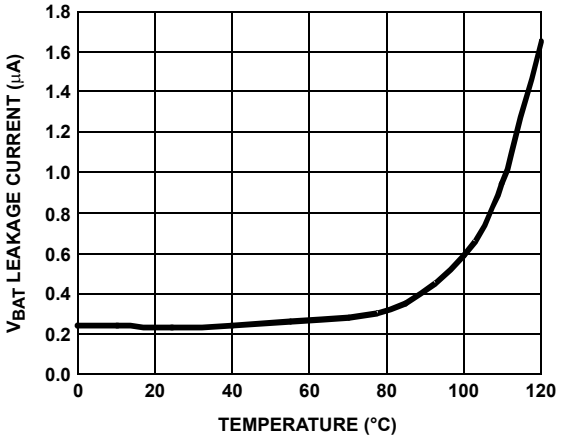


FIGURE 11. REVERSE CURRENT vs TEMPERATURE

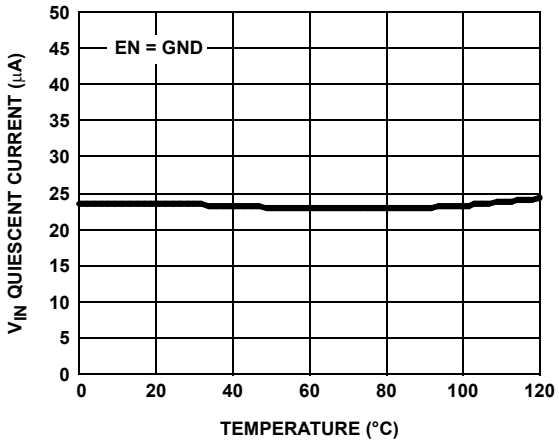


FIGURE 12. INPUT QUIESCENT CURRENT vs TEMPERATURE

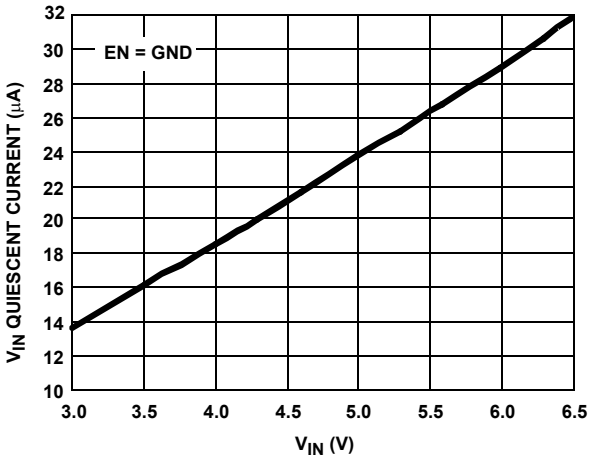


FIGURE 13. INPUT QUIESCENT CURRENT vs INPUT VOLTAGE WHEN SHUTDOWN

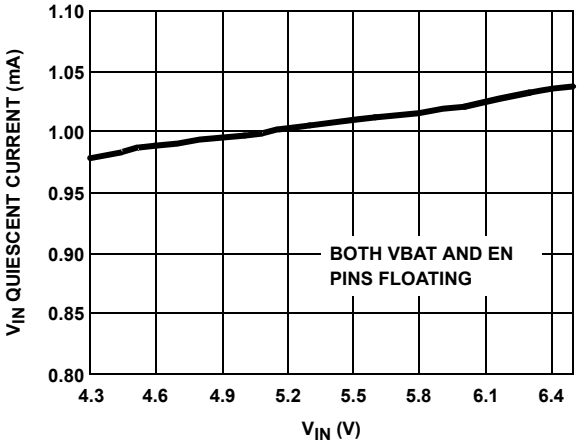


FIGURE 14. INPUT QUIESCENT CURRENT vs INPUT VOLTAGE WHEN NOT SHUTDOWN

Typical Operating Performance The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, unless otherwise noted. **(Continued)**

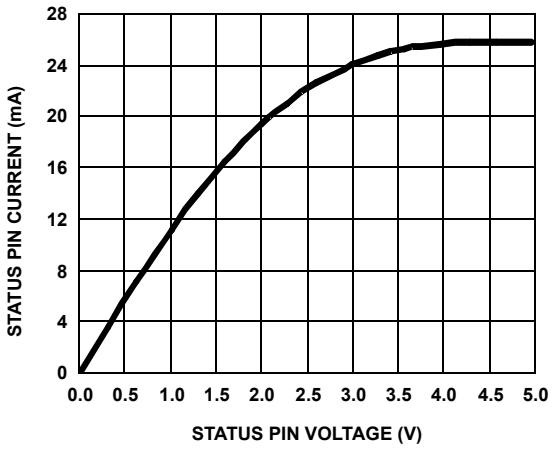


FIGURE 15. STATUS PIN VOLTAGE vs CURRENT WHEN THE OPEN-DRAIN MOSFET TURNS ON

Pin Descriptions

VIN (Pin1)

VIN is the input power source. Connect to a wall adapter.

NC (Pin 2)

No connection for this pin.

STATUS (Pin 3)

STATUS is an open-drain output indicating charging and inhibit states. The STATUS pin is pulled LOW when the charger is charging a battery. It will be forced to high impedence when the charge current drops to I_{MIN}. This high impedence mode will be latched until a recharge cycle or a new charge cycle starts.

TIME (Pin 4)

The TIME pin determines the oscillation period by connecting a timing capacitor between this pin and GND. The oscillator also provides a time reference for the charger.

GND (Pin 5)

GND is the connection to system ground.

EN (Pin 6)

EN is the enable logic input. Connect the EN pin to LOW to disable the charger or leave it floating to enable the charger.

V2P8 (Pin 7)

This is a 2.8V reference voltage output. This pin outputs a 2.8V voltage source when the input voltage is above POR threshold, otherwise it outputs zero. The V2P8 pin can be used as an indication for adapter presence.

IREF (Pin 8)

This is the programming input for the constant charging current. It maintains at 0.8V when the charger is in normal operation.

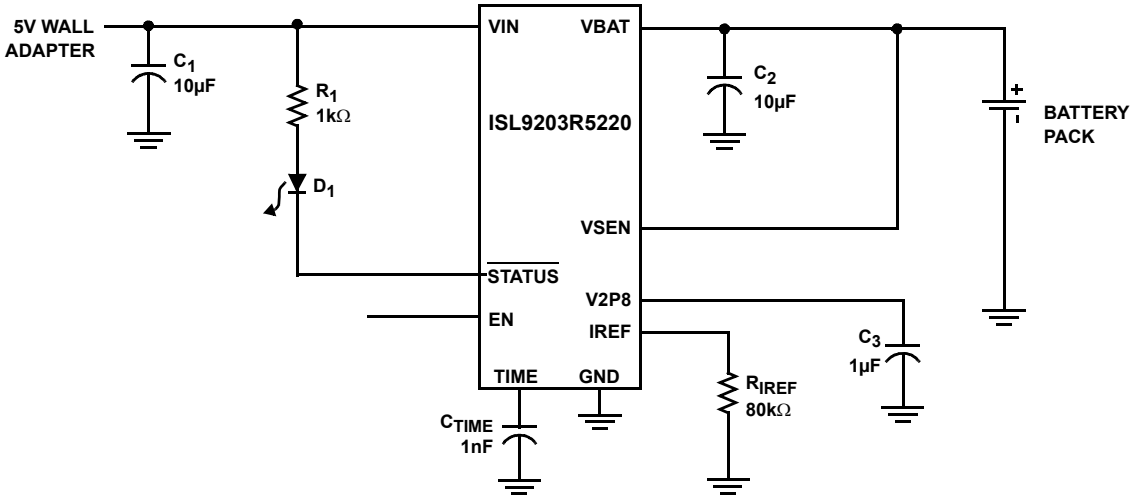
VSEN (Pin 9)

VSEN is the remote voltage sense pin. Connect this pin as close as possible to the battery pack positive connection. If the VSEN pin is floating, its voltage drops to zero volt and the charger operates in the trickle mode.

VBAT (Pin 10)

VBAT is the connection to the battery. Typically a 10µF Tantalum capacitor is needed for stability when there is no battery attached. When a battery is attached, only a 0.1µF ceramic capacitor is required.

Typical Applications



Block Diagram

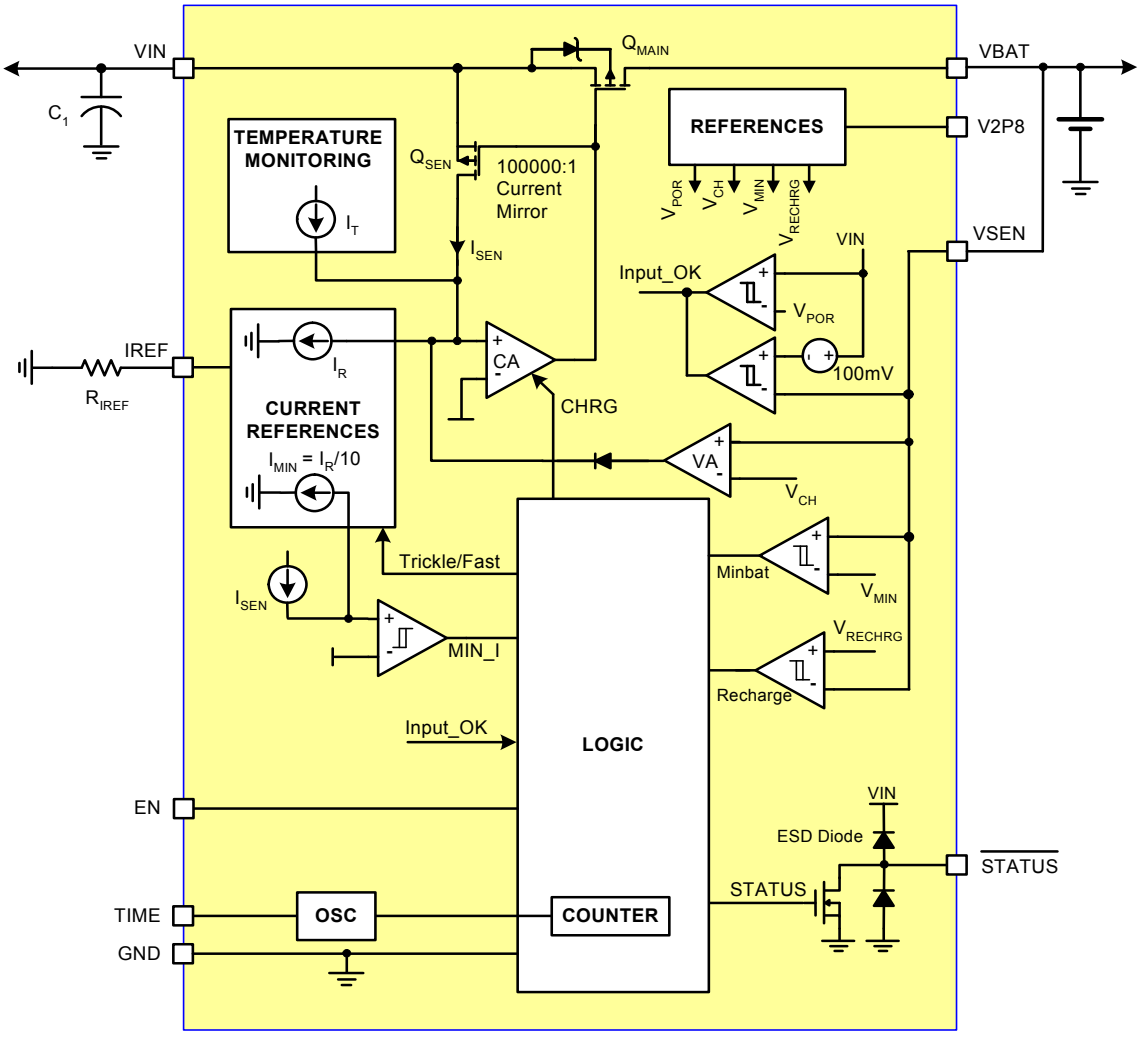


FIGURE 16. BLOCK DIAGRAM

Charging Flow Chart

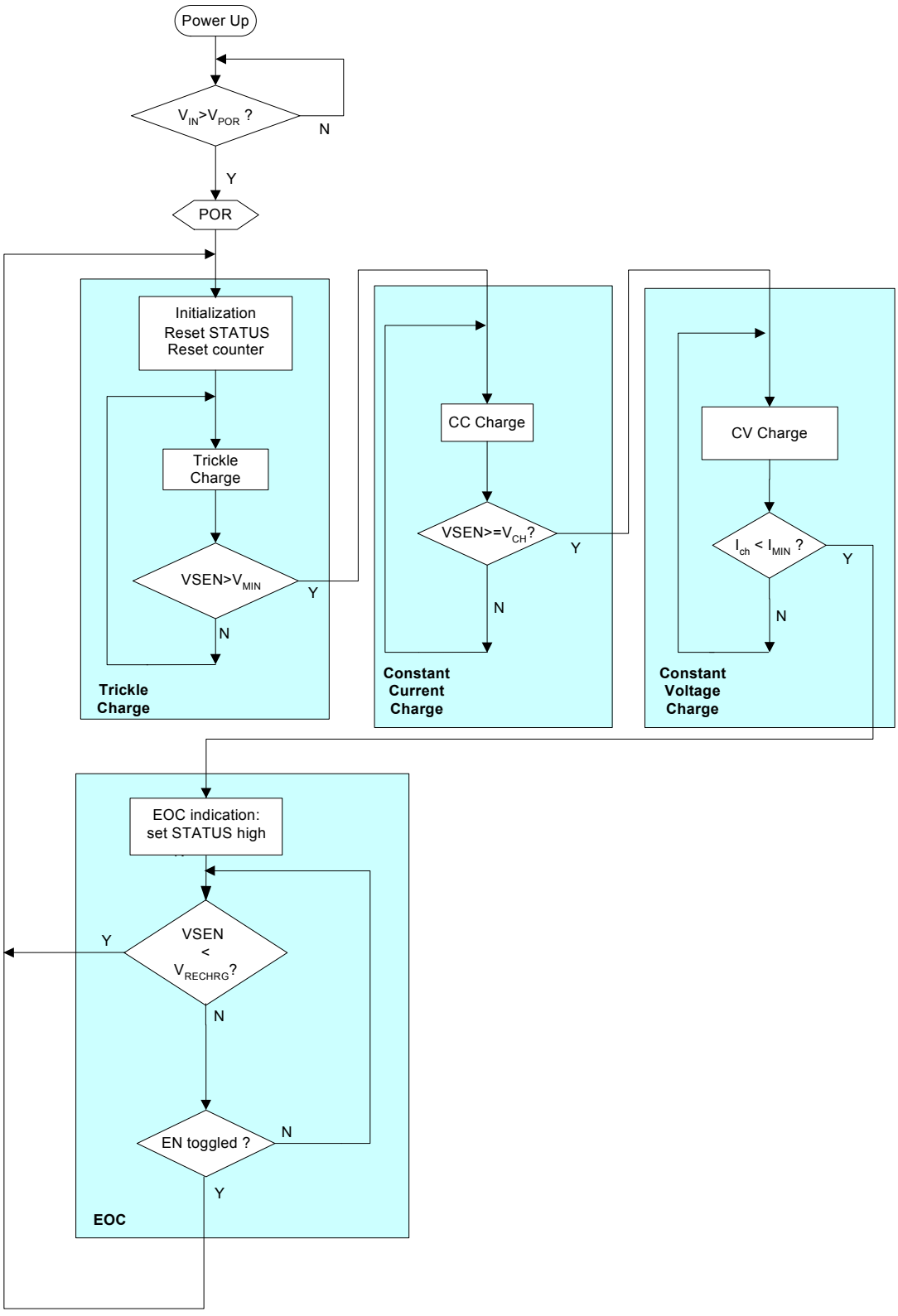


FIGURE 17. CHARGING STATE DIAGRAM

Theory of Operation

The ISL9203R5220 is an integrated charger for single-cell Li-ion or Li-polymer batteries. The ISL9203R5220 functions as a traditional linear charger when powered with a voltage-source adapter. When powered with a current-limited adapter, the charger minimizes the thermal dissipation commonly seen in traditional linear chargers.

As a linear charger, the ISL9203R5220 charges a battery in the popular constant current (CC) and constant voltage (CV) profile. The constant charge current I_{REF} is programmable up to 1.5A with an external resistor. The charge voltage V_{CH} has 1% accuracy over the entire recommended operating condition range. The charger always preconditions the battery with 10% of the programmed current at the beginning of a charge cycle, until the battery voltage is verified to be above the minimum fast charge voltage, V_{MIN}. This low-current preconditioning charge mode is named trickle mode. The verification takes 15 cycles of an internal oscillator whose period is programmable with the timing capacitor.

A thermal-foldback feature removes the thermal concern typically seen in linear chargers. The charger reduces the charge current automatically as the IC internal temperature rises above 100°C to prevent further temperature rise. The thermal-foldback feature guarantees safe operation when the printed circuit board (PCB) is space limited for thermal dissipation.

Two indication pins are available from the charger to indicate the charge status. The V2P8 outputs a 2.8V DC voltage when the input voltage is above the power-on reset (POR) level and can be used as a power-present indication. This pin is capable of sourcing a 2mA current, so it can also be used to bias external circuits. The STATUS pin is an open-drain logic output that goes LOW at the beginning of a charge cycle and stays LOW until the end-of-charge (EOC) condition is qualified. The EOC condition is met when the battery voltage rises above a recharge threshold and the charge current falls below an EOC current threshold. Once the EOC condition is qualified, the STATUS output goes HIGH and is latched. The latch is released at the beginning of a re-charge cycle, when the EN is toggled, or after the chip is power cycled.

If the ISL9203R5220 has not been power cycled and has not had the EN pin toggled, but the VSEN voltage drops below the recharge level, then the device re-enters the charge mode. In this condition, the charger indicates a re-charge cycle by bringing the STATUS pin LOW.

When the wall adapter is not present, the ISL9203R5220 draws less than 1µA of current from the battery.

Figure 18 shows the typical charge curves in a traditional linear charger powered with a constant-voltage adapter. From the top to bottom, the curves represent the constant input voltage, the battery voltage, the charge current and the power dissipation in the charger. The power dissipation P_{CH} is given by the following equation:

$$P_{CH} = (V_{IN} - V_{BAT}) \cdot I_{CHARGE} \quad \text{(EQ. 1)}$$

where I_{CHARGE} is the charge current. The maximum power dissipation occurs during the beginning of the CC mode. The maximum power the IC is capable of dissipating is dependent on the thermal impedance of the printed-circuit board (PCB). Figure 18 shows, with dotted lines, two cases that the charge currents are limited by the maximum power dissipation capability due to the thermal foldback.

When using a current-limited adapter, the thermal situation in the ISL9203R5220 is totally different. Figure 19 shows the typical charge curves when a current-limited adapter is employed. The operation requires the I_{REF} to be programmed higher than the limited current I_{LIM} of the adapter, as shown in Figure 19. The key difference of the charger operating under such conditions occurs during the CC mode.

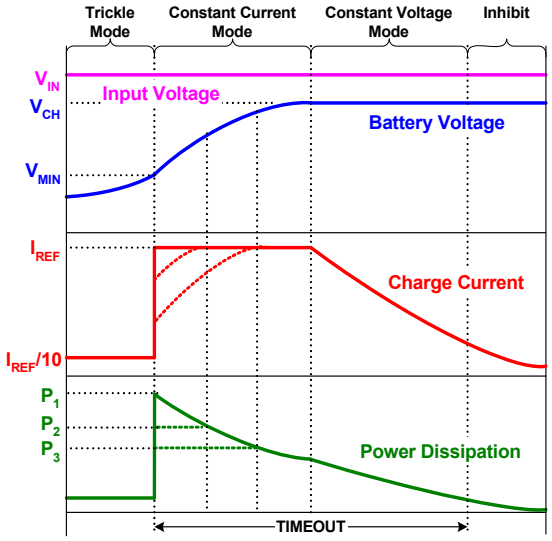


FIGURE 18. TYPICAL CHARGE CURVES USING A CONSTANT-VOLTAGE ADAPTER

The Block Diagram, Figure 16, aids in understanding the operation. The current loop consists of the current amplifier CA and the sense MOSFET Q_{SEN}. The current reference I_R is programmed by the IREF pin. The current amplifier CA regulates the gate of the sense MOSFET Q_{SEN} so that the sensed current I_{SEN} matches the reference current I_R. The main MOSFET Q_{MAIN} and the sense MOSFET Q_{SEN} form a current mirror with a ratio of 100,000:1, that is, the output charge current is 100,000 times I_R.

In the CC mode, the current loop tries to increase the charge current by enhancing the sense MOSFET Q_{SEN}, so that the sensed current matches the reference current. On the other hand, the adapter current is limited, the actual output current will never meet what is required by the current reference. As a result, the current error amplifier CA keeps enhancing the Q_{SEN} as well as the main MOSFET Q_{MAIN}, until they are fully turned on. Therefore, the main MOSFET becomes a power switch instead of a linear regulation device. The power dissipation in the CC mode becomes:

$$P_{CH} = R_{DS(ON)} \cdot I_{CHARGE}^2 \quad \text{(EQ. 2)}$$

where $R_{DS(ON)}$ is the resistance when the main MOSFET is fully turned on. This power is typically much less than the peak power in the traditional linear mode.

The worst power dissipation when using a current-limited adapter typically occurs at the beginning of the CV mode, as shown in Figure 19. The equation 1 applies during the CV mode. When using a very small PCB whose thermal impedance is relatively large, it is possible that the internal temperature can still reach the thermal foldback threshold. In that case, the IC is thermally protected by lowering the charge current, as shown by the dotted lines in the charge current and power curves. Appropriate design of the adapter can further reduce the peak power dissipation of the ISL9203R5220. See the Application Information section of the ISL6292 data sheet (www.intersil.com) for more information.

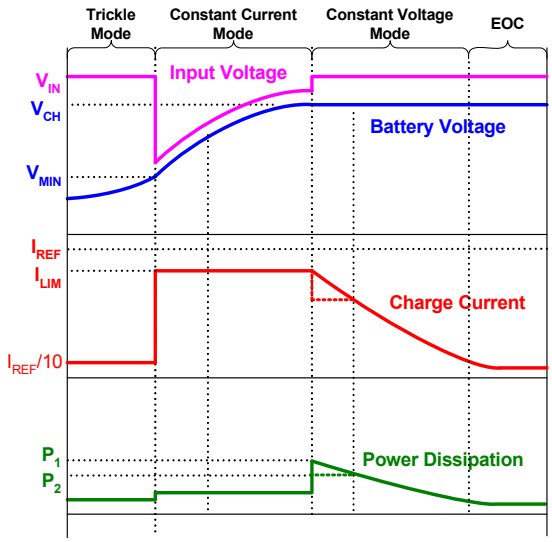


FIGURE 19. TYPICAL CHARGE CURVES USING A CURRENT-LIMITED ADAPTER

Figure 20 illustrates the typical signal waveforms for the linear charger from the power-up to a recharge cycle. More detailed Applications Information is given below.

Applications Information

Power on Reset (POR)

The ISL9203R5220 resets itself as the input voltage rises above the POR rising threshold. The V2P8 pin outputs a 2.8V voltage, the internal oscillator starts to oscillate, the internal timer is reset, and the charger begins to charge the battery. The STATUS pin indicates a LOW logic signal. Figure 20 illustrates the start up of the charger between t_0 to t_2.

The ISL9203R5220 has a typical rising POR threshold of 3.4V and a falling POR threshold of 2.4V. The 2.4V falling threshold guarantees charger operation with a current-limited adapter to minimize the thermal dissipation.

Charge Cycle

A charge cycle consists of three charge modes: trickle mode, constant current (CC) mode, and constant voltage (CV) mode. The charge cycle always starts with the trickle mode until the battery voltage stays above V_{MIN} (2.8V typical) for 15 consecutive cycles of the internal oscillator. If the battery voltage drops below V_{MIN} during the 15 cycles, the 15-cycle counter is reset and the charger stays in the trickle mode. The charger moves to the CC mode after verifying the battery voltage is above V_{MIN}.

When the battery-pack terminal voltage rises to the final charge voltage V_{CH}, the CV mode begins. The terminal voltage is regulated at the constant V_{CH} in the CV mode and the charge current declines. After the charge current drops below I_{MIN} (1/10 of I_{REF}, see Section “End-of-Charge (EOC) Current” for more detail) the ISL9203R5220 indicates the end-of-charge with the STATUS pin. The charging operation does not terminate. Signals in a charge cycle are illustrated in Figure 20 between points t_2 to t_5.

The end of charge indicator (STATUS) will not be set if the charging current is below I_{MIN} within the first 16 cycles after V_{BAT} exceeds the V_{RECHRG} voltage. If the charge current is still below I_{MIN} after these 16 cycles, STATUS goes high to indicate end of charge.

The following events initiate a new charge cycle:

- POR,
- the battery voltage drops below a recharge threshold,
- or, the EN pin is toggled from GND to floating.

Further description of these events are given later in this data sheet.

Recharge

After a charge cycle completes, the charger continues to regulate the output at the constant voltage; but the STATUS pin indicates that the charging is completed. The STATUS pin stays high until the battery voltage drops to below the recharge threshold, V_{RECHRG} (see Electrical Specifications). Then the STATUS pin goes low and a new charge cycle starts at point t_6. The charge cycle ends at point t_7 with the STATUS pin again going high, as shown in Figure 20.

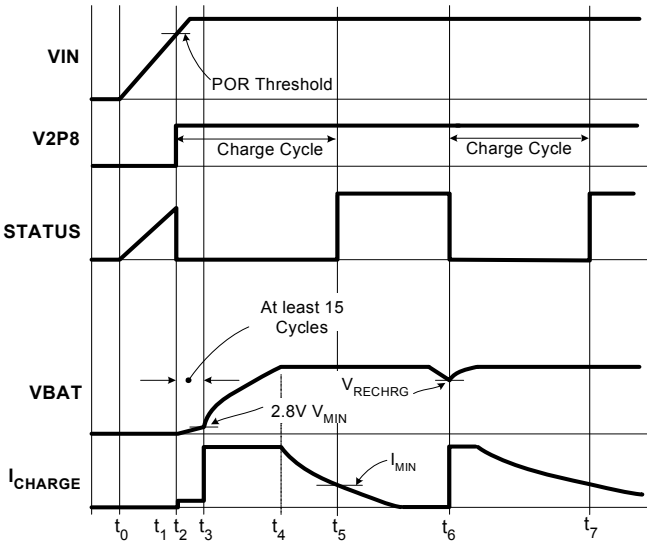


FIGURE 20. OPERATION WAVEFORMS

Internal Oscillator

The internal oscillator establishes a timing reference. The oscillation period is programmable with an external timing capacitor, C_{TIME}, as shown in Typical Applications. The oscillator charges the timing capacitor to 1.5V and then discharges it to 0.5V in one period, both with 10µA current. The period T_{OSC} is:

$$T_{OSC} = 0.2 \cdot 10^6 \cdot C_{TIME} \quad (\text{seconds}) \qquad \text{(EQ. 3)}$$

A 1nF capacitor results in a 0.2ms oscillation period.The accuracy of the period is mainly dependent on the accuracy of the capacitance and the internal current source.

Charge Current Programming

The charge current in the CC mode is programmed by the IREF pin. The voltage of IREF is regulated to a 0.8V reference voltage. The charging current during the constant current mode is 100,000 times that of the current in the R_{IREF} resistor. Hence, the charge current is,

$$I_{REF} = \frac{0.8V}{R_{IREF}} \times 10^5 (A) \qquad \text{(EQ. 4)}$$

Table 1 shows the charge current vs. selected R_{IREF} values. The typical trickle charge current is 10% of the programmed constant charge current. Table 2 shows the trickle charge current tolerance guidance at given R_{IREF} values, when the battery voltage is between 0V to 2.5V.

TABLE 1. CHARGE CURRENT vs R_{IREF} VALUES.

R_{IREF} (kΩ)	CHARGE CURRENT (mA)		
	MIN	TYP	MAX
267 ~ 160	17% lower than TYP Value	= I_{REF} in EQ. 5	17% higher than TYP Value
160	450	500	550
100	720	800	880
88.9	810	900	990
80	900	1000	1100

TABLE 2. TRICKLE CHARGE CURRENT vs R_{IREF} VALUES.

R_{IREF} (kΩ)	TRICKLE CHARGE CURRENT (mA)		
	MIN	TYP	MAX
267	15	30	60
160	30	50	80
100	40	80	120
88.9	45	90	135
80	70	100	150

NOTE: The values in table 2 and table 1 are not tested and are only for guidance in selecting resistor values for mass production tests or in customer's products.

End-of-Charge (EOC) Current

The EOC current I_{MIN} sets the level at which the charger starts to indicate the end of the charge with the STATUS pin, as shown in Figure 20. The charger actually does not terminate charging. In the ISL9203R5220, the EOC current is internally set to 1/10 of the CC charge current, that is,

$$I_{MIN} = \frac{1}{10} \cdot I_{REF} \qquad \text{(EQ. 5)}$$

At the EOC, the STATUS signal rises to HIGH and is latched. The latch is not reset until a recharge cycle or a new charge cycle starts. The tolerance guidance for the EOC current at selected R_{IREF} values are given in Table 3.

TABLE 3. EOC CURRENT vs R_{IREF} VALUES.

R_{IREF} (kΩ)	EOC CURRENT (mA)		
	MIN	TYP	MAX
267	15	30	60
160	30	50	80
100	40	80	120
88.9	45	90	135

TABLE 3. EOC CURRENT vs R_{IREF} VALUES.

R_{IREF} (kΩ)	EOC CURRENT (mA)		
	MIN	TYP	MAX
80	70	100	150

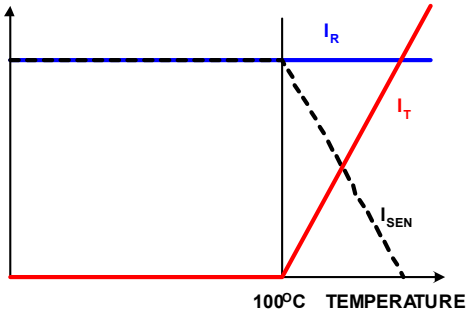


FIGURE 21. CURRENT SIGNALS AT THE AMPLIFIER CA INPUT

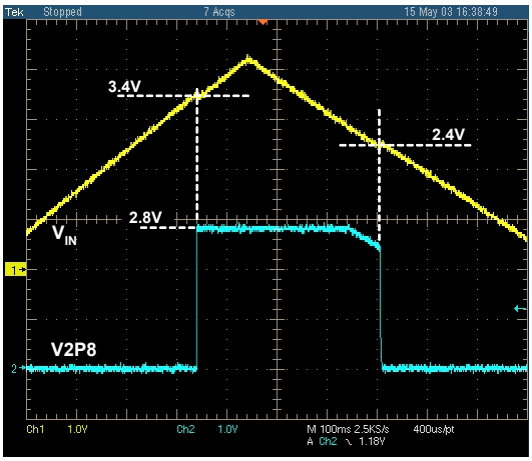


FIGURE 22. THE V2P8 PIN OUTPUT vs THE INPUT VOLTAGE AT THE VIN PIN. VERTICAL: 1V/DIV, HORIZONTAL: 100ms/DIV

NOTE: The values in table 3 are not tested and are only for guidance in selecting resistor values for mass production tests or in customer's products.

Charge Current Thermal Foldback

Over-heating is always a concern in a linear charger. The maximum power dissipation usually occurs at the beginning of a charge cycle when the battery voltage is at its minimum but the charge current is at its maximum. The charge current thermal foldback function in the ISL9203R5220 frees users from the over-heating concern.

Figure 21 shows the current signals at the summing node of the current error amplifier CA in the Block Diagram. I_R is the reference. I_T is the current from the Temperature Monitoring block. The I_T has no impact on the charge current until the internal temperature reaches approximately 100°C; then I_T rises at a rate of 1μA/°C. When I_T rises, the current control loop forces the sensed current I_{SEN} to reduce at the same rate. As a mirrored current, the charge current is 100,000 times that of the sensed current and reduces at a rate of 100mA/°C. For a charger with the constant charge current set at 1A, the charge current is reduced to zero when the internal temperature rises to 110°C. The actual charge current settles between 100°C to 110°C.

Usually the charge current should not drop below I_{MIN} because of the thermal foldback. For some extreme cases if that does happen, the charger does not indicate end-of-charge unless the battery voltage is already above the recharge threshold.

2.8V Bias Voltage

The ISL9203R5220 provides a 2.8V voltage for biasing the internal control and logic circuit. This voltage is also available for external circuits such as the NTC thermistor circuit. The maximum allowed external load is 2mA.

Indications

The ISL9203R5220 has two indications: the input presence and the charge status. The input presence is indicated by the V2P8 pin and the charge status is indicated by the STATUS pin. Figure 22 shows the V2P8 pin voltage vs. the input voltage.

STATUS Pull-Up Resistor

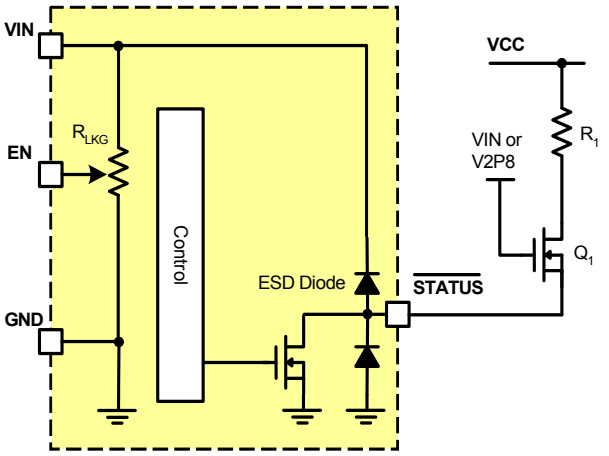
The STATUS pin is an open-drain output that need an external pull-up resistor. It is recommended that this be pulled up to the input voltage or the 2.8V from the V2P8 pin. If the STSTUS pin has to be pulled up to other voltages, the user needs to examine carefully whether or not the ESD diodes will form a leakage current path to the battery when the input power is removed. If the leakage path does exist, an external transistor is required to break the path.

Figure 23 shows the implementation. If the STATUS pin is directly pulled up to the VCC voltage (not shown in Figure 23), a current will flow from the VCC to the STATUS pin, then through the ESD diode to the VIN pin. Any leakage on the VIN pin, caused by an external or internal current path, will result in a current path from VCC to ground.

The N-channel MOSFET Q_1 buffers the STATUS pin. The gate of Q_1 is connected to VIN or the V2P8 pin. When the STATUS pin outputs a logic low signal, Q_1 is turned on and its drain outputs a low signal as well. When STATUS is high impedance, R_1 pulls the Q_1 drain to high. When the input power is removed, the Q_1 gate voltage is also removed, thus the Q_1 drain stays high.

Shutdown

The ISL9203R5220 can be shutdown by pulling the EN pin to ground. When shut down, the charger draws typically less than 30μA current from the input power and the 2.8V output at the V2P8 pin is also turned off. The EN pin needs be



Note:
R_{LKG} is approximately 240kΩ when EN is floating and is approximately 140kΩ when the EN is grounded.

FIGURE 23. PULL-UP CIRCUIT TO AVOID BATTERY LEAKAGE CURRENT IN THE ESD DIODES

driven with an open-drain or open-collector logic output, so that the EN pin is floating when the charger is enabled. If the EN pin is driven by an external source, the POR threshold voltage will be affected.

Input and Output Capacitor Selection

Typically any type of capacitors can be used for the input and the output. Use of a 0.47µF or higher value ceramic capacitor for the input is recommended. When the battery is attached to the charger, the output capacitor can be any ceramic type with the value higher than 0.1µF. However, if there is a chance the charger will be used as an LDO linear regulator, a 10µF tantalum capacitor is recommended. Note that the charger always steps through the 15-cycle V_{MIN} verification time before the charge current rises to the constant charge current, as discussed earlier. Hence, when using as an LDO, the system should make sure not to load the charger heavily until the 15-cycle verification is completed.

Working with Current-Limited Adapter

The ISL9203R5220 can work with a current-limited adapter to significantly reduce the thermal dissipation during charging. Refer to the ISL6292 data sheet, which can be found at http://www.intersil.com, for more details.

Board Layout Recommendations

The ISL9203R5220 internal thermal foldback function limits the charge current when the internal temperature reaches approximately 100°C. In order to maximize the current capability, it is very important that the exposed pad under the package is properly soldered to the board and is connected to other layers through thermal vias. More thermal vias and more copper attached to the exposed pad usually result in better thermal performance. On the other hand, the number of vias is limited by the size of the pad. The 3x3 DFN package allows 8 vias be placed in two rows. Since the pins on the 3x3 DFN package are on only two sides, as much top layer copper as possible should be connected to the exposed pad to minimize the thermal impedance. Refer to the ISL6292 evaluation boards for layout examples.

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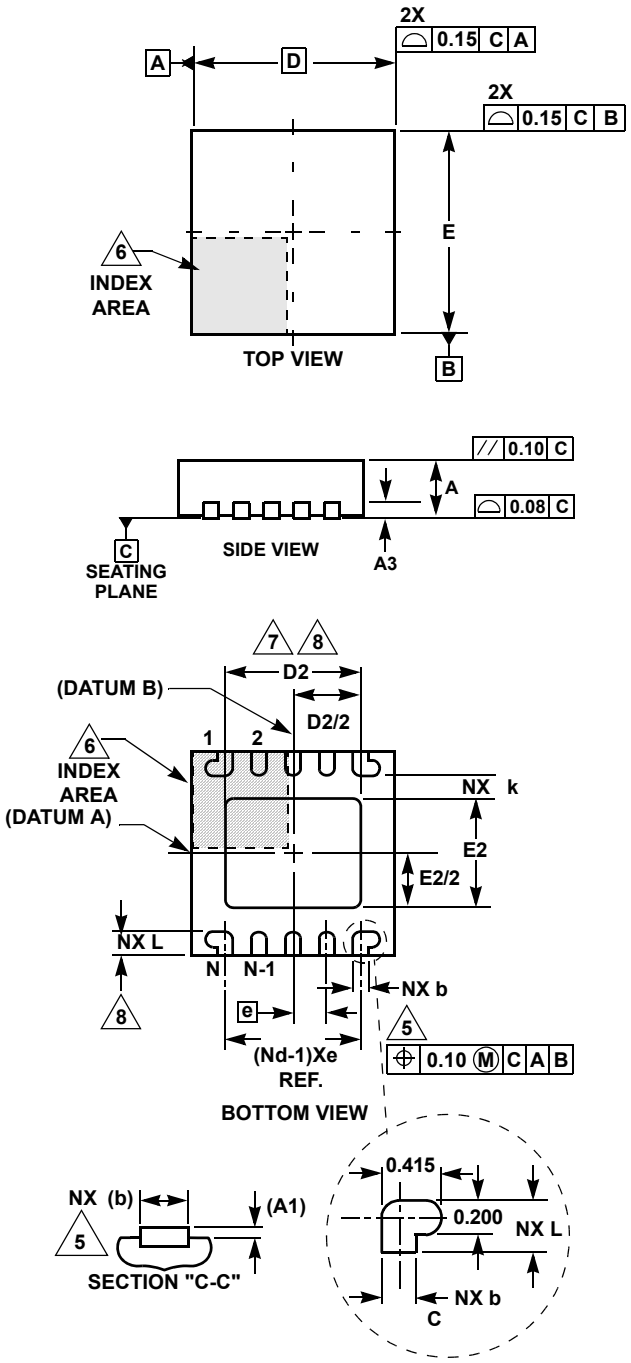
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Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

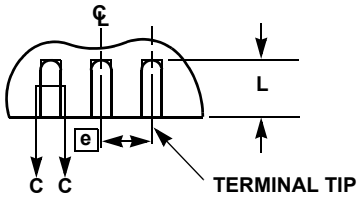
10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

Rev. 3 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE

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