InnoSwitch-CH Family

Off-Line CV/CC Flyback Switcher IC with Integrated 650 V MOSFET, Synchronous Rectification and Feedback

Product Highlights

Highly Integrated, Compact Footprint

- Incorporates flyback controller, 650 V MOSFET, secondary-side sensing and synchronous rectification driver
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Exceptional CV/CC accuracy, independent of transformer design or external components
- Instantaneous transient response ±5% CV with 0%-100%-0% load step

EcoSmart™ – Energy Efficient

- <10 mW no-load at 230 VAC when supplied by transformer bias winding
- Easily meets all global energy efficiency regulations
- Low heat dissipation

Advanced Protection / Safety Features

- Primary sensed output OVP
- Secondary sensed output overshoot clamp
- Secondary sensed output OCP to zero output voltage
- Hysteretic thermal shutdown

Full Safety and Regulatory Compliance

- 100% production HIPOT compliance testing equivalent to 6 kV DC/1 sec
- Reinforced insulation
- Isolation voltage >3,500 VAC
- UL1577 and TUV (EN60950 and EN62368) safety approved
- EN61000-4-8 (100 A/m) and EN61000-4-9 (1000 A/m) compliant

Green Package

- Halogen free and RoHS compliant

Applications

- Chargers and adapters for smart mobile devices
- High efficiency, low voltage, high current power supplies

Description

The InnoSwitch™-CH family of ICs dramatically simplifies the development and manufacturing of low-voltage, high current power supplies, particularly those in compact enclosures or with high efficiency requirements. The InnoSwitch-CH architecture is revolutionary in that the devices incorporate both primary and secondary controllers, with sense elements and a safety-rated feedback mechanism into a single IC.

Close component proximity and innovative use of the integrated communication link permit accurate control of a secondary-side synchronous rectification MOSFET and optimization of primary-side switching to maintain high efficiency across the entire load range. Additionally, the minimal DC bias requirements of the link enables the system to achieve less than 10 mW no-load in challenging applications such as smart-mobile device chargers.

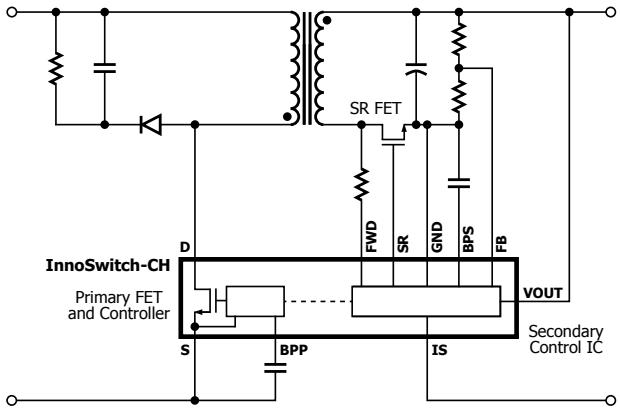


Figure 1. Typical Application/Performance.



Figure 2. High Creepage, Safety-Compliant eSOP Package.

Output Power Table

Product[3,4]	85-265 VAC	
	Adapter[1]	Peak or Open Frame[2]
INN20x3K	12 W	15 W
INN20x4K	15 W	20 W
INN20x5K	20 W	25 W

Table 1. Output Power Table.

Notes:

1. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < = 125 °C.
2. Minimum peak power capability.
3. Package: eSOP-R16B.
4. x = 0 (No cable compensation), x = 2 (6% cable compensation).

This Product is Covered by Patents and/or Pending Patent Applications.

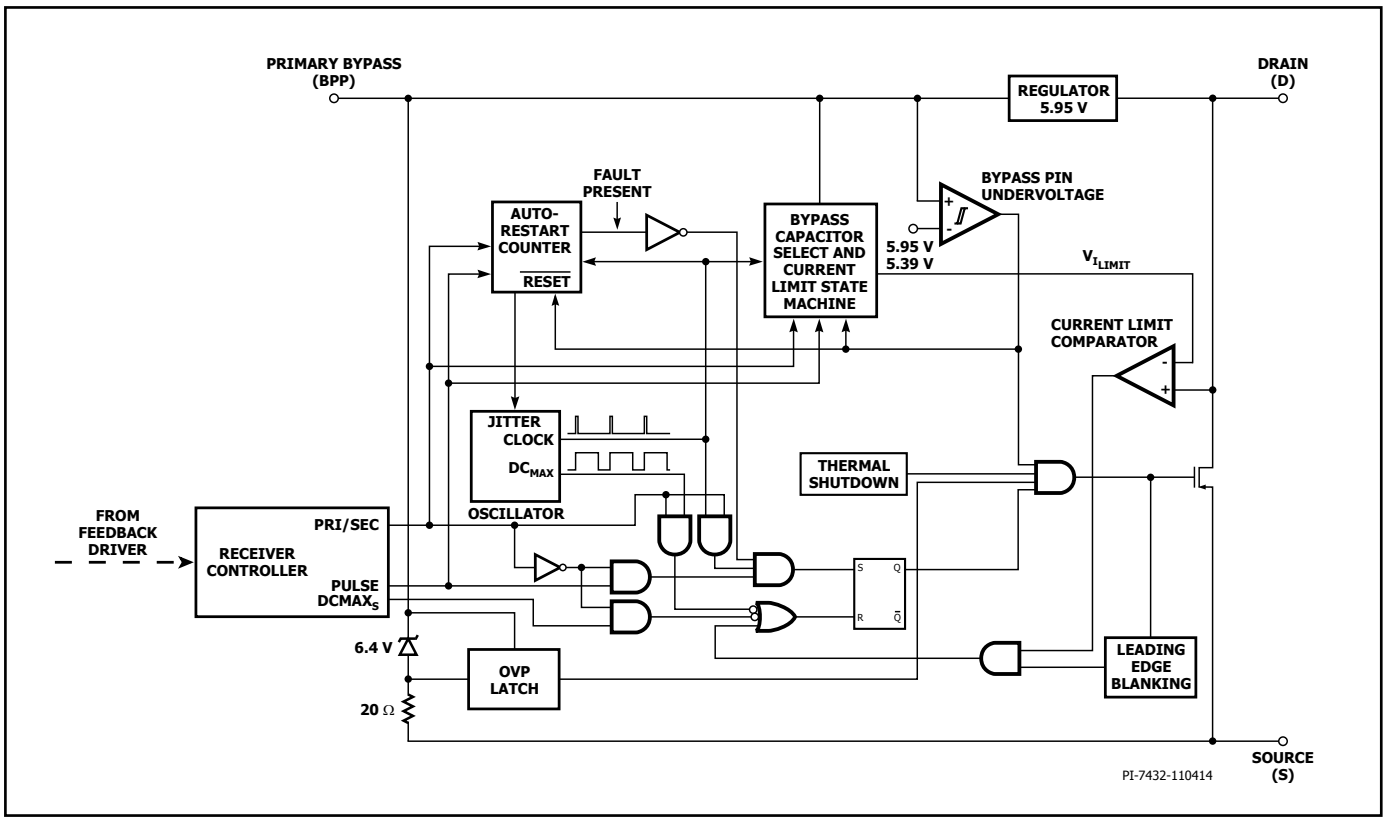


Figure 3. Primary-Side Controller Block Diagram.

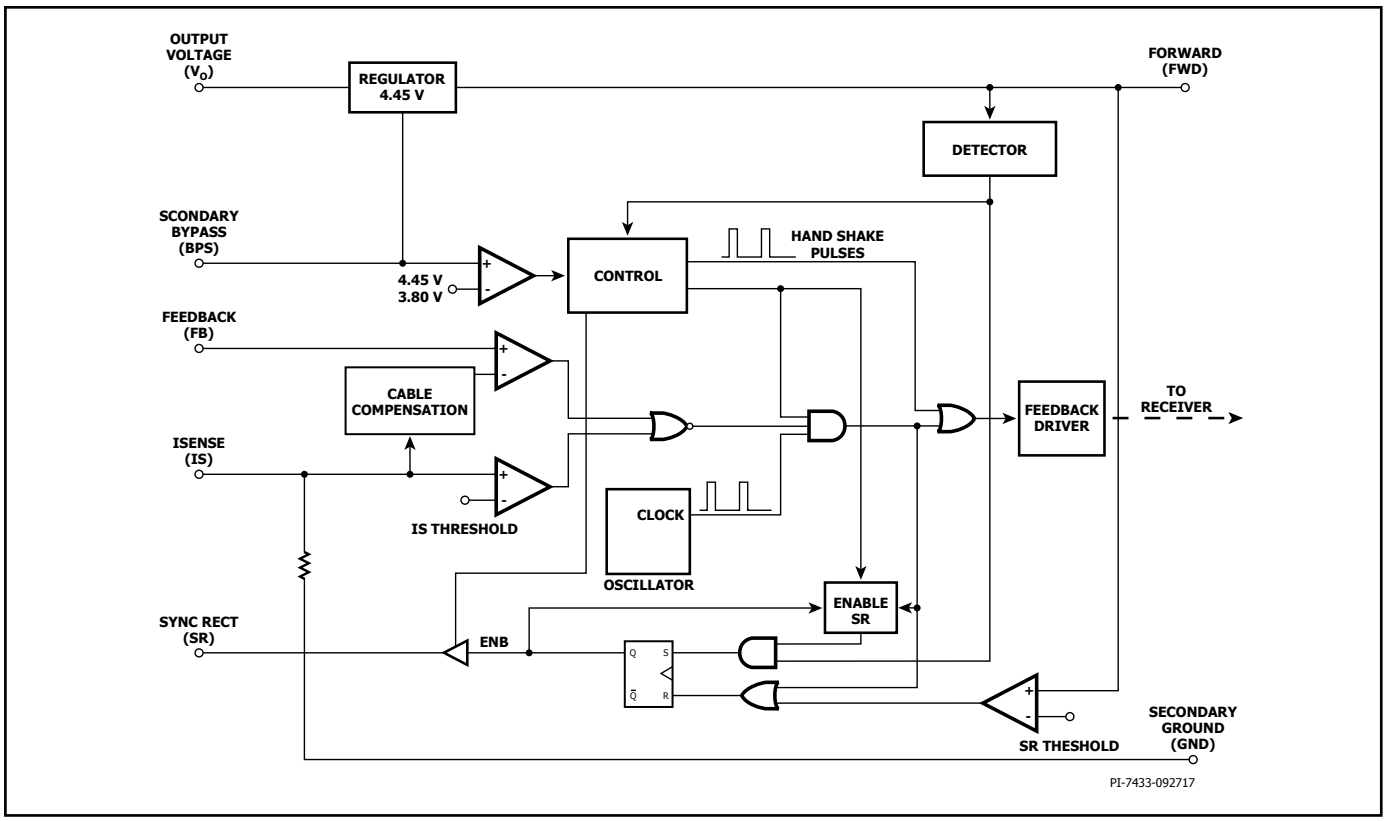


Figure 4. Secondary-Side Controller Block Diagram.

Pin Functional Description

DRAIN (D) Pin (Pin 1)
This pin is the power MOSFET drain connection.

SOURCE (S) Pin (Pin 3-6)
This pin is the power MOSFET source connection. It is also the ground reference for the PRIMARY BYPASS pin.

PRIMARY BYPASS (BPP) Pin (Pin 7)
It is the connection point for an external bypass capacitor for the primary IC supply.

NO CONNECTION (NC) Pin (Pin 8)
This pin should be left open or tied to PRIMARY BYPASS pin.

NO CONNECTION (NC) Pin (Pin 9)
This pin should be left open.

FORWARD (FWD) Pin (Pin 10)
The connection point to the switching node of the transformer output winding for sensing and other functions.

OUTPUT VOLTAGE (VOUT) Pin (Pin 11)
This pin is connected directly to the output voltage of the power supply to provide bias to the secondary IC.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 12)
Connection to external SR FET gate terminal.

SECONDARY BYPASS (BPS) Pin (Pin 13)
It is the connection point for an external bypass capacitor for the secondary IC supply.

FEEDBACK (FB) Pin (Pin 14)
This pin connects to an external resistor divider to set the power supply CV voltage regulation threshold.

SECONDARY GROUND (GND) (Pin 15)
Ground connection for the secondary IC.

ISENSE (IS) Pin (Pin 16)
Connection to the power supply output terminals. Internal current sense is connected between this pin and the SECONDARY GROUND pin.

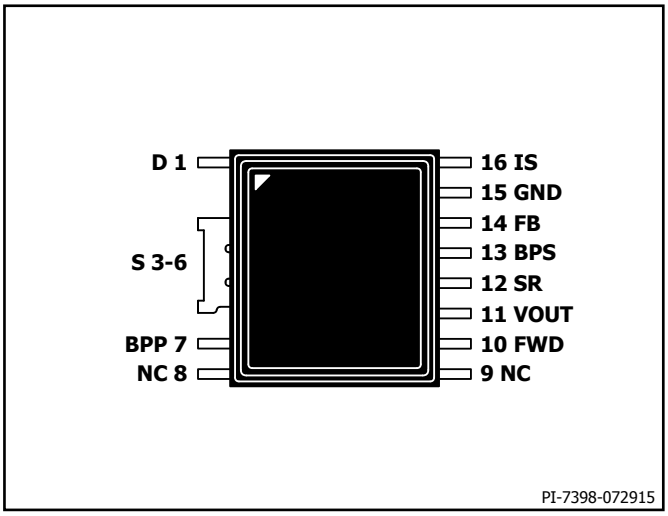


Figure 5. Pin Configuration.

InnoSwitch-CH Functional Description

The InnoSwitch-CH combines a high-voltage power MOSFET switch and both primary-side and secondary-side controllers in one device. The feedback scheme using a proprietary FluxLink coupling scheme using the package lead frame and bond wires to provide a reliable and low-cost means to provide accurate direct sensing of the output voltage and output current on the secondary to communicate information to the primary IC. Unlike conventional PWM (pulse width modulated) controllers, it uses a simple ON/OFF control to regulate the output voltage and current. The primary controller consists of an oscillator, a receiver circuit magnetically coupled to the secondary controller, current limit state machine, 5.95 V regulator on the PRIMARY BYPASS pin, overvoltage circuit, current limit selection circuitry, over temperature protection, leading edge blanking and a 650 V power MOSFET. The InnoSwitch-CH secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, constant voltage (CV) and constant current (CC) control circuitry, a 4.45 V regulator on the SECONDARY BYPASS pin, synchronous rectifier MOSFET driver, frequency jitter oscillator and a host of integrated protection features. Figures 3 and 4 show the functional block diagrams of the primary and secondary controllers with the most important features.

PRIMARY BYPASS Pin Regulator
The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the voltage on the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor. Extremely low power consumption of the internal circuitry allows the InnoSwitch-CH to operate continuously from current it takes from the DRAIN pin.

In addition, there is a shunt regulator clamping the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This facilitates powering the InnoSwitch-CH externally through a bias winding to decrease the no-load consumption to less than 10 mW (5 V output design).

PRIMARY BYPASS Pin Capacitor Selection
The PRIMARY BYPASS pin can use a ceramic capacitor as small as 0.1 μF for decoupling the internal power supply of the device. A larger capacitor size can be used to adjust the current limit. A 1 μF capacitor on the PRIMARY BYPASS pin will select a higher current limit equal to the standard current of the next larger device. A 10 μF capacitor on the PRIMARY BYPASS pin selects a lower current limit equal to the standard current limit of the next smaller device

PRIMARY BYPASS Pin Undervoltage Threshold
The PRIMARY BYPASS pin undervoltage circuitry disables the power MOSFET when the PRIMARY BYPASS pin voltage drops below V_{BPP}-$V_{BPP(H)}$ in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise back above V_{BPP} to enable switching the power MOSFET.

PRIMARY BYPASS Pin Output Overvoltage Latching Function
The PRIMARY BYPASS pin has an OV protection latching feature. A Zener diode in parallel to the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding to activate this protection mechanism. In the event the current into the PRIMARY BYPASS pin exceeds (I_{SD}) the device will disable the power MOSFET switching. The latching condition is reset by bringing the primary bypass below the reset threshold voltage ($V_{BPP(RESET)}$).

Over-Temperature Protection
The thermal shutdown circuitry senses the primary die temperature. This threshold is set to 142 °C with 75 °C hysteresis. When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled. A large hysteresis of 75 °C is provided to prevent over-heating of the PC board due to continuous fault condition.

Current Limit Operation
The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that switch cycle. The current limit state-machine reduces the current limit threshold by discrete amounts under medium and light loads.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned-on. This leading edge blanking time has been set so that current spikes caused by capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse. Each switching cycle is terminated when the Drain current of the primary power MOSFET reaches the current limit of the device.

Auto-Restart
In the event of a fault condition such as output overload, output short-circuit or external component/pin fault, the InnoSwitch-CH enters into auto-restart (AR) operation. In auto-restart operation the power MOSFET switching is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart after the secondary has taken control:

1. Continuous switching requests from the secondary for time period exceeding t_{AR}.
2. No requests for switching cycles from the secondary for a time period exceeding $t_{AR(SK)}$.

The first condition corresponds to a condition wherein the secondary controller makes continuous cycle requests without a skipped-cycle for more than t_{AR} time period. The second method was included to ensure that if communication is lost, the primary tries to restart again. Although this should never be the case in normal operation, this can be useful in the case of system ESD events for example where a loss of communication due to noise disturbing the secondary controller, is resolved when the primary restarts after an auto-restart off time.

The auto-restart alternately enables and disables the switching of the power MOSFET until the fault is removed. The auto-restart counter is gated by the switch oscillator in SOA mode the auto-restart off timer may appear to be longer.

The auto-restart counter is reset once the primary PRIMARY BYPASS pin falls below the undervoltage threshold V_{BPP}-$V_{BPP(HYS)}$.

Safe-Operating-Area (SOA) Protection
In the event there are two consecutive cycles where the primary power MOSFET switch current reaches current limit (I_{LIM}) within the blanking (t_{LEB}) and current limit (t_{ILD}) delay time, the controller will skip approximately 2.5 cycles or ~25 µsec. This provides sufficient time for reset of the transformer without sacrificing start-up time into large capacitive load. Auto-restart timing is increased when the device is operating in SOA-mode.

Primary-Secondary Handshake Protocol
At start-up, the primary initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers). If no feedback signals are received during the auto-restart on-time, the primary goes into auto-restart and repeats. However under normal conditions, the secondary chip will power-up through the FORWARD pin or directly from VOUT and then take over control. From then onwards the secondary is in control of demanding switching cycles when required.

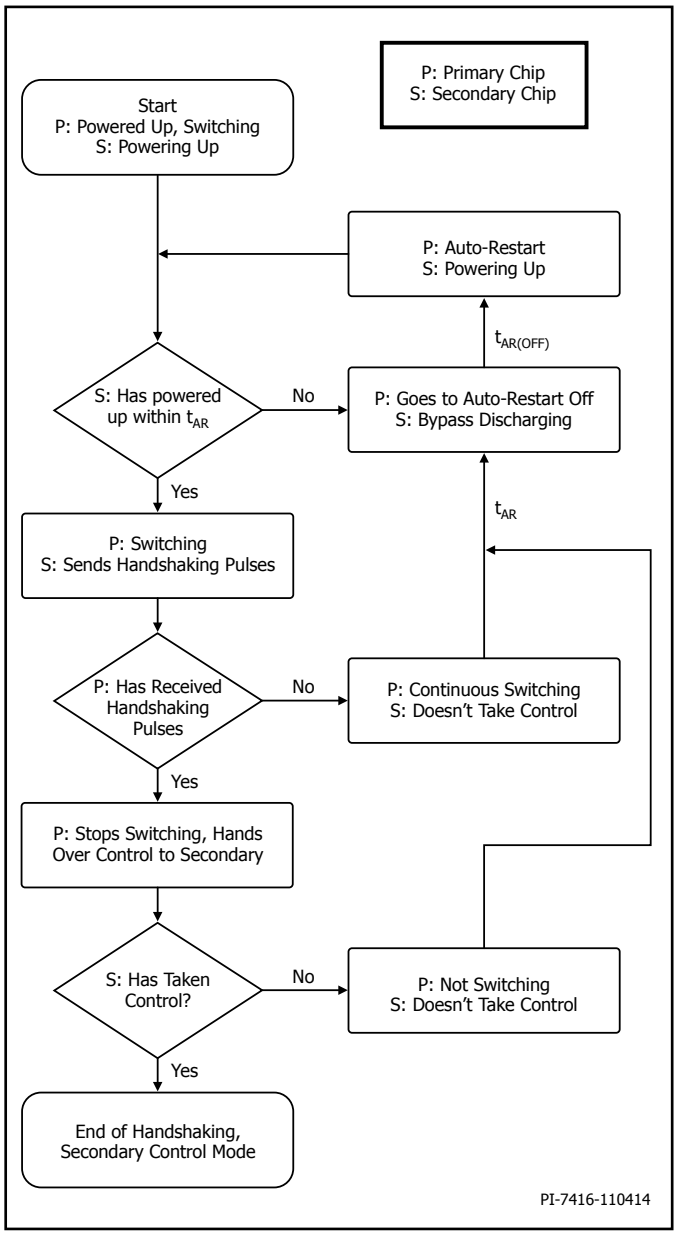


Figure 6. Primary – Secondary Handshake Flowchart.

The handshake flowchart is shown in Figure 6.

In the event the primary stops switching or does not respond to cycle requests from the secondary during normal operation when the secondary has control, the handshake protocol is imitated to ensure that the secondary is ready to assume control once the primary begins switching again. This protocol for an additional handshake is also invoked in the event the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching resulting from a momentary line drop-out or brown-out event. When the primary resumes operation, it will default into a start-up condition and attempt to detect hand-shake pulses from the secondary.

The communication is extremely robust. Measures against loss of communication have been implemented to make the device tolerant to extreme conditions such as surge, ESD events, or failure of external component (single point faults).

In the event the secondary does not detect that the primary responds to requests for 3 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 3 or more consecutive cycles, the secondary controller will initiate a second handshake sequence.

This protection mode also provides additional protection against cross-conduction of the SR MOSFET while the primary is switching with the primary-side in control. This protection mode also prevents output overvoltage in the event the primary is reset while the secondary is still in control and light/medium load conditions exist.

Secondary Controller

The feedback driver block is the drive to the FluxLink communication loop transferring switching pulse requests to the primary IC.

As shown in the block diagram in Figure 4, the secondary controller is powered through a 4.45 V Regulator block by either VOUT or FORWARD pin connections to the SECONDARY BYPASS pin. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the synchronous rectifier MOSFET (SR FET) connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin is also used to sense when to turn off the SR FET in discontinuous mode operation when the voltage across the FET on resistance drops below $V_{SR(TH)}$.

In continuous mode operation the SR FET is turned off when the pulse request is sent to demand the next switching cycle, providing excellent synchronization free of any overlap for the FET turn-off while operating in continuous mode.

The mid-point of an external resistor divider network between the VOUT and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is V_{REF} (1.265V).

The resistor connected between IS and SECONDARY GROUND pins is the bonding wire sense resistor which is used to regulate the output current in constant current regulator mode. The ISENSE pin is connected to the internal bond wire sense resistor and a 33 mV $IS_{V(TH)}$ threshold comparator used to determine the value at which the power supply output current is regulated.

Output Overvoltage Protection

In the event the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~10 mA is applied on the VOUT pin. This bleed current increases to ~140 mA in the event the FEEDBACK pin voltage is raised to beyond ~20% of the internal FEEDBACK pin reference voltage. The current sink on the VOUT pin is intended to discharge the output voltage for momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

FEEDBACK Pin Short Detection

In the event the FEEDBACK pin voltage is below the $V_{FB(OFF)}$ threshold at start-up, the secondary will complete the primary/secondary handshake and will stop requesting pulses to initiate an auto-restart.

The secondary will stop requesting cycles for $t_{AR(SK)}$, to begin primary-side auto-restart of $t_{AR(OFF)}$. In this condition, the total apparent AR off-time is $t_{AR(SK)} + t_{AR(OFF)}$. During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below $V_{FB(OFF)}$ threshold. The deglitch filter on the $V_{FB(OFF)}$ is less than 10 µsec. The secondary will relinquish control after detecting the FEEDBACK pin is shorted to ground.

OUTPUT VOLTAGE Pin Auto-Restart Threshold

The OUTPUT VOLTAGE pin includes a comparator to detect when the output voltage falls below the $V_{OUT(AR)}$ threshold for a duration exceeding $t_{VOUT(AR)}$. The secondary controller will relinquish control when it detects the OUTPUT VOLTAGE pin has fallen below $V_{OUT(AR)}$ for a time duration longer than $t_{VOUT(AR)}$. This threshold is meant to limit the range of constant current (CC) operation.

Cable Drop Compensation (CDC)

The amount of cable drop compensation is a function of the load with respect to the constant current regulation threshold as illustrated in Figure 7 below.

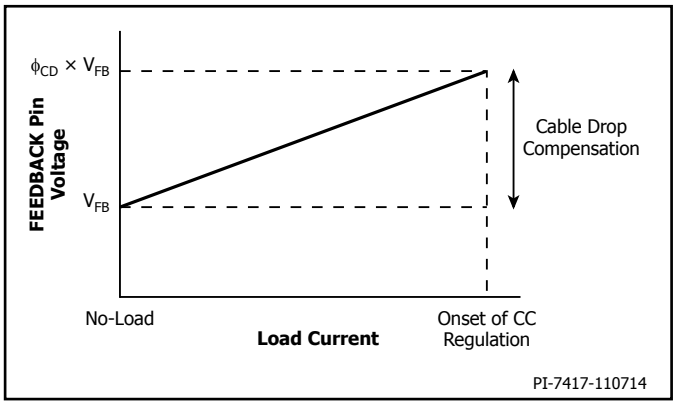


Figure 7. Cable Drop Compensation Characteristic.

The lower feedback pin resistor must be tied to the SECONDARY GROUND pin (not ISENSE pin) to have output cable drop compensation enabled.

Cable drop compensation only applies for 5 V designs. Cable drop compensation function is disabled for higher output voltage designs.

Output Constant Current Regulation

The InnoSwitch-CH regulates the output current through internal sense across bond wires between the ISENSE and SECONDARY GROUND pins. An external diode may be required across the ISENSE-SECONDARY GROUND pins to limit the peak voltage across the bond wire during fault condition. Larger output capacitance especially at higher output voltages, the output capacitor discharge into a short-circuited output can exceed the bond wire fusing current.

SR Disable Protection

On a cycle-by-cycle basis the SR is only engaged in the event a cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event the voltage on the ISENSE pin exceeds approximately 3 times the $IS_{V(TH)}$ threshold, the SR MOSFET drive is disabled until the surge current has diminished to nominal levels.

InnoSwitch-CH Operation

InnoSwitch-CH devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached. Since the highest current limit level and frequency of a InnoSwitch-CH design are constant, the power delivered to the load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the InnoSwitch-CH is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the DC_{MAX} limit is reached.

InnoSwitch-CH senses the output voltage on the FEEDBACK pin using a resistive voltage divider to determine whether or not to proceed with the next switching cycle. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle. This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, and the amount of energy per switch cycle.

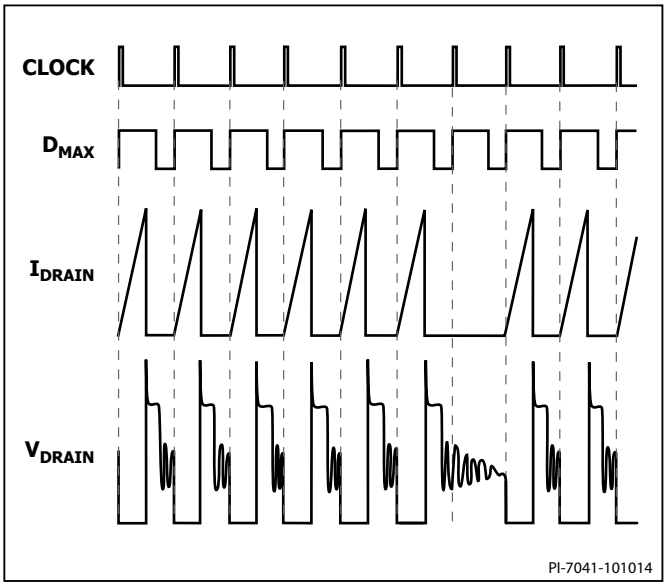


Figure 8. Operation at Near Maximum Loading.

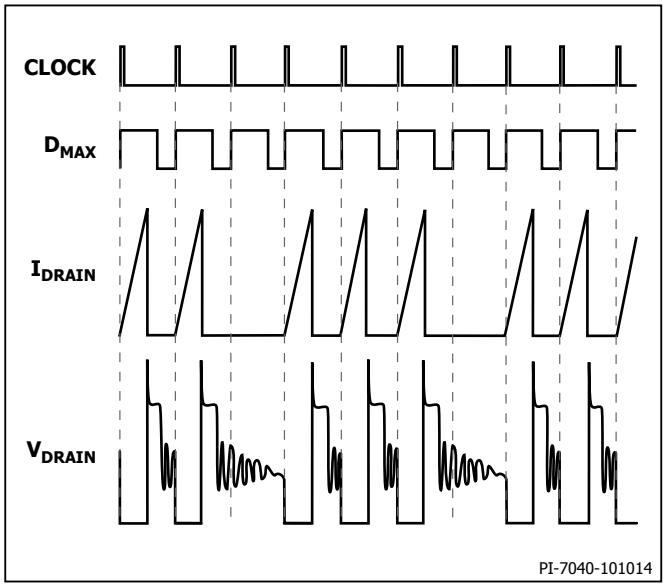


Figure 9. Operation at Moderately Heavy Loading.

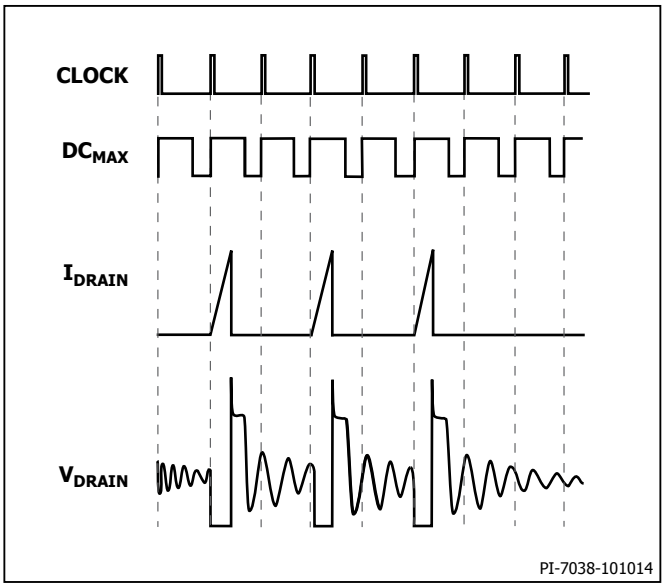


Figure 10. Operation at Medium Loading.

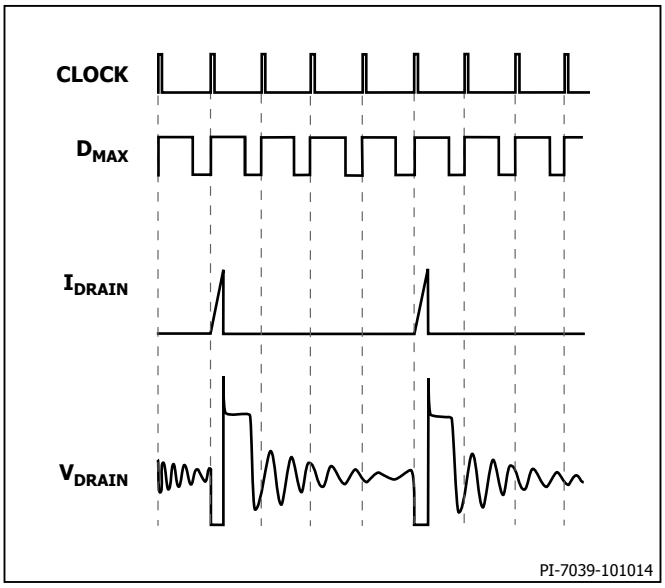


Figure 11. Operation at Very Light Load.

ON/OFF Operation with Current Limit State Machine

The internal clock of the InnoSwitch-CH runs all the time. At the beginning of each clock cycle, the voltage comparator on the FEEDBACK pin decides whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values.

At near maximum load, InnoSwitch-CH will conduct during nearly all of its clock cycles (Figure 8). At slightly lower load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 9). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 10). At very light loads, the current limit will be reduced even further (Figure 11). Only a small percentage of cycles will occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides accurate regulation and excellent transient response.

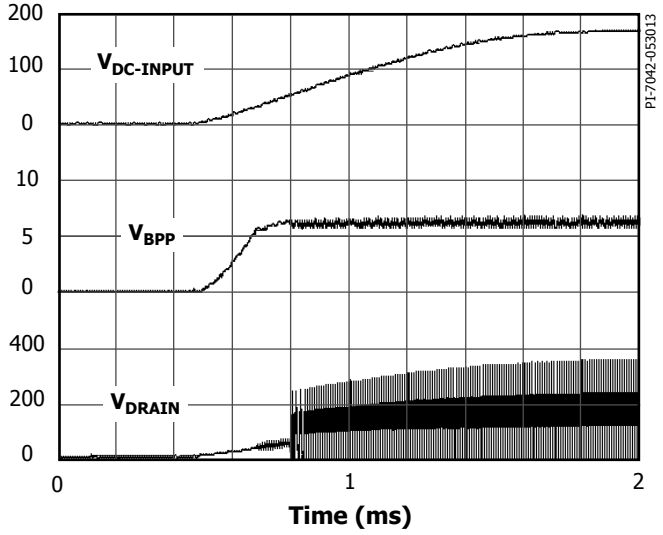


Figure 12. Power-Up Timing.

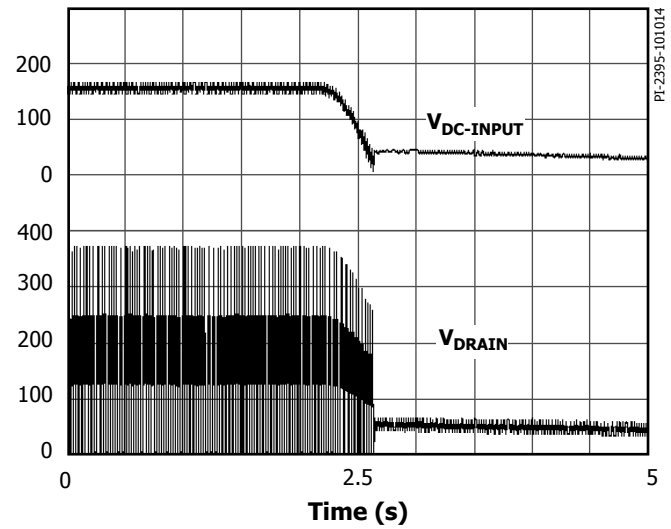


Figure 13. Normal Power-Down Timing.

Applications Example

		VAC			
		85	115	230	265
Efficiency at PCB (%)	Average		84.2	84.2	
	Full Load	82.6	84.2	85.1	84.8
	10% Load	78.3	78.9	78.6	78.7
No-Load Input	(mW)	7	7	8	9

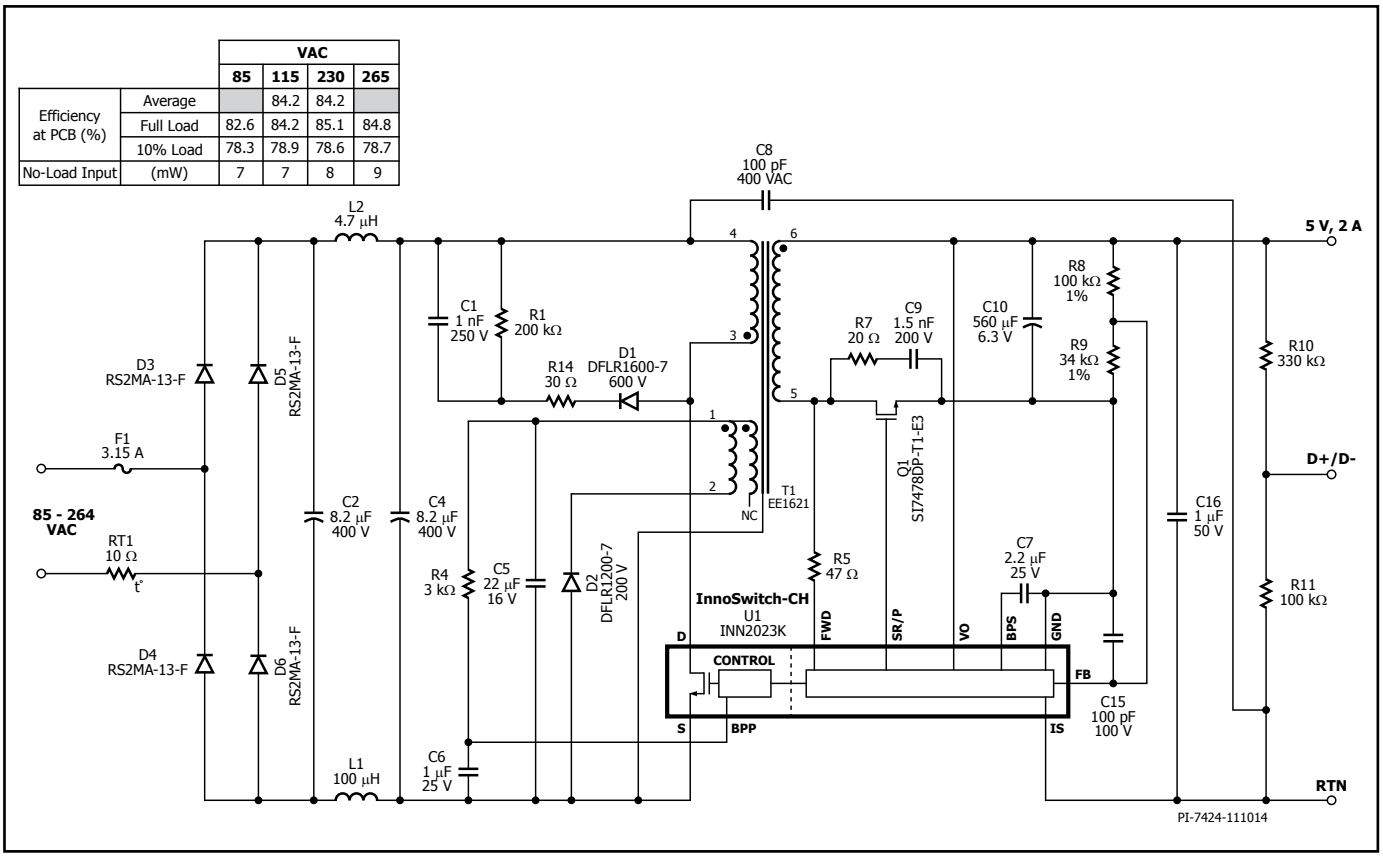


Figure 14. 5 V, 2 A Universal Input Charger.

The circuit shown in Figure 14 is a low cost, very high efficiency charger designed to provide 5 V, 2 A CV/CC charging, using an INN2023K integrated power supply controller.

This single 5 V output charger design features DoE Level 6 and EC CoC 5 compliance (84% measured vs. 79% requirement) and <10 mW no-load input power. The integration offered by InnoSwitch-CH devices reduces the total component count from typically >45 to only 32. The built-in secondary-side synchronous rectification (SR) controller of U1, allows expensive high current Schottky barrier diodes to be replaced with lower cost MOSFETs while increasing efficiency and removing hot spots. With control on the secondary-side, cross conduction problems normally associated with SR are eliminated under all conditions.

The input stage required a small thermistor (RT1) to prevent inrush currents exceeding the specification of D3-D6 and causing fuse F1 to open.

The total input capacitance of capacitor C2 and C4 is sufficient to maintain full output power delivery at 85 VAC, the converter being able to operate at the minimum DC voltage, just before the next AC cycle refreshes the input. The DC voltage is applied to the primary winding of T1. The other end of the primary winding is driven by the MOSFET inside the InnoSwitch-CH IC.

A low-cost RCD clamp formed by diode D1, resistors R1 and R14, and capacitor C1 limits the peak drain voltage of the InnoSwitch-CH IC at the instant of turn-off of the MOSFET. The clamp helps dissipate the energy stored in the leakage reactance of transformer T1 and effectively limits the turn-off voltage spike at the DRAIN pin of U1 to a safe value.

The InnoSwitch-CH IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C6) when AC is first applied. During normal operation the primary-side controller is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R4 limits the current being supplied to the PRIMARY BYPASS pin of the InnoSwitch-CH IC (U1) to be close to the IC supply current so as to minimize no-load input power.

Output regulation is achieved using ON/OFF control, the number of enabled switching cycles are adjusted based on the output load. At high-load, most switching cycles are enabled, and at light-load or no-load, most cycled are disabled or skipped. Once a cycle is enabled, the MOSFET will remain on until the primary current ramps to the device current limit for the specific operating state. There are four operating states (current limits) arranged such that the frequency content of the primary current switching pattern remains out of the audible range until at light-load where the transformer flux density and therefore audible noise generation is at a very low level.

The secondary-side of the InnoSwitch-CH IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

The secondary of the transformer is rectified by MOSFET Q1 and filtered by capacitor C10. Resistor R7 and C9 limit high-frequency

ringing during switching transients that would otherwise create radiated EMI. The gate of Q1 is turned on by secondary-side controller inside the InnoSwitch-CH IC based on the winding voltage sensed via resistor R5 and fed into the FORWARD pin of the IC.

In continuous conduction mode of operation, Q1 is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, Q1 is turned off when the voltage drop across the MOSFET falls below a threshold of approximately -24 mV [$V_{SR(TH)}$].

As both SR and primary MOSFET control resides on the secondary-side, any possibility of cross conduction of the two MOSFETs is eliminated. In turn the time Q1 is on can be maximized for lowest loss and allows removal of a parallel Schottky diode and/or the use of a lower cost higher $R_{DS(ON)}$ device for the same efficiency compared to standalone SR controllers.

The secondary-side of the InnoSwitch-CH IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C7 connected to the SECONDARY BYPASS pin of InnoSwitch-CH IC (U1) provides decoupling for the internal circuitry.

During CC (constant current) operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C7 via resistor R5 and an internal regulator. This allows output current regulation to be maintained down to <2.5 V. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed internally between the ISENSE and SECONDARY GROUND pins with a threshold of approximately 33 mV ($IS_{V(TH)}$) to reduce losses. Once the internal current sense threshold is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

Below the CC threshold, the device operates in constant voltage mode. The output voltage is sensed via resistor divider R8 and R9. Output voltage is regulated so as to achieve a voltage of 1.265 V on the FEEDBACK pin. Capacitor C15 provides decoupling to the FEEDBACK pin that ensure stable operation and prevents switching noise from coupling into the IC.

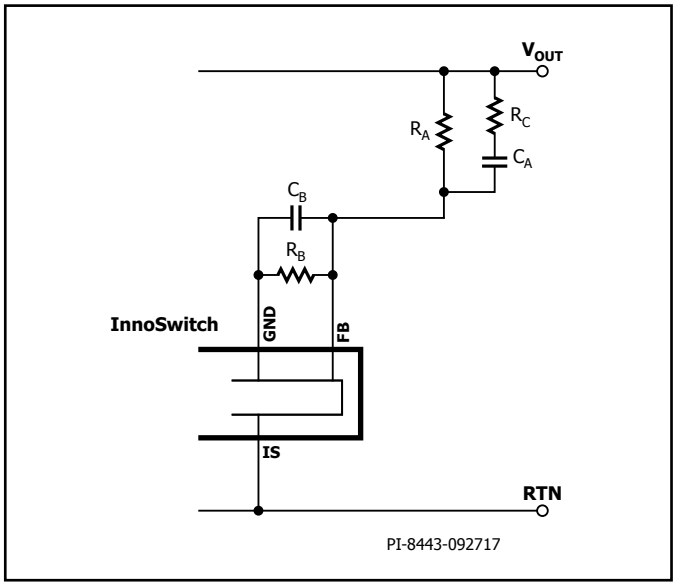


Figure 15. Feedback Network.

Better load regulation and lower output ripple can be achieved by matching the time constants of upper and lower feedback divider network. As shown in Figure 15.

$$R_B C_B \cong R_A C_A$$

Key application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the minimum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be sized to meet these criteria for AC input designs.
2. Efficiency of >82%.
3. Minimum data sheet value of I^2f.
4. Transformer primary inductance tolerance of ±10%.
5. Reflected output voltage (V_{OR}) of 110 V.
6. Voltage only output of 12 V with a synchronous rectifier.
7. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
8. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink is used to keep the SOURCE pin temperature at or below 110 °C.
9. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.

*Below a value of 1, K_p is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_p limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INIT}) from being exceeded at MOSFET turn-on.

Overvoltage Protection

The output overvoltage protection provided by the InnoSwitch-CH IC uses an internal latch that is triggered by a threshold current of approximately 7.6 mA into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a Zener diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin (parallel to R4 in Figure 14). Selecting the Zener diode voltage to be approximately 6 V above the bias winding voltage (28 V for 22 V bias winding) gives good OVP performance for most designs, but can be adjusted to compensate for variations in leakage inductance. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the bias winding diode and/or the OVP Zener diode. The resistor in series with the OVP Zener diode also limits the maximum current into the BYPASS pin.

Reducing No-load Consumption

The InnoSwitch-CH IC can start in self-powered mode from the BYPASS pin capacitor charged through the internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch-CH IC has become operational. Auxiliary or bias winding provided on the transformer is required for this purpose. The addition of a bias winding that provides bias supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption down to <10 mW. Resistor R4 shown in Figure 14 should be adjusted to achieve the lowest no-load input power.

Audible Noise
The cycle skipping mode of operation used in the InnoSwitch-CH IC can generate audio frequency components in the transformer. To limit this audible noise generation the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Ceramic capacitors that use dielectrics such as Z5U, when used in the clamp circuits and especially the bias supply (C1 and C5 in Figure 14) may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type for the clamp or electrolytic for the bias.

Selection of Components

Components for InnoSwitch-CH Primary-Side Circuit

BPP Capacitor
Capacitor connected from the PRIMARY BYAPSS pin of the InnoSwitch-CH IC provides decoupling for the primary-side controller and also selects current limit. A 0.1 μF, 10 μF or 1 μF capacitor may be used as indicated in the InnoSwitch-CH data sheet. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC and design of compact switching power supplies. 16 V or 25 V rated X5R or X7R dielectric capacitors are recommended to ensure minimum capacitance requirements are met.

Bias Winding and External Bias Circuit
The internal regulator connected from the drain pin of the MOSFET to the PRIMARY BYPASS pin of the InnoSwitch-CH primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 1 mA of current to the PRIMARY BYPASS pin.

Turns ratio for the bias winding should be selected such that 9 V is developed across the bias winding at the lowest rated output voltage of the charger at the lowest (or no-load) load condition. If the voltage is lower than this, the no-load input power will be higher than expected.

The bias current from the external circuit should be set to approximately 300 μA to achieve less than 10 mW no load power consumption when operating the charger at no load and 230 VAC input voltage.

A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to prevent snapped recovery typical of fast or ultrafast diodes which typically leads to higher radiated EMI.

A filter capacitor of at least 22 μF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and rated load with the lowest input AC supply voltage.

However a smaller capacitor value <22 μF also can be used as long as there is enough bias current into the PRIMARY BYPASS pin during no-load operation at the lowest rated output voltage such that the internal tap does not turn on.

A small resistor ranging from 2.2 Ω to 10 Ω in series with the bias winding diode is recommended in order to damp the ringing that could get coupled to FORWARD pin from bias winding. Waveforms shown in FORWARD Pin Resistor section are the examples for acceptable and unacceptable waveforms on the FORWARD pin during secondary rectifier on period.

Primary Sensed OVP (Overvoltage Protection)
The voltage developed across the bias winding output tracks the power supply output voltage. Though not precise, a reasonably accurate detection of output voltage condition can be achieved by the primary-side controller using the bias winding voltage. A Zener diode connected from the bias winding output to the PRIMARY BYPASS pin can reliably detect a fault condition that leads to increase in output voltage beyond the set limits and causes the primary-side controller to latch off preventing damage of components due to the fault conditions.

It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady-state conditions at full rated load and lowest rated input voltage and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will not operate under any normal operating conditions and will only operate in case of a fault condition.

Use of the primary sensed OVP protection is highly recommended.

Primary-Side Snubber Clamp
A snubber circuit should be used on the primary-side as shown in the example circuit. This prevents excess voltage spikes at the drain of the MOSFET at the instant of turn-off of the MOSFET during each switching cycle. Though conventional RCD clamps can be used, RCDZ calmps offer the highest efficiency. The circuit example shows in Figure 14 uses RCD clamp with a resistor in series with the clamp diode . This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recover glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Components for InnoSwitch-CH Secondary-Side Circuit

SECONDARY BYPASS Pin – Decoupling Capacitor
A 2.2 μF, 25 V multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch-CH IC. A significantly higher value will lead to output voltage overshoot during start-up and lower values may lead to unpredictable operation. The capacitor must be located adjacent to the IC pins. The 25 V rating is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops with applied voltage. 10 V rated examples are not recommended for this reason. Capacitors with X5R or X7R dielectrics should be used for best results.

FORWARD Pin Resistor
A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current. A higher or lower resistor value should not be used as it can affect device operation such as the synchronous rectifier drive timing.

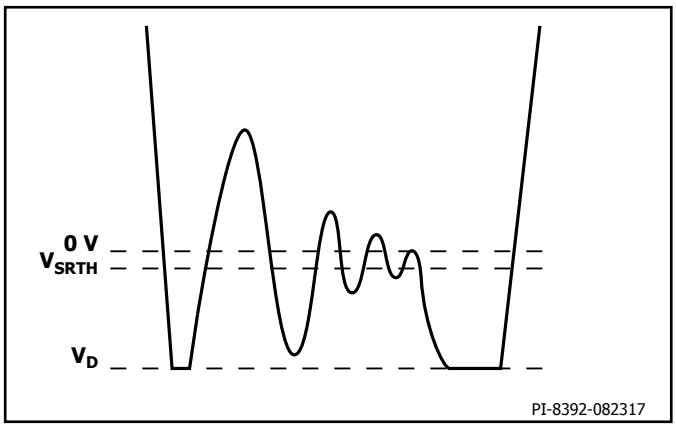


Figure 16. Unacceptable FORWARD Pin Waveform After Handshake With SR MOSFET Conduction During Flyback Cycle.

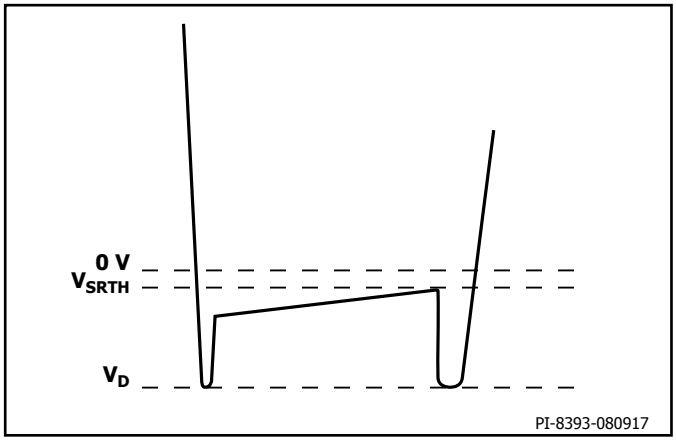


Figure 17. Acceptable FORWARD Pin Waveform After Handshake With SR MOSFET Conduction During Flyback Cycle.

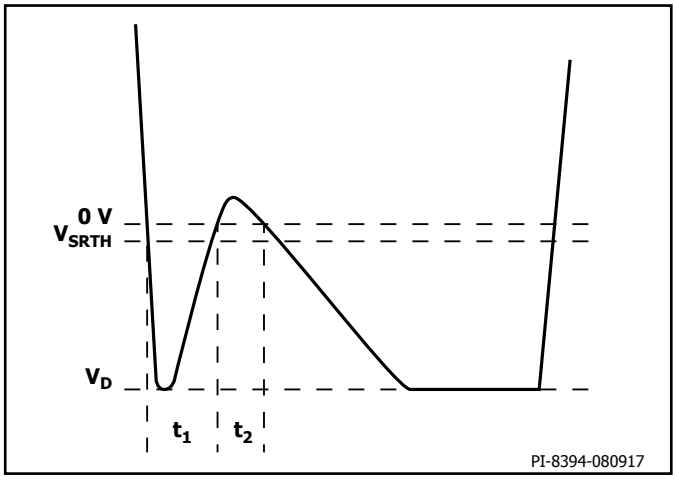


Figure 18. Unacceptable FORWARD Pin Waveform Before Handshake With Body Diode Conduction During Flyback Cycle.

Note:
If t1 + t2 = 1.5 μs ± 50 ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off.

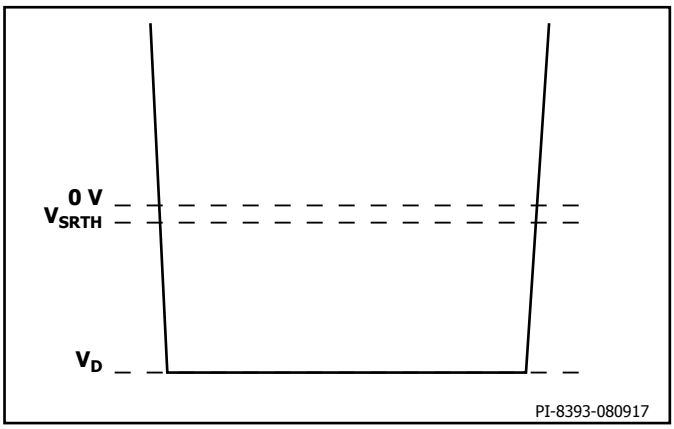


Figure 19. Acceptable FORWARD Pin Waveform Before Handshake With Body Diode Conduction During Flyback Cycle.

SR MOSFET Operation and Selection

Although a simple diode rectifier and filter is adequate for the secondary-winding, use of a SR MOSFET enables significant improvement in operating efficiency often required to meet the European CoC and the U.S. DoE energy efficiency requirements.

The secondary-side controller turns on the SR MOSFET once the flyback cycle begins. The SR MOSFET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch-CH IC and no additional resistors should be connected in the gate circuit of the SR MOSFET.

The SR MOSFET is turned off once the drain voltage of the SR MOSFET drops below -24 mV [$V_{SR(TH)}$]. Therefore the use of MOSFETs with a very small $R_{DS(ON)}$ can be counterproductive as it reduces the MOSFET on-time, commutating the current to the body diode of the MOSFET or an external parallel Schottky diode if used.

A MOSFET with 18 mΩ $R_{DS(ON)}$ is a good choice for designs rated for 5 V, 2 A output. The SR MOSFET driver uses the secondary SECONDARY BYPASS pin for its supply rail and this voltage is typically 4.4 V. A MOSFET with too high a threshold voltage is therefore not suitable and MOSFETs with a low threshold voltage of 1.5 V to 2.5 V are ideal although MOSFETs with a threshold voltage (absolute maximum) as high as 4 V may be used.

There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR MOSFET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch-CH IC detects end of the flyback cycle, voltage across SR MOSFET $R_{DS(ON)}$ drops below 24 mV, the remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR MOSFET or the external parallel Schottky diode.

Use of the Schottky diode parallel to the SR MOSFET may be added to provide higher efficiency and typically a 1 A surface mount Schottky diode is often adequate. The gains are modest, for a 5 V, 2 A design the external diode adds ~0.1% to full load efficiency at 85 VAC and ~0.2% at 230 VAC.

The voltage rating of the Schottky diode and the SR MOSFET should be at least 1.3 to 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated MOSFETs and diodes are suitable for most 5 V designs that use a V_{OR} <60 V.

The interaction between the leakage reactance of the secondary and the MOSFET capacitance (COSS) leads to ringing on the voltage waveforms at the instance of voltage reversal at the winding due to the primary MOSFET turn-on. This ringing can be suppressed using a RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used though a higher resistance value leads to noticeable drop in efficiency. A capacitance of 1 nF to 1.5 nF is adequate for most designs.

Output Capacitor
Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and simultaneously high RMS ripple current rating. These capacitors enable design of compact chargers and adapters.

Typically, 200 μF to 300 μF of aluminum-polymer capacitance is often adequate for every ampere of output current. The other factor that influences choice of the capacitance is the output ripple. Care should be taken to ensure that capacitors with a voltage rating higher than the highest output voltage with sufficient margin (>20%) be used.

Output Voltage Feedback Circuit
The nominal output voltage feedback pin voltage is 1.265 V [V_{FB}]. A voltage divider network should be connected at the output of the power supply to divide the output voltage such that the voltage at the FEEDBACK pin will be 1.265 V when the output voltage is at the set nominal voltage. The lower feedback divider resistor should be tied to the SECONDARY GROUND pin. A 300 pF or higher decoupling capacitor should be connected at the FEEDBACK pin to the SECONDARY GROUND pin of the InnoSwitch-CH IC. This capacitor should be placed physically close to the InnoSwitch-CH IC. An R-C network may also need to be connected across the upper divider resistor in the feedback divider network. Capacitor value should be chosen such that the time constant matches with lower feedback divider to achieve better load regulation and lower output ripple. Recommended value for R is 1 kΩ in order to limit the current flowing through the FEEDBACK pin in case of a short-circuit at the output.

Protection Diode for Secondary Current Shunt
The InnoSwitch-CH IC includes a secondary-side current sense function which enables a precise CC mode of operation. The power supply transitions from CV to CC mode automatically when the output current exceeds the constant current regulation threshold as specified in the data sheet.

To sense the output the load current flows from the ISENSE pin through an internal shunt to the SECONDARY GROUND pin of the IC. The transition to CC operation occurs when the shunt voltage exceeds ~33 mV, the very low sensing voltage ensures very low dissipation.

During an output short-circuit the output filter capacitor (C10 in Figure 1) discharges instantaneously through the internal shunt. Depending on the output voltage, value of the output capacitance and short circuit impedance the energy dissipated in the shunt can be very high.

To prevent any damage to the IC, an external 1 A Schottky diode between the ISENSE and the SECONDARY GROUND pins is recommended for designs with an output voltage above 5 V, where the power supply can be shorted at the output terminals. When this diode is used, the anode should be connected to the ISENSE pin and the cathode should be connected to the SECONDARY GROUND pin.

Recommendations for Circuit Board Layout

See Figure 20 for a recommended circuit board layout for InnoSwitch-CH IC.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and InnoSwitch-CH IC should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and InnoSwitch-CH IC.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the InnoSwitch-CH IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, this area should be maximized for good heat sinking. Similarly for output SR MOSFET, maximize the PCB area connected to the pins on the package through which heat is dissipated in the SR MOSFET.

Sufficient copper area should be provided on the board to keep the InnoSwitch-CH IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the InnoSwitch-CH IC is soldered is sufficiently large to keep the IC temperature below 85 °C when operating the charger at full rated load and at the lowest rated input AC supply voltage. Further de-rating can be applied depending on any additional specific requirements.

Y Capacitor
The placement of the Y capacitor should be directly from the primary input filter capacitor positive terminal to the output positive or return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the InnoSwitch-CH IC. Note – if an input π (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR MOSFET
For best performance, the area of the loop connecting the secondary winding, the output SR MOSFET and the output filter capacitor, should be minimized. In addition, sufficient copper area should be provided at the terminals of the SR MOSFET for heat sinking.

ESD
Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD / hi-pot requirements.

The spark gap is best placed between output positive rail and one of the AC inputs directly. In this configuration a 5 mm spark gap is often sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input.

Drain Node

The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and associated circuit and trace lengths in this circuit should be minimized.

The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the InnoSwitch-CH IC primary-side MOSFET should be kept as small as possible.

Figure 14 shows a design example for an InnoSwitch-CH IC based charger design. Considerations provided in this design are marked in the figure and are listed below:

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area for these loops.
2. A small capacitor in parallel to the clamp diode on the primary side can help reduced radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Common mode chokes are typically required at the input of the charger to sufficiently attenuate common mode noise. The same can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to achieve improved conducted and radiated EMI margins.
5. Values of components of the RC snubber connected across the output SR MOSFET can help reduce high frequency radiated and conducted EMI.
6. A π filter comprising of differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
7. A 1 μF ceramic capacitor when connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Audible Noise Suppression

The state machine used in the InnoSwitch-CH IC automatically adjusts the current limit so as to adjust the operating frequency at light load. This helps to eliminate audible noise that typically results from intermittent switching of the power supply at very light loads.

In case of audible noise from a power supply, following should be considered as guidelines for audible noise reduction:

1. Ensure that the flyback transformers are dip varnished.
2. Often the source of audible noise are ceramic capacitors. Check both the bias winding and primary-side clamp capacitors. To find the source substitute the clamp capacitor with a metalized film type and the bias with an electrolytic type. By far the most common source is the bias capacitor.
3. If the noise is generated by the bias winding filter capacitor, generally, use of a capacitor of higher voltage rating will typically resolve the issue. If the circuit board layout and any physical enclosure size constraints, allow, an electrolytic capacitor should be used instead.

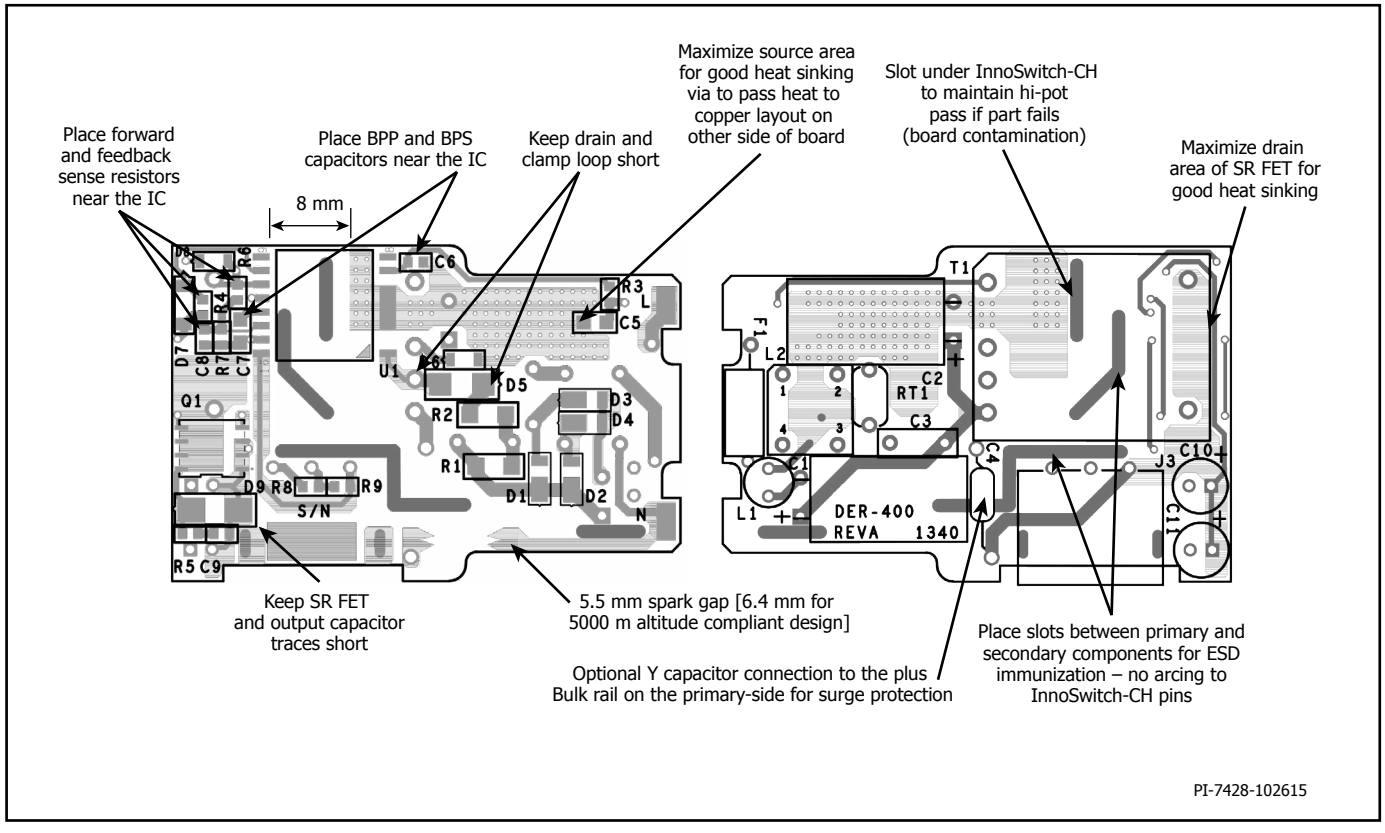


Figure 20. PCB Layout Guidelines. Bottom (Left Side), Top (Right Side).

4. Reducing the AC flux density (ΔB) of the transformer will also lead to reduction in audible noise from the core.
5. If the secondary-winding is terminated with flying leads verify if the wires as vibrating against the bobbin or each other.
6. If the circuit board shows any signs of pulse bunching (multiple switching cycles followed by no switching activity), this could be a cause of audible noise. Pulse bunching can be caused by incorrect circuit board layout in which the feedback node is being affected by switching noise. Guidelines provided for FEEDBACK pin decoupling and the phase lead RC network described in this note can be evaluated. Verify the board layout recommendations associated with feedback divider network have been followed.

Recommendations for Transformer Design

Transformer design must ensure that the power supply is able to deliver the rated power at the lowest operating voltage. The lowest voltage on the rectified DC bus of the power supply depends on the capacitance of the filter capacitor used. At least 2 µF / W is recommended to keep the DC bus voltage always above 70 V though 3 µF/W provides sufficient margin. The ripple on the DC bus should be measured and care should be taken to verify this voltage to confirm the design calculations for transformer primary-winding inductance selection.

Reflected Output Voltage, V_{OR} (V)
This parameter is the secondary-winding voltage during the diode/SR conduction time reflected back to the primary through the turns ratio of the transformer. A V_{OR} of 60 V is ideal for most 5 V only designs. For design optimization purposes, the following should be kept in mind:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch-CH device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR MOSFTs.
3. Higher V_{OR} increases leakage inductance that reduces efficiency of the power supply.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

Ripple to Peak Current Ratio, K_P
Below a value of 1, indicating continuous conduction mode, K_P is the ratio of ripple to peak primary current (Figure 21)

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

Following a value of 1, indicating discontinuous conduction mode, K_P is the ratio of primary MOSFET off time to the secondary diode conduction time.

$$K_P \equiv K_{DP} = \frac{(1-D)\times T}{t}$$
$$= \frac{V_{OR}\times(1-D_{MAX})}{(V_{MIN}-V_{DS})\times D_{MAX}}$$

It is recommended that a K_P close to 0.9 at the minimum DC bus voltage of 70 V should be used for most InnoSwitch-CH designs.

A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side MOSFET resulting in higher InnoSwitch-CH temperature.

Core Type
Choice of suitable core is dependent on the physical design constraints of the enclosure to be used for the charger. It is recommended that cores with low loss should only be used as

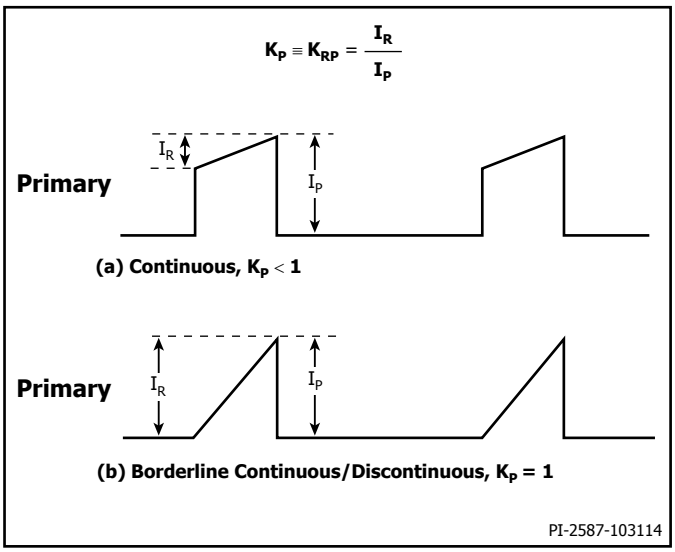


Figure 21. Continuous Mode Current Waveform, $K_P \leq 1$.

charger designs are often thermally challenged due to the small enclosure requirement.

Safety Margin, M (mm)
For designs that require safety isolation between primary and secondary but are not using triple insulated wire the width of the safety margin to be used on each side of the bobbin should be entered here. Typically for universal input designs a total margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical, however if a total margin of 6.2 mm were required then 3.1 mm would still be entered even if the physical margin were only on one side of the bobbin.

For designs using triple insulated wire it may still be necessary to use a small margin in order to meet the required safety creepage distances. Typically many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required.

As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. It is recommended that for compact charger designs using an InnoSwitch-CH IC, triple insulated wire should be used for secondary which then eliminates need for margins.

Primary Layers, L
Primary layers should be in the range of 1 < L < 3 and in general it should be the lowest number that meets the primary current density limit (CMA). Values of ≥200 Cmils/Amp can be used as a starting value for most designs though higher values may be required based on thermal design constraints. Values above 3 layers are possible but the increased leakage inductance and physical fit of the windings should be considered. A split primary construction may be helpful for designs where leakage inductance clamp dissipation is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power charger designs as this typically requires additional common mode filtering which increases cost.

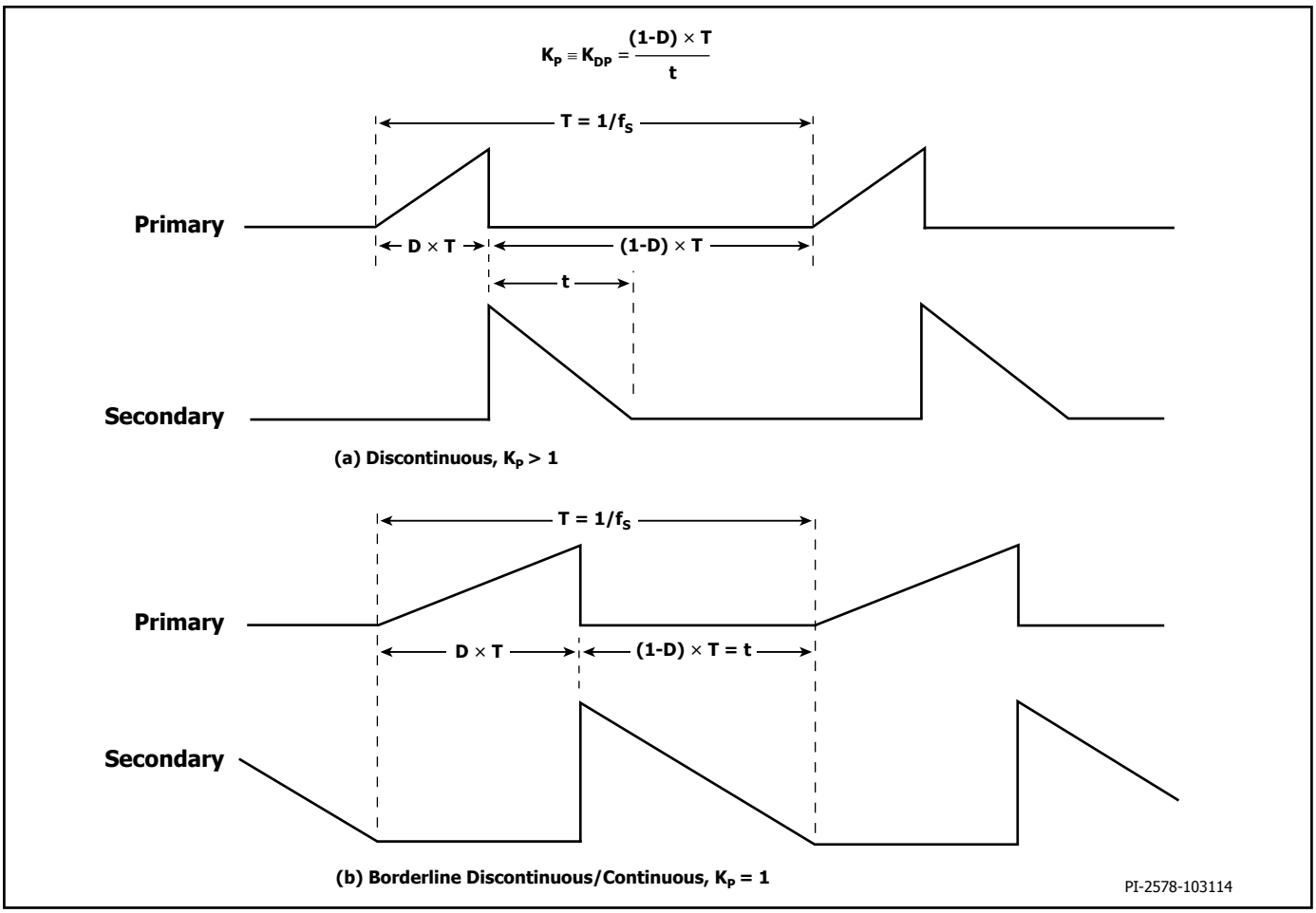


Figure 22. Discontinuous Mode Current Waveform, K_P ≥1.

Maximum Operating Flux Density, B_M (Gauss)

A maximum value of 3000 Gauss during normal operation is recommended to limit the maximum flux density under start-up and output short-circuit. Under these conditions the output voltage is low and little reset of the transformer occurs during the MOSFET off-time. This allows the transformer flux density to staircase above the normal operating level. A value of 3000 Gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch-CH IC provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

Transformer Primary Inductance, (L_p)

Once the lowest operating voltage and the required V_{OR} are determined, transformer primary inductance can be calculated. Care should be taken to ensure that the selected inductance value does not violate the maximum duty cycle specification in the data sheet of the InnoSwitch-CH IC. The PIXIs design spreadsheet which is part of the free PI Expert suite can be used to assist in designing the transformer.

Quick Design Checklist

As with any power supply design, all InnoSwitch-CH designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions.

The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that VDS does not exceed 600 V at highest input voltage and peak (overload) output power. The 50 V margin to the 650 V BV_{DSS} specification gives margin for design variation.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at start-up. Repeat under steady-state conditions and verify that the leading edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for InnoSwitch-CH IC, transformer, output SR MOSFET, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of InnoSwitch-CH IC as specified in the data sheet.

Under low-line, maximum power, a maximum InnoSwitch-CH SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage ..... -0.3 V to 650 V
DRAIN Pin Peak Current[3] INN20x3 ..... 1200 (2250) mA
INN20x4 ..... 1360 (2550) mA
INN20x5 ..... 1680 (3150) mA
PRIMARY BYPASS/SECONDARY BYPASS Pin Voltage ..... -0.3 V to 9 V
PRIMARY BYPASS/SECONDARY BYPASS Pin Current ..... 100 mA
FORWARD Pin Voltage ..... -1.5 V to 150[7] V
FEEDBACK Pin Voltage ..... -0.3 V to 9 V
SR Pin Voltage ..... -0.3 to 9 V[6]
OUTPUT VOLTAGE Pin Voltage ..... -0.3 to 15[8] V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to Source and Secondary Ground, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Higher peak Drain current is allowed while the Drain voltage is simultaneously less than 400 V.
4. Normally limited by internal circuitry.
5. 1/16” from case for 5 seconds.
6. -1.8 V for a duration of ≤500 nsec. See Figure 28.
7. The maximum current out of the FORWARD pin when the FORWARD pin is below Ground is -40 mA.
8. Maximum current into VOUT pin at 15 V should not exceed 10 mA.

Thermal Resistance

Thermal Resistance: eSOP-R16B Package:
(θ_{JA}) ..... 65 °C/W[2], 69 °C/W[1]
(θ_{JC}) ..... 12 °C/W[3]

Notes:
1. Solder to 0.36 sq. in (232 mm^2), 2 oz. (610 g/m^2) copper clad.
2. Solder to 1 sq. in (645 mm^2), 2 oz. (610 g/m^2) copper clad.
3. The case temperature is measured at the plastic surface at the top of the package.

Parameter	Conditions	Rating	Units
Ratings for UL1577 (Adapter power rating is derated power capability)			
Primary-Side Current Rating	Current from pin (3-6) to pin 1	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Current Rating	Current from pin 16 to pin 15	2.5	A
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	0.125	W

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency Applies to Both Primary and Secondary Controllers	f_{OSC}	T_J = 25 °C	Average	93	100	107	kHz
			Peak-to-Peak Jitter		6		
Maximum Duty Cycle	DC_{MAX}	T_J = 0 °C to 125 °C		60			%

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
PRIMARY BYPASS Pin Supply Current	I_{S1}	T_J = 25 °C, V_{BPP} + 0.1 V (MOSFET not Switching) See Note B			250		µA
	I_{S2}	T_J = 25 °C, V_{BPP} + 0.1 V (MOSFET Switching at f_{OSC}) See Note A, C	INN20x3		635	750	
			INN20x4		790	900	
			INN20x5		970	1100	
PRIMARY BYPASS Pin Charge Current	I_{CH1}	T_J = 25 °C, V_{BP} = 0 V See Notes D, E		-5.4	-4.5	-3.6	mA
	I_{CH2}	T_J = 25 °C, V_{BP} = 4 V See Notes D, E		-3.8	-2.9	-2.0	
PRIMARY BYPASS Pin Voltage	V_{BPP}	See Note D		5.73	5.95	6.15	V
PRIMARY BYPASS Pin Voltage Hysteresis	$V_{BPP(H)}$			0.48	0.56	0.65	V
PRIMARY BYPASS Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		6.15	6.45	6.75	V
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.1 µF	I_{LIMIT} See Note E	di/dt = 138 mA/µs T_J = 25 °C	INN20x3	611	650	689	mA
		di/dt = 168 mA/µs T_J = 25 °C	INN20x4	705	750	795	
		di/dt = 213 mA/µs T_J = 25 °C	INN20x5	893	950	1007	
Reduced Current Limit (BPP) Capacitor = 10 µF	$I_{LIMIT-1}$ See Note E	di/dt = 138 mA/µs T_J = 25 °C	INN20x3	500	550	600	mA
		di/dt = 168 mA/µs T_J = 25 °C	INN20x4	591	650	709	
		di/dt = 213 mA/µs T_J = 25 °C	INN20x5	773	850	927	
Increased Current Limit (BPP) Capacitor = 1 µF	$I_{LIMIT+1}$ See Note E	di/dt = 138 mA/µs T_J = 25 °C	INN20x3	682	750	818	mA
		di/dt = 168 mA/µs T_J = 25 °C	INN20x4	773	850	927	
		di/dt = 213 mA/µs T_J = 25 °C	INN20x5	955	1050	1145	
Power Coefficient	I^2f	Standard Current Limit, $I^2f = I_{LIMIT(TYP)}^2 \times f_{OSC(TYP)}$ See Note A	INN20x3-20x5	0.87 × I^2f	I^2f	1.15 × I^2f	A^2Hz

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Power Coefficient	I^2f	Reduced Current Limit, $I^2f = I_{LIMITred(TYP)}^2 \times f_{OSC(TYP)}$ See Note A	INN20x3-20x5	0.84 × I^2f	I^2f	1.18 × I^2f	A^2Hz
		Increased Current Limit, $I^2f = I_{LIMITinc(TYP)}^2 \times f_{OSC(TYP)}$ See Note A	INN20x3-20x5	0.84 × I^2f	I^2f	1.18 × I^2f	
Initial Current Limit	I_{INIT}	T_J = 25 °C See Note A		0.75 × $I_{LIMIT(TYP)}$			mA
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note A		170	250		ns
Current Limit Delay	t_{ILD}	T_J = 25 °C See Note A, F			170		ns
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			75		°C
PRIMARY BYPASS Pin Shutdown Threshold Current	I_{SD}			5.6	7.6	9.6	mA
Primary Bypass Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.8	3.0	3.3	V
Auto-Restart On-Time at f_{osc}	t_{AR}	T_J = 25 °C See Note G		64	77	90	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A, G			1		s
Auto-Restart Off-Time at f_{osc}	$t_{AR(OFF)}$	T_J = 25 °C See Note G				2	s
Short Auto-Restart Off-Time at f_{osc}	$t_{AR(OFF)SH}$	T_J = 25 °C See Note A, G			0.5		s
Output							
ON-State Resistance	$R_{DS(ON)}$	INN20x3 I_D = 750 mA	T_J = 25 °C		3.50	4.10	Ω
			T_J = 100 °C See Note A		5.50	6.30	
		INN20x4 I_D = 850 mA	T_J = 25 °C		2.30	2.70	
			T_J = 100 °C See Note A		3.60	4.20	
		INN20x5 I_D = 1050 mA	T_J = 25 °C		1.70	2.00	
			T_J = 100 °C See Note A		2.70	3.10	
OFF-State Drain Leakage Current	I_{DSS1}	V_{BPP} = 6.2 V, V_{DS} = 520 V, T_J = 125 °C See Note H				200	µA

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output (cont.)							
OFF-State Drain Leakage Current	I_{DSS2}	V_{BPP} = 6.2 V, V_{DS} = 325 V, T_J = 25 °C See Notes A, H			15		µA
Breakdown Voltage	BV_{DSS}	V_{BPP} = 6.2 V T_J = 25 °C See Note I		650			V
Drain Supply Voltage				50			V
Secondary							
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C		1.250	1.265	1.280	V
OUTPUT VOLTAGE Pin Auto-Restart Threshold	$V_{OUT(AR)}$	See Note K		3.00	3.25	3.50	V
Cable Drop Compensation Factor	ϕ_{CD}	T_J = 25 °C	INN202x	1.05	1.06	1.07	
			INN200x	–	1.00	–	
SECONDARY BYPASS Pin Current at No-Load	I_{SNL}	T_J = 25 °C			265	315	µA
SECONDARY BYPASS Pin Voltage	V_{BPS}			4.25	4.45	4.65	V
SECONDARY BYPASS Pin Undervoltage Threshold	$V_{BPS(UVLO)}$			3.45	3.8	4.15	V
SECONDARY BYPASS Pin Undervoltage Hysteresis	$V_{BPS(HYS)}$			0.10	0.65	1.2	V
Output (IS Pin) Current Limit Voltage Threshold	$IS_{V(TH)}$	T_J = 25 °C			33		mV
Constant Current Regulation Threshold	I_{CC}	T_J = 0 °C to 100 °C		2.0	2.2	2.4	A
Normalized Output Current	I_O	T_J = 25 °C		1.00	1.04	1.08	
OUTPUT VOLTAGE Pin AR Timer	$t_{VOUT(AR)}$			8			ms
FEEDBACK Pin Short-Circuit	$V_{FB(OFF)}$				0.1	0.14	V
Synchronous Rectifier							
SYNCHRONOUS RECTIFIER Pin Threshold	$V_{SR(TH)}$	T_J = 25 °C		-19	-24	-29	mV
SYNCHRONOUS RECTIFIER Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_S = 100 kHz		125	162	200	mA

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Synchronous Rectifier[1] (cont.)							
SYNCHRONOUS RECTIFIER Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_S = 100 kHz		230	280	315	mA
SYNCHRONOUS RECTIFIER Pin Drive Voltage	V_{SR}	See Note A		4.2	4.4	4.6	V
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF See Note A	0-100%		71		ns
			10-90%		40		
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF See Note A	0-100%		32		ns
			10-90%		15		
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{SPS} = 4.4 V I_{SR} = 10 mA See Note A			11.5		Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{SPS} = 4.4 V I_{SR} = 10 mA See Note A			3.5		Ω

NOTES:

A. This parameter is derived from characterization.

B. I_{S1} is an estimate of device current consumption at no-load, since the operating frequency is so low under these conditions. Total device consumption at no-load is sum of I_{S1} and I_{DSS2} (this does not include secondary losses)

C. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the Drain. An alternative is to measure the PRIMARY BYPASS pin current at 6.2 V.

D. The PRIMARY BYPASS pin is not intended for sourcing supply current to external circuitry.

E. To ensure correct current limit it is recommended that nominal 0.1 µF/1 µF/10 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal PRIMARY BYPASS Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
	Minimum	Maximum
0.1 µF	-60%	+100%
1 µF	-50%	+100%
10 µF	-50%	N/A

F. This parameter is derived from the change in current limit measured at 1X and 4X of the di/dt shown in the I_{LIMIT} specification.

G. Auto-restart on-time has same temperature characteristics as the oscillator (inversely proportional to frequency).

H. I_{DSS1} is the worst-case OFF-state leakage specification at 80% of BV_{DSS} and the maximum operating junction temperature. I_{DSS2} is a typical specification under worst-case application conditions (rectified 230 VAC) for no-load consumption calculations.

I. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping Drain voltage up to but not exceeding minimum BV_{DSS}.

J. For reference only. This is the total range of current limit threshold which corrects for variations in the current sense bond wire. Both of which are trimmed to set the normalized output constant current.

K. Measured at the VOUT pin of the device. At the end of the cable under load, the apparent auto-restart threshold will be lower.

Typical Performance Characteristics

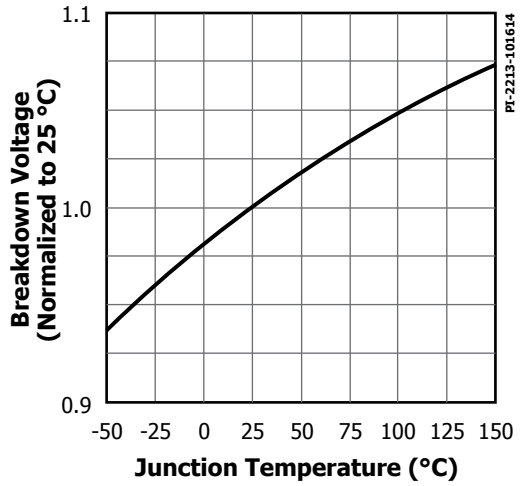


Figure 23. Breakdown vs. Temperature.

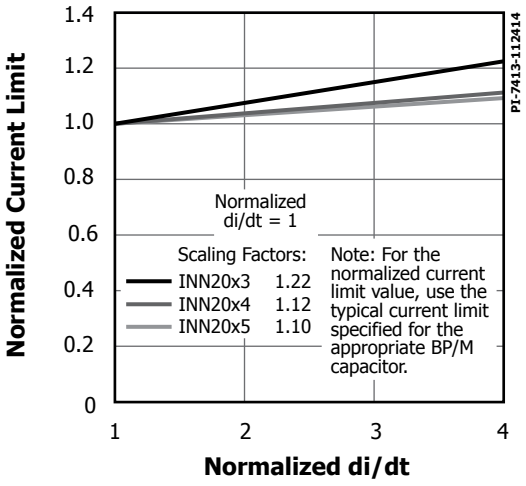


Figure 24. Standard Current Limit Vs. di/dt.

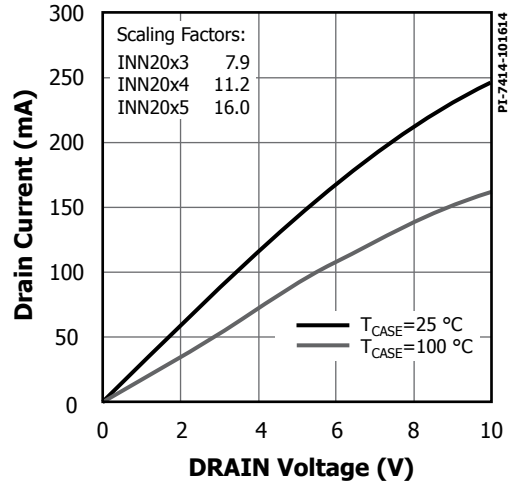


Figure 25. Output Characteristic.

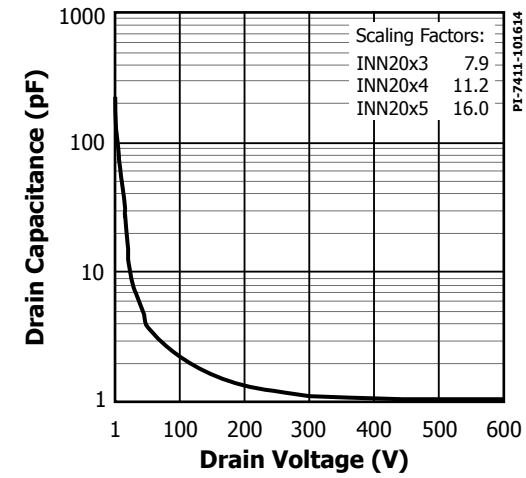


Figure 26. C_{OSS} vs. Drain Voltage.

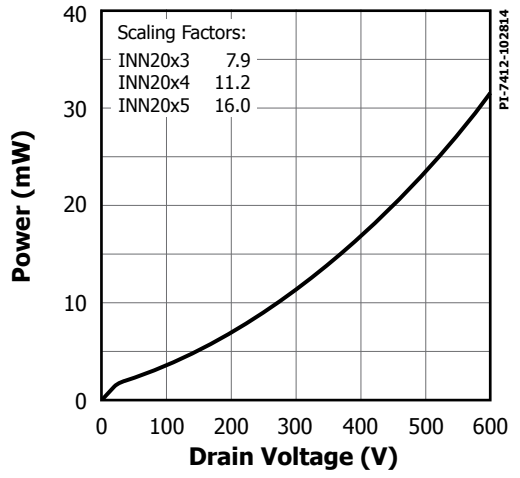


Figure 27. Drain Capacitance Power.

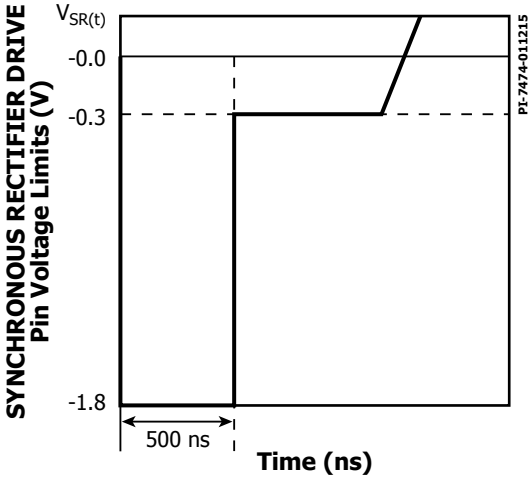
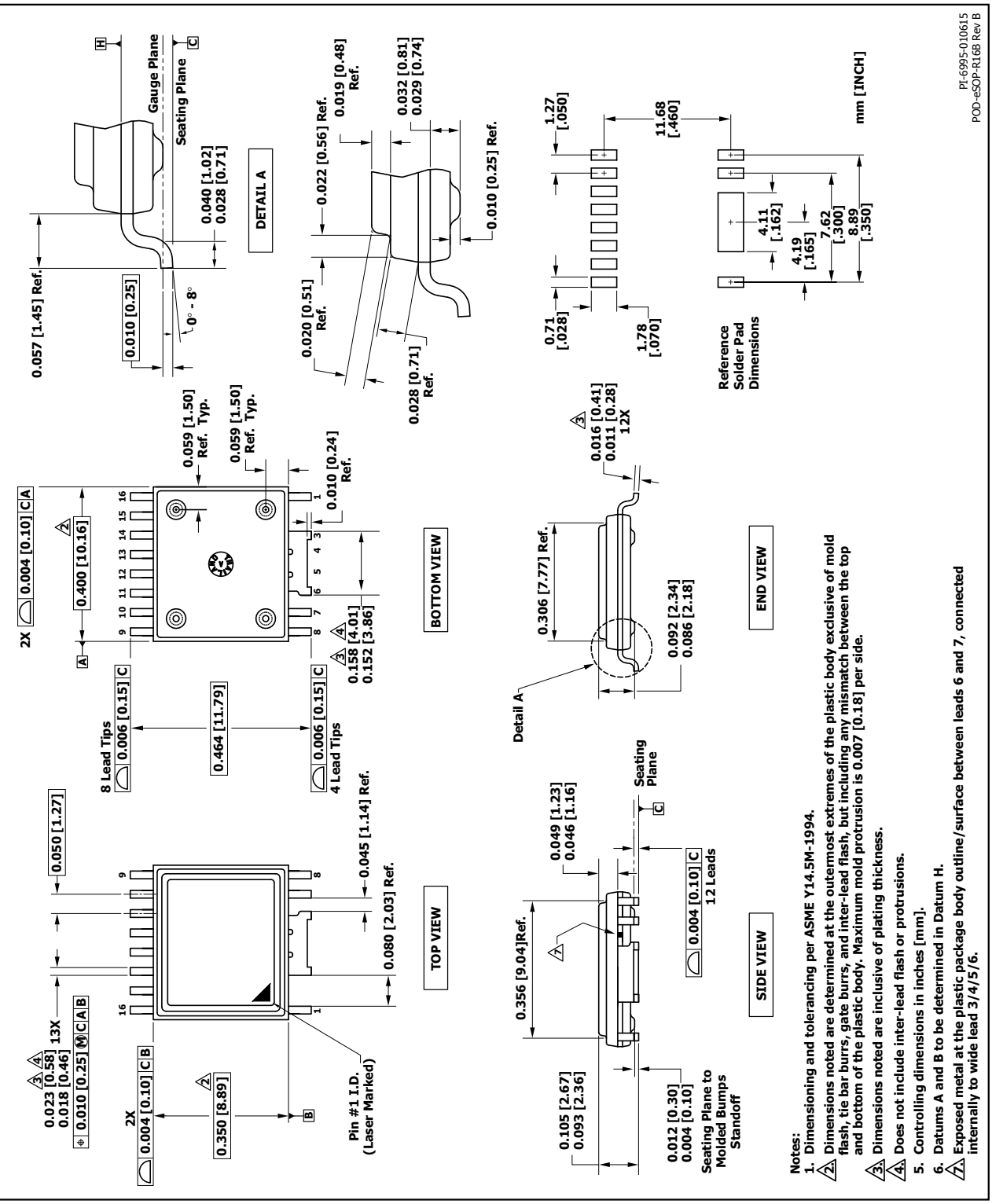


Figure 28. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

eSOP-R16B

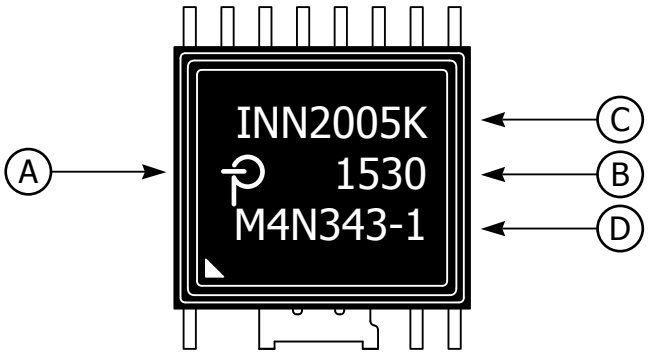


Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined in Datum H.
7. Exposed metal at the plastic package body outline/surface between leads 6 and 7, connected internally to wide lead 3/4/5/6.

PI-6995-010615
POD-eSOP-R16B Rev B

PACKAGE MARKING

eSOP-R16B



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-7765-102715

Part Ordering Table

Product	Cable Compensation
INN2003 INN2023	0% 6%
INN2004 INN2024	0% 6%
INN2005 INN2025	0% 6%

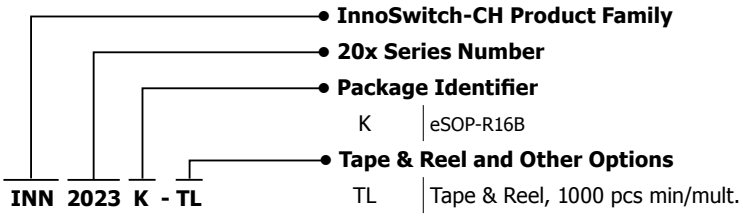
MSL Table

Part Number	MSL Rating
INN2003 INN2023	3
INN2004 INN2024	3
INN2005 INN2025	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 V (max) on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Machine Model ESD	JESD22-A115C	> ±200 V on all pins

Part Ordering Information



Revision	Notes	Date
A	Initial Release.	11/14
B	Added Note 4 to Table 1, updated Auto-Restart section, added $V_{FB(OFF)}$ to Parameter Table, new Figure 23, added Part Ordering Table and added Notes 6 and 7 to Absolute Maximum Ratings table.	01/15
C	Corrected secondary auto-restart from relative specification on the FEEDBACK pin to absolute threshold on the VOUT pin, that was incorrectly documented in previous revision. Updated $I_{SR(PD)}$, $I_{SR(PU)}$ and V_{BPP} limits based on high volume production data.	05/15
D	Added extra information related to Cable Drop Compensation (CDC) function on page 5.	07/15
E	Updated in line with UL Report E358471. Increased Storage, Operating Junction, and Ambient Temperatures and Secondary-Side Current Rating Parameters. Previous Note 7 in Abs Max Ratings Table is no longer required and deleted. Updated Figure 5, page 1 and $R_{DS(ON)}$ Condition parameter.	08/15
F	Corrected Bottom (Left side) of PCB layout in Figure 20, SOURCE (S) Pin description on page 3, added ESD table and eSOP-R16B Package Marking.	11/15
G	Modified page 1 sub-header text.	11/18/15
H	Corrected OUTPUT VOLTAGE Pin Auto-Restart Threshold section. Improved $V_{OUT(AR)}$ limits tolerance, 3.5 V Max.	12/04/15
I	Added Pin 8 and Pin 9 information under Pin Functional Description on page 3.	04/17
J	Corrected error in Figure 4. Updated text and added 4 new waveform schematics in Bias Winding and External Bias Circuit section. Added 1 new figure in Applications Example section.	10/17
K	Updated safety information on page 1.	06/20

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World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
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Germany
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India
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Italy
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Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
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e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
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Phone: +65-6358-2160
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Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
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Taipei 11493, Taiwan R.O.C.
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e-mail: taiwansales@power.com

UK
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