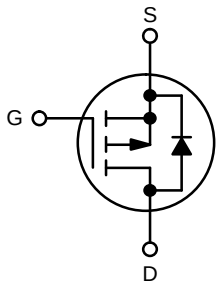
MOSFET – P-Channel, QFET®

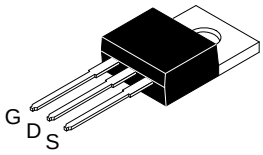
-60 V, -47 A, 26 mΩ

FQP47P06

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
−60 V	26 mΩ @ −10 V	−47 A



P−Channel MOSFET



TO−220−3LD
CASE 340AT

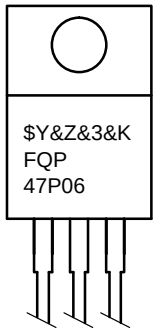
Description

This P−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- −47 A, −60 V, $R_{DS(on)}$ = 26 mΩ (Max.) @ V_{GS} = −10 V, I_D = −23.5 A
- Low Gate Charge (Typ. 84 nC)
- Low Crss (Typ. 320 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating

MARKING DIAGRAM



$Y	= Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Plant Code
&K	= 2−Digits Lot Run Traceability Code
FQP47P06	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FQP47P06	TO−220−3LD	1000 Units / Tube

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

Symbol	Parameter		FQP47P06	Unit
V_{DSS}	Drain−Source Voltage		−60	V
I_D	Drain Current	− Continuous (T_C = 25°C)	−47	A
		− Continuous (T_C = 100°C)	−33.2	A
I_{DM}	Drain Current (Note 1)	− Pulsed	−188	A
V_{GSS}	Gate−Source Voltage		±25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		820	mJ
I_{AR}	Avalanche Current (Note 1)		−47	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		16	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		−7.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		160	W
		− Derate above 25°C	1.06	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 0.43 mH, I_{AS} = −47 A, V_{DD} = −25 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ −47 A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

THERMAL CHARACTERISTICS

Symbol	Characteristic	FQP47P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	0.94	°C/W
$R_{\theta CS}$	Thermal Resistance, Case−to−Sink, Typ.	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−60	−	−	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	−	−0.06	−	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −60 V, V_{GS} = 0 V	−	−	−1	μA
		V_{DS} = −48 V, T_C = 150°C	−	−	−10	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = −25 V, V_{DS} = 0 V	−	−	−100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V	−	−	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−2.0	−	−4.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −23.5 A	−	0.021	0.026	Ω
g_{FS}	Forward Transconductance	V_{DS} = −30 V, I_D = −23.5 A (Note 4)	−	21	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −25 V, V_{GS} = 0 V, f = 1.0 MHz	−	2800	3600	pF
C_{oss}	Output Capacitance		−	1300	1700	pF
C_{rss}	Reverse Transfer Capacitance		−	320	420	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −30 V, I_D = −23.5 A, R_G = 25 Ω (Note 4, 5)	−	50	110	ns
t_r	Turn−On Rise Time		−	450	910	ns
$t_{d(off)}$	Turn−Off Delay Time		−	100	210	ns
t_f	Turn−Off Fall Time		−	195	400	ns
Q_g	Total Gate Charge	V_{DS} = −48 V, I_D = −47 A, V_{GS} = −10 V (Note 4, 5)	−	84	110	nC
Q_{gs}	Gate−Source Charge		−	18	−	nC
Q_{gd}	Gate−Drain Charge		−	44	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATING						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	−47	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		−	−	−188	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −47 A	−	−	−4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = −47 A, dI_F / dt = 100 A/μs (Note 4)	−	130	−	ns
Q_{rr}	Reverse Recovery Charge		−	0.55	−	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width ≤ 300 μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

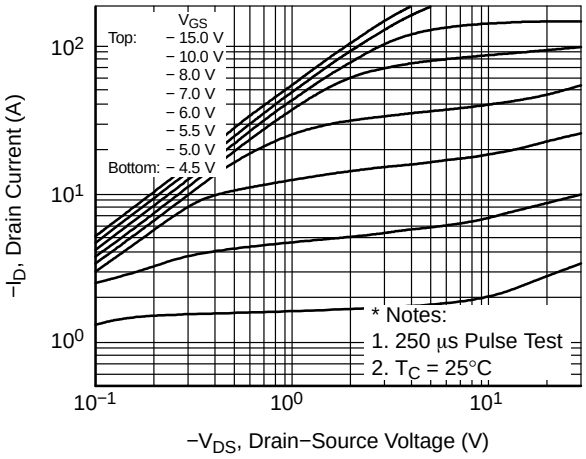

Figure 1. On−Region Characteristics

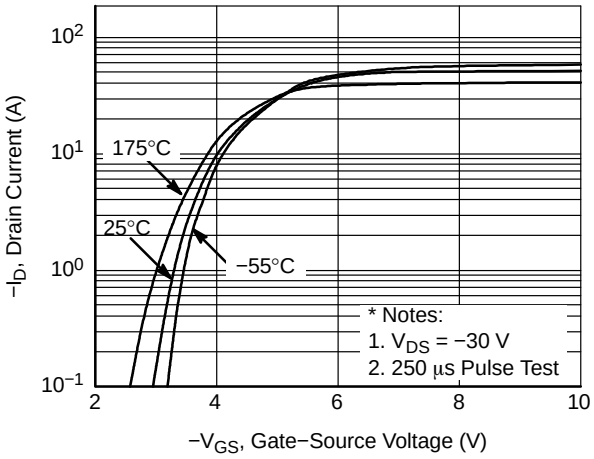

Figure 2. Transfer Characteristics

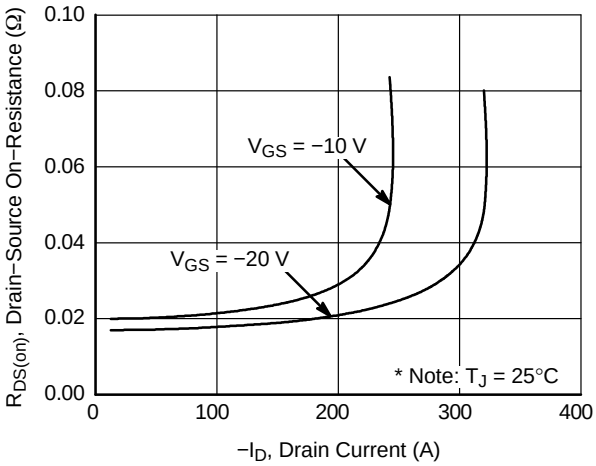

Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

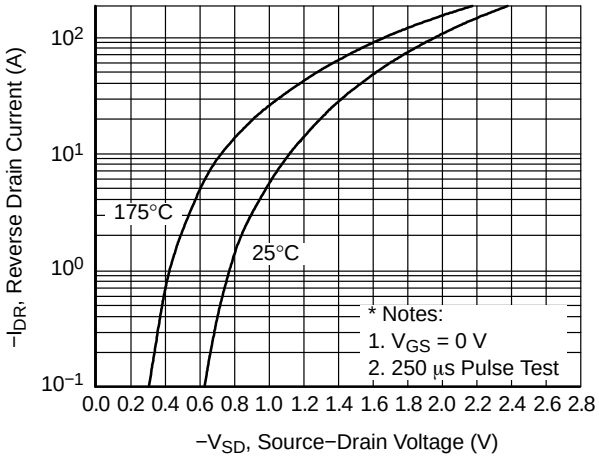

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

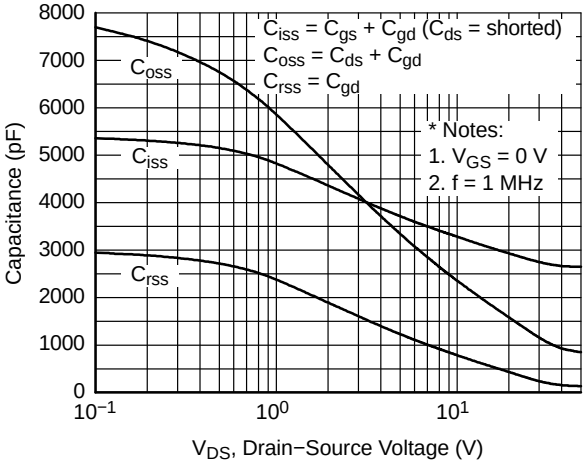

Figure 5. Capacitance Characteristics

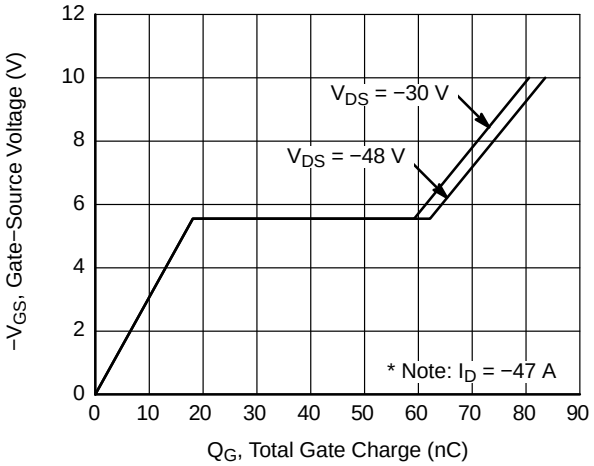

Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (Continued)

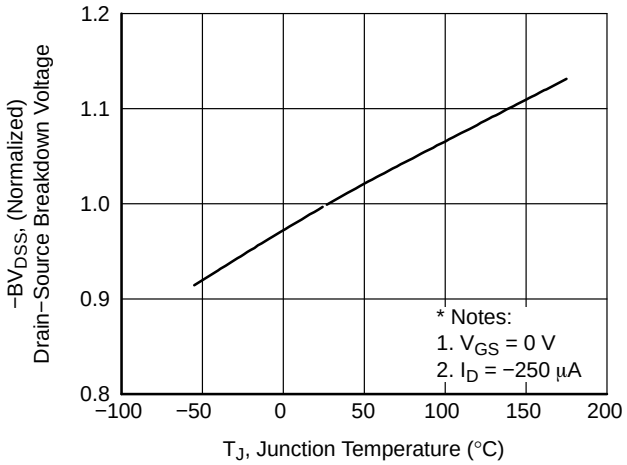

Figure 7. Breakdown Voltage Variation vs. Temperature

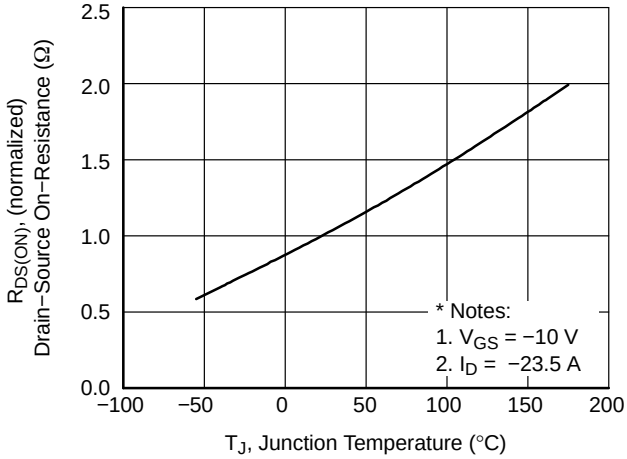

Figure 8. On−Resistance Variation vs. Temperature

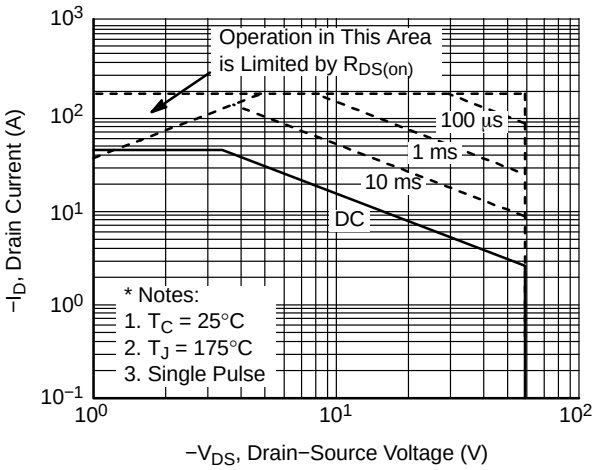

Figure 9. Maximum Safe Operating Area

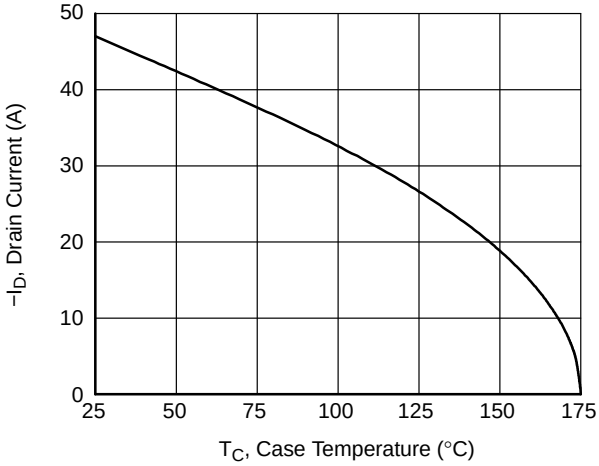

Figure 10. Maximum Drain Current vs. Case Temperature

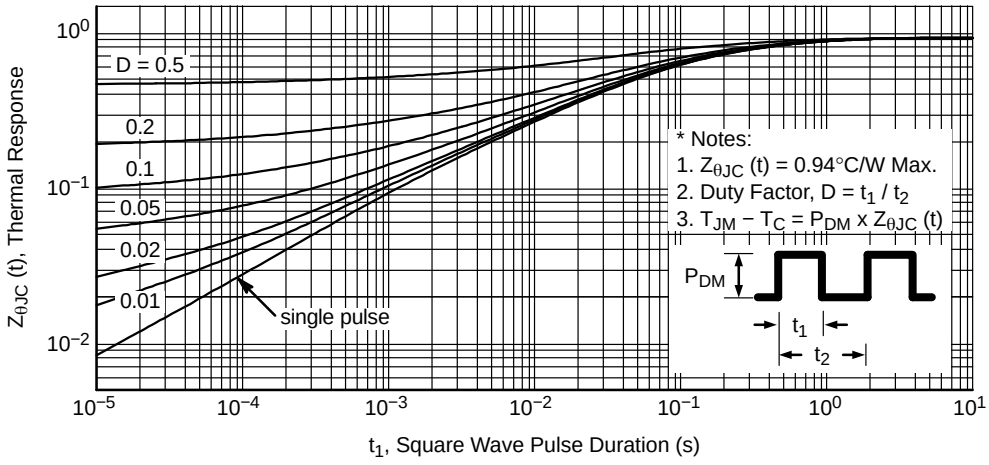

Figure 11. Transient Thermal Response Curve

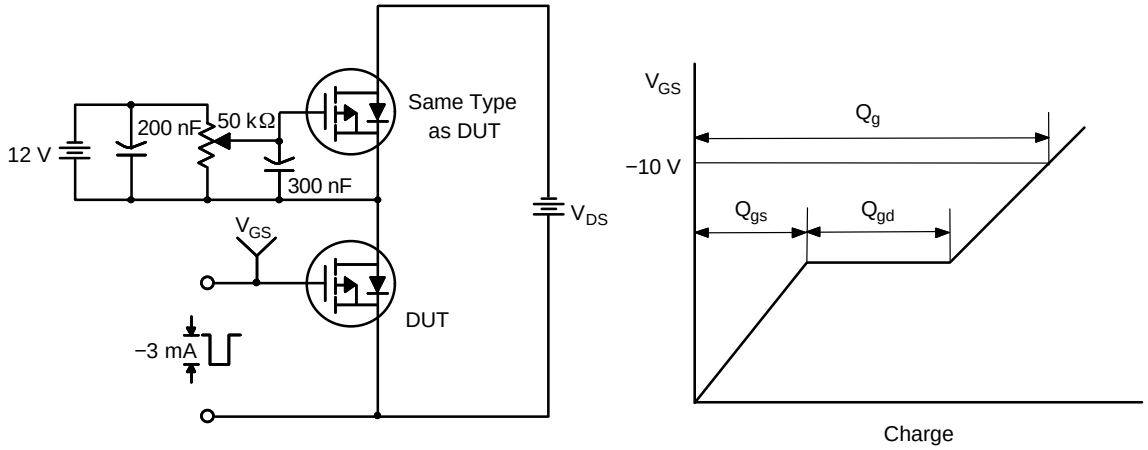

Figure 12. Gate Charge Test Circuit & Waveform

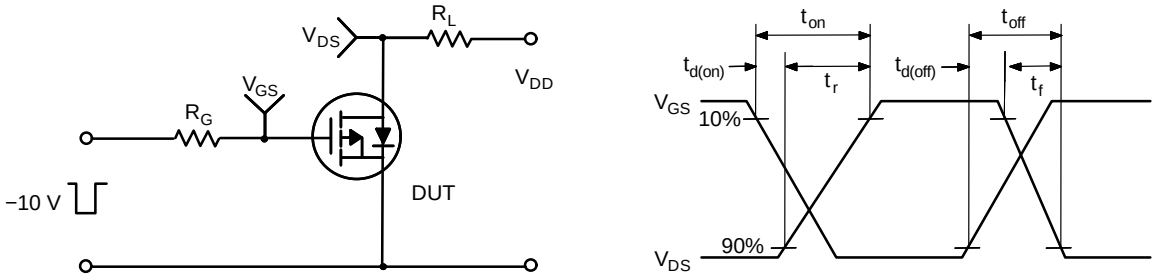

Figure 13. Resistive Switching Test Circuit & Waveforms

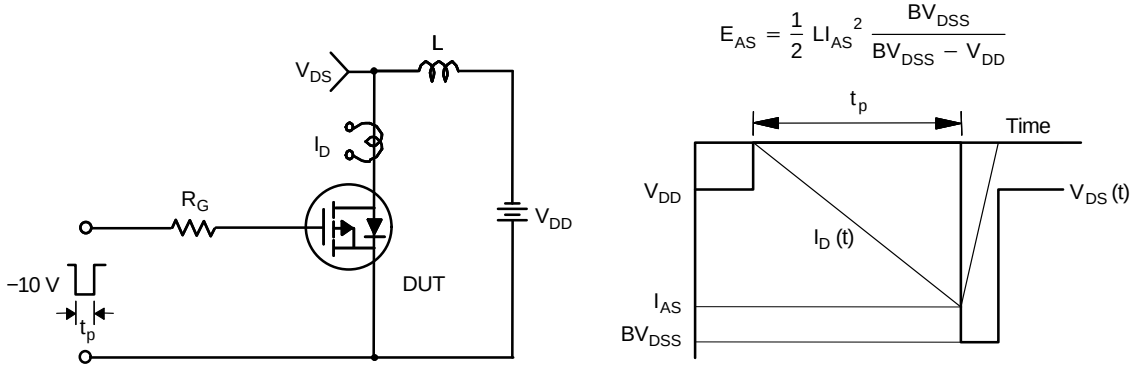

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

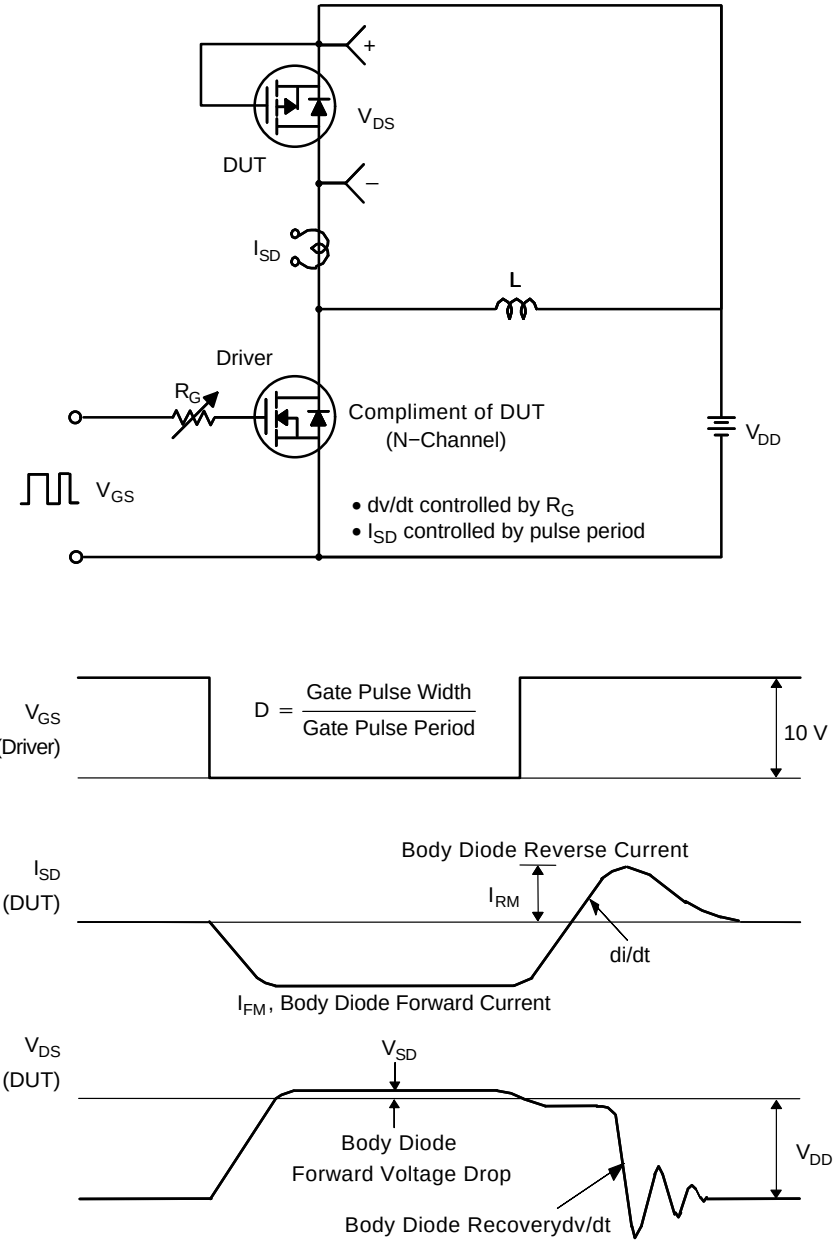

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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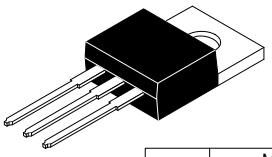
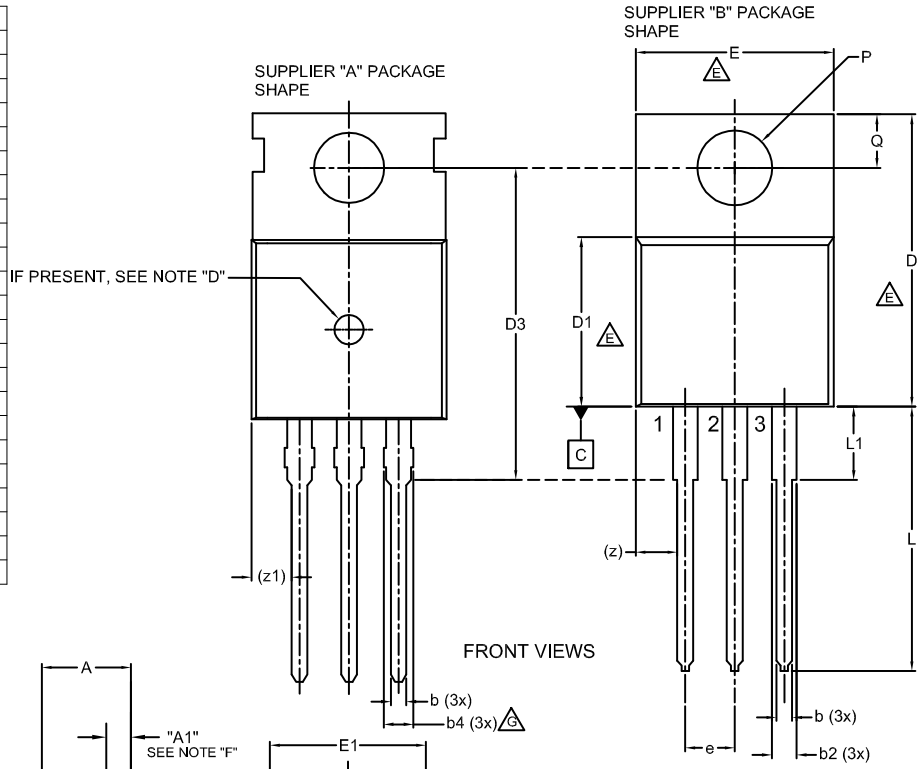
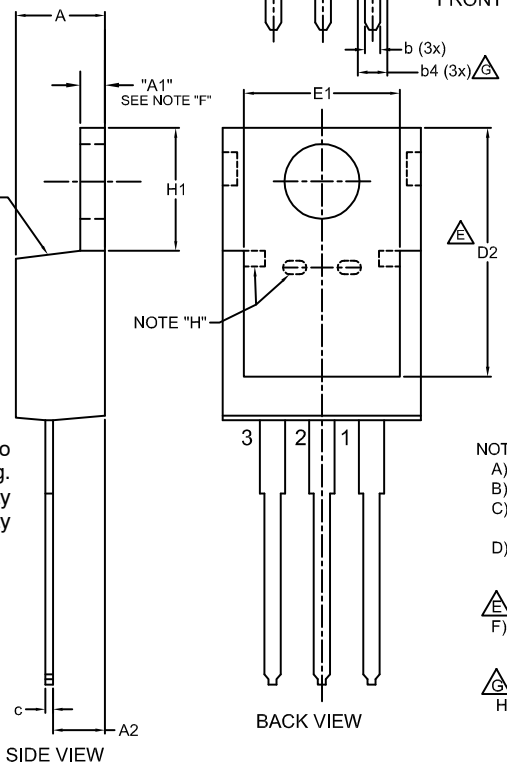


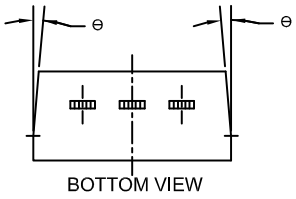
TO−220−3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
Θ	3°	–	5°







GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

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