MOS FET

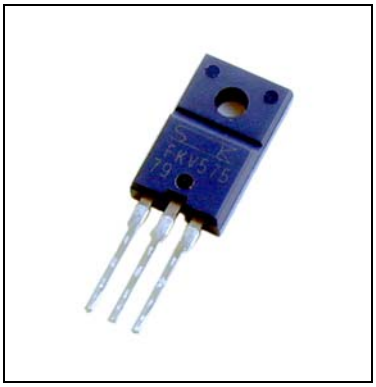
FKV575

November, 2008

■Features

- High Current Capability (ID:75A (DC))
- Low on-resistance (RDS(on):7mΩ typ)
- Avalanche energy guarantee

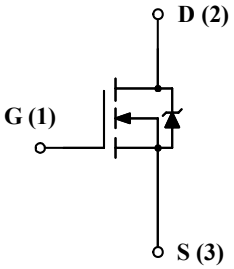
■Package----FM20(TO220 Full Mold)



■Applications

- DC-DC Converters
- High speed switching

■Equivalent circuit



Absolute maximum ratings

(Ta=25°C)

Characteristic	Symbol	Rating	Unit
Drain to Source Voltage	VDSS	50	V
Gate to Source Voltage	VGSS	±20	V
Continuous Drain Current	ID	±75A	A
Pulsed Drain Current	ID(pulse) 1)	±200A	A
Maximum Power Dissipation	PD	40 (Tc=25°C)	W
Single Pulse Avalanche Energy	EAS 2)	300	mJ
Avalanche Current	IAS	75	A
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	−55 to 150	°C

1) PW≤100μs, duty cycle≤1%

2) VDD=20V,L=64μH, ILp=75A,unclamped,RG=50Ω, See Fig.1

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Electrical characteristics

(Ta=25°C)

Characteristic	Symbol	Test Conditions	Limits			Unit
			MIN.	TYP.	MAX.	
Drain to Source breakdown Voltage	V(BR)DSS	ID=100μA,VGS=0V	50			V
Gate to Source Leakage Current	IGSS	VGS=±20V			±100	nA
Drain to Source Leakage Current	IDSS	VDS=50V, VGS=0V			100	μA
Gate Threshold Voltage	VTH	VDS=10V, ID=250μA	3.0		4.5	V
Forward Transconductance	Re(Yfs)	VDS=10V, ID=37A	30			S
Static Drain to Source On-Resistance	RDS(on)	ID=37A, VGS=10V		7	10	mΩ
Input Capacitance	Ciss	VDS=10V VGS=0V f=1MHz		3200		pF
Output Capacitance	Coss			1800		
Reverse Transfer Capacitance	Crss			750		
Turn-On Delay Time	td(on)	ID=37A, VDD≈25V RL=0.7Ω, VGS=10V RG=10Ω See Fig.2		40		ns
Rise Time	tr			280		
Turn-Off Delay Time	td(off)			130		
Fall Time	tf			120		
Total Gate Charge	Qg	ID=37A, VDD≈25V RL=0.7Ω, VGS=10V		70		nC
Gate to Source Charge	Qgs			15		
Gate to Drain Charge	Qgd			30		
Source-Drain Diode Forward Voltage	VSD	ISD=75A,VGS=0V		1.0	1.5	V

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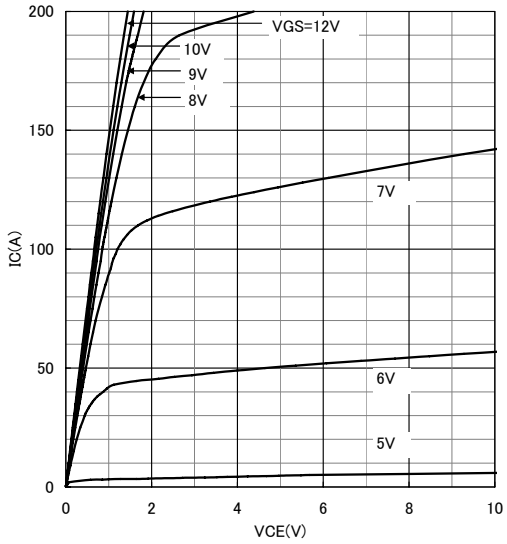
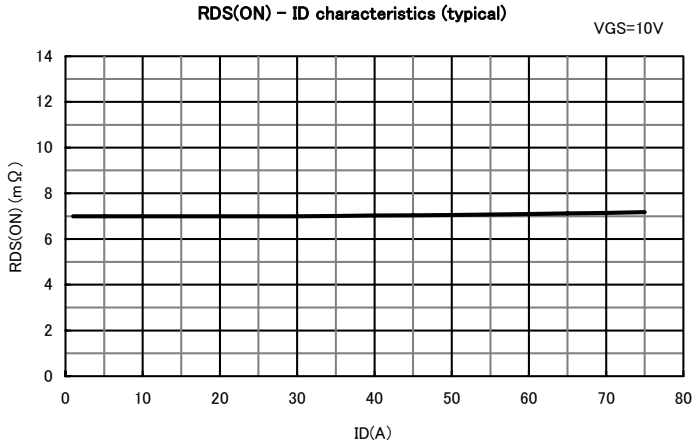
Characteristic Curves (Tc=25℃)

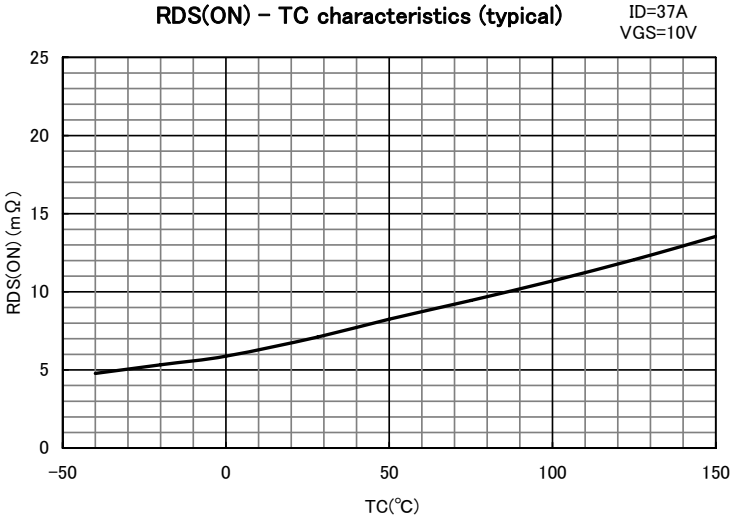
ID – VDS characteristics (typical)



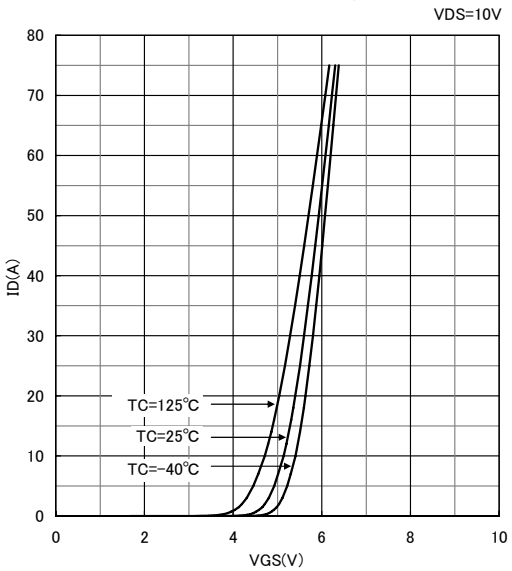
RDS(ON) – ID characteristics (typical)



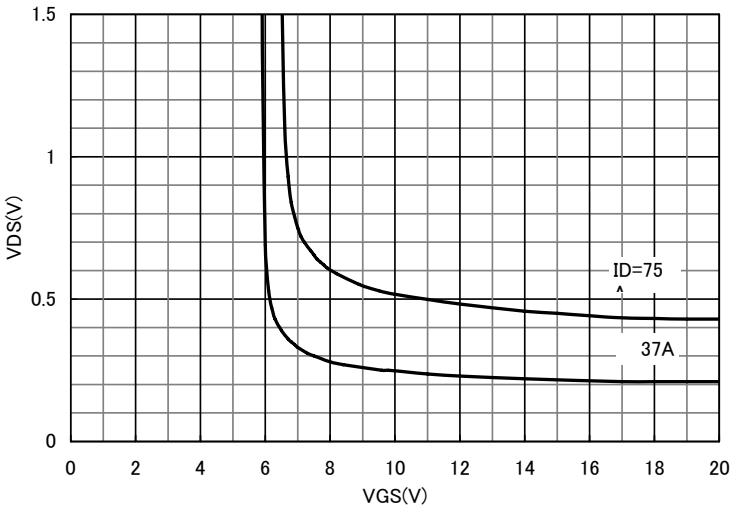
RDS(ON) – TC characteristics (typical)



ID – VGS characteristics (typical)



VDS–VGS characteristics (typical)



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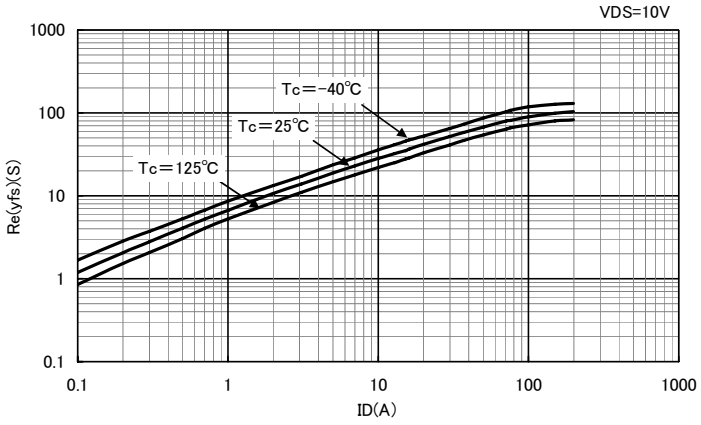
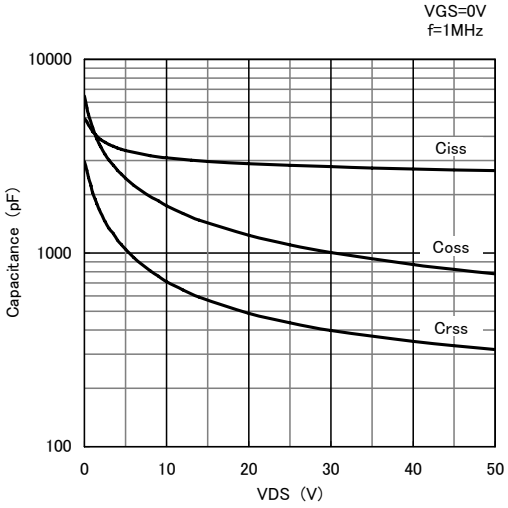
Characteristic Curves (Tc=25℃)

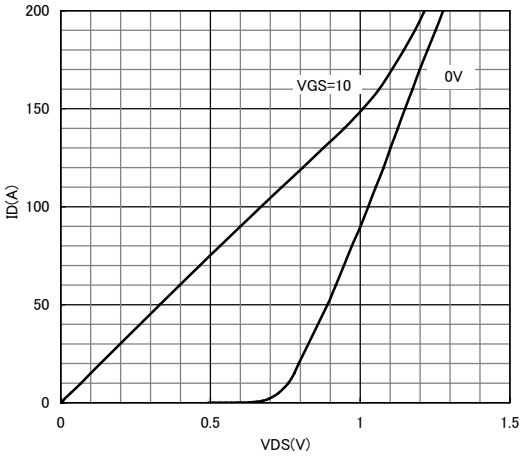
Re(yfs) – ID characteristics (typical)



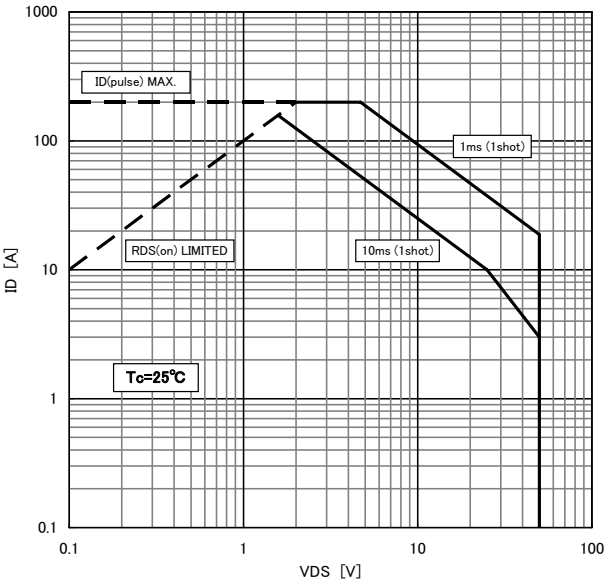
Capacitance—VDS characteristics (typical)



IDR-VSD characteristics (typical)



SAFE OPERATING AREA



PD — Ta characteristics

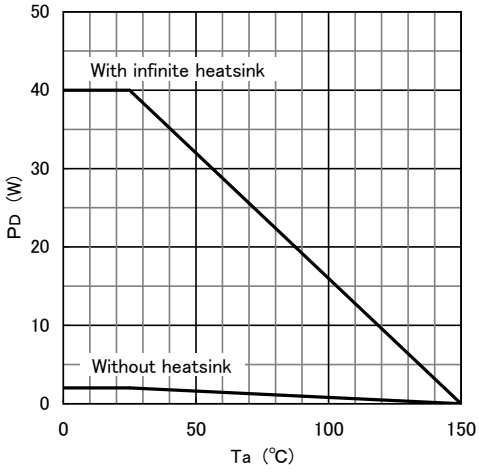
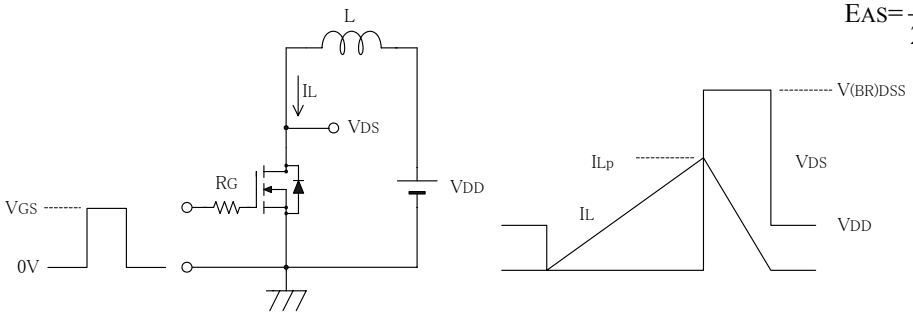


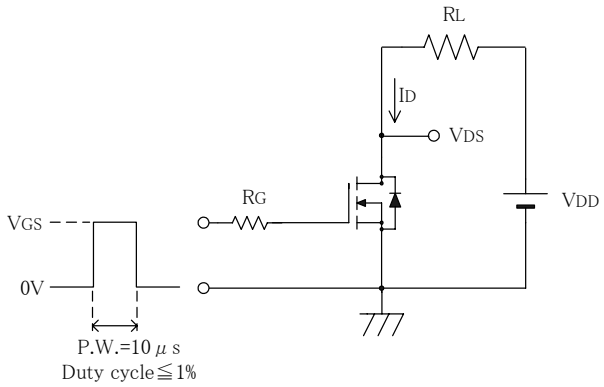
Fig.1 Unclamped Inductive Test Method

$$E_{AS}=\frac{1}{2}\cdot L\cdot I_{LP}^{2}\cdot\frac{V_{(BR)DSS}}{V_{(BR)DSS}-V_{DD}}$$



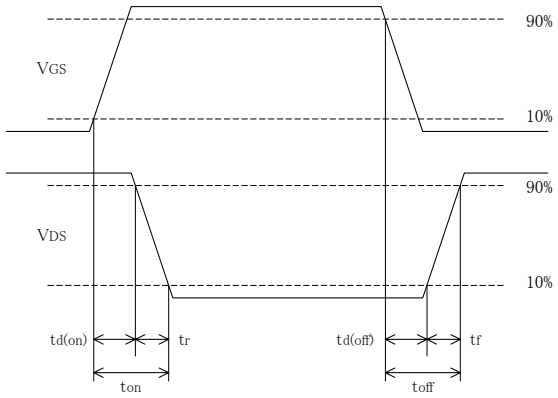
(a) Test Circuit (b) Waveforms

Fig.2 Switching Time Test Method



VDD≈25V
ID=37A
RL=0.7 Ω
VGS=10V
RG=5 Ω

(a) Test Circuit



(b) Waveforms

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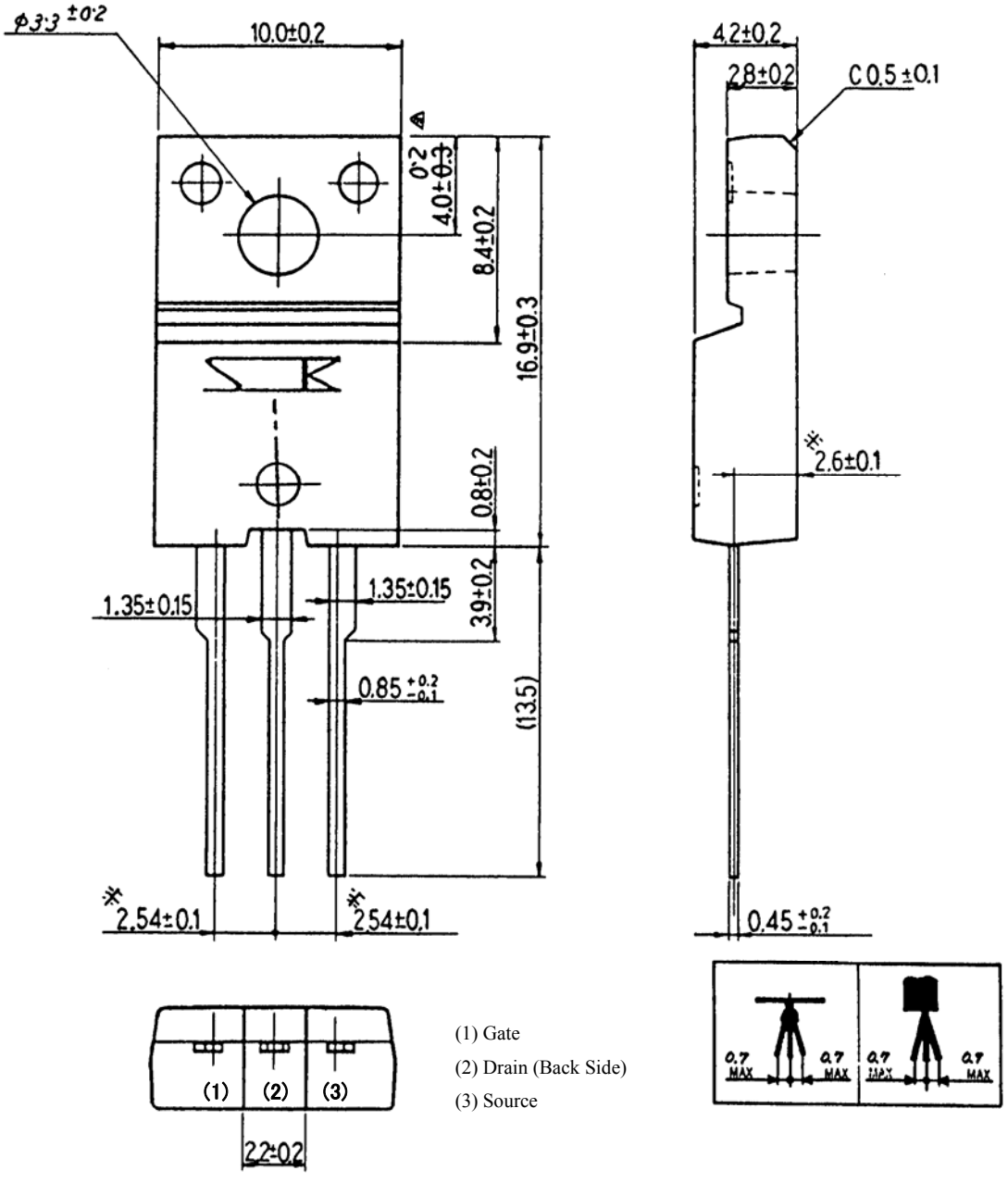
Outline

FM20 (TO220 Full Mold)



(1) Gate
(2) Drain (Back Side)
(3) Source

Weight Approx. 2g

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