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FAIRCHILD SEMICONDUCTOR®

February 2026

FDS5351

N-Channel PowerTrench® MOSFET

60V, 6.1A, 35mΩ

Features

- Max $r_{DS(on)}$ = 35mΩ at V_{GS} = 10V, I_D = 6.1A
- Max $r_{DS(on)}$ = 42mΩ at V_{GS} = 4.5V, I_D = 5.5A
- High performance trench technology for extremely low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- Inverter Switch
- Synchronous Rectifier
- Load Switch

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MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			60	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous			6.1	A
	-Pulsed			30	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	73	mJ
P_D	Power Dissipation	T_A = 25°C	(Note 1a)	5	W
	Power Dissipation	T_A = 25°C	(Note 1b)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS5351	FDS5351	SO-8	13''	12mm	2500units

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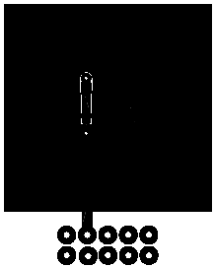
Electrical Characteristics T_J = 25°C unless otherwise noted

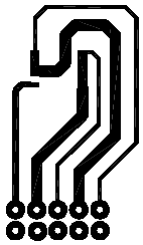
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		55		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48V, V_{GS} = 0V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-6.2		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 6.1A		26..	35.0	mΩ
		V_{GS} = 4.5V, I_D = 5.5A		32.4	42.0	
		V_{GS} = 10V, I_D = 6.1A, T_J= 125°C		..	58.8	
g_{FS}	Forward Transconductance	V_{DD} = 5V, I_D = 6.1A		24		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 30V, $V_{..}$ = 0V, f = 1MHz		985	1310	pF
C_{oss}	Output Capacitance			90	120	pF
C_{rss}	Reverse Transfer Capacitance			50	75	pF
R_g	Gate Resistance	f = 1MHz		1.7		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30V, I_D = 6.1A, V_{GS} = 10V, R_{GEN} = 6Ω		8	16	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			21	34	ns
t_f	Fall Time			2	10	ns
Q_g	Total Gate Charge	V_{GS} = 0V to 10V, V_{DD} = 30V, I_D = 6.1A		19	27	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 4.5V		9	13	nC
Q_{gs}	Gate to Source Charge			3		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 6.1A (Note 2)		0.82	1.3	V
		V_{GS} = 0V, I_S = 2.1A (Note 2)		0.76	1.2	
t_{rr}	Reverse Recovery Time	I_F = 6.1A, di/dt = 100A/μs		24	38	ns
Q_{rr}	Reverse Recovery Charge			15	27	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. UIL condition: Starting T_J = 25°C, L = 3mH, I_{AS} = 7A, V_{DD} = 60V, V_{GS} = 10V.

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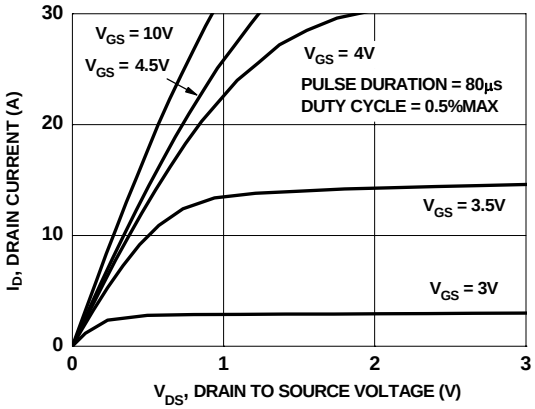

Figure 1. On-Region Characteristics

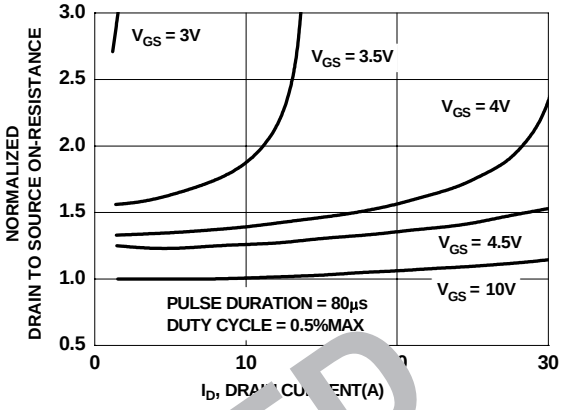

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

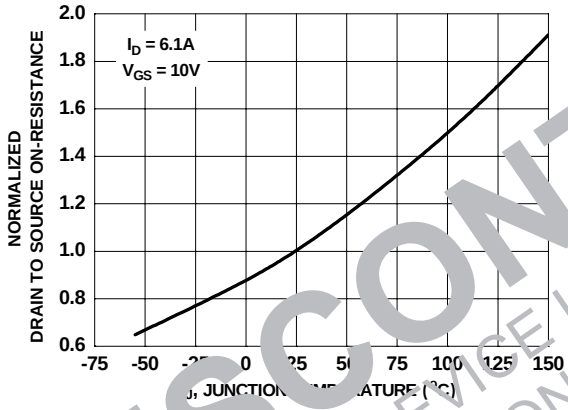

Figure 3. Normalized On-Resistance vs Junction Temperature

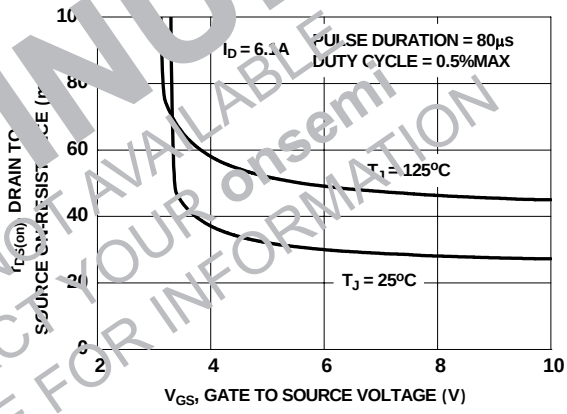

Figure 4. On-Resistance vs Gate to Source Voltage

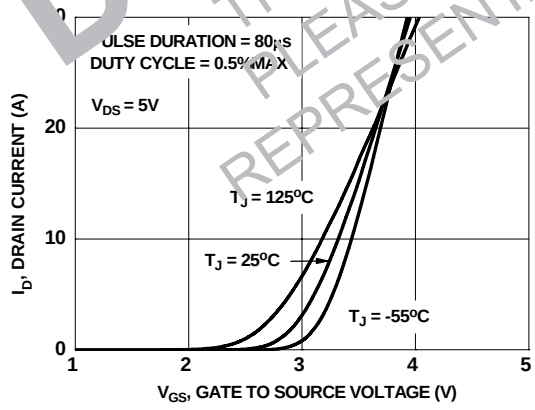

Figure 5. Transfer Characteristics

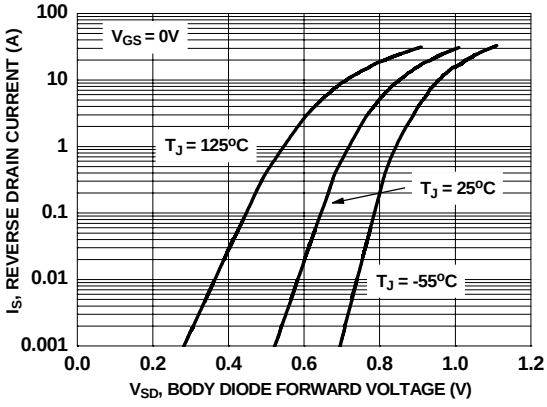

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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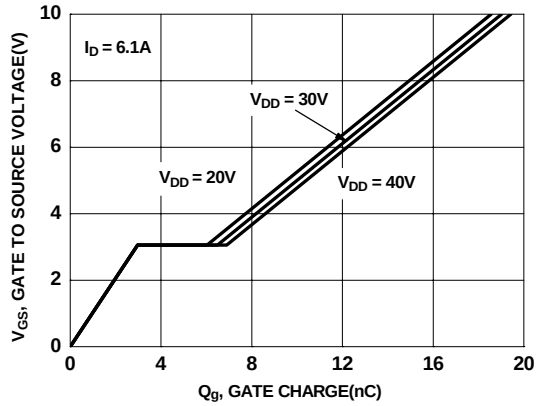

Figure 7. Gate Charge Characteristics

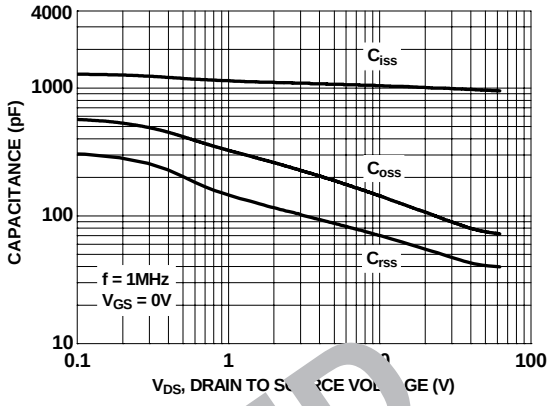

Figure 8. Capacitance vs Drain to Source Voltage

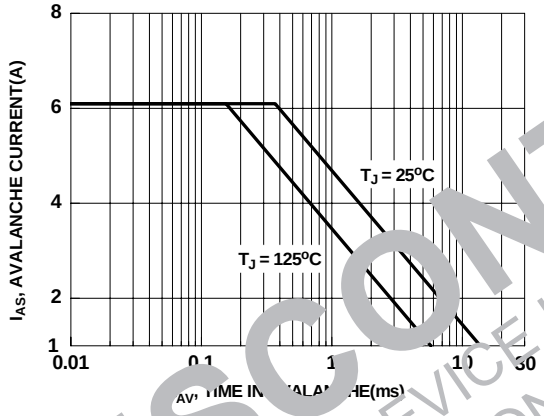

Figure 9. Unclamped Inductive Switching Capability

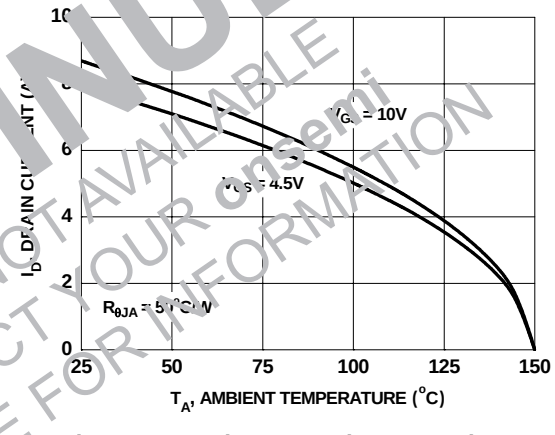

Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

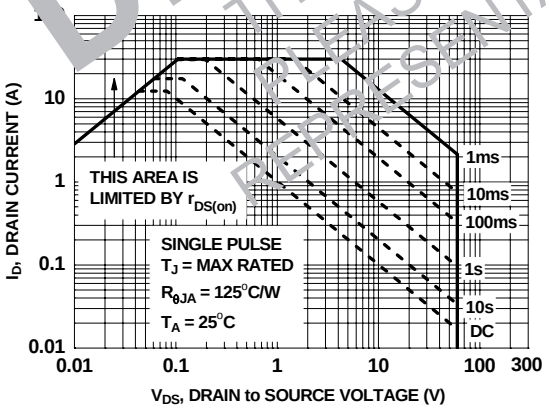

Figure 11. Forward Bias Safe Operating Area

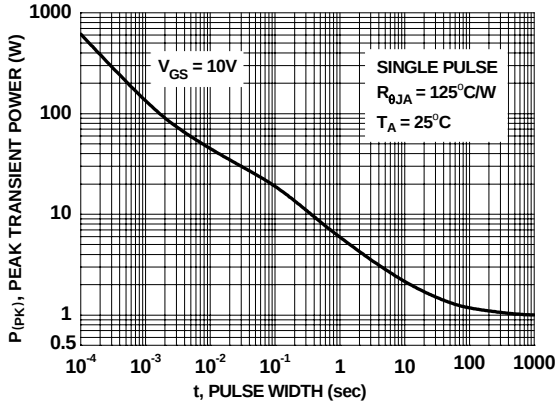

Figure 12. Single Pulse Maximum Power Dissipation

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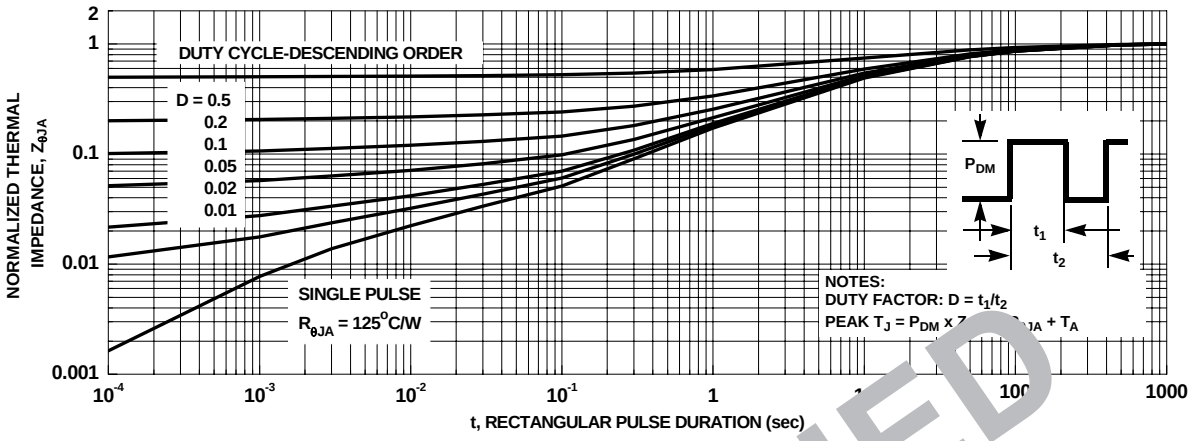

Figure 13. Transient Thermal Response Curve

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