Design Example Report

Title	***72 W Power Supply Using InnoSwitch™4-CZ PowiGaN™ INN4074C-H185, ClampZero™ CPZ1075M, MinE-CAP™ MIN1072M***
Specification	90 VAC – 265 VAC Input; 12 V / 6.0 A Output
Application	Industrial Power Supply
Author	Applications Engineering Department
Document Number	DER-931
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Revision	1.0

Summary and Features

- InnoSwitch4-CZ - active clamp flyback switcher IC with integrated high-voltage PowiGaN, synchronous rectification and FluxLink™ feedback
- Zero voltage switching in both CCM and DCM operating conditions
- All the benefits of secondary-side control with the simplicity of primary-side regulation
    - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 efficiency requirement
- Integrated thermal protection
- <50 mW no-load input power typically (At 230 VAC)
- Output voltage regulation: <±2%, Output ripple: <2%
- Primary sensed overvoltage protection / Output sensed overcurrent protection
- Meets CISPR22 / EN55022 Class B Conducted EMI
- Very high power density: 28.1 W/in^3 without enclosure (72 W / 2.76 in X 1.18 in X 0.79 in)

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 12 V / 6 A output power supply using the InnoSwitch4-CZ INN4074C-H185, ClampZero CPZ1075M, and MinE-CAP MIN1072M. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch4-CZ active clamp controller providing exceptional performance and is paired with the input capacitor volume-reduction capabilities of the MinE-CAP IC.

This document contains the power supply specification, schematic diagram, bill of materials, transformer documentation, printed circuit board layout, and performance data.

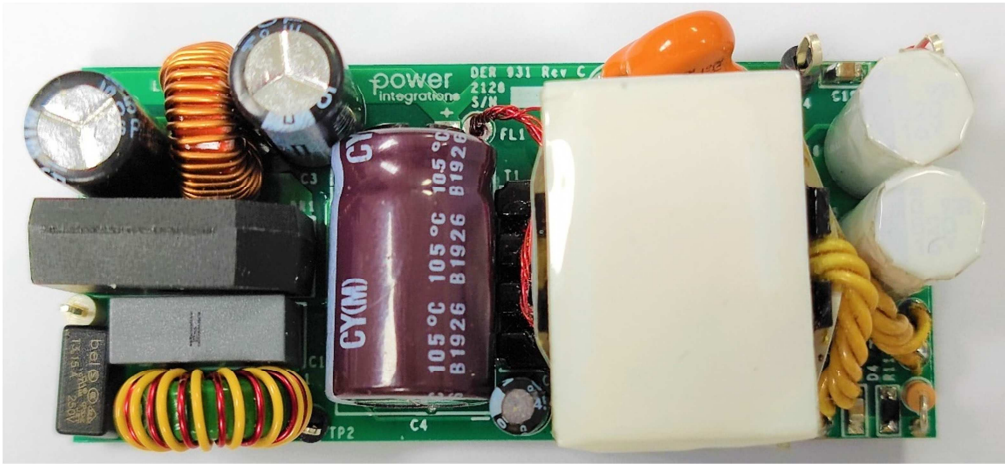


Figure 1 – Populated Circuit Board Photograph, Top.

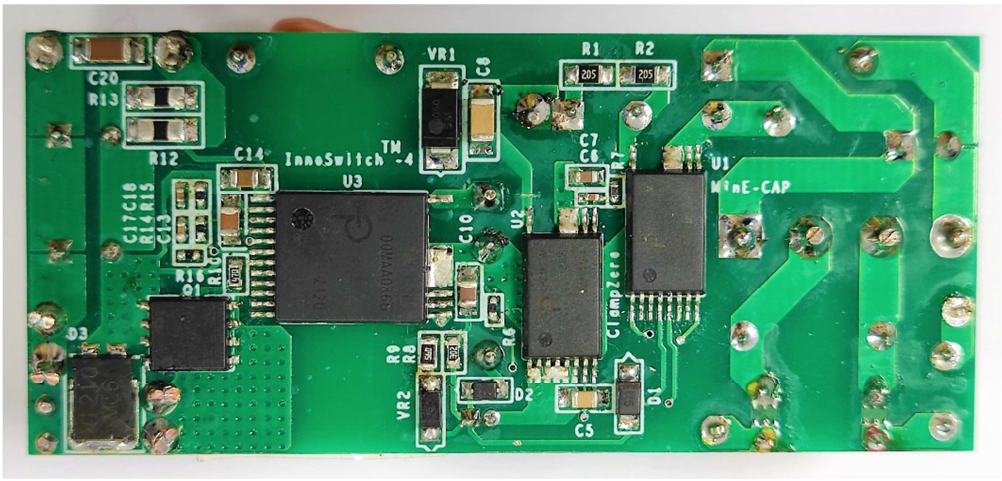


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				50	mW	Measured at 230 VAC.
12 V Output						
Voltage	V_{OUT1}		12		V	± 2%
Current	I_{OUT}	6			A	On Board.
Continuous Power	P_{OUT}			72	W	
Line Regulation						
Load Regulation				2	%	
Ripple Voltage	V_{RIPPLE}			250	mV	On Board.
DoE Average Efficiency				88	%	
CoC Average Efficiency				89	%	
CoC 10% Efficiency				79	%	
Thermals						
Board/Component Temperature				110	°C	Open Frame, Sea Level. Ambient: 24 °C.
Conducted EMI						Meets CISPR22B / EN55022B
Safety						Designed to meet IEC60950 / UL1950 Class II.

3 Schematic

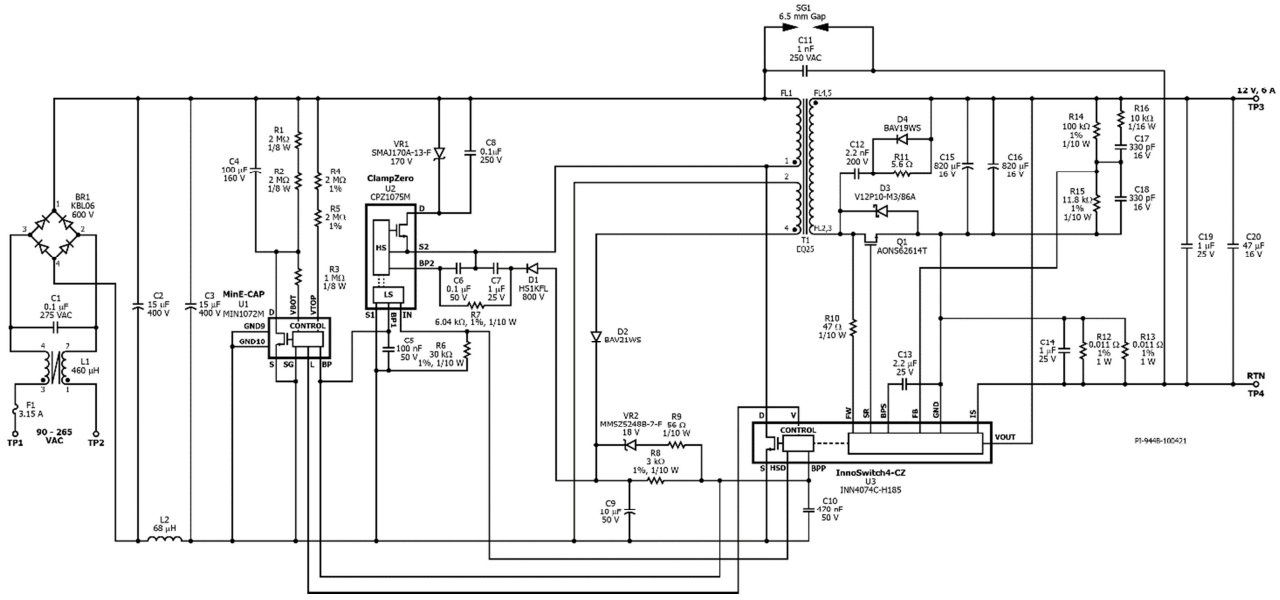


Figure 3 – Schematic.

4 Circuit Description

4.1 *Input Rectifier and EMI Filtering*

Input fuse F1 isolates the circuit and provides protection from component failure. Inductor L1, L2 along with capacitor C1 provide EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors C2, C3 and C4. Y capacitor C11 connected between the power supply output and input helps to reduce common mode EMI.

4.2 *InnoSwitch4-CZ IC Primary*

One end of the transformer primary is connected to the rectified DC bus, while the other is connected to the drain terminal of the PowiGaN switch inside the InnoSwitch4-CZ IC (U3).

The V pin of the InnoSwitch4-CZ IC is connected directly to the L pin of the MinE-CAP IC. Resistors R4 and R5 provide input voltage sensing for both the MinE-CAP IC and InnoSwitch4-CZ ICs. The MinE-CAP IC uses resistors R4 and R5 to monitor the line voltage as well as the voltage across the high-voltage bulk capacitor, C4. Resistor R1 and R2 are bleeder resistors used to help regulate the voltage across C4, while resistor R3 is used by the MinE-CAP IC to sample the voltage at the negative terminal of C4. The MinE-CAP IC combines the information from the VTOP and VBOT pins to determine and control the voltage across the low-voltage bulk capacitor, C4. The InnoSwitch4-CZ IC uses the current from the L pin to determine line under voltage and over voltage conditions. During regular operation, the current from the L pin follows the value of the current flowing through R4 and R5. Thus, the InnoSwitch4-CZ IC operates as if said resistors are directly connected to the V pin. For this specific design, bypass capacitor C5 is shared by both the BPP pin of the InnoSwitch4-CZ IC and the BP pin of the MinE-CAP IC. The value of C10 is chosen based on the desired current limit of the InnoSwitch4-CZ IC. The BYPASS pin of InnoSwitch4-CZ IC also supplies the ClampZero IC (U2) BP1 pin during start-up.

The primary clamp capacitor C8 limits the peak drain voltage of U3 at the instant of turn-off of the PowiGaN switch inside U3. The energy stored in the leakage inductance of transformer T1 will be transferred to capacitor C8. Part of the magnetizing energy will also get transferred to C8 depending on the capacitance value used. Zener diode VR1 is used as a fail-safe to protect the InnoSwitch4-CZ IC from excessive drain voltages if there is any malfunction of the power supply.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4-CZ IC generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U2) turns on, to achieve soft switching of the InnoSwitch4-CZ primary switch, clamp capacitor C8 starts to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer

in the case of DCM operation. A small delay is provided from the instant the high-side switch turns off to achieve zero voltage switching on the primary switch. This delay is programmable by different resistor values of R6.

Capacitor C5 is used to provide local decoupling at the BP1 pin of IC U2. Capacitor C6 provides the decoupling for BP2 pin. Diode D1 and capacitor C7 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R7 limits the current flowing into the BP2 pin.

The InnoSwitch4-CZ IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor C10 when AC is first applied. During normal operation, the primary-side block is powered by a bias winding on the transformer T1. Output of this bias winding is rectified using diode D2 and filtered using capacitor C9 to provide a constant voltage source to supply BPP pin of U3 through resistor R8. Resistor R8 limits the current being supplied to the PRIMARY BYPASS pin of InnoSwitch4-CZ IC U3.

Output regulation is achieved using modulation control, where the frequency and I_{LIM} of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of I_{LIM} in the selected I_{LIM} range, and at light load or no-load, most cycles are disabled, and the ones enabled have a low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR2 with current limiting resistor R9. In a flyback converter, output of the bias winding tracks the output voltage of the converter by the winding turns-ratio. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2, which then causes a current to flow into the BPP pin of InnoSwitch4-CZ IC U3. If the current flowing into the BPP pin increases above the I_{SD} threshold, the U3 controller auto-restarts to prevent any further increase in output voltage.

4.3 *InnoSwitch4-CZ IC Secondary*

The secondary-side of the InnoSwitch4-CZ IC provides output voltage, output current sensing, and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FET Q1 and diode D3 and filtered by capacitors C15 and C16. Capacitor C19 and C20 are used to reduce the high-frequency output voltage ripple. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RCD snubber R11, C12, and D4. Diode D4 minimizes the dissipation in resistor R11.

The gate of Q1 is turned on by the secondary-side controller of IC U3, based on the winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below $V_{SR(TH)}$.

The secondary-side of the IC U3 is self-powered from either the secondary winding forward voltage or the output voltage. However, to improve the system efficiency and reduce the secondary-side internal consumption, a bias winding circuit can be used. Capacitor C13 connected to the BPS pin of InnoSwitch4-CZ U3 provides decoupling for the internal circuitry.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R14 and R15. The voltage across R15 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. The output voltage is regulated to achieve a voltage of 1.265 V on the FB pin. Capacitor C18 provides noise filtering of the signal at the FB pin.

Output current is sensed by monitoring the voltage drop across resistors R12 and R13 between the IS and SECONDARY GROUND pins. A threshold of approximately 35 mV reduces losses. C14 provides filtering on the IS pin from external noise. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current. Resistors R12 and R13 are used for backup protection in case of short-circuit at output.

5 PCB Layout

PCB copper thickness is 2.0 oz.

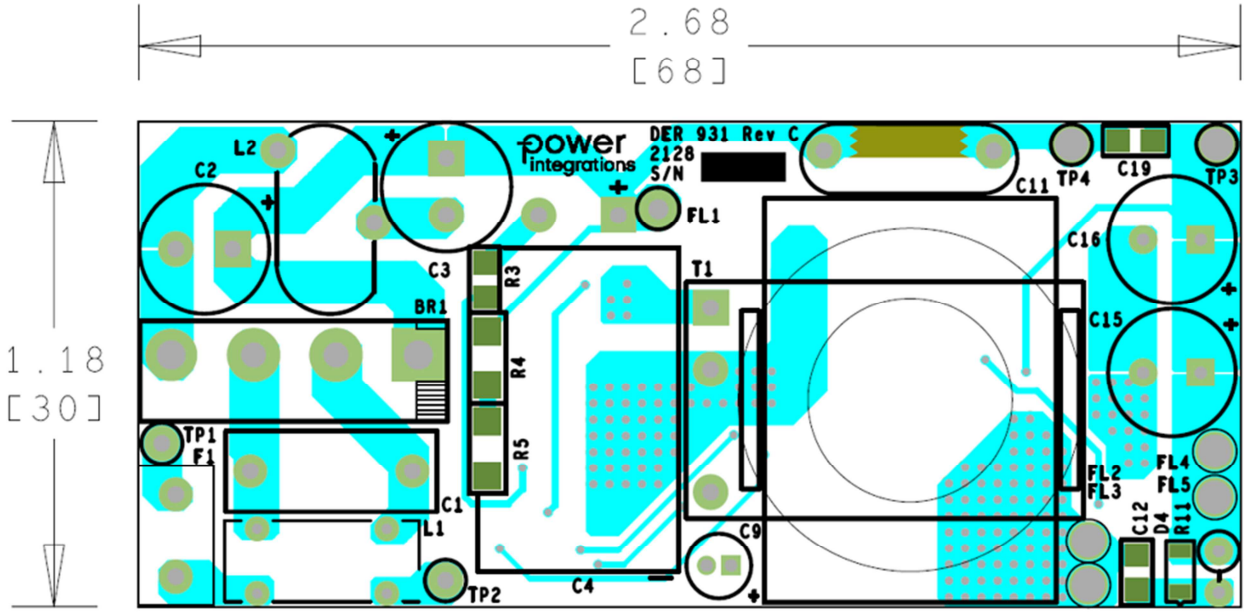


Figure 4 – Printed Circuit Layout, Top.

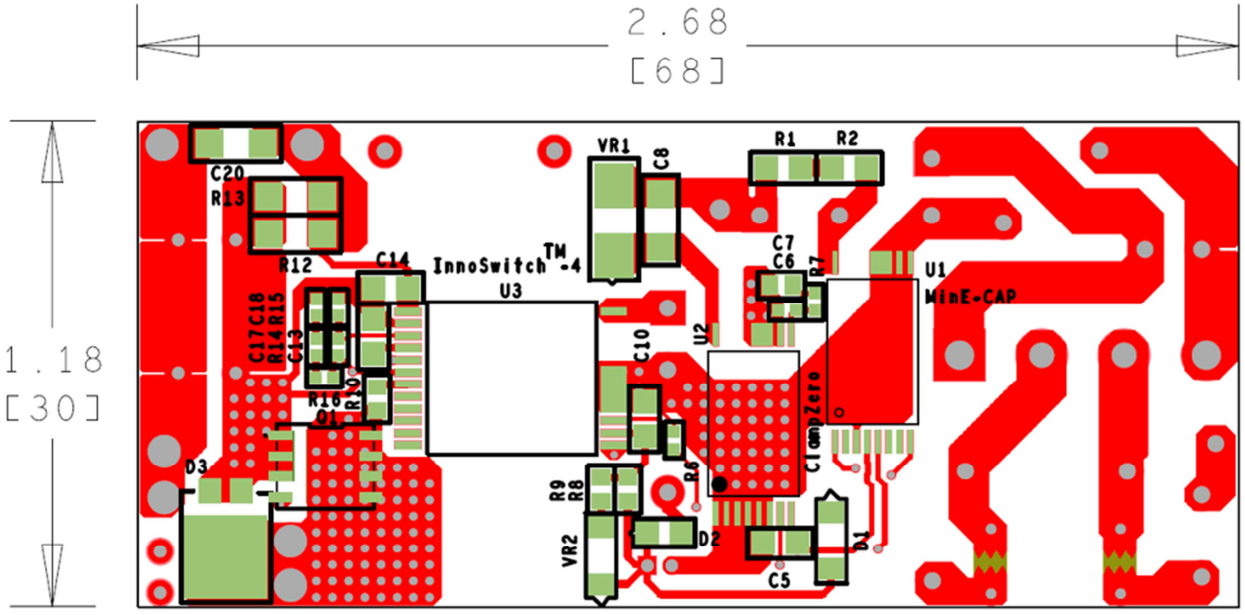


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 4 A, Bridge Rectifier, KBL	KBL06-E4/51	Vishay
2	1	C1	0.1 µF, 20%, 275 VAC, 560 VDC, X2, -40°C ~ 110 °C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	2	C2 C3	15 µF, 400 V, 20%, Electrolytic, (8 x 16), 3.5 mm lead spacing, Radial, Can, 2000 Hrs @ 105 °C	ERK2GM150F16OTO	AiSHi
4	1	C4	Electrolytic, 100 µF, 20%,160 V, Aluminum, Radial, Can 12000 Hrs @ 105°C	UCY2C101MHD1TO	Nichicon
5	1	C5	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
6	1	C6	0.1 µF, ±10%, 50 V, Ceramic, X7R, Soft Termination, 0402	C1005X7R1H104K050BE	TDK
7	1	C7	1 µF, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
8	1	C8	0.1 µF, 250 V, ±10%, Ceramic, X7R, 1206	C3216X7R2E104K160AA	TDK
9	1	C9	10 µF, 20%, 50 V, Aluminum, Radial, Can 5000 Hrs @ 105 °C (5 x 12.5 mm)	UPV1H100MFD	Nichicon
10	1	C10	470 nF, ±10%,50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung
11	1	C11	1 nF, Ceramic, Y1	440LD10-R	Vishay
12	1	C12	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
13	1	C13	2.2 µF, 25 V, Ceramic, X7R, 0805	CL21B225KAFNNWE	Samsung
14	1	C14	1 µF, ±10%, 25 V, Ceramic, X7R, 0805	08053C105K4T2A	AVX
15	2	C15 C16	820 µF, ±20%, 16 V, Al Organic Polymer, Gen. Purpose, 20000 Hrs @ 105 °C, -55 °C ~ 105 °C, 0.315" Dia (8.00 mm), 0.689"H (17.50 mm), 0.138" LS (3.50 mm)	APSG160ELL821MH16S	United Chemi-con
16	2	C17 C18	330 pF 16 V, Ceramic, X7R, 0402	C0402C331K4RACTU	Kemet
17	1	C19	1 µF, ±10%, 25 V, Ceramic, X7R, 0805	GCM21BR71E105KA56L	Murata
18	1	C20	47 µF, 16 V, X5R, 1206	3216X5R1C476M	TDK
19	1	D1	800 V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
20	1	D2	250 V, 200 mW, Diode, SOD323	BAV21WS-7-F	ON Semi
21	1	D3	100 V, 12 A, Schottky, SMD, TO-277A	V12P10-M3/86A	Vishay
22	1	D4	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
23	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
24	1	FL1	Flying Lead, Hole size 50 mils	N/A	N/A
25	4	FL2-FL5	Flying Lead, Hole size 70 mils	N/A	N/A
26	1	L1	460 µH, Toroidal Common Mode Choke, custom, DER-931, wound on 32-00315-00 core	32-00416-00	Power Integrations
27	1	L2	68 µH, Unshielded Toroidal Inductor, 2 A, 55 mΩ Max, Radial, Vertical (Open)	7447033	Wurth
28	1	Q1	MOSFET, N-Channel, 60 V, 142 W (Ta), 70 W (Tc), SMT, 8-DFN-EP (5x6)	AONS62614T	Alpha & Omega Semi
29	2	R1 R2	RES, 2 MΩ, 5%, 1/8 W, Thick Film, 0805	KTR10EZPJ205	Rohm
30	1	R3	RES, 1.0 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ105V	Panasonic
31	2	R4 R5	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
32	1	R6	RES, 30.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3002X	Panasonic
33	1	R7	RES, 6.04 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF6041X	Panasonic
34	1	R8	RES, 3 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3001V	Panasonic
35	1	R9	RES, 56 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ560V	Panasonic
36	1	R10	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
37	1	R11	RES, 5.6 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-5R6	Yageo
38	2	R12 R13	0.011 Ω, ±1%, ±75ppm/°C, 1 W, 1206, Automotive AEC-Q200, Current Sense, -55 °C ~ 155 °C	ERJ-8CWFR011V	Panasonic
39	1	R14	RES, 100.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1003X	Panasonic
40	1	R15	RES, 11.8 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1182X	Panasonic

41	1	R16	RES, 10 kΩ, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
42	1	SG1	Spark Gap 6.5 mm 2 pin		
43	1	T1	Bobbin, EQ25, 4 pins, 4pri, 0sec	TBI-235-01091.1206	TBI Transformer Bobbin Industrial Co, tbi-tw.com
44	1	TP1	Test Point, WHT, Miniature TH MOUNT	5002	Keystone
45	2	TP2 TP4	Test Point, BLK, Miniature TH MOUNT	5001	Keystone
46	1	TP3	Test Point, RED, Miniature TH MOUNT	5000	Keystone
47	1	U1	MinE-CAP	MIN1072M	Power Integrations
48	1	U2	Clampzero, MinSOP-16	CPZ1075M	Power Integrations
49	1	U3	InnoSwitch4-CZ, insop-24D	INN4074C-H185	Power Integrations
50	1	VR1	TVS Diode, 275 V Clamp, 1.4 A Ipp, Tvs Diode, SMT, SMA SMAJ (DO-214AC)	SMAJ170A-13-F	Diodes, Inc.
51	1	VR2	Diode Zener 18 V 500 mW SOD123	MMSZ5248B-7-F	Diodes, Inc.

7 Transformer Design Spreadsheet

1	ACDC_InnoSwitch4-CZ_Flyback_052621; Rev.1.0; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4 CZ Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	90		90	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	130.0		130.0	uF	Input capacitor
9	VOUT	12.00		12.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	6.000		6.000	A	Output current
12	POUT			72.00	W	Output power
13	EFFICIENCY	0.93		0.93		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z	0.50		0.50		Z-factor estimate
15	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	AUTO		INN4074		Generic device code
22	DEVICE_CODE			INN4074C		Actual device code
23	POUT_MAX			75	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.62	Ω	Primary switch on time drain resistance at 100 degC
25	ILIMIT_MIN			1.953	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			2.100	A	Typical current limit of the primary switch
27	ILIMIT_MAX			2.247	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.50	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			573.4	V	Peak drain voltage on the primary switch during turn-off
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	102000		102000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
36	VOR	130.0		130.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			93.22	V	Valley of the minimum input AC voltage at full load
38	KP			0.58		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.584		Primary switch duty cycle
41	TIME_ON			10.47	us	Primary switch on-time
42	TIME_OFF			3.58	us	Primary switch off-time
43	LPRIMARY_MIN			459.9	uH	Minimum primary inductance
44	LPRIMARY_TYP			484.1	uH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance

46	LPRIMARY_MAX			508.3	uH	Maximum primary inductance
48	**PRIMARY CURRENT**					
49	IPEAK_PRIMARY			2.173	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.818	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.806	A	Primary switch average current
52	IRIPPLE_PRIMARY			1.585	A	Primary switch ripple current
53	IRMS_PRIMARY			1.111	A	Primary switch RMS current
55	**SECONDARY CURRENT**					
56	IPEAK_SECONDARY			23.904	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			8.997	A	Secondary winding current pedestal
58	IRMS_SECONDARY			10.322	A	Secondary winding RMS current
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	**CORE SELECTION**					
64	CORE	EQ25		EQ25		Core selection
65	CORE CODE			EQ25-3C95		Core code
66	AE	94.20		94.20	mm^2	Core cross sectional area
67	LE			41.40	mm	Core magnetic path length
68	AL			5710	nH/turns^2	Ungapped core effective inductance
69	VE			4145.0	mm^3	Core volume
70	BOBBIN			TBI-235-01091.1206		Bobbin
71	AW			34.83	mm^2	Window area of the bobbin
72	BW			8.10	mm	Bobbin width
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			33		Primary turns
77	BPEAK			3761	Gauss	Peak flux density
78	BMAX			3518	Gauss	Maximum flux density
79	BAC			1261	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			445	nH/turns^2	Typical gapped core effective inductance
81	LG			0.246	mm	Core gap length
83	**PRIMARY BIAS WINDING**					
84	NBIAS_PRIMARY			3		Primary bias winding number of turns
86	**SECONDARY WINDING**					
87	NSECONDARY	3		3		Secondary winding number of turns
89	**SECONDARY BIAS WINDING**					
90	NBIAS_SECONDARY			2		Secondary bias winding number of turns
94	**PRIMARY COMPONENTS SELECTION**					
95	**ClampZero**					
96	LLEAK			4.84	uH	Primary winding leakage inductance
97	CCLAMP			100.0	nF	Primary clamp capacitor
98	RD_CLAMPZERO	AUTO		60	kΩ	HSD resistor
99	TLLDL/THLDL			100.0	ns	HSD resistor programmed delay
100	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			45.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
101	TIME_VDS_VALLEY			45.3	ns	Time taken by the VDS ring to reach its first valley
102	IPEAK_CLAMPZERO			2.128	A	Active clamp peak current
104	**LINE UNDERVOLTAGE**					
105	BROWN-IN REQURED			72.0	V	Required AC RMS line voltage brown-in threshold
106	RLS			3.64	MΩ	Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV

						threshold
107	BROWN-IN ACTUAL			73.0	V	Actual AC RMS brown-in threshold
108	BROWN-OUT ACTUAL			66.0	V	Actual AC RMS brown-out threshold
110	**LINE OVERVOLTAGE**					
111	OVERVOLTAGE_LINE			304.2	V	Actual AC RMS line over-voltage threshold
113	**BIAS DIODE**					
114	VBIAS_PRIMARY	10.0		10.0	V	Rectified primary bias voltage
115	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
116	VREVERSE_BIASDIODE_PRIMARY			43.94	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
117	CBIAS_PRIMARY			22	uF	Bias winding rectification capacitor
118	CBPP			0.47	uF	BPP pin capacitor
122	**SECONDARY COMPONENTS**					
123	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
124	RFB_LOWER			11.80	kΩ	Lower feedback resistor
125	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
127	**SECONDARY BIAS DIODE**					
128	VBIAS_SECONDARY			6.0	V	Rectified secondary bias voltage
129	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
130	VREVERSE_BIASDIODE_SECONDARY			28.63	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
131	CBIAS_SECONDARY			10	uF	Bias winding rectification capacitor
132	CBPS			2.20	uF	BPP pin capacitor
135	**MULTIPLE OUTPUT PARAMETERS**					
136	**OUTPUT 1z**					
137	VOUT1			12.00	V	Output 1 voltage
138	IOUT1			6.00	A	Output 1 current
139	POUT1			72.00	W	Output 1 power
140	IRMS_SECONDARY1			10.322	A	Root mean squared value of the secondary current for output 1
141	IRIPPLE_CAP_OUTPUT1			8.399	A	Current ripple on the secondary waveform for output 1
142	NSECONDARY1			3		Number of turns for output 1
143	VREVERSE_RECTIFIER1			45.94	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
144	SRFET1	Auto		AON6244		Secondary rectifier (Logic MOSFET) for output 1
145	VF_SRFET1			0.037	V	SRFET on-time drain voltage for output 1
146	VBREAKDOWN_SRFET1			60	V	SRFET breakdown voltage for output 1
147	RDSON_SRFET1			6.2	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1

8 Transformer Specification

8.1 *Electrical Diagram*

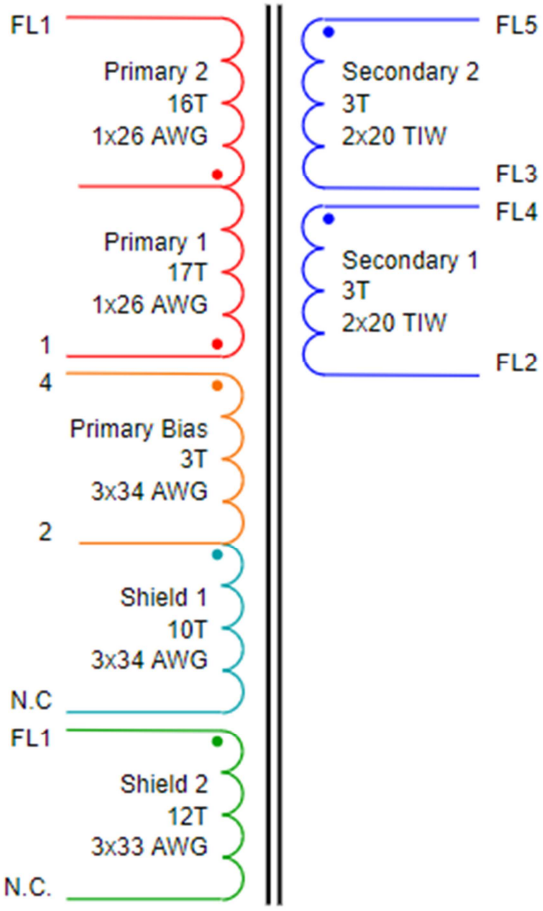


Figure 6 – Electrical Diagram.

8.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and FL1, with all other windings open.	484 µH± 5%
Resonant Frequency	Between pin 1 and FL1, other windings open	1,000 kHz (Min.)
Primary Leakage Inductance	Between pin 1 and FL1, with pins: FL8-FL10 shorted	6 µH (Max.)

8.3 *Material List*

Item	Description
[1]	Core: EQ25, Ferroxcube: 3C95.
[2]	Bobbin: EQ25-Vert-4pins (4/0).
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #33 AWG, Double Coated.
[6]	Magnet Wire: #20 AWG, Triple Insulated Wire.
[7]	Copper Tape: 2 mils Thickness, Soft.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 3 mm Width.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 5 mm Width.
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 8.5 mm Width.
[11]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 9.5 mm Width.
[12]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 16.4 mm Width.
[13]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 18.2 mm Width.
[14]	Varnish: Dolph BC-359.

8.4 *Transformer Build Diagram*

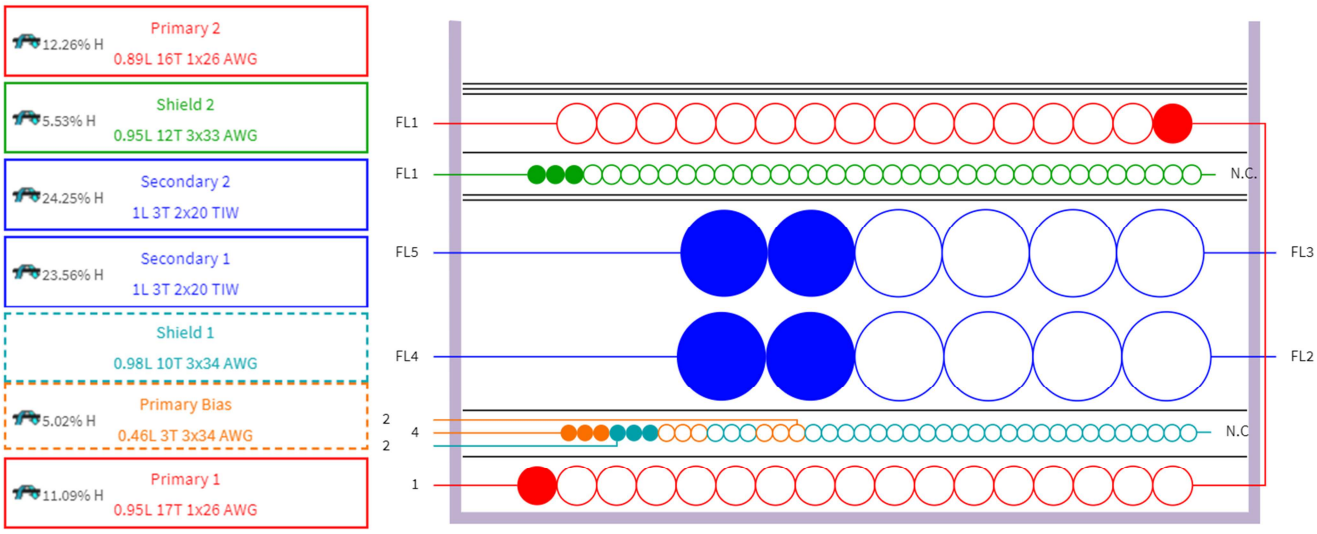
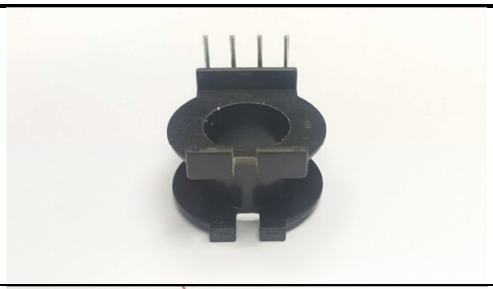
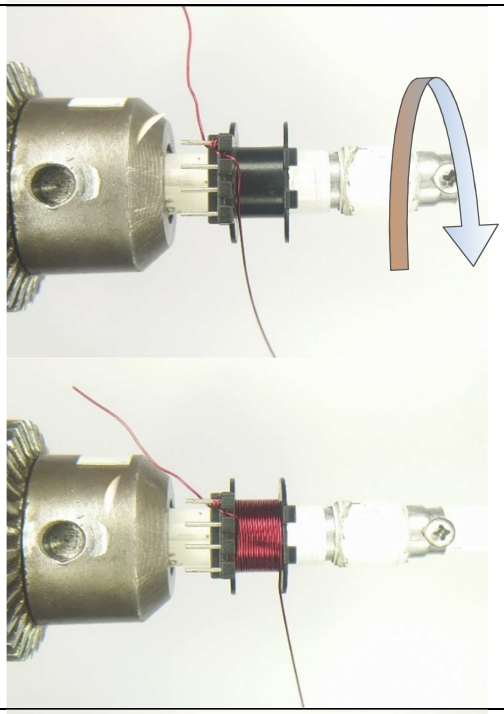
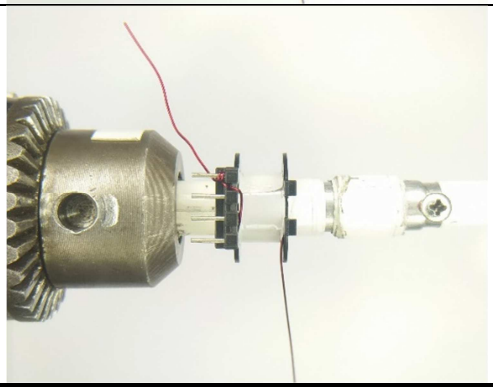
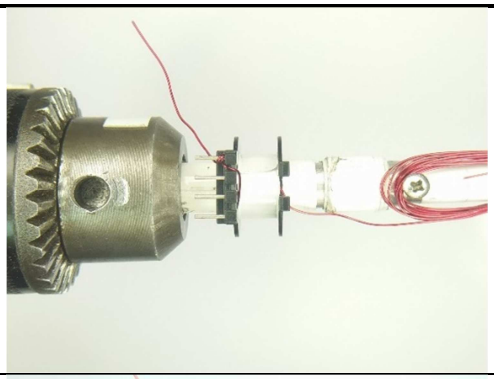
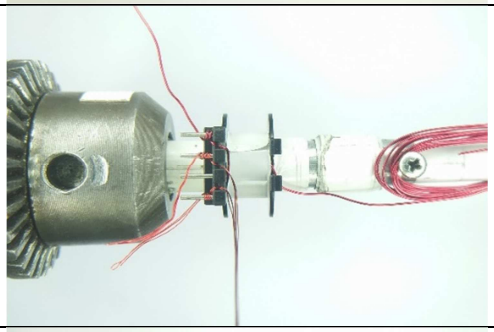
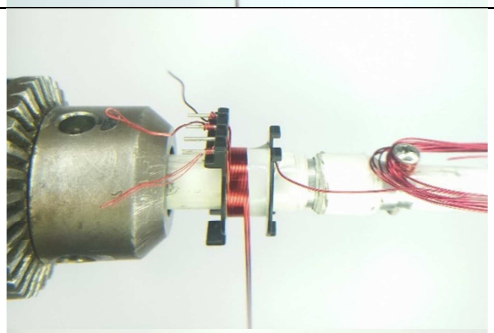
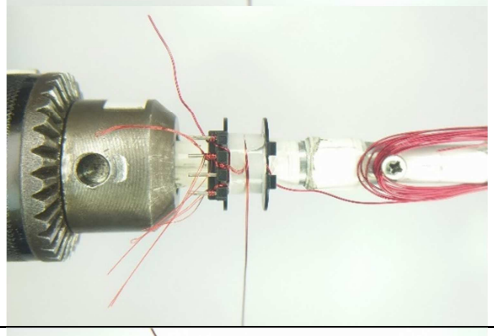
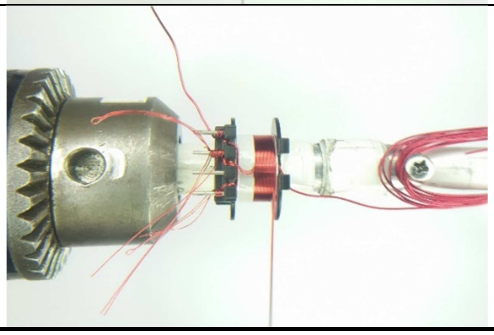
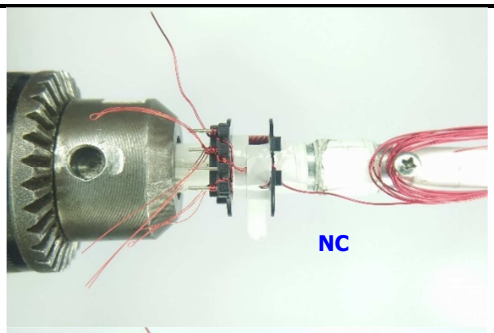
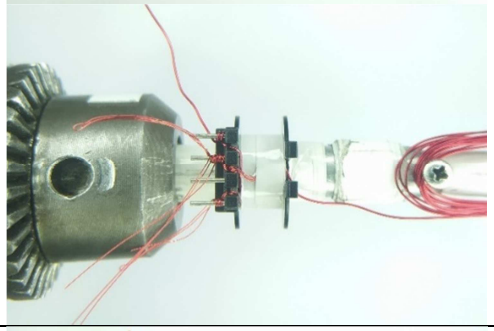
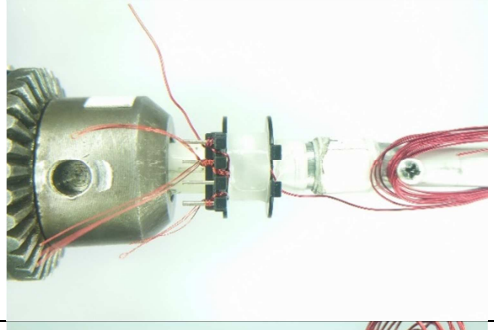
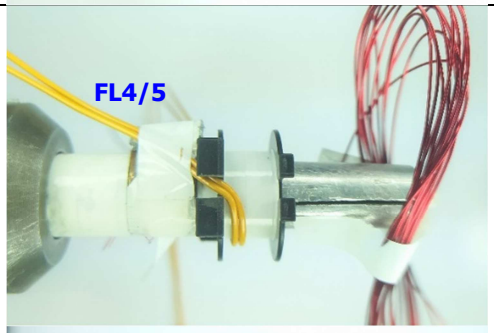
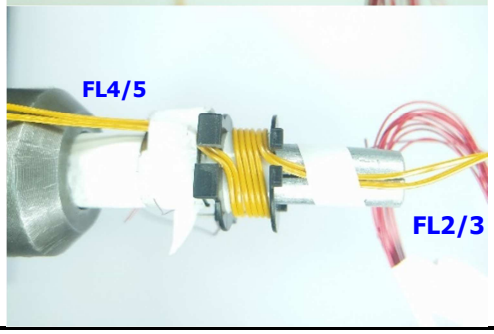


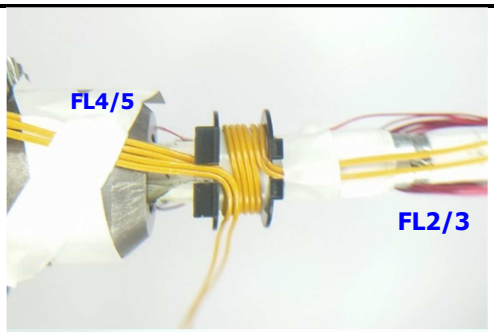
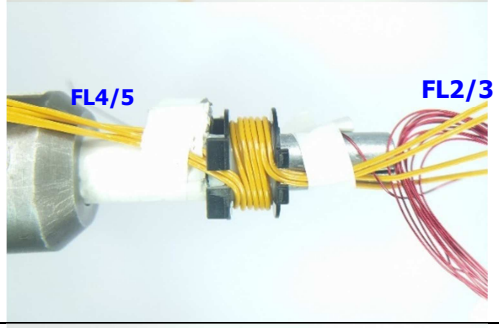
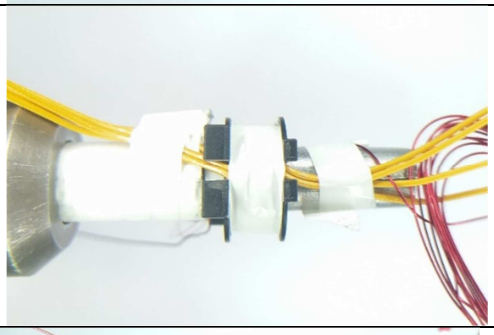
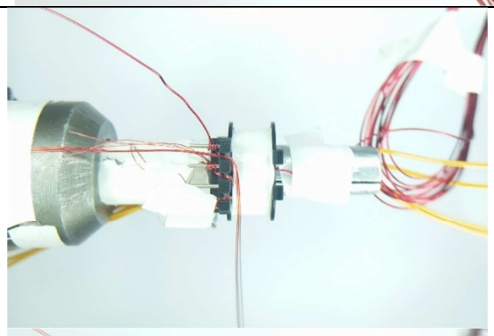
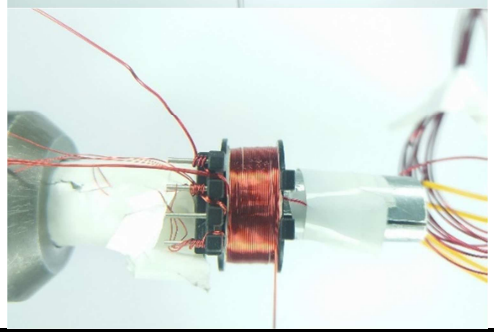
Figure 7 – Transformer Construction Diagram.

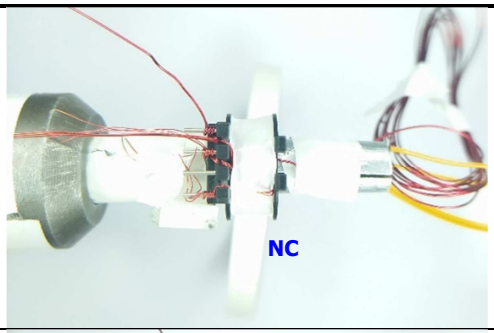
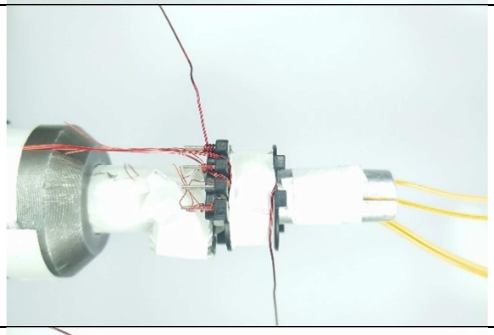
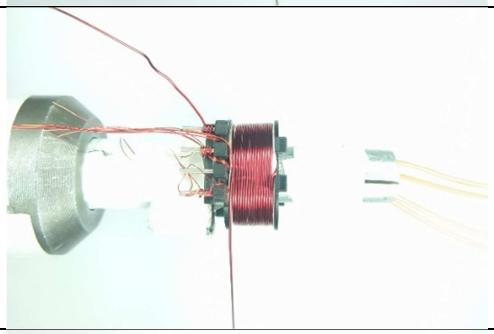
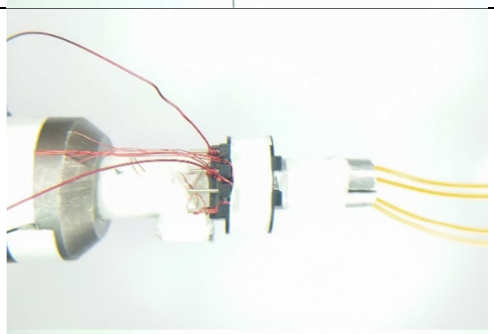
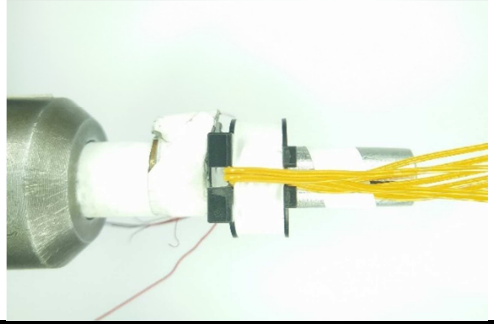
8.5 *Winding Illustrations*

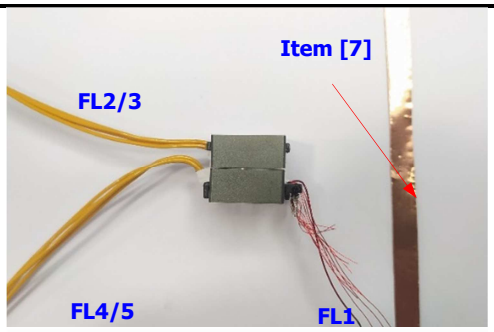
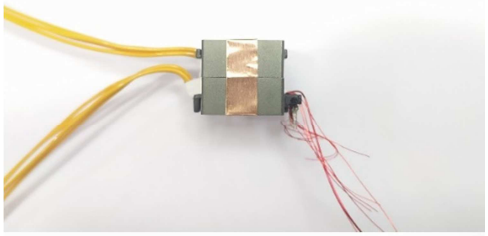
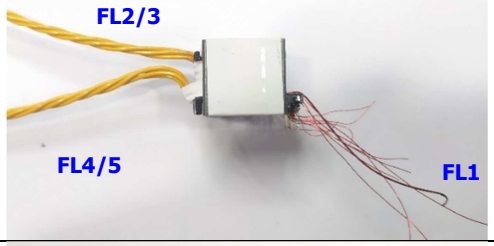
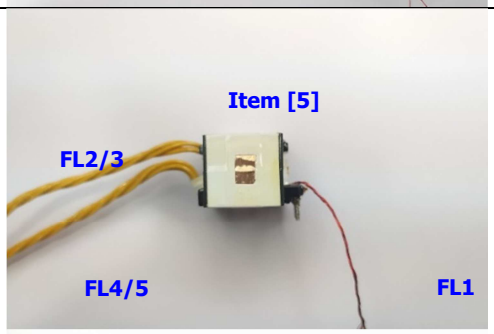
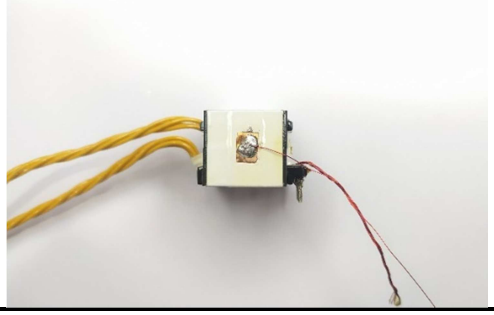
Winding Preparation		Start by creating a 3 mm wide slot on the flange on the secondary-side of the bobbin Item [2]. Place the bobbin on the mandrel with pin side of the bobbin on the left side. Winding direction is clock-wise.
1st Primary		Start at pin 1, wind Primary 1 17 turns of wire Item [3] in 1 layer, from left to right.
Insulation		Apply 1 layer of tape Item [10]. At the last turn of Primary 1, exit the wire out of the bobbin. Leave enough length (1 meter) of this wire for Primary 2.

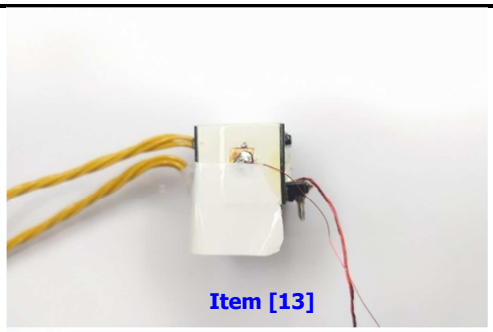
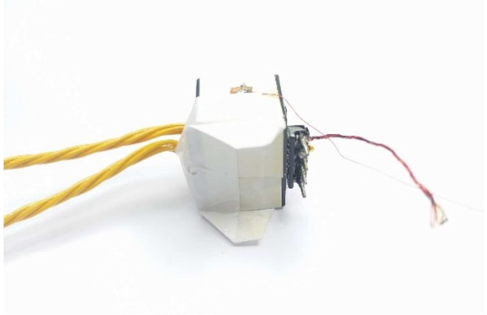
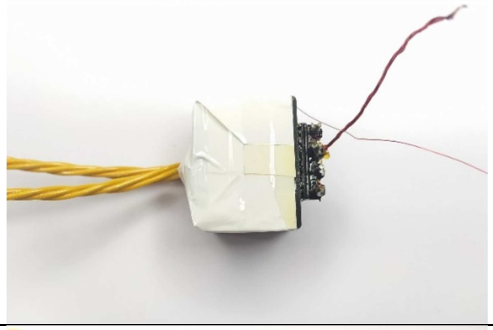
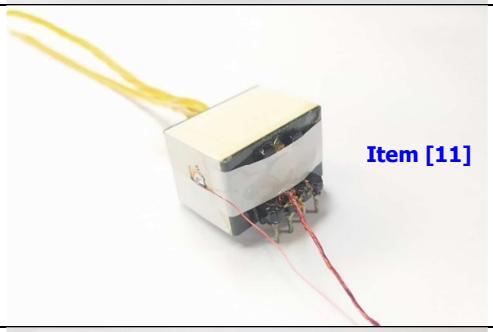
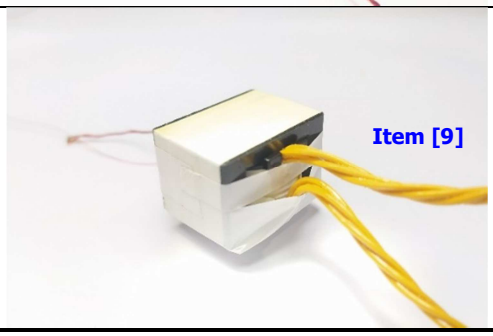
		
Primary Bias & Shield 1		Use 3 strands of wire Item [4], starting at pin 4 for Primary Bias and 3 strands of wire Item [4], starting at pin 2 for Shield 1. Wind all 6 wires in parallel.
Primary Bias Termination	 	At 3rd turn, put 1 layer of tape Item [8] over the windings. Next, bring the wires for Primary Bias back to the left to terminate at pin 2.
Shield Winding 1 Termination		Continue winding 7 more turns of Shield-1 to complete 10 turns. At the end of the turns, secure the winding with tape Item [9]. Cut short the wires for Shield 1 and leave ~2 mm as No-Connect (NC). Finish the 1 layer of tape to cover the remainder of the layer.

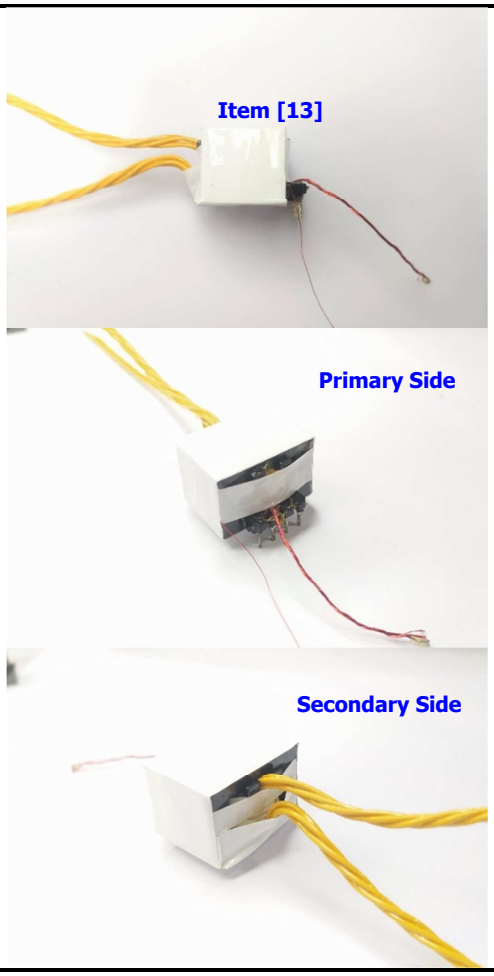
	 	
Insulation		Apply 1 layer of tape Item [10].
WD4 Secondary	 	Start at the slot on the left on secondary side of the bobbin, Wind Secondary 1 using 2 strands of wire Item [6], leave ~50mm floating, and mark as FL4/5, wind 3 turns in 1 layer. At the last turn, exit the wire at the slot on the right also leave ~ 50mm floating and mark as FL2/3 for 1st half of Secondary. Repeat another winding for Secondary 2 as above for 2nd half of Secondary which is parallel with 1st half Secondary.

	 	
Insulation		Apply 2 layers of tape Item [11]. (*It is important to apply the tapes so that the layer next to it will be as flat as possible)*
WD6 **Shield2**	 	Starting at pin 3, wind Shield-2 using 12 tri-filar turns of wire Item [5]. At the last turn, secure the winding with tape Item [10]. Cut short the wires and leave ~2 mm as No-Connect. (*It is important that the shield winding is as flat as possible so that there will be no gaps in between the windings)*

		
Insulation		Complete the 1 layer of tape Item [10] to cover Shield 2.
WD7 **2nd Primary**		Using wire remaining from Primary 1, wind 16 turns of Primary 2, right to left. At the last turn, bring the wire the wire out, leave ~50 mm floating and label FL1.
Insulation	 	Apply 2 layers of tape Item [10]. Fold the wire FL4/5 so that its termination is now on the right side of the bobbin. Put 3 layers of tape Item [8] on the left side of the bobbin to support the folded wire.

Finish	  	Gap cores to achieve the inductance target specified in the Electrical Specifications table. Cut out ~7 mm wide copper tape item [7] and wrap 1 layer around the core. Secure with 2 layers of tape Item [12] around the core. Twist FL2/3 and FL4/5. (*Be careful not to scratch the TIW insulation with the transformer core.)* Varnish using Item [14].
Core grounding	 	Core Grounding: Slice a small hole and solder wire Item [5]. Label the termination FL1.

Core insulation 1	  	Place tape Item [13] on the secondary-side of the transformer and wrap up to cover the side and the bottom. Also, ensure that the tape covers the whole width of the core. Repeat the process to place another layer of tape Item [13] using the same method.
Core insulation 2		Place tape Item [11] on the primary side of the transformer to cover the windings
Core insulation 3		Place tape Item [9] on the secondary-side of the transformer to cover the area between FL2/3 and FL4/5

Core insulation 4		Wrap the transformer using 2 layers of tape Item [13]. Make sure that there are no openings in the bottom side of the transformer which can touch the board.

9 Common Mode Choke Specifications

9.1 *460 µH Common Mode Choke (L1)*

9.1.1 Electrical Diagram



Figure 8 – Inductor Electrical Diagram.

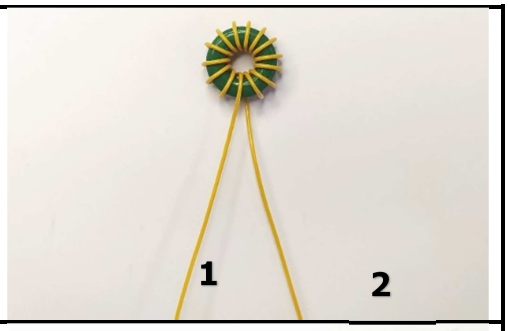
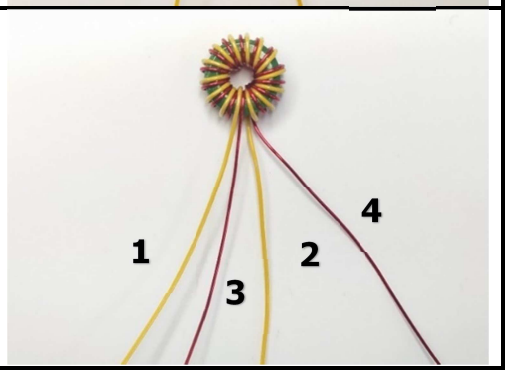
9.1.2 Electrical Specifications

Inductance	Pins 1 - 2 measured at 100 kHz, 0.4 A RMS.	460 µH ±20%
Primary Leakage Inductance	Pins 1 - 2, with 3 - 4 shorted.	< 1 µH

9.1.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTOR TOROID 12 mm O.D.; Mfg Part number: GL50 T 12X6X4-C Dim: 12mm O.D. x 4 mm I.D. x 6 mm Th.
[2]	Magnet Wire: #24 AWG.
[3]	Triple Insulated Wire #24 AWG.

9.1.4 Common Mode Choke Construction

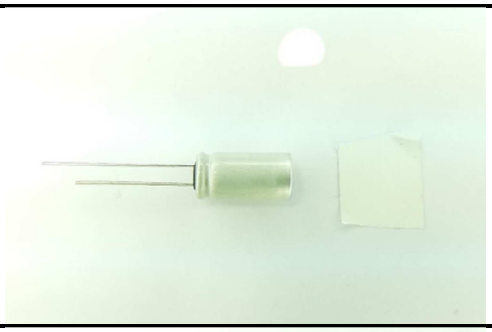
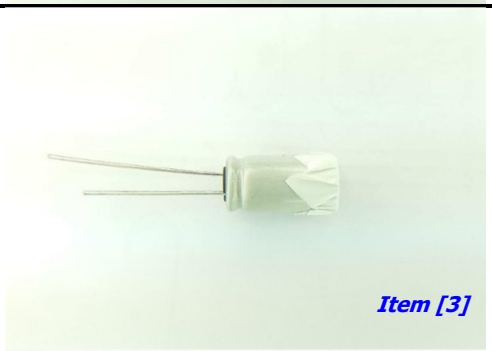
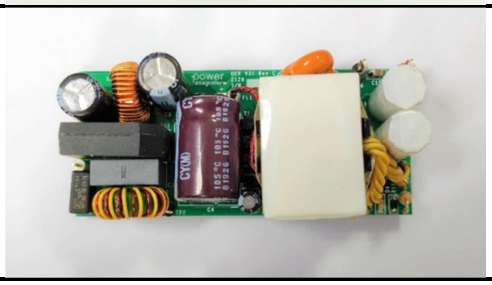
Mark the start end of the winding as 1 and wind 13 turns of Item [2] on Item [1]. Mark the end of this winding as 2. Leave ~50 mm floating.	
Repeat the same procedure as above for the other winding using Item [3], making sure that the start/end and the direction of winding is the same as the first winding. Leave ~50 mm floating. Mark the start of this winding as 3 and the end as 4.	

10 PCB Assembly Instructions

10.1 *Material List*

Item	Description
[1]	Capacitor C19 on DER-931 Schematic.
[2]	Capacitor C20 on DER-931 Schematic.
[3]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 16.4 mm Wide, 25 mm Long.

10.2 *Output Capacitor Assembly Instructions*

	
 	Cover the top of C19 and C20 with tape Item [3]. After which, wrap 2 layers of Item [3] around the capacitors to insulate the capacitor form transformer core.
	Finished assembly.

Note: Cut all the TH (PTH and NPTH) pins to <0.5 mm on the bottom side of the board after completing the assembly.

11 Performance Data

All the performance data have been taken on the board unless otherwise specifically mentioned.

11.1 *No-Load Input Power*

11.1.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Load	0%
Soak Time per Line	60 minutes
Integration time	10 minutes

11.1.2 Test Results

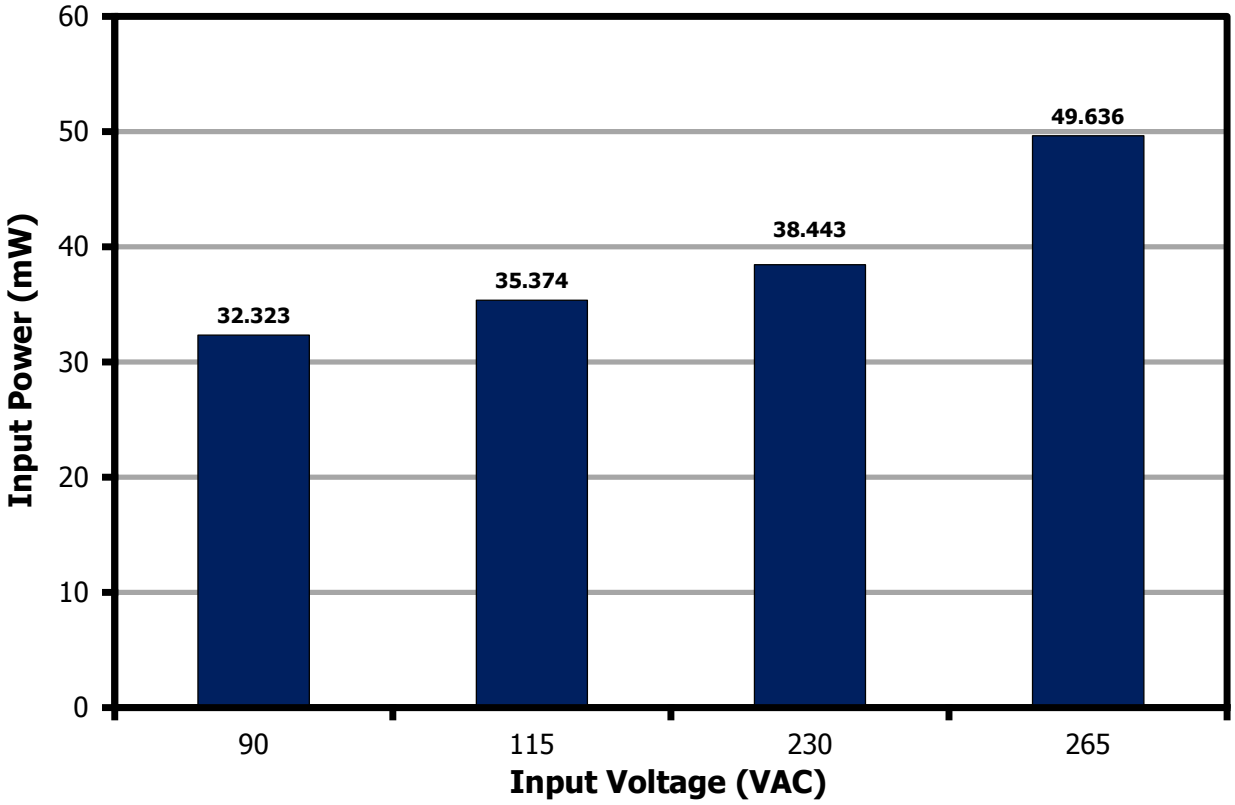


Figure 9 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

11.2 *Average Efficiency*

11.2.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Load	100%, 75%, 50%, 25%, 10%
Soak Time per Line	30 minutes
Delay Time per Load	5 minutes
Integration time	1 minute

11.2.2 DOE and CoC Requirements

		Test	Average	Average	10% Load
Output Voltage	**Model**	**Power [W]**	**DOE6 Limit**	**CoC v5 Tier 2**	**CoC v5 Tier 2**
12	>6 V	12	88.00%	89.00%	79.00%

11.2.3 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	**230 VAC**	**115 VAC**	**230 VAC**
12	72	92.69	94.00	91.32	91.85

11.2.4 Average and 10% Efficiency at 90 VAC Input

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	70.84	92.04	92.72
75	53.44	92.86	
50	35.83	93.01	
25	17.96	92.96	
10	7.17	91.49	

11.2.5 Average and 10% Efficiency at 115 VAC Input

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	71.02	92.53	92.69
75	53.57	92.70	
50	35.86	92.76	
25	17.96	92.77	
10	7.17	91.32	

11.2.6 Average and 10% Efficiency at 230 VAC Input

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	71.52	94.11	94.00
75	53.80	94.12	
50	35.93	94.07	
25	17.97	93.70	
10	7.17	91.85	

11.2.7 Average and 10% Efficiency at 265 VAC Input

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	71.62	94.05	93.87
75	53.84	94.04	
50	35.94	93.95	
25	17.97	93.45	
10	7.17	91.23	

11.2.8 DoE/CoC Comparison with Measured Data

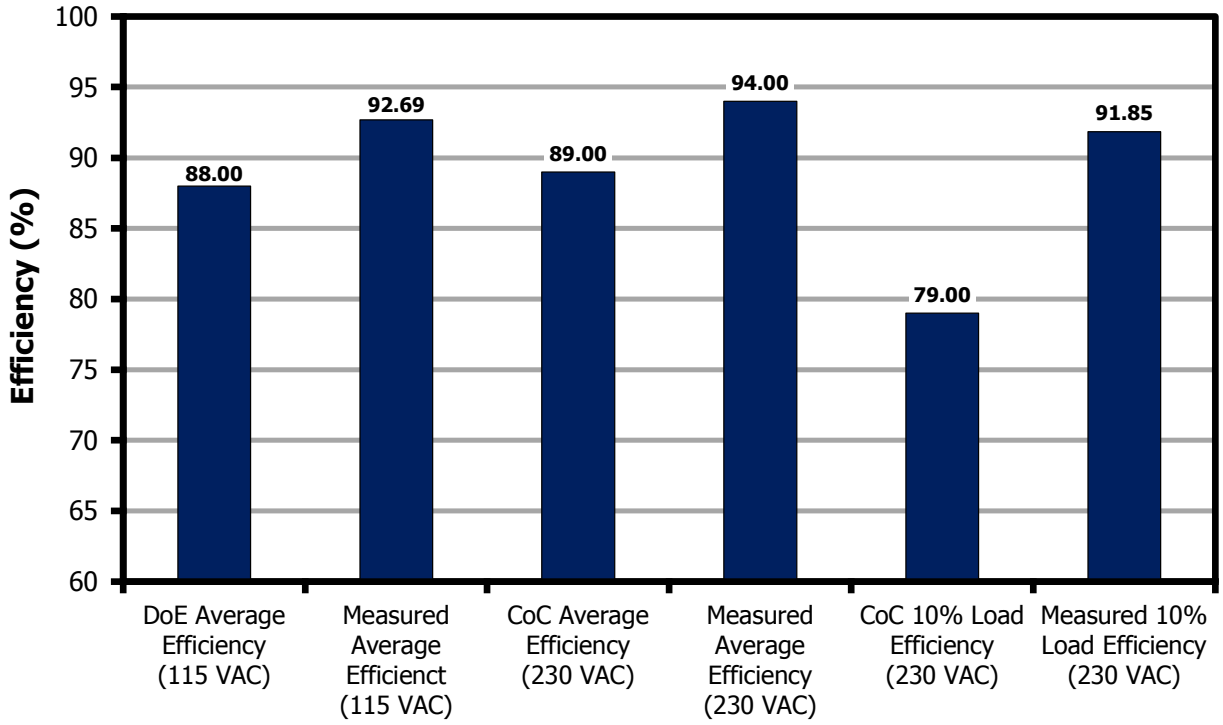


Figure 10 – DoE/CoC Data Comparison at 115 VAC and 230 VAC.

11.3 *Full-load Efficiency vs. Line*

11.3.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Load	100%
Soak Time per Line	30 minutes
Integration Time	1 minute

11.3.2 Test Results

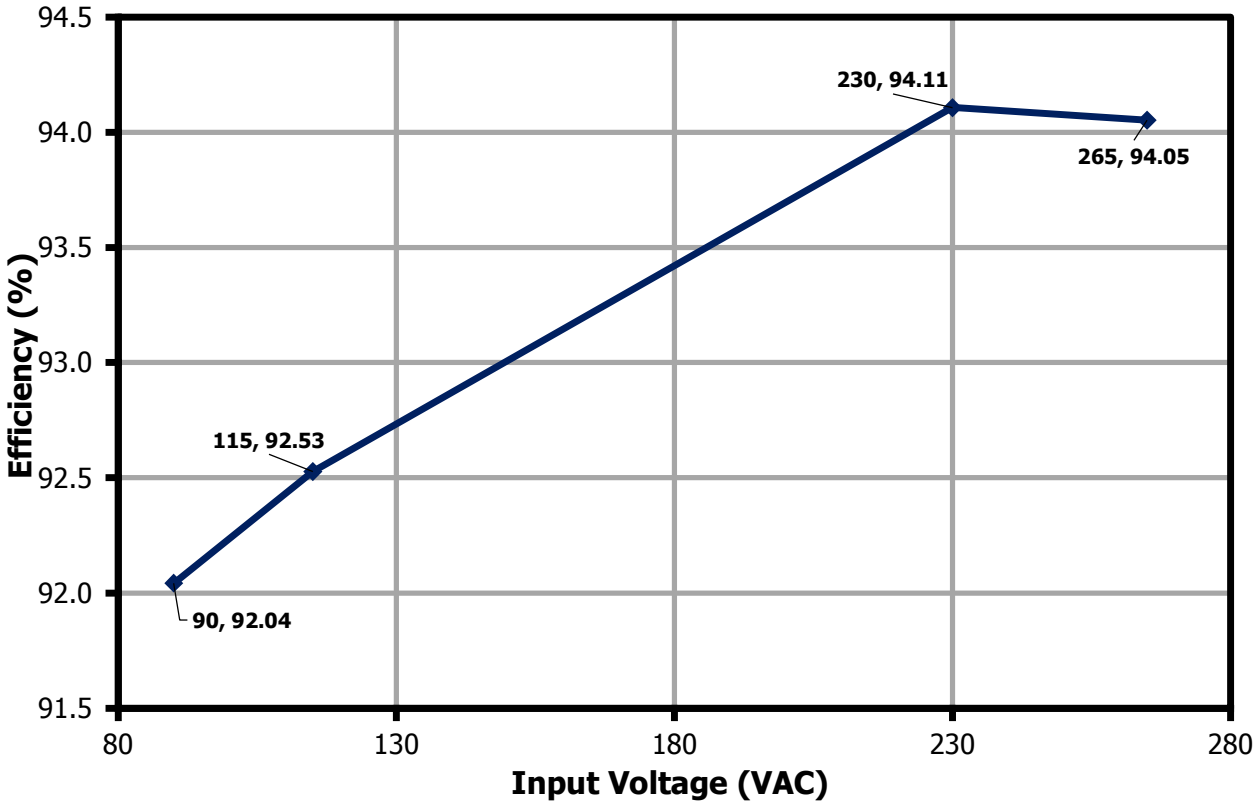


Figure 11 – Full-load Efficiency vs. Line, Room Ambient.

11.4 *Load Regulation (On Board)*

11.4.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Load	100%
Soak Time per Line	30 minutes
Delay Time per Load	5 minutes
Integration Time	1 minute

11.4.2 Test Results

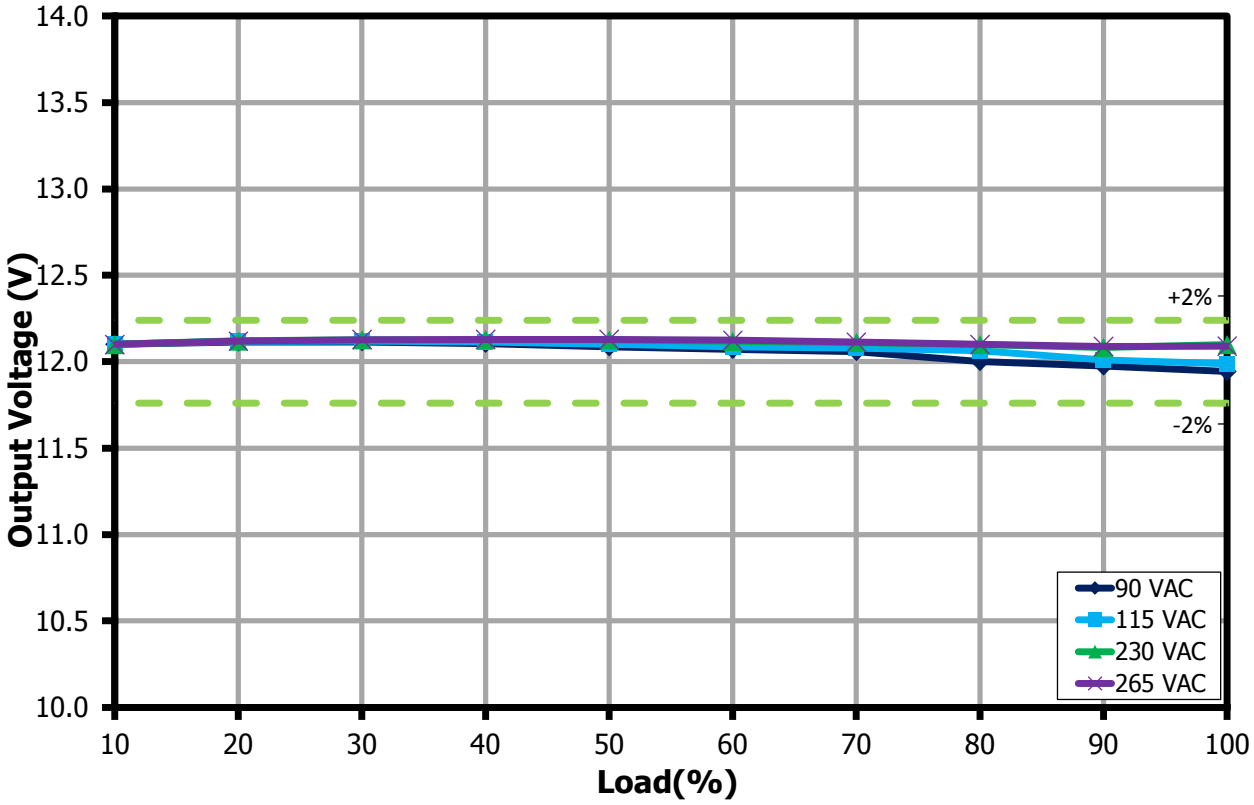


Figure 12 – Output Voltage vs. Output Load, Room Temperature.

11.5 *Line Regulation (On Board)*

11.5.1 Test Set-up

Parameter	Value
Input Voltage	90, 100, 115, 132, 150, 180, 200, 230, 265 VAC
Output Load	100%
Soak Time per Line	30 minutes
Integration Time	1 minute

11.5.2 Test Results

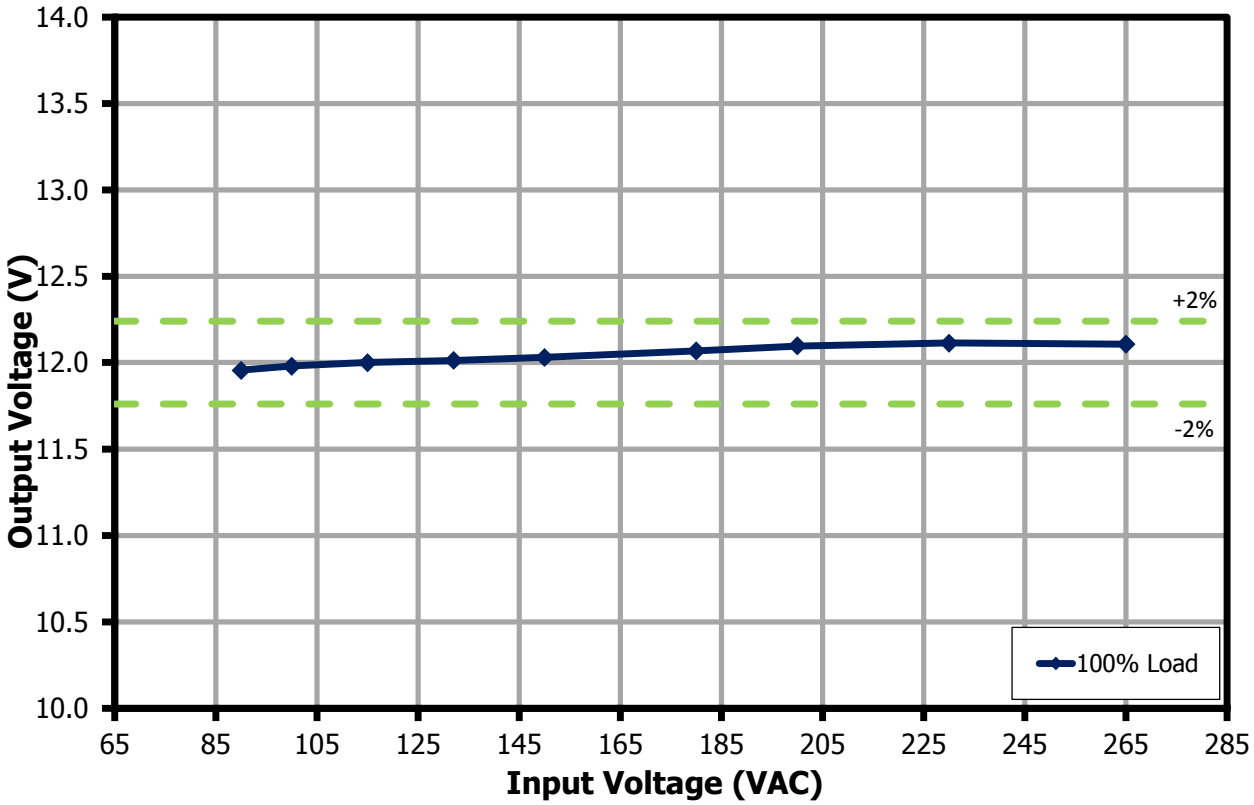


Figure 13 – Output Voltage vs. Input Line Voltage, Room Temperature.

12 Thermal Performance

12.1 *Test Set-up*

Parameter	Value
Input Voltage	90 VAC, 265 VAC
Output Load	100%
Soak Time per Line	60 minutes
Enclosure	Device is placed inside an acrylic box

12.2 *Thermal Images and Measurement*

12.2.1 90 VAC, 12 V / 6A

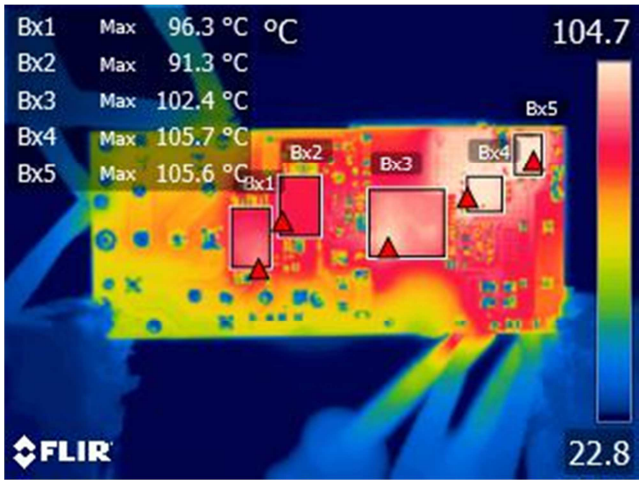


Figure 14 – Bottom Thermal Image, T_{AMB} = 22.8 ºC.
Bx1: MinE-CAP, U1 = 96.3 ºC.
Bx2: ClampZero, U2 = 91.3 ºC.
Bx3: InnoSwitch4-CZ, U3 = 102.4 ºC.
Bx4: SRFET, Q1 = 105.7 ºC.
Bx5: Schottky Diode, D3 = 105.6 ºC.

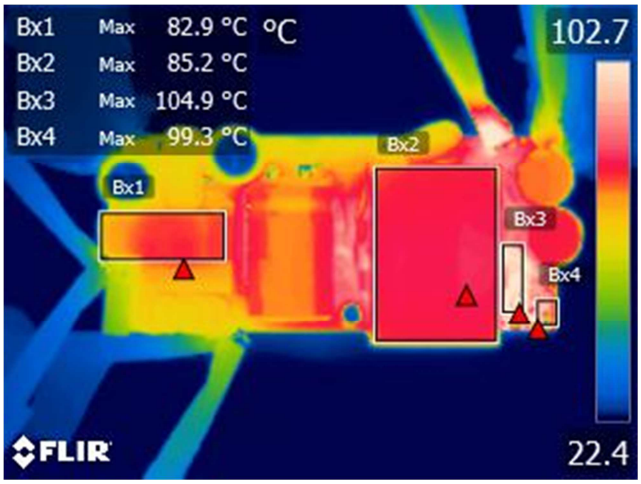


Figure 15 – Top Thermal Image, T_{AMB} = 22.4 ºC.
Bx1: Bridge, BR1 = 82.9 ºC.
Bx2: Transformer Core, T1 = 85.2 ºC.
Bx3: Secondary Winding, FL2/3 = 104.9 ºC.
Bx4: Snubber Resistor, R11 = 99.3 ºC.

12.2.2 265 VAC, 12 V / 6 A

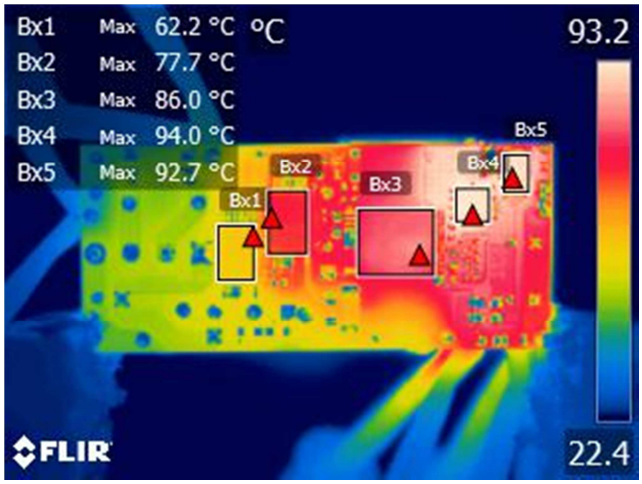


Figure 16 – Bottom Thermal Image, T_{AMB} = 22.4 ºC.
Bx1: MinE-CAP, U1 = 62.2 ºC.
Bx2: ClampZero, U2 = 77.7 ºC.
Bx3: InnoSwitch4-CZ, U3 = 86.0 ºC.
Bx4: SRFET, Q1 = 94.0 ºC.
Bx5: Schottky Diode, D3 = 92.7 ºC.

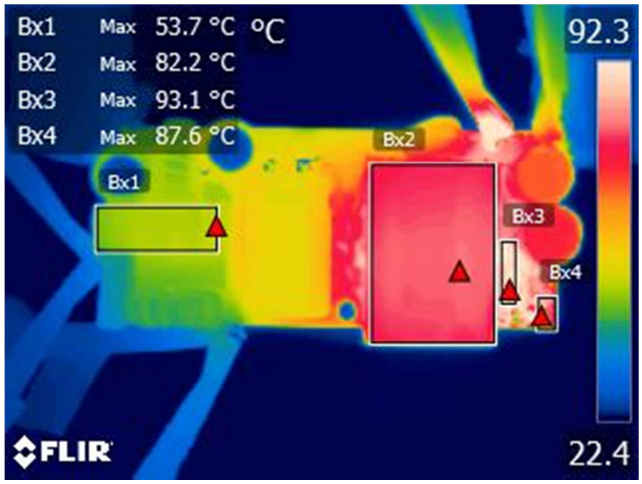


Figure 17 – Top Thermal Image, T_{AMB} = 22.4 ºC.
Bx1: Bridge, BR1 = 53.7 ºC.
Bx2: Transformer Core, T1 = 82.2 ºC.
Bx3: Secondary Winding, FL2/3 = 93.1 ºC.
Bx4: Snubber Resistor, R11 = 87.6 ºC.

12.3 *Thermal Data Summary*

Parameter	Temperature (°C) at 90 VAC	Temperature (°C) at 265 VAC
MinE-CAP (U1)	96.3	62.2
ClampZero (U2)	91.3	77.7
InnoSwitch4-CZ (U3)	102.4	86.0
SRFET (Q1)	105.7	94.0
Schottky Diode (D3)	105.6	92.7
Bridge (BR1)	82.9	53.7
Transformer Core (T1)	85.2	82.2
Secondary Winding (FL2/3)	104.9	93.1
Snubber Resistor (R11)	99.3	87.6
Ambient Temperature	22.4	22.4

13 Waveforms

13.1 *Output Voltage Start-up Waveforms*

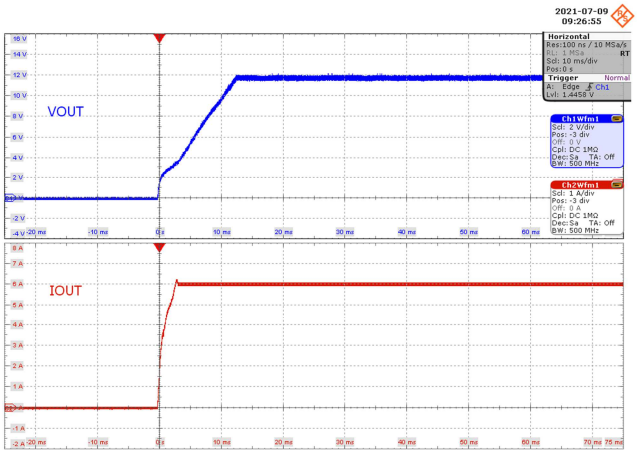


Figure 18 – Output Voltage Start-up.
90 VAC, 100% Load.
Ch1/Upper: V_{OUT}, 2 V / div.
Ch2/Lower: I_{OUT}, 1 A / div.
Timebase: 10 ms / div.

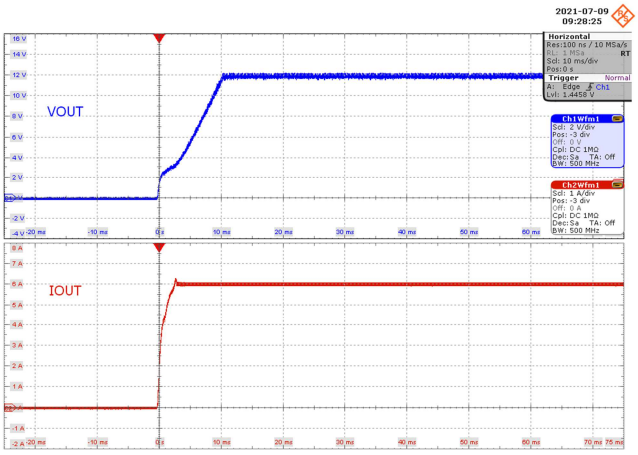


Figure 19 – Output Voltage Start-up.
265 VAC, 100% Load.
Ch1/Upper: V_{OUT}, 2 V / div.
Ch2/Lower: I_{OUT}, 1 A / div.
Timebase: 10 ms / div.

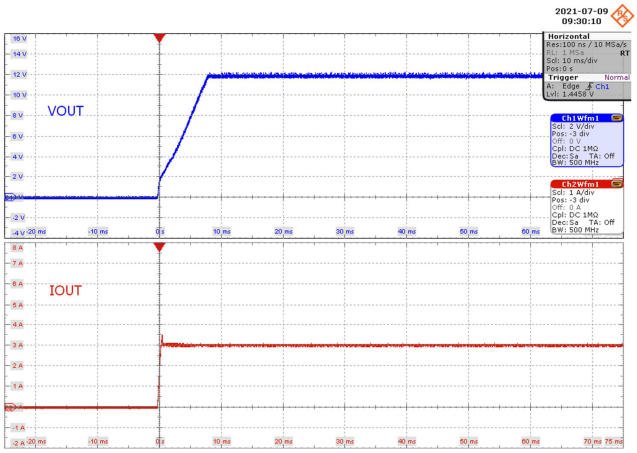


Figure 20 – Output Voltage Start-up.
90 VAC, 50% Load.
Ch1/Upper: V_{OUT}, 2 V / div.
Ch2/Lower: I_{OUT}, 1 A / div.
Timebase: 10 ms / div.

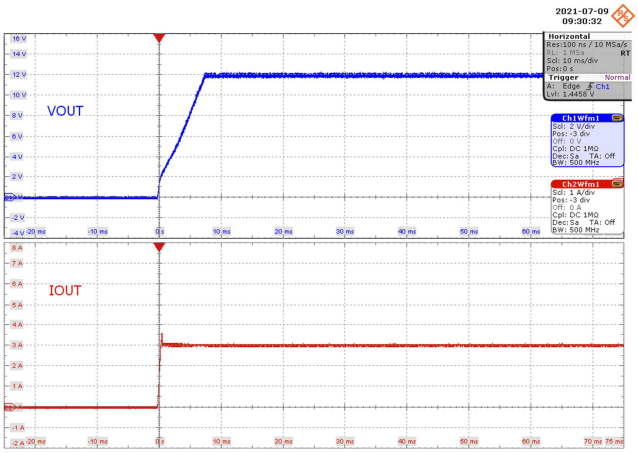


Figure 21 – Output Voltage Start-up.
265 VAC, 50% Load.
Ch1/Upper: V_{OUT}, 2 V / div.
Ch2/Lower: I_{OUT}, 1 A / div.
Timebase: 10 ms / div.

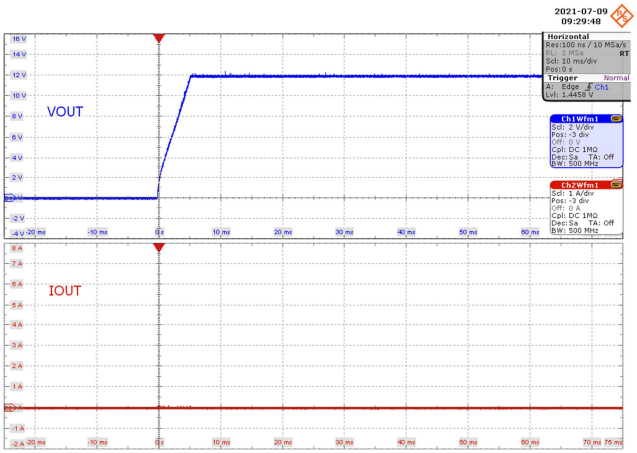


Figure 22 – Output Voltage Start-up.
90 VAC, 0% Load.
Ch1/Upper: V_{OUT}, 2 V / div.
Ch2/Lower: I_{OUT}, 1 A / div.
Timebase: 10 ms / div.

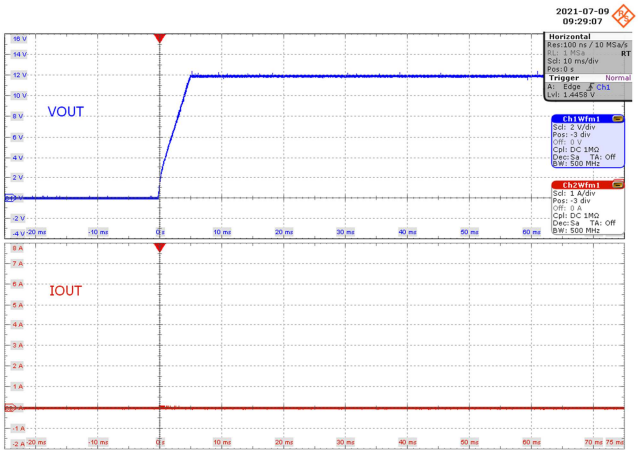


Figure 23 – Output Voltage Start-up.
265 VAC, 0% Load.
Ch1/Upper: V_{OUT}, 2 V / div.
Ch2/Lower: I_{OUT}, 1 A / div.
Timebase: 10 ms / div.

13.2 *Primary Drain Voltage and Current Start-up Waveforms*

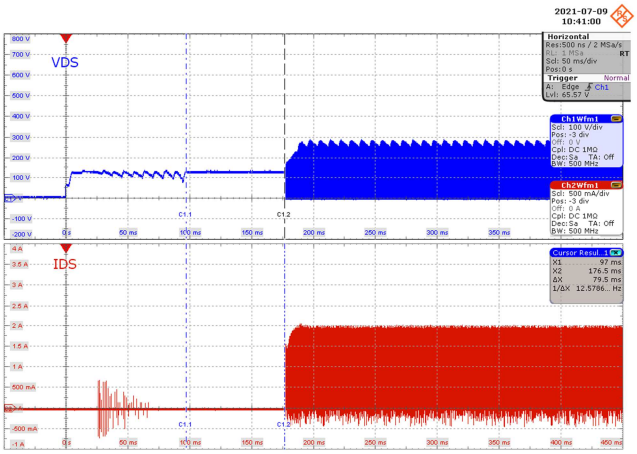


Figure 24 – Primary Drain Voltage and Current Start-up.
90 VAC, 100% Load.
Ch1/Upper: V_{DS}, 100 V / div.
Ch2/Lower: I_{DS}, 500 mA / div.
Timebase: 50 ms / div.

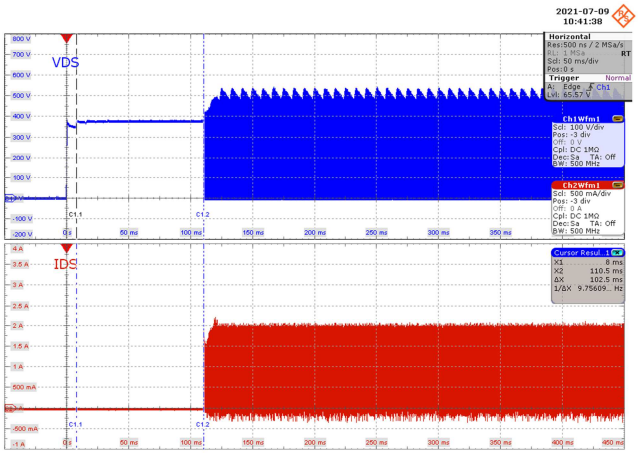


Figure 25 – Primary Drain Voltage and Current Start-up.
265 VAC, 100% Load.
Ch1/Upper: V_{DS}, 100 V / div.
Ch2/Lower: I_{DS}, 500 mA / div.
Timebase: 50 ms / div.

13.3 *Load Transient Response (On Board)*

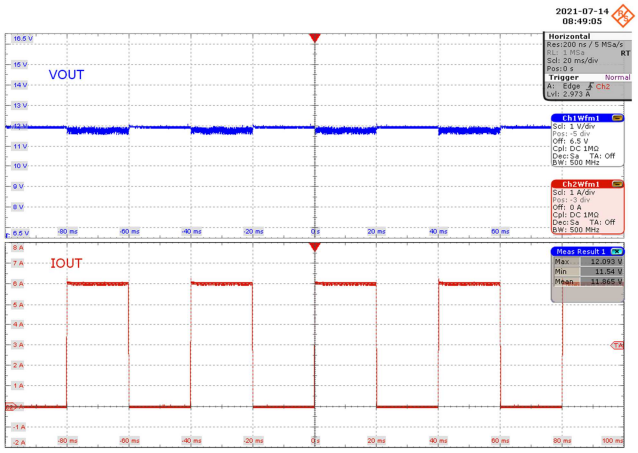


Figure 26 – Transient Response.
90 VAC, 0% – 100% Load Step.
V_{MIN}: 11.54 V, V_{MAX}: 12.093 V.
Ch1/Upper: V_{OUT}, 1 V / div.
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

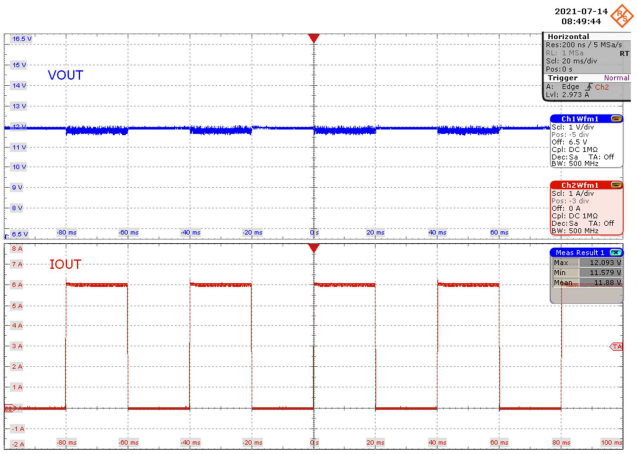


Figure 27 – Transient Response.
115 VAC, 0% – 100% Load Step.
V_{MIN}: 11.579 V, V_{MAX}: 12.093 V.
Ch1/Upper: V_{OUT}, 1 V / div.,
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

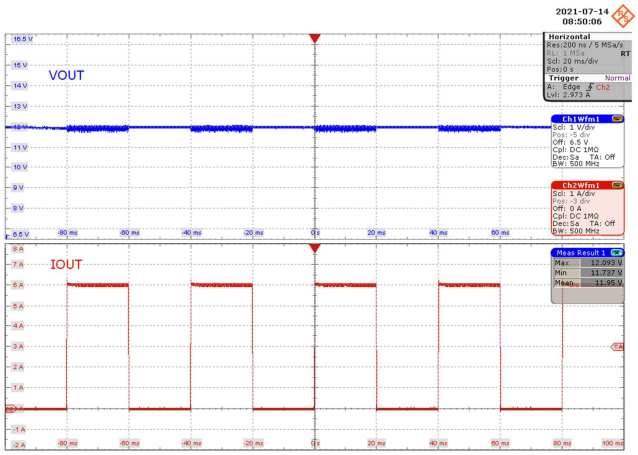


Figure 28– Transient Response.
230 VAC, 0% – 100% Load Step.
V_{MIN}: 11.737 V, V_{MAX}: 12.093 V.
Ch1/Upper: V_{OUT}, 1 V / div.
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

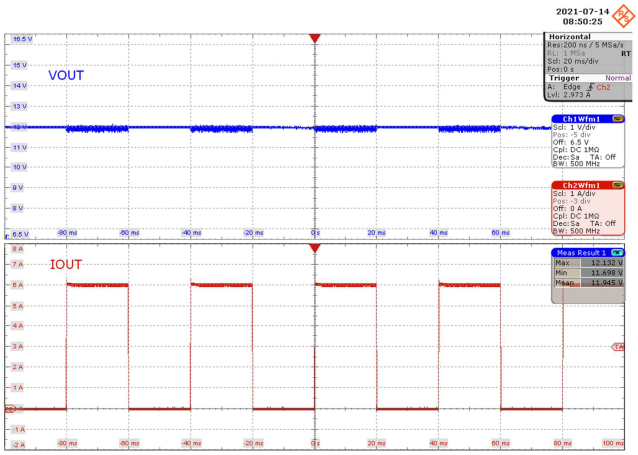


Figure 29 – Transient Response.
265 VAC, 0% – 100% Load Step.
V_{MIN}: 11.698 V, V_{MAX}: 12.132 V.
Ch1/Upper: V_{OUT}, 1 V / div.
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

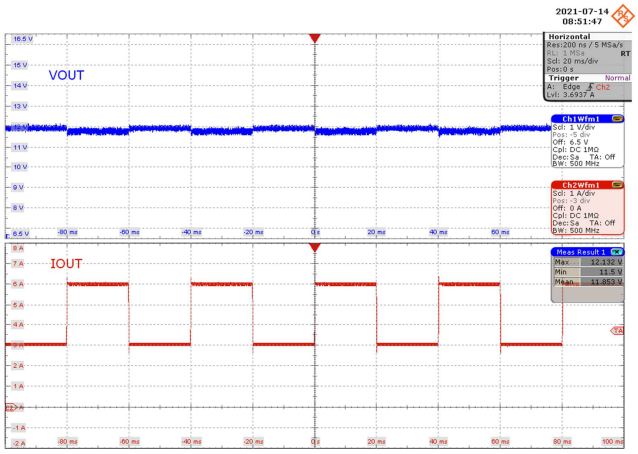


Figure 30 – Transient Response.
90 VAC, 50% – 100% Load Step.
V_{MIN}: 11.5 V, V_{MAX}: 12.132 V.
Ch1/Upper: V_{OUT}, 1 V / div.
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

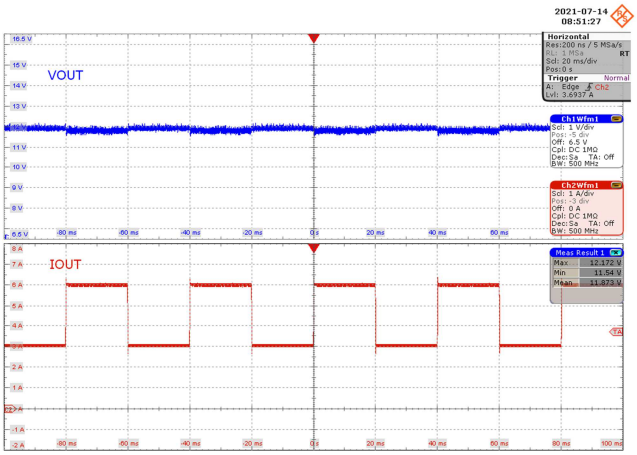


Figure 31 – Transient Response.
115 VAC, 50% – 100% Load Step.
V_{MIN}: 11.54 V, V_{MAX}: 12.172 V.
Ch1/Upper: V_{OUT}, 1 V / div.
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

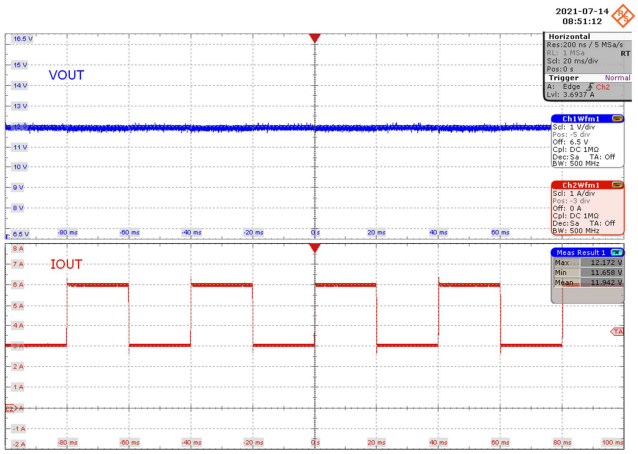


Figure 32 – Transient Response.
230 VAC, 50% – 100% Load Step.
V_{MIN}: 11.658 V, V_{MAX}: 12.172 V.
Ch1/Upper: V_{OUT}, 1 V / div.
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

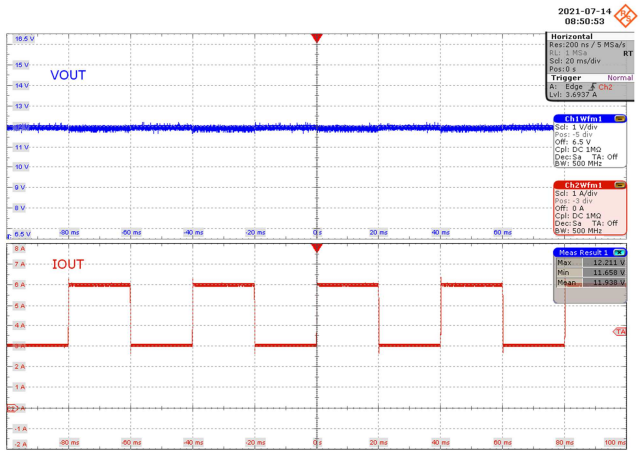


Figure 33 – Transient Response.
265 VAC, 50% – 100% Load Step.
V_{MIN}: 11.658 V, V_{MAX}: 12.211 V.
Ch1/Upper: V_{OUT}, 1 V / div.
Ch2/Lower: I_{LOAD}, 1 A / div.
Timebase: 20 ms / div.

13.4 ***Switching Waveforms***

13.4.1 Drain Voltage and Current

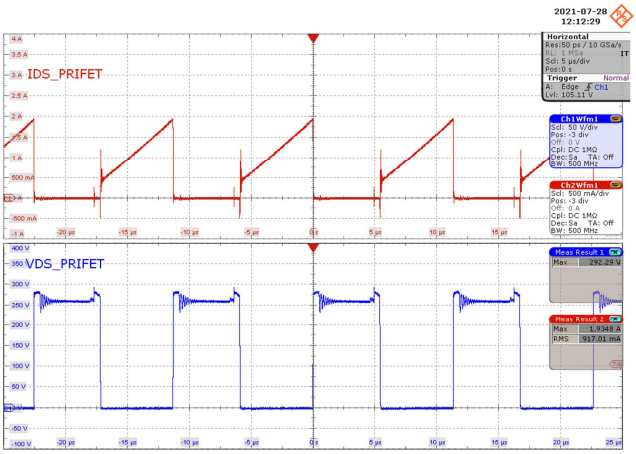


Figure 34 – Drain Voltage and Current Waveforms.
90 VAC, 100% Load.
V_{DRAIN_max} = 292.29 V.
Ch2/Upper: I_{DS_PRIFET}, 0.5 A / div.
Ch1/Lower: V_{DS_PRIFET}, 50 V / div.
Timebase: 5 µs / div.

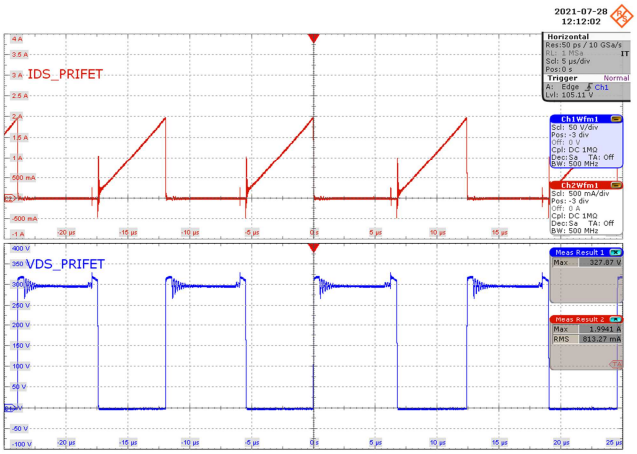


Figure 35 – Drain Voltage and Current Waveforms.
115 VAC, 100% Load.
V_{DRAIN_max} = 327.87 V.
Ch2/Upper: I_{DS_PRIFET}, 0.5 A / div.
Ch1/Lower: V_{DS_PRIFET}, 50 V / div.
Timebase: 5 µs / div.

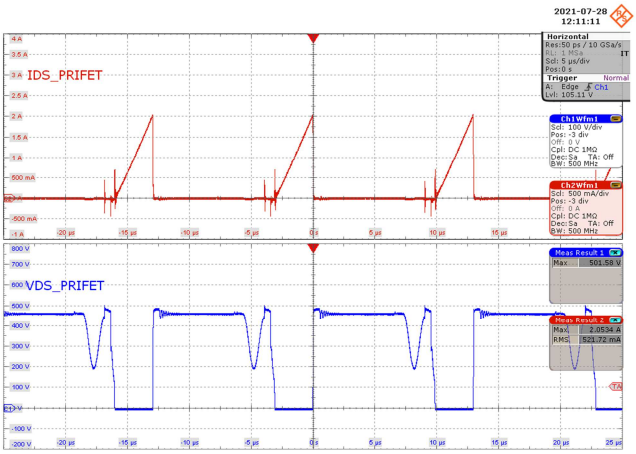


Figure 36 – Drain Voltage and Current Waveforms.
230 VAC, 100% Load.
V_{DRAIN_max} = 501.58 V.
Ch2/Upper: I_{DS_PRIFET}, 0.5 A / div.
Ch1/Lower: V_{DS_PRIFET}, 100 V / div.
Timebase: 5 µs / div.

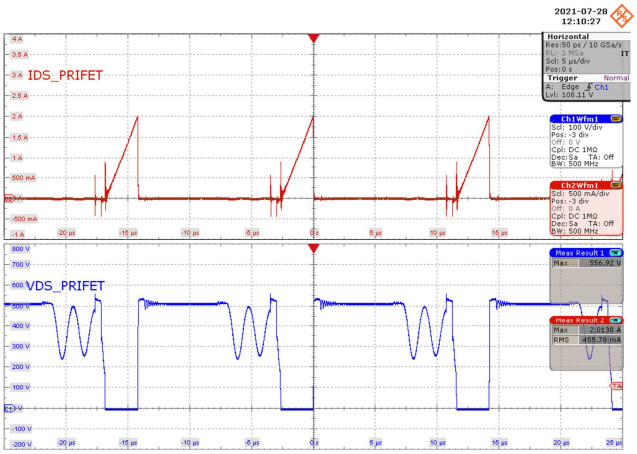


Figure 37 – Drain Voltage and Current Waveforms.
265 VAC, 100% Load.
V_{DRAIN_max} = 556.92 V.
Ch2/Upper: I_{DS_PRIFET}, 0.5 A / div.
Ch1/Lower: V_{DS_PRIFET}, 100 V / div.
Timebase: 5 µs / div.

13.4.2 ClampZero Drain Voltage and current

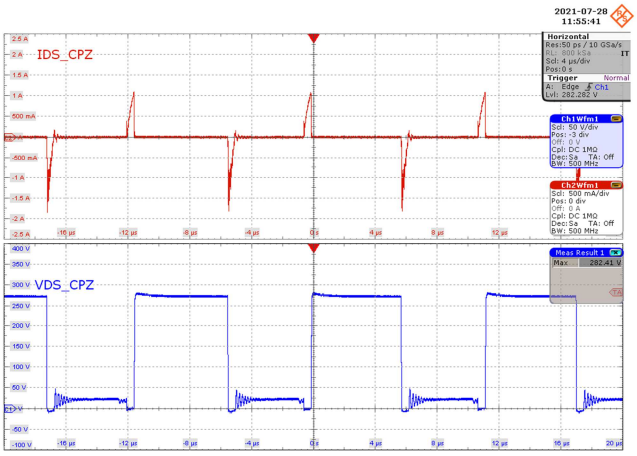


Figure 38 – ClampZero Voltage and Current Waveforms. 90 VAC, 100% Load.
V_{DS,CPZ_max} = 282.41 V
Ch2/Upper: I_{DS_CPZ}, 0.5 A / div.
Ch1/Lower: V_{DS_CPZ}, 50 V / div.
Timebase: 4 µs / div.

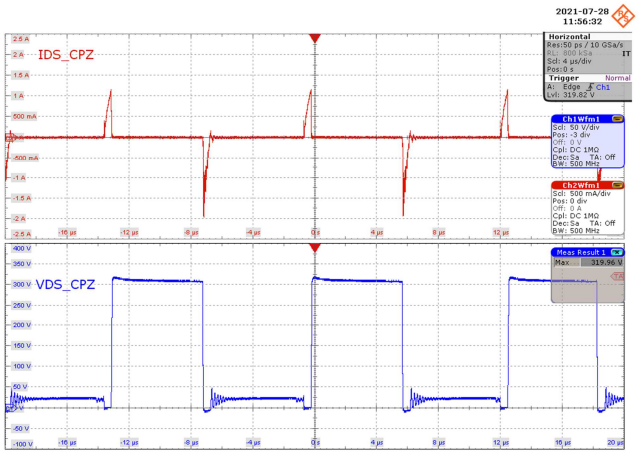


Figure 39 – ClampZero Voltage and Current Waveforms. 115 VAC, 100% Load.
V_{DS,CPZ_max} = 319.96 V
Ch2/Upper: I_{DS_CPZ}, 0.5 A / div.
Ch1/Lower: V_{DS_CPZ}, 50 V / div.
Timebase: 4 µs / div.

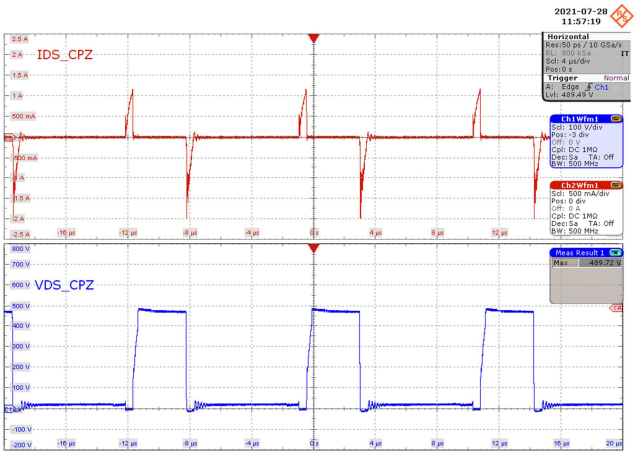


Figure 40 – ClampZero Voltage and Current Waveforms. 230 VAC, 100% Load.
V_{DS,CPZ_max} = 489.72 V
Ch2/Upper: I_{DS_CPZ}, 0.5 A / div.
Ch1/Lower: V_{DS_CPZ}, 100 V / div.
Timebase: 4 µs / div.

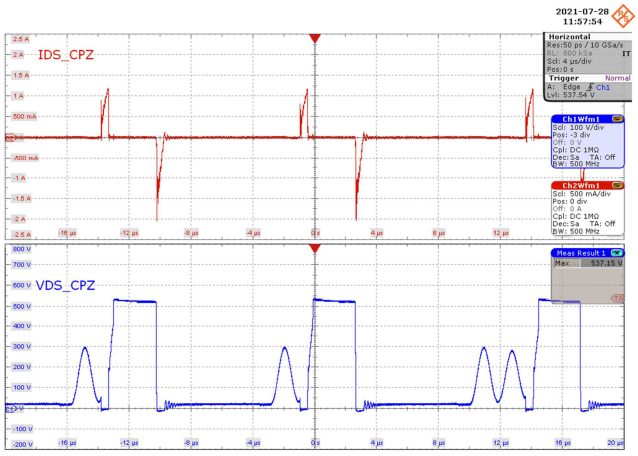


Figure 41 – ClampZero Voltage and Current Waveforms. 265 VAC, 100% Load.
V_{DS,CPZ_max} = 537.15 V
Ch2/Upper: I_{DS_CPZ}, 0.5 A / div.
Ch1/Lower: V_{DS_CPZ}, 50 V / div.
Timebase: 4 µs / div.

13.4.3 SR FET Voltage

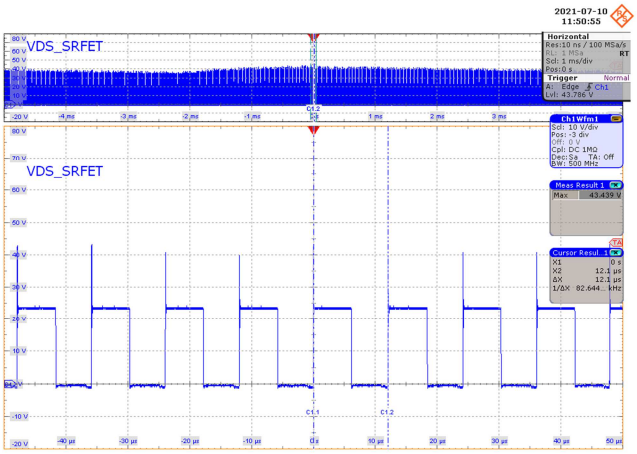


Figure 42 – SR FET Voltage Waveforms.
90 VAC, 100% Load.
$V_{DS,SRFET_max}$ = 43.439 V.
Ch1: V_{DS_SRFET}, 10 V / div.
Timebase: 1 ms / div.

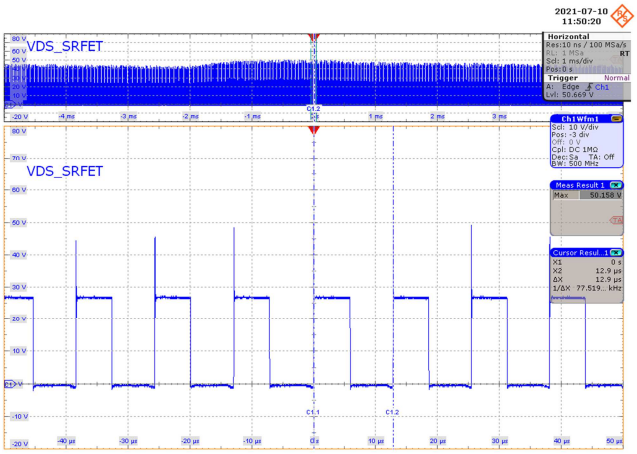


Figure 43 – SR FET Voltage Waveforms.
115 VAC, 100% Load.
$V_{DS,SRFET_max}$ = 50.158 V.
Ch1: V_{DS_SRFET}, 10 V / div.
Timebase: 1 ms / div.

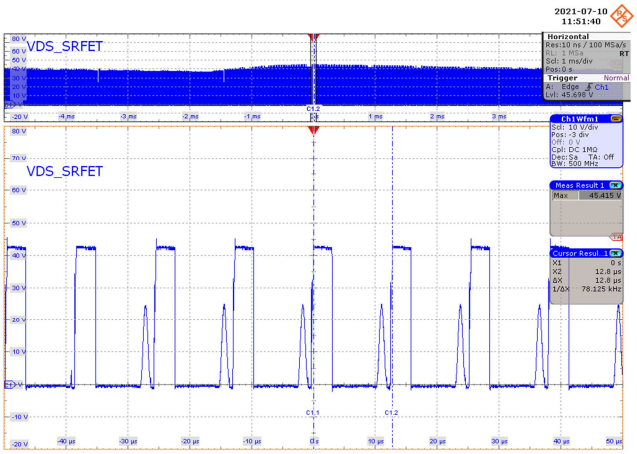


Figure 44 – SR FET Voltage Waveforms.
230 VAC, 100% Load.
$V_{DS,SRFET_max}$ = 45.415 V.
Ch1: V_{DS_SRFET}, 10 V / div.
Timebase: 1 ms / div.

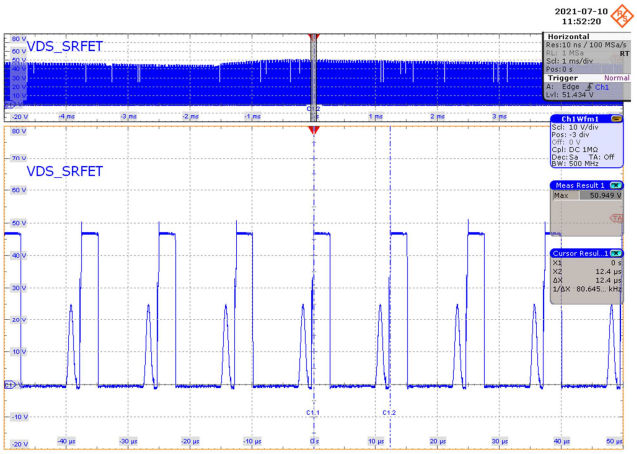


Figure 45 – SR FET Voltage Waveforms.
265 VAC, 100% Load.
$V_{DS,SRFET_max}$ = 50.949 V.
Ch1: V_{DS_SRFET}, 10 V / div.
Timebase: 1 ms / div.

13.5 *Output Ripple Measurements*

13.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF / 50 V ceramic type and one (1) 47 µF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

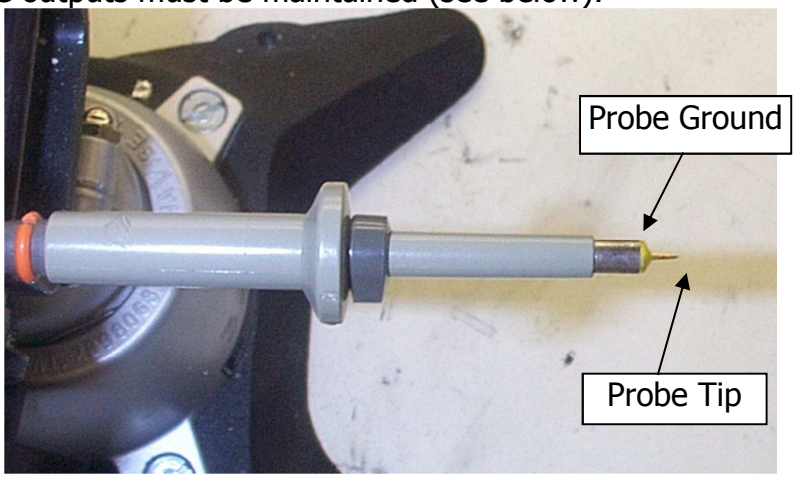


Figure 46 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

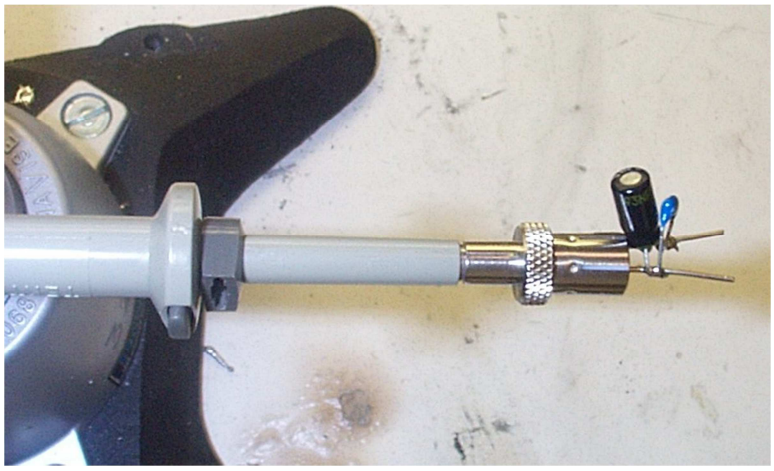


Figure 47 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.6 ***Ripple Waveforms***

13.6.1.1 100% Load

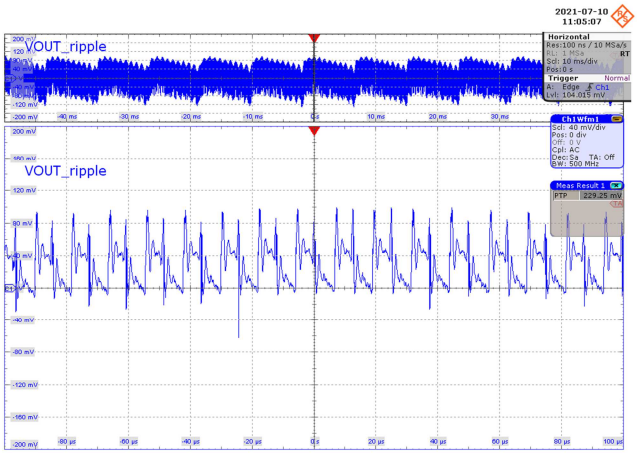


Figure 48 – Output Ripple. (PK-PK – 229 mV).
90 VAC Input, 100% Load.
V_{PK-PK}: 229 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

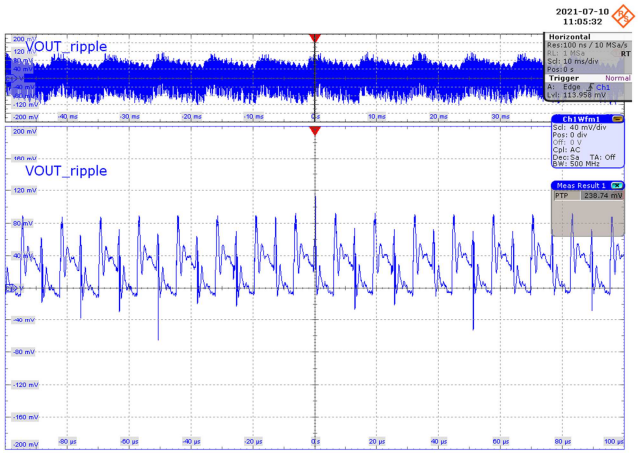


Figure 49 – Output Ripple.
115 VAC Input, 100% Load.
V_{PK-PK}: 239 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

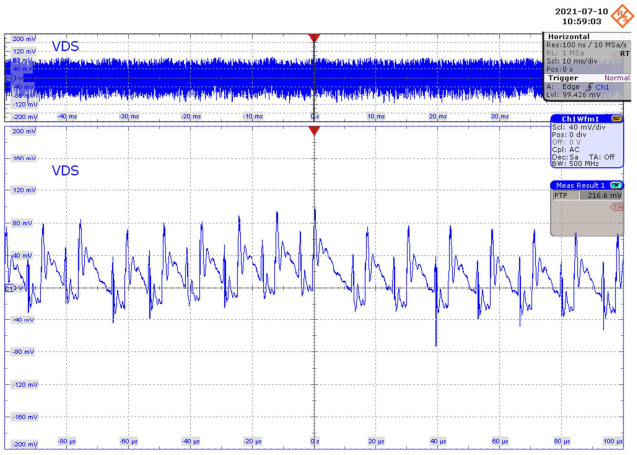


Figure 50 – Output Ripple.
230 VAC Input, 100% Load.
V_{PK-PK}: 217 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

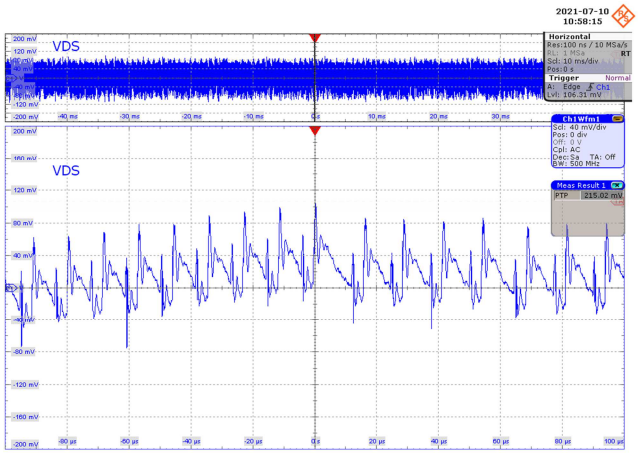


Figure 51 – Output Ripple.
265 VAC Input, 100% Load.
V_{PK-PK}: 215 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

13.6.1.2 75% Load

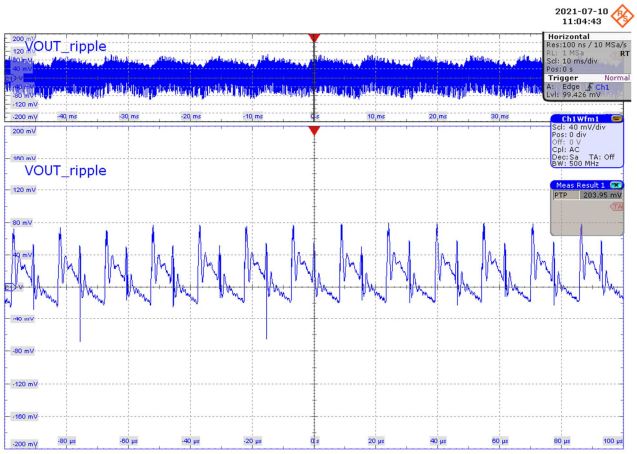


Figure 52 – Output Ripple.
90 VAC Input, 75% Load.
V_{PK-PK}: 204 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

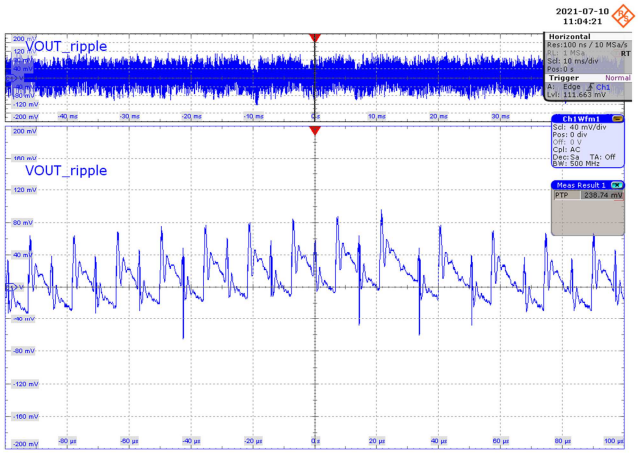


Figure 53 – Output Ripple.
115 VAC Input, 75% Load.
V_{PK-PK}: 239 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

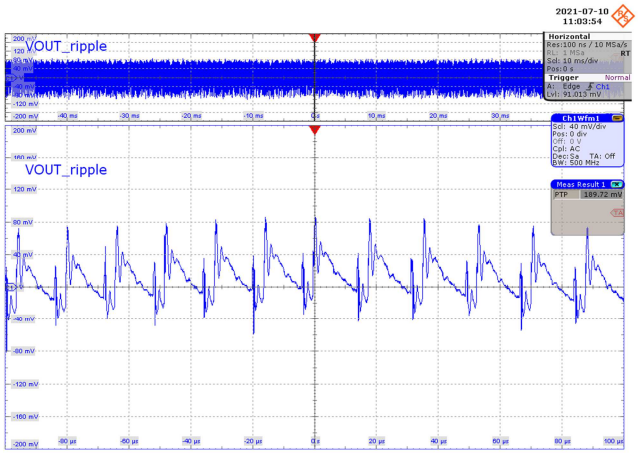


Figure 54 – Output Ripple.
230 VAC Input, 75% Load.
V_{PK-PK}: 190 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

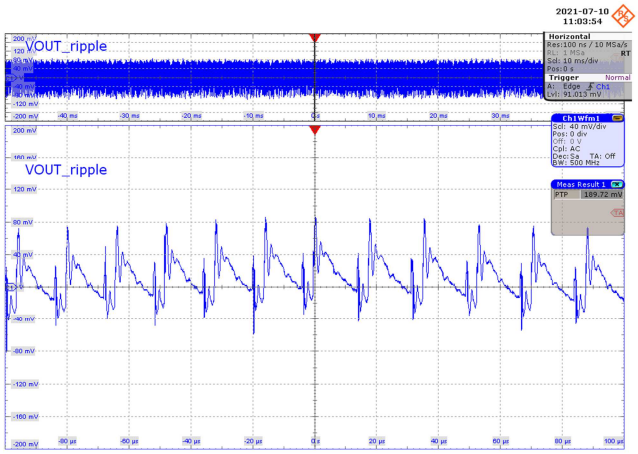


Figure 55 – Output Ripple.
265 VAC Input, 75% Load.
V_{PK-PK}: 190 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

13.6.1.3 50% Load

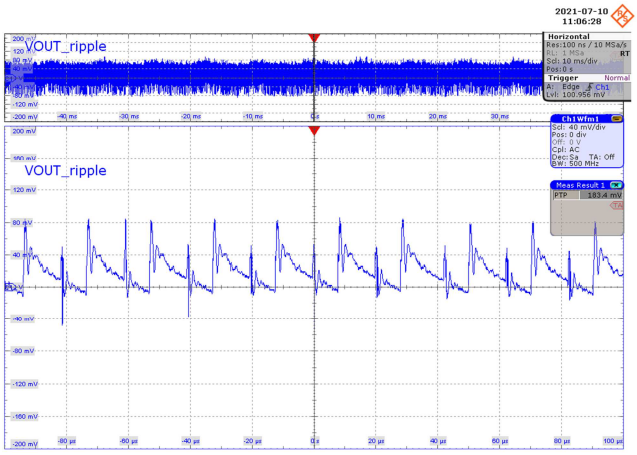


Figure 56 – Output Ripple.
90 VAC Input, 50% Load.
V_{PK-PK}: 183 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

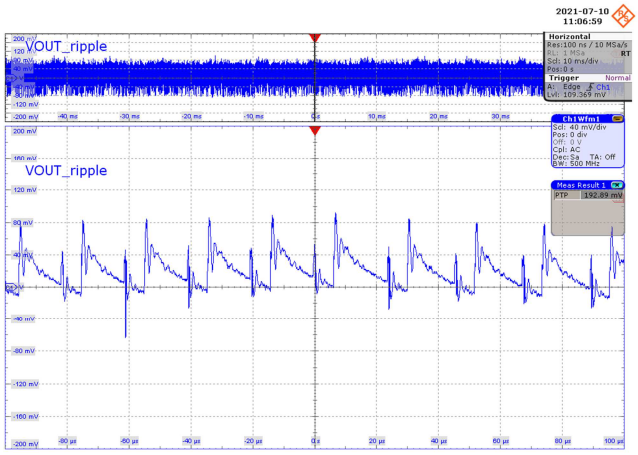


Figure 57 – Output Ripple.
115 VAC Input, 50% Load.
V_{PK-PK}: 193 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

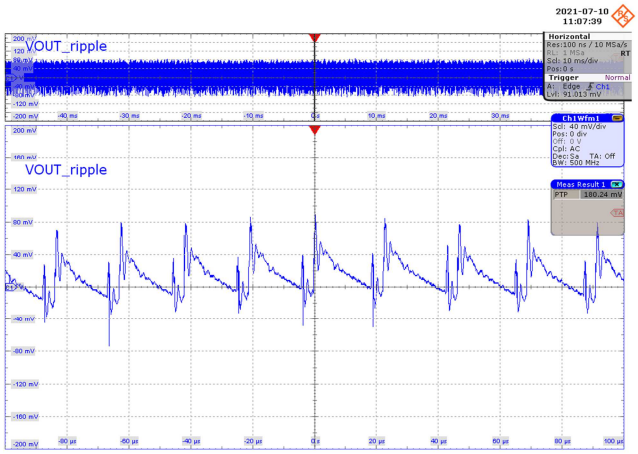


Figure 58 – Output Ripple.
230 VAC Input, 50% Load.
V_{PK-PK}: 180 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

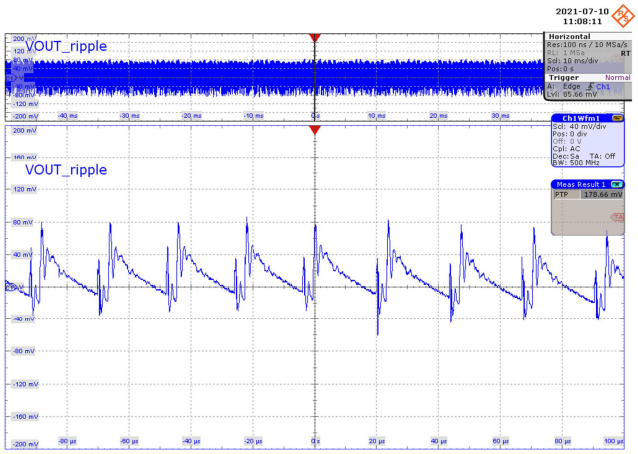


Figure 59 – Output Ripple.
265 VAC Input, 50% Load.
V_{PK-PK}: 179 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

13.6.1.4 25% Load

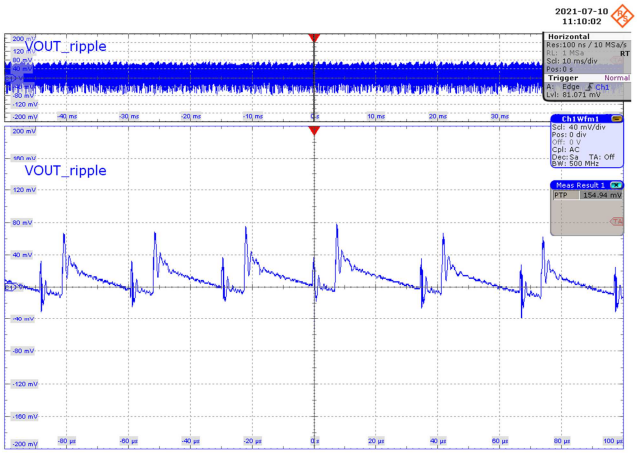


Figure 60 – Output Ripple.
90 VAC Input, 25% Load.
V_{PK-PK}: 155 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

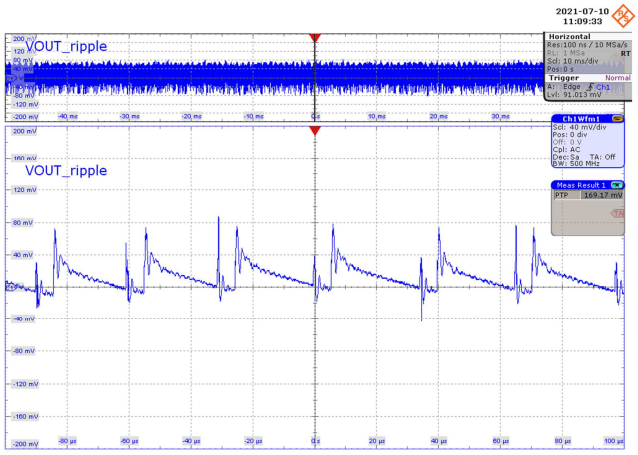


Figure 61 – Output Ripple.
115 VAC Input, 25% Load.
V_{PK-PK}: 169 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

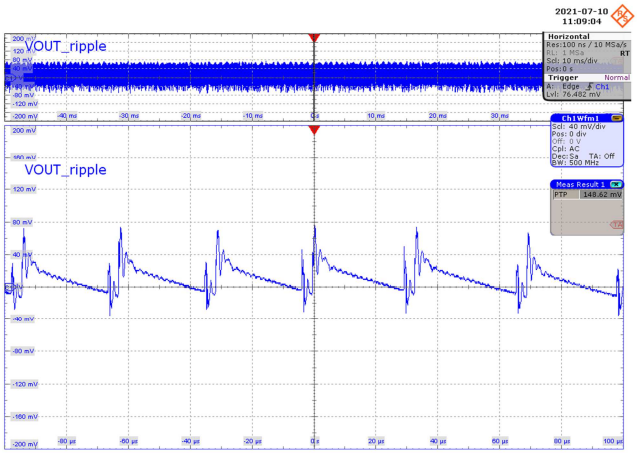


Figure 62 – Output Ripple.
230 VAC Input, 25% Load.
V_{PK-PK}: 149 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

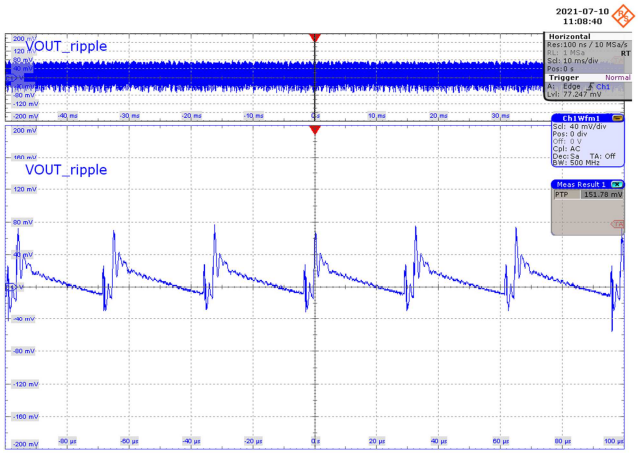


Figure 63 – Output Ripple.
265 VAC Input, 25% Load.
V_{PK-PK}: 152 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

13.6.1.5 10% Load

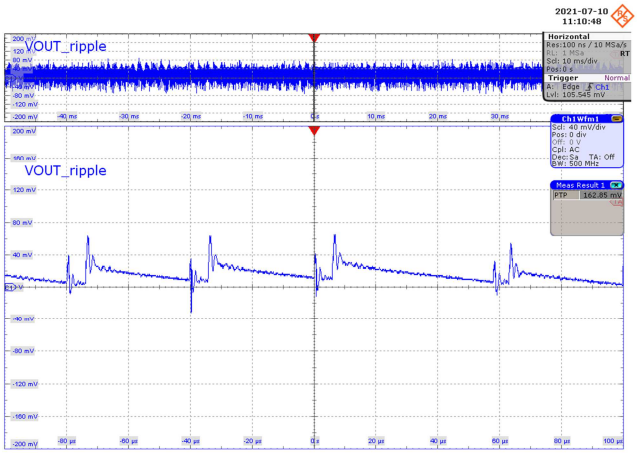


Figure 64 – Output Ripple.
90 VAC Input, 10% Load.
V_{PK-PK}: 163 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

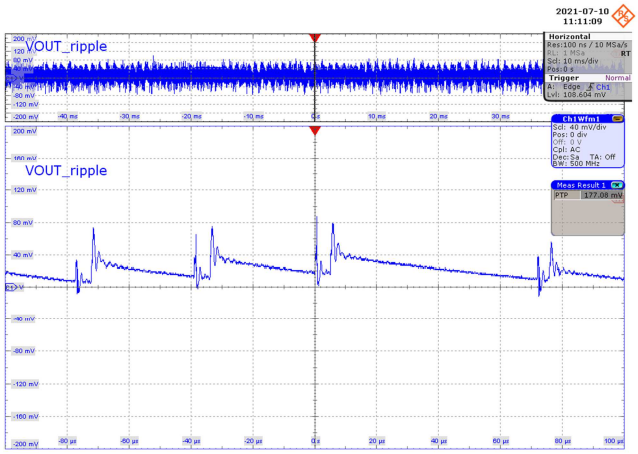


Figure 65 – Output Ripple.
115 VAC Input, 10% Load.
V_{PK-PK}: 177 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

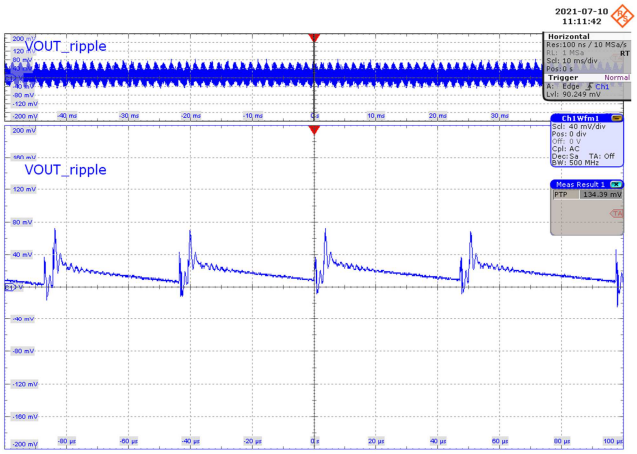


Figure 66 – Output Ripple.
230 VAC Input, 10% Load.
V_{PK-PK}: 134 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

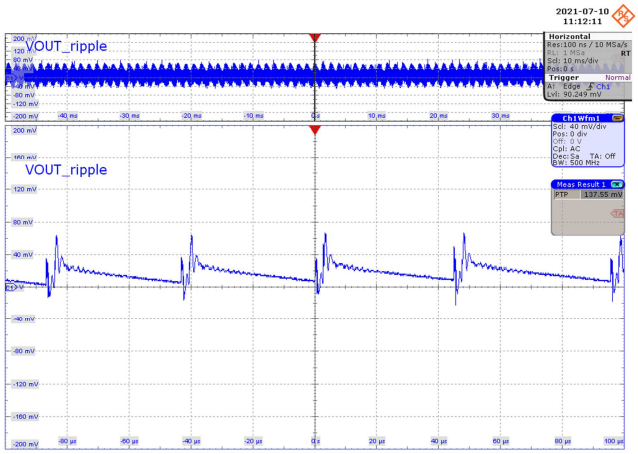


Figure 67 – Output Ripple.
265 VAC Input, 10% Load.
V_{PK-PK}: 138 mV
Ch1: V_{OUT}, 40 mV / div.
Timebase: 10 ms / div.

14 Conducted EMI

14.1 *Test set-up*

Parameter	Value
Input Voltage	115 VAC, 230 VAC
Output Load	100%
Soak Time per Line	15 minutes
Termination	Floating output ground

14.2 *Floating Ground (QP / AV)*

14.2.1 12 V, 100% Load

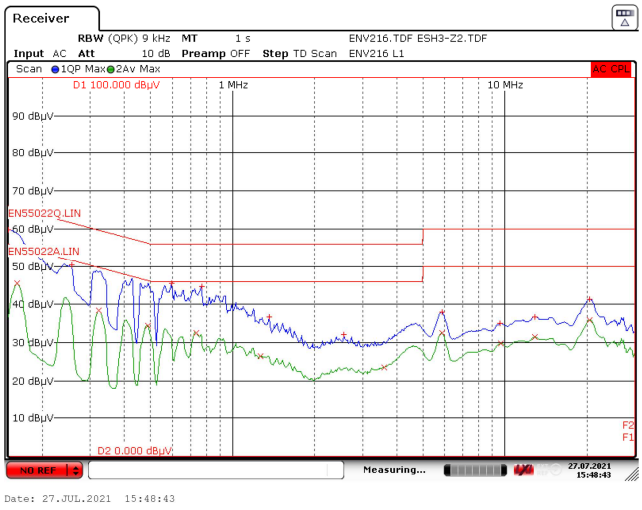


Figure 68 – 12 V / 100% Load for 115 VAC - Line.

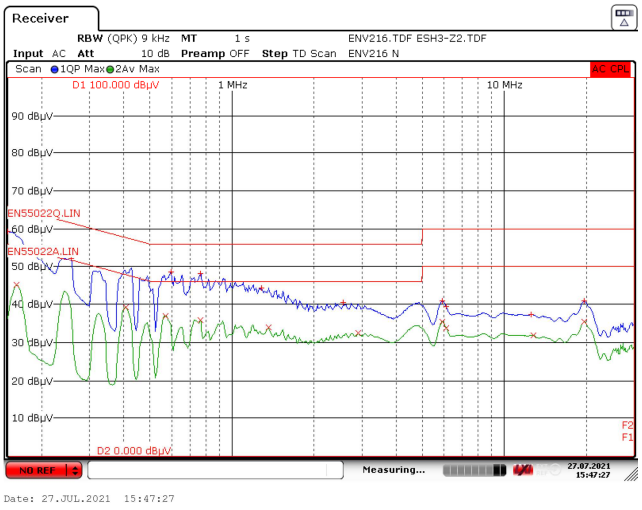


Figure 69 – 12 V / 100% Load for 115 VAC - Neutral.

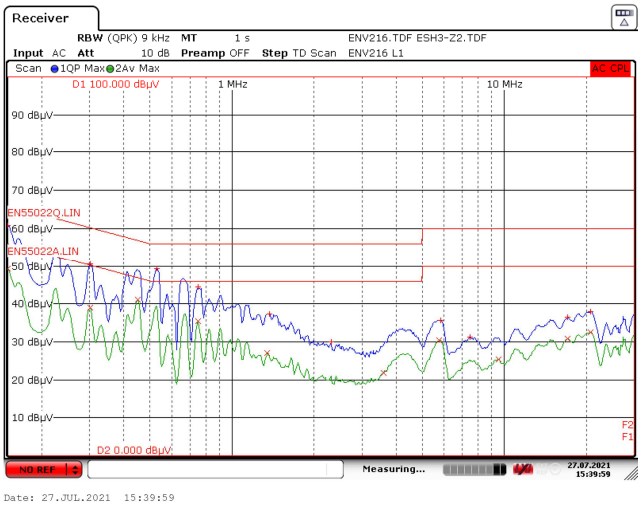


Figure 70 – 12 V / 100% Load for 230 VAC - Line.

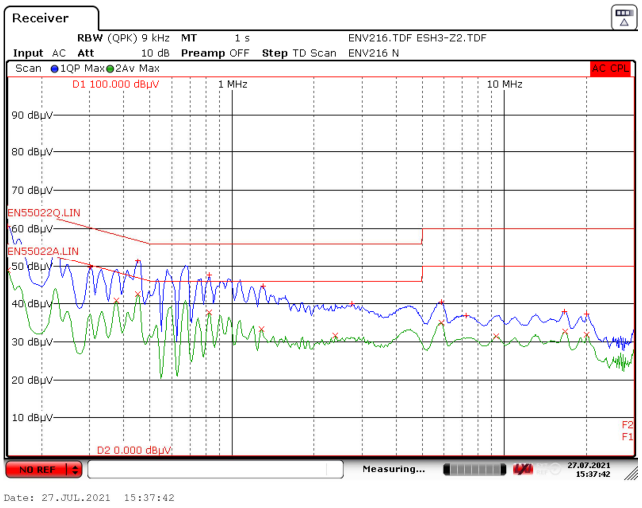


Figure 71 – 12 V / 100% Load for 230 VAC - Neutral.

15 Line Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at 0º, 90º, 180º, 270º phase angles with 10 strikes for each condition at 230 VAC input, and full load output.

15.1 *Differential Mode Test Surge (L to N), 230 VAC Input*

Parameter	Value
Input	230 VAC
Output	12V, 6A
Coupling	IEC (L->N)
Impedance	2Ω
Repetition Time	60 s
Number of Strikes per Test	10
Surge Voltage	±1000 V
Phase Angle	0º, 90º, 180º, 270º

Surge Level (V)	Phase Angle (°)	Number of Strikes	Test Result
+1000	0	10	Pass
-1000	0	10	Pass
+1000	90	10	Pass
-1000	90	10	Pass
+1000	180	10	Pass
-1000	180	10	Pass
+1000	270	10	Pass
-1000	270	10	Pass

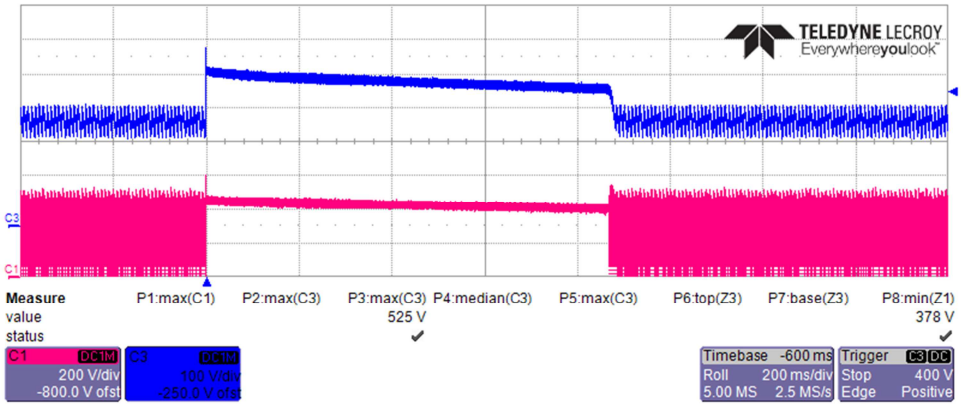


Figure 72 – Bulk Capacitor and Primary Drain Voltage at Differential Mode Surge 230 VAC, 12.0 V, 6 A Load.
Surge: Differential Mode (L to N), Combinational Wave, +1 kV, 90º Phase.
C3: $V_{BULK(400\ V)}$, 100 V / div. C1: V_{DRAIN}, 200 V / div.
Time: 200 ms / div.

15.2 *Common Mode surge (L to PE), 230 VAC Input*

Parameter	Value
Input	230 VAC
Output	12V, 6A
Coupling	IEC (L->PE)
Impedance	12Ω
Repetition Time	60 s
Number of Strikes per Test	10
Surge Voltage	±1000 V
Phase Angle	0º, 90º, 180º, 270º

Surge Level (V)	Injection Phase (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

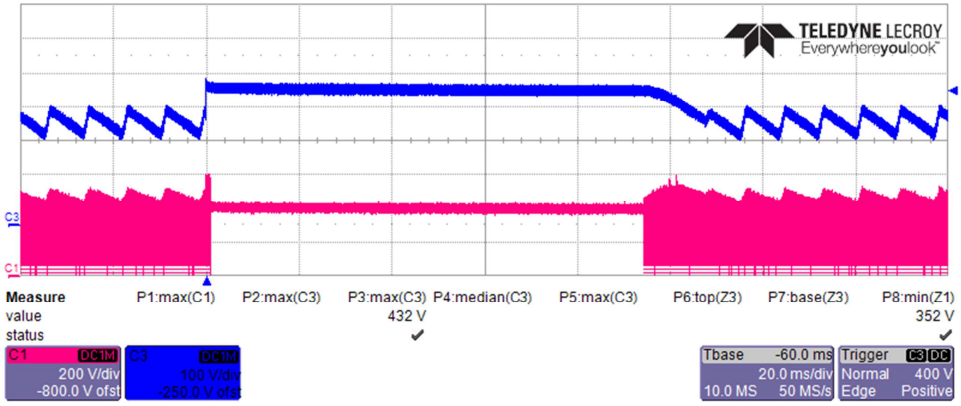


Figure 73 – Bulk Capacitor and Primary Drain Voltage at Differential Mode Surge
230 VAC, 12.0 V, 6 A Load.
Surge: Common Mode (L1 to PE), Combinational Wave, +1 kV, 90º Phase.
C3: $V_{BULK(400\ V)}$, 100 V / div. C1: V_{DRAIN}, 200 V / div.
Time: 20 ms / div.

15.3 *Common Mode Surge (N to PE), 230 VAC Input*

Parameter	Value
Input	230 VAC
Output	12V, 6A
Coupling	IEC (N->PE)
Impedance	12Ω
Repetition Time	60 s
Number of Strikes per Test	10
Surge Voltage	±1000 V
Phase Angle	0º, 90º, 180º, 270º

Surge Level (V)	Injection Phase (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

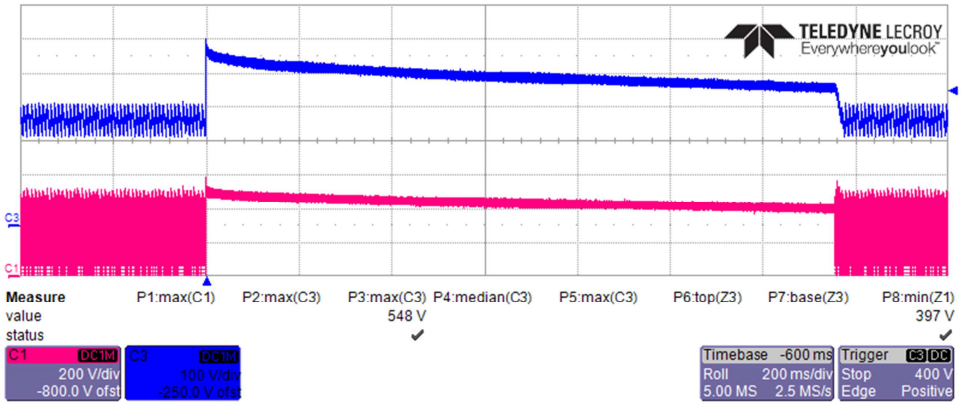


Figure 74 – Bulk Capacitor and Primary Drain Voltage at Differential Mode Surge 230 VAC, 12.0 V, 6 A Load.
Surge: Common Mode (N to PE), Combinational Wave, +1 kV, 90º Phase.
C3: $V_{BULK(400\ V)}$, 100 V / div. C1: V_{DRAIN}, 200 V / div.
Time: 200 ms / div.

15.4 *Common Mode Surge (L, N to PE), 230 VAC Input*

Parameter	Value
Input	230 VAC
Output	12V, 6A
Coupling	IEC (L,N->PE)
Impedance	12Ω
Repetition Time	60 s
Number of Strikes per Test	10
Surge Voltage	±1000 V
Phase Angle	0º, 90º, 180º, 270º

Surge Level (V)	Injection Phase (°)	Number of Strikes	Test Result
+2000	0	10	Pass
-2000	0	10	Pass
+2000	90	10	Pass
-2000	90	10	Pass
+2000	180	10	Pass
-2000	180	10	Pass
+2000	270	10	Pass
-2000	270	10	Pass

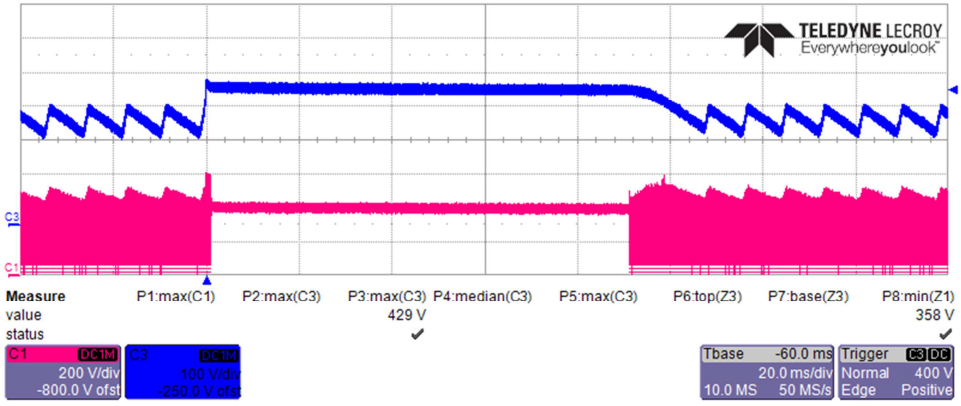


Figure 75 – Bulk Capacitor and Primary Drain Voltage at Differential Mode Surge 230 VAC, 12.0 V, 6 A Load.
Surge: Common Mode (L1,L2 to PE), Combinational Wave, +1 kV, 90º Phase.
C3: $V_{BULK(400\ V)}$, 100 V / div. C1: V_{DRAIN}, 200 V / div.
Time: 20 ms / div.

16 ESD

The unit was tested at 230 VAC input, full load with ±16.5 kV air discharge and ±8.8 kV contact discharge at the positive and negative nodes of the output with 10 strikes for each condition.

A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover, or a complete loss of function which is not recoverable.

16.1 *Test set-up*

Parameter	Value
Input Voltage	230 VAC
Output Load	100%
ESD Requirements	±8.8 kV for Contact Discharge ±16.5 kV for Air Discharge
ESD Strike Location	Output terminals on board
Number of Strikes per Test	10

16.2 *Air Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (On Board)	Number of Strikes	Test Result
+16.5	VOUT	10	Pass
-16.5	VOUT	10	Pass
+16.5	GND	10	Pass
-16.5	GND	10	Pass

16.3 *Contact Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (On Board)	Number of Strikes	Test Result
+8.8	VOUT	10	Pass
-8.8	VOUT	10	Pass
+8.8	GND	10	Pass
-8.8	GND	10	Pass

17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
02-Nov-21	ET	1.0	Initial Release	Apps & Mktg

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