CHY103
ChiPhy™ Family

Charger Interface Physical Layer IC with Complete System Level Protection

Product Highlights

- Supports Quick Charge 3.0 Class A and Class B specification
- Adaptive output overvoltage protection (AOVP)
- Secondary over-temperature protection (SOTP)
- Output soft short-circuit protection (OSSP)
- Remote shutdown protection (RESP)
  - Enables Powered Device to shutdown adapter
- Selectable hysteretic or latching shutdown
- Power consumption below 1 mW at 5 V output
- Supports InnoSwitch™, TinySwitch™, and TOPSwitch™

Typical Applications

- Battery chargers for smart phones, tablets, netbooks, digital cameras, and bluetooth accessories
- USB power output ports such as battery banks or car chargers

Description

CHY103 is a USB mobile device charger interface IC which implements the Qualcomm's Quick Charge 3.0 specification for adaptive voltage battery charging. It incorporates all necessary functions to add Quick Charge 3.0 capability to circuits incorporating Power Integrations' switcher ICs such as InnoSwitch, TinySwitch, TOPSwitch and other charger solutions employing traditional secondary-side feedback schemes.

CHY103 supports the full output voltage range of Quick Charge 3.0, including 200 mV micro-stepped voltage levels from 3.6 V to 12 V (Class A) and up to 20 V (Class B). CHY103 provides a suite of system level protection features protecting the power supply and connected Powered Device (PD) from excessive output voltages, secondary-side thermal overload, and faulty power delivery while adapter is unplugged. Additionally it allows the PD to remotely shutdown the power supply through USB data lines. The shutdown type can be configured as either hysteretic or latching.

CHY103 automatically detects whether a connected PD is Quick Charge 3.0 or Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD that is not compliant to Quick Charge 2.0 or 3.0 is detected, the CHY103 disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.

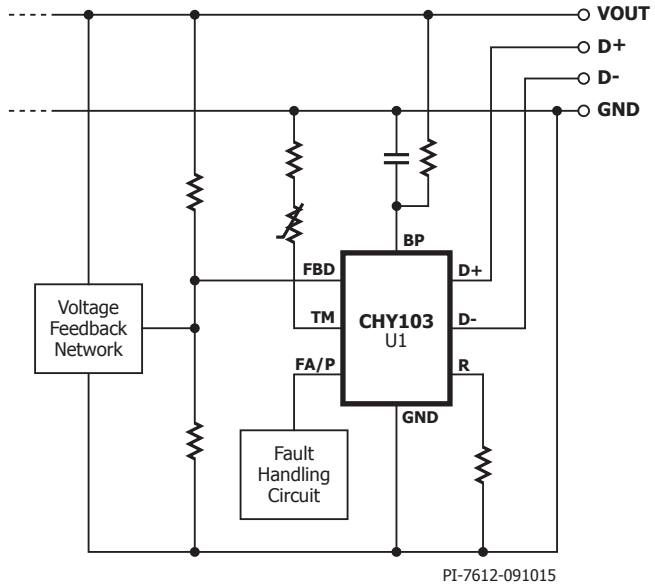


Figure 1. Typical Application Schematic.

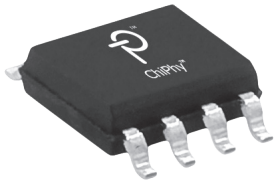


Figure 2. SO-8 (D Package).

This Product is Covered by Patents and/or Pending Patent Applications.

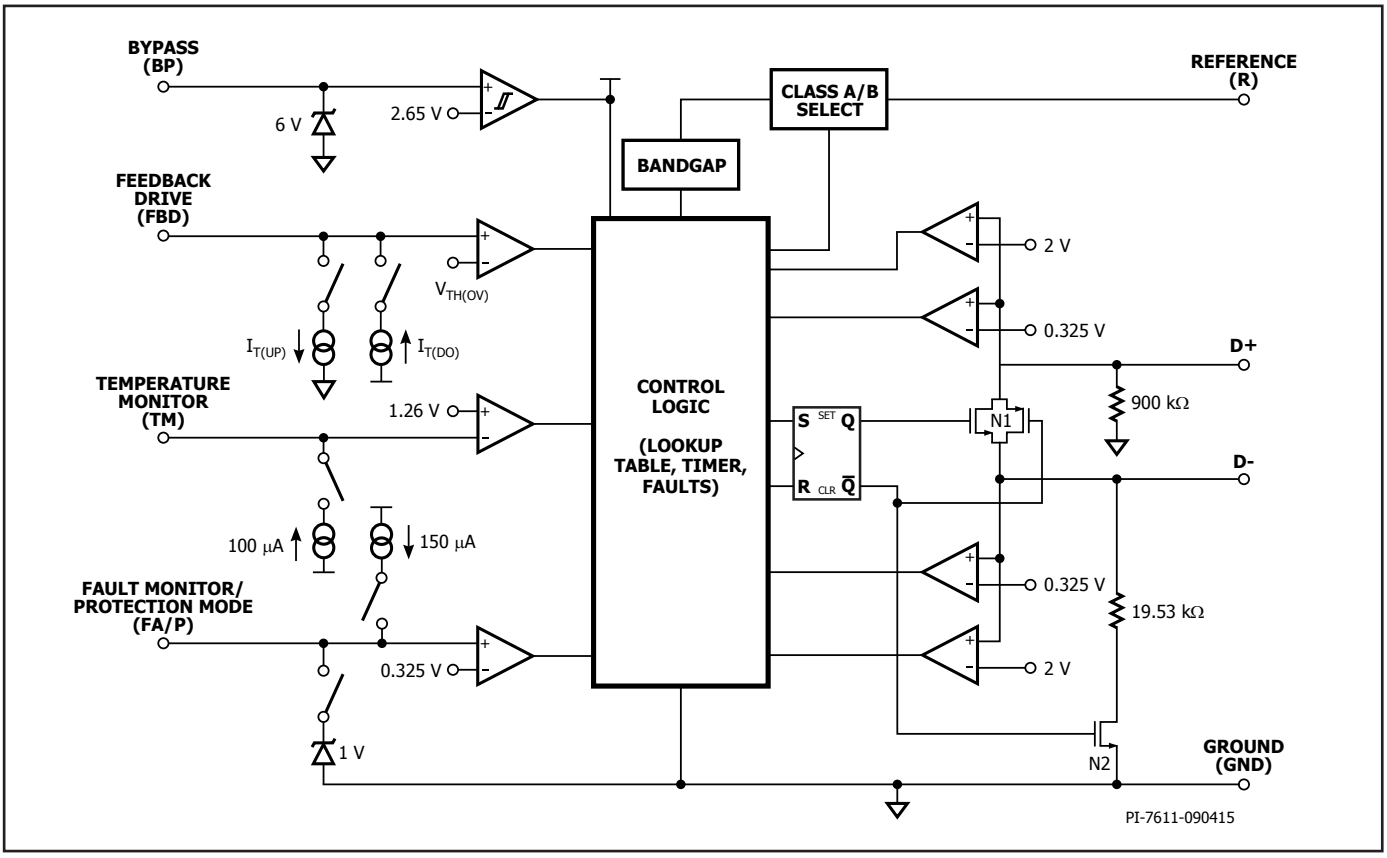


Figure 3. Functional Block Diagram.

Pin Functional Description

TEMPERATURE MONITOR (TM) Pin:
Connection point for optional external temperature sensor (NTC resistor).

FAULT MONITOR/PROTECTION MODE (FA/P) Pin:
Protection mode output driving external shutdown circuitry in case a fault is detected. Optional monitor input for faulty power delivery while output cable is unplugged.

GROUND (GND) Pin:
Ground.

FEEDBACK DRIVE (FBD) Pin:
Feedback loop drive output connected to reference input of external power supply error amplifier to set output voltage. Monitors output voltage through voltage divider connected to output rail.

BYPASS (BP) Pin:
Connection point for an external bypass capacitor for the internally generated supply voltage.

REFERENCE (R) Pin:
Connected to internal band-gap reference. Provides reference current and output voltage range selection (Class A or Class B) through connected resistor.

DATA LINE (D+) Pin:
USB D+ data line input.

DATA LINE (D-): Pin:
USB D- data line input.

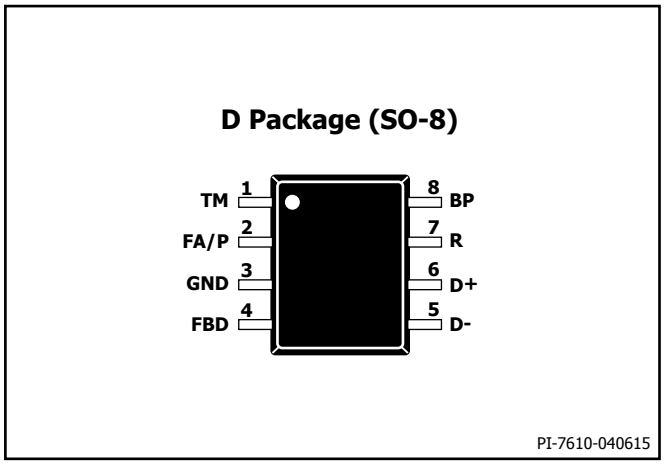


Figure 4. Pin Configuration.

Functional Description

CHY103 is a USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 3.0 specification. It incorporates all necessary functions to add Quick Charge 3.0 capability to Power Integrations' switcher ICs such as InnoSwitch, TinySwitch, and TOPSwitch.

CHY103 also supports other solutions with traditional secondary-side feedback schemes such as TL431 for instance.

Figure 5 depicts CHY103 interfacing with Power Integrations' InnoSwitch switcher IC in a configuration with hysteretic power supply shutdown, secondary thermal protection, and faulty power delivery protection when USB cable is unplugged.

CHY103 supports the full output range of Quick Charge 3.0 Class A (3.6 V to 12 V) or Class B (3.6 V to 20 V) and its subset Quick Charge 2.0 Class A (5 V, 9 V, or 12 V) or Class B (5 V, 9 V, 12 V, and 20 V). It automatically detects either Quick Charge 3.0 or Quick Charge 2.0 capable powered devices (PD) or legacy PDs compliant with USB Battery Charging Specification revision 1.2 and only enables output voltage adjustments accordingly.

Shunt Regulator

The internal shunt regulator clamps the BYPASS pin at 6 V when current is provided through an external resistor (R_{BP} in Figure 5). This facilitates powering CHY103 externally over a wide output voltage range of 3.6 V to 20 V. Recommended values are R_{BP} = 2.21 kΩ ±1% and C_{BP} = 470 nF.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry resets the CHY103 when the BYPASS pin voltage drops below 2.9 V. Once the BYPASS pin voltage drops below 2.9 V it must rise back to 3.1 V to commence correct operation.

Reference and Output Voltage Range Selection Input

Resistor R_{REF} at the REFERENCE pin is connected to an internal band gap reference and provides an accurate reference current for internal timing circuits. Resistor R_{REF} is furthermore used to select the output voltage range. R_{REF} = 38.3 kΩ ±1% selects Class A (12 V maximum output voltage) and R_{REF} = 12.4 kΩ ±1% selects Class B (20 V maximum output voltage).

Quick Charge 3.0 Interface

At power-up CHY103 turns on switch N1 (see Figure 3) short-circuiting USB data lines D+ and D- for the initial handshake between AC-DC adapter (DCP) and powered device (PD) as described in the USB Battery Charging specification revision 1.2. After the USB BC 1.2 handshake is completed, CHY103 will turn off switch N1 if it detects a Quick Charge 3.0 or Quick Charge 2.0 compliant PD. At this point the Quick Charge 2.0 handshake followed by the Quick Charge 3.0 handshake can take place as described in the Quick Charge 2.0 and Quick Charge 3.0 protocol specification. Upon completion of the Quick Charge 2.0 and Quick Charge 3.0 handshakes, CHY103 will turn on switch N2 (see Figure 3) connecting a 19.53 kΩ pull-down resistor to USB data line D-.

Table 1 summarizes the output voltage lookup and model select table and corresponding AC-DC adapter output voltages.

Portable Device (PD)		CHY103	
D+	**D-**	**Power Supply Output**	**Note**
0.6 V	0.6 V	12 V	Class A
3.3 V	0.6 V	9 V	Class A
0.6 V	3.3 V	Continuous Mode	Class A/B with ±0.2 V step size
3.3 V	3.3 V	20 V	Class B
0.6 V	GND	5 V	Default mode

Table 1. Quick Charge 3.0 Output Voltage Lookup and Mode Select Table.

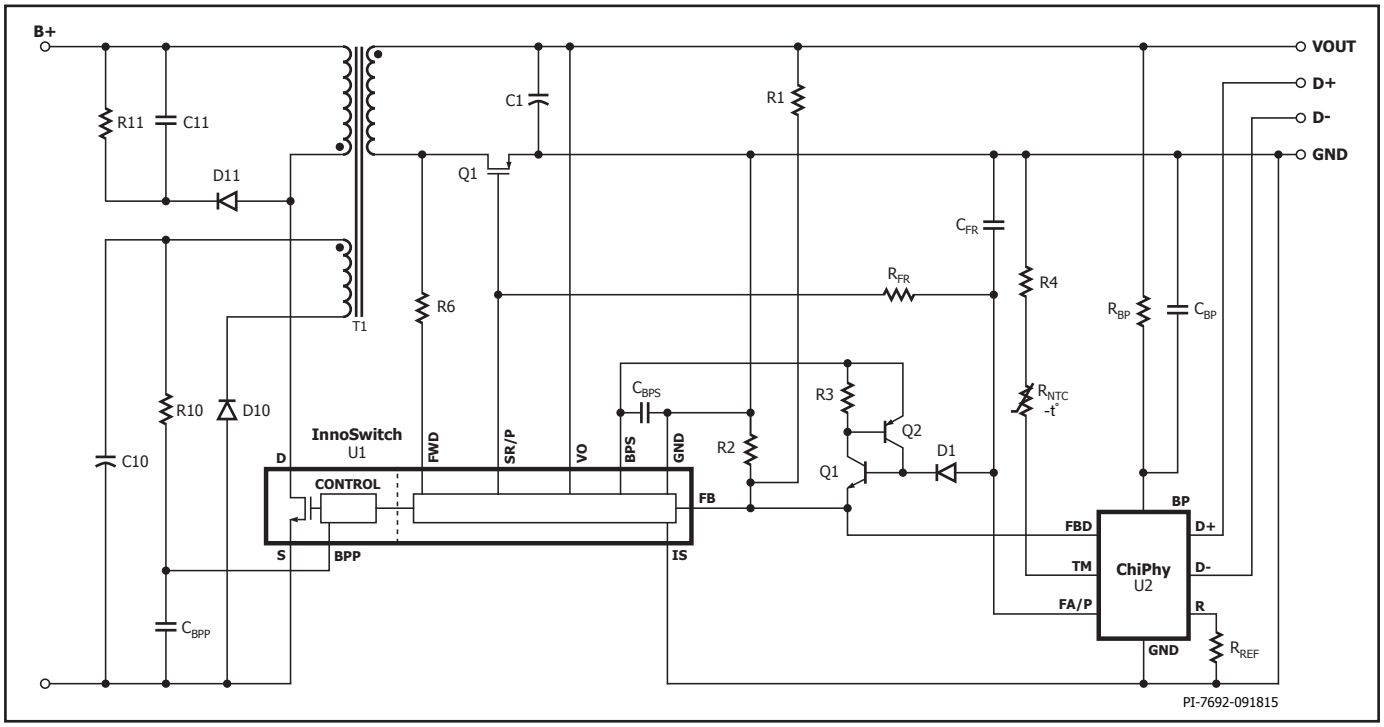


Figure 5. CHY103 with Power Integrations InnoSwitch Switcher IC with Hysteretic Fault Shutdown Protection.

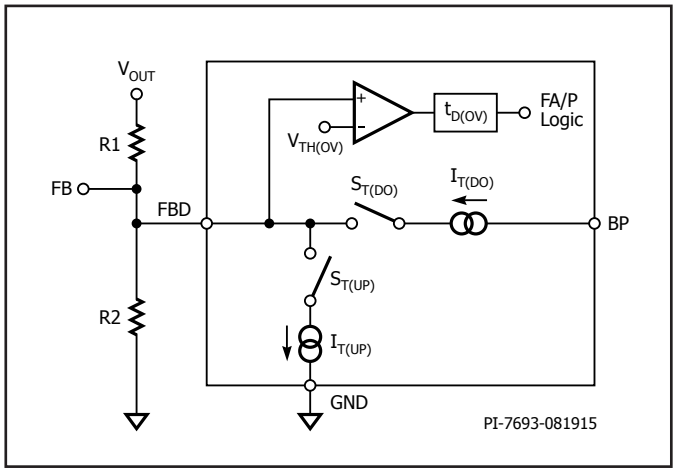


Figure 6. CHY103 FEEDBACK Pin Drive Output and Overvoltage Monitor Input.

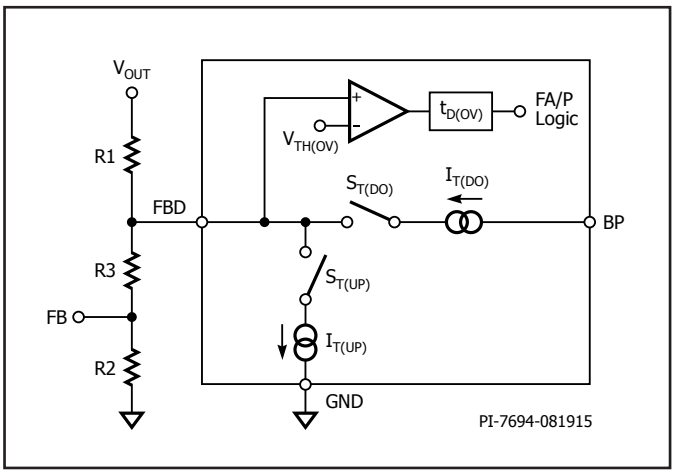


Figure 7. CHY103 interface with control loop reference voltages <1.265 V.

When the USB cable is unplugged the voltage level at D+ is pulled down by CHY103's internal resistor (see Figure 3). Once it drops below 0.325 V CHY103 will enter default mode (switch N1 is on, switch N2 is off) and sets the default output voltage of 5 V.

Feedback Loop Drive

CHY103 sets the respective output power supply voltage regulation point by directly driving the reference input of the power supply control loop error amplifier through an internal current sink $I_{T(UP)}$ and source $I_{T(DO)}$ (see Figure 6).

In default mode with a 5 V output both, the internal current source and current sink are off. To meet the output voltage step size requirement of ±0.2 V in Quick Charge 3.0 continuous mode, the mandatory value for the upper resistor in the output sensing voltage divider is R1 = 100.0 kΩ ±1%. For a FEEDBACK pin reference voltage of 1.265 V for instance used by Power Integrations' InnoSwitch switcher IC the resulting value for R2 = 34.0 kΩ ±1% to set the default output voltage to 5 V.

CHY103 can also interface with power supply control loop reference voltages lower than 1.265 V by adding resistor R3 as depicted in Figure 7.

The output voltage is determined at default 5 V output in the configuration shown in Figure 7 as follows:

$$V_{OUT} = \frac{V_{FB} \times R1}{R2} + \frac{V_{FB} \times (R2 + R3)}{R2}$$

Protection Mode

In case CHY103 detects a fault it activates its protection mode by pulling the FAULT MONITOR/PROTECTION pin high to the BYPASS pin

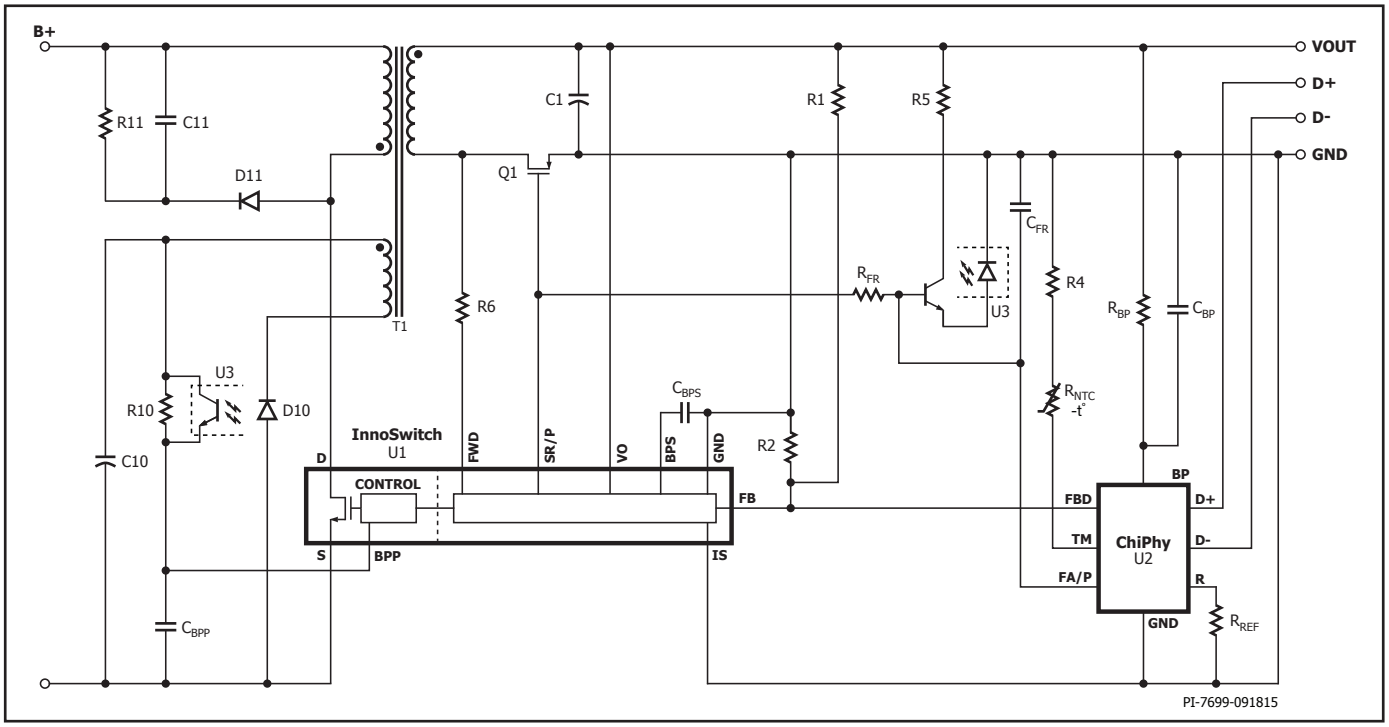


Figure 8. Primary-Side Latching Shutdown Protection Mode.

through a 150 μA current source. This signal can for instance be used to initiate hysteretic shutdown in a power supply employing InnoSwitch through circuitry Q1, Q2, D1, and R3 as shown in Figure 5.

Alternatively a primary-side latching shutdown can be configured by driving optocoupler U3 through Q1 and R5 as depicted in Figure 8. The FA/P pin is clamped internally to 1 V during normal operation.

Adaptive Output Overvoltage Protection

CHY103 monitors the voltage present at the FEEDBACK DRIVE pin in order to prevent excessive output voltage levels in case the power supply control loop lost regulation. The OV comparator threshold $V_{TH(OV)}$ (see Figure 6) is adapted to the set output voltage level (5 V, 9 V, 12 V, or 20 V) outside Quick Charge 3.0 continuous mode. As soon as the output voltage reaches 120% of the set output voltage CHY103 activates the protection mode if the OV fault is present for at least 50 μs. Adaptive OVP is blanked for 500 ms when set output voltage is stepped down outside of continuous mode (for instance from 9 V to 5 V).

In Quick Charge 3.0 continuous mode the OV comparator threshold is fixed to the respective maximum output voltage set by resistor R_{REF}. The resulting actual output OV level $V_{OUT(OV)}$ in continuous mode depends on the respective voltage $V_{OUT(SET)}$ and is as follows:

$$V_{OUT(OV)} = V_{OUT(SET)} + 2.4\,V$$

System Level Fault Protection

CHY103 offers an optional system level check to verify that power delivered by the power supply is not caused by a possible soft-short circuit present at the output but is requested by a connected PD. The system fault check is either activated automatically by CHY103 when no PD is connected (D+ is below 0.325 V) or can be initiated remotely through the connected PD as outlined in the flowchart shown in Figure 9.

The FAULT MONITOR/PROTECTION pin monitors the switching frequency of InnoSwitch through a voltage to frequency converter R_{FR} and C_{FR} (refer to Figure 5). When the voltage at the FAULT MONITOR/PROTECTION pin exceeds 0.325 V, a fault is flagged and CHY103 activates the protection mode if the fault is present for at least 40 ms. The fault monitor input is only active when no PD is connected (D+ is below 0.325 V) or a connected PD initiates a remote system level

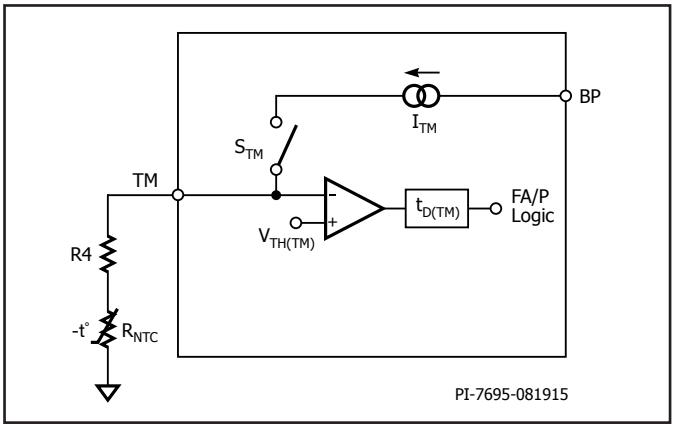


Figure 10. Optional Thermal Monitor Through NTC Resistor.

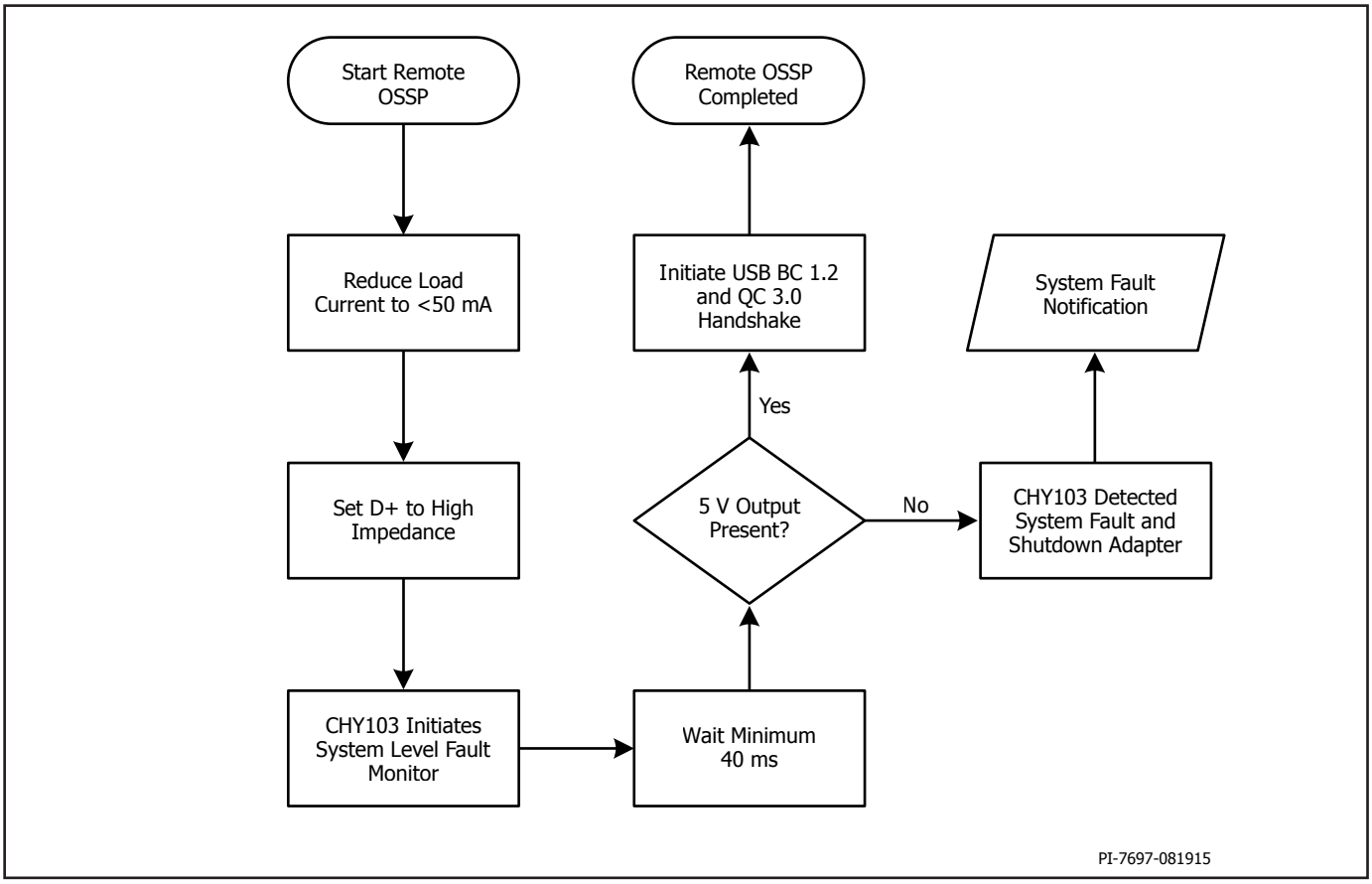


Figure 9. Remote System Level Check Flowchart.

check (see Figure 9). This way CHY103 can detect faulty power delivery which could be for instance caused by a soft short-circuit in the power supply output socket. Recommended component values are R_{FR} = 1 MΩ and C_{FR} = 1 pF.

Note that in very noisy environments noise pickup through a potentially connected USB cable may prevent correct detection of a faulty power delivery when no PD is attached despite CHY103's internal D+ pull-down resistor $R_{DAT(LKG)}$. If a power supply with CHY103 is expected to supply PDs that are not fully USB BC 1.2 compliant (e.g. leave data lines floating after handshake), it is recommended to disable this protection function by removing R_{FR} and C_{FR} (see Figure 5) and by connecting the FAULT MONITORING/ PROTECTION pin to Ground through a 470 kΩ resistor.

Temperature Sensing

CHY103 can optionally monitor temperature through an NTC resistor as depicted in Figure 10. The NTC resistor could be for instance positioned at the adapter output socket or plastic enclosure.

Current source I_{TM} is periodically turned on and the resulting voltage level at the TEMPERATURE MONITOR pin is compared to the internal threshold $V_{TH(TM)}$. CHY103 will activate the protection mode if the voltage level present at the TEMPERATURE MONITOR pin is below 1.20 V for at least 1 ms. Resistor R4 is used for tuning the shutdown temperature threshold to the desired level. For a NTC resistance value $R_{NTC(TSD)}$ at the desired shutdown temperature TSD R4 is chosen as follows:

$$R4 = 12\ \text{k}\Omega - R_{NTC(TSD)}$$

The thermal protection function can be disabled by pulling the TEMPERATURE MONITOR pin high to the BYPASS pin through a 200 kΩ resistor.

Remote Shutdown

CHY103 allows the powered device (PD) to shut down the power supply in case of a remote fault condition. The Remote Shutdown Protection (RESP) sequence required to activate the protection mode

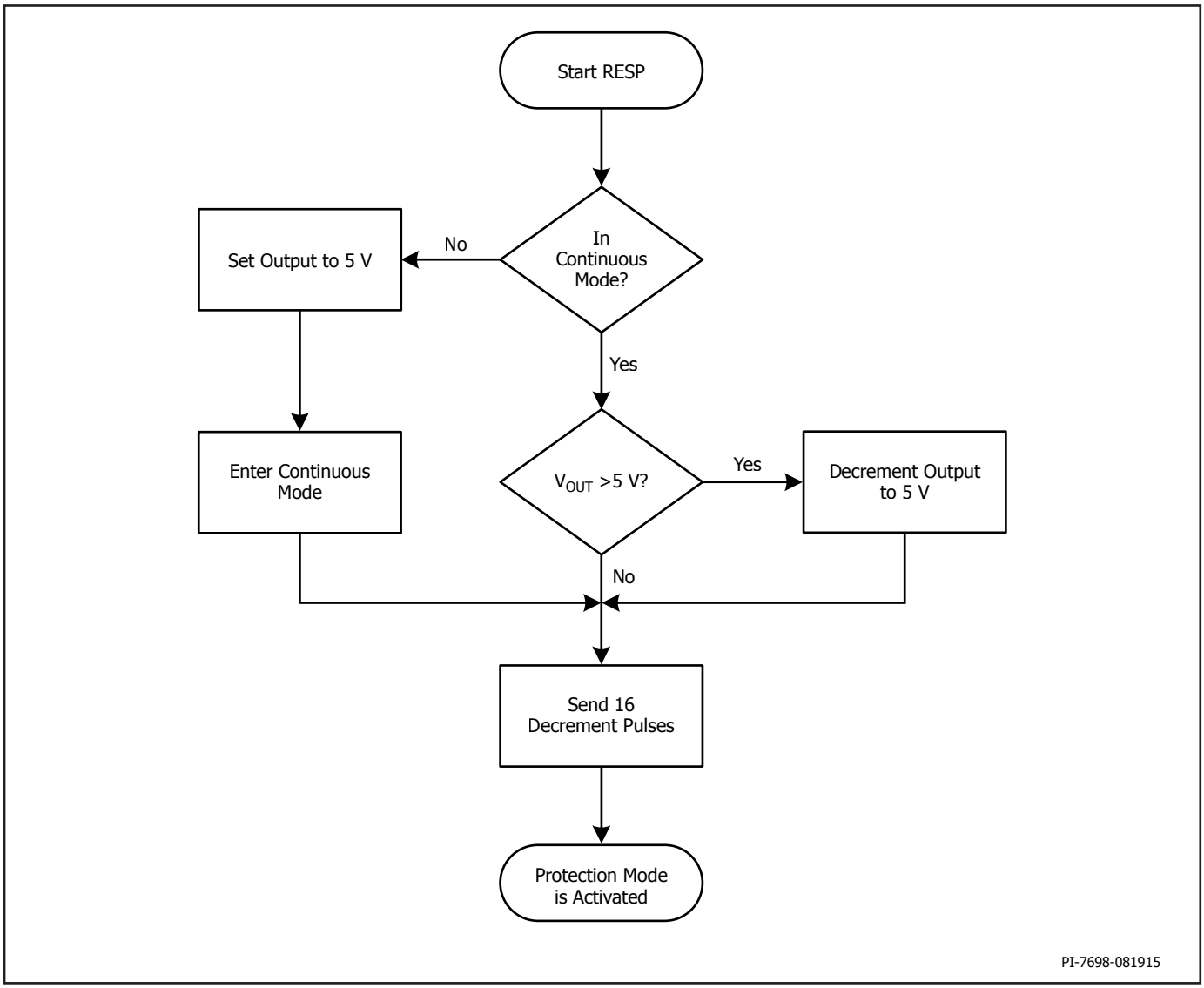


Figure 11. Remote Shutdown Protection Flowchart.

is depicted in Figure 11. Note that CHY103 will not decrement the output voltage below the minimum Quick Charge 3.0 output level of 3.6 V during the shutdown sequence.

For applications that require the power supply to be tolerant to high ESD stress levels (for instance ±15 kV air discharge), it is recommended to connected 1N4148 or equivalent diodes to the USB data line D- and D+ as depicted in Figure 12.

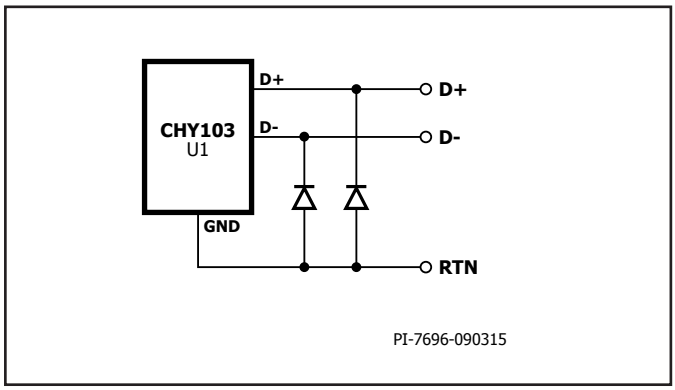


Figure 12. Data Lines High ESD Level Protection.

Application Example

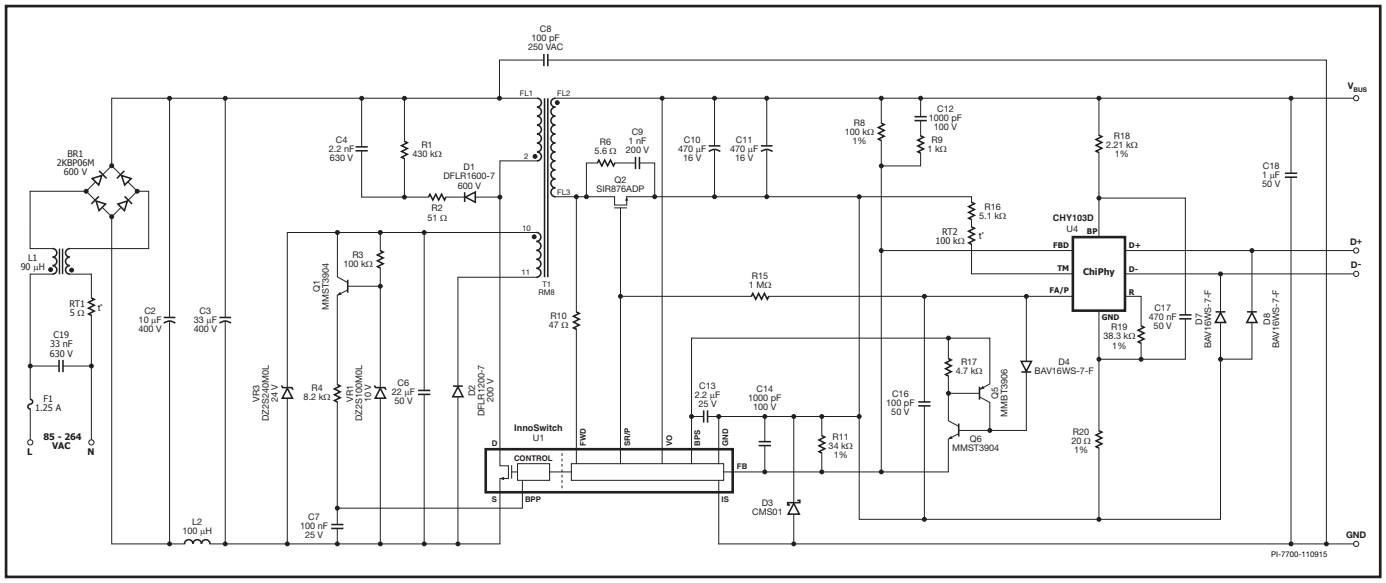


Figure 13. 5 V, 2 A; 9 V, 2 A; 12 V, 1.4 A Universal Input Charger.

The circuit shown in Figure 13 is a high efficiency universal input charger for 5 V, 2 A; 9 V, 2 A; 12 V, 1.4 A outputs, using Power Integration's InnoSwitch integrated power supply controller and CHY103 IC as a charger interface complying with the latest Quick Charge 3.0 specification. This application example highlights key points for designing a properly functioning QC 3.0 compatible power supply using the CHY103 IC.

Circuit Design Considerations

CHY103 Side

REFERENCE Pin

Resistor R19 is the reference resistor and must be 38.3 kΩ ±1% for selecting Class A (12 V max.) mode of operation and 12.4 kΩ ±1% for selecting Class B (20 V max.) mode of operation.

BYPASS Pin

Resistor R18 is recommended to be 2.21 kΩ to provide sufficient supply voltage for the CHY103 IC at the minimum output voltage (3.6 V). It also limits the current flowing into the BYPASS pin and thus into the shunt regulator at the BYPASS pin to less than 8 mA for the maximum set output voltage of 20 V.

The BYPASS pin decoupling capacitor C17 is recommended to be 470 nF. A 50 V rated X5R or X7R dielectric capacitor is recommended for best results.

FAULT MONITOR/PROTECTION MODE Pin

Recommended values for R15 and C16 are 1 MΩ and 100 pF respectively. It is needed to detect a loaded condition and trigger protection in case of loading in the absence of a portable device.

D+/D- Short to V_o Protection Circuit

Resistor R20 (20 Ω) is recommended to protect the CHY103 IC in case of a short-circuit between D+ or D- to V_{BUS}.

TEMPERATURE MONITOR Pin

Resistor R16 and RT2 are needed if additional system level thermal protection is required. Recommended values are R28 = 5.1 kΩ and RT2 = 100 kΩ.

InnoSwitch Side

Transformer Design

The transformer needs to be designed to deliver the maximum output power of 18 W (9 V, 2 A). Also, the auxiliary winding turns should provide enough bias supply voltage at the lowest rated output voltage of the charger (3.6 V) at no-load condition to supply at least 1 mA of current to the PRIMARY BYPASS (BPP) pin of the InnoSwitch IC.

PRIMARY BYPASS Pin

Since the bias winding voltage is a function of the output voltage which varies from 3.6 V to 12 V, a linear regulator comprising of resistor R3, BJT Q1 and Zener diode VR1 limits the current through R4. As a result, the current being supplied to the PRIMARY BYPASS pin of the InnoSwitch IC doesn't exceed the needed PRIMARY BYPASS pin supply current (I_{S2}~1 mA, InnoSwitch data sheet) at higher output voltages (>10 V) so as to minimize no-load input power at these voltages.

Diodes D7 and D8 should be used at the output terminal, to offer ESD protection for D+ and D- pins.

InnoSwitch FEEDBACK Pin

It is recommended to use a 1 nF capacitor for the InnoSwitch IC FEEDBACK pin decoupling capacitor.

The feedback divider network R8 and R11 must be 100 kΩ ±1% and 34 kΩ ±1% respectively for the CHY103 IC to have a fixed step size of 200 mV.

Resistor R9 and capacitor C12 form a phase lead (feed-forward) network that ensures stable operation and minimizes output voltage overshoot and undershoot during transient load conditions. This phase lead network prevents pulse bunching. Recommended values are R9 = 1 kΩ and C12 = 1000 pF.

Fault Protection

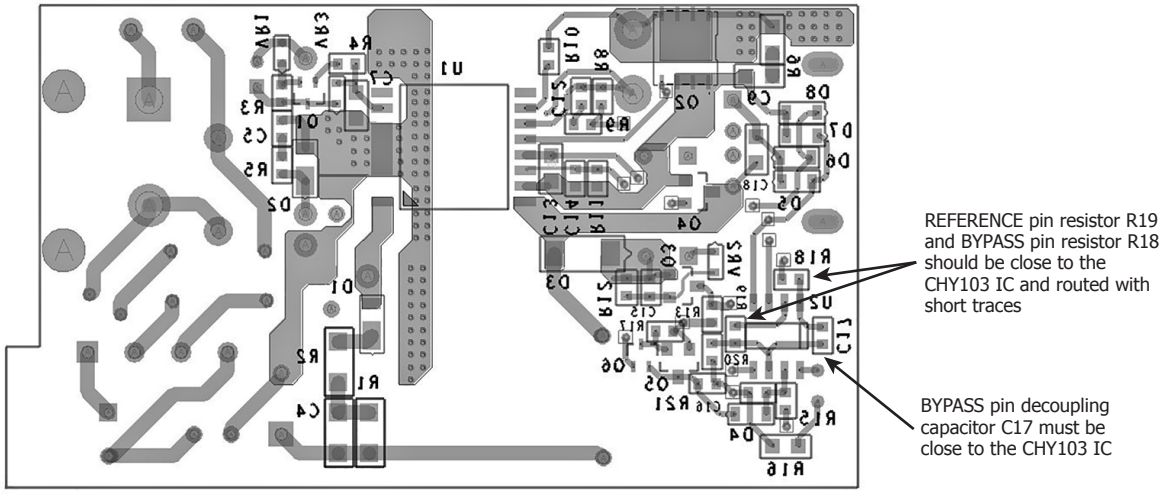
Fault protection by primary-side latching shutdown can be achieved by using an optocoupler U3 as shown in Figure 8. This circuit should be designed such that the InnoSwitch PRIMARY BYPASS pin current should be more than at least 9.6 mA (i.e. the PRIMARY BYPASS pin

shutdown threshold current of the InnoSwitch IC) at the time as per to InnoSwitch-IC data sheet when the optocoupler conducts. If the optocoupler transistor current is such that the primary bypass current does not exceed the PRIMARY BYPASS pin shutdown threshold current value, then even though CHY103 IC's protection feature would work (CHY103 IC FAULT MONITOR/PROTECTION MODE pin goes high), the power supply would not latch off to protect the device from any damage.

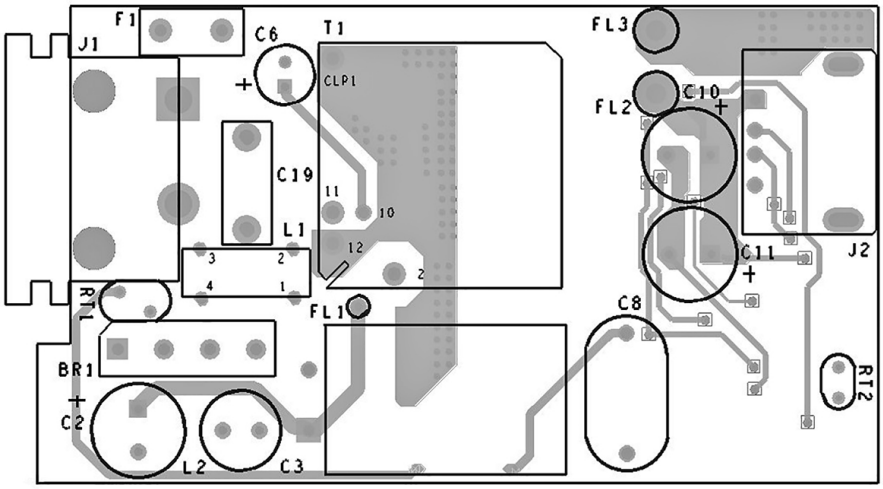
Alternatively a non-latching protection scheme can be implemented as described in the Protection Mode section of the data sheet (Figure 5). With the circuit proposed in Figure 5, during a fault condition (CHY103 IC FAULT MONITOR/PROTECTION MODE pin goes high), the InnoSwitch-IC FEEDBACK pin voltage will be raised above the maximum V_{FB} value (=1.28 V as per the InnoSwitch data sheet), which causes the InnoSwitch IC to stop switching. Once the InnoSwitch IC has stopped switching for a time equal to $t_{AR(SK)}$ (as per to InnoSwitch data sheet), auto-restart of the InnoSwitch IC will follow. This process will repeat until the fault condition is removed.

Layout Design Considerations

- The decoupling capacitor C17 must be located directly adjacent to the BYPASS pin and should be routed with short traces.
- Resistors R19 for providing reference current to the IC and resistor R18 for providing bias supply to the IC should be placed as close to the IC as possible and should be routed with short traces.
- The FEEDBACK DRIVE pin of CHY103 is connected to the FEEDBACK pin of InnoSwitch and hence a close placement of the two ICs is recommended.
- It is also recommended to place capacitor C16 close to the CHY103 IC.



PCB – Bottom Side



PCB – Top Side

PI-7701-090415

Figure 14. PCB Layout Design.

Absolute Maximum Ratings[3]

BYPASS Pin Voltage ..... -0.3 to 9 V
REFERENCE Pin Voltage ..... -0.3 to 9 V
TM/FA/P/FBD Pin Voltage ..... -0.3 to 9 V
D+/D- Pin Voltage ..... -0.3 to 6.5 V
BYPASS Pin Current .....25 mA
D+/D- Pin Current ..... 1 mA[1]
Operating Junction Temperature..... -40 °C to +150 °C
Operating Ambient Temperature..... -40 °C to +105 °C
Storage Temperature .....-65 °C to 150 °C
Lead Temperature[2] .....260 °C

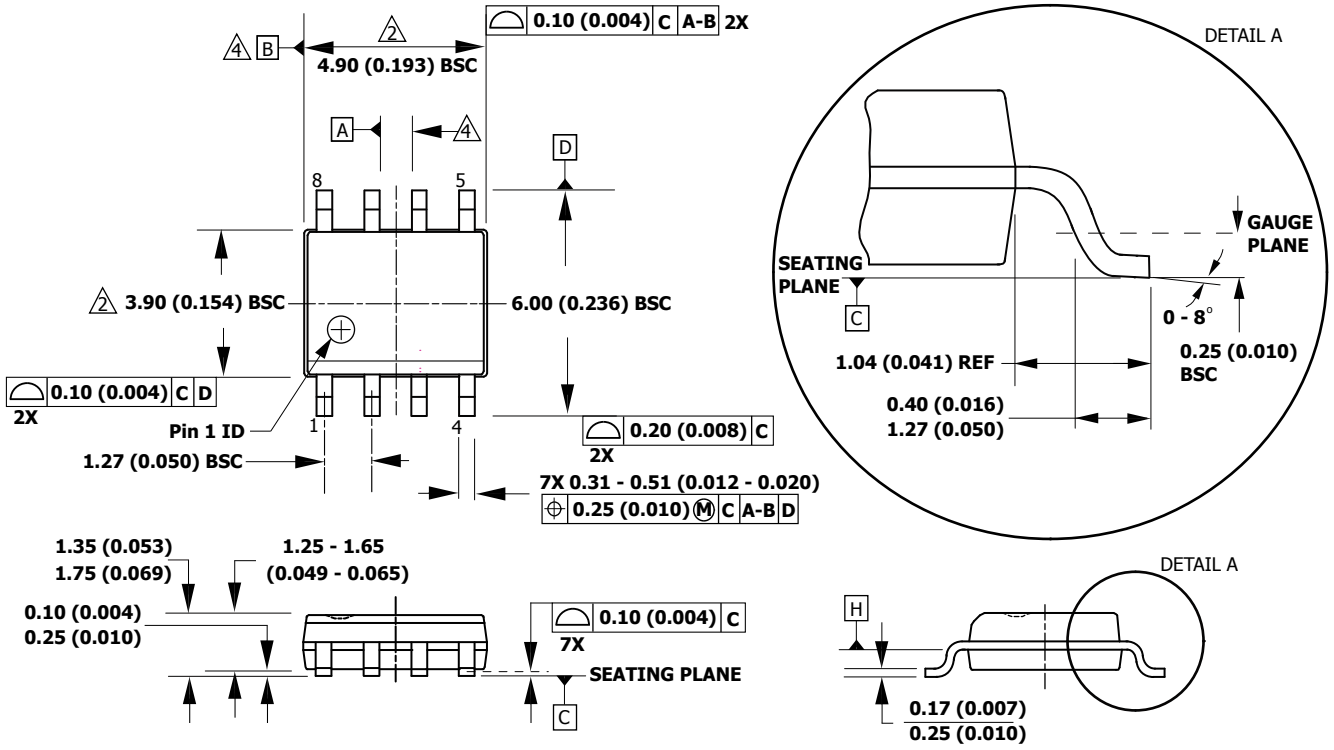
Notes:
1. Per USB BC 1.2 and HVDCP specifications.
2. 1/16 in. from case for 5 seconds.
3. The Absolute Maximum Ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Supply and Reference Function						
BYPASS Pin Voltage	V_{BP}	T_J = +25 °C	3.1	4.3	6.3	V
Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$		2.7	2.9	3.1	V
BYPASS Pin Source Current	I_{BPSC}	V_{BP} = 4.3 V, R_{REF} = 38.3 kΩ, T_J = 25 °C			200	µA
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 8 mA	5.7	6	6.3	V
REFERENCE Pin Voltage	V_R	R_{REF} = 38.3 kΩ Class A	0.350	0.383	0.395	V
		R_{REF} = 12.4 kΩ Class B	0.350	0.372	0.400	
Data Line D+ and D- Functions (HVDCP Interface)						
Data Detect Voltage	$V_{DAT(REF)}$		0.250	0.325	0.400	V
Output Voltage Selection Reference	$V_{SEL(REF)}$		1.8	2	2.2	V
Data Lines Short-Circuit Delay	$T_{DAT(SHORT)}$	V_{OUT} ≥ 0.8 V		10	20	ms
D+ High Glitch Filter Time	$T_{GLITCH(BC)\ DONE}$		1000		1500	ms
D- Low Glitch Filter Time	$T_{GLITCH(DM)\ LOW}$		1			ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)\ CHANGE}$		20	40	60	ms
Continuous Mode Glitch Filter Time	$T_{GLITCH(CONT)\ CHANGE}$		100		200	µs
D+ Leakage Resistance	$R_{DAT(LKG)}$	V_{BP} = 3.1-6.3 V, VD+ = 0.5-3.6 V Switch N1 is Off	300	900	1500	kΩ
D- Pull-Down Resistance	$R_{DM(DWN)}$		14.25	19.53	24.5	kΩ
Switch N1 On-Resistance	$R_{DS(ON)N1}$	V_{BP} = 4.3 V, V_{D+} ≤ 3.6 V, I_{DRAIN} = 200 µA		17	25	Ω
Data Line Capacitance	$C_{DCP(PWR)}$	See Note A			1	nF

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to +85 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
FEEDBACK Pin Drive Functions							
Toggle Up Current Source Step	$\Delta I_{T(UP)}$			1.737	1.930	2.123	µA
Toggle Down Current Source Step	$\Delta I_{T(DO)}$			1.737	1.930	2.123	µA
Protection Functions							
Output Overvoltage Threshold	$V_{TH(OV)}$	QC 2.0 Mode Class A / Class B	$I_{T(UP)}$ = 0 (5 V)	1.44	1.52	1.60	V
			$I_{T(UP)}$ = 40 µA (9 V)	1.60	1.72	1.84	
			$I_{T(UP)}$ = 70 µA (12 V)	1.74	1.87	2.00	
			$I_{T(UP)}$ = 150 µA (20 V)	2.12	2.28	2.44	
		QC 3.0 Continuous Mode	R_{REF} = 38.3 kΩ Class A	1.74	1.87	2.00	
			R_{REF} = 12.4 kΩ Class B	2.12	2.28	2.44	
Output OV Detection Delay Time	$t_{D(OV)}$				50		µs
Output OV Detection Blanking Time	$t_{B(OV)}$			500			ms
Output Socket Fault Detection Threshold	$V_{TH(FA)}$			0.250	0.325	0.400	V
Socket Fault Detection Delay Time	$t_{D(FA)}$				40		ms
FA/P Pin Clamp Voltage	V_{CL}	I_{CLAMP} = 100 µA			1		V
Over-Temperature Detection Threshold	$V_{TH(TM)}$			1.12	1.20	1.28	V
Over-Temperature Detection Delay Time	$t_{D(TM)}$				1		ms
Temperature Monitor Current Source	I_{TM}				100		µA
Temperature Monitor Current On-Time	$t_{ON(ITM)}$				12		ms
Temperature Monitor Current Duty Ratio	D_{ITM}				1		%
Protection Mode Current Source	I_P			100	150	200	µA

NOTES:
A. Guaranteed by design. Not tested in production.

SO-8 (D Package)



D08A

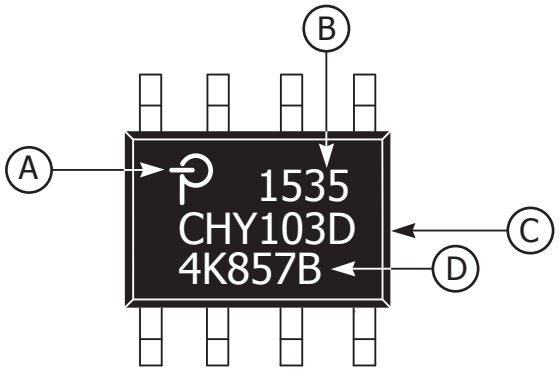
Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

PI-5615-020515

PACKAGE MARKING

SO-8 Package Marking



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-7788-111115

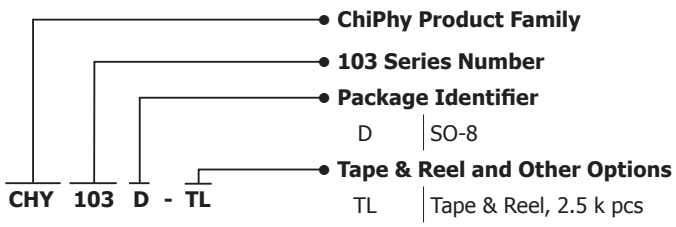
MSL Table

Part Number	MSL Rating
CHY103DG	1

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 V (max) on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Machine Model ESD	JESD22-A115C	> ±200 V on all pins

Part Ordering Information



Notes

Revision	Notes	Date
B	Code A data sheet.	09/15
C	Schematic error corrections made to Figures 5, 8 and 13.	09/18/15
D	Updated V_R values.	9/23/15
E	Made correction to Figure 13, and updated $\Delta I_{T(UP)}$ and $\Delta I_{T(DO)}$ parameter limits. Added MSL, ESD and Latch-up tables, added Package Marking.	11/11/15
F	Updated text on page 7 in Remote Shutdown section and page 8 in D+/D- Short to V_O Protection Circuit and Primary BYPASS Pin sections.	12/02/15
G	Updated D+/D- Pin Voltage in Abs Max Ratings section, $V_{BP(RESET)}$ and $R_{DS(ON)N1}$ parameters per PCN-16241.	06/16

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