CHY100
ChiPhy™ Family

Charger Interface Physical Layer IC

Product Highlights

- Fully supports Quick Charge 2.0 specification
  - Class A: 5 V, 9 V, and 12 V output voltage
  - Class B: 5 V, 9 V, 12 V, and 20 V output voltage
- USB battery charging specification revision 1.2 compatible
  - Automatic USB DCP shorting D+ to D- line
  - Default 5 V mode operation
- Supports TOPSwitch and TinySwitch
- Very low power consumption
  - Below 1 mW at 5 V output
- Fail safe operation
  - Adjacent pin-to-pin short-circuit fault
  - Open circuit pin fault

Typical Applications

- Battery chargers for smart phones, tablets, netbooks, digital cameras, and bluetooth accessories
- USB power output ports

Description

CHY100 is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 2.0 specification. It incorporates all necessary functions to add Quick Charge 2.0 capability to Power Integrations' switcher ICs such as TOPSwitch or TinySwitch and other solutions employing traditional feedback schemes.

CHY100 supports the full output voltage range of either Class A or Class B. Optionally Class B can be inhibited for protecting the battery charger from accidental damage.

CHY100 automatically detects whether a connected Powered Device (PD) is Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0 is detected the CHY100 disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.

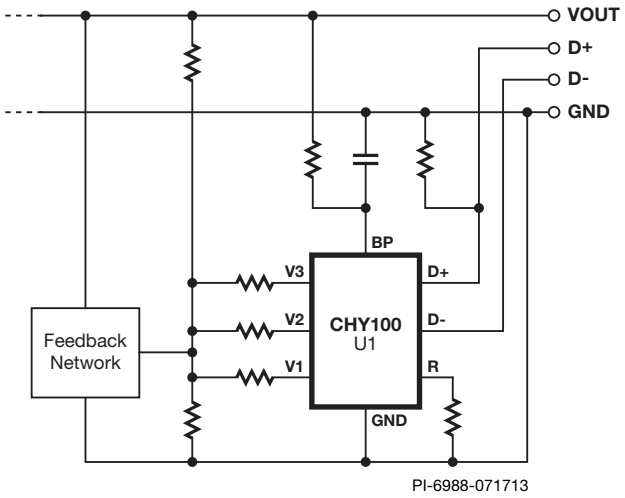
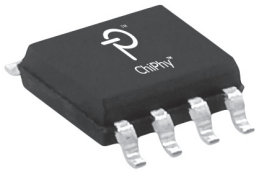


Figure 1. Typical Application Schematic.



SO-8 (D Package)

Figure 2. Package Option.

This Product is Covered by Patents and/or Pending Patent Applications.

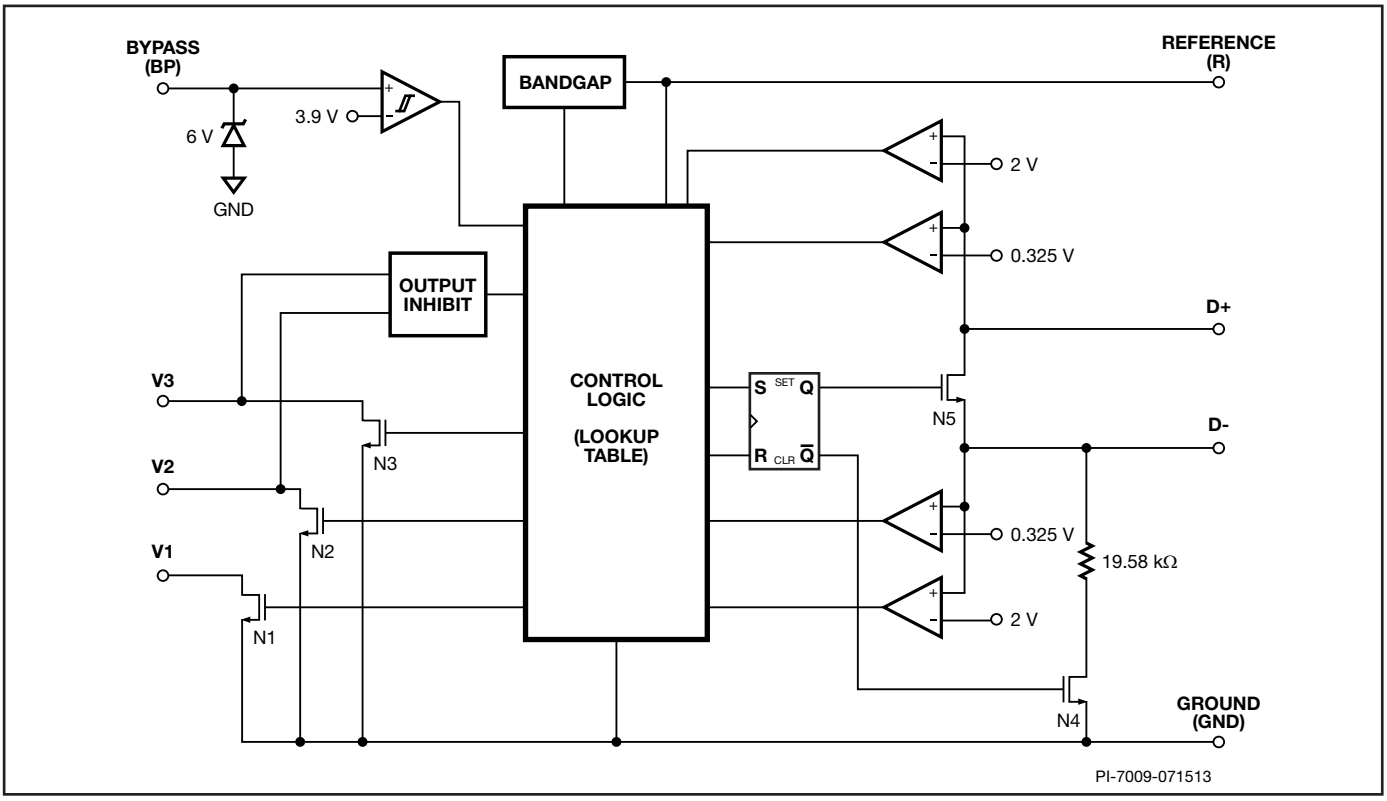


Figure 3. Functional Block Diagram.

Pin Functional Description

GROUND (GND) Pin
Ground.

V1 Pin
Open Drain input of output voltage adjustment switch. Active for 9 V, 12 V, and 20 V output setting.

V2 Pin
Open Drain input of output voltage adjustment switch. Active for 12 V, and 20 V output setting.

V3 Pin
Open Drain input of output voltage adjustment switch. Active for 20 V output setting.

BYPASS (BP) Pin
Connection point for an external bypass capacitor for the internally generated supply voltage.

REFERENCE (R) Pin
Connected to internal band-gap reference. Provides reference current through connected resistor.

DATA LINE D+ Pin
USB D+ data line input.

DATA LINE D- Pin
USB D- data line input.

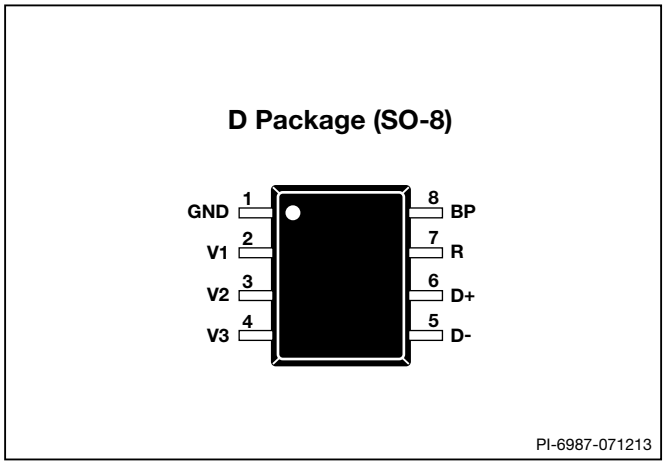


Figure 4. Pin Configuration.

Functional Description

CHY100 is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 2.0 specification. It incorporates all necessary functions to add Quick Charge 2.0 capability to Power Integrations' integrated switcher ICs such as TOPSwitch or TinySwitch.

CHY100 also supports other solutions with traditional feedback schemes like optocoupler and secondary reference regulator TL431 as depicted in Figure 5.

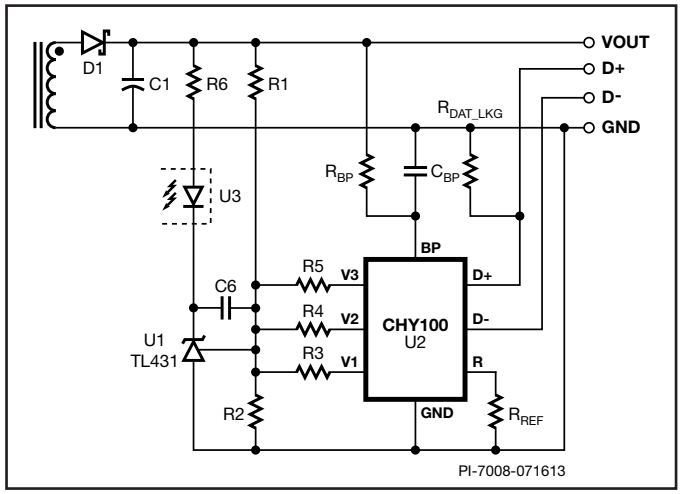


Figure 5. CHY100 with Traditional Output Regulation (CV Only).

CHY100 supports the full output voltage range of Quick Charge 2.0 Class A (5 V, 9 V, or 12 V) or Class B (5 V, 9 V, 12 V, or 20 V). It automatically detects either Quick Charge 2.0 capable powered devices (PD) or legacy PDs compliant with the USB Battery Charging Specification revision 1.2 and only enables output voltage adjustment accordingly.

Shunt Regulator

The internal shunt regulator clamps the BYPASS pin at 6 V when current is provided through an external resistor (R_{BP} in Figure 5). This facilitates powering of CHY100 externally over the wide power supply output voltage range of 5 V to 20 V. Recommended values are R_{BP} = 4.53 kΩ and C_{BP} = 220 nF.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry resets the CHY100 when the BYPASS pin voltage drops below 3.9 V. Once the BYPASS pin voltage drops below 3.9 V it must rise back to 4 V to enable correct operation.

Reference Input

Resister R_{REF} at the REFERENCE pin is connected to an internal band gap reference and provides an accurate reference current for internal timing circuits. The recommended value is R_{REF} = 127 kΩ.

Quick Charge 2.0 Interface

At power-up CHY100 turns on switch N5 (see Figure 3) in 20 ms or less after the BYPASS pin voltage has reached 4 V. Switch N4 and output switches N1 to N3 remain off. This sets the default 5 V output voltage level. With D+ and D- short-circuited the normal handshake between the AC-DC adapter (DCP) and powered devices (PD) as described in the USB Battery Charging Specification 1.2 can commence. After switch N5 has been turned on CHY100 starts monitoring the voltage level at D+. If it continuously stays above $V_{DAT(REF)}$ (typ. 0.325 V) and below $V_{SEL(REF)}$ (typ. 2 V) for at least 1.25 seconds CHY100 will enter Quick Charge 2.0 operation mode. If the voltage at D+ drops any time below 0.325 V CHY100 resets the 1.25 seconds timer and stays in USB Battery Charging Specification 1.2 compatibility mode with a default output voltage of 5 V.

Once CHY100 has entered Quick Charge 2.0 operation mode switch N5 will be turned off. Additionally switch N4 is turned on connecting a 19.53 kΩ pull-down resistor to D-. As soon as the voltage at D- has dropped low (<0.325 V) for at least 1 ms CHY100 starts accepting requests for different AC-DC adapter output voltages by means of applied voltage levels at data lines D+ and D- through the powered device. Table 1 summarizes the output voltage lookup table, corresponding AC-DC adapter output voltages and status of switches N1 to N3.

D+	D-	Output	Switch Status
0.6 V	0.6 V	12 V	N1 = N2 = On, N3 = Off
3.3 V	0.6 V	9 V	N1 = On, N2 = N3 = Off
3.3 V	3.3 V	20 V	N1 = N2 = N3 = On
0.6 V	GND	5 V (default)	N1 = N2 = N3 = Off

Table 1. Output Voltage Lookup Table.

For Quick Charge 2.0 Class A support only, the V3 pin has to be connected to the BYPASS pin (directly or through a resistor up to 100 kΩ). This will inhibit any requests for setting a 20 V output.

At USB cable disconnect the voltage level at D+ is pulled down by resistor $R_{DAT(LKG)}$ (see Figure 5). Once it drops below 0.325 V CHY100 will turn on switch N5 (thereby short-circuiting D+ and D-) and turns off switches N1 to N4. This sets the default output voltage of 5 V. The recommended value for $R_{DAT(LKG)}$ = 390 kΩ.

Absolute Maximum Ratings

BYPASS Pin Voltage ..... -0.3 to 9 V
REFERENCE Pin Voltage ..... -0.3 to 9 V
V1/V2/V3 Pin Voltage ..... -0.3 to 9 V
D+/D- Pin Voltage ..... -0.3 to 5 V
BYPASS Pin Current .....25 mA
V1/V2/V3 Pin Current .....0.5 mA
D+/D- Pin Current ..... 1 mA

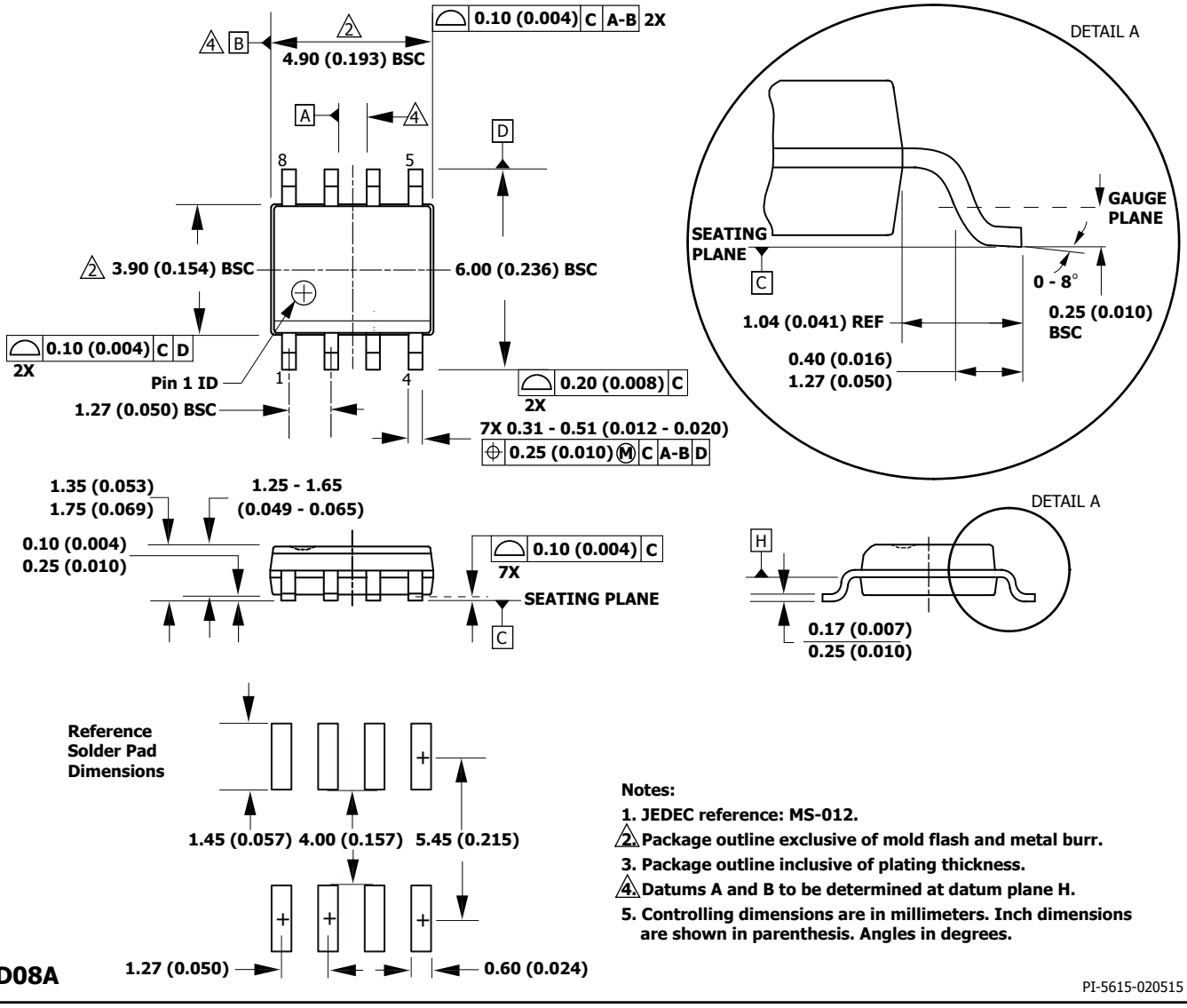
Operating Junction Temperature..... -40 °C to +150 °C
Operating Ambient Temperature.....-40 °C to 105 °C
Storage Temperature .....-65 °C to 150 °C
Lead Temperature(1) .....260 °C

Notes:
1. 1/16 in. from case for 5 seconds.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Supply, Reference and Protection Functions						
BYPASS Pin Voltage	V_{BP}		4	5	6	V
Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$		2.0		3.9	V
BYPASS Pin Source Current	I_{BPSC}	V_{BP} = 4.3 V, T_J = 25 °C N1 = N2 = N3 = Off			135	µA
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 3 mA	5.7	6	6.3	V
REFERENCE Pin Voltage	V_R		1.18	1.23	1.28	V
HVDCP Functions						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	$V_{SEL(REF)}$		1.8	2	2.2	V
12 V / 20 V Output Inhibit Threshold	V_{INH}		V_{BP} -0.6			V
Data Lines Short-Circuit Delay	$T_{DAT(SHORT)}$	V_{OUT} ≥ 0.8 V See Figure 5		10	20	ms
D+ High Glitch Filter Time	$T_{GLITCH(BC)DONE}$		1000	1250	1500	ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)CHANGE}$		20	40	60	ms
D- Pull-Down Resistance	$R_{DM(DWN)}$		14.25	19.53	24.5	kΩ
Switch N1 On-Resistance	$R_{DS(ON)N1}$	I_{N1} = 200 µA			300	Ω
Switch N2 On-Resistance	$R_{DS(ON)N2}$	I_{N2} = 200 µA			300	Ω
Switch N3 On-Resistance	$R_{DS(ON)N3}$	I_{N3} = 200 µA			300	Ω
Switch N4 On-Resistance	$R_{DS(ON)N4}$	I_{N4} = 200 µA			300	Ω
Switch N5 On-Resistance	$R_{DS(ON)N5}$	I_{N5} = 200 µA, $V_{(D+)}$ ≤ 3.6 V		20	40	Ω
Data Line Capacitance	$C_{DCP(PWR)}$	See Note A			1	nF

NOTES:
A. Guaranteed by design. Not tested in production.

SO-8 (D Package)



D08A

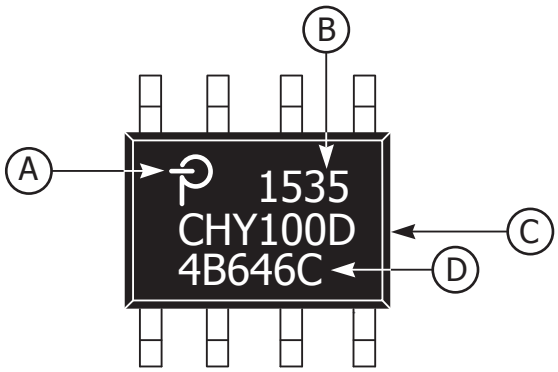
Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

PI-5615-020515

PACKAGE MARKING

SO-8 Package Marking



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-8059-083016

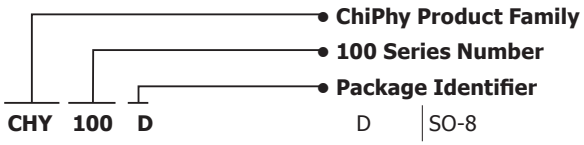
MSL Table

Part Number	MSL Rating
CHY100D	1

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 V (max) on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Machine Model ESD	JESD22-A115C	> ±200 V on all pins

Part Ordering Information



Revision	Notes	Date
A	Initial Release.	07/13
B	Extended Ambient Temperature to -40 °C.	01/14
C	Added Note for Class A Charger on page 3.	03/14
D	Updated with new Brand Style.	06/15
E	Added Package Marking, MSL Table, ESD and Latch-Up Table.	08/16

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