# BQ77216xx Voltage and Temperature Protection for 3-Series to 16-Series Cell Li-Ion Batteries with Internal Delay Timer

## 1 Features

- 3-series cell to 16-series cell protection
- High-accuracy overvoltage protection
  - ± 10mV at 25°C
  - ± 20mV from 0°C to 60°C
- Overvoltage protection options from 3.55V to 5.1V
- Undervoltage protection with options from 1.0V to 3.5V
- Open-wire connection detection
- Overtemperature protection
- Undertemperature protection
- Random cell connection
- Functional safety-capable
- Fixed internal delay timers
- Fixed detections thresholds
- Fixed output drive type for each of COUT and DOUT
  - Active high or active low
  - Active high drive to 6V
  - Open drain with the ability to be pulled up externally to VDD
- Low power consumption $I_{CC}$ ≈ 1µA ($V_{CELL(ALL)}$ < $V_{OV}$)
- Low leakage current per cell input < 100nA with open wire detection disabled
- Package footprint options:
  - Leaded 24-pin TSSOP with 0.65mm lead pitch

## 2 Applications

- Protection for Li-ion battery packs used in:
  - Handheld garden tools
  - Handheld power tools
  - Cordless vacuum cleaners
  - UPS battery backup
  - Light electric vehicles (eBike, eScooter, pedal-assist bicycles)

## 3 Description

The BQ77216xx family of products provides a range of voltage and temperature monitoring, including overvoltage (OVP), undervoltage (UVP), open wire (OW), undertemperature (UT), and overtemperature (OT) protection for Li-ion battery pack systems. Each cell is monitored independently for overvoltage, undervoltage, and open-wire conditions. With the addition of an external NTC thermistor, the device can detect undertemperature and overtemperature conditions.

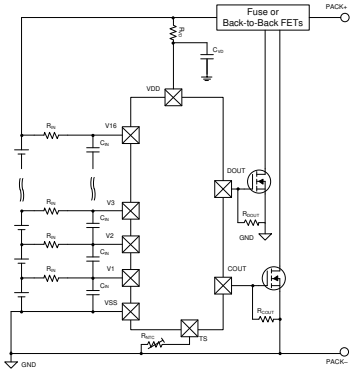
In the BQ77216xx device, an internal delay timer is initiated upon detection of an overvoltage, undervoltage, open-wire,undertemperature, or overtemperature condition. Upon expiration of the delay timer, the respective output is triggered into its active state (either high or low, depending on the configuration).

Overvoltage triggers the COUT pin if a fault is detected, and undervoltage triggers the DOUT pin if a fault is detected. If an overtemperature or open-wire fault is detected, then the DOUT and COUT are triggered. For quicker production-line testing, the BQ77216xx device provides a Customer Test Mode (CTM) with greatly reduced delay time.

**Package Information**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| BQ77216xx (1) | TSSOP (24) | 4.40mm × 7.80mm (6.40mm × 7.80mm, including leads) |

(1) For available packages and preprogrammed device versions, see the orderable addendum at the end of the data sheet and the *Device Comparison Table*.




**Simplified Schematic**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Device Comparison Table

**Table 4-1. BQ77216xx Device Comparison**

| PART NUMBER | $T_A$ | PACKAGE | PACKAGE DESIGNATOR | OVP (V) | OV HYSTERESIS (V) | OVP DELAY | UVP (V) | UVP DELAY |
|---|---|---|---|---|---|---|---|---|
| BQ7721600 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.325 | 0.100 | 1s | 2.25 | 1s |
| BQ7721602 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.325 | 0.100 | 1s | 2.25 | 1s |
| BQ7721603 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.3 | 0.100 | 2s | 2 | 2s |
| BQ7721605 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.225 | 0.100 | 1s | 2.6 | 1s |
| BQ7721606 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.275 | 0.100 | 1s | 2.5 | 1s |
| BQ7721607 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.25 | 0.100 | 4s | 2.5 | 2s |
| BQ7721609 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.35 | 0.200 | 4s | Disabled | |
| BQ7721610 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.25 | 0.100 | 4s | 2.5 | 2s |
| BQ7721611 | –40°C to 110°C | 24-Pin TSSOP | PW | 3.8 | 0.200 | 4s | 1.5 | 1s |
| BQ7721612 | –40°C to 110°C | 24-Pin TSSOP | PW | 3.6 | 0.200 | 2s | 2.0 | 2s |
| BQ7721613 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.25 | 0.100 | 4s | 2.0 | 2s |
| BQ7721614 | –40°C to 110°C | 24-Pin TSSOP | PW | 3.9 | 0.100 | 4s | 1.85 | 2s |
| BQ7721615 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.23 | 0.100 | 4s | 2.0 | 2s |
| BQ7721616 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.18 | 0.100 | 4s | 2.0 | 2s |
| BQ7721617 | –40°C to 110°C | 24-Pin TSSOP | PW | 3.8 | 0.100 | 2s | 1.5 | 2s |
| BQ7721618 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.22 | 0.200 | 4s | 2.2 | 2s |
| BQ7721619 | –40°C to 110°C | 24-Pin TSSOP | PW | 4.22 | 0.200 | 2s | 2.1 | 1s |
| BQ7721620 | –40°C to 110°C | 24-Pin TSSOP | PW | 3.7 | 0.100 | 1s | 1.8 | 2s |
| BQ77216xx (1) | –40°C to 110°C | 24-Pin TSSOP | PW | 3.55 – 5.10 | 0.100, 0.200 | 0.25s, 0.5s, 1s, 2s, 4s | 1.0 – 3.5 | 0.25s, 0.5s, 1s, 2s |

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**Table 4-2. BQ77216xx Device Comparison (continued)**

| PART NUMBER | UV HYSTERESIS (V) | OTC (°C) | UTC (°C) | OW | LATCH | OUTPUT DRIVE | TAPE AND REEL |
|---|---|---|---|---|---|---|---|
| BQ7721600 | 0.100 | 70 | NA | Enabled | Disabled | Active Low | BQ7721600PWR |
| BQ7721602 | 0.100 | 70 | NA | Enabled | Disabled | Active High, 6V Drive | BQ7721602PWR |
| BQ7721603 | 0.100 | 75 | NA | Enabled | Disabled | Active High, 6V Drive | BQ7721603PWR |
| BQ7721605 | 0.200 | 75 | NA | Disabled | Disabled | Active High, 6V Drive | BQ7721605PWR |
| BQ7721606 | 0.200 | 75 | NA | Disabled | Disabled | Active High, 6V Drive | BQ7721606PWR |
| BQ7721607 | 0.100 | 83 | –30 | Enabled | Disabled | Active High, 6V Drive | BQ7721607PWR |
| BQ7721609 | Disabled | 83 | NA | Enabled | Disabled | Active High, 6V Drive | BQ7721609PWR |
| BQ7721610 | 0.100 | 83 | NA | Enabled | Disabled | Active High, 6V Drive (COUT) Active Low (DOUT) | BQ7721610PWR |
| BQ7721611 | 0.200 | 70 | NA | Disabled | Disabled | Active High, 6V Drive | BQ7721611PWR |
| BQ7721612 | 0.200 | 75 | NA | Disabled | Disabled | Active Low | BQ7721612PWR |
| BQ7721613 | 0.200 | 83 | –30 | Enabled | Disabled | Active High, 6V Drive | BQ7721613PWR |
| BQ7721614 | 0.100 | 75 | NA | Enabled | Disabled | Active High, 6V Drive | BQ7721614PWR |
| BQ7721615 | 0.200 | 83 | -20 | Disabled | Disabled | Active High, 6V Drive | BQ7721615PWR |
| BQ7721616 | 0.200 | 80 | -20 | Disabled | Disabled | Active High, 6V Drive | BQ7721616PWR |
| BQ7721617 | 0.200 | NA | NA | Disabled | Disabled | Active High, 6V Drive | BQ7721617PWR |
| BQ7721618 | 0.200 | 83 | -20 | Disabled | Disabled | Active High, 6V Drive | BQ7721618PWR |
| BQ7721619 | 0.200 | 83 | -10 | Disabled | Disabled | Active High, 6V Drive | BQ7721619PWR |
| BQ7721620 | 0.200 | 83 | -10 | Disabled | Disabled | Active High, 6V Drive | BQ7721620PWR |
| BQ77216xx(1) | 0.100, 0.200 | 62, 65, 70, 75, 80, 83, Disabled | -30, -20, -10, 0, Disabled | Enabled, Disabled | Enabled, Disabled | Open Drain Active Low, Active High 6V, Active High VDD | TBD |

(1) Contact TI for more information.


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# 5 Pin Configuration and Functions

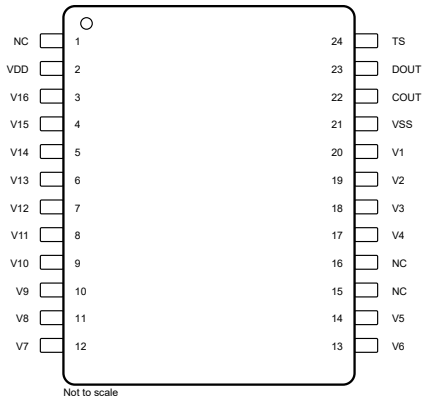


**Table 5-1. 24-Lead Pin Functions**

| NO. | NAME | TYPE | DESCRIPTION (1) |
|---|---|---|---|
| 1 | NC | — | Not electrically connected and can be left floating |
| 2 | VDD | P | Power supply |
| 3 | V16 | I | Sense input for positive voltage of the sixteenth cell from the bottom of the stack |
| 4 | V15 | I | Sense input for positive voltage of the fifteenth cell from the bottom of the stack |
| 5 | V14 | I | Sense input for positive voltage of the fourteenth cell from the bottom of the stack |
| 6 | V13 | I | Sense input for positive voltage of the thirteenth cell from the bottom of the stack |
| 7 | V12 | I | Sense input for positive voltage of the twelfth cell from the bottom of the stack |
| 8 | V11 | I | Sense input for positive voltage of the eleventh cell from the bottom of the stack |
| 9 | V10 | I | Sense input for positive voltage of the tenth cell from the bottom of the stack |
| 10 | V9 | I | Sense input for positive voltage of the ninth cell from the bottom of the stack |
| 11 | V8 | I | Sense input for positive voltage of the eighth cell from the bottom of the stack |
| 12 | V7 | I | Sense input for positive voltage of the seventh cell from the bottom of the stack |
| 13 | V6 | I | Sense input for positive voltage of the sixth cell from the bottom of the stack |
| 14 | V5 | I | Sense input for positive voltage of the fifth cell from the bottom of the stack |
| 15 | NC | — | Not electrically connected and can be left floating |
| 16 | NC | — | Not electrically connected and can be left floating |
| 17 | V4 | I | Sense input for positive voltage of the fourth cell from the bottom of the stack |
| 18 | V3 | I | Sense input for positive voltage of the third cell from the bottom of the stack |
| 19 | V2 | I | Sense input for positive voltage of the second cell from the bottom of the stack |
| 20 | V1 | I | Sense input for positive voltage of the lowest cell in the stack |
| 21 | VSS | P | Electrically connected to IC ground and negative terminal of the lowest cell in the stack |
| 22 | COUT | O | Output drive for overvoltage, open wire, undertemperature, and overtemperature. It can be left floating if not used. |
| 23 | DOUT | O | Output drive for undervoltage, open wire, undertemperature, and overtemperature. It can be left floating if not used. |
| 24 | TS | I | Temperature sensor input. If not used, connect it with a 10kΩ resistor to VSS. |

(1) I = Input, O = Output, P = Power Connection

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range | VDD – VSS | –0.3 | 85 | V |
| Input voltage range | Vn – VSS where n = 1 to 16 | –0.3 | 85 | V |
| | TS | –0.3 | 1.5 | V |
| Output voltage range | COUT – VSS, DOUT – VSS | –0.3 | 85 | V |
| Functional temperature, $T_{FUNC}$ | | –40 | 110 | °C |
| Storage temperature, $T_{STG}$ | | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage (1) | 5 | | 75 | V |
| $V_{IN}$ | Input voltage range of Vn - Vn-1 where n = 2 to 16 and V1 - VSS | 0 | | 5 | V |
| | TS | 0 | | 1.5 | V |
| $V_{CTM}$ | Customer Test Mode Entry $V_{DD}$ > V16 + $V_{CTM}$ | 12 | | 13 | V |
| $C_{TS}$ | Total capacitance on the TS Pin | | | 200 | pF |
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| $T_J$ | Junction temperature | –65 | | 150 | °C |

(1) $V_{DD}$ is equal to top of stack voltage


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## 6.4 Thermal Information

| THERMAL METRIC(1) | | DEVICE PW (TSSOP) 24 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 40.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53.1 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 4.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 52.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | NA | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 6.5 DC Characteristics

Typical values stated where $T_A$ = 25°C and VDD = 58V, MIN/MAX values stated where $T_A$ = –40°C to 85°C and VDD = 5V to 75V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OVER VOLTAGE PROTECTION (OV)** | | | | | | |
| $V_{OV}$ | OV Detection Range | | 3.55 | | 5.1 | V |
| $V_{OV_STEP}$ | OV Detection Steps | | | 25 | | mV |
| $V_{OV_HYS}$ | OV Detection Hysteresis | Selected OV Hysteresis depends on the part number. See the device selection table for details. | | $V_{OV}$ – 100 | | mV |
| | | Selected OV Hysteresis depends on the part number. See the device selection table for details. | | $V_{OV}$ – 200 | | mV |
| $V_{OV_ACC}$ | OV Detection Accuracy | $T_A$ = 25°C | –10 | | 10 | mV |
| | OV Detection Accuracy | 0°C ≤ $T_A$ ≤ 60°C | –20 | | 20 | mV |
| | OV Detection Accuracy | –40°C ≤ $T_A$ ≤ 110°C | –50 | | 50 | mV |
| **UNDER VOLTAGE PROTECTION (UV)** | | | | | | |
| $V_{UV}$ | UV Detection Range | | 1.0 | | 3.5 | V |
| $V_{UV_STEP}$ | UV Detection Steps | | | 50 | | mV |
| $V_{UV_HYS}$ | UV Detection Hysteresis | Selected OV Hysteresis depends on the part number. See the device selection table for details. | | $V_{UV}$ + 100 | | mV |
| | | Selected OV Hysteresis depends on the part number. See the device selection table for details. | | $V_{UV}$ + 200 | | mV |
| $V_{UV_ACC}$ | UV Detection Accuracy | $T_A$ = 25°C | –30 | | 30 | mV |
| | UV Detection Accuracy | –40 ≤ $T_A$ ≤ 110°C | –50 | | 50 | mV |
| $V_{UV_MIN}$ | UV Detection Disabled Threshold | Vn – Vn-1 where n = 2 to 16 and V1 – VSS | 450 | 500 | 550 | mV |
| **OVER TEMPERATURE PROTECTION (OT)** | | | | | | |
| $T_{OT}$ | OT Detection Range | Available options: 62°C, 65°C, 70°C, 75°C, 80°C, 83°C | 62.0 | | 83.0 | °C |

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## 6.5 DC Characteristics (continued)

Typical values stated where $T_A$ = 25°C and VDD = 58V, MIN/MAX values stated where $T_A$ = –40°C to 85°C and VDD = 5V to 75V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{OT_EXT}$ | OT Detection External Resistance | 62°C | | 2850 | | Ω |
| | | 65°C | | 2570 | | |
| | | 70°C | | 2195 | | |
| | | 75°C | | 1915 | | |
| | | 80°C | | 1651 | | |
| | | 83°C | | 1525 | | |
| $T_{OT_ACC}$ (1) | OT Detection Accuracy | | –5 | | 5 | °C |
| $T_{OT_HYS}$ (2) | OT Detection Hysteresis | | | –10 | | °C |
| | | | | 4186 | | Ω |
| | | | | 3530 | | Ω |
| $R_{NTC}$ | Internal Pullup Resistor | After TI Factory Trim | 19.5 | 20 | 20.6 | kΩ |
| **OPEN WIRE PROTECTION (OW)** | | | | | | |
| $V_{OW}$ | OW Detection Threshold | Vn < Vn-1 where n = 2 to 16 | | –200 | | mV |
| | | V1 – VSS | | 500 | | mV |
| $V_{OW_HYS}$ | OW Detection Hysteresis | Vn < Vn-1 where n = 1 to 16 | | $V_{OW}$ +100 | | mV |
| $V_{OW_ACC}$ | OW Detection Accuracy | –40 °C ≤ $T_A$ ≤ 110°C | –25 | | 25 | mV |
| **SUPPLY AND LEAKAGE CURRENT** | | | | | | |
| $I_{CC}$ | Supply Current | No fault detected | | 2 | 3.5 | µA |
| $I_{IN}$ (2) | Input Current at Vx Pins | Vn – Vn-1 and V1 – VSS = 4V, where n = 2 to 16, Open Wire Enabled | –0.3 | | 0.3 | µA |
| | | Vn – Vn-1 and V1 – VSS = 4V, where n = 2 to 16, Open Wire Disabled | –0.1 | | 0.1 | µA |
| **OUTPUT DRIVE, COUT and DOUT, CMOS ACTIVE HIGH VERSIONS ONLY** | | | | | | |
| $V_{OUT_AH}$ | Output Drive Voltage for COUT and DOUT, Active High 6V | Vn – Vn-1 or V1 – VSS > $V_{OV}$, where n = 2 to 16, VDD = 58V, $I_{OH}$ = 100µA measured out of COUT, DOUT pin | 6 | | | V |
| | Output Drive Voltage for COUT and DOUT, Active High VDD | VDD – $V_{COUT}$ or $V_{DOUT}$, Vn – Vn-1 or V1 – VSS > $V_{OV}$, where n = 2 to 16, $I_{OH}$ = 10µA measured out of COUT, DOUT pin | 0 | 1 | 1.5 | V |
| | Output Drive Voltage for COUT and DOUT, Active High 6V | VDD – $V_{COUT}$ or $V_{DOUT}$, if 15 of 16 cells are short-circuited and only one cell remains powered and > $V_{OV}$, VDD = Vx (cell voltage), $I_{OH}$ = 100µA, | 0 | 1 | 1.5 | V |
| | Output Drive Voltage for COUT and DOUT, Active High 6V and VDD | Vn – Vn-1 and V1 – VSS < $V_{OV}$, where n = 2 to 16, VDD = 58V, $I_{OH}$ = 100µA measured into pin | | 250 | 400 | mV |
| $R_{OUT_AH}$ | Internal Pullup Resistor | | 80 | 100 | 120 | kΩ |
| $I_{OUT_AH_H}$ | OUT Source Current (during OV) | Vn – Vn-1 or V1 – VSS > $V_{OV}$, where n = 2 to 16, VDD = 58V, OUT = 0V. Measured out of COUT, DOUT pin | | | 4.5 | mA |
| $I_{OUT_AH_L}$ | OUT Sink Current (no OV) | Vn – Vn-1 and V1 – VSS < $V_{OV}$, where n = 2 to 16, VDD = 58V, OUT = VDD. Measured into COUT, DOUT pin | 0.3 | | 3 | mA |
| **OUTPUT DRIVE, COUT and DOUT, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY** | | | | | | |
| $V_{OUT_AL}$ | Output Drive Voltage for COUT and DOUT, Active Low | Vn – Vn-1 or V1 – VSS > $V_{OV}$, where n = 2 to 16, VDD = 58V, $I_{OH}$ = 100µA measured into COUT, DOUT pin | | 250 | 400 | mV |


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## 6.5 DC Characteristics (continued)

Typical values stated where $T_A$ = 25°C and VDD = 58V, MIN/MAX values stated where $T_A$ = –40°C to 85°C and VDD = 5V to 75V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OUT_AL_L}$ | OUT Source Current (during OV) | Vn – Vn-1 or V1 – VSS > $V_{OV}$, where n = 2 to 16, VDD = 58V, OUT = VDD. Measured into COUT, DOUT pin | 0.3 | | 3 | mA |
| $I_{OUT_AL_H}$ | OUT Sink Current (no OV) | Vn – Vn-1 and V1 – VSS < $V_{OV}$, where n = 2 to 16, VDD = 58V, OUT = VDD. Measured out of COUT, DOUT pin | | | 100 | nA |

(1) Assured by Design. This accuracy assumes the external resistance is within ±2% of the R_OT_EXT values for the corresponding temperature threshold.
(2) Assured by Design

## 6.6 Timing Requirements

Typical values stated where $T_A$ = 25°C and VDD = 58V, MIN/MAX values stated where $T_A$ = –40°C to 85°C and VDD = 5V to 85V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{OV_DELAY}$ | OV Delay Time | | | 0.25 | | s |
| | | | | 0.5 | | s |
| | | | | 1 | | s |
| | | | | 2 | | s |
| | | | | 4 | | s |
| $t_{UV_DELAY}$ | UV Delay Time | | | 0.25 | | s |
| | | | | 0.5 | | s |
| | | | | 1 | | s |
| | | | | 2 | | s |
| $t_{OT_DELAY}$ | OT Delay Time | | | 4 | | s |
| $t_{OW_DELAY}$ | OW Delay Time | | | 4 | | s |
| $t_{DELAY_ACC}$ | Delay Time Accuracy | For 0.25s, 0.5s delays | –128 | | 128 | ms |
| $t_{DELAY_ACC}$ | Delay Time Accuracy | For 1s delays | –150 | | 150 | ms |
| $t_{DELAY_DR}$ | Delay time drift across operating temp | For all delays other than 0.25s, 0.5s, 1s delays | –10% | | 10% | |
| $t_{CTM_DELAY}$ | Fault Detection Delay Time during Customer Test Mode | See Customer Test Mode. | | 50 | | ms |

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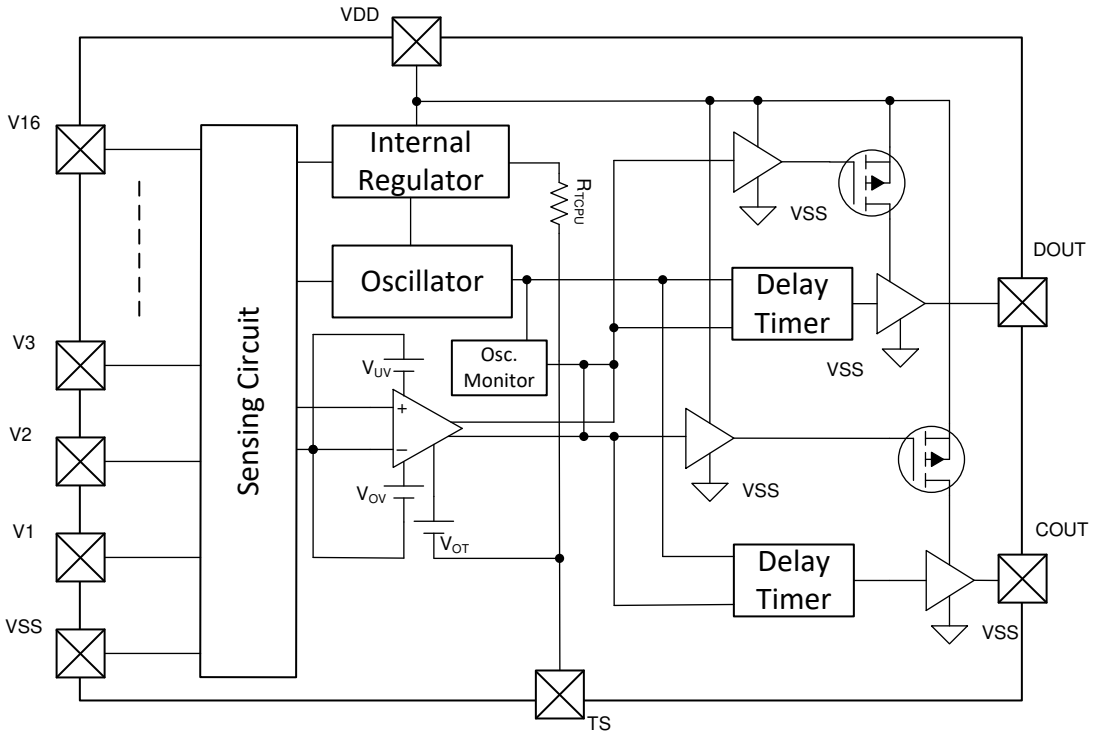
# 7 Detailed Description

## 7.1 Overview

The BQ77216xx family of devices provides a range of voltage and temperature monitoring including overvoltage (OVP), undervoltage (UVP), open wire (OW), and overtemperature (OT) protection for Li-ion battery pack systems. Each cell is monitored independently for overvoltage, undervoltage, and open-wire conditions. With the addition of an external NTC thermistor, the device can detect overtemperature conditions. An internal delay timer is initiated upon detection of an overvoltage, undervoltage, open-wire, or overtemperature condition. Upon expiration of the delay timer, the respective output is triggered into its active state (either high or low, depending on the configuration). The overvoltage triggers the COUT pin if a fault is detected, and undervoltage triggers the DOUT pin if a fault is detected. If an undertemperature, overtemperature, or open-wire fault is detected, then both the DOUT and COUT are triggered.

For quicker production-line testing, the BQ77216xx device provides a Customer Test Mode (CTM) with greatly reduced delay time.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### *7.3.1 Voltage Fault Detection*

In the BQ77216xx device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, $V_{OV}$. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the COUT pin goes from inactive to active state. The timer is reset if the cell voltage falls below the recovery threshold ($V_{OV}$ – $V_{OV_HYS}$). Undervoltage is detected by comparing the actual cell voltage to a protection voltage reference, $V_{UV}$. If any cell voltage falls below the programmed UV value, a timer circuit is activated. When the timer expires, the DOUT pin goes from inactive to active state. The timer is reset if the cell voltage rises below the recovery threshold ($V_{UV}$ + $V_{UV_HYS}$).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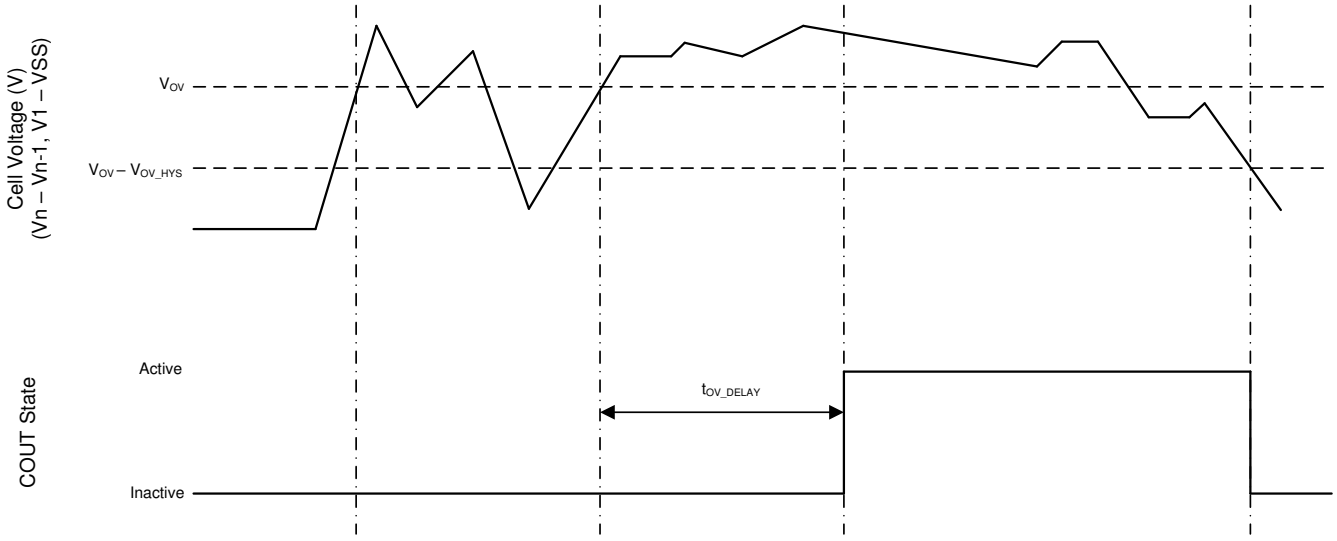


**Figure 7-1. Timing for Overvoltage Sensing**

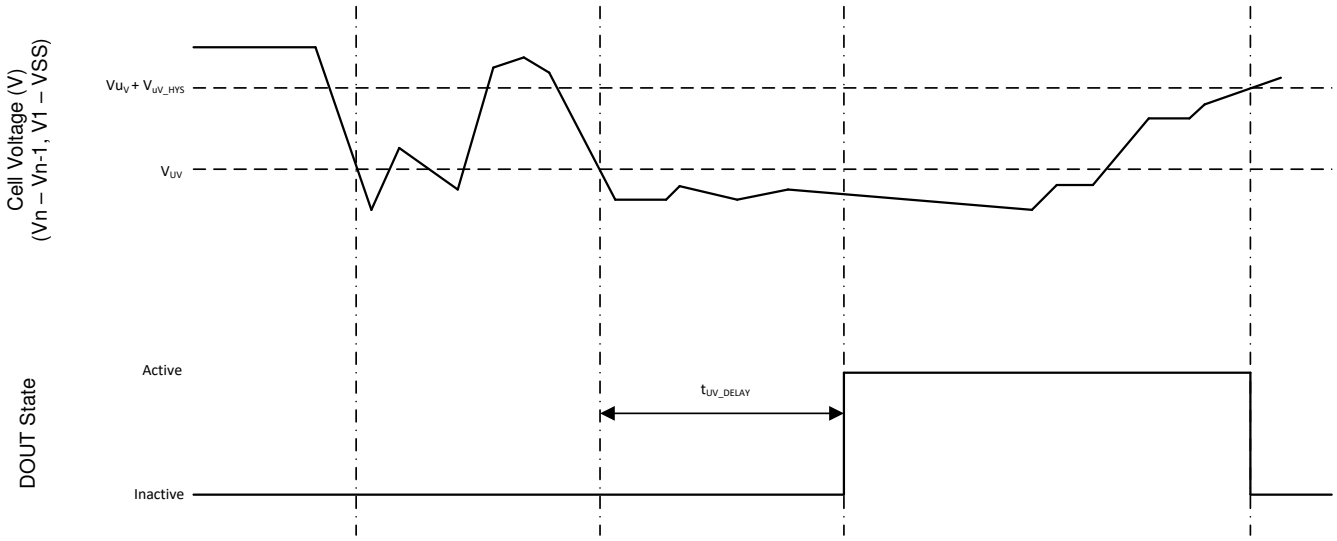


**Figure 7-2. Timing for Undervoltage Sensing**

### *7.3.2 Open-Wire Fault Detection*

In the BQ77216xx device, each cell input is monitored independently to determine if the input is connected to a cell or not by applying a 50µA pull down current to ground that is activated for 128µs every 128ms. If the device detects that Vn < Vn–1 – $V_{OW}$ V, then a timer is activated. When the timer expires, the COUT and DOUT pins go from an inactive to active state. The timer is reset if the cell input rises above or below the recovery threshold ($V_{OW}$ + $V_{OW_HYS}$).

### *7.3.3 Temperature Fault Detection*

In the BQ77216xx device, the TS pin is ratiometrically monitored with an internal pullup resistance $R_{NTC}$. Overtemperature is detected by evaluating the TS input voltage to determine the external resistance falls below a protection resistance, $R_{OT_EXT}$. If the resistance falls below the programmed OT value, a timer circuit is activated. When the timer expires, the COUT and DOUT pins go from inactive to active state. The timer is reset if the resistance rises above the recovery threshold ($R_{OT}$ + $R_{OT_HYS}$). Under temperature is detected by evaluating the TS input voltage to determine the external resistance falls below a protection resistance, $R_{UT_EXT}$. If the resistance rises above the programmed UT value, a timer circuit is activated. When the timer expires, the

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COUT and DOUT pins go from inactive to active state. The timer is reset if the resistance falls below above the recovery threshold ($R_{OT}$ – $R_{OT_HYS}$) If external capacitance is added to the TS pin, it needs to be within the spec limit shown in recommended operating conditions.

**Note**

Texas Instruments does not recommend adding an external capacitor to the TS pin. The capacitance on this pin will affect the TS measurement accuracy if greater than $C_{TS}$.

#### *7.3.4 Oscillator Health Check*

The device can detect if the internal oscillator slows down below the $f_{OSC_FAULT}$ threshold. When this occurs then the COUT and DOUT go from inactive to active state. If the oscillator returns to normal then the fault recovers.

#### *7.3.5 Sense Positive Input for Vx*

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input are required for noise filtering and stable voltage monitoring.

#### *7.3.6 Output Drive, COUT and DOUT*

These pins serve as the fault signal outputs and may be ordered in either active HIGH with drive to 6V or active LOW options configured through internal OTP.

The COUT and DOUT respond per the following table when a fault is detected if the specific fault is enabled.

**Table 7-1. Fault Detection vs COUT and DOUT Action**

| FAULT Detected | COUT | DOUT |
|---|---|---|
| Overvoltage | Active | Inactive |
| Undervoltage | Inactive | Active |
| Open Wire | Active | Active |
| Overtemperature | Active | Active |
| Oscillator Health | Active | Active |

#### *7.3.7 The LATCH Function*

The device can be enabled to latch the fault signal, which effectively disables the recovery functions of all fault detections. The only way to recover from a fault state when the latch is enabled is a POR of the device.

#### *7.3.8 Supply Input, VDD*

This pin is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

### 7.4 Device Functional Modes

#### *7.4.1 NORMAL Mode*

When COUT and DOUT are inactive (no fault detected), the device operates in NORMAL mode and monitors for voltage, open-wire, and temperature faults.

The COUT and DOUT pins are inactive and if configured:

- Active high is low.
- Active low is being externally pulled up and is an open drain.

#### *7.4.2 FAULT Mode*

FAULT mode is entered if the COUT or DOUT pins are activated. The OUT pin is either pulled high internally if configured as active high or is pulled low internally if configured as active low. When COUT and DOUT are deactivated, the device returns to NORMAL mode.


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### 7.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least $V_{CTM}$ higher than V16 (see Figure 7-3). The delay timer is greater than 10ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to a V16 voltage differential of 10V so that the decrease in this value automatically causes an exit.

**CAUTION**

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (VCn–VCn-1) and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 7-3 shows the timing for the Customer Test Mode.

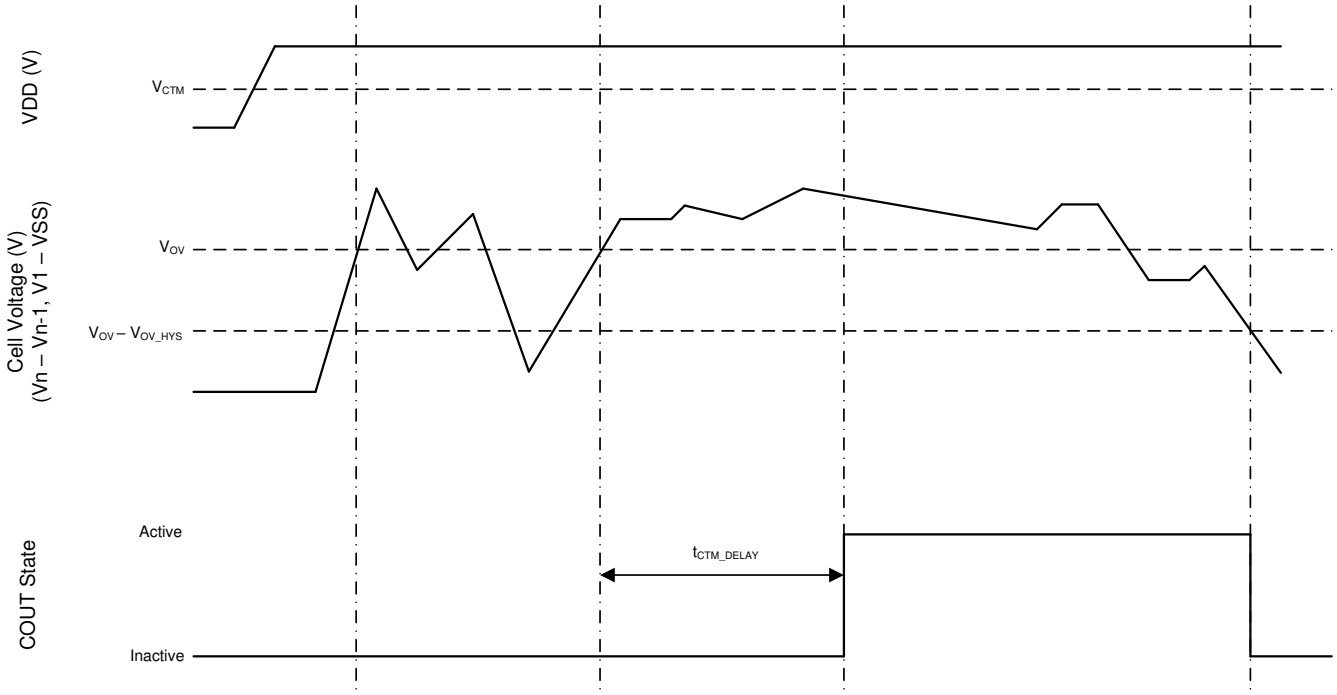


**Figure 7-3. Timing for Customer Test Mode**

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

Changes to the ranges stated in Table 8-1 will impact the accuracy of the cell measurements.

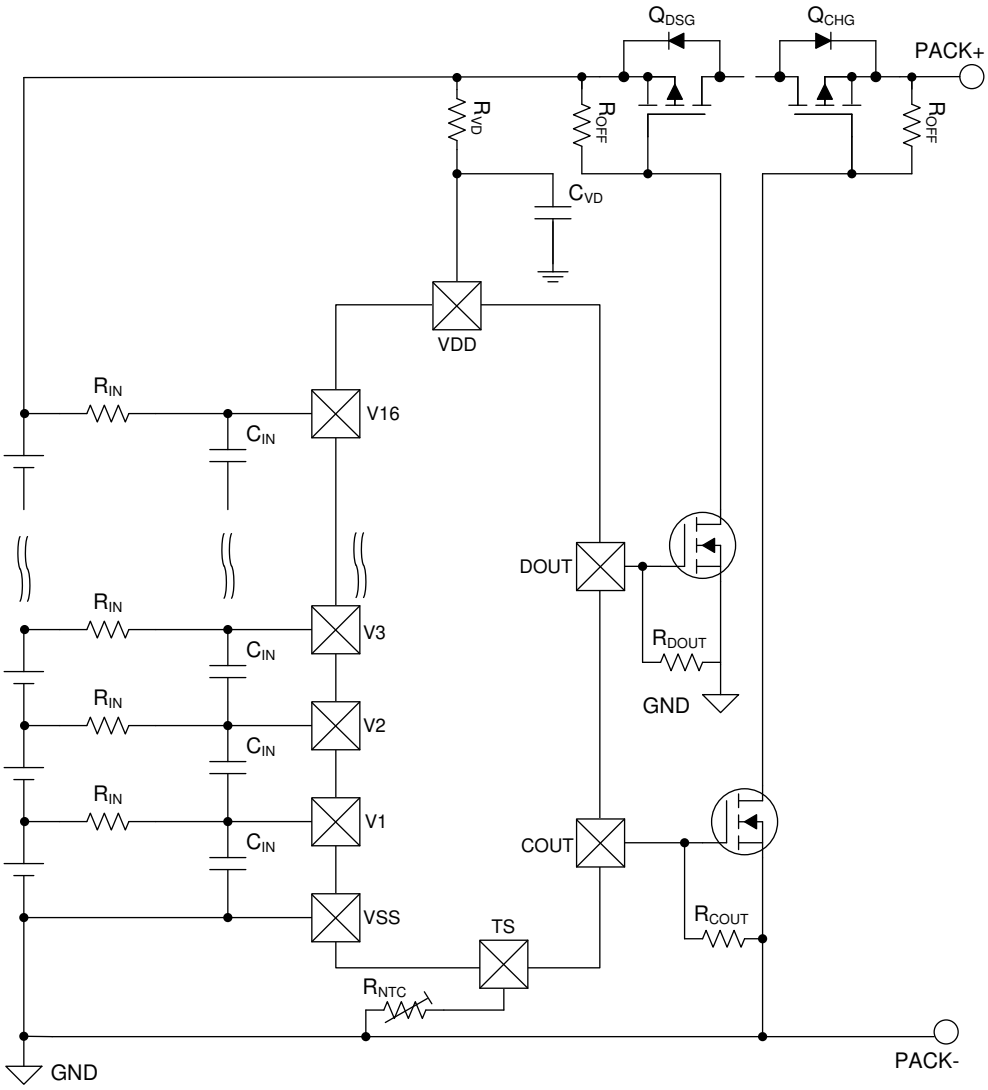


**Figure 8-1. Application Configuration**

### *8.1.1 Design Requirements*

Changes to the ranges stated in Table 8-1 will impact the accuracy of the cell measurements. Figure 8-1 shows each external component.


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**Table 8-1. Parameters**

| PARAMETER | EXTERNAL COMPONENT | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage monitor filter resistance | $R_{IN}$ | 900 | 1000 | 1100 | Ω |
| Voltage monitor filter capacitance | $C_{IN}$ | 0.01 | | 0.1 | µF |
| Supply voltage filter resistance | $R_{VD}$ | 100 | 300 | 1K | Ω |
| Supply voltage filter capacitance | $C_{VD}$ | 0.05 | 0.1 | 1 | µF |

**Note**

The device is calibrated using an $R_{IN}$ value = 1kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and $V_{OV}$ trigger level.

### *8.1.2 Detailed Design Procedure*

Figure 8-2 shows the measurement for current consumption for the product for both VDD and Vx.

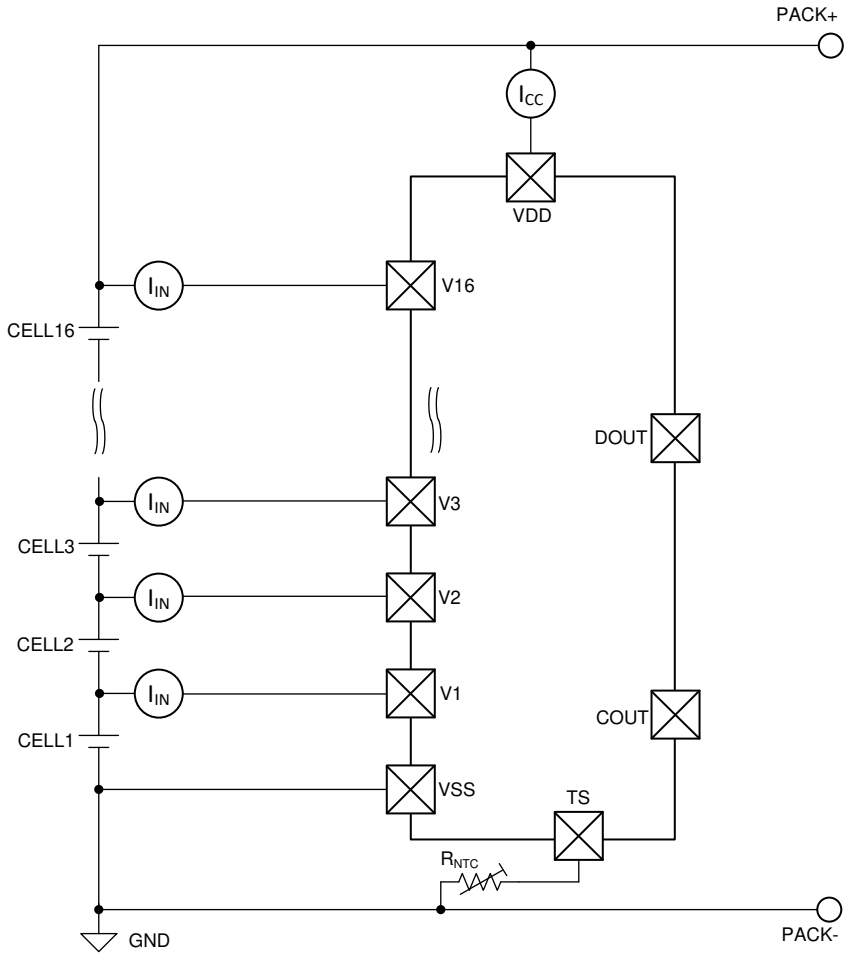


**Figure 8-2. Configuration for IC Current Consumption Test**

#### 8.1.2.1 Cell Connection Sequence

The BQ77216xx device can be connected to the array of cells in any order without damaging the device.

During cell attachment, the device could detect a fault if the cells are not connected within a fault detection delay period. If this occurs, then COUT and/or DOUT could transition from inactive to active. Both COUT and DOUT can be tied to VSS or VDD to prevent any change in output state during cell attach.

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## 8.2 Systems Example

In this application example, the choice of a FUSE or FETs is required on the COUT and DOUT pins—configured as an active-high drive to 6V outputs.

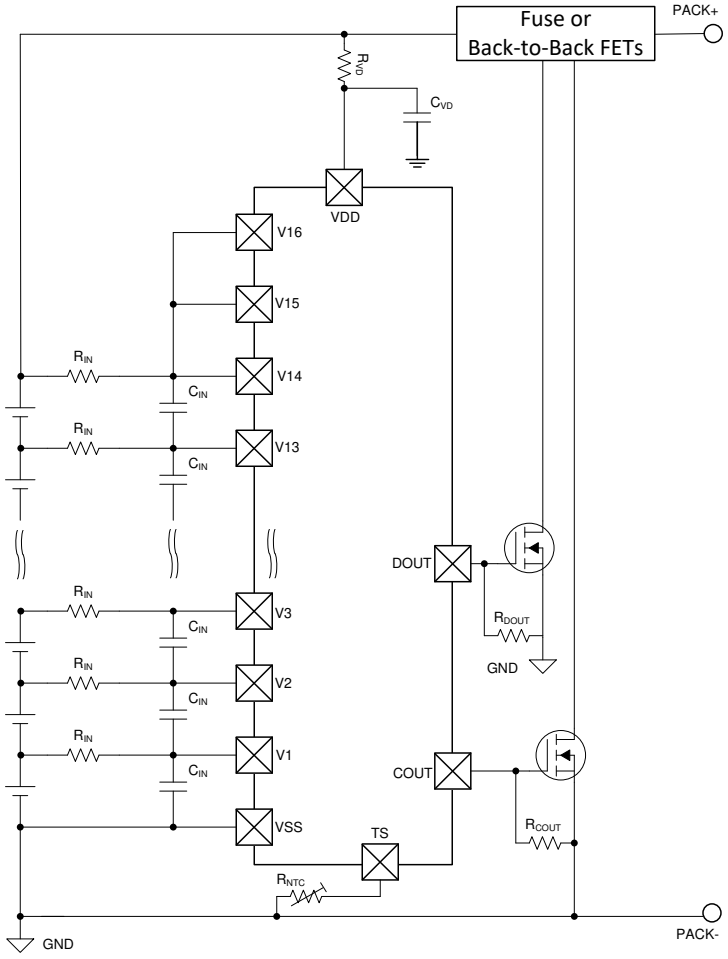


**Figure 8-3. 14-Series Cell Configuration with Active High 6V Option**

When pairing with the BQ769x2 or BQ76940 devices, the top cell must be used. For the BQ77216xx device to drive the CHG and DSG FETs, the active high 6V option is preferred. Its COUT and DOUT are controlling two N-CH FETs to jointly control the CHG and DSG FETs with the monitoring device. For such joint architecture, the open-wire feature of the BQ77216xx device may be affected if the primary protector or monitor device is actively measuring the cells. Care is needed to ensure the $V_{OW}$ spec of the BQ77216xx device is met or to choose a version of the BQ77216xx device with open wire disabled. When working with a BQ769x2 device, set the LOOP_SLOW to 0x11 to ensure the BQ77216xx $V_{OW}$ spec is met.


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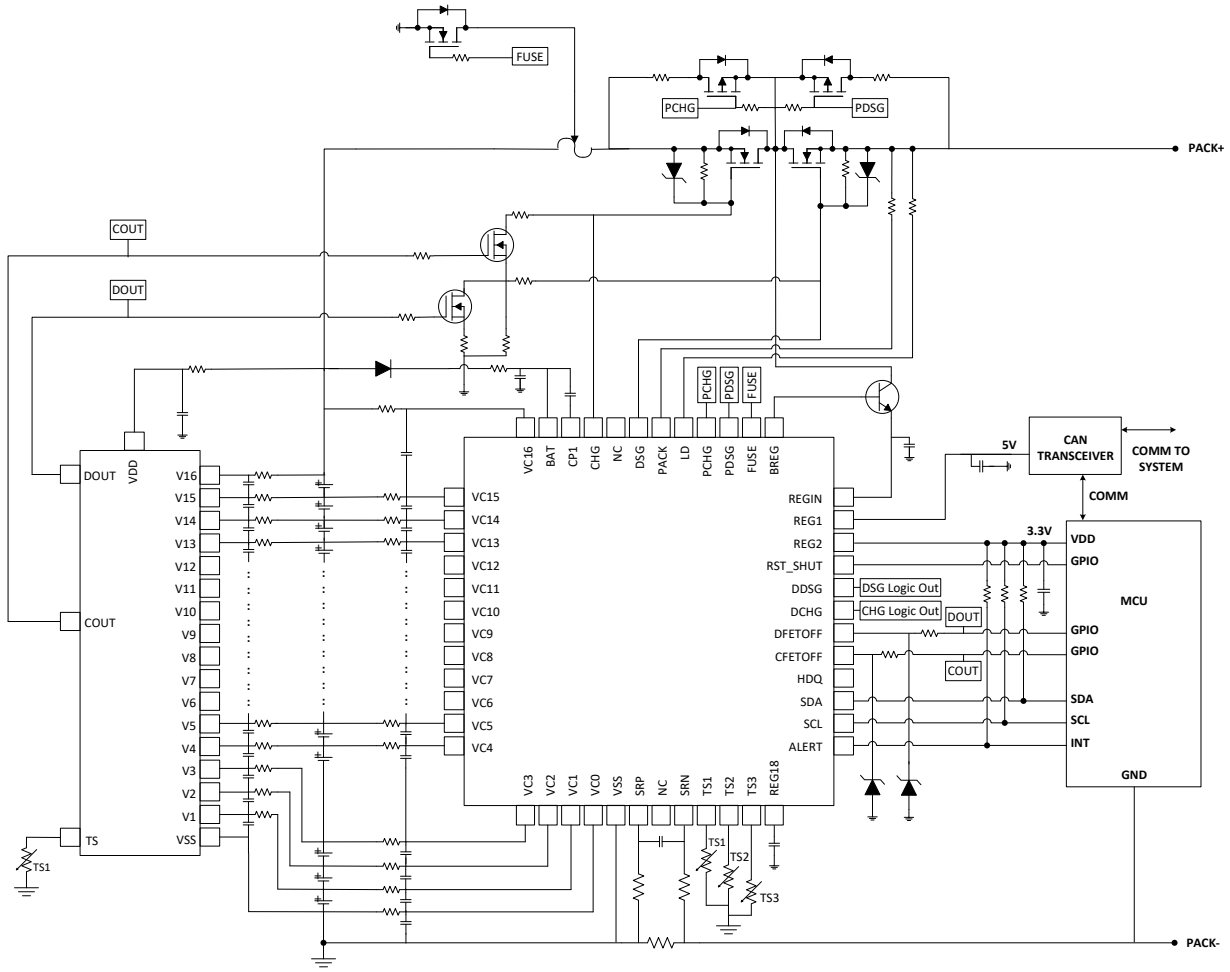


**Figure 8-4. BQ77216 with BQ76952**

## 9 Power Supply Recommendations

The maximum power supply of this device is 85V on VDD.

# 10 Layout

## 10.1 Layout Guidelines

- Ensure the RC filters for the Vn and VDD pins are placed as close as possible to the target terminal.
- The VSS pin should be routed to the CELL– terminal.

## 10.2 Layout Example

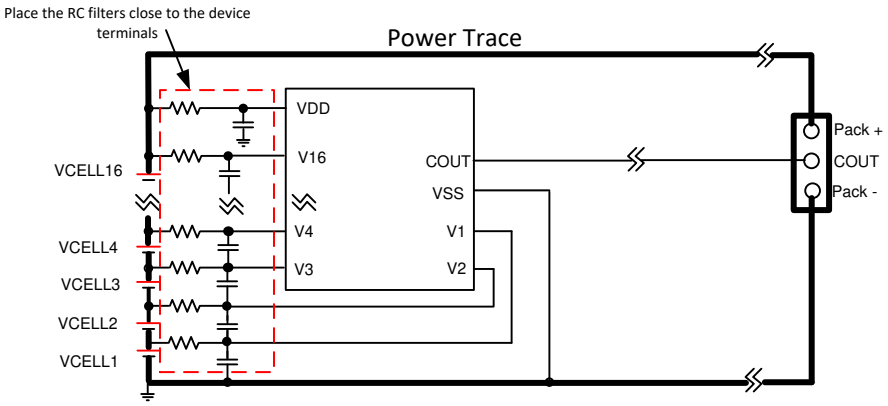


**Figure 10-1. Example Layout**


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# 11 Device and Documentation Support

## 11.1 Third-Party Products Disclaimer

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## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision K (April 2025) to Revision L (September 2025) | Page |
|---|---|
| • Added BQ7721619 to the *Device Comparison Table* | 3 |

| Changes from Revision J (November 2023) to Revision K (April 2025) | Page |
|---|---|
| • Updated the *Features* | 1 |
| • Updated the *Description* | 1 |
| • Updated the *Device Comparison Table* | 3 |

| Changes from Revision I (July 2023) to Revision J (November 2023) | Page |
|---|---|
| • Updated the *Device Comparison Table* | 3 |
| • Updated the TS pin description | 5 |
| • Added the undertemperature protection description | 11 |

| Changes from Revision H (March 2023) to Revision I (July 2023) | Page |
|---|---|
| • Updated the *Device Comparison Table* | 3 |

| Changes from Revision G (July 2022) to Revision H (March 2023) | Page |
|---|---|
| • Updated the *Device Comparison Table* | 3 |

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| BQ7721600PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ7721600 |
| BQ7721600PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ7721600 |
| BQ7721602PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ7721602 |
| BQ7721602PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ7721602 |
| BQ7721603PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ7721603 |
| BQ7721603PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ7721603 |
| BQ7721605PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721605 |
| BQ7721605PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721605 |
| BQ7721606PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721606 |
| BQ7721606PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721606 |
| BQ7721607PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721607 |
| BQ7721607PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721607 |
| BQ7721609PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721609 |
| BQ7721609PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721609 |
| BQ7721610PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721610 |
| BQ7721610PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721610 |
| BQ7721611PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721611 |
| BQ7721611PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721611 |
| BQ7721612PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721612 |
| BQ7721612PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721612 |
| BQ7721613PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721613 |
| BQ7721613PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721613 |
| BQ7721614PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721614 |
| BQ7721614PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721614 |
| BQ7721615PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721615 |
| BQ7721615PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721615 |
| BQ7721616PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721616 |
| BQ7721616PWR.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721616 |
| BQ7721617PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721617 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| BQ7721618PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721618 |
| BQ7721619PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721619 |
| BQ7721620PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 110 | BQ7721620 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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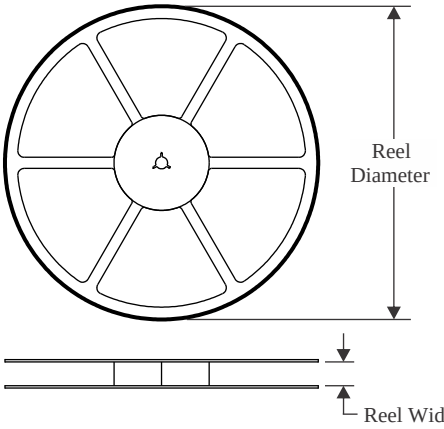
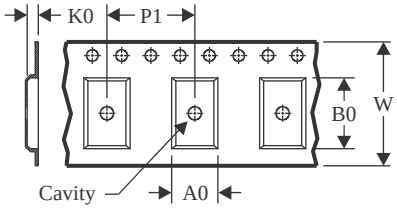
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

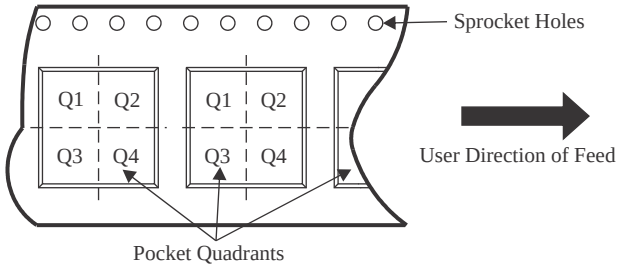



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

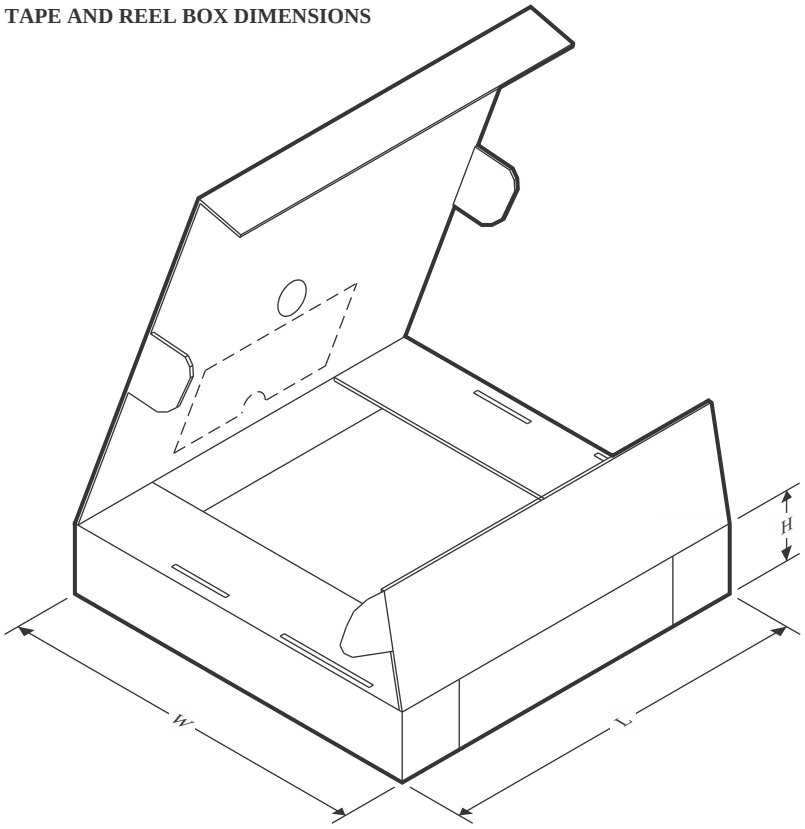



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ7721600PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721602PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721603PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721605PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721606PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721607PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721609PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721610PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721611PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721612PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721613PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721614PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721615PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721616PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721617PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721618PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ7721619PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| BQ7721620PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

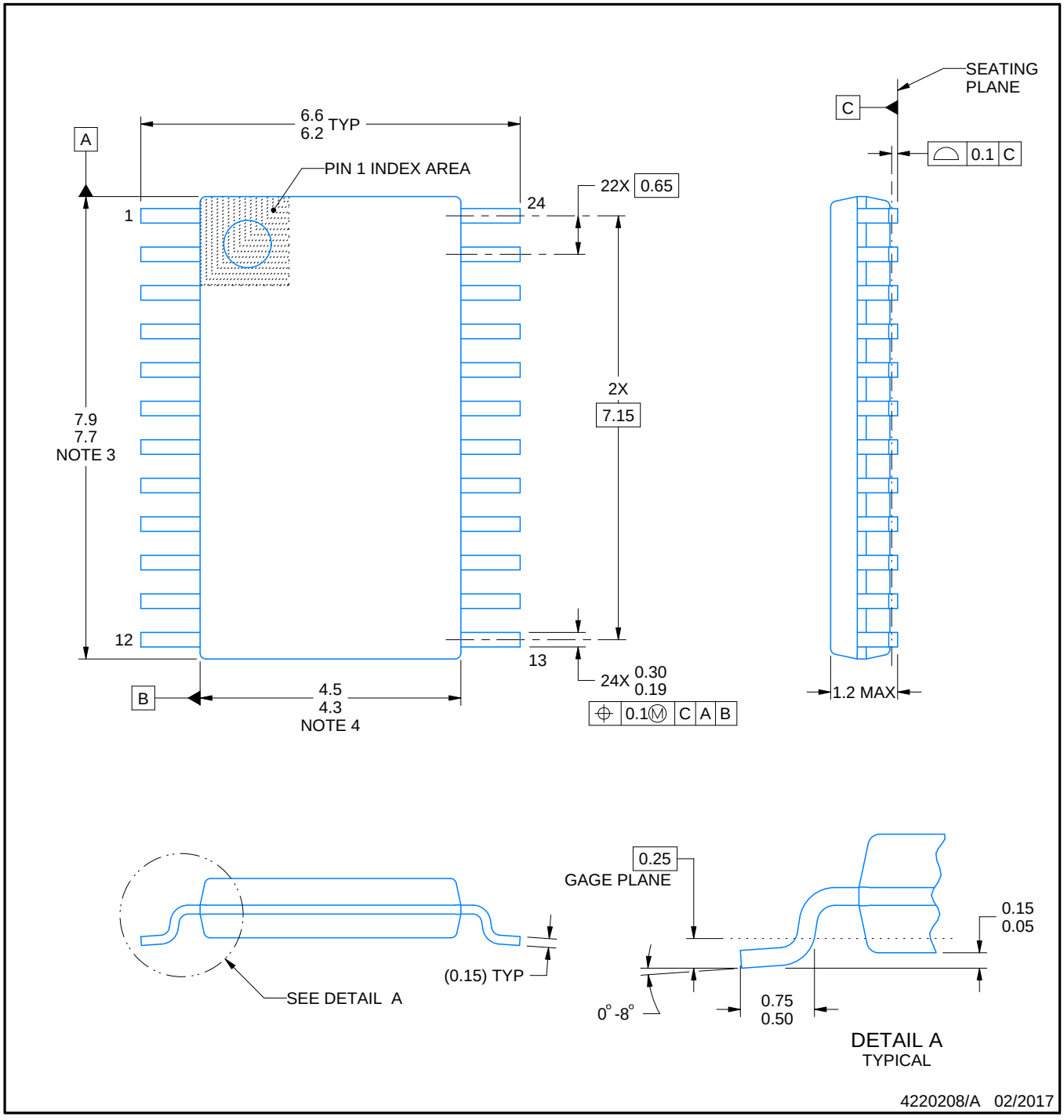
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ7721600PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721602PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721603PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721605PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721606PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721607PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721609PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721610PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721611PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721612PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721613PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721614PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721615PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721616PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721617PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721618PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721619PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |
| BQ7721620PWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## PW0024A

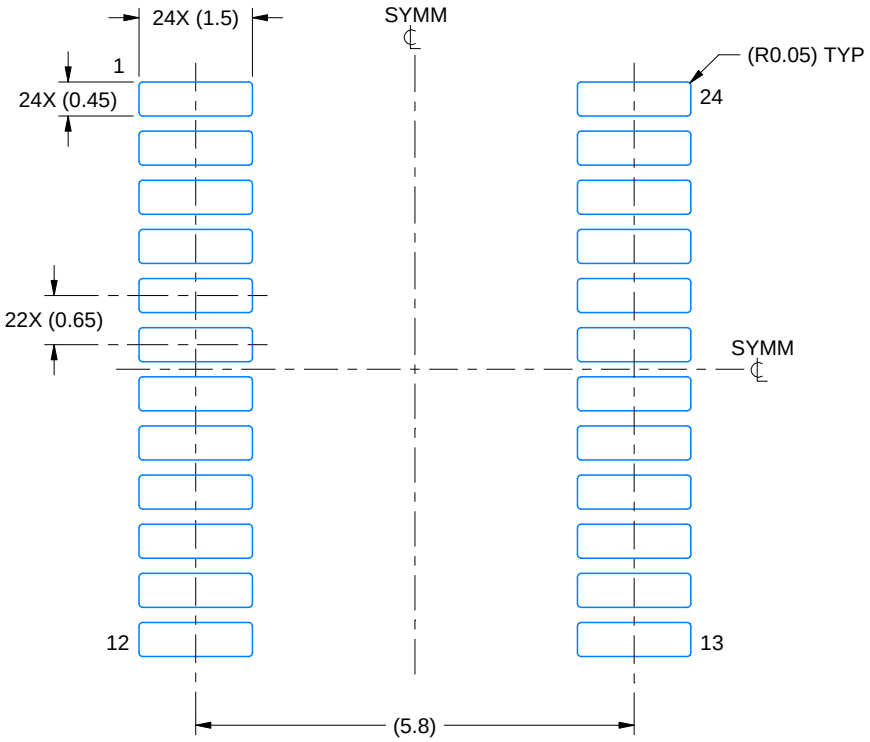
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

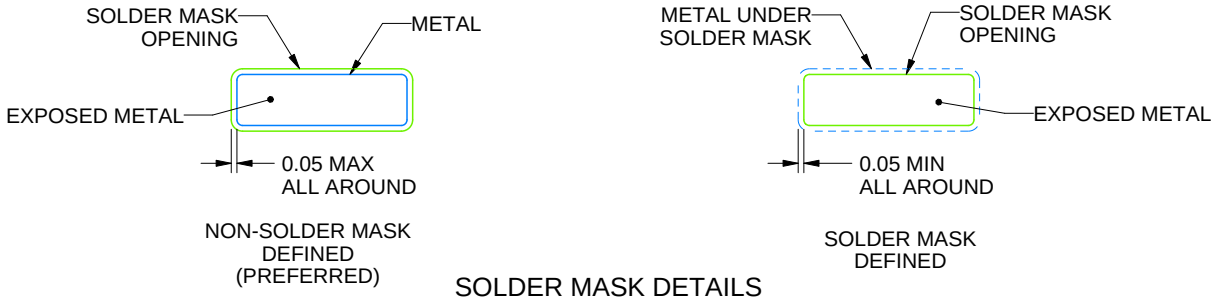



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

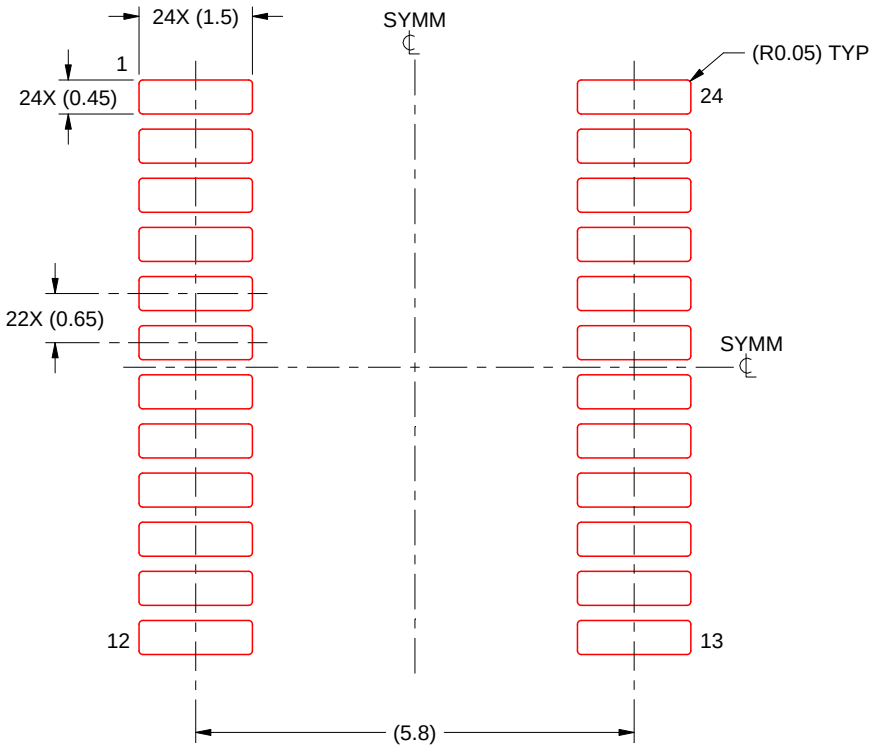



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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