BQ25960H I²C Controlled, Single Cell 8-A Switched Cap Parallel Battery Charger with Integrated Bypass Mode and Dual-Input Selector

1 Features

- 98.1% peak efficiency switched cap parallel charger supporting 8-A fast charge
- Patent pending dual phase switched cap architecture optimized for highest efficiency
  - Input voltage is 2x battery voltage
  - Output current is 2x of input current
  - Reduces power loss across input cable
- Integrated 5-A Bypass Mode fast charge
  - 21-mΩ R_{dson} charging path resistance to support 5-A input and 5-A output charging current
- Dual-input power mux controller for source selection during fast charging and USB On-The-Go (OTG)/ reverse TX Mode
- Provide gate drive signal for external OVP GaN FETs and OVP N-FETs
- Support minimum 1.2V I2C pullup
- Support wide range of input voltage
  - Up to 12.75-V operational input voltage
  - Maximum 40-V input voltage with optional external ACFET and 20-V without external ACFET
- Parallel charging with synchronized dual BQ25960H operations for up to 13-A charging current
- Integrated programmable protection features for safe operation
  - Input overvoltage protection (BUSOVP) and battery overvoltage protection (BATOVP)
  - Input overcurrent protection (BUSOCP) and battery overcurrent protection (BATOCP)
  - Output overvoltage protection (VOUTOVP)
  - Input undercurrent protection (BUSUCP) and input reverse-current protection (BUSRCP) to detect adapter unplug and prevent boost-back
  - Battery and connector temperature monitoring (TSBAT_FLT and TSBUS_FLT)
  - Junction overtemperature protection (TDIE_FLT)
- Programmable settings for system optimization
  - Interrupts and interrupt masks
  - ADC readings and configuration
  - Alarm functions for host control
- Integrated 16-bit ADC for voltage, current, and temperature monitoring

2 Applications

- Smartphone
- Tablet

3 Description

The BQ25960H is a 98.1% peak efficiency, 8-A battery charging solution using switch capacitor architecture for 1-cell Li-ion battery. The switched cap architecture allows the cable current to be half the charging current, reducing the cable power loss, and limiting temperature rise. The dual-phase architecture increases charging efficiency and reduces the input and output cap requirements. When used with a main charger such as BQ2561x or BQ2589x, the system enables full charging cycle from trickle charge to termination with low power loss at Constant Current (CC) and Constant Voltage (CV) Mode.

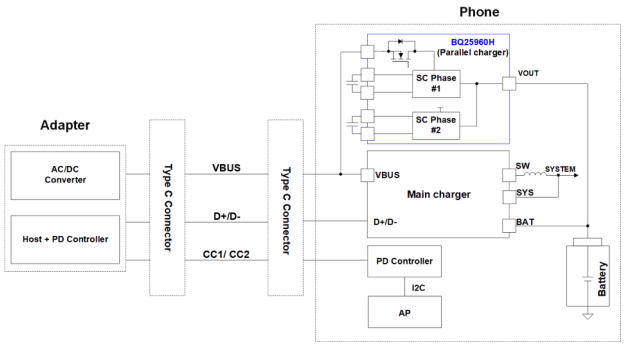
The BQ25960H supports 5-A Bypass Mode charge (previously called battery switch charge) through internal MOSFETs. The R_{dson} in Bypass Mode charging path is 21 mΩ for high-current operation. The integrated Bypass Mode allows backward compatibility of 5-V fast charging adapter to charge 1-cell battery.

The device supports dual input configuration through integrated mux control and driver for external N-FETs. It also allows single input with no external N-FET or single N-FET.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
BQ25960H	DSBGA (36)	2.55 mm x 2.55 mm

(1) For all available packages, see Section 14.



Simplified Schematic

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Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Description (continued)....3
5 Device Comparison Table....4
6 Pin Configuration and Functions....5
7 Specifications....7
7.1 Absolute Maximum Ratings....7
7.2 ESD Ratings....7
7.3 Recommended Operating Conditions....7
7.4 Thermal Information....8
7.5 Electrical Characteristics....8
7.6 Timing Requirements....12
7.7 Typical Characteristics....13
8 Detailed Description....15
8.1 Overview....15
8.2 Functional Block Diagram....16
8.3 Feature Description....17
8.4 Programming....30
8.5 Register Maps....33
9 Application and Implementation....63
9.1 Application Information....63
9.2 Typical Application....63
10 Power Supply Recommendations....69
11 Layout....70
11.1 Layout Guidelines....70
11.2 Layout Example....70
12 Device and Documentation Support....71
12.1 Device Support....71
12.2 Documentation Support....71
12.3 Receiving Notification of Documentation Updates....71
12.4 Support Resources....71
12.5 Trademarks....71
12.6 Electrostatic Discharge Caution....71
12.7 Glossary....71
13 Revision History....71
14 Mechanical, Packaging, and Orderable Information....72
14.1 Package Option Addendum....73
14.2 Tape and Reel Information....74
14.3 Mechanical Data....76

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4 Description (continued)

The device integrates all the necessary protection features to support safe charging, including input overvoltage and overcurrent protection, output overvoltage and overcurrent protection, input undercurrent and reverse-current protection, temperature sensing for the battery and cable, and junction overtemperature protection in both Switched Cap and Bypass Mode.

The device includes a 16-bit analog-to-digital converter (ADC) to provide VAC voltage, bus voltage, bus current, output voltage, battery voltage, battery current, input connector temperature, battery temperature, junction temperature, and other calculated measurements needed to manage the charging of the battery from the adapter, or wireless input, or power bank.

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5 Device Comparison Table

FUNCTION	BQ25960	BQ25960H
Package	YBG-36	YBG-36
Die size	6.5 mm^2	6.5 mm^2
Battery	1 cell	1 cell
Input MUX control	Dual input power MUX control	Dual input power MUX control
Bypass Mode	Yes	Yes
Minimum I2C voltage	1.8 V	1.2 V
GaN FET Support	No	Yes
Recommended charging current	8 A	8 A
Default VAC2OVP	6.5 V	14 V

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6 Pin Configuration and Functions

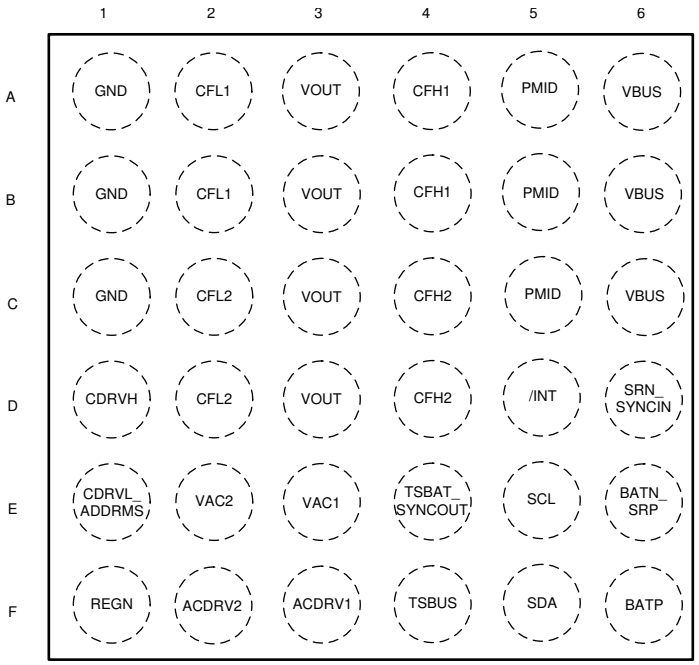

Figure 6-1. YBG Package - BQ25960H 36-Pin DSBGA Top View

Table 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
F3	ACDRV1	P	**Input FETs Driver Pin 1 -** The charge pump output to drive the port #1 input N-channel MOSFET (ACFET1) and the reverse blocking N-channel MOSFET (RBFET1). ACDRV1 voltage becomes 5 V above the common drain connection of the ACFET1 and RBFET1, when the turn-on condition is met. If ACFET1 and RBFET1 are not used, connect ACDRV1 to ground.
F2	ACDRV2	P	**Input FETs Driver Pin 2 -**The charge pump output to drive the port #2 input N-channel MOSFET (ACFET2) and the reverse blocking N-channel MOSFET (RBFET2). ACDRV2 voltage becomes 5 V above the common drain connection of the ACFET2 and RBFET2, when the turn-on condition is met. If ACFET2 and RBFET2 are not used, connect ACDRV2 to ground.
E6	BATN_SRP	AI	**Negative input for battery voltage sensing and positive input for battery current sensing-** Connect to negative terminal of battery pack. It is also used for battery current sensing. Place RSNS (2 mΩ or 5 mΩ) between BATN_SRP and SRN_SYNCIN. Short BATN_SRP to SRN_SYNCIN together and place 100-Ω series resistance between pin and negative terminal if RSNS is not being used.
F6	BATP	AI	**Positive input for battery voltage sensing** - Connect to positive terminal of battery pack. Place 100-Ω series resistance between pin and positive terminal.
D1	CDRVH	AIO	**Charge pump for gate drive** - Connect a 0.22-µF cap between CDRVH and CDRVL_ADDRMS.
E1	CDRVL_ADDRMS	AIO	**Charge pump for gate drive -** Connect a 0.22-µF cap between CDRVH and CDRVL_ADDRMS. During Power ON Reset (POR), this pin is used to assign the address of the device and the mode of the device as Standalone, Primary, or Secondary.
A4, B4	CFH1	P	**Switched cap flying cap connection -**Connect 1 to 3 22-µF caps in parallel between this pin and CFL1.
C4, D4	CFH2	P	**Switched cap flying cap connection** -Connect 1 to 3 22-µF caps in parallel between this pin and CFL2.
A2, B2	CFL1	P	**Switched cap flying cap connection** -Connect 1 to 3 22-µF caps in parallel between this pin and CFH1.

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Table 6-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
C2, D2	CFL2	P	**Switched cap flying cap connection** -Connect 1 to 3 22-µF caps in parallel between this pin and CFH2.
D5	$\overline{INT}$	DO	**Open drain, active low interrupt output** - Pull up to voltage with 10-kΩ resistor. Normally high, the device asserts low to report status and faults. $\overline{INT}$ is pulsed low for t_{INT}.
A1, B1, C1	GND	P	**Ground return**
A5, B5, C5	PMID	P	**Input to the switched cap power stage** -Connect 10-µF cap to PMID.
F1	REGN	AO	**Charger internal LDO output** - Connect a 4.7-µF cap between this pin and GND. When in Primary/Secondary Mode, connect through 1-kΩ resistor to the TSBAT_SYNCOUT and SRN_SYNCIN pins. Do not use REGN for any other function.
E5	SCL	DI	**I^2C interface clock** - Pull up to 3.3 V with 10-kΩ resistor.
F5	SDA	DIO	**I^2C interface data** - Pull up to 3.3 V with 10-kΩ resistor.
D6	SRN_SYNCIN	AI	**Negative input for battery current sensing** - Place RSNS (2 mΩ or 5 mΩ) between SRN_SYNCIN and SRP. Short to SRP and SRN_SYNCIN together if not used. If configured as a secondary for dual charger configuration, this pin functions as SYNCIN, and connect to TSBAT_SYNCOUT of Primary, and connect a 1-kΩ pullup resistor to REGN.
E4	TSBAT_SYNCOUT	AI	**Battery temperature voltage input and Primary Mode SYNCOUT** - Requires external resistor divider, NTC, and voltage reference. See the TSBAT section for choosing the resister divider values. If the device is in Primary Mode, connect this pin to SRN_SYNCIN of the Secondary device.
F4	TSBUS	AI	**BUS temperature voltage input** - Requires external resistor divider, NTC, and voltage reference. See the TSBUS section for choosing the resister divider values.
A6, B6, C6	VBUS	P	**Device power input** - Connect 1-µF capacitor from VBUS to GND.
A3, B3, C3, D3	VOUT	P	**Device power output** - Connect 22-µF capacitor from VOUT to GND.
E3	VAC1	AI	**VAC1 input detection** - Connected to VBUS if ACFET1 and RBFET1 are not used.
E2	VAC2	AI	**VAC2 input detection** - Connected to VBUS if ACFET2 and RBFET2 are not used.

(1) Type: P = Power , AIO = Analog Input/Output , AI = Analog Input, DO = Digital Output, AO = Analog Output, DIO = Digital Input/Output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VAC1, VAC2 (converter not switching)	–2	40	V
	VBUS (converter not switching)	–2	20	V
	PMID (converter not switching)	–0.3	20	V
	ACDRV1, ACDRV2	–0.3	30	V
	CFL1, CFL2	–0.3	7	V
	CFH1 to VOUT, CFH2 to VOUT	–0.3	7	V
	VOUT	–0.3	7	V
	BATP, BATN_SRP	–0.3	6	V
	$\overline{INT}$, SDA, SCL, CDRVL_ADDRMS, SRN_SYNCIN, TSBAT_SYNCOUT, TSBUS	–0.3	6	V
	CDRVH	–0.3	20	V
Output Sink Current	$\overline{INT}$		6	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VAC1, VAC2	Input voltage at VAC1 and VAC2			12	V
VBUS	Input voltage at VBUS			12	V
PMID	Input voltage at PMID			12	V
PMID-CFH1, PMID-CFH2	Voltage across QCH1, QCH2			6	V
CFH1-VOUT, CFH2-VOUT	Voltage across QDH1, QDH2			6	V
VOUT-CFL1, VOUT-CFL2	Voltage across QCL1, QCL2			6	V
CFL1, CFL2	Voltage across QDL1, QDL2			6	V
ICHG	Charging current			8	A
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		120	°C
C_{CFLY}	Effective CFLY capacitance	6.6	20		µF
C_{VBUS}	Effective VBUS capacitance	0.2	1		µF
C_{PMID}	Effective PMID capacitance	2	10		µF

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7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{OUT}	Effective VOUT capacitance	2	10		µF
C_{REGN}	Effective REGN capacitance	1	4.7		µF
C_{DRV}	Effective DRV capacitance	44	220		nF

7.4 Thermal Information

THERMAL METRIC[1]		BQ25960 YBG (DSBGA) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	54.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

VBUS=8V, VOUT=4V, T_J= -40°C to +85°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current	ADC disabled, charge disabled, VBUS, VAC1, and VAC2 not present, VBAT=4V		12	20	µA
		ADC enabled (slowest mode), charge disabled, VBUS, VAC1, and VAC2 not present, VBAT=4V		480	750	µA
I_{Q_VAC}	Quiescent VAC current	ADC disabled, charge disabled, ACDRV disabled, EN_HIZ=1, VAC1 or VAC2 =8V		90		µA
		ADC enabled, charge disabled, ACDRV enabled, VAC1 or VAC2= 8V		1330		µA
INTERNAL THRESHOLD						
$V_{VACUVLOZ}$	VAC rising threshold for active I^2C, no VOUT, no VBUS	VAC1 or VAC2 rising	3.24	3.4	3.6	V
$V_{VACUVLO}$	VAC falling threshold for I^2C stop working	VAC1 or VAC2 falling	3.05	3.2	3.4	V
$V_{VACPRESENT}$	VAC rising threshold to turn on ACFET-RBFET	VAC1 or VAC2 rising	3.3	3.4	3.5	V
	VAC falling threshold to turn off ACFET-RBFET	VAC1 or VAC2 falling	3.1	3.2	3.3	V
$V_{VBUSUVLOZ}$	VBUS rising threshold for active I^2C, no VOUT, no VAC	VBUS rising	3.24	3.4	3.6	V
$V_{VBUSUVLO}$	VBUS falling threshold for I^2C stop working	VBUS falling	2.65	2.8	2.95	V
$V_{VBUSPRESENT}$	VBUS rising threshold to allow user set CHG_EN =1	VBUS rising	3.3	3.4	3.5	V
	VBUS falling	VBUS falling	3.1	3.2	3.3	V

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7.5 Electrical Characteristics (continued)

VBUS=8V, VOUT=4V, T_J= -40°C to +85°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VOUTUVLOZ}$	VOUT rising threshold for active I^2C, no VAC, no VBUS	VOUT rising	2.48	2.6	2.72	V
$V_{VOUTUVLO}$	VOUT falling threshold for I^2C stop working	VOUT falling	2.25	2.4	2.55	V
$V_{VOUTPRESENT}$	VOUT rising to threshold allow user set CHG_EN =1	VOUT rising	3.0	3.1	3.2	V
	VOUT falling	VOUT falling	2.9	3.0	3.1	V
RESISTANCE						
R_{ON_BLK}	VBUS to PMID resistance	VBUS=8V		6.1	10.5	mΩ
R_{ON_CH1}	PMID to CFH1 resistance	PMID=8V		19.3	26.8	mΩ
R_{ON_DH1}	CFH1 to VOUT resistance	CFLY=4V		11.4	16.8	mΩ
R_{ON_CL1}	VOUT to CFL1 resistance	VOUT=4V		11.8	18	mΩ
R_{ON_DL1}	CFL1 to GND resistance	CFLY=4V		12	18.3	mΩ
R_{ON_CH2}	PMID to CFH2 resistance	PMID=8V		19.3	26.8	mΩ
R_{ON_DH2}	CFH2 to VOUT resistance	CFLY=4V		11.4	16.8	mΩ
R_{ON_CL2}	VOUT to CFL2 resistance	VOUT=4V		11.8	18	mΩ
R_{ON_DL2}	CFL2 to GND resistance	CFLY=4V		12	18.3	mΩ
R_{VBUS_PD}	VBUS pull down resistance			5		kΩ
R_{VAC_PD}	VAC pull down resistance for both VAC1 and VAC2	VAC=10V		125		Ω
PROTECTION AND ALARM THRESHOLD AND ACCURACY						
V_{BATOVP_RANGE}	Battery over-voltage range		3.491		4.759	V
V_{BATOVP_STEP}	Typical battery over-voltage step			9.985		mV
I_{BATP}	BATP leakage current				1.2	μA
I_{BATN}	BATN leakage current				1	nA
V_{BATOVP_ACC}	Battery over-voltage accuracy	VBATOVP = 4.390V	4.346	4.390	4.434	V
V_{OUTOVP_ACC}	VOUT over-voltage accuracy	VOUTOVP= 5V	4.9	5	5.1	V
I_{BATOCP_RANGE}	Battery over-current range		2.05		8.7125	A
I_{BATOCP_STEP}	Typical battery over-current step			102.5		mA
I_{BATOCP_ACC}	Battery over-current accuracy	IBATOCP=6.15A, RSNS=2mΩ T_J = –20°C - 85°C	5.842	6.15	6.458	A
V_{BUSOVP_RANGE}	VBUS over-voltage range	Switched Cap Mode	7		12.75	V
		Bypass Mode	3.5		6.5	
V_{BUSOVP_STEP}	Typical VBUS over-voltage step	Switched Cap Mode		50		mV
		Bypass Mode		25		mV
V_{BUSOVP_ACC}	VBUS over-voltage accuracy	VBUSOVP = 4.45V	4.39	4.45	4.488	V
		VBUSOVP = 9V	8.91	9	9.09	V
$V_{BUS_ERRHI_RISING_SC}$	VBUS ERRHI rising threshold for switched cap mode stop switching	VOUT=4V		9.6		V
$V_{BUS_ERRHI_FALLING_SC}$	VBUS ERRHI falling threshold for switched cap mode start switching	VOUT=4V		9.4		V
$V_{BUS_ERRHI_RISING_BYPASS}$	VBUS ERRHI rising threshold for bypass mode stop switching	VOUT=4V		4.8		V
$V_{BUS_ERRHI_FALLING_BYPASS}$	VBUS ERRHI falling threshold for bypass mode start switching	VOUT=4V		4.68		V

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7.5 Electrical Characteristics (continued)

VBUS=8V, VOUT=4V, T_J= -40°C to +85°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VACOVP_RANGE}	VAC over-voltage range		6.5		18	V
V_{VACOVP_ACC}	VAC over-voltage accuracy	VACOVP=6.5V	6.3	6.5	6.6	V
		VACOVP=10.5V	10.2	10.5	10.7	V
		VACOVP=14V	13.6	14	14.3	V
V_{VACOVP_HYS}	VACOVP hysteresis			3		%
V_{ACDRV}	ACDRV voltage to external FET	VAC=8V	4.5	5	5.5	V
I_{ACDRV}	ACDRV current capability		20			µA
I_{BUSOCP_RANGE}	Input over-current range	Switched Cap Mode	1.0175		4.579	A
		Bypass Mode	1.0475		6.809	A
I_{BUSOCP_STEP}	Typical input over current step	Switched Cap Mode		254		mA
		Bypass Mode		262		mA
I_{BUSOCP_ACC}	Input over current accuracy	IBUSOCP=3.05A, switched cap mode T_J = –20°C - 85°C	2.897	3.05	3.206	A
		IBUSOCP=3.14A, bypass mode T_J = –20°C - 85°C	2.983	3.14	3.297	A
I_{BUSUCP_ACC}	Input under-current accuracy	BUSUCP=250mA, T_J = –20°C - 85°C	100	250	450	mA
I_{BUSRCP_ACC}	Input reverse-current accuracy	BUSRCP=300mA, T_J = -20°C - 85°C	150	300	450	mA
$TS_{BUS_FLT_RANGE}$	TSBUS fault % of V_{REGN} range		0		50	%
$TS_{BUS_FLT_STEP}$	TSBUS fault % of V_{REGN} step size			0.1953		%
TS_{BUSFLT_ACC}	TSBUS fault accuracy	TSBUS_FLT=20.12%	18.5	20.12	21.5	%
$TS_{BAT_FLT_RANGE}$	TSBAT fault % of V_{REGN} range		0		50	%
$TS_{BAT_FLT_STEP}$	TSBAT fault % of V_{REGN} step size			0.1953		%
$TS_{BAT_FLT_ACC}$	TSBAT voltage accuracy	TSBAT_FLT=20.12%	18.5	20.12	21.5	%
$T_{DIE_FLT_RANGE}$	TDIE over-temperature range		80		140	°C
$T_{DIE_FLT_STEP}$	TDIE over-temperature step			20		°C
$T_{DIE_ALM_RANGE}$	TDIE over-temperature alarm range		25		150	°C
$T_{DIE_ALM_STEP}$	TDIE over-temperature alarm step			0.5		°C
ADC MEASUREMENT PERFORMANCE						
t_{ADC_CONV}	Conversion-time, Each Measurement	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		ms
		ADC_SAMPLE[1:0] = 10		6		ms
		ADC_SAMPLE[1:0] = 11		3		ms
ADC_{RES}	Effective Resolution	ADC_SAMPLE[1:0] = 00	14	15		bit
		ADC_SAMPLE[1:0] = 01	13	14		bit
		ADC_SAMPLE[1:0] = 10	12	13		bit
		ADC_SAMPLE[1:0] = 11	10	11		bit
ADC MEASUREMENT RANGES AND ACCURACY						
I_{BUSADC_RANGE}	ADC BUS current range		0		7	A
I_{BUSADC_LSB}	ADC BUS current LSB	Switched Cap Mode		0.9972		mA
	ADC BUS current LSB	Bypass Mode		1.0279		mA

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7.5 Electrical Characteristics (continued)

VBUS=8V, VOUT=4V, T_J= -40°C to +85°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BUSADC_OFFSET}	ADC BUS current offset	Switched Cap Mode		66		mA
	ADC BUS current offset	Bypass Mode		64		mA
I_{BUSADC_ACC}	ADC BUS current accuracy	IBUS=2A, ADC_SAMPLE[1:0]=00, T_J = –20°C - 85°C	1.9	2	2.1	A
		IBUS=3A, ADC_SAMPLE[1:0]=00, T_J = –20°C - 85°C	2.85	3	3.15	A
V_{BUSADC_RANGE}	ADC BUS voltage range		0		16.39	V
V_{BUSADC_LSB}	ADC BUS voltage LSB			1.002		mV
V_{BUSADC_ACC}	ADC BUS voltage accuracy	VBUS=4V, ADC_SAMPLE[1:0]=00	3.96	4	4.04	V
		VBUS=8V, ADC_SAMPLE[1:0]=00	7.92	8	8.08	V
V_{AC1ADC_RANGE}	ADC VAC1 voltage range		0		14	V
V_{AC1ADC_STEP}	ADC VAC1 voltage LSB			1.0008		mV
V_{AC1ADC_OFFSET}	ADC VAC1 voltage offset			3		mV
V_{AC1ADC_ACC}	ADC VAC1 voltage accuracy	VAC1=4V, ADC_SAMPLE[1:0]=00	3.96	4	4.04	V
		VAC1=8V, ADC_SAMPLE[1:0]=00	7.92	8	8.08	V
V_{AC2ADC_RANGE}	ADC VAC2 voltage range		0		14	V
V_{AC2ADC_LSB}	ADC VAC2 voltage LSB			1.0006		mV
V_{AC2ADC_OFFSET}	ADC VAC2 voltage offset			5		mV
V_{AC2ADC_ACC}	ADC VAC2 voltage accuracy	VAC2=4V, ADC_SAMPLE[1:0]=00	3.96	4	4.04	V
V_{AC2ADC_ACC}	ADC VAC2 voltage accuracy	VAC2=8V, ADC_SAMPLE[1:0]=00	7.92	8	8.08	V
V_{BATADC_RANGE}	ADC BAT voltage range		0		6	V
V_{BATADC_LSB}	ADC BAT voltage LSB			1.0017		mV
V_{BATADC_OFFSET}	ADC BAT voltage offset			1		mV
V_{BATADC_ACC}	ADC BAT voltage accuracy	VBAT=4V, ADC_SAMPLE[1:0]=00	3.96	4	4.04	V
		VBAT=4.4V, ADC_SAMPLE[1:0]=00	4.356	4.4	4.444	V
V_{OUTADC_RANGE}	ADC VOUT voltage range		0		6	V
V_{OUTADC_LSB}	ADC VOUT voltage LSB			1.0037		mV
V_{OUTADC_OFFSET}	ADC VOUT voltage offset			2		mV
V_{OUTADC_ACC}	ADC VOUT voltage accuracy	VOUT=4V, ADC_SAMPLE[1:0]=00	3.98	4	4.02	V
		VOUT=4.4V, ADC_SAMPLE[1:0]=00	4.378	4.4	4.422	V
I_{BATADC_RANGE}	ADC battery current range		-12		12	A
I_{BATADC_LSB}	ADC battery current LSB			0.999		mA
I_{BATADC_OFFSET}	ADC battery current offset			-150		mA
$I_{BATADC_ACC_2mOhm}$	ADC battery current accuracy through 2mOhm sense resistor	IBAT=4A, ADC_SAMPLE[1:0]=00, T_J = –20°C - 85°C	3.92	4.00	4.08	A
		IBAT=6A, ADC_SAMPLE[1:0]=00, T_J = –20°C - 85°C	5.88	6.00	6.12	A
TS_{BUSADC_RANGE}	ADC TSBUS % of V_{REGN} range		0		50	%
TS_{BUSADC_STEP}	ADC TSBUS % of V_{REGN} range LSB			0.0986		%
TS_{BUSADC_OFFSET}	ADC TSBUS % of V_{REGN} range offset			0.1		%
TS_{BUSADC_ACC}	ADC TSBUS accuracy	TSBUS=20% of V_{REGN}, ADC_SAMPLE[1:0]=00	19	20	21	%
TS_{BATADC_RANGE}	ADC TSBAT % of V_{REGN} range		0		50	%

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7.5 Electrical Characteristics (continued)

VBUS=8V, VOUT=4V, T_J= -40°C to +85°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{BATADC_STEP}	ADC TSBAT % of V_{REGN} range LSB			0.0976		%
TS_{BATADC_OFFSET}	ADC TSBAT % of V_{REGN} range offset			0.065		%
TS_{BATADC_ACC}	ADC TSBAT accuracy	TSBAT=20% of V_{REGN}, ADC_SAMPLE[10]=00	19	20	21	%
$TDIE_{_ADC_RANGE}$	ADC TDIE range		-40		150	°C
$TDIE_{_ADC_STEP}$	ADC TDIE step			0.5079		°C
$TDIE_{_ADC_OFFSET}$	ADC TDIE offset			-3.5		°C
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{BUS}=8V, I_{REGN}=20mA		5.0		V
I_{REGN}	REGN LDO current limit	V_{BUS}=8V, V_{REGN}=4.5V	40			mA
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL	Pull up rail 1.2V	0.78			V
V_{IL}	Input low threshold level	Pull up rail 1.2V			0.42	V
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{BIAS}	High-level leakage current	Pull up rail 1.2V			1	µA
LOGIC OUTPUT PIN ($\overline{INT}$, TSBAT_SYNCOUT)						
V_{OL}	Output low threshold level, $\overline{INT}$ pin	Sink current = 5mA			0.4	V
I_{OUT}	High-level leakage current, $\overline{INT}$ pin	Pull up rail 1.8V			1	µA
LOGIC INPUT PIN (SRN_SYNCIN)						
$V_{IH_SRN_SYNCIN}$	Input high threshold level, SRN_SYNCIN		1.3			V
$V_{IL_SRN_SYNCIN}$	Input low threshold level, SRN_SYNCIN				0.4	V
$I_{IN_SRN_SYNCIN}$	High level leakage current	Pull-up rail 1.8V			1	µA

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
TIMINGS					
t_{VACOVP}	VAC OVP response time		100		ns
t_{BATOCP}	IBAT OCP response time		640		µs
t_{INT}	Duration that $\overline{INT}$ is pulled low when an event occurs		256		µs
$t_{ALM_DEBOUNCE}$	Time between consecutive faults for ALM indication		120		ms
I2C INTERFACE					
f_{SCL}	SCL clock frequency			1000	kHz

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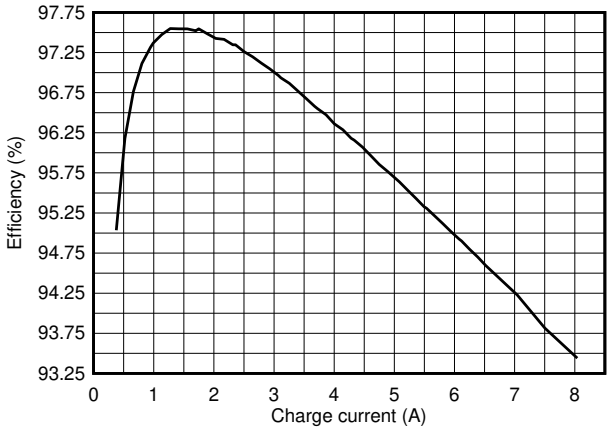
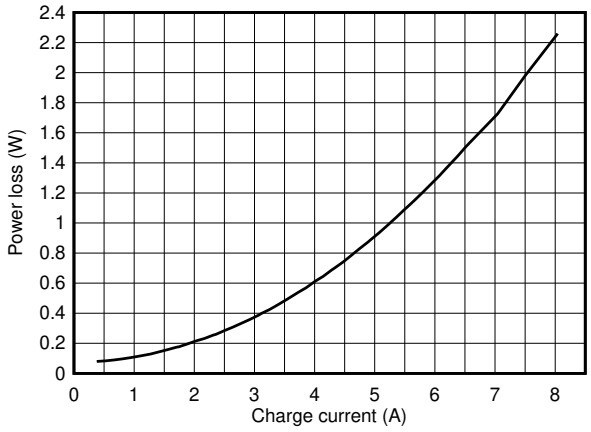
7.7 Typical Characteristics

Typical characteristics are taken with the BMS041 for switching test and GRM188R61C226M is used as CFLY.



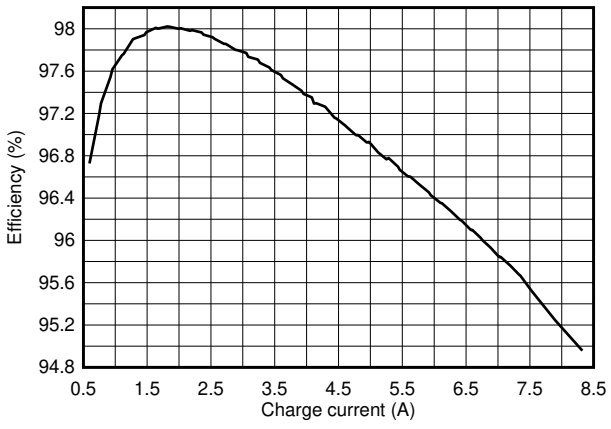
VBAT = 4.0 V, FSW = 500 kHz

Figure 7-1. Battery Charge Efficiency vs. Charge Current, 1 x 22-µF CFLY per Phase Switching Frequency



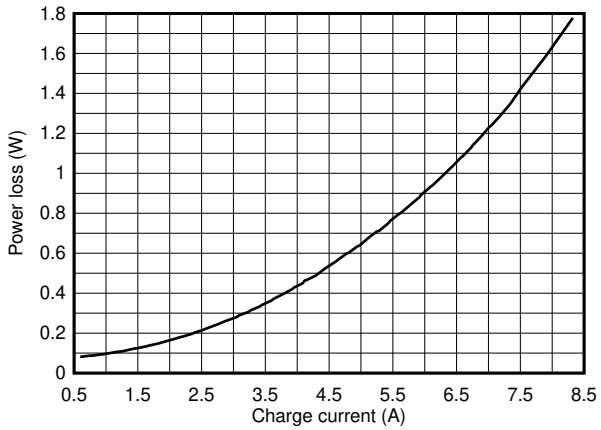
VBAT = 4.0 V, FSW = 500 kHz

Figure 7-2. Battery Charge Power Loss vs. Charge Current, 1 x 22-µF CFLY per Phase Switching Frequency



VBAT = 4.0 V, FSW = 500 kHz

Figure 7-3. Battery Charge Efficiency vs. Charge Current, 2 x 22-µF CFLY per Phase



VBAT = 4.0 V, FSW = 500 kHz

Figure 7-4. Battery Charge Power Loss vs. Charge Current, 2 x 22-µF CFLY per Phase

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7.7 Typical Characteristics (continued)

Typical characteristics are taken with the BMS041 for switching test and GRM188R61C226M is used as CFLY.

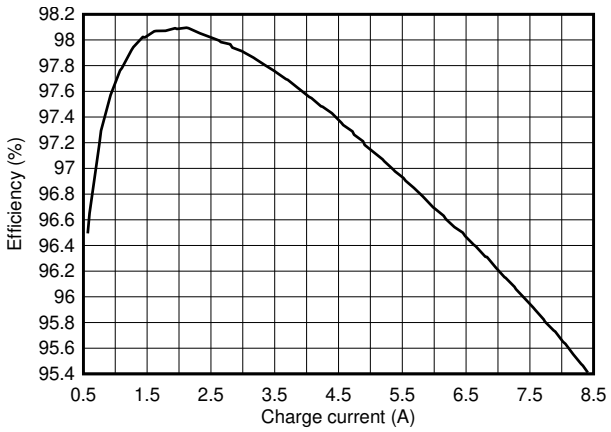

Figure 7-5. Battery Charge Efficiency vs. Charge Current, 3 x 22-µF CFLY per Phase

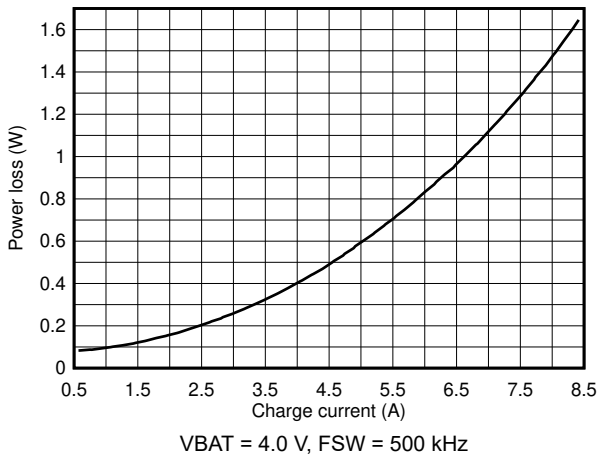

Figure 7-6. Battery Charge Power Loss vs. Charge Current, 3 x 22-µF CFLY per Phase

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8 Detailed Description

8.1 Overview

The BQ25960H is a 98.1% peak efficiency, 8-A battery charging solution using a switched cap architecture for 1-cell Li-ion battery. This architecture allows the cable current to be half the charging current, reducing the cable power loss, and limiting temperature rise. The dual-phase architecture increases charging efficiency and reduces the input and output cap requirements. When used with a main charger such as BQ2561x or BQ2589x, the system the system enables full charging cycle from trickle charge to termination with low power loss at Constant Current (CC) and Constant Voltage (CV) mode.

The device also operates in bypass mode charging the battery directly from VBUS through QB, QCH1 and QDH1 in parallel with QCH2 and QDH2. The impedance in bypass mode is limited to 21 mΩ for 5-A charging current.

The device supports dual input power path management which manages the power flowing from two different input sources. The inputs selection is controlled by host through I^2C with default source #1 as the primary input and the source #2 as the secondary source.

The device integrates all the necessary protection features to ensure safe charging, including input overvoltage and overcurrent protection, output overvoltage and overcurrent protection, temperature sensing for the battery and cable, and monitoring the die temperature.

The device includes a 16-bit ADC to provide bus voltage, bus current, output voltage, battery voltage, battery current, input connector temperature, battery temperature, junction temperature, and other calculated measurements needed to manage the charging of the battery from the smart wall adapter or wireless input or power bank.

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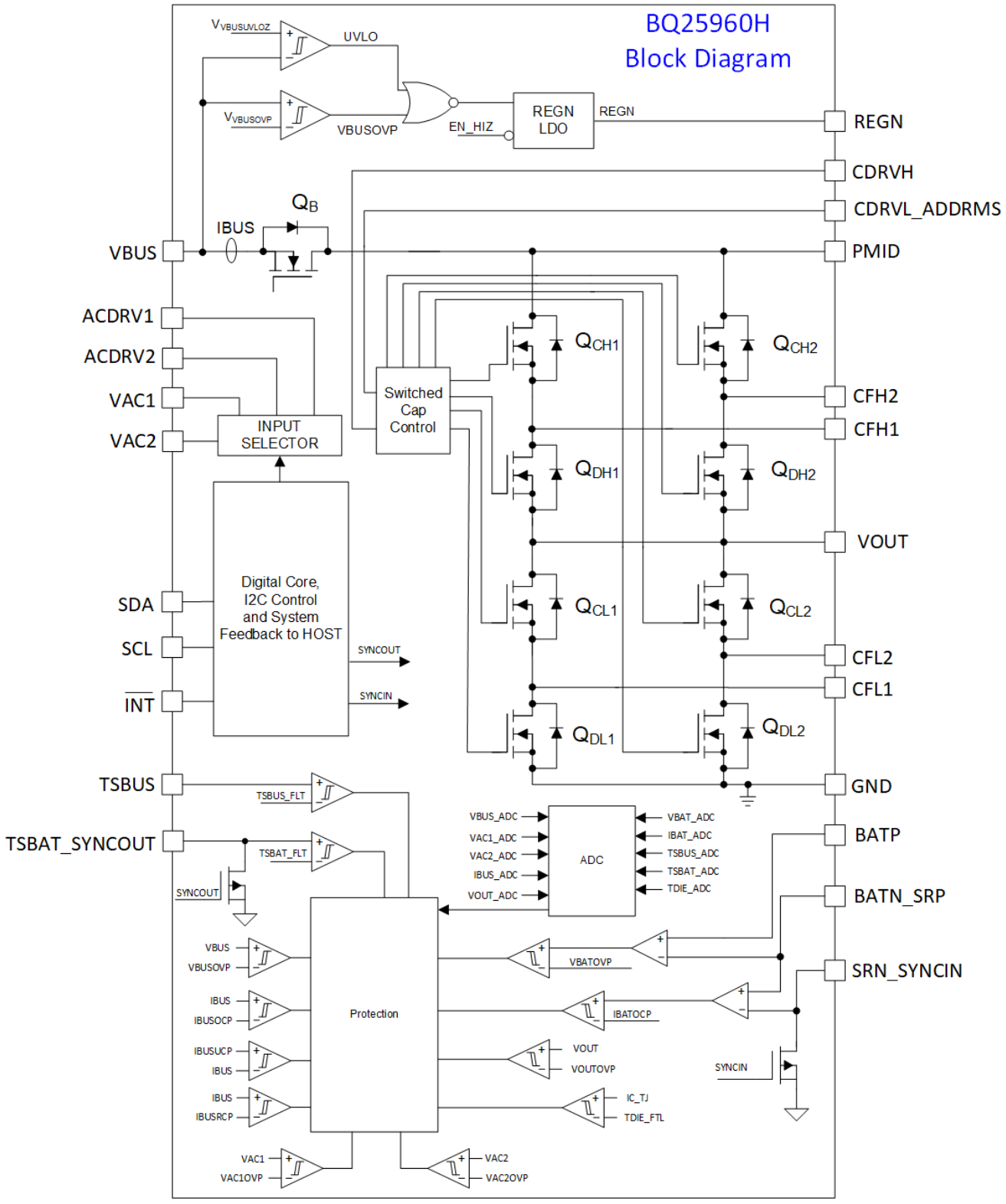
8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Charging System

BQ25960H is a single-cell high efficiency switched cap charger, used in parallel with a switching mode charger. A host must set up the protections and alarms on BQ25960H prior to enabling the BQ25960H. The host must monitor the alarms generated by BQ25960H and communicate with the smart adapter to control the current delivered to the charger.

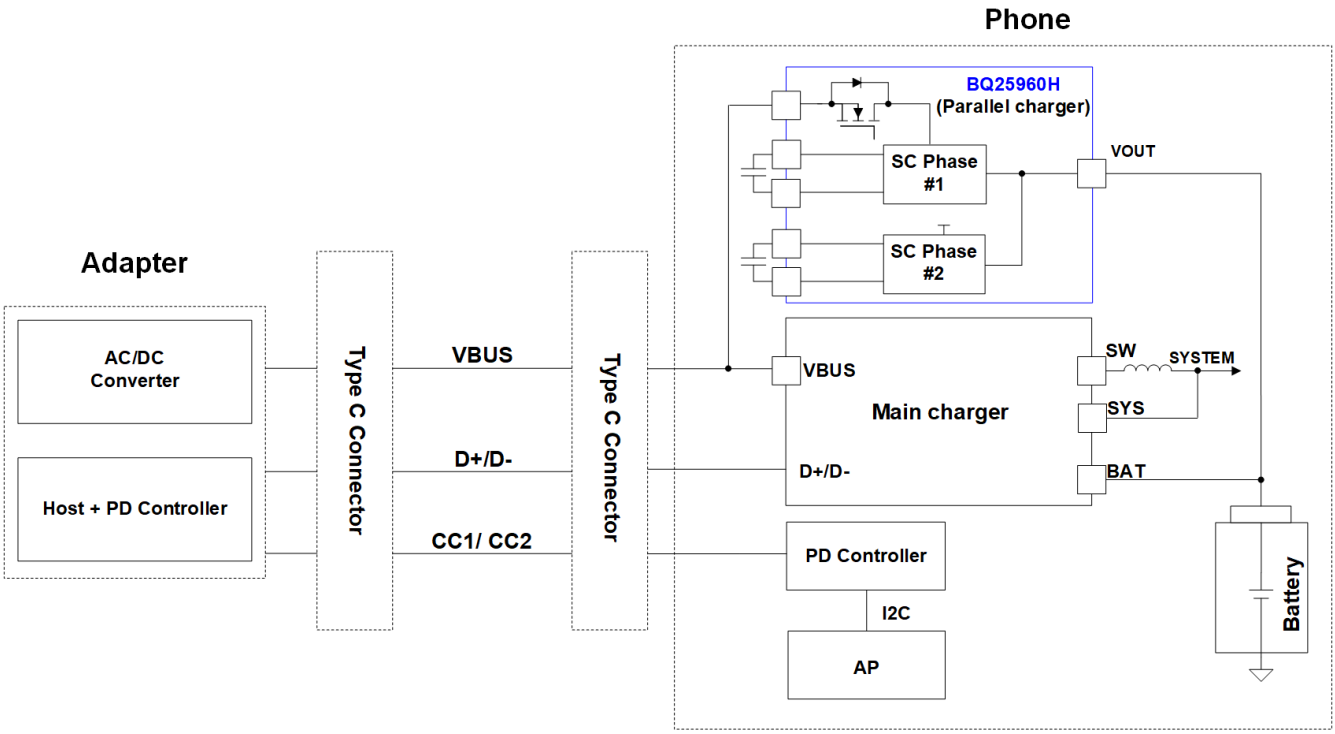

Figure 8-1. BQ25960H System Diagram

8.3.2 Battery Charging Profile

The system will have a specific battery charging profile that is unique due to the switched cap architecture. The charging will be controlled by the main charger such as the BQ2561x or BQ2589x until ystem voltage reaches minimum system regulation voltage V_{SYSMIN}. Once the battery voltage reaches V_{SYSMIN} (3.5 V), the adapter can negotiate for a higher bus voltage, enable BQ25960H charging, and regulate the current on VBUS to charge the battery. In the CC phase, the protection in BQ25960H will not regulate the battery voltage, but will provide feedback to the system to increase and decrease current as needed, as well as disable the blocking and switching FETs if the voltage is exceeded. Once the CV point is reached, the BQ25960H will provide feedback to the adapter to reduce the current, effectively tapering the current until a point where the main charger takes over again. The BQ25960H can operate as long as input current is above the BUSUCP threshold.

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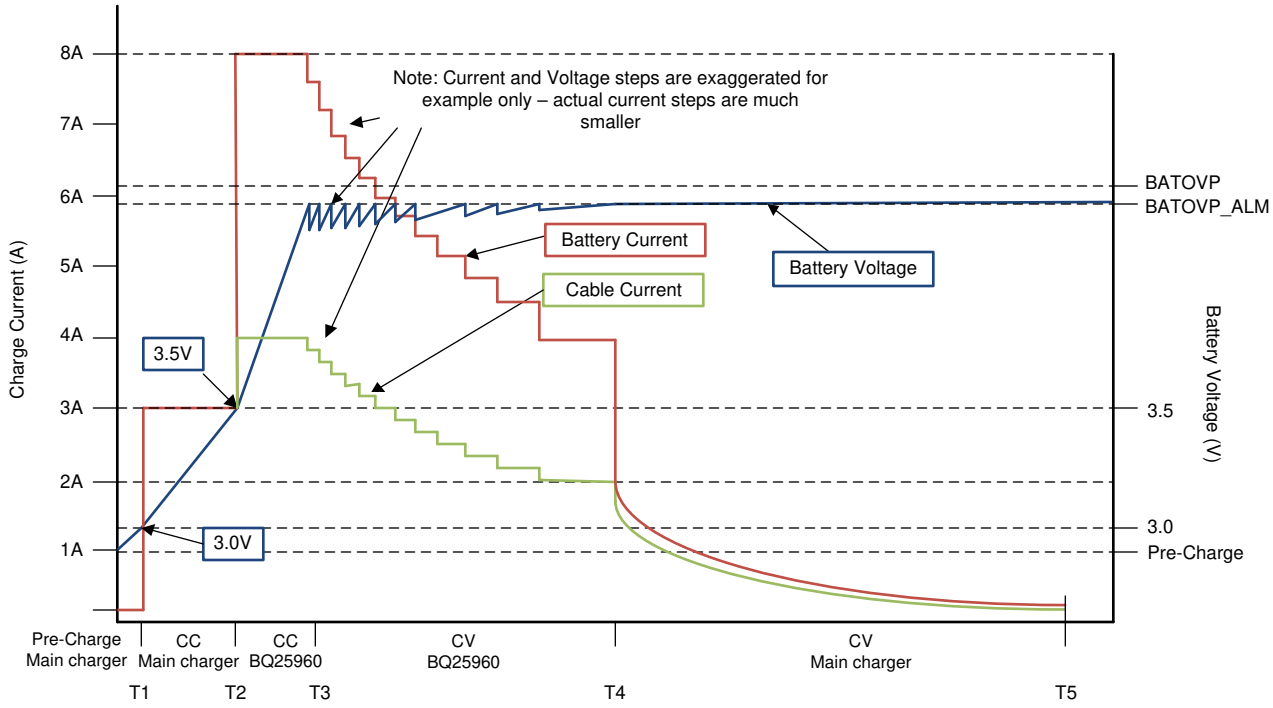

Figure 8-2. BQ25960H System Charging Profile

8.3.3 Device Power Up

The device is powered from the higher of VAC1 or VAC2 (with VAC1 being primary input), VBUS or VOUT (battery). The voltage must be greater than the $V_{VACUVLOZ}$, $V_{VBUSUVLOZ}$ or $V_{VOUTUVLOZ}$ threshold to be a valid supply. When VAC1 or VAC2 rises above $V_{VACUVLOZ}$ or VBUS rises above $V_{VBUSUVLOZ}$ or VOUT rises above $V_{VOUTUVLOZ}$, I^2C interface is ready for communication and all the registers are reset to default value. The host needs to wait VBUSPRESENT_STAT and VOUTPRESENT_STAT go high before setting CHG_EN =1 and start charging.

8.3.4 Device HIZ State

The device enters HIZ mode when EN_HIZ bit is set to '1'. When device is in HIZ mode, the converter stops switching, ADC stops converting, ACDRV is turned off and REGN LDO is forced off even when the adapter is present and no fault condition is present. The device exits HIZ Mode when EN_HIZ is set to '0' by host or device POR.

The faults conditions force the converter stop switching and clear CHG_EN bit, but keep REGN on and EN_HIZ bit = 0. More details can be found in the Device Protection section.

8.3.5 Dual Input Bi-Directional Power Path Management

The device has two ACDRV pins to drive two sets of N-channel ACFET-RBFET, which select and manage the input power from two different input sources. A single GaN FET can be used to replace an ACFET-RBFET combination and will be treated the same as an ACFET-RBFET combination. In the POR sequence, the device detects if the protection FET(s) are populated based on if ACDRV pin is shorted to ground or not, and then updates the status register ACRB1_CONFIG_STAT or ACRB2_CONFIG_STAT to indicate the presence of AC protection FETs. If the external ACFET-RBFET or GaN FET is not populated in the schematic, then tie VAC to VBUS and connect ACDRV to GND. The device supports:

1. single input without external FET
2. single input with one single ACFET
3. dual input with one set of ACFET-RBFET
4. dual input with two sets of ACFET-RBFET

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The power-up sequences for different applications are described in detail below.

8.3.5.1 ACDRV Turn-On Condition

The ACDRV controls input power MUX for both BQ25960H and main charger. In order to turn the ACDRV, all of the following conditions must be valid:

1. The corresponding AC-RB FET is populated: VAC is not short to VBUS and ACDRV is not short to ground
2. VAC is above $V_{VACpresent}$ threshold
3. VAC is below V_{VACOVP} threshold
4. DIS_ACDRV_BOTH is not set to '1'
5. EN_HIZ is not set to '1'
6. VBUS is below $V_{VBUSpresent}$ threshold

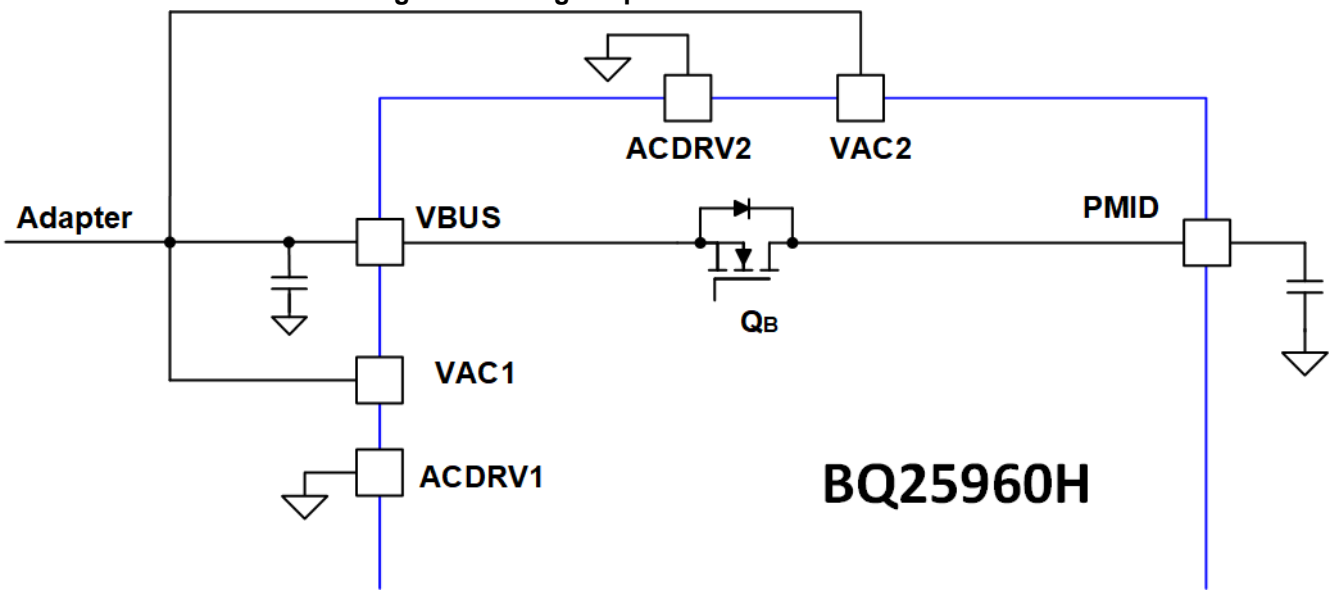
8.3.5.2 Single Input from VAC to VBUS without ACFET-RBFET

In this scenario, VAC1 and VAC2 are both shorted to VBUS, ACDRV1 and ACDRV2 are pulled down to ground. The table below summarizes the VAC1/VAC2, ACDRV1/ACDRV2 connection, register control, and status functions.

Table 8-1. Single Input without External FET Summary

INPUT CONFIGURATION	SINGLE INPUT
External FET connection	No external FET
Input pin connection	VAC1 and VAC2 short to VBUS
ACDRV pin connection	ACDRV1 and ACDRV2 short to ground
ACDRV1_STAT	0
ACDRV2_STAT	0
DIS_ACDRV_BOTH	1
ACRB1_CONFIG_STAT	0
ACRB2_CONFIG_STAT	0
EN_HIZ	No impact on ACDRV

Figure 8-3. Single input without ACFET-RBFET



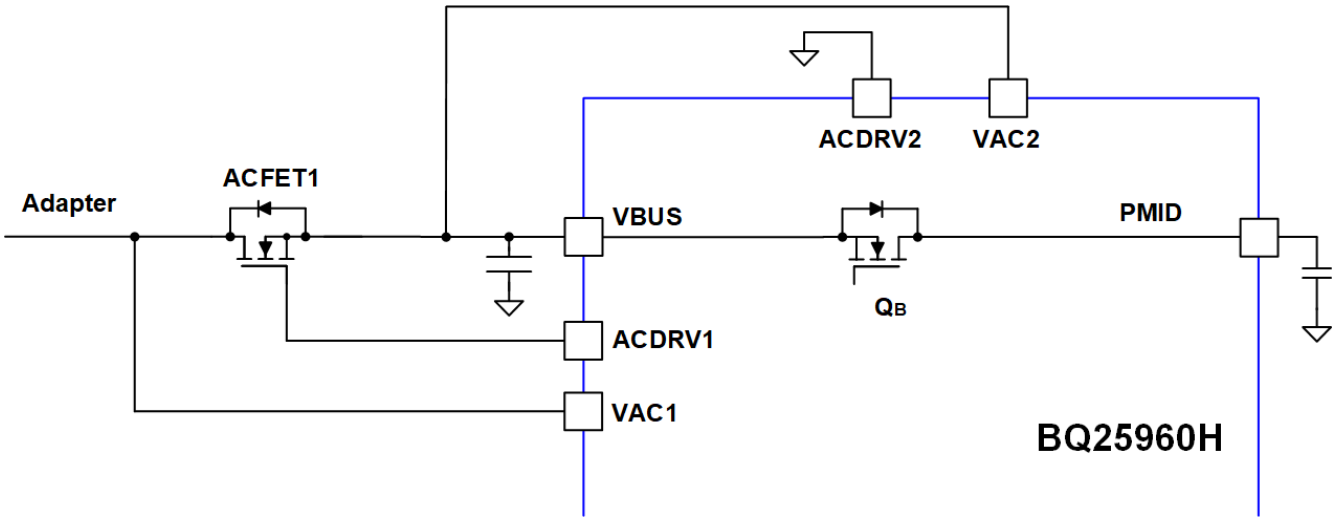
8.3.5.3 Single Input with ACFET1

In this scenario, ACFET1 without RBFET1 is populated, but ACFET2-RBFET2 is not. VAC2 is short to VBUS and ACDRV2 is pulled down to ground. The table below summarizes the VAC1/ VAC2, ACDRV1/ACDRV2 connection, register control, and status functions. Use VAC1 for single input configuration.

Table 8-2. Single Input with Single ACFET1

INPUT CONFIGURATION	SINGLE INPUT
External FET connection	ACFET1, no ACFET2-RBFET2
Input pin connection	VAC1 connected to input source VAC2 short to VBUS
ACDRV pin connection	ACDRV1 active ACDRV2 tie to ground
ACDRV1_STAT	1: ACDRV1 is ON 0: ACDRV1 is OFF
ACDRV2_STAT	0
DIS_ACDRV_BOTH	0: Allow ACDRV1 to turn on if the conditions of ACDRV turn on are met. 1: Force ACDRV1 OFF
ACRB1_CONFIG_STAT	1
ACRB2_CONFIG_STAT	0
EN_HIZ	0: Allow ACDRV1 to turn on if the conditions of ACDRV turn on are met. 1: Force ACDRV1 OFF

Figure 8-4. Single Input with ACFET



8.3.5.4 Dual Input with ACFET1-RBFET1

In this scenario, ACFET1-RBFET1 is populated, but ACFET2-RBFET2 is not. VAC2 is short to VBUS and ACDRV2 is pulled down to ground. The table below summarizes the connection, register control and status functions. Use VAC1 for adapter input and VBUS for wireless input.

Table 8-3. Dual Input with ACFET1-RBFET1

INPUT CONFIGURATION	DUAL INPUT
External FET connection	ACFET1-RBFET1, no ACFET2-RBFET2
Input pin connection	VAC1 connected to input source 1 VAC2 short to VBUS
ACDRV pin connection	ACDRV1 active ACDRV2 short to ground

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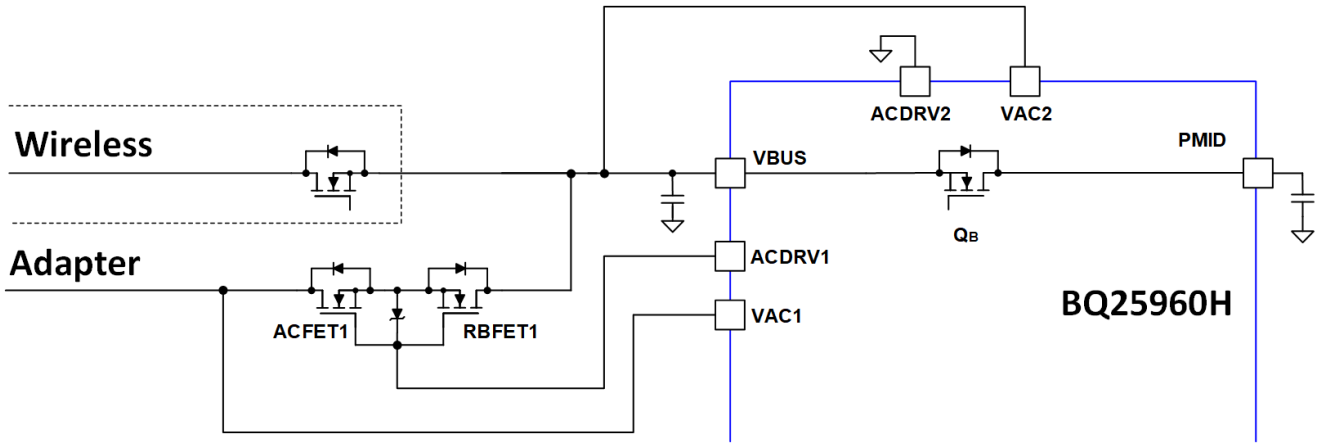
Table 8-3. Dual Input with ACFET1-RBFET1 (continued)

INPUT CONFIGURATION	DUAL INPUT
ACDRV1_STAT	0: ACDRV1 OFF 1: ACDRV1 ON
ACDRV2_STAT	0
DIS_ACDRV_BOTH	0: Allow ACDRV1 to turn on if other conditions of ACDRV turn on are met 1: Force ACDRV1 OFF
ACRB1_CONFIG_STAT	1
ACRB2_CONFIG_STAT	0
EN_HIZ	0: Allow ACDRV1 to turn on if other conditions of ACDRV turn on are met 1: Force ACDRV1 OFF

Figure 8-5. Dual Input with ACFET-RBFET1



8.3.5.5 Dual Input with ACFET1-RBFET1 and ACFET2-RBFET2

In this scenario, both ACFET1-RBFET1 and ACFET2-RBFET2 are populated and the device supports dual input. The table below summarizes the connection, register control and status functions. Connect input with high OVP threshold to VAC1.

Table 8-4. Dual Input with Both ACFET1-RBFET1 and ACFET2-RBFET2 Summary

INPUT CONFIGURATION	DUAL INPUT
External FET connection	ACFET1-RBFET1, ACFET1-RBFET2
Input pin connection	VAC1 connected to input source 1 VAC2 connected to input source 2 **No input source allowed to connect to VBUS**
ACDRV pin connection	ACDRV1 and ACDRV2 active
ACDRV1_STAT	0: ACDRV1 OFF 1: ACDRV1 ON Once device is in dual input configuration with ACFET1-RBFET1 and ACFET2-RBFET2, the host can use this bit to swap the input between VAC1 and VAC2 if both VAC1 and VAC2 are valid.
ACDRV2_STAT	0: ACDRV2 OFF 1: ACDRV2 ON Once device is in dual input configuration with ACFET1-RBFET1 and ACFET2-RBFET2, the host can use this bit to swap the input between VAC1 and VAC2 if both VAC1 and VAC2 are valid.

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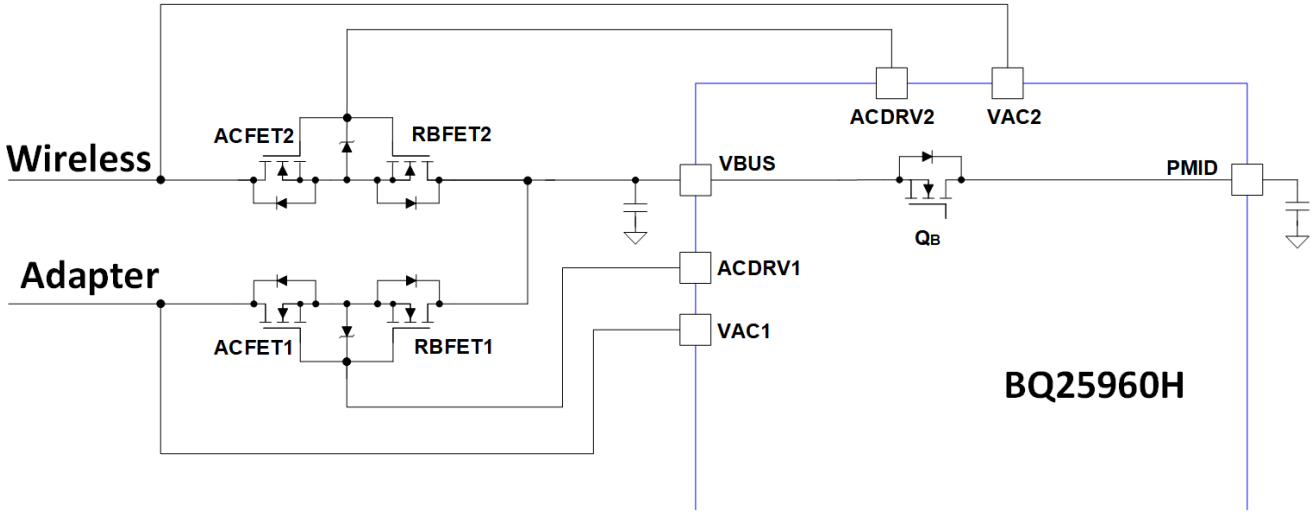
Table 8-4. Dual Input with Both ACFET1-RBFET1 and ACFET2-RBFET2 Summary (continued)

INPUT CONFIGURATION	DUAL INPUT
DIS_ACDRV_BOTH	0: Allow ACDRV to turn on. By default, ACDRV1 is turned on if the conditions of ACDRV turn on are met, ACDRV1_STAT=1 and ACDRV2_STAT =0. In On-The-GO (OTG) or Reverse TX Mode, refer to OTG and Reverse TX Mode Operation session for turn on precedence. 1: Force both ACDRV to turn off, both ACDRV1_STAT and ACDRV2_STAT become 0.
ACRB1_CONFIG_STAT	1
ACRB2_CONFIG_STAT	1
EN_HIZ	0: Allow ACDRV to turn on for the port w/ VAC present if the conditions of ACDRV turn on are met. ACDRV1 is turned on since VAC1 is the primary input source when both VAC1 and VAC2 present and the turn on conditions are met. 1: Turns off both ACDRV

Figure 8-6. Two Inputs with ACFET-RBFET1 and ACFET-RBFET2



8.3.5.6 OTG and Reverse TX Mode Operation

When the main charger is in OTG or reverse TX Mode, the input power MUX (ACFET-RBFET) also controls which port is desired for OTG output.

To enter OTG or reverse TX Mode, the host should follow the steps below:

1. Host writes EN_OTG =1
2. BQ25960H sets DIS_ACDRV_BOTH =1
3. Host writes DIS_ACDRV_BOTH=0, and then writes ACDRV1_STAT=1 or ACDRV2_STAT=1 depending on which port is desired for OTG or reverse TX output
4. Host enables OTG Mode on main charger
5. If VBUSOVP or VACOVP fault occurs, ACDRV will be disabled but EN_OTG is still '1'. Host needs to write ACDRV1_STAT high or ACDRV2_STAT high when the fault is cleared. Set VAC1OVP and VAC2OVP to the same threshold in the OTG Mode
6. EN_OTG is cleared when watchdog timer expires

To exit OTG or Reverse TX Mode, the host should follow the steps below:

1. Turn off main OTG or reverse TX source
2. Turn on VBUS pulldown resistor (R_{VBUS_PD}) by setting BUS_PD_EN=1 or VAC pulldown resistor R_{VAC_PD} by setting VAC1_PD_EN=1 or VAC2_PD_EN=1, depending on which port is to be discharged
3. Wait for VBUS and VAC to be discharged

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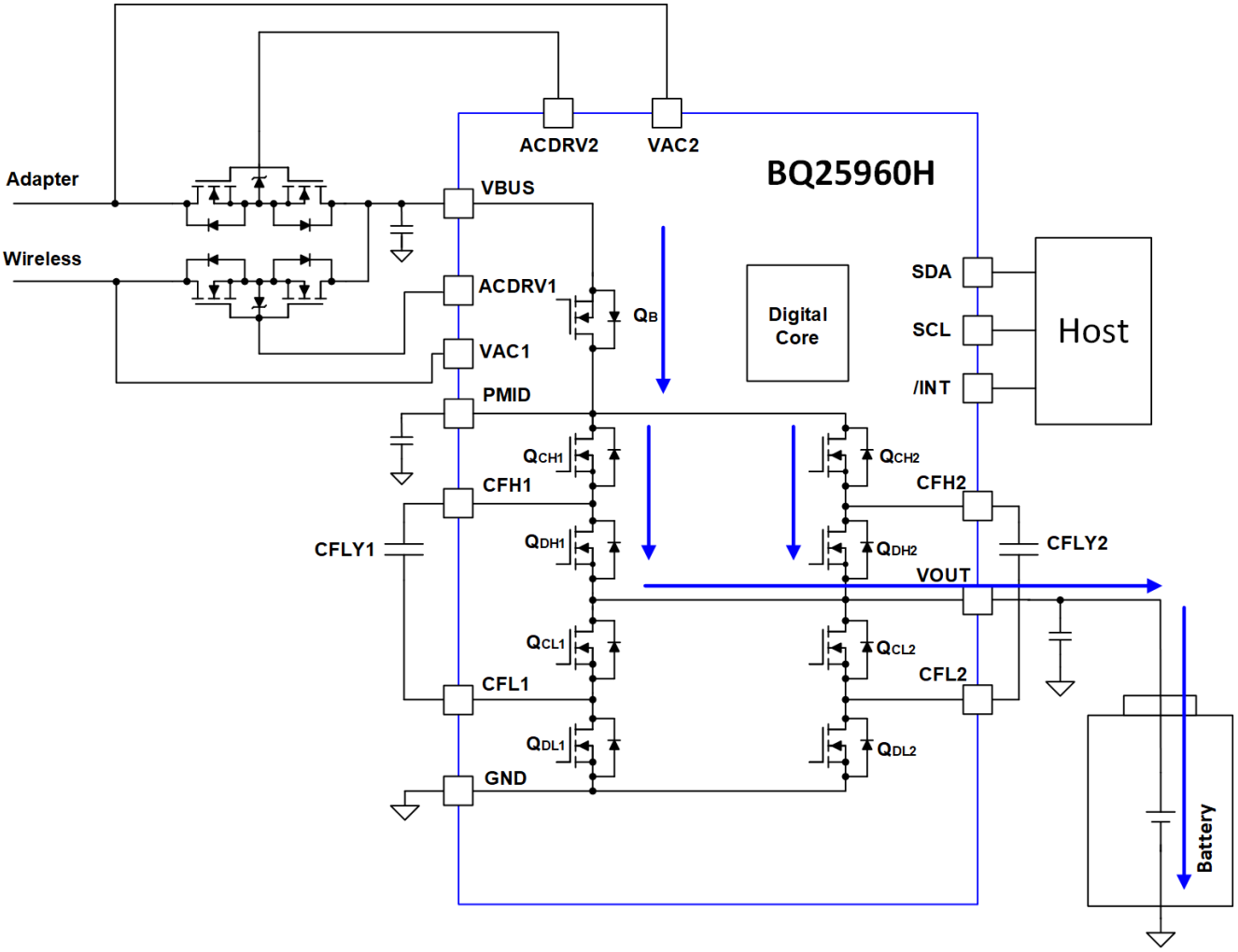
4. Turn off ACDRV by setting ACDRV1_STAT=0 or ACDRV2_STAT=0
5. Exit OTG Mode by setting EN_OTG=0

8.3.6 Bypass Mode Operation

When host determines the adapter support bypass mode charging, the device can enable Bypass mode by setting EN_BYPASS=1. Blocking FET (Q_B) and four high side switching FET (QCH1 and QDH1/ QCH2 and QDH2) are turned on to charge from adapter to battery. During Bypass Mode, when fault occurs, CHG_EN is cleared but EN_BYPASS stays '1'.

Figure 8-7. BQ25960H Bypass Mode



To change from Bypass Mode to Switched Cap Mode or from Switched Cap to Bypass Mode, the host would first set CHG_EN=0 to stop the converter and then set EN_BYPASS to desired value. The host sets desired protection threshold based on the selected operation modes and then host enables charge by setting CHG_EN=1.

8.3.7 Charging Start-Up

The host can start Switched Cap or Bypass Mode charging follow the steps below:

1. Both VBUS and VOUT need to be present. Host can check the status through VBUSPRESENT_STAT (REG15[2]) and VOUTPRSENT_STAT (REG15[5]). Both of them need to be '1'.
2. Host sets all the protections to the desired thresholds. Refer to the Device Modes and Protection Status section for proper setting.

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3. Host sets either Switched Cap Mode or Bypass Mode through EN_BYPASS bit (REG0F[3]) based on adapter type.
4. Host sets the desired switching frequency in Switched Cap Mode through FSW_SET [2:0] bits (REG10[7:5]).
5. Host sets BUS under current protection (BUSUCP) to 250 mA though BUSUCP bit (REG05[6])=1
6. Host sets charger configuration bits: CHG_CONFIG_1 (REG05[3])=1.
7. Host can enable charge by setting CHG_EN=1.
8. Once charge has been enabled, the CONV_ACTIVE_STAT bit is set to '1' to indicate either switched cap or bypass is active, and current starts to flow to the battery.
9. When watchdog timer expires, CHG_EN is reset to '0' and charging stops. Host needs to read or write any register bit before watchdog expires, or disable watchdog timer (set REG10[2]=1) to prevent watchdog timer from expiring.

8.3.8 Adapter Removal

If adapter is removed during soft start timer, CHG_EN will be cleared after soft-start timer expires. The user can program the soft-start timer in SS_TIMEOUT register. If adapter is removed after soft-start timer expires, converter stops switching and CHG_EN is cleared after the deglitch time programmed in IBUSUCP_FALL_DG_SEL register. The device prevents boost back when the adapter is removed during and after the soft-start timer. To accelerate VBUS or VAC discharge after adapter removal, the user to turn on the VBUS pulldown resistor (R_{VBUS_PD}) and VAC pulldown current resistor (R_{VAC_PD}) by setting BUS_PD_EN or VAC1_PD_EN or VAC2_PD_EN to '1'.

8.3.9 Integrated 16-Bit ADC for Monitoring and Smart Adapter Feedback

The integrated 16-bit ADC of the device allows the user to get critical system information for optimizing the behavior of the charger control. The control of the ADC is done through the ADC control register. The ADC_EN bit provides the ability to enable and disable the ADC to conserve power. The ADC_RATE bit allows continuous conversion or one-shot behavior. The ADC_AVG bit enables or disables (default) averaging. ADC_AVG_INIT starts average using the existing (default) or using a new ADC value.

To enable the ADC, the ADC_EN bit must be set to ‘1’. The ADC is allowed to operate if the V_{VAC}>$V_{VACPRESENT}$, V_{VBUS}>$V_{VBUSPRESENT}$ or V_{VOUT}>$V_{VOUTPRESENT}$ is valid. If ADC_EN is set to ‘1’ before VAC, VBUS or VOUT reach their respective PRESENT threshold, then the ADC conversion will be postponed until one of the power supplies reaches the threshold.

The ADC_SAMPLE bits control the sample speed of the ADC, with conversion times of t_{ADC_CONV}. The integrated ADC has two rate conversion options: a 1-shot mode and a continuous conversion mode set by the ADC_RATE bit. By default, all ADC parameters will be converted in 1-shot or continuous conversion mode unless disabled in the ADC CONTROL 1 and ADC_CONTROL 2 register. If an ADC parameter is disabled by setting the corresponding bit in the ADC CONTROL 1 and ADC_CONTROL 2 register, then the value in that register will be from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place). If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC CONTROL 1 and ADC_CONTROL 2 register is set to ‘0’.

The ADC_DONE_* bits signal when a conversion is complete in 1-shot mode only. During continuous conversion mode, the ADC_DONE_* bits have no meaning and will be ‘0’.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = ‘0’ to disable the ADC. ADC readings are only valid for DC states and not for transients. When host writes ADC_EN=0, the ADC stops immediately. If the host wants to exit ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE to one-shot, and the ADC will stop at the end of a complete cycle of conversions, or

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2. Write all the DIS bits low, and the ADC will stop at the end of the current measurement.

When external sense resistor (RSNS) is placed and IBATADC is used, it is recommended to use 375-kHz switching frequency.

8.3.10 Device Modes and Protection Status

Table 8-5 shows the features and modes of the device depending on the conditions of the device.

Table 8-5. Device Modes and Protection Status

FUNCTIONS AVAILABLE	STATE			
	BATTERY ONLY VAC1/ VAC2/ VBUS NOT PRESENT	INPUT PRESENT	INPUT PRESENT	INPUT PRESENT
		CHARGE DISABLED	DURING SOFTSTART TIMER	AFTER SOFTSTART TIMER
I^2C allowed	X	X	X	X
ADC	X	X	X	X
ACDRV gate drive		X	X	X
VACOVP		X	X	X
TDIE_ALM		X	X	X
TDIE_TFL		X	X	X
BUSOVP_ALM			X	X
BUSOCP_ALM			X	X
BATOVP_ALM			X	X
BATOCP_ALM			X	X
BATUCP_ALM			X	X
VOUTOVP		X	X	X
TSBUS_FLT		X	X	X
TSBAT_ FLT		X	X	X
BUSOVP		X	X	X
BATOVP		X	X	X
BATOCP			X	X
BUSOCP			X	X
BUSUCP				X
BUSRCP			X	X

Tripping any of these protections causes Q_B to be off and converter stops switching. Masking the fault or alarm does NOT disable the protection, but only keeps an $\overline{INT}$ from being triggered by the event. Disabling the fault or alarm protection other than BUSUCP holds that STAT and FLAG bits in reset, and also prevents an interrupt from occurring. Disable BUSUCP protection still sets STAT and FLAT bits and sends interrupt to alert host but keeps converter running when triggered.

When any OVP, OCP, RCP or overtemperature fault event is triggered, the CHG_EN bit is set to ‘0’ to disable charging, and the charging start-up sequence must be followed to begin charging again.

8.3.10.1 Input Overvoltage, Overcurrent, Undercurrent, Reverse-Current and Short-Circuit Protection

Input overvoltage protection with external single or back-to-back N-channel FET(s): The device integrates the functionality of an input overvoltage protector. With external single or back-to-back N-channel FET(s), the device blocks high input voltage exceeding VACOVP threshold (VAC1OVP or VAC2OVP). This eliminates the need for a separate OVP device to protect the overall system. The integrated VACOVP feature has a response time of t_{VACOVP} (the actual time to turn off external FET(s) will be longer and depends upon the FET(s) gate

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capacitance). The VAC1OVP and VAC2OVP setting is adjustable in the VAC control register. The part allows the user to have different VAC1OVP and VAC2OVP settings. Always put the high VACOVP threshold input to VAC1.

When VAC1OVP or VAC2OVP is tripped, corresponding ACDRV is turned off and VAC1OVP_STAT or VAC2OVP_STAT and VAC1OVP_FLAG or VAC2OVP_FLAG is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by VAC1OVP_MASK or VAC2OVP_MASK). When VAC2OVP is triggered, the device sends multiple interrupts when the fault persists. Use VAC1 as input unless both VAC1 and VAC2 are needed.

Input overvoltage protection (BUSOVP): The BUSOVP threshold is adjustable in the BUSOVP register. When BUSOVP is tripped, switched cap or bypass mode is disabled and CHG_EN is set to '0'. BUSOVP_STAT and BUSOVP_FLAG is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by BUSOVP_MASK). The start-up sequence must be followed to resume charging.

Input overcurrent protection (BUSOCP): Input overcurrent protection monitors the current flow into VBUS. The overcurrent protection threshold is adjustable in the BUSOCP register. When BUSOCP is tripped, Switched Cap or Bypass Mode is disabled and CHG_EN is set to '0'. BUSOCP_STAT and BUSOCP_FLAG is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by BUSOCP_MASK). The start-up sequence must be followed to resume charging.

Input undercurrent protection (**BUSUCP)**: BUS undercurrent protection (UCP) is implemented to detect adapter unplug. Set BUSUCP =1 (REG05[6]) before enable charge. When BUSUCP is enabled (BUSUCP_DIS=0), if the current is below BUSUCP after soft start timer (programmable in SS_TIMEOUT[2:0]) expires, Switched Cap or Bypass Mode is disabled and CHG_EN is set to '0'. BUSUCP_STAT and BUSUCP_FLAG is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by BUSUCP_MASK). The start-up sequence must be followed to resume charging. The deglitch time for BUSUCP is programmable in IBUSUCP_FALL_DG_SET[1:0] register. Please note that BUSUCP deglitch time needs to be set shorter than soft start timer in order for BUSUCP to be effective.

When BUSUCP is disabled (BUSUCP_DIS=1), if the current is below BUSUCP after soft-start timer expires, CHG_EN is not set to '0', BUSUCP_STAT and BUSUCP_FLAG is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by BUSUCP_MASK). The host can determine if charge needs to be stopped in this case.

Input reverse-current protection (**BUSRCP**): The device monitors the current flow from VBUS to VBAT to ensure there is no reverse current (current flow from VBAT to VBUS). In an event that a reverse current flow is detected when BUSRCP_DIS is set to '0', the Switched Cap or Bypass is disabled and CHG_EN is set to '0'. The start-up sequence must be followed to resume charging. To disable BUSRCP, set REG05[1:0] to '00' and then set BUSRCP_DIS=1.

RCP is always active when converter is switching and BUSRCP_DIS is set to '0'. When RCP is tripped, BUSRCP_STAT and BUSRCP_FLAG is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by BUSRCP_MASK).

Input overvoltage and overcurrent protection alarm (**BUSOVP_ALM and BUSOCP_ALM):** In addition to input overvoltage and overcurrent, the device also integrates alarm function BUSOVP_ALM and BUSOCP_ALM. When alarm is triggered, the corresponding STAT and FLAG bit is set to '1' and $\overline{INT}$ is asserted low to alert the host (unless it is masked by the MASK bit). However, CHG_EN is not cleared and host can reduce input voltage or input current to prevent VBUS reaching VBUSOVP threshold or IBUS reaching IBUSOCP threshold.

VBUS_ERRHI: the device monitors VBUS to VOUT voltage ratio. If VBUS/VOUT is greater than $V_{BUS_ERRHI_RISING}$ threshold, the converter does not switch but CHG_EN is kept at '1'. The converter automatically starts switching when the VBUS/VOUT drops below $V_{BUS_ERRHI_FALLING}$ threshold.

8.3.10.2 Battery Overvoltage and Overcurrent Protection

BATOVP and BATOVP_ALM: The device integrates both overcurrent and overvoltage protection for the battery. The device monitors the battery voltage on BATP and BATN_SRP. In order to reduce the possibility of battery terminal shorts during manufacturing, 100-Ω series resistors on BATP is required. If external sense resistor is not used, place 100-Ω series resistors on BATN as well. The device is intended to be operated within the window formed by the BATOVP and BATOVP_ALM. When the BATOVP_ALM is reached, an interrupt is

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sent to the host to reduce the charge current and thereby not reaching the BATOVP threshold. If BATOVP is reached, the switched cap or bypass is disabled and CHG_EN is set to '0', and the start-up sequence must be followed to resume charging. At the same time, BATOVP_STAT and BATOVP_FLAG are set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by BATOVP_MASK). BATOVP and BATOVP_ALM is disabled when BATOVP_DIS and BATOVP_ALM_DIS is set to '1'.

BATOCP and BATOCP_ALM: The device monitors current through the battery by monitoring the voltage across the external series battery sense resistor. The differential voltage of this sense resistor is measured on BATN_SRP and SRN_SYNCIN. The device is intended to be operated within the window formed by the BATOCP and BATOCP_ALM. When the BATOCP_ALM is reached, an interrupt is sent to the host to reduce the charge current from reaching the BATOCP threshold. If BATOCP is reached, the Switched Cap or Bypass is disabled after a deglitch time of t_{BATOCP} and CHG_EN is set to '0', and the start-up sequence must be followed to resume charging. At the same time, BATOCP_STAT and BATOCP_FLAG are set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by BATOCP_MASK). BATOCP and BATOCP_ALM is disabled when BATOCP_DIS and BATOCP_ALM_DIS is set to '1'.

VOUTOVP: The device also monitors output voltage between VOUT and ground in case of battery removal to protect the system. If VOUTOVP is reached and VOUTOVP_DIS=0, the Switched Cap or Bypass is disabled and CHG_EN is set to '0', and the start-up sequence must be followed to resume charging. At the same time, VOUTOVP_STAT and VOUTOVP_FLAG is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by VOUTOVP_MASK). If VOUTOVP_DIS =1, the protection is disabled.

8.3.10.3 IC Internal Thermal Shutdown, TSBUS, and TSBAT Temperature Monitoring

The device has three temperature sensing mechanisms to protect the device and system during charging:

1. TSBUS for monitoring the cable connector temperature
2. TSBAT for monitoring the battery temperature
3. TDIE for monitoring the internal junction temperature of the device

The TSBUS and TSBAT both rely on a resistor divider that has an external pullup voltage to REGN. Place a negative coefficient thermistor (NTC) in parallel to the low-side resistor. A fault on the TSBUS and TSBAT pin is triggered on the falling edge of the voltage threshold, signifying a "hot" temperature. The threshold is adjusted using the TSBUS_FLT and TSBAT_FLT registers.

The typical TS resistor network on TSBAT_SYNCOUT is illustrated in Figure 8-8. The resistor network on TSBUS is the same.

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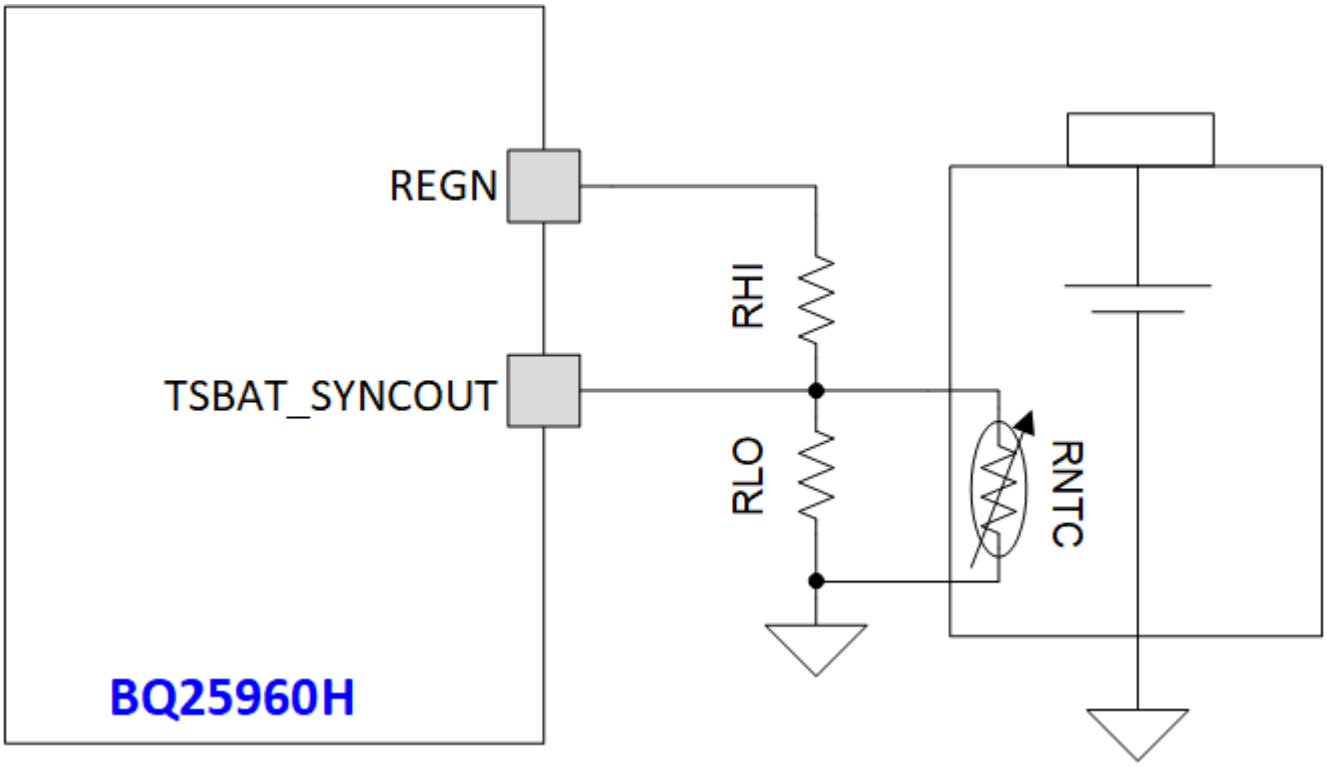

Figure 8-8. TSBAT_SYNCOUT Resistor Network

The RLO and RHI resistors should be chosen depending on the NTC used. If a 10-kΩ NTC is used, use 10-kΩ resistors for RLO and RHI. If a 100-kΩ NTC is used, use 100-kΩ resistors for RLO and RHI. The ratio of VTS/REGN can be from 0% to 50%, and the voltage at the TS pin is determined by the following equation.

$$TSBUS\ or\ TSBAT\ (V) = \frac{\frac{1}{(\frac{1}{RNTC} + \frac{1}{RLO})}}{RHI + \frac{1}{(\frac{1}{RNTC} + \frac{1}{RLO})}} \times VREGN \quad (1)$$

The percentage of the TS pin voltage is determined by the following equation.

$$TSBUS\ or\ TSBAT\ (\%) = \frac{\frac{1}{(\frac{1}{RNTC} + \frac{1}{RLO})}}{RHI + \frac{1}{(\frac{1}{RNTC} + \frac{1}{RLO})}} \quad (2)$$

Additionally, the device measures internal junction temperature, with adjustable threshold TDIE_FLT in TDIE_FLT register.

If the TSBUS_FLT, TSBAT_FLT, and TDIE_FLT thresholds are reached, the Switched Cap or Bypass Mode is disabled and CHG_EN is set to ‘0’, and the start-up sequence must be followed to resume charging. The corresponding STAT and FLAG bit is set to ‘1’ unless it is masked by the MASK bit. If TSBUS, TSBAT, or TDIE protections are not used, the functions can be disabled in the register by setting the TSBUS_FLT_DIS, TSBAT_FLT_DIS, or TDIE_FLT_DIS bit to ‘1’.

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TSBUS_TSBAT_ALM_STAT and FLAG is set to ‘1’ unless it is masked by corresponding mask bit when one of the following conditions is met: 1) TSBUS is within 5% of TSBUS_FLT threshold or 2) TSBAT is within of TSBAT_FLT. If the TSBUS_FLT or TSBAT_FLT is disabled, it will not trigger a TSBUS_TSBAT_ALM interrupt. Using the TDIE_ALM register, an alarm can be set to notify the host when the device die temperature exceeds a threshold. The TDIE_ALM_STAT and TDIE_ALM_FLAG bit is set to ‘1’ unless it is masked by TDIE_ALM_MASK bit. The device will not automatically stop switching when reaching the alarm threshold and the host may decide on the steps to take to lower the temperature, such as reducing the charge current.

8.3.11 $\overline{INT}$ Pin, STAT, FLAG, and MASK Registers

The $\overline{INT}$ pin is an open drain pin that needs to be pulled up to a voltage with a pullup resistor. $\overline{INT}$ is normally high and will assert low for t_{INT} when the device needs to alert the host of a fault or status change.

The fields in the STAT registers show the current status of the device, and are updated as the status changes. The fields in the FLAG registers indicate that the event has occurred, and the field is cleared when read. If the event persists after the FLAG register has been read and cleared, another $\overline{INT}$ signal is not sent to prevent host keep receiving interrupts. The fields in the MASK registers allow the user to disable the interrupt on the $\overline{INT}$ pin, but the STAT and FLAG registers are still updated even though $\overline{INT}$ is not pulled low.

8.3.12 Dual Charger Operation Using Primary and Secondary Modes

For higher power systems, it is possible to use two devices in dual charger configuration. This allows each device to operate at lower charging current with higher efficiency compared with single device operating at the same total charging current. The CDRVL_ADDRMS pin is used to configure the functionality of the device as Standalone, Primary or Secondary during POR. Refer to Section 8.3.13 for proper setting. When configured as a primary, the TSBAT_SYNCOUT pin functions as SYNCOUT, and the SRN_SYNCIN pin functions as SRN. When configured as a Secondary, the TSBAT_SYNCOUT pin functions as TSBAT, and the SRN_SYNCIN pin functions as SYNCIN. ACDRV1 and ACDRV2 are controlled by the primary, and ACDRV1 and ACDRV2 on the secondary should be grounded. Pull the SYNCIN/SYNCOUT pins to REGN on the primary BQ25960H through a 1-kΩ resistor. The maximum switching frequency in primary and secondary mode is 500 kHz.

The dual charger can operate in Primary and Secondary Mode in Bypass Mode as well. In both Bypass and Switched Cap Mode, the current distribution between the two devices depends on loop impedance and the chargers do not balance it. In order balance the current, the board layout needs to be as symmetrical as possible.

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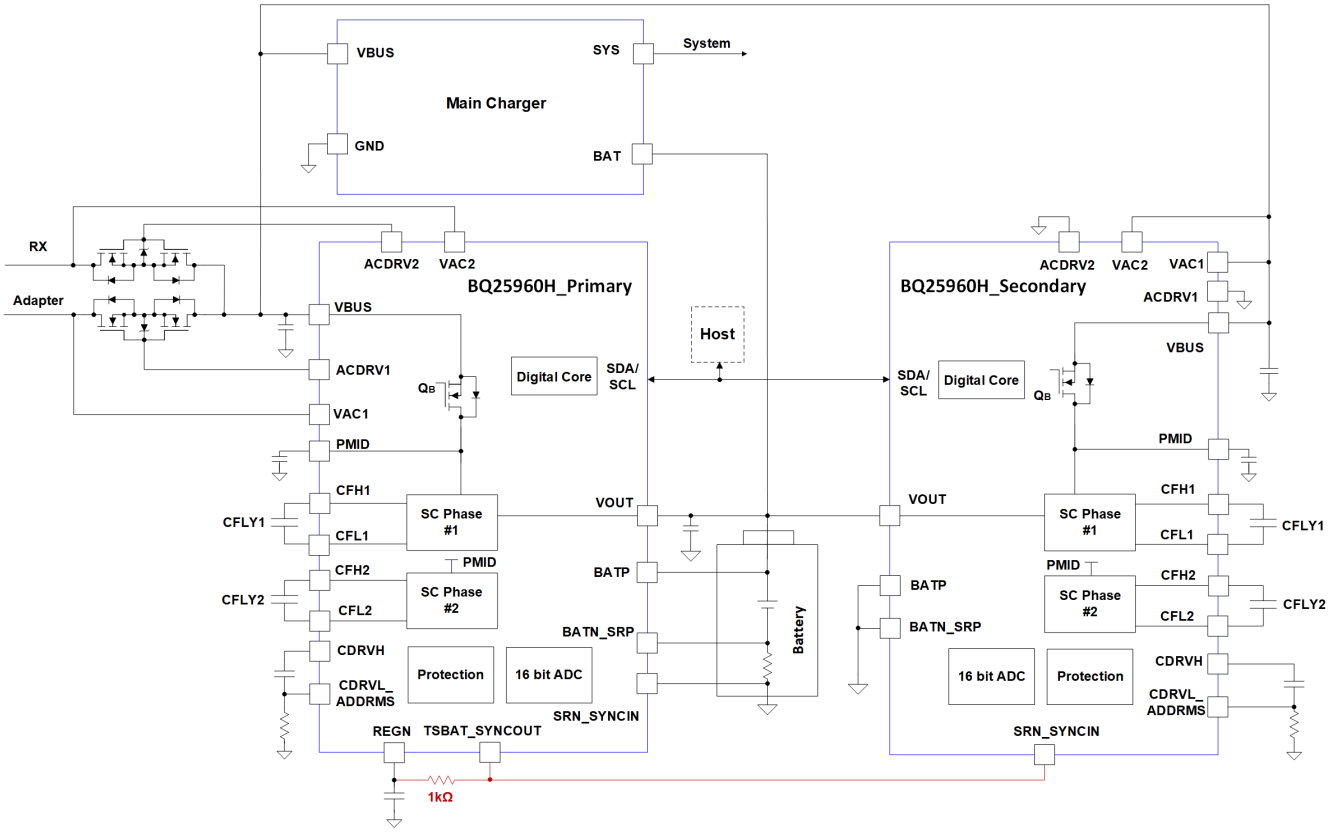

Figure 8-9. Parallel Operation of BQ25960H

8.3.13 CDRVH and CDRVL_ADDRMS Functions

The device requires a cap between the CDRVH and CDRVL_ADDRMS pin to operate correctly. The CDRVL_ADDRMS pin also allows setting the default I²C address and device operation mode. Pull to GND with a resistor for the desired setting shown in Table 8-6. The surface mount resistor with ±1% tolerance is recommended. After POR, the host can read back the device's configuration from MS register (REG12[1:0]).

Table 8-6. I²C Address and Mode Selection

R_{ADDRMS} (kΩ)	I²C ADDRESS	CONFIGURATION
>75.0	0x65	Standalone
6.19	0x67	Standalone
8.06	0x66	Dual charger (Secondary)
10.5	0x66	Dual charger (Primary)
14.0	0x66	Standalone
18.2	0x67	Dual charger (Secondary)
27.4	0x65	Dual charger (Primary)

8.4 Programming

The device uses an I²C compatible interface to program and read many parameters. I²C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor, see I²C BUS Specification, Version 5, October 2012). The BUS consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the BUS is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C BUS through open drain I/O terminals, SDA and SCL. A master device, usually a microcontroller or digital signal processor, controls the BUS. The master is responsible for generating the SCL signal and device addresses. The master

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also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the BUS under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I²C BUS™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery management solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The I²C circuitry is powered from the battery in active battery mode. The battery voltage must stay above VBATUVLO when no VIN is present to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The device only supports 7-bit addressing. The device 7-bit address is determined by the ADDR pin on the device.

8.4.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in the figure below. All I²C-compatible devices should recognize a start condition.

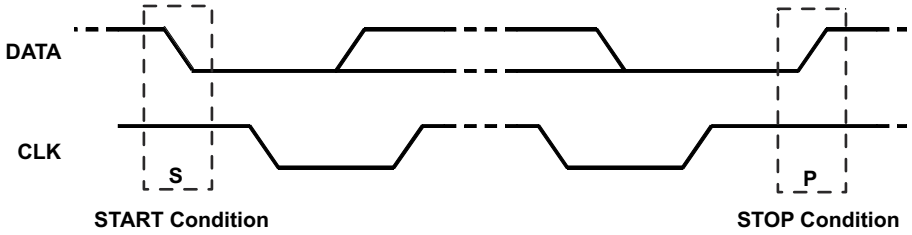

Figure 8-10. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 8-11). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates and acknowledge (see Figure 8-12) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

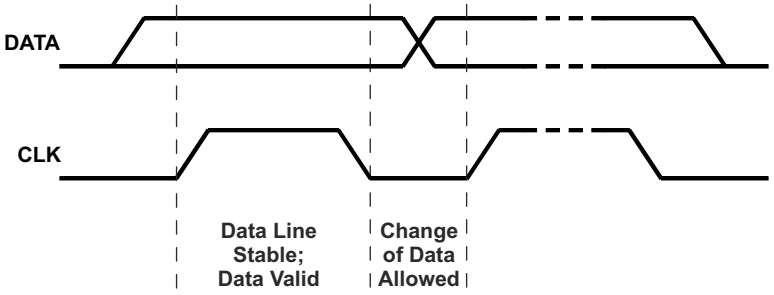

Figure 8-11. Bit Transfer on the Serial Interface

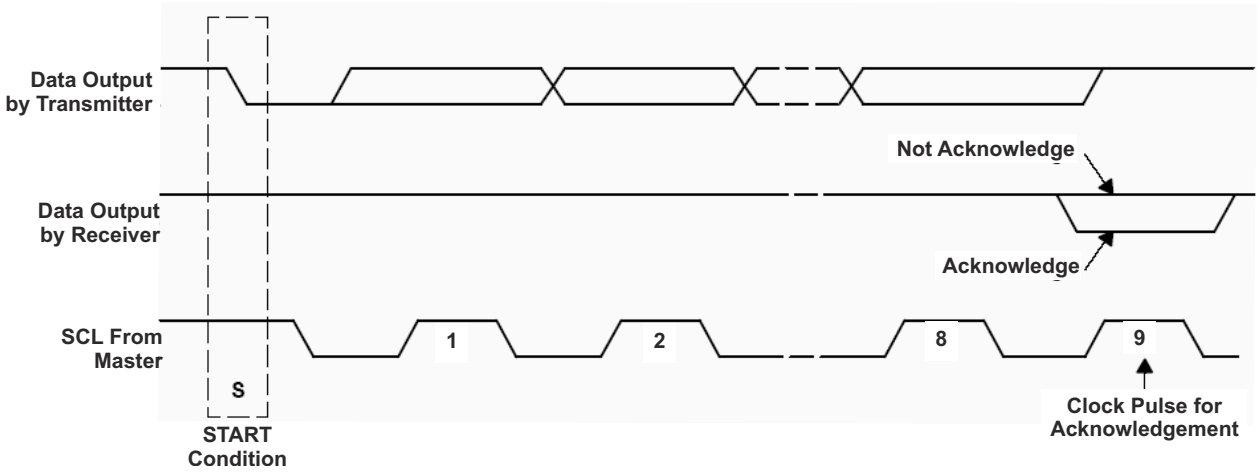

Figure 8-12. Acknowledge on the I²C BUS

The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which on is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 8-13). This releases the BUS and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the BUS is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I²C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section will result in 0xFFh being read out.

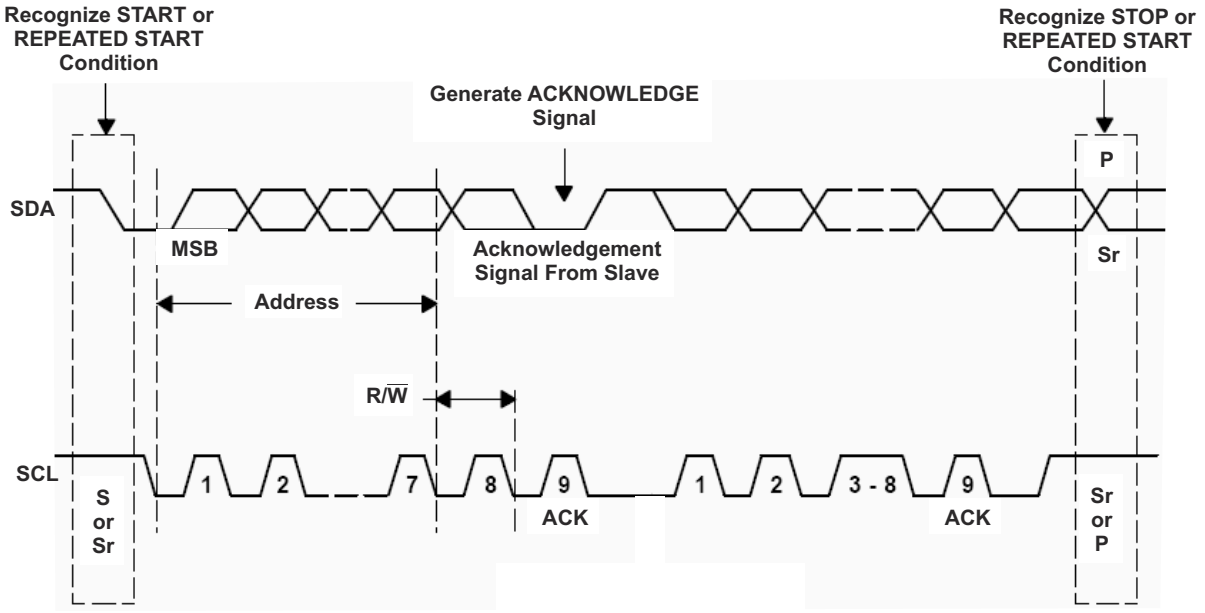

Figure 8-13. BUS Protocol

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8.5 Register Maps

8.5.1 I²C Registers

Table 8-7 lists the I²C registers. All register offset addresses not listed in Table 8-7 should be considered as reserved locations and the register contents should not be modified. All register bits marked 'RESERVED' in Field column should not be modified.

Table 8-7. I²C Registers

Offset	Acronym	Register Name	Section
0h	REG00_BATOVP	BATOVP	Go
1h	REG01_BATOVP_ALM	BATOVP_ALM	Go
2h	REG02_BATOCP	BATOCP	Go
3h	REG03_BATOCP_ALM	BATOCP_ALM	Go
4h	REG04_BATUCP_ALM	BATUCP_ALM	Go
5h	REG05_CHARGER_CONTROL 1	CHARGER_CONTROL 1	Go
6h	REG06_BUSOVP	BUSOVP	Go
7h	REG07_BUSOVP_ALM	BUSOVP_ALM	Go
8h	REG08_BUSOCP	BUSOCP	Go
9h	REG09_BUSOCP_ALM	BUSOCP_ALM	Go
Ah	REG0A_TEMP_CONTROL	TEMP CONTROL	Go
Bh	REG0B_TDIE_ALM	TDIE_ALM	Go
Ch	REG0C_TSBUS_FLT	TSBUS_FLT	Go
Dh	REG0D_TSBAT_FLT	TSBAT_FLT	Go
Eh	REG0E_VAC_CONTROL	VAC CONTROL	Go
Fh	REG0F_CHARGER_CONTROL 2	CHARGER CONTROL 2	Go
10h	REG10_CHARGER_CONTROL 3	CHARGER CONTROL 3	Go
11h	REG11_CHARGER_CONTROL 4	CHARGER CONTROL 4	Go
12h	REG12_CHARGER_CONTROL 5	CHARGER CONTROL 5	Go
13h	REG13_STAT 1	STAT 1	Go
14h	REG14_STAT 2	STAT 2	Go
15h	REG15_STAT 3	STAT 3	Go
16h	REG16_STAT 4	STAT 4	Go
17h	REG17_STAT 5	STAT 5	Go
18h	REG18_FLAG 1	FLAG 1	Go
19h	REG19_FLAG 2	FLAG 2	Go
1Ah	REG1A_FLAG 3	FLAG 3	Go
1Bh	REG1B_FLAG 4	FLAG 4	Go
1Ch	REG1C_FLAG 5	FLAG 5	Go
1Dh	REG1D_MASK 1	MASK 1	Go
1Eh	REG1E_MASK 2	MASK 2	Go
1Fh	REG1F_MASK 3	MASK 3	Go
20h	REG20_MASK 4	MASK 4	Go
21h	REG21_MASK 5	MASK 5	Go
22h	REG22_DEVICE_INFO	DEVICE INFO	Go
23h	REG23_ADC_CONTROL 1	ADC_CONTROL 1	Go
24h	REG24_ADC_CONTROL 2	ADC_CONTROL 2	Go
25h	REG25_IBUS_ADC	IBUS_ADC	Go
27h	REG27_VBUS_ADC	VBUS_ADC	Go
29h	REG29_VAC1_ADC	VAC1_ADC	Go

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Table 8-7. I²C Registers (continued)

Offset	Acronym	Register Name	Section
2Bh	REG2B_VAC2_ADC	VAC2_ADC	Go
2Dh	REG2D_VOUT_ADC	VOUT_ADC	Go
2Fh	REG2F_VBAT_ADC	VBAT_ADC	Go
31h	REG31_IBAT_ADC	IBAT_ADC	Go
33h	REG33_TSBUS_ADC	TSBUS_ADC	Go
35h	REG35_TSBAT_ADC	TSBAT_ADC	Go
37h	REG37_TDIE_ADC	TDIE_ADC	Go

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

Table 8-8. I2C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.5.1.1 REG00_BATOVP Register (Offset = 0h) [reset = 5Ah]

REG00_BATOVP is shown in Table 8-9

Return to the Summary Table.

BATOVP

Table 8-9. REG00_BATOVP Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BATOVP_DIS	R/W	0h	Reset by: REG_RST	Disable BATOVP Type : R/W POR: 0b 0h = Enable 1h = Disable
6-0	BATOVP_6:0	R/W	5Ah	Reset by: REG_RST	Battery Overvoltage Setting. When the battery voltage reaches the programmed threshold, Q_B and switching FETs are turned off and CHG_EN is set to '0'. The host controller should monitor the bus voltage to ensure that the adapter keeps the voltage under the BATOVP threshold for proper operation. Type : R/W POR: 4390 mV (5Ah) Range : 3491 mV - 4759 mV Fixed Offset : 3491 mV Bit Step Size : 9.985 mV

8.5.1.2 REG01_BATOVP_ALM Register (Offset = 1h) [reset = 46h]

REG01_BATOVP_ALM is shown in Table 8-10.

Return to the Summary Table.

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BATOVP_ALM

Table 8-10. REG01_BATOVP_ALM Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BATOVP_ALM_DIS	R/W	0h	Reset by: REG_RST	Disable BATOVP_ALM Type : R/W POR: 0b 0h = Enable 1h = Disable
6-0	BATOVP_ALM_6:0	R/W	46h	Reset by: REG_RST	When battery voltage goes above the programmed threshold, an $\overline{INT}$ is sent. The BATOVP_ALM should be set lower than BATOVP and the host controller should monitor the battery voltage to ensure that the adapter keeps the voltage under BATOVP threshold for proper operation. Type : R/W POR: 4200 mV (46h) Range : 3500 mV - 4770 mV Fixed Offset : 3500 mV Bit Step Size : 10 mV

8.5.1.3 REG02_BATOCP Register (Offset = 2h) [reset = 47h]

REG02_BATOCP is shown in Table 8-11.

Return to the Summary Table.

BATOCP

Table 8-11. REG02_BATOCP Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BATOCP_DIS	R/W	0h	Reset by: REG_RST	Disable BATOCP Type : R/W POR: 0b 0h = Enable 1h = Disable
6-0	BATOCP_6:0	R/W	47h	Reset by: REG_RST	Battery Overcurrent Protection Setting. When battery current reaches the programmed threshold, the Q_B and switching FETs are disabled and CHG_EN is set to '0'. The host controller should monitor the battery current to ensure that the adapter keeps the current under the threshold for proper operation. Type : R/W POR: 7277.5 mA (47h) Range : 2050 mA - 8712.5 mA Fixed Offset : 0 mA Bit Step Size : 102.5 mA

8.5.1.4 REG03_BATOCP_ALM Register (Offset = 3h) [reset = 46h]

REG03_BATOCP_ALM is shown in Table 8-12.

Return to the Summary Table.

BATOCP_ALM

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Table 8-12. REG03_BATOCP_ALM Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BATOCP_ALM_DIS	R/W	0h	Reset by: REG_RST	Disable BATOCP_ALM Type : R/W POR: 0b 0h = Enable 1h = Disable
6-0	BATOCP_ALM_6:0	R/W	46h	Reset by: REG_RST	Battery Overcurrent Alarm Setting. When battery current reaches the programmed threshold, an $\overline{INT}$ is sent. The BATOCP_ALM should be set lower than BATOCP and the host controller should monitor the battery current to ensure that the adapter keeps the current under BATOCP threshold for proper operation. Type : R/W POR: 7000 mA (46h) Range : 0 mA - 12700 mA Fixed Offset : 0 mA Bit Step Size : 100 mA

8.5.1.5 REG04_BATUCP_ALM (Offset = 4h) [reset = 28h]

REG04_BATUCP_ALM is shown in Table 8-13.

Return to the Summary Table.

BATUCP_ALM

Table 8-13. REG04_BATUCP_ALM Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BATUCP_ALM_DIS	R/W	0h	Reset by: REG_RST	Disable BATUCP_ALM Type : R/W POR: 0b 0h = Enable 1h = Disable
6-0	BATUCP_ALM_6:0	R/W	28h	Reset by: REG_RST	Battery Undercurrent Alarm setting. When battery current falls below the programmed threshold, an $\overline{INT}$ is sent. The host controller should monitor the battery current to determine when to disable the device and hand over charging to the main charger. Type : R/W POR: 2000 mA (28h) Range : 0 mA - 4500 mA Fixed Offset : 0 mA Bit Step Size : 50 mA

8.5.1.6 REG05_CHARGER_CONTROL 1 Register (Offset = 5h) [reset = 2h]

REG05_CHARGER_CONTRL 1 is shown in Table 8-14.

Return to the Summary Table.

CHARGER_CONTROL 1

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Table 8-14. REG05_CHARGER_CONTROL 1 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BUSUCP_DIS	R/W	0h	Reset by: REG_RST	Disable BUSUCP Type : R/W POR: 0b 0h = Enable, BUSUCP turns off Q_B and switching FETs, BUSUCP_STAT and FLAG is set to '1', and $\overline{INT}$ is sent to host. 1h = Disable, BUSUCP does not turn off Q_B or switching FETs, but BUSUCP_STAT and FLAG is set to '1', and $\overline{INT}$ is sent to host.
6	BUSUCP	R/W	0h	Reset by: REG_RST	BUSUCP Setting. If input current is below BUSUCP threshold after soft start timer expires, the Q_B and switching FETs are turned off and CHG_EN is set to '0' and $\overline{INT}$ is sent if BUSUCP_DIS=0. If BUSUCP_DIS=1, $\overline{INT}$ is sent to host but converter keeps running. Change this bit to '1' before CHG_EN is set to '1' in order for BUSUCP to be effective. Type : R/W POR: 0b 0h = RESERVED 1h = 250 mA
5	BUSRCP_DIS	R/W	0h	Reset by: REG_RST	Disable BUSRCP Type : R/W POR: 0b 0h = Enable 1h = Disable
4	BUSRCP	R/W	0h	Reset by: REG_RST	BUSRCP Setting, if IBUS is below BUSRCP threshold, the Q_B and switching FETs are turned off and CHG_EN is set to '0' and $\overline{INT}$ is sent. Keep this bit set to '0' in order for BUSRCP to be effective. Type : R/W POR: 0b 0h = 300 mA 1h = RESERVED
3	CHG_CONFIG_1	R/W	0h	Reset by: REG_RST	Charger Configuration 1. Set this bit to '1' before CHG_EN is set to '1'. Type : R/W POR: 0h
2	VBUS_ERRHI_DIS	R/W	0h	Reset by: REG_RST	Disable VBUS_ERRHI Type : R/W POR: 0b 0h = Enable, converter does not switching, but Q_B is turned on when device is in VBUS_ERRHI 1h = Disable, both converter and Q_B is turned on when device is in VBUS_ERRHI
1-0	RESERVED	R/W	2h	Reset by: REG_RST	RESERVED Type : R/W POR: 10b

8.5.1.7 REG06_BUSOVP Register (Offset = 6h) [reset = 26h]

REG06_BUSOVP is shown in Table 8-15.

Return to the Summary Table.

BUSOVP

Table 8-15. REG06_BUSOVP Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BUS_PD_EN	R/W	0h	Reset by: REG_RST	VBUS Pulldown Resistor Control Type : R/W POR: 0b 0h = Disable 1h = Enable
6-0	BUSOVP_6:0	R/W	26h	Reset by: REG_RST	Bus Overvoltage Setting. When the bus voltage reaches the programmed threshold, Q_B and switching FETs are turned off and CHG_EN is set to '0'. The host controller should monitor the bus voltage to ensure that the adapter keeps the voltage under the BUSOVP threshold for proper operation. Switched cap mode: Type : R/W POR: 8900 mV (26h) Range : 7000 mV - 12750 mV Fixed Offset : 7000 mV Bit Step Size : 50 mV Bypass Mode: Type : R/W POR: 4450 mV (26h) Range : 3500 mV - 6500 mV Fixed Offset : 3500 mV Bit Step Size : 25 mV

8.5.1.8 REG07_BUSOVP_ALM Register (Offset = 7h) [reset = 22h]

REG07_BUSOVP_ALM is shown in Table 8-16.

Return to the Summary Table.

BUSOVP_ALM

Table 8-16. REG07_BUSOVP_ALM Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BUSOVP_ALM_DIS	R/W	0h	Reset by: REG_RST	Disable BUSOVP_ALM Type : R/W POR: 0b 0h = Enable 1h = Disable
6-0	BUSOVP_ALM_6:0	R/W	22h	Reset by: REG_RST	Bus Overvoltage Alarm Setting. When the bus voltage reaches the programmed threshold, an $\overline{INT}$ is sent. The host controller should monitor the bus voltage to ensure that the adapter keeps the voltage under the BUSOVP threshold for proper operation. Switched Cap Mode: Type : R/W POR: 8700 mV (22h) Range : 7000 mV - 13350 mV Fixed Offset : 7000 mV Bit Step Size : 50 mV Bypass Mode: Type : R/W POR: 4350 mV (22h) Range : 3500 mV - 6675 mV Fixed Offset : 3500 mV Bit Step Size : 25 mV

8.5.1.9 REG08_BUSOCP Register (Offset = 8h) [reset = Bh]

REG08_BUSOCP is shown in Table 8-17.

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Return to the Summary Table.

BUSOCP

Table 8-17. REG08_BUSOCP Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7-5	RESERVED	R	0h		RESERVED
4-0	BUSOCP_4:0	R/W	Bh	Reset by: REG_RST	BUS Overcurrent Protection Setting. When the bus current reaches the programmed threshold, the output is disabled. The host controller should monitor the bus current to ensure that the adapter keeps the current under this threshold for proper operation. Type : R/W Switched Cap Mode: POR: 3816 mA (Bh) Range: 1017.5 mA - 4579 mA Fixed Offset : 1017.5 mA Bit Step Size : 254 mA Bypass Mode: POR: 3928 mA (Bh) Range: 1047.5 mA - 6809 mA Fixed Offset : 1047.5 mA Bit Step Size : 262 mA

8.5.1.10 REG09_BUSOCP_ALM Register (Offset = 9h) [reset = Ch]

REG09_BUSOCP_ALM is shown in Table 8-18.

Return to the Summary Table.

BUSOCP_ALM

Table 8-18. REG09_BUSOCP_ALM Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BUSOCP_ALM_DIS	R/W	0h	Reset by: REG_RST	Disable BUSOCP_ALM Type : R/W POR: 0b 0h = Enable 1h = Disable
6-5	RESERVED	R	0h		RESERVED
4-0	BUSOCP_ALM_4:0	R/W	Ah	Reset by: REG_RST	Bus Overvoltage Alarm Setting. When the bus current reaches the programmed threshold, an $\overline{INT}$ is sent. The host controller should monitor the bus current to ensure that the adapter keeps the current under the BUSOCP threshold for proper operation. Type : R/W POR: 3500 mA (Ah) Range : 1000 mA - 8750 mA Fixed Offset : 1000 mA Bit Step Size : 250 mA

8.5.1.11 REG0A_TEMP_CONTROL Register (Offset = Ah) [reset = 60h]

REG0A_TEMP_CONTROL is shown in Table 8-19.

Return to the Summary Table.

TEMP_CONTROL

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Table 8-19. REG0A_TEMP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	TDIE_FLT_DIS	R/W	0h	Reset by: REG_RST	Disable TDIE Overtemperature Protection Type : R/W POR: 0b 0h = TDIE_FLT enable 1h = TDIE_FLT disable
6-5	TDIE_FLT_1:0	R/W	3h	Reset by: REG_RST	TDIE Overtemperature Setting. When the junction temperature reaches the programmed threshold, the Q_B and switching FETs are turned off and CHG_EN is set to '0'. Type : R/W POR: 11b 0h = 80C 1h = 100C 2h = 120C 3h = 140C
4	TDIE_ALM_DIS	R/W	0h	Reset by: REG_RST	Disable TDIE Overtemperature Alarm Type : R/W POR: 0b 0h = TDIE_ALM enable 1h = TDIE_ALM disable
3	TSBUS_FLT_DIS	R/W	0h	Reset by: REG_RST	Disable TSBUS_FLT Type : R/W POR: 0b 0h = TSBUS_FLT enable 1h = TSBUS_FLT disable
2	TSBAT_FLT_DIS	R/W	0h	Reset by: REG_RST	Disable TSBAT_FLT Type : R/W POR: 0b 0h = TSBAT_FLT enable 1h = TSBAT_FLT disable
1-0	RESERVED	R	0h		RESERVED Type : R POR: 00b

8.5.1.12 REG0B_TDIE_ALM Register (Offset = Bh) [reset = C8h]

REG0B_TDIE_ALM is shown in Table 8-20.

Return to the Summary Table.

TDIE_ALM

Table 8-20. REG0B_TDIE_ALM Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7-0	TDIE_ALM_7:0	R/W	C8h	Reset by: REG_RST	Die Overtemperature Alarm Setting. When the junction temperature reaches the programmed threshold, an $\overline{INT}$ is sent. Type : R/W POR: 125°C (C8h) Range : 25°C - 150°C Fixed Offset : 25°C Bit Step Size : 0.5°C

8.5.1.13 REG0C_TSBUS_FLT Register (Offset = Ch) [reset = 15h]

REG0C_TSBUS_FLT is shown in Table 8-21.

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Return to the Summary Table.

TSBUS_FLT

Table 8-21. REG0C_TSBUS_FLT Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7-0	TSBUS_FLT_7:0	R/W	15h	Reset by: REG_RST	TSBUS Percentage Fault Threshold. When the TSBUS/REGN ratio drops below the programmed threshold, the Q_B and switching FETs are turned off and CHG_EN is set to '0'. Type : R/W POR: 4.10151% (15h) Range : 0% - 49.8041% Fixed Offset : 0% Bit Step Size : 0.19531%

8.5.1.14 REG0D_TSBAT_FLT Register (Offset = Dh) [reset = 15h]

REG0D_TSBAT_FLG is shown in Table 8-22.

Return to the Summary Table.

TSBAT_FLG

Table 8-22. REG0D_TSBAT_FLT Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7-0	TSBAT_FLT_7:0	R/W	15h	Reset by: REG_RST	TSBAT Percentage Fault Threshold. When the TSBAT/REGN ratio drops below the programmed threshold, the Q_B and switching FETs are turned off and CHG_EN is set to '0'. Type : R/W POR: 4.10151% (15h) Range : 0% - 49.8041% Fixed Offset : 0% Bit Step Size : 0.19531%

8.5.1.15 REG0E_VAC_CONTROL Register (Offset = Eh) [reset = Ch]

REG0E_VAC_CONTROL is shown in Table 8-23.

Return to the Summary Table.

VAC_CONTROL

Table 8-23. REG0E_VAC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7-5	VAC1OVP_2:0	R/W	0h	Reset by: REG_RST	VAC1OVP Setting. When VAC1 voltage reaches the programmed threshold, ACDRV1 is turned off. Type : R/W POR: 000b 0h = 6.5 V 1h = 10.5 V 2h = 12 V 3h = 14 V 4h = 16 V 5h = 18 V

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Table 8-23. REG0E_VAC_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Note	Description
4-2	VAC2OVP_2:0	R/W	3h	Reset by: REG_RST	VAC2OVP Setting. When VAC2 voltage reaches the programmed threshold, ACDRV2 is turned off. Type : R/W POR: 011b 0h = 6.5 V 1h = 10.5 V 2h = 12 V 3h = 14 V 4h = 16 V 5h = 18 V
1	VAC1_PD_EN	R/W	0h	Reset by: REG_RST	Enable VAC1 Pulldown Resistor Type : R/W POR: 0b 0h = Disable 1h = Enable
0	VAC2_PD_EN	R/W	0h	Reset by: REG_RST	Enable VAC2 Pulldown Resistor Type : R/W POR: 0b 0h = Disable 1h = Enable

8.5.1.16 REG0F_CHARGER_CONTROL 2 Register (Offset = Fh) [reset = 0h]

REG0F_CHARGER_CONTROL 2 is shown in Table 8-24.

Return to the Summary Table.

CHARGER CONTROL 2

Table 8-24. REG0F_CHARGER_CONTROL 2 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	REG_RST	R/W	0h	Reset by: REG_RST	Register Reset. Reset registers to default values and reset timer. This bit automatically goes back to '0' after reset. Type : R/W POR: 0b 0h = Not reset register 1h = Reset register
6	EN_HIZ	R/W	0h	Reset by: REG_RST	Enable HIZ Mode. When device is in HIZ mode, converter stops switching, ADC stops converting, ACDRV is turned off and the REGN LDO is forced off. Type : R/W POR: 0b 0h = Disable HIZ mode 1h = Enable HIZ mode
5	EN_OTG	R/W	0h	Reset by: WATCHDOG REG_RST	Power Path Control During the OTG and Reverse TX Mode Type : R/W POR: 0b 0h = Don't allow host to control ACDRV(s) 1h = Allow host to control ACDRV(s)
4	CHG_EN	R/W	0h	Reset by: WATCHDOG REG_RST	Charge Enable Type : R/W POR: 0b 0h = Disable charge 1h = Enable charge

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Table 8-24. REG0F_CHARGER_CONTROL 2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Note	Description
3	EN_BYPASS	R/W	0h	Reset by: WATCHDOG REG_RST	Enable Bypass Mode Type : R/W POR: 0b 0h = Disable Bypass Mode 1h = Enable Bypass Mode
2	DIS_ACDRV_BOTH	R/W	0h		Disable Both ACDRV. When this bit is set, the device forces both ACDRV off. It is not reset by the REG_RST or the WATCHDOG. Type : R/W POR: 0b 0h = ACDRV1 and ACDRV2 can be turned on 1h = ACDRV1 and ACDRV2 are forced off
1	ACDRV1_STAT	R/W	0h		External ACFET1-RBFET1 Gate Driver Status. For dual input with two sets ACFET-RBFET, this bit can be used to swap input. It is not reset by the REG_RST or the WATCHDOG. Type : R/W POR: 0b 0h = ACDRV1 is OFF 1h = ACDRV1 is ON
0	ACDRV2_STAT	R/W	0h		External ACFET2-RBFET2 Gate Driver Status. For dual input with two sets ACFET-RBFET, this bit can be used to swap input. It is not reset by the REG_RST or the WATCHDOG. Type : R/W POR: 0b 0h = ACDRV2 is OFF 1h = ACDRV2 is ON

8.5.1.17 REG10_CHARGER_CONTROL 3 Register (Offset = 10h) [reset = 83h]

REG10_CHARGER_CONTROL 3 is shown in Table 8-25.

Return to the Summary Table.

CHARGER CONTROL 3

Table 8-25. REG10_CHARGER_CONTROL 3 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7-5	FSW_SET_2:0	R/W	4h		Set Switching Frequency in Switched Cap Mode. It is not reset by the REG_RST or the WATCHDOG. Type : R/W POR: 100b 0h = 187.5 kHz 1h = 250 kHz 2h = 300 kHz 3h = 375 kHz 4h = 500 kHz 5h = 750 kHz The maximum switching frequency is 500 kHz in dual charger configuration.
4-3	WATCHDOG_1:0	R/W	0h	Reset by: REG_RST	Watchdog Timer Type : R/W POR: 00b 0h = 0.5 s 1h = 1 s 2h = 5 s 3h = 30 s

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Table 8-25. REG10_CHARGER_CONTROL 3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Note	Description
2	WATCHDOG_DIS	R/W	0h	Reset by: REG_RST	Watchdog Timer Control Type : R/W POR: 0b 0h = Enable 1h = Disable
1-0	RESERVED	R	3h		RESERVED

8.5.1.18 REG11_CHARGER_CONTROL 4 Register (Offset = 11h) [reset = 71h]

REG11_CHARGER_CONTROL 4 is shown in Table 8-26.

Return to the Summary Table.

CHARGER CONTROL 4

Table 8-26. REG11_CHARGER_CONTROL 4 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	RSNS	R/W	0h	Reset by: REG_RST	Battery Current Sense Resistor Value Type : R/W POR: 0b 0h = 2 mΩ 1h = 5 mΩ
6-4	SS_TIMEOUT_2:0	R/W	7h		Soft Start Timeout to Check if Input Current is Above BUSUCP Threshold. It is not reset by the REG_RST or the WATCHDOG. Type : R/W POR: 111b 0h = 6.25 ms 1h = 12.5 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 400 ms 6h = 1.5 s 7h = 10 s
3-2	IBUSUCP_FALL_DG_SEL_1:0	R/W	0h	Reset by: REG_RST	BUSUCP Deglitch Timer Type : R/W POR: 00b 0h = 0.01 ms 1h = 5 ms 2h = 50 ms 3h = 150 ms
1-0	RESERVED	R/W	1h	Reset by: REG_RST	RESERVED Type : R/W POR: 1b

8.5.1.19 REG12_CHARGER_CONTROL 5 Register (Offset = 12h) [reset = 60h]

REG12_CHARGER_CONTROL 5 is shown in Table 8-27.

Return to the Summary Table.

CHARGER CONTROL 5

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Table 8-27. REG12_CHARGER_CONTROL 5 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	VOUTOVP_DIS	R/W	0h	Reset by: REG_RST	Disable VOUTOVP Type : R/W POR: 0b 0h = Enable 1h = Disable
6-5	VOUTOVP_1:0	R/W	3h	Reset by: REG_RST	VOUTOVP Protection. When output voltage is above the programmed threshold, Q_B and switching FETs are turned off and CHG_EN is set to '0'. Type : R/W POR: 11b 0h = 4.7 V 1h = 4.8 V 2h = 4.9 V 3h = 5.0 V
4-3	FREQ_SHIFT_1:0	R/W	0h	Reset by: REG_RST	Adjust Switching Frequency Type : R/W POR: 00b 0h = Nominal switching frequency set in REG10[7:5] 1h = Set switching frequency 10% higher than normal 2h = Set switching frequency 10% lower than normal
2	RESERVED	R/W	0h	Reset by: REG_RST	RESERVED Type : R/W POR: 0b
1-0	MS_1:0	R	0h		Primary, Secondary, Standalone Operation Type : R POR: 00b 0h = Standalone 1h = Secondary 2h = Primary

8.5.1.20 REG13_STAT 1 Register (Offset = 13h) [reset = 0h]

REG13_STAT 1 is shown in Table 8-28.

Return to the Summary Table.

STAT 1

Table 8-28. REG13_STAT 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BATOVP_STAT	R	0h	BATOVP Status Type : R POR: 0b 0h = Not in BATOVP 1h = In BATOVP
6	BATOVP_ALM_STAT	R	0h	BATOVP_ALM Status Type : R POR: 0b 0h = Not in BATOVP_ALM 1h = In BATOVP_ALM
5	VOUTOVP_STAT	R	0h	VOUTOVP Status Type : R POR: 0b 0h = Not in VOUTOVP 1h = in VOUTOVP

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Table 8-28. REG13_STAT 1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	BATOCP_STAT	R	0h	BATOCP Status Type : R POR: 0b 0h = Not in BATOCP 1h = In BATOCP
3	BATOCP_ALM_STAT	R	0h	BATOCP_ALM Status Type : R POR: 0b 0h = Not in BATOCP_ALM 1h = In BATOCP_ALM
2	BATUCP_ALM_STAT	R	0h	BATUCP_ALM Status Type : R POR: 0b 0h = Not in BATUCP_ALM 1h = In BATUCP_ALM
1	BUSOVP_STAT	R	0h	VBUSOVP Status Type : R POR: 0b 0h = Not in VBUS OVP 1h = In VBUS OVP
0	BUSOVP_ALM_STAT	R	0h	BUSOVP_ALM Status Type : R POR: 0b 0h = Not in BUSOVP_ALM 1h = In BUSOVP_ALM

8.5.1.21 REG14_STAT 2 Register (Offset = 14h) [reset = 0h]

REG14_STAT 2 is shown in Table 8-29.

Return to the Summary Table.

STAT 2

Table 8-29. REG14_STAT 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSOCP_STAT	R	0h	BUSOCP Status Type : R POR: 0b 0h = Not in BUSOCP 1h = In BUSOCP
6	BUSOCP_ALM_STAT	R	0h	BUSOCP_ALM Status Type : R POR: 0b 0h = Not in BUSOCP_ALM 1h = In BUSOCP_ALM
5	BUSUCP_STAT	R	0h	BUSUCP Status Type : R POR: 0b 0h = Not in BUSUCP 1h = In BUSUCP
4	BUSRCP_STAT	R	0h	BUSRCP Status Type : R POR: 0b 0h = Not in BUSRCP 1h = In BUSRCP

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Table 8-29. REG14_STAT 2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R	0h	RESERVED
2	CFLY_SHORT_STAT	R	0h	CFLY Short Detection Status Type : R POR: 0b 0h = CFLY not shorted 1h = CFLY shorted
1-0	RESERVED	R	0h	RESERVED

8.5.1.22 REG15_STAT 3 Register (Offset = 15h) [reset = 0h]

REG15_STAT 3 is shown in Table 8-30.

Return to the Summary Table.

STAT 3

Table 8-30. REG15_STAT 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VAC1OVP_STAT	R	0h	VAC1 OVP Status Type : R POR: 0b 0h = Not in VAC1 OVP 1h = In VAC1 OVP
6	VAC2OVP_STAT	R	0h	VAC2 OVP Status Type : R POR: 0b 0h = Not in VAC2 OVP 1h = In VAC2 OVP
5	VOUTPRESENT_STAT	R	0h	VOUT Present Status Type : R POR: 0b 0h = VOUT not present 1h = VOUT present
4	VAC1PRESENT_STAT	R	0h	VAC1 Present Status Type : R POR: 0b 0h = VAC1 not present 1h = VAC1 present
3	VAC2PRESENT_STAT	R	0h	VAC2 Present Status Type : R POR: 0b 0h = VAC2 not present 1h = VAC2 present
2	VBUSPRESENT_STAT	R	0h	VBUS Present Status Type : R POR: 0b 0h = VBUS not present 1h = VBUS present
1	ACRB1_CONFIG_STAT	R	0h	ACFET1-RBFET1 Status Type : R POR: 0b 0h = ACFET1-RBFET1 is not placed 1h = ACFET1-RBFET1 is placed

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Table 8-30. REG15_STAT 3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ACRB2_CONFIG_STAT	R	0h	ACFET2-RBFET2 Status Type : R POR: 0b 0h = ACFET2-RBFET2 is not placed 1h = ACFET2-RBFET2 is placed

8.5.1.23 REG16_STAT 4 Register (Offset = 16h) [reset = 0h]

REG16_STAT 4 is shown in Table 8-31.

Return to the Summary Table.

STAT 4

Table 8-31. REG16_STAT 4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_DONE_STAT	R	0h	ADC Conversion Status (in One-Shot Mode only) Note: Always reads 0 in continuous mode Type : R POR: 0b 0h = Conversion not complete 1h = Conversion complete
6	SS_TIMEOUT_STAT	R	0h	Soft-Start Timeout Status Type : R POR: 0b 0h = Device not in soft timeout 1h = Device in soft timeout
5	TSBUS_TSBAT_ALM_STAT	R	0h	TSBUS and TSBAT ALM Status Type : R POR: 0b 0h = TSBUS or TSBAT threshold is NOT within 5% of the TSBUS_FLT or TSBAT_FLT set threshold 1h = TSBUS or TSBAT threshold is within 5% of the TSBUS_FLT or TSBAT_FLT set threshold
4	TSBUS_FLT_STAT	R	0h	TSBUS_FLT Status Type : R POR: 0b 0h = Not in TSBUS_FLT 1h = In TSBUS_FLT
3	TSBAT_FLT_STAT	R	0h	TSBAT_FLT Status Type : R POR: 0b 0h = Not in TSBAT_FLT 1h = In TSBAT_FLT
2	TDIE_FLT_STAT	R	0h	TDIE Fault Status Type : R POR: 0b 0h = Not in TDIE fault 1h = In TDIE fault
1	TDIE_ALM_STAT	R	0h	TDIE_ALM Status Type : R POR: 0b 0h = Not in TDIE_ALM 1h = In TDIE_ALM

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Table 8-31. REG16_STAT 4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WD_STAT	R	0h	I²C Watch Dog Status Type : R POR: 0b 0h = Normal 1h = WD timer expired

8.5.1.24 REG17_STAT 5 Register (Offset = 17h) [reset = 0h]

REG17_STAT 5 is shown in Table 8-32.

Return to the Summary Table.

STAT 5

Table 8-32. REG17_STAT 5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REGN_GOOD_STAT	R	0h	REGN_GOOD Status Type : R POR: 0b 0h = REGN not good 1h = REGN good
6	CONV_ACTIVE_STAT	R	0h	Converter Active Status Type : R POR: 0b 0h = Converter not running 1h = Converter running
5	RESERVED	R	0h	RESERVED
4	VBUS_ERRHI_STAT	R	0h	VBUS_ERRHI Status Type : R POR: 0b 0h = Not in VBUS_ERRHI status 1h = In VBUS_ERRHI status
3-0	RESERVED	R	0h	RESERVED

8.5.1.25 REG18_FLAG 1 Register (Offset = 18h) [reset = 0h]

REG18_FLAG 1 is shown in Table 8-33.

Return to the Summary Table.

FLAG 1

Table 8-33. REG18_FLAG 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BATOVP_FLAG	R	0h	BATOVP Flag Type : R POR: 0b 0h = Normal 1h = BATOVP status changed
6	BATOVP_ALM_FLAG	R	0h	BATOVP_ALM Flag Type : R POR: 0b 0h = Normal 1h = BATOVP_ALM status changed

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Table 8-33. REG18_FLAG 1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	VOUTOVP_FLAG	R	0h	VOUTOVP Flag Type : R POR: 0b 0h = Normal 1h = VOUTOVP status changed
4	BATOCP_FLAG	R	0h	BATOCP Flag Type : R POR: 0b 0h = Normal 1h = BATOCP status changed
3	BATOCP_ALM_FLAG	R	0h	BATOCP_ALM Flag Type : R POR: 0b 0h = Normal 1h = BATOCP_ALM status changed
2	BATUCP_ALM_FLAG	R	0h	BATUCP_ALM Flag Type : R POR: 0b 0h = Normal 1h = BATUCP_ALM status changed
1	BUSOVP_FLAG	R	0h	BUSOVP Flag Type : R POR: 0b 0h = Normal 1h = BUSOVP status changed
0	BUSOVP_ALM_FLAG	R	0h	BUSOVP_ALM Flag Type : R POR: 0b 0h = Normal 1h = BUSOVP_ALM status changed

8.5.1.26 REG19_FLAG 2 Register (Offset = 19h) [reset = 0h]

REG19_FLAG 2 is shown in Table 8-34.

Return to the Summary Table.

FLAG 2

Table 8-34. REG19_FLAG 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSOCP_FLAG	R	0h	BUSOCP Flag Type : R POR: 0b 0h = Normal 1h = BUSOCP status changed
6	BUSOCP_ALM_FLAG	R	0h	BUSOCP_ALM Flag Type : R POR: 0b 0h = Normal 1h = BUSOCP_ALM status changed
5	BUSUCP_FLAG	R	0h	BUSUCP Flag Type : R POR: 0b 0h = Normal 1h = BUSUCP status changed

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Table 8-34. REG19_FLAG 2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	BUSRCP_FLAG	R	0h	BUSRCP Flag Type : R POR: 0b 0h = Normal 1h = BUSRCP status changed
3	RESERVED	R	0h	RESERVED
2	CFLY_SHORT_FLAG	R	0h	CFLY Short Flag Type : R POR: 0b 0h = Normal 1h = CFLY_SHORT status changed
1-0	RESERVED	R	0h	RESERVED

8.5.1.27 REG1A_FLAG 3 Register (Offset = 1Ah) [reset = 0h]

REG1A_FLAG 3 is shown in Table 8-35.

Return to the Summary Table.

FLAG 3

Table 8-35. REG1A_FLAG 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VAC1OVP_FLAG	R	0h	VAC1OVP Flag Type : R POR: 0b 0h = Normal 1h = VAC1 OVP status changed
6	VAC2OVP_FLAG	R	0h	VAC2OVP Flag Type : R POR: 0b 0h = Normal 1h = VAC2 OVP status changed
5	VOUTPRESENT_FLAG	R	0h	VOUT Present Flag Type : R POR: 0b 0h = Normal 1h = VOUT present status changed
4	VAC1PRESENT_FLAG	R	0h	VAC1 Present Flag Type : R POR: 0b 0h = Normal 1h = VAC1 present status changed
3	VAC2PRESENT_FLAG	R	0h	VAC2 Present Flag Type : R POR: 0b 0h = Normal 1h = VAC2 present status changed
2	VBUSPRESENT_FLAG	R	0h	VBUS Present Flag Type : R POR: 0b 0h = Normal 1h = VBUS present status changed

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Table 8-35. REG1A_FLAG 3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ACRB1_CONFIG_FLAG	R	0h	ACFET1-RBFET1_CONFIG Flag Type : R POR: 0b 0h = Normal 1h = ACFET1-RBFET1_CONFIG status changed
0	ACRB2_CONFIG_FLAG	R	0h	ACFET2-RBFET2_CONFIG Flag Type : R POR: 0b 0h = Normal 1h = ACFET2-RBFET2_CONFIG status changed

8.5.1.28 REG1B_FLAG 4 Register (Offset = 1Bh) [reset = 0h]

REG1B_FLAG 4 is shown in Table 8-36.

Return to the Summary Table.

FLAG 4

Table 8-36. REG1B_FLAG 4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_DONE_FLAG	R	0h	ADC Conversion Flag (in One-Shot Mode only) Type : R POR: 0b 0h = Normal 1h = ADC conversion done status changed
6	SS_TIMEOUT_FLAG	R	0h	Soft-Start Timeout Flag Type : R POR: 0b 0h = Normal 1h = Soft start timeout status changed
5	TSBUS_TSBAT_ALM_FLAG	R	0h	TSBUS_TSBAT_ALM Flag Type : R POR: 0b 0h = Normal 1h = Converter active status changed
4	TSBUS_FLT_FLAG	R	0h	TSBUS_FLT Flag Type : R POR: 0b 0h = Normal 1h = TSBUS_FLT status changed
3	TSBAT_FLT_FLAG	R	0h	TSBAT_FLT Flag Type : R POR: 0b 0h = Normal 1h = TSBAT_FLT status changed
2	TDIE_FLT_FLAG	R	0h	TDIE_FLT Flag Type : R POR: 0b 0h = Normal 1h = TDIE_FLT status changed
1	TDIE_ALM_FLAG	R	0h	TDIE_ALM Flag Type : R POR: 0b 0h = Normal 1h = TDIE_ALM status changed

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Table 8-36. REG1B_FLAG 4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WD_FLAG	R	0h	I²C Watch Dog Timer Flag Type : R POR: 0b 0h = Normal 1h = WD timer status changed

8.5.1.29 REG1C_FLAG 5 Register (Offset = 1Ch) [reset = 0h]

REG1C_FLAG 5 is shown in Table 8-37.

Return to the Summary Table.

FLAG 5

Table 8-37. REG1C_FLAG 5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REGN_GOOD_FLAG	R	0h	REGN_GOOD Flag Type : R POR: 0b 0h = Normal 1h = REGN_GOOD status changed
6	CONV_ACTIVE_FLAG	R	0h	Converter Active Flag Type : R POR: 0b 0h = Normal 1h = Converter active status changed
5	RESERVED	R	0h	RESERVED
4	VBUS_ERRHI_FLAG	R	0h	VBUS_ERRHI Flag Type : R POR: 0b 0h = Normal 1h = VBUS_ERRHI status changed
3-0	RESERVED	R	0h	RESERVED

8.5.1.30 REG1D_MASK 1 Register (Offset = 1Dh) [reset = 0h]

REG1D_MASK 1 is shown in Table 8-38.

Return to the Summary Table.

MASK 1

Table 8-38. REG1D_MASK 1 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BATOVP_MASK	R/W	0h	Reset by: REG_RST	BATOVP Mask Type : R/W POR: 0b 0h = BATOVP flag produce $\overline{INT}$ 1h = BATOVP flag does not produce $\overline{INT}$
6	BATOVP_ALM_MASK	R/W	0h	Reset by: REG_RST	BATOVP_ALM Mask Type : R/W POR: 0b 0h = BATOVP_ALM flag produce $\overline{INT}$ 1h = BATOVP _ALM flag does not produce $\overline{INT}$

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Table 8-38. REG1D_MASK 1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Note	Description
5	VOUTOVP_MASK	R/W	0h	Reset by: REG_RST	VOUTOVP Mask Type : R/W POR: 0b 0h = VOUTOVP flag produce $\overline{INT}$ 1h = VOUTOVP flag does not produce $\overline{INT}$
4	BATOCP_MASK	R/W	0h	Reset by: REG_RST	BATOCP Mask Type : R/W POR: 0b 0h = BATOCP flag produce $\overline{INT}$ 1h = BATOCP flag does not produce $\overline{INT}$
3	BATOCP_ALM_MASK	R/W	0h	Reset by: REG_RST	BATOCP_ALM Mask Type : R/W POR: 0b 0h = BATOCP_ALM flag produce $\overline{INT}$ 1h = BATOCP_ALM flag does not produce $\overline{INT}$
2	BATUCP_ALM_MASK	R/W	0h	Reset by: REG_RST	BATUCP_ALM Mask Type : R/W POR: 0b 0h = BATUCP_ALM flag produce $\overline{INT}$ 1h = BATUCP_ALM flag does not produce $\overline{INT}$
1	BUSOVP_MASK	R/W	0h	Reset by: REG_RST	BUSOVP Mask Type : R/W POR: 0b 0h = BUSOVP flag produce $\overline{INT}$ 1h = BUSOVP flag does not produce $\overline{INT}$
0	BUSOVP_ALM_MASK	R/W	0h	Reset by: REG_RST	BUSOVP_ALM Mask Type : R/W POR: 0b 0h = BUSOVP_ALM flag produce $\overline{INT}$ 1h = BUSOVP_ALM flag does not produce $\overline{INT}$

8.5.1.31 REG1E_MASK 2 Register (Offset = 1Eh) [reset = 0h]

REG1E_MASK 2 is shown in Table 8-39.

Return to the Summary Table.

MASK 2

Table 8-39. REG1E_MASK 2 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	BUSOCP_MASK	R/W	0h	Reset by: REG_RST	BUSOCP Mask Type : R/W POR: 0b 0h = BUSOCP flag produce $\overline{INT}$ 1h = BUSOCP flag does not produce $\overline{INT}$
6	BUSOCP_ALM_MASK	R/W	0h	Reset by: REG_RST	BUSOCP_ALM Mask Type : R/W POR: 0b 0h = BUSOCP_ALM flag produce $\overline{INT}$ 1h = BUSOCP_ALM flag does not produce $\overline{INT}$
5	BUSUCP_MASK	R/W	0h	Reset by: REG_RST	BUSUCP Mask Type : R/W POR: 0b 0h = BUSUCP flag produce $\overline{INT}$ 1h = BUSUCP flag does not produce $\overline{INT}$

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Table 8-39. REG1E_MASK 2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Note	Description
4	BUSRCP_MASK	R/W	0h	Reset by: REG_RST	BUSRCP Mask Type : R/W POR: 0b 0h = BUSRCP flag produce $\overline{INT}$ 1h = BUSRCP flag does not produce $\overline{INT}$
3	RESERVED	R/W	0h	Reset by: REG_RST	RESERVED
2	CFLY_SHORT_MASK	R/W	0h	Reset by: REG_RST	CFLY_SHORT Mask Type : R/W POR: 0b 0h = CFLY_SHORT flag produce $\overline{INT}$ 1h = CFLY_SHORT flag does not produce $\overline{INT}$
1	RESERVED	R/W	0h	Reset by: REG_RST	RESERVED Type : R/W POR: 0h
0	RESERVED	R	0h		RESERVED

8.5.1.32 REG1F_MASK 3 Register (Offset = 1Fh) [reset = 0h]

REG1F_MASK 3 is shown in Table 8-40.

Return to the Summary Table.

MASK 3

Table 8-40. REG1F_MASK 3 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	VAC1OVP_MASK	R/W	0h	Reset by: REG_RST	VAC1OVP Mask Type : R/W POR: 0b 0h = VAC1OVP flag produce $\overline{INT}$ 1h = VAC1OVP flag does not produce $\overline{INT}$
6	VAC2OVP_MASK	R/W	0h	Reset by: REG_RST	VAC2OVP Mask Type : R/W POR: 0b 0h = VAC2OVP flag produce $\overline{INT}$ 1h = VAC2OVP flag does not produce $\overline{INT}$
5	VOUTPRESENT_MASK	R/W	0h	Reset by: REG_RST	VOUTPRESENT Mask Type : R/W POR: 0b 0h = VOUTPRESENT flag produce $\overline{INT}$ 1h = VOUTPRESENT flag does not produce $\overline{INT}$
4	VAC1PRESENT_MASK	R/W	0h	Reset by: REG_RST	VAC1PRESENT Mask Type : R/W POR: 0b 0h = VAC1PRESENT flag produce $\overline{INT}$ 1h = VAC1PRESENT flag does not produce $\overline{INT}$
3	VAC2PRESENT_MASK	R/W	0h	Reset by: REG_RST	VAC2PRESENT Mask Type : R/W POR: 0b 0h = VAC2PRESENT flag produce $\overline{INT}$ 1h = VAC2PRESENT flag does not produce $\overline{INT}$

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Table 8-40. REG1F_MASK 3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Note	Description
2	VBUSPRESENT_MASK	R/W	0h	Reset by: REG_RST	VBUSPRESENT Mask Type : R/W POR: 0b 0h = VBUSPRESENT flag produce $\overline{INT}$ 1h = VBUSPRESENT flag does not produce $\overline{INT}$
1	ACRB1_CONFIG_MASK	R/W	0h	Reset by: REG_RST	ACFET1-RBFET1 CONFIG Mask Type : R/W POR: 0b 0h = ACRB1_CONFIG flag produce $\overline{INT}$ 1h = ACRB1_CONFIG flag does not produce $\overline{INT}$
0	ACRB2_CONFIG_MASK	R/W	0h	Reset by: REG_RST	ACFET2-RBFET2 CONFIG Mask Type : R/W POR: 0b 0h = ACRB2_CONFIG flag produce $\overline{INT}$ 1h = ACRB2_CONFIG flag does not produce $\overline{INT}$

8.5.1.33 REG20_MASK 4 Register (Offset = 20h) [reset = 0h]

REG20_MASK 4 is shown in Table 8-41.

Return to the Summary Table.

MASK 4

Table 8-41. REG20_MASK 4 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	ADC_DONE_MASK	R/W	0h	Reset by: REG_RST	ADC_DONE Mask Type : R/W POR: 0b 0h = ADC_DONE flag produce $\overline{INT}$ 1h = ADC_DONE flag does not produce $\overline{INT}$
6	SS_TIMEOUT_MASK	R/W	0h	Reset by: REG_RST	SS_TIMEOUT Mask Type : R/W POR: 0b 0h = SS_TIMEOUT flag produce $\overline{INT}$ 1h = SS_TIMEOUT flag does not produce $\overline{INT}$
5	TSBUS_TSBAT_ALM_MASK	R/W	0h	Reset by: REG_RST	TSBUS_TSBAT_ALM Mask Type : R/W POR: 0b 0h = TSBUS_TSBAT_ALM flag produce $\overline{INT}$ 1h = TSBUS_TSBAT_ALM flag does not produce $\overline{INT}$
4	TSBUS_FLT_MASK	R/W	0h	Reset by: REG_RST	TSBUS_FLT Mask Type : R/W POR: 0b 0h = TSBUS_FLT flag produce $\overline{INT}$ 1h = TSBUS_FLT flag does not produce $\overline{INT}$
3	TSBAT_FLT_MASK	R/W	0h	Reset by: REG_RST	TSBAT_FLT Mask Type : R/W POR: 0b 0h = TSBAT_FLT flag produce $\overline{INT}$ 1h = TSBAT_FLT flag does not produce $\overline{INT}$
2	TDIE_FLT_MASK	R/W	0h	Reset by: REG_RST	TDIE_FLT Mask Type : R/W POR: 0b 0h = TDIE_FLT flag produce $\overline{INT}$ 1h = TDIE_FLT flag does not produce $\overline{INT}$

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Table 8-41. REG20_MASK 4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Note	Description
1	TDIE_ALM_MASK	R/W	0h	Reset by: REG_RST	TDIE_ALM Mask Type : R/W POR: 0b 0h = TDIE_ALM flag produce $\overline{INT}$ 1h = TDIE_ALM flag does not produce $\overline{INT}$
0	WD_MASK	R/W	0h	Reset by: REG_RST	Watchdog Mask Type : R/W POR: 0b 0h = WD flag produce $\overline{INT}$ 1h = WD flag does not produce $\overline{INT}$

8.5.1.34 REG21_MASK 5 Register (Offset = 21h) [reset = 0h]

REG21_MASK 5 is shown in Table 8-42.

Return to the Summary Table.

MASK 5

Table 8-42. REG21_MASK 5 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	REGN_GOOD_MASK	R/W	0h	Reset by: REG_RST	REGN_GOOD Mask Type : R/W POR: 0b 0h = REGN_GOOD flag produce $\overline{INT}$ 1h = REGN_GOOD flag does not produce $\overline{INT}$
6	CONV_ACTIVE_MASK	R/W	0h	Reset by: REG_RST	CONV_ACTIVE Mask Type : R/W POR: 0b 0h = CONV_ACTIVE flag produce $\overline{INT}$ 1h = CONV_ACTIVE flag does not produce $\overline{INT}$
5	RESERVED	R/W	0h	Reset by: REG_RST	RESERVED Type : R/W POR: 0h
4	VBUS_ERRHI_MASK	R/W	0h	Reset by: REG_RST	VBUS_ERRHI Mask Type : R/W POR: 0b 0h = VBUS_ERRHI flag produce $\overline{INT}$ 1h = VBUS_ERRHI flag does not produce $\overline{INT}$
3-0	RESERVED	R	0h		RESERVED

8.5.1.35 REG22_DEVICE_INFO Register (Offset = 22h) [reset = 0h]

REG22_DEVICE_INFO is shown in Table 8-43.

Return to the Summary Table.

DEVICE INFO

Table 8-43. REG22_DEVICE_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DEVICE_REV_3:0	R	0h	Device Revision Type : R POR: 0h

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Table 8-43. REG22_DEVICE_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DEVICE_ID_3:0	R	0h	Device ID Type : R POR: 0h

8.5.1.36 REG23_ADC_CONTROL 1 Register (Offset = 23h) [reset = 0h]

REG23_ADC_CONTROL 1 is shown in Table 8-44.

Return to the Summary Table.

ADC_CONTROL 1

Table 8-44. REG23_ADC_CONTROL 1 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	ADC_EN	R/W	0h	Reset by: WATCHDOG REG_RST	ADC Enable Type : R/W POR: 0b 0h = Disable 1h = Enable
6	ADC_RATE	R/W	0h	Reset by: REG_RST	ADC Rate Type : R/W POR: 0b 0h = Continuous conversion 1h = 1 shot
5	ADC_AVG	R/W	0h	Reset by: REG_RST	ADC Average Type : R/W POR: 0b 0h = Single value 1h = Running average
4	ADC_AVG_INIT	R/W	0h	Reset by: REG_RST	ADC Average Initial Value Type : R/W POR: 0b 0h = Start average using the existing register value 1h = Start average using a new conversion
3-2	ADC_SAMPLE_1:0	R/W	0h	Reset by: REG_RST	ADC Sample Speed Type : R/W POR: 00b 0h = 15 bit 1h = 14 bit 2h = 13 bit 3h = 11 bit
1	IBUS_ADC_DIS	R/W	0h	Reset by: REG_RST	IBUS ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
0	VBUS_ADC_DIS	R/W	0h	Reset by: REG_RST	VBUS ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable

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8.5.1.37 REG24_ADC_CONTROL 2 Register (Offset = 24h) [reset = 0h]

REG24_ADC_CONTROL 2 is shown in Table 8-45.

Return to the Summary Table.

ADC_CONTROL 2

Table 8-45. REG24_ADC_CONTROL 2 Register Field Descriptions

Bit	Field	Type	Reset	Note	Description
7	VAC1_ADC_DIS	R/W	0h	Reset by: REG_RST	VAC1 ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
6	VAC2_ADC_DIS	R/W	0h	Reset by: REG_RST	VAC2 ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
5	VOUT_ADC_DIS	R/W	0h	Reset by: REG_RST	VOUT ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
4	VBAT_ADC_DIS	R/W	0h	Reset by: REG_RST	VBAT ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
3	IBAT_ADC_DIS	R/W	0h	Reset by: REG_RST	IBAT ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
2	TSBUS_ADC_DIS	R/W	0h	Reset by: REG_RST	TSBUS ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
1	TSBAT_ADC_DIS	R/W	0h	Reset by: REG_RST	TSBAT ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable
0	TDIE_ADC_DIS	R/W	0h	Reset by: REG_RST	TDIE ADC Control Type : R/W POR: 0b 0h = Enable 1h = Disable

8.5.1.38 REG25_IBUS_ADC Register (Offset = 25h) [reset = 0h]

REG25_IBUS_ADC is shown in Table 8-46.

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IBUS_ADC

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Table 8-46. REG25_IBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IBUS_ADC_15:0	R	0h	IBUS ADC Reading Type : R POR: 0 mA (0h) Range : 0 mA - 7000 mA Switched Cap Mode: Fixed Offset : 66 mA Bit Step Size : 0.9972 mA Bypass Mode: Fixed Offset : 64 mA Bit Step Size : 1.0279 mA

8.5.1.39 REG27_VBUS_ADC Register (Offset = 27h) [reset = 0h]

REG27_VBUS_ADC is shown in Table 8-47.

Return to the Summary Table.

VBUS_ADC

Table 8-47. REG27_VBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBUS_ADC_15:0	R	0h	VBUS ADC Reading Type : R POR: 0 mV (0h) Range : 0 mV - 16385 mV Fixed Offset : 0 mV Bit Step Size : 1.002 mV

8.5.1.40 REG29_VAC1_ADC Register (Offset = 29h) [reset = 0h]

REG29_VAC1_ADC is shown in Table 8-48.

Return to the Summary Table.

VAC1_ADC

Table 8-48. REG29_VAC1_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VAC1_ADC_15:0	R	0h	VAC1 ADC Reading Type : R POR: 0 mV (0h) Range : 0 mV - 14000 mV Fixed Offset : 3 mV Bit Step Size : 1.0008 mV

8.5.1.41 REG2B_VAC2_ADC Register (Offset = 2Bh) [reset = 0h]

REG2B_VAC2_ADC is shown in Table 8-49.

Return to the Summary Table.

VAC2_ADC

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Table 8-49. REG2B_VAC2_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VAC2_ADC_15:0	R	0h	VAC2 ADC Reading Type : R POR: 0 mV (0h) Range : 0 mV - 14000 mV Fixed Offset : 5 mV Bit Step Size : 1.0006 mV

8.5.1.42 REG2D_VOUT_ADC Register (Offset = 2Dh) [reset = 0h]

REG2D_VOUT_ADC is shown in Table 8-50.

Return to the Summary Table.

VOUT_ADC

Table 8-50. REG2D_VOUT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VOUT_ADC_15:0	R	0h	VOUT ADC Reading Type : R POR: 0 mV (0h) Range : 0 mV - 6000 mV Fixed Offset : 2 mV Bit Step Size : 1.0037 mV

8.5.1.43 REG2F_VBAT_ADC Register (Offset = 2Fh) [reset = 0h]

REG2F_VBAT_ADC is shown in Table 8-51.

Return to the Summary Table.

VBAT_ADC

Table 8-51. REG2F_VBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBAT_ADC_15:0	R	0h	VBAT ADC Reading Type : R POR: 0 mV (0h) Range : 0 mV - 6000 mV Fixed Offset : 1 mV Bit Step Size : 1.0017 mV

8.5.1.44 REG31_IBAT_ADC Register (Offset = 31h) [reset = 0h]

REG31_IBAT_ADC is shown in Table 8-52.

Return to the Summary Table.

IBAT_ADC

Table 8-52. REG31_IBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IBAT_ADC_15:0	R	0h	IBAT ADC Reading Type : R POR: 0 mA (0h) Range : 0 mA - 12000 mA Fixed Offset : -150 mA Bit Step Size : 0.999 mA

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8.5.1.45 REG33_TSBUS_ADC Register (Offset = 33h) [reset = 0h]

REG33_TSBUS_ADC is shown in Table 8-53.

Return to the Summary Table.

TSBUS_ADC

Table 8-53. REG33_TSBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TSBUS_ADC_15:0	R	0h	TSBUS ADC Reading Type : R POR: 0% (0h) Range : 0% - 50% Fixed Offset : 0.1% Bit Step Size : 0.09860%

8.5.1.46 REG35_TSBAT_ADC Register (Offset = 35h) [reset = 0h]

REG35_TSBAT_ADC is shown in Table 8-54.

Return to the Summary Table.

TSBAT_ADC

Table 8-54. REG35_TSBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TSBAT_ADC_15:0	R	0h	TSBAT ADC Reading Type : R POR: 0% (0h) Range : 0% - 50% Fixed Offset : 0.065% Bit Step Size : 0.09762%

8.5.1.47 REG37_TDIE_ADC Register (Offset = 37h) [reset = 0h]

REG37_TDIE_ADC is shown in Table 8-55.

Return to the Summary Table.

TDIE_ADC

Table 8-55. REG37_TDIE_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TDIE_ADC_15:0	R	0h	TDIE ADC Reading Type : R POR: 0°C (0h) Range : -40°C - 150°C Fixed Offset : -3.5°C Bit Step Size : 0.5079°C

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I^2C controlled parallel charger along with a standard switching charger, however, it can also be used with a linear charger or PMIC with integrated charger as well. BQ25960H can start fast charging after the main charger completes pre-charging. BQ25960H will then hand back charging to the main charger when final current tapering is desired. This point is usually where the efficiency of the main charger is acceptable for the application. The device can be used to charge Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. To take advantage of the high charge current capabilities of the BQ25960H, it may be necessary to charge in excess of 1C. In this case, be sure to follow the battery manufacturers recommendations closely.

9.2 Typical Application

A typical schematic is shown below with all the optional and required components shown.

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9.2.1 Standalone Application Information (for use with main charger)

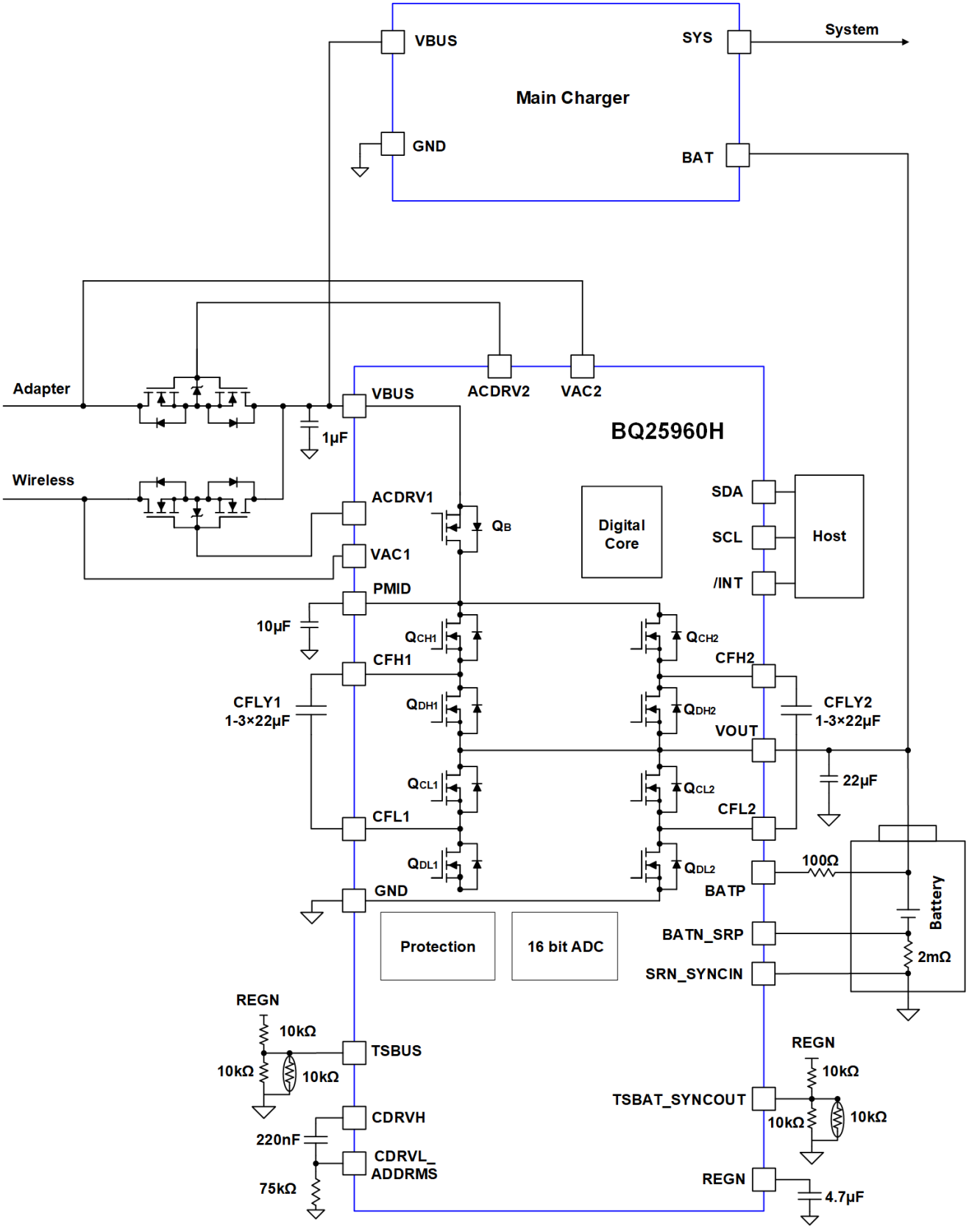

Figure 9-1. BQ25960H Typical Application Diagram with Dual Input

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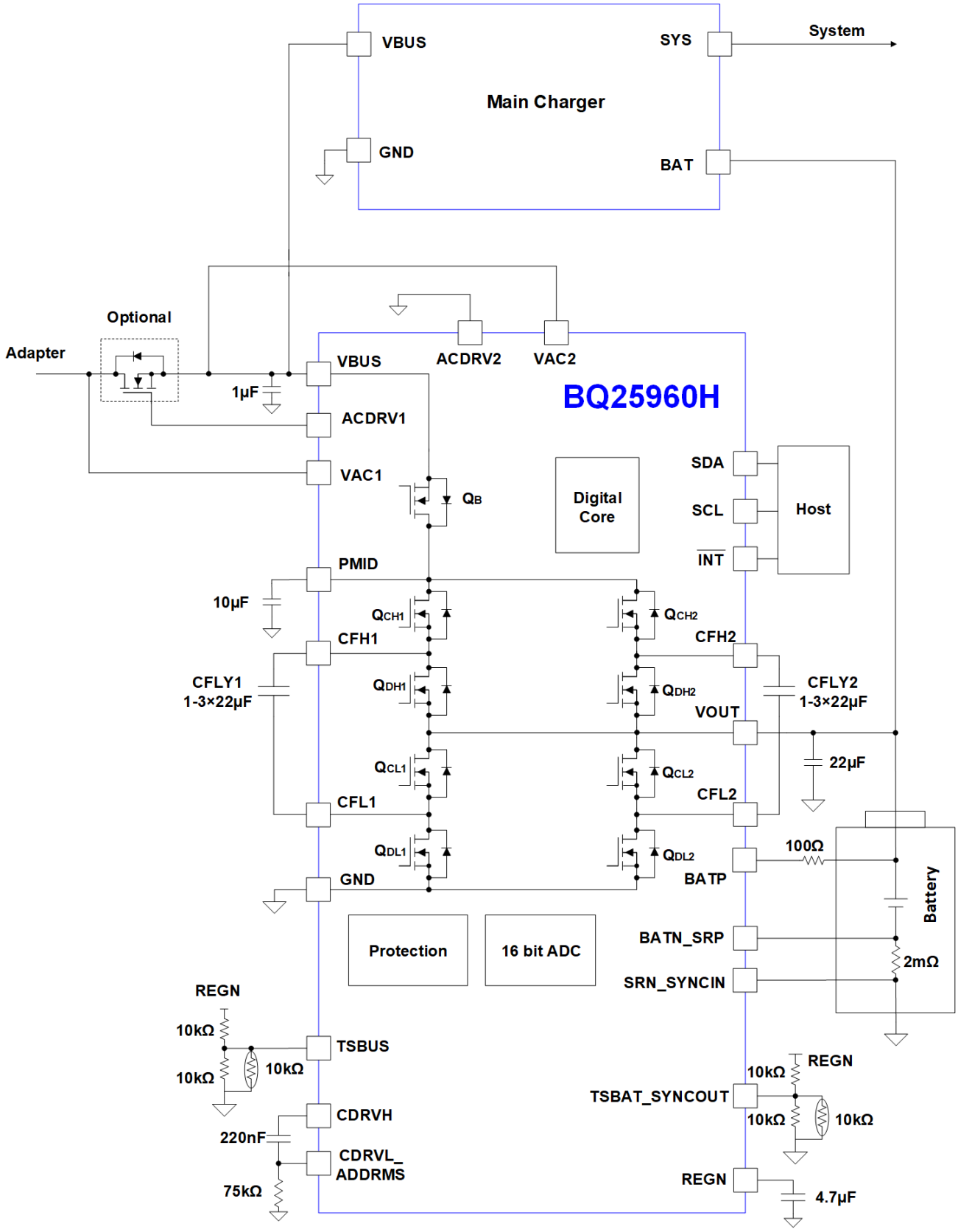

Figure 9-2. BQ25960H Typical Application Diagram with Single Input

9.2.1.1 Design Requirements

The design requires a smart wall adapter to provide the proper input voltage and input current to the BQ25960H, following the USB_PD Programmable Power Supply (PPS) voltage steps and current steps. The design shown is capable of charging up to 8 A, although this may not be practical for some applications due to the total power loss at this operating point. Careful consideration of the thermal constraints, space constraints, and operating conditions should be done to ensure acceptable performance.

9.2.1.2 Detailed Design Procedure

The first step is to determine the number of CFLY caps to put on each phase of the design. It is important to consider the current rating of the caps, their ESR, and the capacitance rating. Be sure to consider the bias voltage derating for the caps, as the CFLY caps are biased to half of the input voltage, and this will affect their effective capacitance. An optimal system will have 3 22-µF caps per phase, for a total of 6 caps per device. It is possible to use fewer caps if the board space is limited. Using fewer caps will result in higher voltage and current ripple on the output, as well as lower efficiency.

The default switching frequency, f_{SW}, for the power stage is 500 kHz. The switching frequency can be adjusted in register 0x10h using the FSW_SET bits. It is recommended to select 500 kHz if IBATADC is not used and 375 kHz if IBATADC is used.

It is recommended to use 1-µF cap on VBUS, 10-µF cap on PMID and 22-µF cap on VOUT.

9.2.1.3 Application Curves

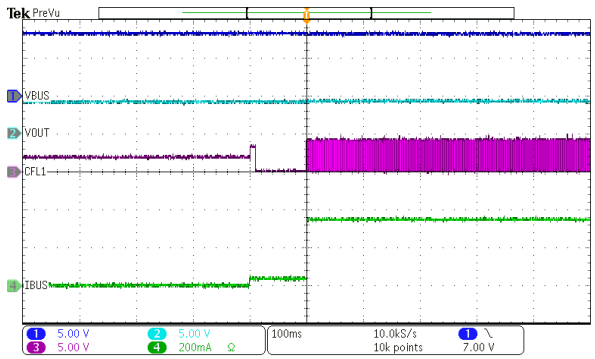

Figure 9-3. Switched Cap Mode Power Up

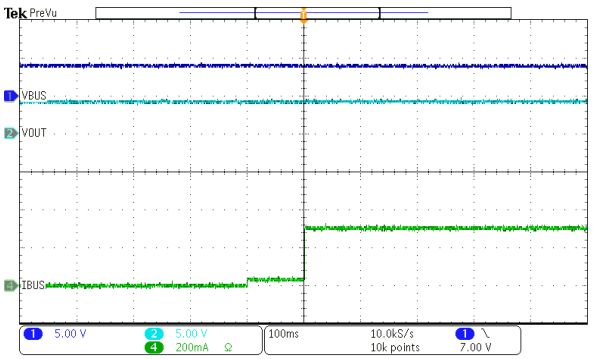

Figure 9-4. Bypass Mode Power Up

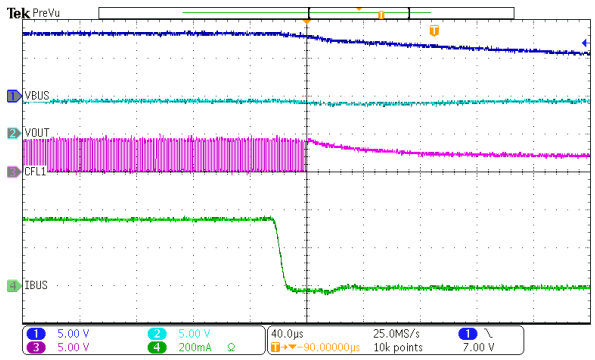

Figure 9-5. Adapter Unplug in Switched Cap Mode

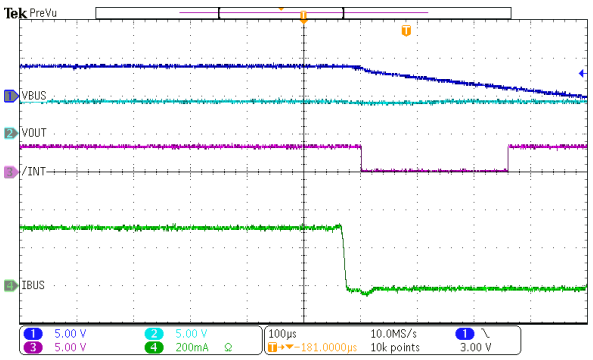

Figure 9-6. Adapter Unplug in Bypass Mode

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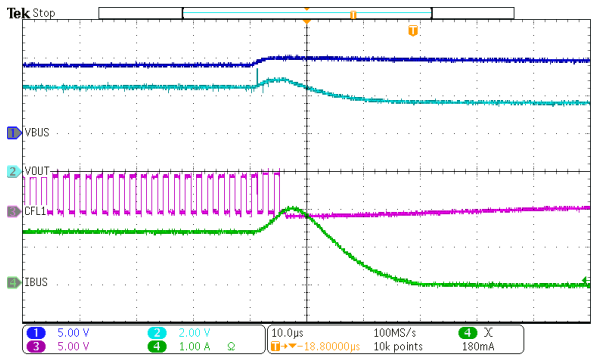

Figure 9-7. VBUSOVP in Switched Cap Mode

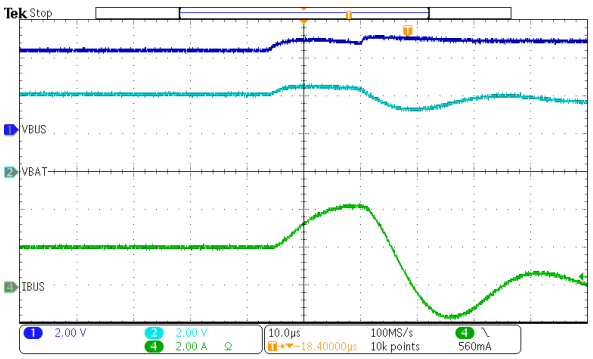

Figure 9-8. VBUSOVP in Bypass Mode

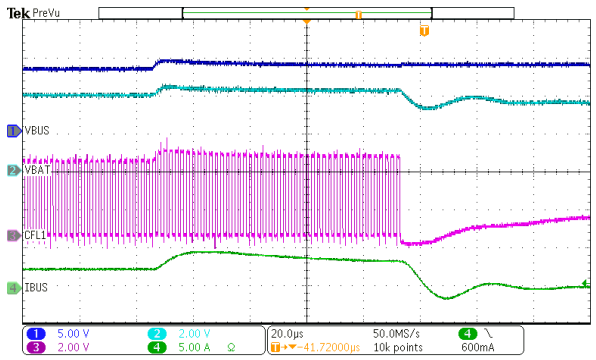

Figure 9-9. IBUSOCP in Switched Cap Mode

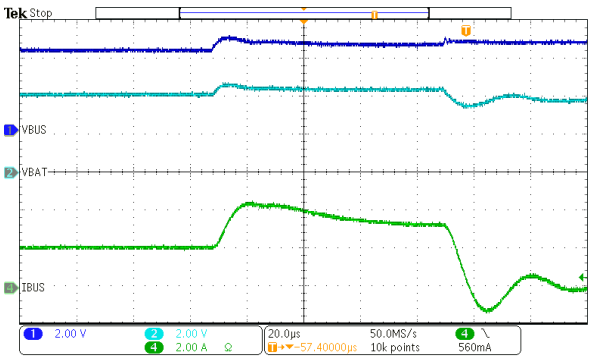

Figure 9-10. IBUSOCP in Bypass Mode

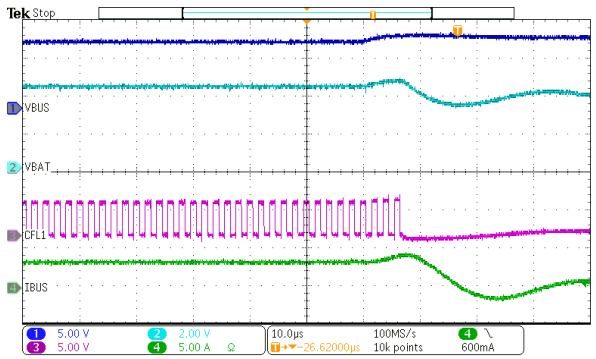

Figure 9-11. VBATOVP in Switched Cap Mode

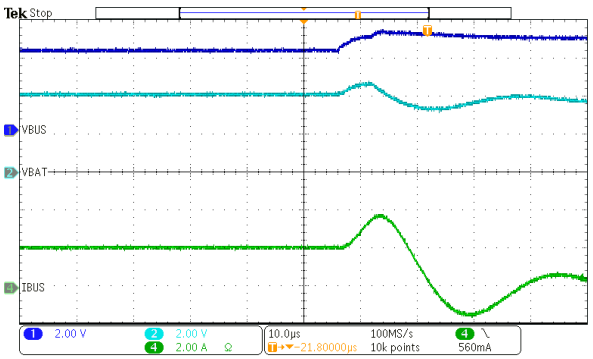

Figure 9-12. VBATOVP in Bypass Mode

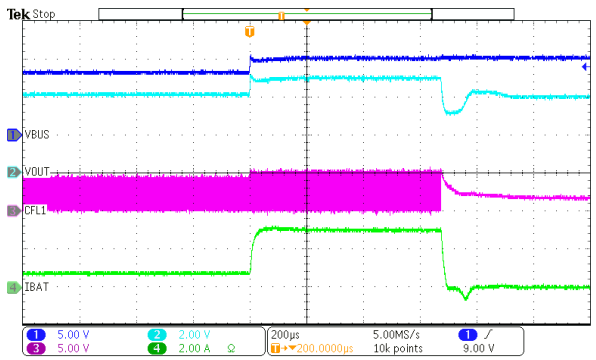

Figure 9-13. IBATOCP in Switched Cap Mode

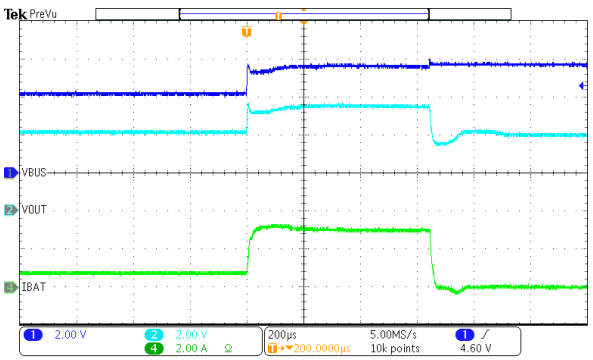

Figure 9-14. IBATOCP in Bypass Mode

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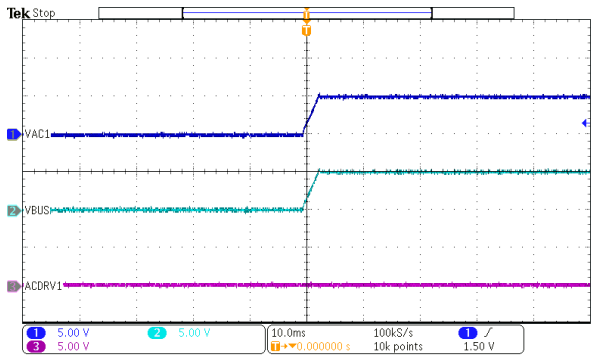
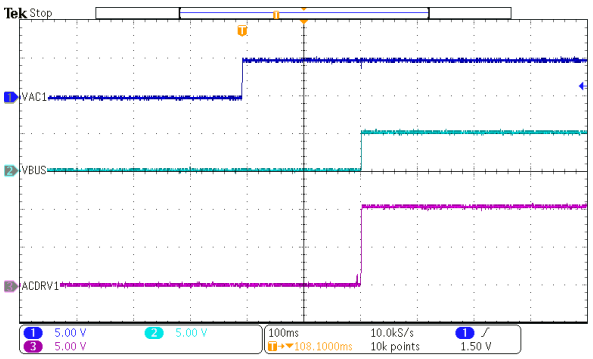


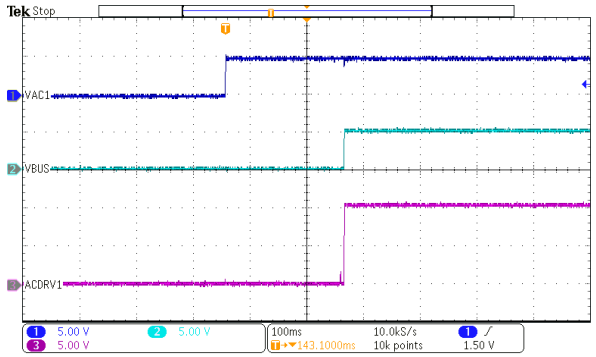
VAC1 and VAC2 short to VBUS, ACDRV1 and ACDRV2 short to ground

Figure 9-15. Power Up without AC-RFFET



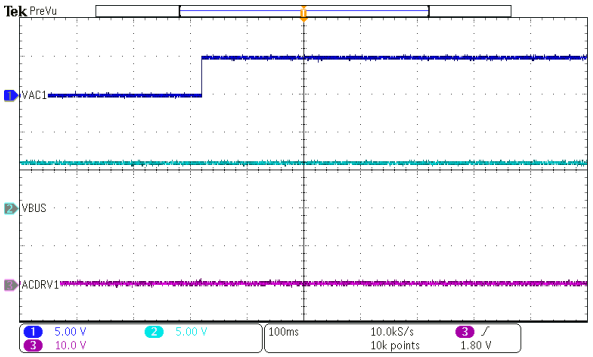
VAC1 connected to input source, VAC2 short to VBUS, ACDRV1 active, ACDRV2 short to ground

Figure 9-16. Power Up from VAC1 with Single ACFET1



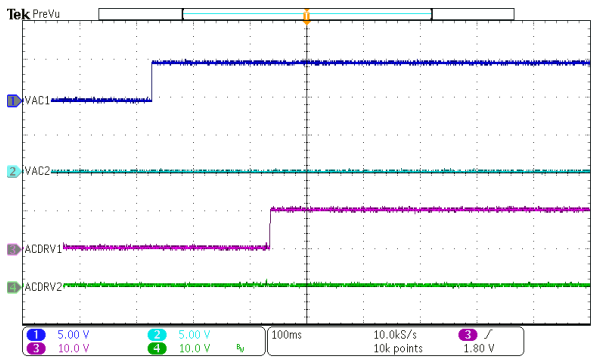
VAC1 connected to input source 1, VBUS connected to input source 2, VAC2 short to VBUS, ACDRV1 active, ACDRV2 short to ground

Figure 9-17. Power Up from VAC1 with ACFET1-RBFET1



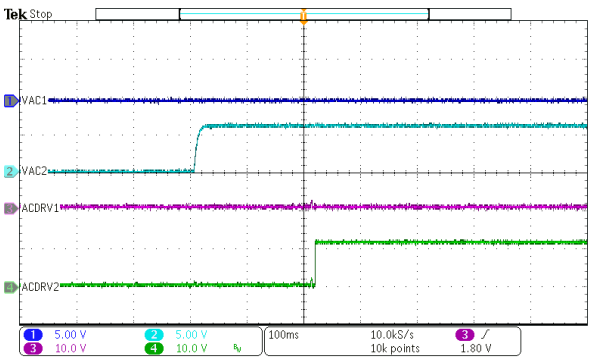
VAC1 connected to input source 1, VBUS connected to input source 2, VAC2 short to VBUS, ACDRV1 active, ACDRV2 short to ground

Figure 9-18. Plugin VAC1 When Device is Power Up From VBUS with ACFET1-RBFET1



VAC1 connected to input source 1, VAC2 connected to input source 2, ACDRV1 and ACDRV2 active

Figure 9-19. Power Up from VAC1 with ACFET1-RBFET1 and ACFET2-RBFET2



VAC1 connected to input source 1, VAC2 connected to input source 2, ACDRV1 and ACumDRV2 active

Figure 9-20. Power Up from VAC2 with ACFET1-RBFET1 and ACFET2-RBFET2

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10 Power Supply Recommendations

The BQ25960H can be powered by a standard power supply capable of meeting the input voltage and current requirements for evaluation. In the actual application, it must be used with a wall adapter that supports USB Power Delivery (PD) Programmable Power Supply (PPS) specifications.

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11 Layout

11.1 Layout Guidelines

Layout is very important to maximize the electrical and thermal performance of the total system. General guidelines are provided, but the form factor, board stack-up, and proximity of other components also need to be considered to maximize the performance.

1. VBUS and VOUT traces should be as short and wide as possible to accommodate for high current.
2. Copper trace of VBUS and VOUT should run at least 150 mil (3.81 mm) straight (perpendicular to WCSP ball array) before making turns.
3. CFLY caps should be placed as close as possible to the device and CFLY trace should be as wide as possible until close to the IC.
4. CLFY pours should be as symmetrical between CFH pads and CFL pads as possible.
5. Place low ESR bypass capacitors to ground for VBUS, PMID, and VOUT. The capacitor should be placed as close to the device pins as possible.
6. The CFLY pads should be as small as possible, and the CFLY caps placed as close as possible to the device, as these are switching pins and this will help reduce EMI.
7. Do not route so the power planes are interrupted by signal traces.

Refer to the EVM design and more information in the *BQ25960EVM (BMS041) Evaluation Module User's Guide* for the recommended component placement with trace and via locations.

11.2 Layout Example

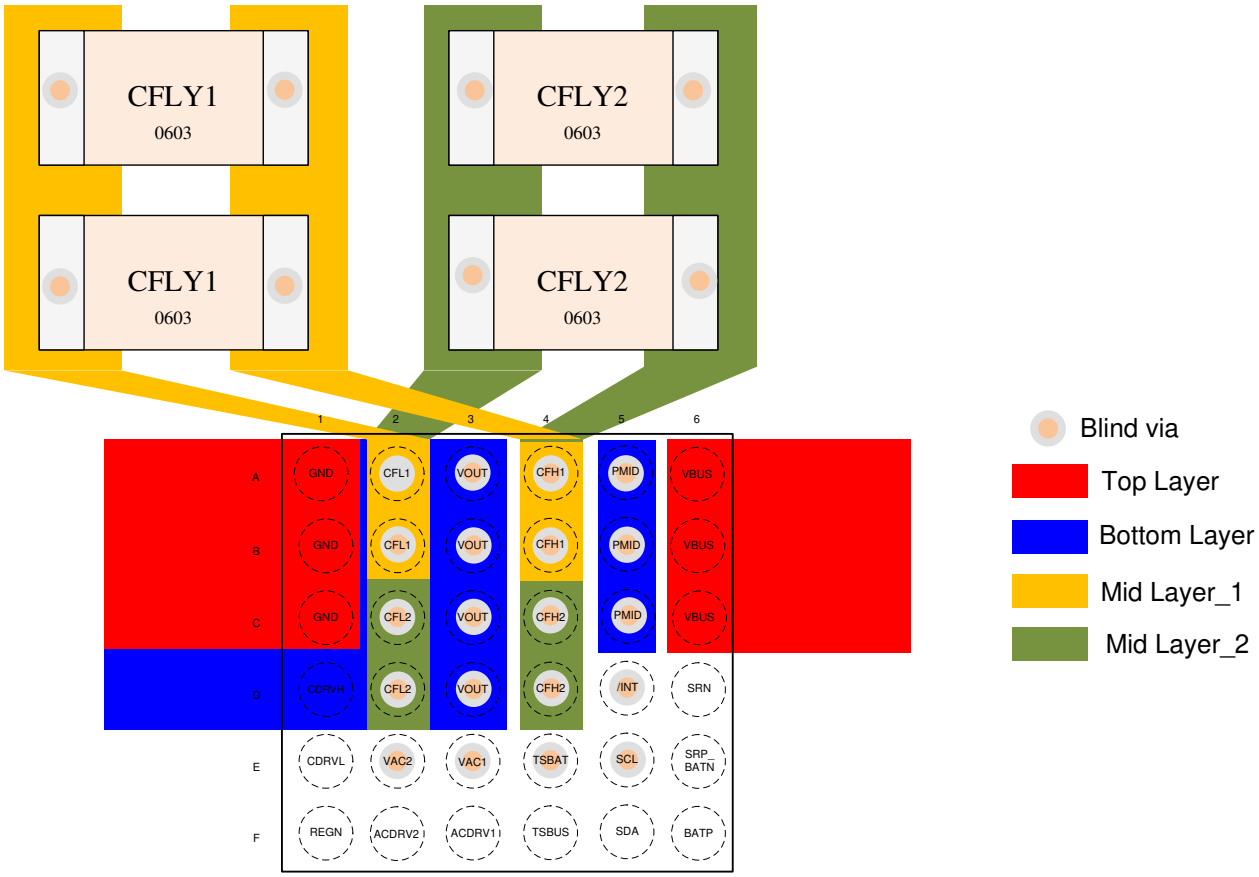

Figure 11-1. BQ25960H Layout Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *BQ25960EVM (BMS041) Evaluation Module User's Guide*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2023) to Revision A (July 2025)	Page
• Changed V_{BATADC_LSB} from 1.017mV (typical) to 1.0017mV (typical) in Electrical Characteristics	7
• Changed Bit Step Size from 1.017mV to 1.0017mV in REG2F_VBAT_ADC Register	33

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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14.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
BQ25960HYBGR	ACTIVE	DSBGA	YBG	36	6000	RoHS & Green	SNAGCU	Level-1-260 C-UNLIM	–40 to 85	BQ25960H

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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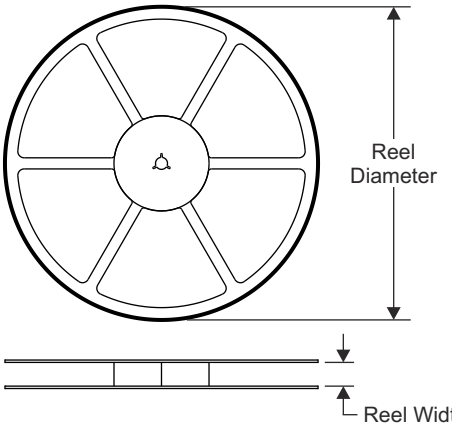
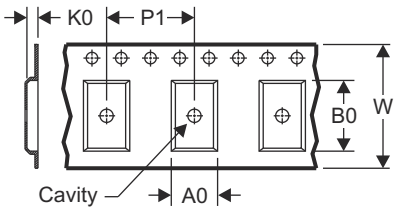
14.2 Tape and Reel Information

REEL DIMENSIONS

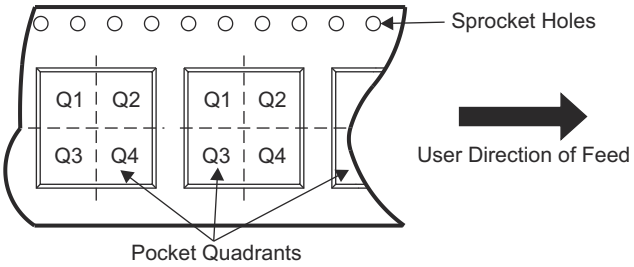


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25960HYBGR	DSBGA	YBG	36	6000	330.0	12.4	2.73	2.73	0.68	4.0	12.0	Q1

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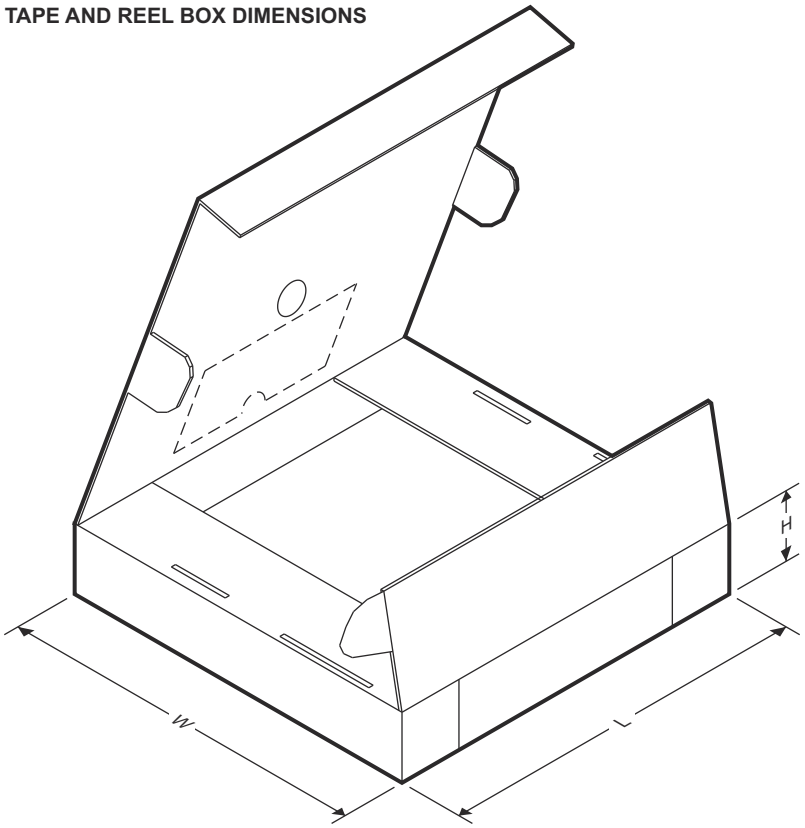
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25960HYBGR	DSBGA	YBG	36	6000	360.0	360.0	36.0
BQ25960HYBGR	DSBGA	YBG	36	6000	367.0	367.0	35.0

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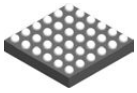
14.3 Mechanical Data

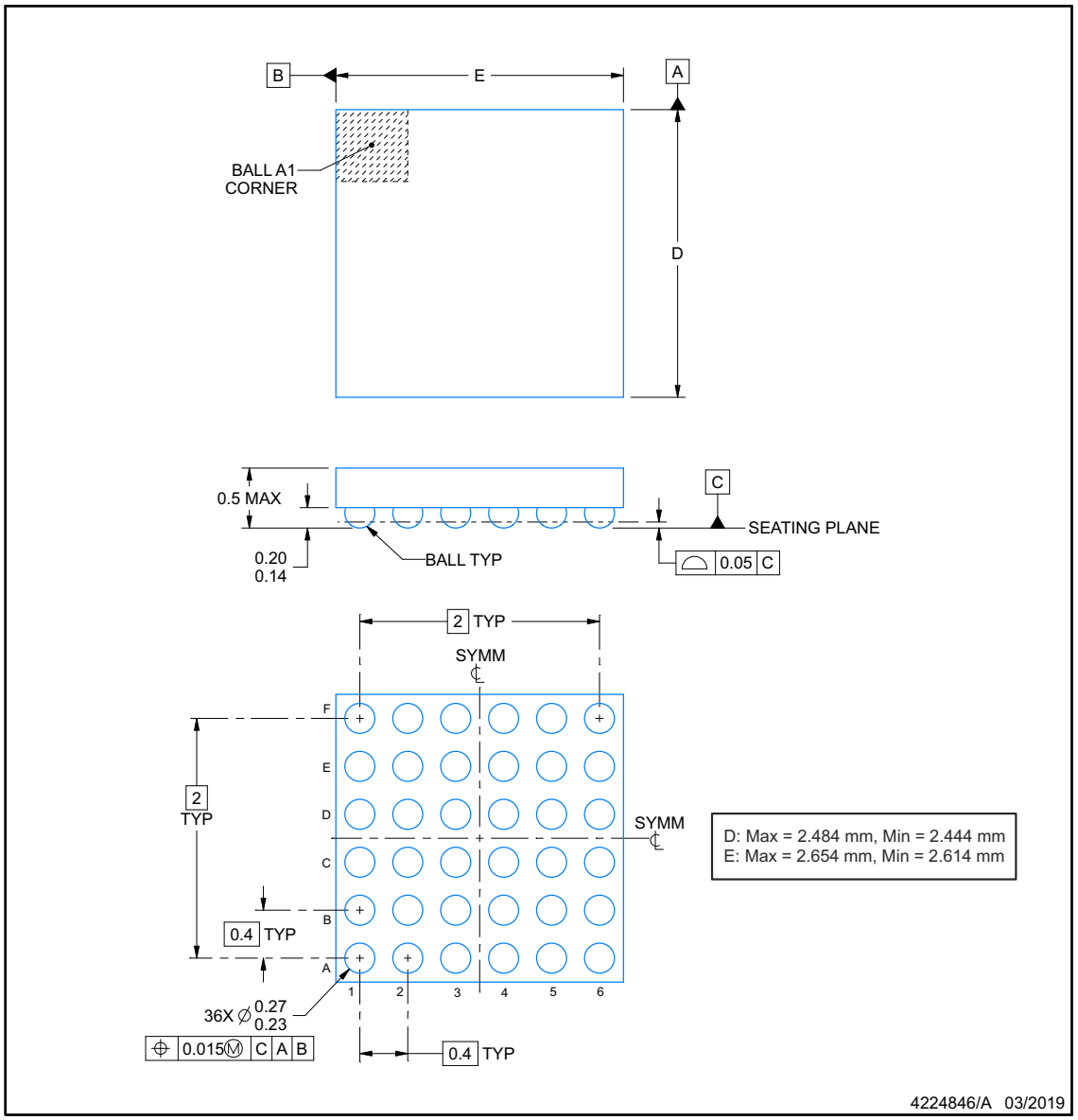


PACKAGE OUTLINE

YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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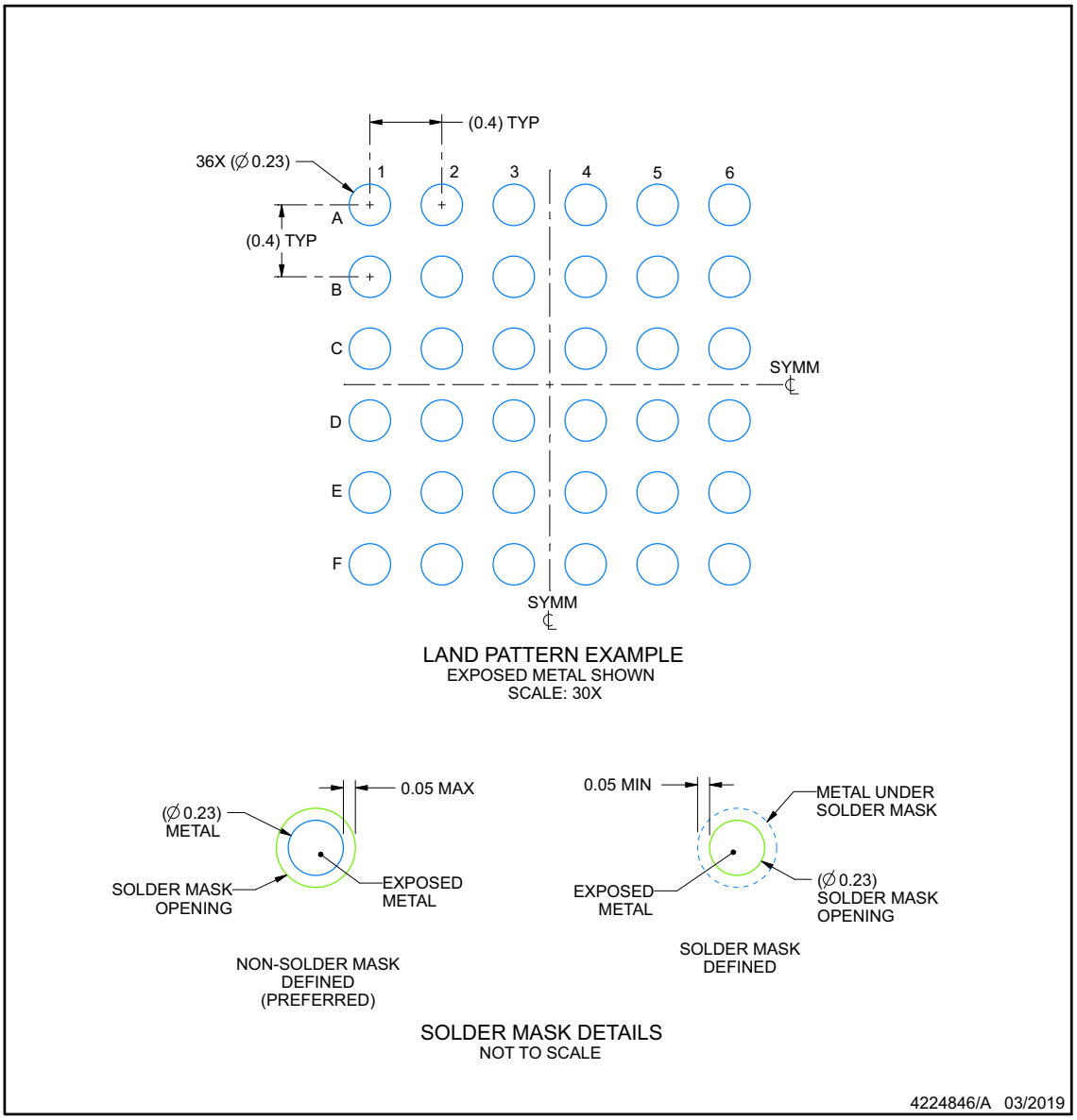
EXAMPLE BOARD LAYOUT

YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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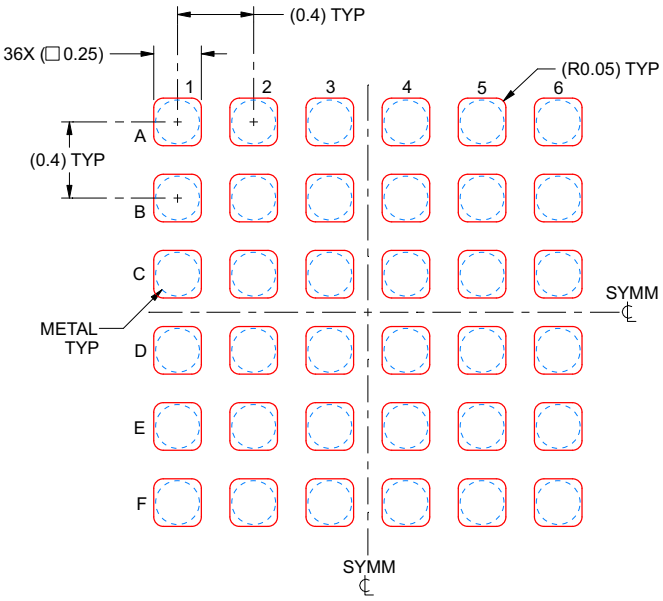
EXAMPLE STENCIL DESIGN

YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224846/A 03/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25960HYBGR	Active	Production	DSBGA (YBG) | 36	6000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25960H
BQ25960HYBGR.A	Active	Production	DSBGA (YBG) | 36	6000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25960H
BQ25960HYBGR.B	Active	Production	DSBGA (YBG) | 36	6000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25960H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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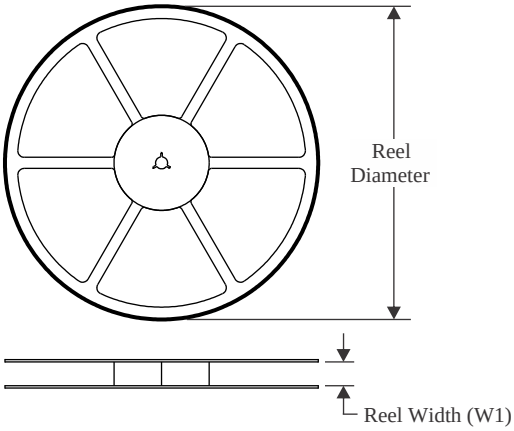
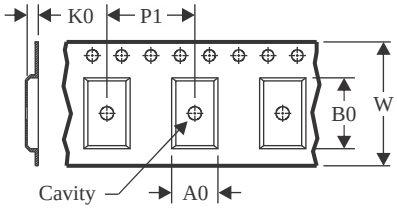
TAPE AND REEL INFORMATION

REEL DIMENSIONS

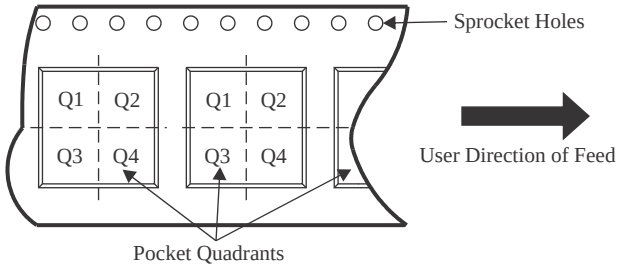


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

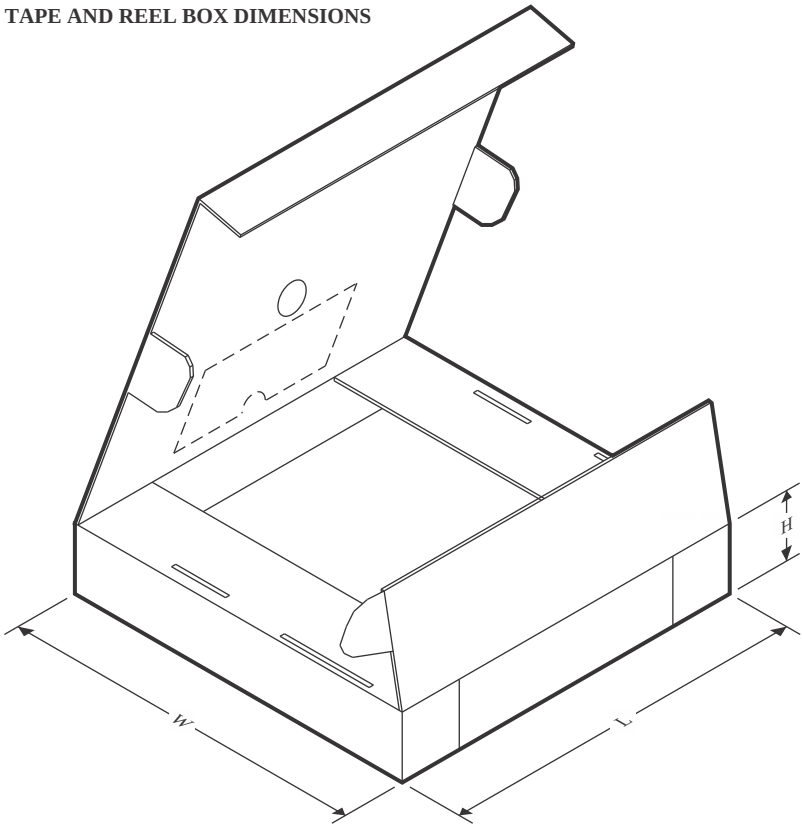
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25960HYBGR	DSBGA	YBG	36	6000	330.0	12.4	2.73	2.73	0.68	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

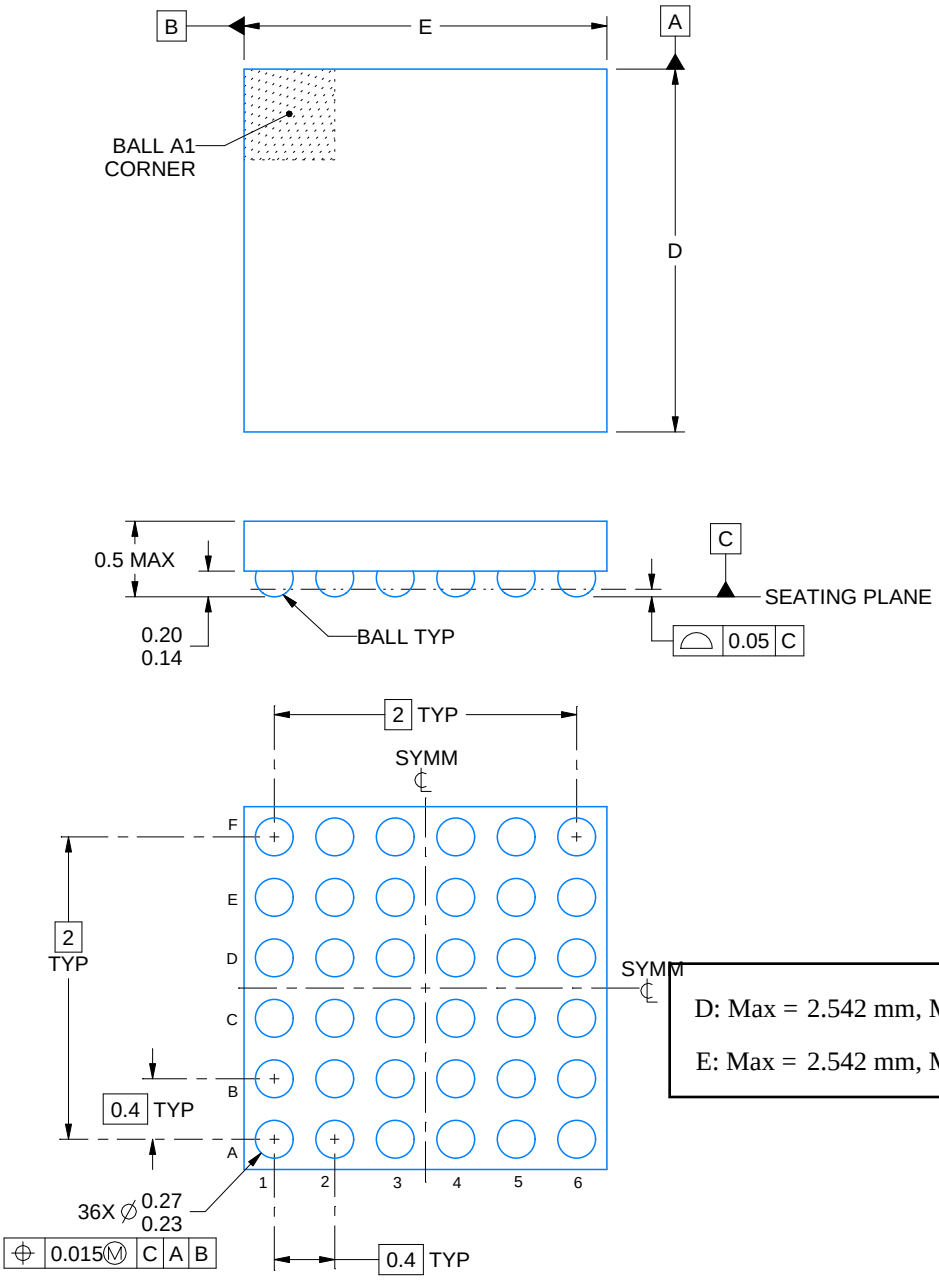
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25960HYBGR	DSBGA	YBG	36	6000	367.0	367.0	35.0

PACKAGE OUTLINE

YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4224846/A 03/2019

NOTES:

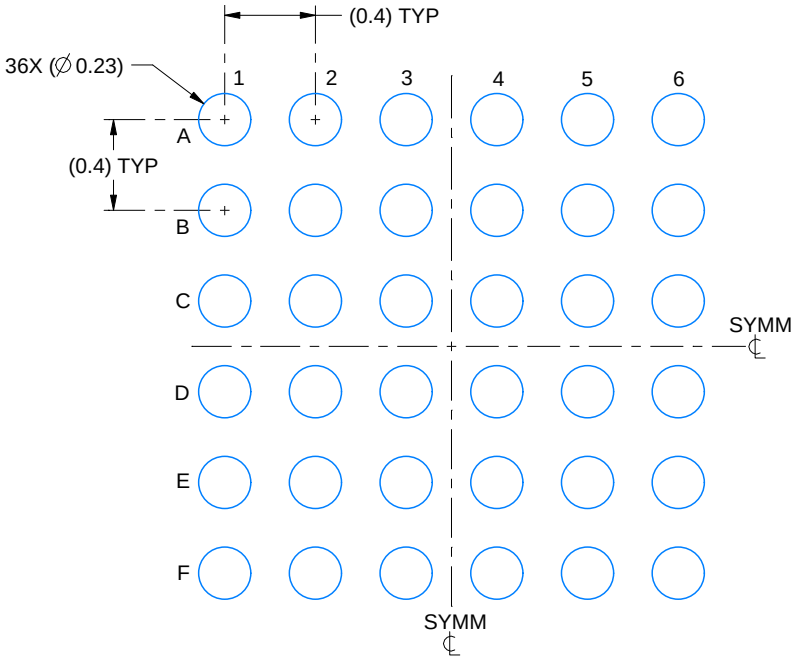
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

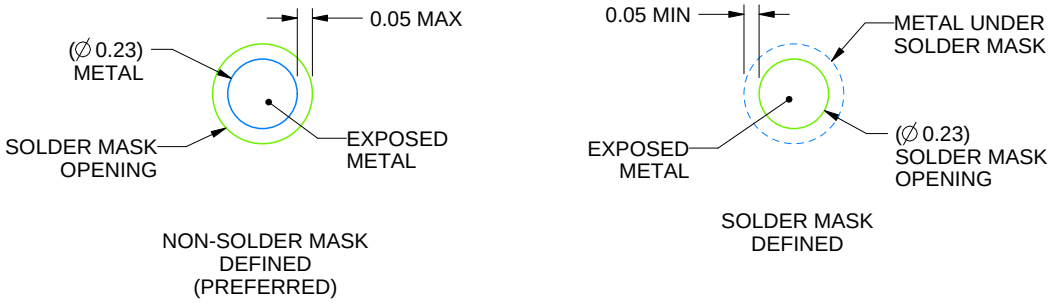
YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

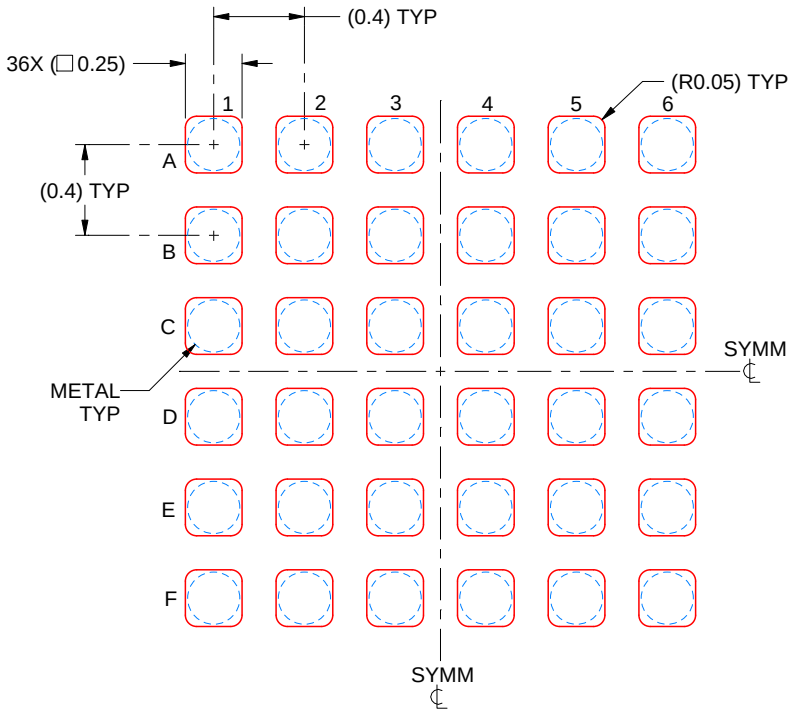


SOLDER MASK DETAILS
NOT TO SCALE

4224846/A 03/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224846/A 03/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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