# BQ25770G 40V, SMBus, 2- to 5-Cell, Narrow VDC Quasi Dual Phase Buck-Boost Battery Charge Controller for GaN HEMT With System Power Monitor and Processor Hot Monitor

## 1 Features

- TI patented quasi dual phase buck-boost narrow voltage DC (NVDC) charger for USB-C Extended Power Range (EPR) interface platform
  - 3.5V to 40V input range to charge 2- to 5-cell battery
  - Charge current up to 16.3A/30A based on 5mΩ/2mΩ sensing resistor
  - Input current limit up to 8.2A/16.4A based on 10mΩ/5mΩ sensing resistor
  - Support USB 2.0, USB 3.0, USB 3.1, USB-C power delivery and extended power range input current setting
  - Input Current Optimizer (ICO) to extract max input power without overloading the adapter
  - Integrated Fast Role Swap (FRS) feature following USB-PD specification
  - Seamless transition between quasi dual phase buck, buck-boost, and boost operations
  - Input current and voltage regulation (IINDPM and VINDPM) against source overload
  - Battery supplements system when adapter is fully loaded
- TI patented dual ramdom spread spectrum (DRSS) for meeting IEC-CISPR 32 EMI specification
- TI patented Pass Through Mode (PTM) for >99% efficiency and battery fast charging support
- IMVP8/IMVP9 compliant system features for Intel platform
  - Enhanced Vmin Active Protection (VAP) mode supplements battery from input capacitors during system peak power spike following latest Intel specification
  - Comprehensive $\overline{\text{PROCHOT}}$ profile
  - Two level discharge current limit $\overline{\text{PROCHOT}}$ profile to avoid battery wear out
  - System power monitor (PSYS)
- Input and battery current monitor through dedicated pins
- Integrated 16-bit ADC to monitor voltage, current and power
- Battery MOSFET ideal diode operation in supplement mode
- Power up USB port from battery (USB OTG)
  - 3V to 5V OTG
  - Output current limit up to 3A based on 10mΩ sensing resistor
- 600kHz/800kHz programmable switching frequency
- SMBus host control interface for flexible system configuration
- High accuracy for the regulation and monitor
  - ±0.5% Charge voltage regulation
  - ±2% Charge current regulation
  - ±2% Input current regulation
  - ±2% Input/charge current monitor
- Safety
  - Thermal regulation and thermal shutdown
  - Input, system, battery overvoltage protection
  - Input, MOSFET, inductor overcurrent protection
- Package: 36-Pins 4.0mm × 5.0mm WQFN

## 2 Applications

- Standard notebook PC,Chromebook
- Appliances: battery charger,Oxygen concentrator

## 3 Description

The BQ25770G is a synchronous NVDC buck-boost battery charge controller to charge a 2- to 5-cell battery from a wide range of input sources including USB adapter, extended power range (EPR) USB-C Power Delivery (PD) sources, standard power range (SPR) USB-C Power Delivery (PD) sources and traditional adapters. The device offers a low component count, high efficiency solution for space constrained, 2- to 5-cell battery charging applications.

The NVDC configuration allows the system to be regulated based on battery voltage, but not drop below system minimum voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds input source rating, the battery goes into supplement mode and prevents the system from crashing.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE (NOM) |
|---|---|---|---|
| BQ25770G | REE (WQFN, 36) | 4.00 mm × 5.00 mm | 4.00 mm × 5.00 mm |

(1) For all available packages, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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During power up, the charger sets the converter to a buck, boost, or buck-boost configuration based on the input source and battery conditions. The charger seamlessly transits between the buck, boost, and buck-boost operation modes without host control. The TI patented quasi dual phase converter can interleave dual phase under high power buck mode helping thermal distribution and reduce each inductor size. At same time it only needs two boost side switching MOSFETs to save overall system area and cost due to limited power operation under boost mode.

In the absence of an input source, the BQ25770G supports the USB On-the-Go (OTG) function from a 2- to 5-cell battery to generate an adjustable 3V to 5V output on VBUS with 20mV resolution.

When only a battery powers the system and no external load is connected to the USB OTG port, the BQ25770G implements the latest Intel Vmin Active Protection (VAP) feature, in which the device charges up the VBUS voltage from the battery to store some energy in the input decoupling capacitors. During a system peak power spike, the energy stored in the input capacitors supplements the system, to prevent the system voltage from dropping below the minimum system voltage and causing a system crash.

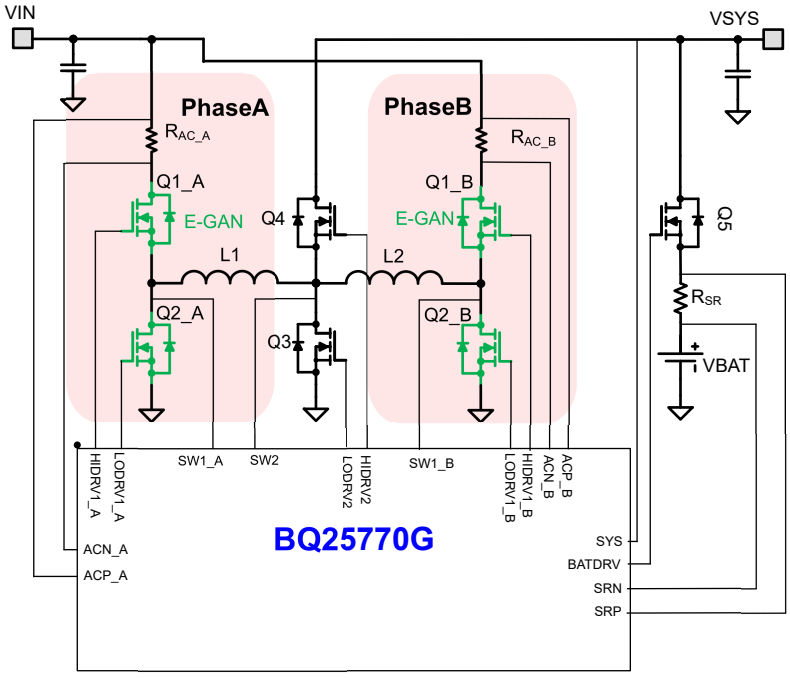
The BQ25770G monitors adapter current, battery current, and system power. The flexibly programmable $\overline{\text{PROCHOT}}$ output goes directly to the CPU for throttling back when needed.

The latest version of the USB-C PD specification includes Fast Role Swap (FRS) to ensure power role swapping occurs in a timely fashion so that the device(s) connected to the dock can avoid experiencing momentary power loss or glitching. This device integrates FRS in compliance with the PD specification.

TI patented switching frequency dithering pattern can significantly reduce EMI noise over the whole conductive EMI frequency range (150kHz to 30MHz). Multiple dithering scale options are available and provide flexibility for different applications. The ditherring feature greatly simplify EMI noise filter design.

The charger operate in the TI patented Pass Through Mode (PTM) to improve efficiency over the full load range. In PTM, input power directly pass through the charger to the system. Switching losses of the MOSFETs and inductor core loss can be saved thus achieving high efficiency operation.

The BQ25770G is available in a 36-pin 4mm × 5mm WQFN package.




**Simplified Application Diagram**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# 4 Device Comparison Table

| | BQ25710 | BQ25720 | BQ25770 | BQ25770G |
|---|---|---|---|---|
| Interface | SMBus | SMBus | SMBus | SMBus |
| Device Address | 09h | 09h | 09h | 09h |
| Input Voltage Range | 3.5V~24V | 3.5V~26V | 3.5V~40V | 3.5V~40V |
| Maximum Charge Current (RSR=5mΩ) | 8.128 A | 16.256 A | 16.320 A | 16.320 A |
| Switching Frequency (Hz) | 800 k/1.2 M | 800 k/1.2 M | 600 k/800 k | 600 k/800 k |
| Cell Count | 1s to 4s | 1s to 4s | 2s to 5s | 2s to 5s |
| Input Current Sense Resistor | 10 mΩ/20 mΩ | 10 mΩ/5 mΩ | 10 mΩ/5 mΩ | 10 mΩ/5 mΩ |
| Charge Current Sense Resistor | 10 mΩ/20 mΩ | 10 mΩ/5 mΩ | 5 mΩ/ 2 mΩ | 5 mΩ/ 2 mΩ |
| Independent Comparator Latch | Non Latch | Latch/Non latch (default) | Latch/Non latch (default) | Latch/Non latch (default) |
| VSYS_UVP | 2.4 V | 2.4 V ~ 8.0 V (0.8-V step size) Default: 2.4 V | 2.4 V ~ 8.0 V (0.8-V step size) Default: 2.4 V | 2.4 V ~ 8.0 V (0.8-V step size) Default: 2.4 V |
| OTG Voltage Range | 3.0 V to 20.8 V | 3.0 V to 24 V | 3.0 V to 5 V | 3.0 V to 5 V |
| Frequency Dithering | No | Yes | Yes | Yes |
| Quasi Dual Phase | No | No | Yes | Yes |
| Buck dual phase GAN Gate Drive | No | No | No | Yes |


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# 5 Pin Configuration and Functions

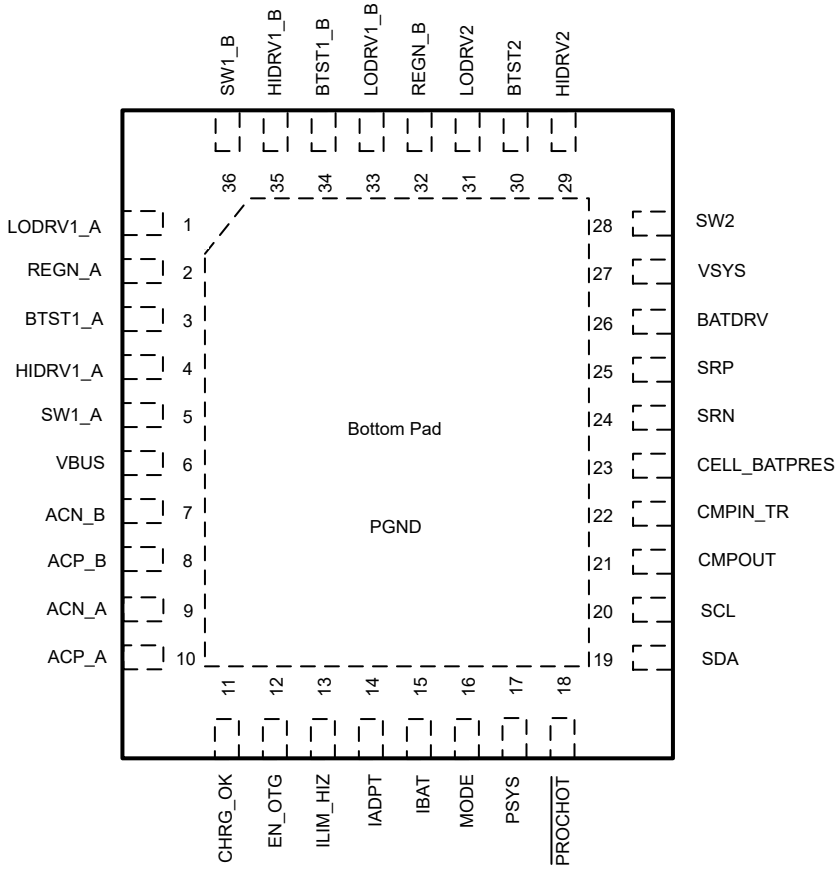


**Figure 5-1. BQ25770G 36-Pin WQFN Top View**

**Table 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| LODRV1_A | 1 | AO | Buck phase A low side power MOSFET (Q2_A) driver. Connect to low side N-channel MOSFET gate. |
| REGN_A | 2 | PWR | 5-V linear regulator output supplied from VBUS or VSYS. The LDO is active when VBUS above $V_{VBUS_CONVEN}$. Connect a 2.2- or 3.3-µF ceramic capacitor from REGN_A to power ground. REGN_A pin output is for power stage gate drive and pull up voltage source. |
| BTST1_A | 3 | PWR | Buck phase A high side power MOSFET driver power supply. Connect a 0.1-µF capacitor between SW1_A and BTST1_A. The bootstrap diode between REGN_A and BTST1_A is integrated. |
| HIDRV1_A | 4 | AO | Buck phase A high side power MOSFET (Q1_A) driver. Connect to high side N-channel MOSFET gate. |
| SW1_A | 5 | PWR | Buck phase A switching node. Connect to the source of the phase A buck half bridge high side n-channel MOSFET. |
| VBUS | 6 | PWR | Charger input voltage. An input low-pass filter of 1 Ω and 0.47 µF (minimum) is recommended. |
| ACN_B | 7 | PWR | Phase B input current sense amplifier negative input. A RC low-pass filter is required to be placed between the sense resistor and the ACN_B pin to suppress the high frequency noise in the input current signal. Refer to Section 8.2.2.1 for filter design. |
| ACP_B | 8 | PWR | Phase B input current sense amplifier positive input. A RC low-pass filter is required to be placed between the sense resistor and the ACP_B pin to suppress the high frequency noise in the input current signal. Refer to Section 8.2.2.1 for filter design. |

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**Table 5-1. Pin Functions (continued)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| ACN_A | 9 | PWR | Phase A input current sense amplifier negative input. A RC low-pass filter is required to be placed between the sense resistor and the ACN_A pin to suppress the high frequency noise in the input current signal. Refer to Section 8.2.2.1 for filter design. |
| ACP_A | 10 | PWR | Phase A input current sense amplifier positive input. A RC low-pass filter is required to be placed between the sense resistor and the ACP_A pin to suppress the high frequency noise in the input current signal. Refer to Section 8.2.2.1 for filter design. |
| CHRG_OK | 11 | DO | Open drain active high indicator to inform the system good power source is connected to the charger input. Connect to the pullup rail via a 10-kΩ resistor. When VBUS rises above 3.5 V and falls below $V_{ACOV_FALL}$, CHRG_OK is HIGH after 50-ms deglitch time. When VBUS falls below 3.2 V or rises above $V_{ACOV_RISE}$, CHRG_OK is LOW. When specific faults occur, CHRG_OK is asserted LOW. The pin can also be configured as interrupt source when CHRG_STAT changes with user register CHRG_OK_INT=1b. |
| EN_OTG | 12 | DI | Active HIGH to enable OTG, VAP or FRS modes. 1) When OTG_VAP_MODE=1b and EN_OTG=1b, pulling high this pin can enable OTG mode. 2) When OTG_VAP_MODE=1b and EN_FRS=1b, pulling high this pin can enable FRS mode in forward operation. 3) When OTG_VAP_MODE=0b, pulling high EN_OTG pin to enable VAP mode. Refer to Table 7-5for details. |
| ILIM_HIZ | 13 | AI | Input current limit setting pin. Program ILIM_HIZ voltage by connecting a resistor divider from REGN_A rail to ground. The pin voltage is calculated as: $V_{(ILIM_HIZ)}$ = 1 V + 40 × IINDPM × Rac, in which IIN_DPM is the target input current limit.<br>When the pin voltage is above $V_{ILIM_ENZ}$ threshold, the external current limit function is disabled neglecting EN_EXTILIM bit status. When the pin voltage drops below $V_{ILIM_EN}$ threshold, then external current limit will follow EN_EXTILIM bit status. If EN_EXTILIM = 1b the input current limit used by the charger is the lower setting of ILIM_HIZ pin and IIN_HOST register. If EN_EXTILIM = 0b input current limit is only determined by IIN_HOST register. When the pin voltage is below 0.4 V, the device enters high impedance (HIZ) mode with low quiescent current. When the pin voltage is above 0.8 V, the device is out of HIZ mode. The ILIM_HIZ pin voltage is continuous read and used for updating current limit setting (If EN_EXTILIM=1b ), this allows dynamic change input current limit setting by adjusting this pin voltage. |
| IADPT | 14 | AO | The adapter current monitoring output pin. $V_{IADPT}$ = 20 or 40 × ($V_{ACP_B}$ – $V_{ACN_B}$+$V_{ACP_A}$ – $V_{ACN_A}$) with ratio selectable through IADPT_GAIN bit. Place a 100-pF or less ceramic decoupling capacitor from IADPT pin to ground. This pin can be floating if not in use. IADPT output voltage is clamped below 3.2 V. |
| IBAT | 15 | AO | The battery current monitoring output pin. $V_{IBAT}$ = 8 or 64 × ($V_{SRP}$ – $V_{SRN}$) for charge current, or $V_{IBAT}$ = 8 or 64 × ($V_{SRN}$ – $V_{SRP}$) for discharge current, with ratio selectable through IBAT_GAIN bit. Place a 100-pF or less ceramic decoupling capacitor from IBAT pin to ground. This pin can be floating if not in use. Its output voltage is clamped below 3.2 V. |
| MODE | 16 | AI | Charger operation mode pin. Pull down resistor is needed on this MODE pin referring to Table 7-1. |
| PSYS | 17 | AO | Current mode system power monitor. The output current is proportional to the total power from the adapter and the battery. The gain is selectable through host communication interface. Place a resistor from PSYS to ground to generate output voltage. This pin can be floating if not in use. Its output voltage is clamped at 3.2 V. Place a capacitor in parallel with the resistor for filtering. |
| $\overline{\text{PROCHOT}}$ | 18 | DO | Active low open drain output indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the $\overline{\text{PROCHOT}}$ profile is triggered, a pulse is asserted. The minimum pulse width is adjustable through PROCHOT_WIDTH bits. |
| SDA | 19 | DI/O | open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to specifications. When communication frequency is increased to 1 Mhz, the pullup resistance may need to be reduced accordingly based on line capacitance. |
| SCL | 20 | DI | clock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to specifications. When communication frequency is increased to 1 Mhz, the pullup resistance may need to be reduced accordingly based on line capacitance. |
| CMPOUT | 21 | DO | Open-drain output of independent comparator. Place a pullup resistor from CMPOUT to pullup supply rail. Comparator polarity and deglitch time are selectable through user register. |


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**Table 5-1. Pin Functions (continued)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| CMPIN_TR | 22 | AI | Input of independent comparator, the independent comparator compares the voltage sensed on CMPIN_TR pin with internal reference, and its output is on CMPOUT pin. Comparator polarity and deglitch time is selectable by the host. With polarity HIGH (CMP_POL = 1b), place a resistor between CMPIN_TR and CMPOUT to program hysteresis. With polarity LOW (CMP_POL = 0b), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN_TR to ground. When CMPIN_TR_SELECT=1b , it is the temperature feedback pin for an internally compensated temperature regulation loop. |
| CELL_BATPRES | 23 | AI | Battery cell selection pin for 2–5-cell battery setting. CELL_BATPRES pin should be biased from REGN_A through a resistor divider (40% for 2s, 55% for 3s ,75% for 4s and 100% for 5s). CELL_BATPRES pin also sets SYSOVP thresholds to 12 V for 2-cell, 17 V for 3-cell, 22 V for 4-cell and 27 V for 5-cell. CELL_BATPRES pin is pulled below $V_{CELL_BATPRES_FALL}$ to indicate battery removal. No external cap is allowed at CELL_BATPRES pin. The total pull down impedance externally from CELL_BATPRES pin to GND should be no larger than 1 MΩ. |
| SRN | 24 | PWR | Charge current sense amplifier negative input. SRN pin is for battery voltage sensing as well. Connect a 0.1-µF filter cap cross battery charging sensing resistor and use 10-Ω contact resistor between SRN pin and battery charging sensing resistor. |
| SRP | 25 | PWR | Charge current sense amplifier positive input. Connect a 0.1-µF filter cap cross battery charging sensing resistor and use 10-Ω contact resistor between SRP pin and battery charging sensing resistor. |
| BATDRV | 26 | AO | N-channel battery FET (BATFET) gate driver output. It is shorted to SRP to turn off the BATFET. It goes 5 V above SRP to fully turn on BATFET. BATFET is in linear mode to regulate VSYS at VSYS_MIN() when battery is depleted below VSYS_MIN() setting. BATFET is fully on during fast charge and works as an ideal-diode in supplement mode. |
| VSYS | 27 | PWR | Charger system voltage sensing pin. |
| SW2 | 28 | PWR | Boost side switching node. Connect to the source of the boost half bridge high side N-channel MOSFET. |
| HIDRV2 | 29 | AO | Boost high side power MOSFET(Q4) driver. Connect to high side N-channel MOSFET gate. |
| BTST2 | 30 | PWR | Boost high side power MOSFET driver power supply. Connect a 0.1-µF capacitor between SW2 and BTST2. The bootstrap diode between REGN_B and BTST2 is integrated. |
| LODRV2 | 31 | AO | Boost low side power MOSFET (Q3) driver. Connect to low side N-channel MOSFET gate. |
| REGN_B | 32 | PWR | 5-V linear regulator output supplied from VBUS or VSYS. The LDO is active when VBUS above $V_{VBUS_CONVEN}$. Connect a 2.2- or 3.3-µF ceramic capacitor from REGN_B to power ground. REGN_B pin output is for power stage gate drive. Internally connected to REGN_A. |
| LODRV1_B | 33 | AO | Buck phase B low side power MOSFET (Q2_B) driver. Connect to low side N-channel MOSFET gate. |
| BTST1_B | 34 | PWR | Buck phase B high side power MOSFET driver power supply. Connect a 0.1-µF capacitor between SW1_B and BTST1_B. The bootstrap diode between REGN_B and BTST1_B is integrated. |
| HIDRV1_B | 35 | AO | Buck phase B high side power MOSFET (Q1_B) driver. Connect to high side N-channel MOSFET gate. |
| SW1_B | 36 | PWR | Buck side phase B switching node. Connect to the source of the phase B buck half bridge high side N-channel MOSFET. |
| Bottom pad (PGND) | – | PWR | Exposed pad beneath the IC as common PGND. Unless otherwise stated, signals are referenced to the PGND pin. Use the bottom pads as the thermal pad for heat dissipation. Have multiple vias on the thermal pad plane connecting to power ground planes. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | ACN_A, ACP_A,ACN_B,ACP_B,VBUS, VSYS | –0.3 | 45 | V |
| | SW1_A, SW1_B, SW2 | –2 | 45 | |
| | SRN, SRP | –0.3 | 30 | |
| | BATDRV | –0.3 | 35 | |
| | BTST1_A, BTST1_B, HIDRV1_A, HIDRV1_B | –0.3 | 50 | |
| | BTST2, HIDRV2 | –0.3 | 50 | |
| | LODRV1_A,LODRV1_B, LODRV2 (25nS) | –4 | 5.5 | |
| | HIDRV1_A,HIDRV1_B (25nS) | –4 | 50 | |
| | HIDRV2 (25nS) | –4 | 50 | |
| | SW1_A,SW1_B (25nS) | –4 | 45 | |
| | SW2 (25nS) | –4 | 45 | |
| | SDA, SCL, REGN_A,REGN_B, CHRG_OK, CELL_BATPRES, ILIM_HIZ, LODRV1_A, LODRV1_B, LODRV2, CMPIN_TR, CMPOUT, MODE, EN_OTG | –0.3 | 5.5 | |
| | /PROCHOT | –0.3 | 5.5 | |
| | IADPT, IBAT, PSYS | –0.3 | 3.6 | |
| Differential Voltage | BTST1_A-SW1_A, BTST1_B-SW1_B, BTST2-SW2, HIDRV1_A-SW1_A,HIDRV1_B-SW1_B, HIDRV2-SW2, BATDRV-SRP | –0.3 | 5.5 | V |
| | SRP-SRN, ACP_A-ACN_A,ACP_B-ACN_B | –0.3 | 0.3 | |
| Temperature | Junction temperature range, $T_J$ | –40 | 150 | °C |
| Temperature | Storage temperature, $T_{stg}$ | –55 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | ACP_A,ACN_A,ACP_B, ACN_B, VBUS | 0 | | 40 | V |
| | VSYS | 0 | | 23 | |
| | SRP, SRN | 0 | | 23 | |
| | SW1_A, SW1_B | –2 | | 40 | |
| | SW2 | –2 | | 23 | |
| | BTST1_A, BTST1_B, HIDRV1_A,HIDRV1_B | 0 | | 45 | |
| | BTST2, HIDRV2, BATDRV | 0 | | 28 | |
| | SDA, SCL,REGN_A,REGN_B, CHRG_OK, CELL_BATPRES, ILIM_HIZ, LODRV1_A, LODRV1_B, LODRV2, CMPIN_TR,CMPOUT, MODE, EN_OTG | 0 | | 5.3 | |
| | /PROCHOT | 0 | | 5 | |
| | IADPT, IBAT, PSYS | 0 | | 3.3 | |
| Differential Voltage | BTST1_A-SW1_A, BTST1_B-SW1_B, BTST2-SW2, HIDRV1_A-SW1_A, HIDRV1_B-SW1_B, HIDRV2-SW2, BATDRV-SRP | 0 | | 5 | V |
| | SRP-SRN, ACP_A-ACN_A, ACP_B-ACN_B | –0.2 | | 0.2 | |
| Temperature | Junction temperature range, $T_J$ | –40 | | 125 | °C |
| | Storage temperature, $T_{stg}$ | –40 | | 85 | |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | BQ2577X REE (WQFN) 36 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (JEDEC[1]) | 35.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 22.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 13.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **MAX SYSTEM VOLTAGE REGULATION** | | | | | | |
| $V_{SYSMAX_RNG}$ | System Voltage Regulation, measured on $V_{SYS}$ (charge disabled) | | 5.16 | | 23.16 | V |

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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{SYSMAX_ACC}$ | System voltage regulation accuracy (charge disabled) | CHARGE_VOLTAGE() = 0x1482 (21.000 V) | | $V_{SRN}$ + 200 mV | | V |
| | | | –0.6% | | 0.6% | |
| | | CHARGE_VOLTAGE() = 0x1068H (16.800 V) | | $V_{SRN}$ + 200 mV | | V |
| | | | –0.6% | | 0.6% | |
| | | CHARGE_VOLTAGE() = 0x0C4EH (12.600 V) | | $V_{SRN}$ + 200 mV | | V |
| | | | –0.6% | | 0.6% | |
| | | CHARGE_VOLTAGE() = 0x0834H (8.400 V) | | $V_{SRN}$ + 200 mV | | V |
| | | | –1% | | 1% | |
| **MINIMUM SYSTEM VOLTAGE REGULATION** | | | | | | |
| $V_{SYSMIN_RNG}$ | System Voltage Regulation, measured on $V_{SYS}$ | | 5.00 | | 23.00 | V |
| $V_{SYSMIN_REG_ACC}$ | Minimum System Voltage Regulation Accuracy (VBAT below REG0x3E() setting) | VSYS_MIN() = 0x0C08H | | 15.40 | | V |
| | | | –0.9% | | 0.9% | |
| | | VSYS_MIN() = 0x099CH | | 12.30 | | V |
| | | | –0.9% | | 0.9% | |
| | | VSYS_MIN() = 0x0730H | | 9.20 | | V |
| | | | –1.3% | | 1.1% | |
| | | VSYS_MIN() = 0x0528H | | 6.60 | | V |
| | | | –1.5% | | 1.50% | |
| **CHARGE VOLTAGE REGULATION** | | | | | | |
| $V_{BAT_RNG}$ | Battery voltage regulation | | 5.00 | | 23.00 | V |
| $V_{BAT_REG_ACC}$ | Battery voltage regulation accuracy (charge enable) (0°C to 85°C) | CHARGE_VOLTAGE() = 0x1482H | | 21.0 | | V |
| | | | –0.5% | | 0.6% | |
| | | CHARGE_VOLTAGE()= 0x1068H | | 16.8 | | V |
| | | | –0.5% | | 0.6% | |
| | | CHARGE_VOLTAGE() = 0x0C4EH | | 12.6 | | V |
| | | | –0.5% | | 0.6% | |
| | | CHARGE_VOLTAGE() = 0x0834H | | 8.4 | | V |
| | | | –0.5% | | 0.6% | |
| **CHARGE CURRENT REGULATION IN FAST CHARGE** | | | | | | |
| $V_{IREG_CHG_RNG}$ | Charge current regulation differential voltage range with 5-mΩ sensing resistor | $V_{IREG_CHG}$ = $V_{SRP}$ – $V_{SRN}$ | 128 | | 16320 | mA |


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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CHRG_REG_ACC}$ | Charge current regulation accuracy 5-mΩ sensing resistor, VBAT above VSYS_MIN() setting (0°C to 85°C) | CHARGE_CURRENT() = 0x600H, VBAT=7.4V/11.1V/14.8V/18.5V | | 12288 | | mA |
| | | | –1.5% | | 1.5% | |
| | | CHARGE_CURRENT() = 0x400H, VBAT=7.4V/11.1V/14.8V/18.5V | | 8192 | | mA |
| | | | –2.0% | | 2.0% | |
| | | CHARGE_CURRENT() = 0x200H, VBAT=7.4V/11.1V/14.8V/18.5V | | 4096 | | mA |
| | | | –3.0% | | 3.0% | |
| | | CHARGE_CURRENT() = 0x100H, VBAT=7.4V/11.1V/14.8V/18.5V | | 2048 | | mA |
| | | | –5.0% | | 5.0% | |
| | | CHARGE_CURRENT() = 0x080H VBAT=7.4V/11.1V/14.8V/18.5V | | 1024 | | mA |
| | | | –8.0% | | 8.0% | |
| **CHARGE CURRENT REGULATION IN PRE-CHARGE(LDO MODE)** | | | | | | |
| $V_{PRECHG_RANGE}$ | Pre-charge Current Range 5-mΩ SRP/SRN series resistor, VBAT below REG0x3E() setting (0°C to 85°C) | $V_{IREG_PRECHG}$ = $V_{SRP}$ - $V_{SRN}$, IPRECHG() = 0x10H~0xFCH | 128 | | 2016 | mA |
| $I_{PRECHRG_REG_ACC}$ | Pre-charge current regulation accuracy with 5-mΩ SRP/SRN series resistor, VBAT below VSYS_MIN() setting (0°C to 85°C) RSNS_RSR=0b | IPRECHG() = 0x80H,CHARGE_CURRENT() = 0x100H | | 1024 | | mA |
| | | | –10.0% | | 10.0% | |
| | | IPRECHG() = 0x40H,CHARGE_CURRENT() = 0x100H | | 512 | | mA |
| | | | –15.0% | | 15.0% | |
| | | IPRECHG() = 0x20H,CHARGE_CURRENT() = 0x100H | | 256 | | mA |
| | | | –20.0% | | 20.0% | |
| | | IPRECHG() = 0x10H,CHARGE_CURRENT() = 0x100H | | 128 | | mA |
| | | | –30.0% | | 30.0% | |
| **TERMINATION CURRENT AND RECHARGE(AUTONOMOUS CHARGING)** | | | | | | |
| $V_{TERM_RANGE}$ | Termination Current Range 5-mΩ SRP/SRN series resistor, VBAT below REG0x3E() setting (0°C to 85°C) | $V_{IREG_TERM}$ = $V_{SRP}$ - $V_{SRN}$, ITERM() = 0x10H~0xFCH | 128 | | 2016 | mA |
| $V_{RECHG}$ | Battery automatic recharge threshold(0°C to 85°C) | VSRN falling threshold as negative offset based on CHARGE_VOLTAGE()=12.6V, VRECHG()=1111b | | 800.0 | | mV |
| | | VSRN falling threshold as negative offset based on CHARGE_VOLTAGE()=12.6V,VRECHG()=0111b | | 400.0 | | mV |
| | | VSRN falling threshold as negative offset based on CHARGE_VOLTAGE()=12.6V,VRECHG()=0011b | | 200.0 | | mV |
| | | VSRN falling threshold as negative offset based on CHARGE_VOLTAGE()=12.6V,VRECHG()=0001b | | 100.0 | | mV |
| **INPUT CURRENT REGULATION** | | | | | | |

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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IREG_DPM_RNG}$ | Input current regulation range with 10-mΩ ACP/ACN series resistor | $V_{IREG_DPM}$ = $V_{ACP_A}$ – $V_{ACN_A}$ +$V_{ACP_B}$ - $V_{ACN_B}$ | 400 | | 8200 | mA |
| $I_{IIN_DPM_REG_ACC}$ | Input current regulation accuracy with 10-mΩ ACP/ACN series resistor | IIN_HOST() = 0x0C4H | 4750 | 4900 | 5000 | mA |
| | | IIN_HOST() = 0x074H | 2800 | 2900 | 3000 | mA |
| | | IIN_HOST() = 0x024H | 800 | 900 | 1000 | mA |
| | | IIN_HOST() = 0x010H | 300 | 400 | 510 | mA |
| $V_{IREG_DPM_RNG_ILIM}$ | Voltage range for input current regulation (ILIM_HIZ Pin) | | 1.15 | | 4.0 | V |
| $I_{IIN_DPM_REG_ACC_ILIM}$ | Input Current Regulation Accuracy on ILIM_HIZ pin $V_{ILIM_HIZ}$ = 1 V + 40 × $I_{IIN_DPM}$ × $R_{AC}$, with 10-mΩ ACP/ACN series resistor | $V_{ILIM_HIZ}$ = 3.0 V | 4800 | 5000 | 5200 | mA |
| | | $V_{ILIM_HIZ}$ = 2.2 V | 2800 | 3000 | 3200 | mA |
| | | $V_{ILIM_HIZ}$ = 1.4 V | 800 | 1000 | 1200 | mA |
| | | $V_{ILIM_HIZ}$ = 1.2 V | 300 | 500 | 700 | mA |
| $I_{LEAK_ILIM}$ | ILIM_HIZ pin leakage current | | –1 | | 1 | µA |
| **INPUT VOLTAGE REGULATION** | | | | | | |
| **OTG CURRENT REGULATION** | | | | | | |
| $V_{IOTG_REG_RNG}$ | OTG output current regulation range with 10-mΩ ACP/ACN series resistor | $V_{IOTG_REG}$ = $V_{ACP_A}$ – $V_{ACN_A}$ +$V_{ACP_B}$ - $V_{ACN_B}$ | 100 | | 3000 | mA |
| $I_{OTG_ACC}$ | OTG output current regulation accuracy with 25-mA LSB and 10-mΩ ACP/ACN series resistor | OTG_Current() = 0x078H | 2850 | 3000 | 3150 | mA |
| | | OTG_Current() = 0x03CH | 1350 | 1500 | 1650 | mA |
| | | OTG_Current() = 0x014H | 350 | 500 | 650 | mA |
| **OTG VOLTAGE REGULATION** | | | | | | |
| $V_{OTG_REG_RNG}$ | OTG voltage regulation range | Voltage on VBUS | 3 | | 5 | V |
| $V_{OTG_REG_ACC}$ | OTG voltage regulation accuracy | OTG_Voltage()=0x0FAH | | 5.00 | | V |
| $V_{OTG_REG_ACC}$ | OTG voltage regulation accuracy | | –3% | | 3% | |
| **REGN REGULATOR** | | | | | | |
| $V_{REGN_REG}$ | REGN regulator voltage | VBUS = 10 V, REGN_EXT=0b | 4.80 | 5.00 | 5.10 | V |
| $V_{REGN_REG_EXT}$ | REGN regulator voltage with external over drive | VBUS = 10 V, REGN_EXT=1b | 4.35 | 4.50 | 4.65 | V |
| $I_{REGN_LIM_CHARGING}$ | REGN current limit when converter is enabled | VBUS = 10 V, force $V_{REGN}$ =4 V | 150.00 | 191.00 | | mA |
| $I_{REGN_LIM_LWPWR}$ | REGN current limit when in battery only low power mode | VBUS = 0 V, $V_{VBAT}$ = 18 V, force $V_{REGN}$ =4 V, EN_LWPWR=1b, EN_REGN_LWPWR=1b, | 3.00 | 12.00 | | mA |
| $V_{REGN_OK_FALL}$ | REGN regulator voltage valid falling threshold | | 2.8 | 3.20 | | V |
| $V_{REGN_OK_RISE}$ | REGN regulator voltage valid rising threshold | | 3.10 | 3.40 | 3.60 | V |
| $V_{REGN_OV_RISE}$ | REGN regulator voltage over voltage rising threshold | | 5.30 | 5.50 | 5.60 | V |
| $V_{REGN_OV_FALL}$ | REGN regulator voltage over voltage falling threshold | | 5.10 | 5.30 | 5.50 | V |
| **QUIESCENT CURRENT** | | | | | | |
| $I_{SD_BAT}$ | System powered by battery. $I_{SRN}$ + $I_{SRP}$ + $I_{SW2}$ + $I_{BTST2}$ + $I_{SW1_A\&B}$ + $I_{BTST1_A\&B}$ + $I_{ACP_A\&B}$ + $I_{ACN_A\&B}$ + $I_{VBUS}$ + $I_{VSYS}$ | VBAT = 18 V, in low power mode(EN_LWPWR = 1b), Comparator off(EN_LWPWR_CMP=0b, CMP_EN=1b), BATDRV is Off (BATFET_ENZ=1b), REGN is off(EN_REGN_LWPWR=0b), PSYS is off(PSYS_CONFIG=11b), Continuous ADC is off(ADC_RATE=1b) | | 12.0 | 20.0 | µA |


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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{Q_BAT1}$ | System powered by battery. $I_{SRN}$ + $I_{SRP}$ + $I_{SW2}$ + $I_{BTST2}$ + $I_{SW1_A\&B}$ + $I_{BTST1_A\&B}$ + $I_{ACP_A\&B}$ + $I_{ACN_A\&B}$ + $I_{VBUS}$ + $I_{VSYS}$ | VBAT = 18 V, in low power mode(EN_LWPWR = 1b), Comparator off(EN_LWPWR_CMP=0b), BATDRV is On (BATFET_ENZ=0b, CMP_EN=1b), REGN is off(EN_REGN_LWPWR=0b), PSYS is off(PSYS_CONFIG=11b), IBAT is off(EN_IBAT=0b), Continuous ADC is off(ADC_RATE=1b) | | 20 | 30 | µA |
| $I_{Q_BAT2}$ | System powered by battery. $I_{SRN}$ + $I_{SRP}$ + $I_{SW2}$ + $I_{BTST2}$ + $I_{SW1_A\&B}$ + $I_{BTST1_A\&B}$ + $I_{ACP_A\&B}$ + $I_{ACN_A\&B}$ + $I_{VBUS}$ + $I_{VSYS}$ | VBAT = 18 V, in low power mode(EN_LWPWR = 1b), Comparator on(EN_LWPWR_CMP=1b, CMP_EN=1b), BATDRV is On (BATFET_ENZ=0b), REGN is off (EN_REGN_LWPWR=0b), PSYS is off(PSYS_CONFIG=11b), IBAT is off(EN_IBAT=0b), Continuous ADC is off(ADC_RATE=1b) | | 30 | 45 | µA |
| $I_{Q_BAT3}$ | System powered by battery. $I_{SRN}$ + $I_{SRP}$ + $I_{SW2}$ + $I_{BTST2}$ + $I_{SW1_A\&B}$ + $I_{BTST1_A\&B}$ + $I_{ACP_A\&B}$ + $I_{ACN_A\&B}$ + $I_{VBUS}$ + $I_{VSYS}$ | VBAT = 18 V, in low power mode(EN_LWPWR = 1b, CMP_EN=1b), Comparator on(EN_LWPWR_CMP=1b),BATDRV is On (BATFET_ENZ=0b), REGN is on scaled down to 5mA (EN_REGN_LWPWR=1b), PSYS is off(PSYS_CONFIG=11b), IBAT is off(EN_IBAT=0b), Continuous ADC is off(ADC_RATE=1b) | | 110 | 150 | µA |
| $I_{Q_BAT4}$ | System powered by battery. $I_{SRN}$ + $I_{SRP}$ + $I_{SW2}$ + $I_{BTST2}$ + $I_{SW1_A\&B}$ + $I_{BTST1_A\&B}$ + $I_{ACP_A\&B}$ + $I_{ACN_A\&B}$ + $I_{VBUS}$ + $I_{VSYS}$ | VBAT = 18 V, in performance mode(EN_LWPWR = 0b, CMP_EN=1b), Comparator on(EN_LWPWR_CMP=1b),BATDRV is On (BATFET_ENZ=0b), REGN is on in full power,PSYS is on(PSYS_CONFIG=00b), IBAT is on(EN_IBAT=1b), Continuous ADC is off(ADC_RATE=1b) | | 800 | 1000 | µA |
| $I_{Q_BAT5}$ | System powered by battery. $I_{SRN}$ + $I_{SRP}$ + $I_{SW2}$ + $I_{BTST2}$ + $I_{SW1_A\&B}$ + $I_{BTST1_A\&B}$ + $I_{ACP_A\&B}$ + $I_{ACN_A\&B}$ + $I_{VBUS}$ + $I_{VSYS}$ | VBAT = 18 V, in performance mode(EN_LWPWR = 0b), Comparator on(EN_LWPWR_CMP=1b, CMP_EN=1b),BATDRV is On (BATFET_ENZ=0b), REGN is on in full power,PSYS is On(PSYS_CONFIG=00b), IBAT is on(EN_IBAT=1b),Continuous ADC is on(ADC_RATE=0b, ADC_EN=1b, enable at least 1 channel EN_ADC_VBAT=1b) | | 950 | 1100 | µA |
| $I_{Q_HIZ}$ | Converter under HIZ mode and system powered by battery. $I_{SRN}$ + $I_{SRP}$ + $I_{SW2}$ + $I_{BTST2}$ + $I_{SW1_A\&B}$ + $I_{BTST1_A\&B}$ + $I_{ACP_A\&B}$ + $I_{ACN_A\&B}$ + $I_{VBUS}$ + $I_{VSYS}$ | VIN = 28 V, VBAT = 12.6 V, 3s, EN_HIZ=1b; in HIZ mode | | 1000 | 1150 | µA |
| $I_{Q_VAC}$ | Input current in buck mode, no load, $I_{VBUS}$ + $I_{ACP}$ + $I_{ACN}$ + $I_{VSYS}$ + $I_{SRP}$ + $I_{SRN}$ + $I_{SW1}$ + $I_{BTST}$ + $I_{SW2}$ + $I_{BTST2}$ | VIN = 28 V, VBAT = 12.6 V, 3s, EN_LEARN=1b, no switching | | 1000 | 1150 | mA |
| | | VIN = 28 V, VBAT = 12.6 V, 3s, EN_OOA = 0b; switching at zero load | | 2.50 | | mA |
| **CURRENT SENSE AMPLIFIER** | | | | | | |
| $V_{IADPT_CLAMP}$ | $I_{ADPT}$ output clamp voltage | | 3.1 | 3.2 | 3.3 | V |
| $I_{IADPT}$ | $I_{ADPT}$ output current | | 1 | | 2.5 | mA |

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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $A_{IADPT}$ | Input current sensing gain | $V_{(IADPT)}$ / ($V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$), IADPT_GAIN = 0 | | 20 | | V/V |
| | | $V_{(IADPT)}$ / ($V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$), IADPT_GAIN = 1 | | 40 | | V/V |
| $V_{IADPT_ACC}$ | Input current monitor accuracy | $V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$ = 61.44 mV, IADPT_GAIN = 0 | –2.5% | | 1.5% | |
| | | $V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$ = 40.96 mV, IADPT_GAIN = 0 | –3.5% | | 2% | |
| | | IADPT_GAIN = 0$V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$ = 20.48 mV, IADPT_GAIN = 0 | –6% | | 3% | |
| | | $V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$ =10.24 mV, IADPT_GAIN = 0 | –15% | | 6% | |
| | | $V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$ =5.12 mV, IADPT_GAIN = 0 | –25% | | 10% | |
| $C_{IADPT_MAX}$ | Maximum capacitance at IADPT Pin | | | | 100 | pF |
| $V_{IBAT_CLAMP}$ | IBAT output clamp voltage | | 3.1 | 3.2 | 3.3 | V |
| $I_{IBAT}$ | IBAT output current | | 1 | | 2.5 | mA |
| $A_{IBAT}$ | Charge and discharge current sensing gain on IBAT pin | $V_{(IBAT)}$ / $V_{(SRN-SRP)}$, IBAT_GAIN = 0, | | 8 | | V/V |
| | | $V_{(IBAT)}$ / $V_{(SRN-SRP)}$, IBAT_GAIN = 1, | | 64 | | V/V |
| $I_{IBAT_CHG_ACC}$ | Charge and discharge current monitor accuracy on IBAT pin | $V_{SRN}$-$V_{SRP}$= 61.44 mV, IBAT_GAIN=0b | –1.5% | | 2% | |
| | | $V_{SRN}$-$V_{SRP}$= 40.96 mV, IBAT_GAIN=0b | –2% | | 3% | |
| | | $V_{SRN}$-$V_{SRP}$= 20.48 mV, IBAT_GAIN=0b | –3% | | 7% | |
| | | $V_{SRN}$-$V_{SRP}$= 10.24 mV, IBAT_GAIN=0b | –6% | | 13% | |
| | | $V_{SRN}$-$V_{SRP}$= 5.12 mV, IBAT_GAIN=0b | –12% | | 27% | |
| $C_{IBAT_MAX}$ | Maximum capacitance at IBAT Pin | | | | 100 | pF |
| **SYSTEM POWER SENSE AMPLIFIER** | | | | | | |
| $V_{PSYS}$ | PSYS output voltage range | | 0 | | 3.3 | V |
| $I_{PSYS}$ | PSYS output current | | 0 | | 260.00 | µA |
| $A_{PSYS}$ | PSYS system gain | $I_{(PSYS)}$ / ($P_{(IN)}$ +$P_{(BAT)}$), PSYS_CONFIG =00b;PSYS_RATIO =1b | | 1 | | µA/W |
| $V_{PSYS_ACC_ADPT}$ | PSYS gain accuracy (PSYS_CONFIG = 00b) | Adapter only monitor system power: VBUS= 28 V IBUS=3.6A (100W), TA = 0 to 85°C, PSYS_RATIO=1b, RAC=10mΩ, RSR=5mΩ. | –3% | | 4.5% | |
| $V_{PSYS_ACC_BAT}$ | PSYS gain accuracy (PSYS_CONFIG = 00b) | Battery only monitor system power: VBAT= 11.1 V IBAT=9.1A (100W), TA = 0 to 85°C, PSYS_RATIO=1b, RAC=10mΩ, RSR=5mΩ. | –3.5% | | 2% | |
| $V_{PSYS_CLAMP}$ | PSYS clamp voltage | | 3.1 | | 3.3 | V |
| **INTEGRATED ANALOG TO DIGITAL CONVERSION (ADC)** | | | | | | |
| $ADC_{RES}$ | ADC Effective resolution | ADC_SAMPLE[1:0]=00b | 14 | 15 | | bits |
| $ADC_{RES}$ | ADC Effective resolution | ADC_SAMPLE[1:0]=01b | 13 | 14 | | bits |
| $ADC_{RES}$ | ADC Effective resolution | ADC_SAMPLE[1:0]=10b | 12 | 13 | | bits |
| ADC_VBUS | ADC Input voltage reading at ADC_VBUS() register | Range | 0 | | 65534 | mV |
| | | LSB | | 2 | | mV |
| | | Accuracy at VIN=28V | –2 | | 2 | % |


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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ADC_IIN | ADC Input voltage reading at ADC_IIN() register | Range | –16383.5 | | 16383.5 | mA |
| | | LSB based on 10mohm RAC | | 0.5 | | mA |
| | | Accuracy at $V_{ACP_A}$-$V_{ACN_A}$+$V_{ACP_B}$-$V_{ACN_B}$ = 50 mV | –4 | | 2.5 | % |
| ADC_VSYS | ADC Input voltage reading at ADC_VSYS() register | Range | 0 | | 65534 | mV |
| | | LSB | | 2 | | mV |
| | | Accuracy at VSYS=9V | –2 | | 2 | % |
| ADC_VBAT | ADC Input voltage reading at ADC_VBAT() register | Range | 0 | | 32767 | mV |
| | | LSB | | 1 | | mV |
| | | Accuracy at VBAT=9V | –2 | | 1 | % |
| ADC_PSYS | ADC Input voltage reading at ADC_PSYS() register | Range | 0 | | 4095 | mV |
| | | LSB | | 1 | | mV |
| | | Accuracy at V_PSYS=2V | –2 | | 2 | % |
| ADC_CMPIN_TR | ADC Input voltage reading at ADC_CMPIN_TR() register | Range | 0 | | 4095 | mV |
| | | LSB | | 1 | | mV |
| | | Accuracy at V_CMPIN_TR=2V | –2 | | 2 | % |
| **CMPIN_TR PIN Voltage under TEMPERATURE REGULATION(TREG)** | | | | | | |
| $V_{TREG}$ | CMPIN_TR pin voltage under temperature regulation | | | 1.200 | | V |
| $V_{TREG_ACC}$ | CMPIN_TR pin voltage accuracy under temperature regulation | | –2.0% | | 2.0% | |
| $V_{TREG_PP}$ | TREG PROCHOT PROFILE thereshold level | | 1.07 | 1.100 | 1.13 | V |
| **SLEEP COMPARATOR FOR FORWARD MODE BETWEEN VBUS and ACP_A(SC_VBUSACP)** | | | | | | |
| $V_{SC_VBUSACP_rising}$ | VBUS-ACP_A rising threshold for sleep comparator to shut down converter when Efuse/PFET is not fully on | | 700 | 850 | 1000 | mV |
| $V_{SC_VBUSACP_falling}$ | VBUS-ACP_A falling threshold for sleep comparator to recover converter swithcing after Efuse/PFET is fully on | | 650 | 800 | 950 | mV |
| **HIGH DUTY BUCK EXIT COMPARATOR (HDBCP)** | | | | | | |
| $V_{HDBCP_VSYS_RISE}$ | VSYS rising/ VBUS falling threshold for comparator to exit high duty buck mode by forcing HIGH_DUTY_BUCK=0b | | 97.2% | 97.7% | 98.2% | |
| $V_{HDBCP_HYS}$ | Hystersis when VSYS falling/VBUS rising based on 97.5%*VBUS threshold to allow writing HIGH_DUTY_BUCK bit to 1b | | | 200.0 | | mV |
| $t_{HDBCP_VSYS_DEG}$ | Comparator deglitch time for both rising and falling edge | | | 15.0 | | us |
| **VMIN ACTIVE PROTECTION(VAP) PROCHOT COMPARATOR** | | | | | | |
| $V_{SYS_TH1Z}$ | VAP VSYS rising threshold 1 | VSYS_TH1()=001110b | 6.4 | 6.55 | 6.7 | V |
| $V_{SYS_TH1}$ | VAP VSYS falling threshold 1 | VSYS_TH1()=001110b | 6.25 | 6.4 | 6.55 | V |
| $V_{SYS_TH1_HYST}$ | VAP VSYS threshold 1 hysteresis | | | 150 | | mV |
| $V_{SYS_TH2Z}$ | VAP VSYS rising threshold 2 | VSYS_TH2()=001001b | 5.9 | 6.05 | 6.20 | V |
| $V_{SYS_TH2}$ | VAP VSYS falling threshold 2 | VSYS_TH2()=001001b | 5.75 | 5.9 | 6.05 | V |

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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{SYS_TH2_HYST}$ | VAP VSYS threshold 2 hysteresis | | | 150 | | mV |
| $V_{BUS_VAP_THZ}$ | Convervative VAP VBUS rising threshold | VBUS_VAP_TH()=0000000b | 3.35 | 3.5 | 3.65 | V |
| $V_{BUS_VAP_TH}$ | Convervative VAP VBUS falling threshold | VBUS_VAP_TH()=0000000b | 3.05 | 3.2 | 3.35 | V |
| $V_{BUS_VAP_TH_HYST}$ | Convervative VAP VBUS threshold hysteresis | | | 300 | | mV |
| **PEAK POWER MODE LEVEL2 ADAPTER CURRENT LIMIT(ILIM2)** | | | | | | |
| $I_{LIM2_VTH}$ | Based on percentage of IINDPM(ILIM1) level | ILIM2_VTH=01001b | | 150% | | |
| $V_{ILIM2_CEILING}$ | ILIM2 high clamp based on dual phase total input current sense voltage ACP_A -ACN_A +ACP_B -ACN_B | Set IIN_HOST() to maximum, and ILIM2_VTH=11110b | 240 | 258 | 275 | mV |
| **PEAK POWER MODE SYSTEM VOLTAGE SAG COMPARATOR(SYS_SAG)** | | | | | | |
| $V_{SYS_SAG}$ | VSYS undershoot comparator threshold to trigger peak power mode ILIM2 as percentage of VSYS_MIN() | EN_PKPWR_VSYS=1b | 91.4% | 93.25% | 95.0% | |
| $V_{SYS_SAG_HYST}$ | VSYS undervoltage hysteresis | | | 100 | | mV |
| **VSYS UNDER VOLTAGE PROTECTION COMPARATOR(VSYS_UVP)** | | | | | | |
| $V_{SYS_UVLOZ}$ | VSYS undervoltage rising threshold | VSYS rising | 2.35 | 2.55 | 2.75 | V |
| $V_{SYS_UVLO}$ | VSYS undervoltage falling threshold | VSYS falling VSYS_UVP()=000b | 2.2 | 2.4 | 2.6 | V |
| $V_{SYS_UVLOZ}$ | VSYS undervoltage rising threshold | VSYS rising | 4.75 | 4.95 | 5.15 | V |
| $V_{SYS_UVLO}$ | VSYS undervoltage falling threshold | VSYS falling VSYS_UVP()=011b | 4.6 | 4.8 | 5.0 | V |
| $V_{SYS_UVLOZ}$ | VSYS undervoltage rising threshold | VSYS rising | 7.15 | 7.35 | 7.55 | V |
| $V_{SYS_UVLO}$ | VSYS undervoltage falling threshold | VSYS falling VSYS_UVP()=110b | 7.0 | 7.2 | 7.4 | V |
| **VBUS UNDER VOLTAGE LOCKOUT COMPARATOR(VBUS_UVLO)** | | | | | | |
| $V_{VBUS_UVLOZ}$ | VBUS undervoltage rising threshold | VBUS rising | 2.5 | 2.7 | 2.9 | V |
| $V_{VBUS_UVLO}$ | VBUS undervoltage falling threshold | VBUS falling | 2.3 | 2.6 | 2.8 | V |
| $V_{VBUS_CONVEN}$ | VBUS converter enable rising threshold | VBUS rising | 3.1 | 3.4 | 3.7 | V |
| $V_{VBUS_CONVENZ}$ | VBUS converter enable falling threshold | VBUS falling | 2.9 | 3.2 | 3.5 | V |
| **VBAT UNDER VOLTAGE LOCKOUT COMPARATOR(VBAT_UVLO)** | | | | | | |
| $V_{VBAT_UVLOZ}$ | VBAT undervoltage rising threshold | VSRN rising | 3.5 | 3.95 | 4.25 | V |
| $V_{VBAT_UVLO}$ | VBAT undervoltage falling threshold | VSRN falling | 3.3 | 3.75 | 4.05 | V |
| $V_{VBAT_UVLO_HYST}$ | VBAT undervoltage hysteresis | | | 200 | | mV |
| $V_{VBAT_OTGEN}$ | VBAT OTG enable rising threshold | VSRN rising | 4.80 | 5.0 | 5.20 | V |
| $V_{VBAT_OTGENZ}$ | VBAT OTG enable falling threshold | VSRN falling | 4.45 | 4.65 | 4.85 | V |
| $V_{VBAT_OTGEN_HYST}$ | VBAT OTG enable hysteresis | | | 350 | | mV |
| **VBUS UNDER VOLTAGE PROTECTION COMPARATOR (OTG MODE)** | | | | | | |
| $V_{VBUS_OTG_UV}$ | VBUS undervoltage falling threshold | As percentage of OTG_VOLTAGE() setting | 65% | 75% | 85% | |
| $V_{VBUS_OTG_UVZ}$ | VBUS undervoltage rising threshold hysteresis based on falling threshold | | | 100 | | mV |
| **VBUS OVER VOLTAGE PROTECTION COMPARATOR (OTG MODE)** | | | | | | |
| $V_{VBUS_OTG_OV}$ | VBUS overvoltage rising threshold | As percentage of OTG_VOLTAGE() setting= 12V | 110% | 118% | 125% | |


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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VBUS_OTG_OVZ}$ | VBUS overvoltage falling threshold | As percentage of OTG_VOLTAGE() setting= 12V | 100% | 105% | 110% | |
| **PRE-CHARGE to FAST CHARGE COMPARATOR** | | | | | | |
| $V_{BAT_PRECHG_Z}$ | VBAT rising threshold | VBAT rising as negative offset of VSYS_MIN() | -150 | 50 | 200 | mV |
| $V_{BAT_PRECHG}$ | VBAT falling threshold | VBAT falling as negative offset of VSYS_MIN() | -50 | 150 | 300 | mV |
| $V_{BAT_PRECHG_HYST}$ | VBAT hysterisis | | | 100 | | mV |
| **TRICKLE CHARGE to PRE-CHARGE TRANSITION** | | | | | | |
| $V_{BAT_SHORT_Z}$ | VBAT short rising threshold | VBAT rising | 2.9 | 3.0 | 3.1 | V |
| $V_{BAT_SHORT}$ | VBAT short falling threshold | VBAT falling | 2.80 | 2.9 | 3.0 | V |
| $V_{BAT_SHORT_HYST}$ | VBAT short hysteresis | | | 100.0 | | mV |
| $I_{BAT_SHORT}$ | VBAT short trickle charge current maximum clamp | | | 128.0 | | mA |
| **INPUT OVER CURRENT COMPARATOR (ACOC)** | | | | | | |
| $V_{ACOC}$ | ACP to ACN rising threshold, w.r.t. ILIM2 in REG0x33[15:11] | Voltage across input sense resistor rising, Reg0x31[2] = 1 | 170 | 200 | 230 | % |
| $V_{ACOC_FLOOR}$ | ACOC low clamp based on dual phase total input current sense ACP_A -ACN_A +ACP_B -ACN_B | Set IIN_HOST() to minimum | 46 | 50 | 54 | mV |
| $V_{ACOC_CEILING}$ | ACOC high clamp based on dual phase total input current sense ACP_A -ACN_A +ACP_B -ACN_B | Set IIN_HOST() to maximum | 174 | 180 | 184 | mV |
| **SYSTEM OVER-VOLTAGE COMPARATOR (SYSOVP)** | | | | | | |
| $V_{SYSOVP_RISE}$ | System overvoltage rising threshold to turn off converter | 2 s | 11.85 | 12.15 | 12.35 | V |
| | | 3 s | 16.8 | 17.15 | 17.4 | V |
| | | 4 s | 21.90 | 22.3 | 22.60 | V |
| | | 5 s | 26.90 | 27.3 | 27.70 | V |
| $V_{SYSOVP_FALL}$ | System overvoltage falling threshold | 2 s | | 11.6 | | V |
| | | 3 s | | 16.60 | | V |
| | | 4 s | | 21.7 | | V |
| | | 5 s | | 26.80 | | V |
| $I_{SYSOVP}$ | Discharge current during SYSOVP | Through VSYS pin | | 20 | | mA |
| **BAT OVER-VOLTAGE COMPARATOR (BATOVP)** | | | | | | |
| $V_{BATOVP_RISE}$ | Overvoltage rising threshold as percentage of CHARGE_VOLTAGE() | 2 s - 5 s | 107.8% | 108.8% | 109.6% | |
| $V_{BATOVP_FALL}$ | Overvoltage falling threshold as percentage of CHARGE_VOLTAGE() | 2 s - 5 s | 104.4% | 105.5% | 106.5% | |
| $V_{BATOVP_HYST}$ | Overvoltage hysteresis as percentage of CHARGE_VOLTAGE() | 2 s - 5 s | | 3.3% | | |
| $I_{BATOVP}$ | Discharge current during BATOVP | Through VSYS pin | | 20 | | mA |
| **CONVERTER OVER-CURRENT COMPARATOR (OCP_SW2)** | | | | | | |
| $V_{OCP_LIMIT_SW2}$ | Converter Over-Current Limit through Q4 VDS | OCP_SW2_HIGH_RANGE=0 | | 150 | | mV |
| | | OCP_SW2_HIGH_RANGE=1 | | 260 | | mV |
| $V_{OCP_LIMIT__SYSSHORT_SW2}$ | Under OTG_UVP, Converter Over-Current Limit through and Q4 VDS | OCP_SW2_HIGH_RANGE=0 | | 90 | | mV |
| | | OCP_SW2_HIGH_RANGE=1 | | 150 | | mV |
| **CONVERTER OVER-CURRENT COMPARATOR (OCP_SW1X)** | | | | | | |

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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OCP_LIMIT_SW1X_RAC}$ | Converter Over-Current Limit through RAC | OCP_SW1X_HIGH_RANGE=0 | | 150 | | mV |
| | | OCP_SW1X_HIGH_RANGE=1 | | 260 | | mV |
| $V_{OCP_LIMIT_SYSSHORT_SW1X_RAC}$ | Under SYS_UVP, Converter Over-Current Limit through RAC | OCP_SW1X_HIGH_RANGE=0 | | 90 | | mV |
| | | OCP_SW1X_HIGH_RANGE=1 | | 150 | | mV |
| **THERMAL SHUTDOWN COMPARATOR** | | | | | | |
| $T_{SHUT_RISE}$ | Thermal shutdown rising temperature | Temperature increasing | | 155 | | °C |
| $T_{SHUT_FALL}$ | Thermal shutdown falling temperature | Temperature reducing | | 135 | | °C |
| $T_{SHUT_HYS}$ | Thermal shutdown hysteresis | | | 20 | | °C |
| **ICRIT PROCHOT COMPARATOR** | | | | | | |
| $V_{ICRIT_PRO}$ | Input current rising threshold for throttling as 10% above ILIM2_VTH() | Only when ILIM2 setting is higher than 4A | 104.5% | 110% | 117.5% | |
| **INOM PROCHOT COMPARATOR** | | | | | | |
| $V_{INOM_PRO}$ | INOM rising threshold as 10% above IIN_DPM() and EN_EXTILIM=0b | Accuracy is ensured only when IIN_DPM() is 2A or higher. There is minimum clamp at 500mA. Accuracy between 500mA and 2A may be impaired. | 104% | 110% | 117% | |
| **BATTERY DISCHARGE CURRENT LIMIT PROCHOT COMPARATOR(IDCHG_TH1 and IDCHG_TH2)** | | | | | | |
| $I_{DCHG_TH1}$ | IDCHG threshold1 voltage across SRN and SRP pins for throttling CPU | IDCHG_TH1()=010000b | | 47.5 | | mV |
| | | | –3.0% | | 3.2% | |
| $I_{DCHG_DGLT1}$ | IDCHG threshold1 deglitch time | IDCHG_DEG1()=01b | | 1.25 | | sec |
| $I_{DCHG_TH2}$ | IDCHG threshold2 voltage across SRN and SRP pins | IDCHG_TH1()=010000b, IDCHG_TH2()=001b | | 71.25 | | mV |
| | | | –3.0% | | 3.2% | |
| $I_{DCHG_DGLT2}$ | IDCHG threshold2 deglitch time | IDCHG_DEG2()=01b | | 1.6 | | ms |
| **INDEPENDENT COMPARATOR** | | | | | | |
| $V_{INDEP_CMP}$ | Independent comparator threshold | Comparator CMPIN_TR threshold to trigger CMPOUT pulling down, Negative polarity CMP_POL=0b. | 1.18 | 1.2 | 1.23 | V |
| $V_{INDEP_CMP_HYS}$ | Independent comparator hysteresis | Comparator CMPIN_TR hysterisis threshold | | 100 | | mV |
| **PWM OSCILLATOR AND RAMP** | | | | | | |
| $F_{SW}$ | PWM switching frequency | PWM_FREQ= 0 | 690 | 770 | 850 | kHz |
| $F_{SW}$ | PWM switching frequency | PWM_FREQ= 1 | 540 | 600 | 660 | kHz |
| **BATFET GATE DRIVER (BATDRV for NFET)** | | | | | | |
| $V_{BATDRV_ON}$ | Gate drive voltage on NMOS BATFET | | 4.70 | 5.00 | 5.40 | V |
| $V_{BATDRV_SUPPLEMENT}$ | BATFET Source-Drain voltage during ideal diode regulation under supplement mode | | | 30.00 | | mV |
| $I_{BATDRV_ON}$ | BATDRV on, VBATDRV=VBAT+2V | | 30 | 40 | | µA |
| $I_{BATDRV_OFF}$ | BATDRV off, BATDRV=VBAT+2V | | 0.54 | 0.85 | | mA |
| **PWM HIGH SIDE DRIVER (HIDRV1_A for Q1_A, HIDRV1_B for Q1_B)** | | | | | | |
| $R_{DS_HI_ON_Q1}$ | High side driver (HSD) turn on resistance | $V_{BTST1}$ - $V_{SW1}$ = 4.5 V | | 1.00 | | Ω |
| $R_{DS_HI_OFF_Q1}$ | High side driver turn off resistance | $V_{BTST1}$ - $V_{SW1}$ = 4.5 V | | 0.4 | 0.6 | Ω |
| $V_{BTST1_REFRESH}$ | Bootstrap refresh comparator falling threshold voltage | $V_{BTST1}$ - $V_{SW1}$ when low side refresh pulse is requested | 3.0 | 3.3 | 3.6 | V |
| **PWM LOW SIDE DRIVER (LODRV1_A for Q2_A, LODRV1_B for Q2_B)** | | | | | | |


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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DS_LO_ON_Q2}$ | Low side driver (LSD) turn on resistance | $V_{BTST1}$ - $V_{SW1}$ = 4.5 V | | 1.0 | | Ω |
| $R_{DS_LO_OFF_Q2}$ | Low side driver turn off resistance | $V_{BTST1}$ - $V_{SW1}$ = 4.5 V | | 0.4 | 0.6 | Ω |
| **PWM HIGH SIDE DRIVER (HIDRV2 for Q4)** | | | | | | |
| $R_{DS_HI_ON_Q4}$ | High side driver (HSD) turn on resistance | $V_{BTST2}$ - $V_{SW2}$ = 4.5 V | | 1.50 | | Ω |
| $R_{DS_HI_OFF_Q4}$ | High side driver turn off resistance | $V_{BTST2}$ - $V_{SW2}$ = 4.5 V | | 0.50 | 0.80 | Ω |
| $V_{BTST2_REFRESH}$ | Bootstrap refresh comparator falling threshold voltage | $V_{BTST2}$ - $V_{SW2}$ when low side refresh pulse is requested | 3.0 | 3.3 | 3.6 | V |
| **PWM LOW SIDE DRIVER (LODRV2 for Q3)** | | | | | | |
| $R_{DS_LO_ON_Q3}$ | Low side driver (LSD) turn on resistance | $V_{BTST2}$ - $V_{SW2}$ = 4.5 V | | 1.10 | | Ω |
| $R_{DS_LO_OFF_Q3}$ | Low side driver turn off resistance | $V_{BTST2}$ - $V_{SW2}$ = 4.5 V | | 0.40 | 0.70 | Ω |
| **INTERNAL SOFT START During Charge Enable** | | | | | | |
| $SS_{STEP_DAC}$ | Soft Start Step Size | | | 8 | | mA |
| **INTEGRATED BTST DIODE (D1_X)** | | | | | | |
| $V_{F_D1}$ | Forward bias voltage | IF = 20 mA at 25°C | | 0.8 | | V |
| **INTEGRATED BTST DIODE (D2)** | | | | | | |
| $V_{F_D2}$ | Forward bias voltage | IF = 20 mA at 25°C | | 0.8 | | V |
| **INTERFACE** | | | | | | |
| **LOGIC INPUT (SDA, SCL, EN_OTG)** | | | | | | |
| $V_{IN_LO_EN_OTG}$ | Input low level for EN_OTG pin | | | | 0.8 | V |
| $V_{IN_HI_EN_OTG}$ | Input high level for EN_OTG pin | | 1.35 | | | V |
| **LOGIC OUTPUT OPEN DRAIN SDA** | | | | | | |
| $V_{OUT_LO_SDA}$ | Output Saturation Voltage | 5 mA drain current | | | 0.3 | V |
| $V_{OUT_LEAK_SDA}$ | Leakage Current | V = 5.5V | –1 | | 1 | µA |
| **LOGIC OUTPUT OPEN DRAIN CHRG_OK** | | | | | | |
| $V_{OUT_LO_CHRG_OK}$ | Output Saturation Voltage | 5 mA drain current | | | 0.4 | V |
| $V_{OUT_LEAK_CHRG_OK}$ | Leakage Current | V = 5.5V | –1 | | 1 | µA |
| **LOGIC OUTPUT OPEN DRAIN CMPOUT** | | | | | | |
| $V_{OUT_LO_CMPOUT}$ | Output Saturation Voltage | 5 mA drain current | | | 0.4 | V |
| $V_{OUT_LEAK_CMPOUT}$ | Leakage Current | V = 5.5V | –1 | | 1 | µA |
| **LOGIC OUTPUT OPEN DRAIN (PROCHOT)** | | | | | | |
| $V_{OUT_LO_PROCHOT}$ | Output saturation voltage | 50 Ω pullup to 1.05 V / 5-mA | | | 0.4 | V |
| $V_{OUT_LEAK_PROCHOT}$ | Leakage current | V = 5.5 V | –1 | | 1 | µA |
| **ANALOG INPUT (ILIM_HIZ)** | | | | | | |
| $V_{HIZ_LOW}$ | Voltage to get out of HIZ mode | ILIM_HIZ pin rising | | 0.7 | 0.8 | V |
| $V_{HIZ_HIGH}$ | Voltage to enable HIZ mode | ILIM_HIZ pin falling | 0.4 | 0.5 | | V |
| $V_{ILIM_ENZ}$ | Voltage to disable external current limit function on ILIM_HIZ pin (EN_EXTLIM=1b) | ILIM_HIZ pin rising | | 4.1 | 4.2 | V |
| $V_{ILIM_EN}$ | Voltage to enable external current limit function on ILIM_HIZ pin (EN_EXTLIM=1b) | ILIM_HIZ pin falling | 3.9 | 4.0 | | V |

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## 6.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ}$ < $V_{VBUS}$ < $V_{ACOV_FALL}$ , $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT (CELL_BATPRES)** | | | | | | |
| $V_{CELL_5S}$ | 5S | CELL_BATPRES pin voltage as percentage of REGN = 5 V | 90.0% | 100.0% | | |
| $V_{CELL_4S}$ | 4S | CELL_BATPRES pin voltage as percentage of REGN = 5 V | 68.4% | 75.0% | 81.5% | |
| $V_{CELL_3S}$ | 3S | CELL_BATPRES pin voltage as percentage of REGN = 5 V | 51.7% | 55.0% | 65.0% | |
| $V_{CELL_2S}$ | 2S | CELL_BATPRES pin voltage as percentage of REGN = 5 V | 18.4% | 40.0% | 48.5% | |
| $V_{CELL_BATPRES_RISE}$ | Battery is present | CELL_BATPRES rising | 18.0% | | | |
| $V_{CELL_BATPRES_FALL}$ | Battery is removed | CELL_BATPRES falling | | | 14.7% | |

## 6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Comparator and Battery Charger Timing** | | | | | |
| $t_{TRANS_CHG}$ | Charge current transit from pre-charge level to fast-charge level time duration | | 5 | | ms |
| **HOST COMMUNICATION FAILURE** | | | | | |
| $t_{BOOT}$ | Deglitch for watchdog reset signal | 10 | | | ms |
| $t_{WDI}$ | Watchdog timeout period, REG0x12[14:13]=01 | 4 | 5.5 | 7 | s |
| | Watchdog timeout period, REG0x12[14:13]=10 | 70 | 88 | 105 | s |
| | Watchdog timeout period, REG0x12[14:13]=11 | 140 | 175 | 210 | s |


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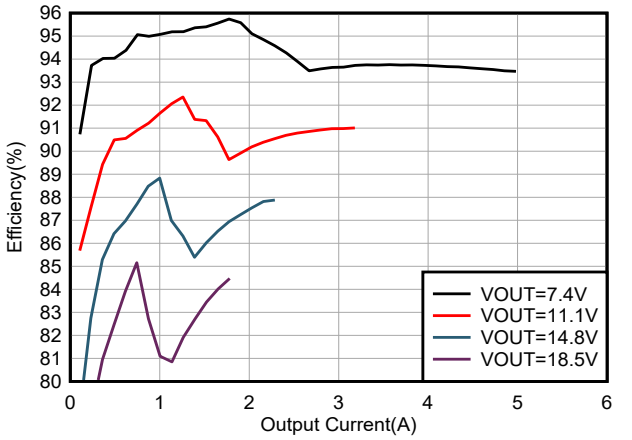
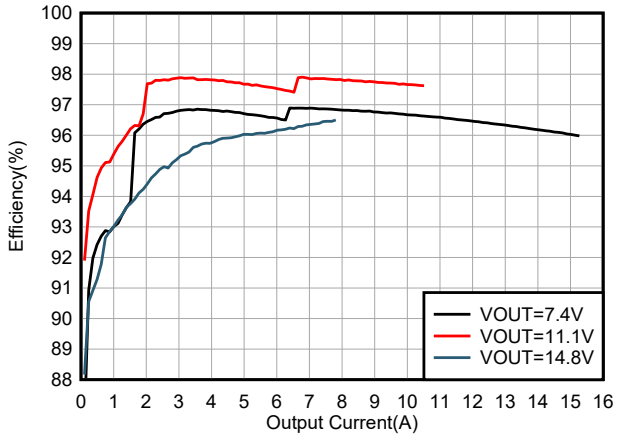
## 6.7 Typical Characteristics BQ25770G

$R_{AC}$ = 10 mΩ, $R_{SR}$ = 5 mΩ, Inductance = 3.3 µH, CCM Frequency = 600 kHz



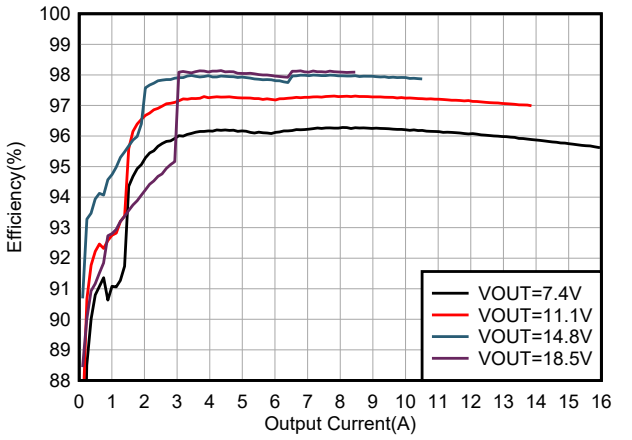

VIN = 5 V CCM 600 kHz VOUT = System voltage

**Figure 6-1. System Efficiency**



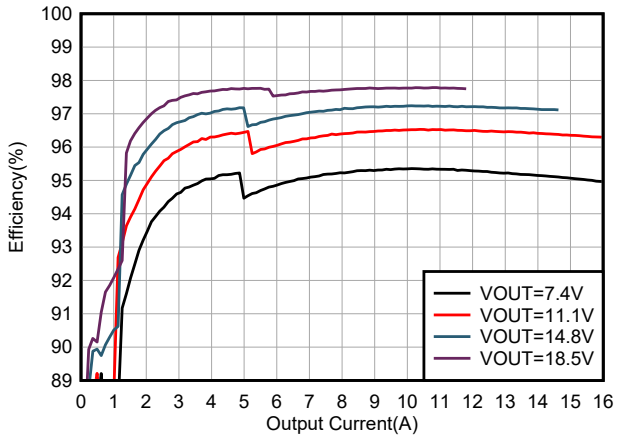

VIN = 15V CCM 600 kHz VOUT = System voltage

**Figure 6-2. System Efficiency**



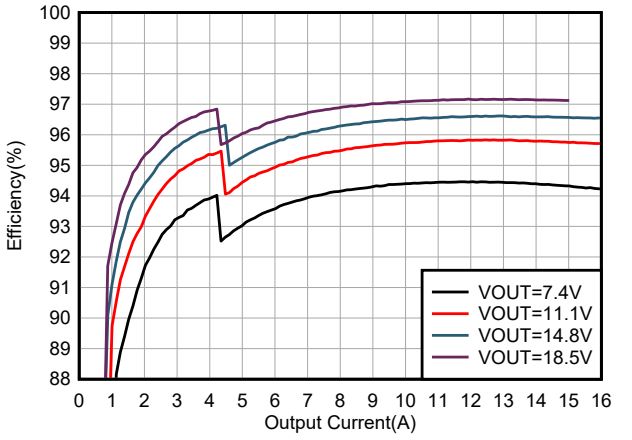

VIN = 20 V CCM 600 kHz VOUT = System voltage

**Figure 6-3. System Efficiency**



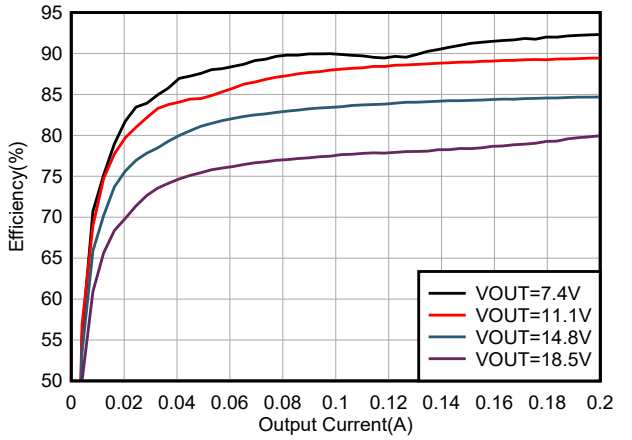

VIN = 28 V CCM 600 kHz VOUT = System voltage

**Figure 6-4. System Efficiency**




VIN = 36 V CCM 600 kHz VOUT = System voltage

**Figure 6-5. System Efficiency**




VIN = 5 V EN_OOA = 0b VOUT = System voltage

**Figure 6-6. Light Load System Efficiency**

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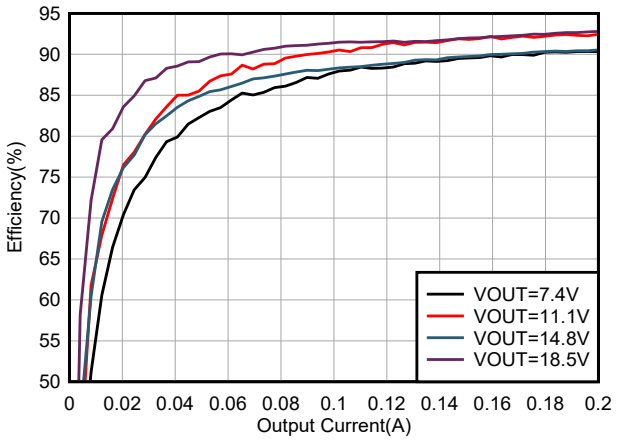
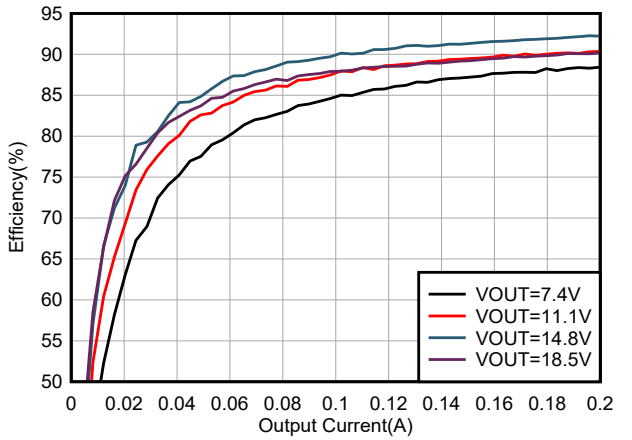
## 6.7 Typical Characteristics BQ25770G (continued)



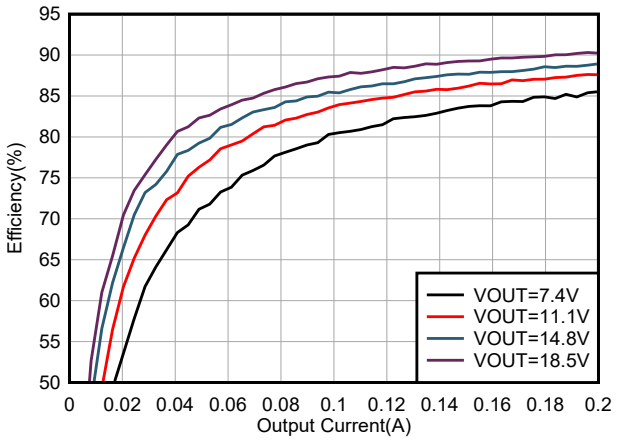

VIN = 15 V EN_OOA = 0b VOUT = System voltage

**Figure 6-7. Light Load System Efficiency**



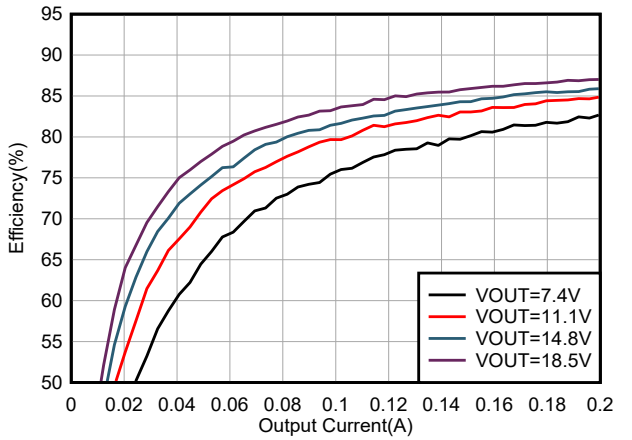

VIN = 20 V EN_OOA = 0b VOUT = System voltage

**Figure 6-8. Light Load System Efficiency**



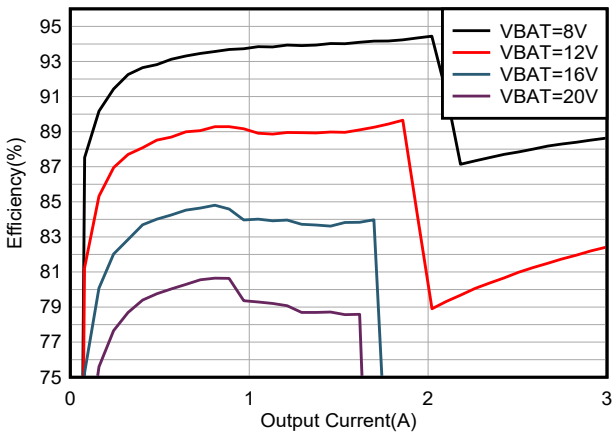

VIN = 28 V EN_OOA = 0b VOUT = System voltage

**Figure 6-9. Light Load System Efficiency**



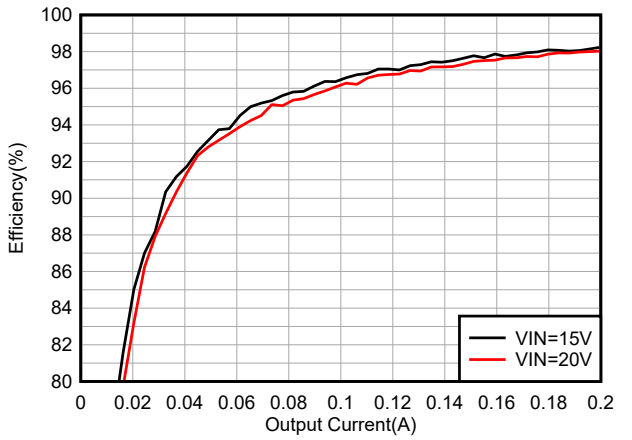

VIN = 36 V EN_OOA = 0b VOUT = System voltage

**Figure 6-10. Light Load System Efficiency**




VOTG= 5 V CCM 600 kHz

**Figure 6-11. OTG Efficiency**




VOUT = VIN EN_PTM=1b

**Figure 6-12. PTM Mode Ligh Load System Efficiency**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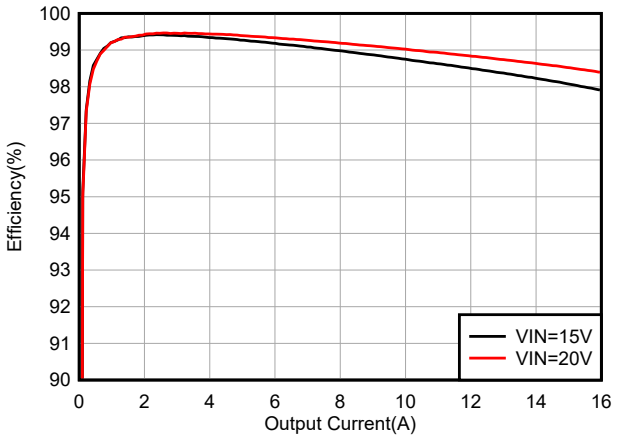
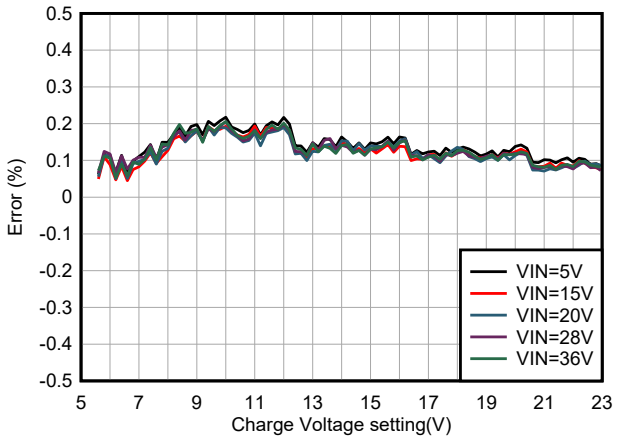
## 6.7 Typical Characteristics BQ25770G (continued)



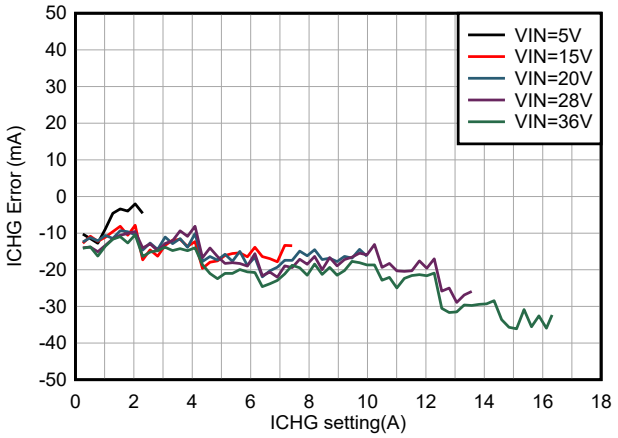

VOUT = VIN EN_PTM=1b

**Figure 6-13. PTM Mode Heavy Load System Efficiency**



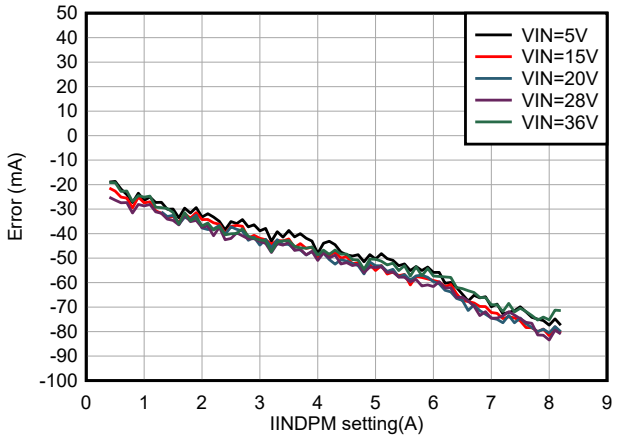

ICHG = 1024 mA CCM 600 kHz

**Figure 6-14. Battery Voltage Regulation Accuracy**



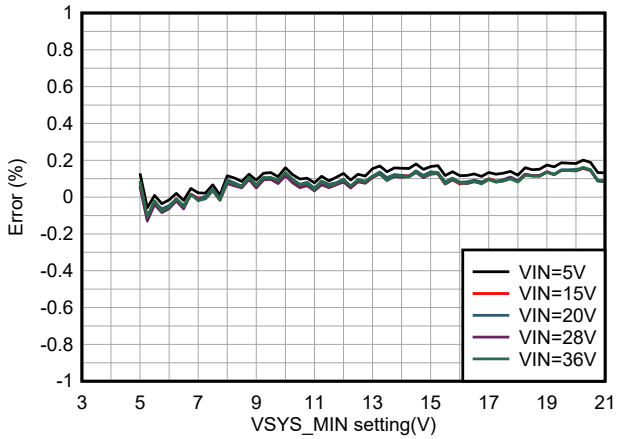

VBAT = 14.8 V CCM 600 kHz

**Figure 6-15. Battery Charge Current Regulation Accuracy**




VBAT = 14.8 V CCM 600 kHz IINDPM set =0.4~8.2 A

**Figure 6-16. Input Current Regulation Accuracy (IIN_DPM)**




VBAT = 0.5 V CCM 600 kHz EN_OOA = 0b

**Figure 6-17. Minimum System Voltage Regulation Accuracy**

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# 7 Detailed Description

## 7.1 Overview

The BQ25770G is a Narrow VDC buck-boost charger controller for portable electronics such as notebook, detachable, ultrabook, tablet, and other mobile devices with rechargeable batteries. It provides seamless transition between different converter operation modes (buck, boost, or buck-boost), fast transient response, and high light load efficiency.

The BQ25570G supports a wide range of power sources, including USB-C PD EPR ports, legacy USB ports, traditional AC-DC adapters, and so forth. It takes input voltage from 3.5 V to 40 V and charges a battery of 2 to 5-cell in series. In the absence of an input source, the BQ25770G supports the USB On-the-Go (OTG) function from a cell battery to generate an adjustable 3 V to 5 V at the USB port with 20-mV resolution.

The BQ25770G features Dynamic Power Management (DPM) to limit input power and avoid AC adapter overloading. During battery charging, as system power increases, charging current is reduced to maintain total input current below adapter rating. If system power demand temporarily exceeds adapter rating, the BQ25770G supports the NVDC architecture to allow battery discharge energy to supplement system power.

The BQ25770G monitors adapter current, battery current, and system power. The flexibility of the programmable $\overline{\text{PROCHOT}}$ output goes directly to the CPU for throttling back when needed.

The latest version of the USB-C PD specification includes Fast Role Swap (FRS) to ensure power role swapping occurs in a timely fashion so that the device(s) connected to the dock never experience momentary power loss or glitching. The device integrates FRS with compliance to the USB-C PD specification.

The TI patented switching frequency dithering pattern can significantly reduce EMI noise over the entire conductive EMI frequency range (150 kHz to 30 Mhz). Multiple dithering scale options are available to provide flexibility for different applications to simplify EMI noise filter design.

In order to be compliant with Intel IMVP8 / IMVP9, the BQ25770G includes a PSYS function to monitor the total platform power from the adapter and battery. Besides PSYS, it provides both an independent input current buffer (IADPT) and a battery current buffer (IBAT) with highly accurate current sense amplifiers. If the platform power exceeds the available power from the adapter and battery, a $\overline{\text{PROCHOT}}$ signal is asserted to the CPU so that the CPU optimizes its performance to the power available to the system.

The host controls input current, charge current, and charge voltage registers with high resolution, high accuracy regulation limits. It also sets the $\overline{\text{PROCHOT}}$ timing and threshold profile to meet system requirements.


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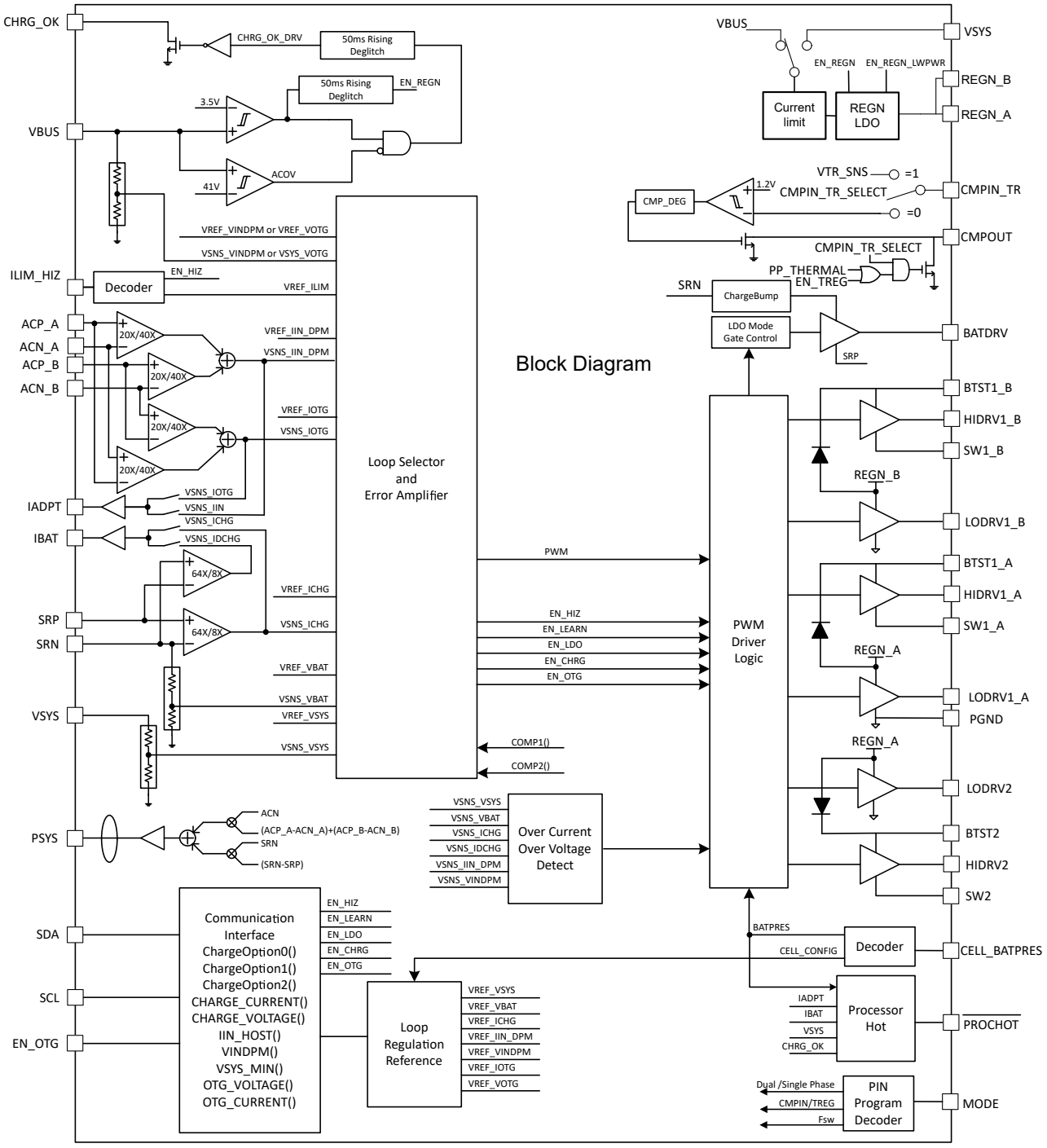
## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Power-Up Sequence

The device powers up from the higher voltage of VBUS or VBAT through internal power selector. The charger starts up when VBUS exceeds $V_{VBUS_UVLOZ}$ or VBAT exceeds $V_{VBAT_UVLOZ}$ for 5ms. Upon POR(power on reset) the charger resets all the registers to the default state. Another 5 ms later, the user registers become accessible to the host. When VBAT> VBAT_UVLO: if VBUS falls below VBUS_UVLO then adapter removal is detected to enter battery only low power mode. When VBAT< VBAT_UVLO: if VBUS falls below VBUS_UVLO then device is off without I2C communication and device will POR when VBUS rise above VBUS_UVLOZ.

Power up sequence when the charger is powered up from VBUS:

- After VBUS rises above $V_{VBUS_UVLOZ}$, there is 50ms deglitch time. After this 50ms deglitch time, charger enables REGN_A/B LDOs. CHRG_OK pin goes high and STAT_AC is set to 1b once REGN_A/B voltages ramp up. (If EN_LWPWR set to 0b then device will be in performance mode, REGN_A/B will be kept on there is a battery present before VBUS is plugged in)
- MODE pin detection is executed after device POR to determine converter topology, converter compensation option and converter switching frequency.
- VBUS qualification is then executed. During VBUS qualification process, there is a internal 20mA current sink 100ms pulse adding on VBUS pin to make sure the input source is strong enough to pass qualification. During this 100ms if $V_{VBUS_CONVEN}$<VBUS <$V_{ACOV_RISE}$, then charger passes VBUS qualification and proceeds to the next step. However, if $V_{VBUS_UVLOZ}$ < VBUS < $V_{VBUS_CONVEN}$ or VBUS> $V_{ACOV_RISE}$ then charger fails VBUS qualification, the charger will re-qualify VBUS every 2 s. During this 2 s, even if VBUS rise up higher than $V_{VBUS_CONVEN,}$ the converter is still shutting down due to failing VBUS qualification at the beginning.
- During VBUS qualification, Battery cell configuration is read at CELL_BATPRES pin voltage and compared to REGN_A/B to determine cell configuration. The default value of CHARGE_VOLTAGE(), CHARGE_CURRENT(),VRECHG(), VSYS_MIN() and SYSOVP thresholds are loaded respectively. Also IINDPM is detected at ILIM_HIZ pin steady state voltage.
- After passing the qualification, VBUS ADC is executed one time to read the no-load VBUS voltage and save the value into ADC_VBUS() register.
- Check voltage between VBUS and ACP_A (VBUS-ACP_A) is below $V_{SC_VBUSACP_FALLING}$ to make sure eFuse or PFETs are fully turned on. If not, hold on converter power up until SC_VBUSACP is not triggered.
- Normally 226 ms after VBUS above $V_{VBUS_CONVEN}$, converter powers up. If SC_VBUSACP keeps triggered then converter power up could wait until it is cleared.

Power up sequence when the charger is powered up from VBAT:

- If only battery is present and the voltage is above $V_{VBAT_UVLOZ}$ , charger wakes up and the BATFET is turned on and connecting the battery to system.
- MODE pin detection is executed right after device POR to determine converter topology, converter compensation option and converter switching frequency.
- By default, the charger is in low power mode (EN_LWPWR = 1b) with lowest quiescent current. The REGN_A/B LDO is turned off by default but when EN_LWPWR=1, the LDO is turned on, the LDO current limit is reduced to 5mA in order to minimize the quiescent current.
- The adapter present comparator is activated, to monitor the VBUS voltage.
- SDA and SDL lines stand by waiting for host commands.
- Device can move to performance mode by configuring EN_LWPWR = 0b. The host can enable IBAT buffer through setting EN_IBAT=1b to monitor discharge current. The PSYS also can be enabled by the host. CELL_BATPRES pin detection is executed one time when CELL_BATPRES pin is pulled up or REGN_A/B rise up from GND to steady state value. Note under battery only low power mode, CELL_BATPRES detection is not executed.
- In performance mode, the REGN_A/B LDO is always available to provide an accurate reference and gate drive voltage for the converter.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### 7.3.2 MODE Pin Detection

Fixed pull down resistor is needed on MODE pin for charger multi-function programming. Refer to Table 7-1for typical resistance corresponding to each programming code. Both E96(±1%) and E48 (±2%) tolerance resistors can be used here. The two programming items are:

- Compensation Adjustment : The device can support both normal compensation and slower bandwidth compensation under extreme application scenario. When input VBUS effective capacitance is higher than 10uF, recommend to adopt "normal" option to get best transient performance; when input VBUS capacitance is lower than 10uF, recommend to adopt "slow" option to ensure converter operation stability.
- Switching frequency: The device supports both 600kHz and 800kHz switching frequency. Based on MODE pin detection, PWM_FREQ bit will be programmed accordingly.

**Table 7-1. MODE Pin Programming Table**

| MODE_STAT BIT | MINIMUM RESISTANCE | TYPICAL RESISTANCE | MAXIMUM RESISTANCE | TOPOLOGY | COMPENSATION ADJUSTMENT | PWM_FREQ BIT |
|---|---|---|---|---|---|---|
| 000b | 0 kΩ | 3.57 | 3.79 kΩ | Quasi dual phase buck-boost | Normal | 1b (600 kHz) |
| 001b | 4.42 kΩ | 4.64 kΩ | 4.87 kΩ | Quasi dual phase buck-boost | Normal | 0b (800 kHz) |
| 010b | 5.76 kΩ | 6.04 kΩ | 6.34 kΩ | Quasi dual phase buck-boost | Slow | 1b (600 kHz) |
| 011b | 7.87 kΩ | 8.25 kΩ | 8.66 kΩ | Quasi dual phase buck-boost | Slow | 0b (800 kHz) |
| High Fault (000b) | 47.5 kΩ | -- | Open circuit | Quasi dual phase buck-boost | Normal | 1b (600 kHz) |

### 7.3.3 REGN Regulator (REGN LDO)

The REGN LDO regulator provides a regulated bias supply for the IC and external pull up. Additionally, REGN voltage is also used to drive the buck-boost switching FETs. The pull-up rail of CELL_BATPRES pin and ILIM_HIZ pin can be connected to REGN as well. When there is no valid external 5V voltage source available on the system then REGN LDO will be powered from either the VBUS pin or VSYS pin. REGN power selector selects the lower of VBUS and VSYS if both greater than 6V; should select the higher of VBUS and VSYS is they're both lower than 6V; and should select the one higher than 6V if there is only one higher than 6V. Both REGN_A and REGN_B pins are connected to REGN LDO internally, no external connections between REGN_A and REGN_B are needed, however 2.2uF local decoupling capacitance are needed for both REGN_A and REGN_B pins.

When there is a qualified 5V supply in the system, it can be leveraged as a REGN source. This can reduce power loss from the internal LDO, especially when both VBUS and VSYS are much higher than 5V. The LDO can be configured to be over-driven by external 5V source. Then REGN pin will change from an analog output pin to an analog input pin. REGN_EXT bit is employed to configure in the following method.

- When there is no qualified external 5V source, host should configure REGN_EXT=0b(default status), then the internal REGN LDO regulation output voltage is 5V to normally support internal bias and switching MOSFET gate drive. There is an internal current limit to prevent LDO from over load. The current limit level is $I_{REGN_LIM_CHARGING}$ and it is marked as current limit 1.
- When there is dedicated qualified external 5V source(above 4.8V and below $V_{REGN_OV_RISE}$) and REGN is the only load on external source, host should configure REGN_EXT=1b to reduce internal REGN LDO regulation output voltage to be $V_{REGN_REG_EXT}$(4.5V), then external 5V regulator can over drive internal LDO. Maximum500mA current limit is needed for external power supply to prevent over current damaging on internal bootstrap diode. Application diagram is referring to Figure 7-1.
- When the external 5V source (above 4.8V and below $V_{REGN_OV_RISE}$) is also supporting other loads besides REGN, a dedicated blocking circuit is needed to prevent REGN current from sourcing into external loads before external 5V buck converter ramp up shown in Figure 7-2. Before external 5V regulator power good(PG) is active, the $Q_{BLK}$ serves to block external loading impact on REGN_A pin. After external 5V ramps up, external 5V regulation PG is active and $Q_{BLK}$ is turned on to distribute 5V to REGN_A

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pin. Host should configure REGN_EXT=1b to reduce internal REGN LDO regulation output voltage to be $V_{REGN_REG_EXT}$(4.5V), then external 5V regulator can over drive to internal LDO automatically.

- When external 5V source is above $V_{REGN_OV_RISE}$, the charger should stop switching, pull down CHRG_OK pin and trigger FAULT_REGN status bit referring to Section 7.3.26.11.

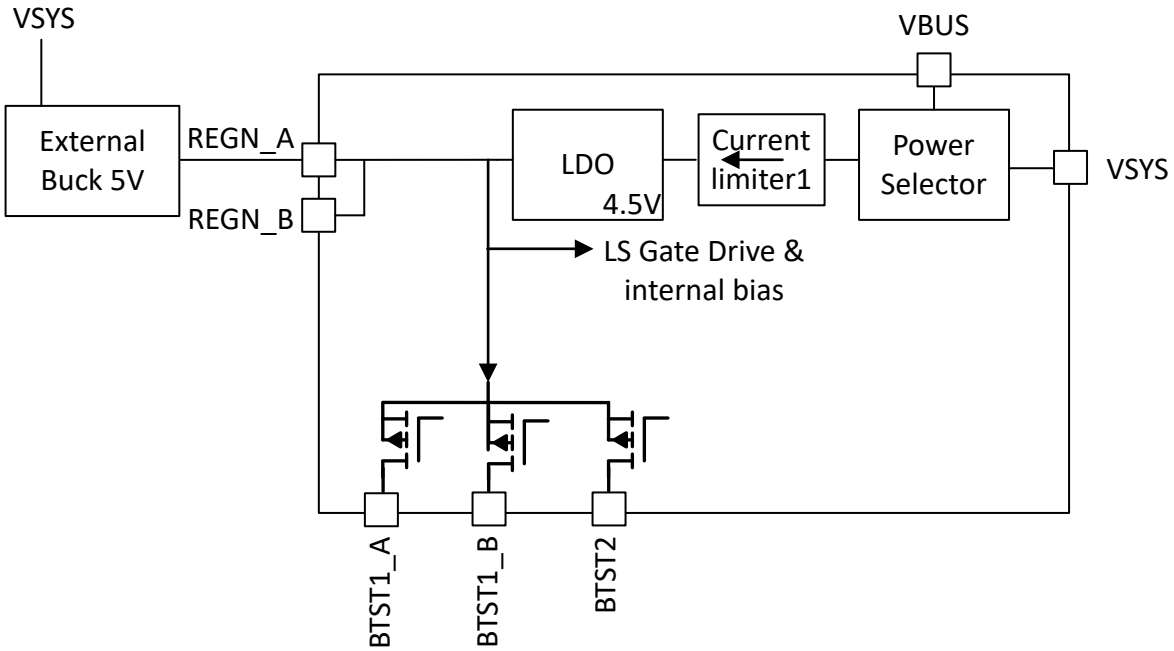


**Figure 7-1. External Dedicated 5-V Source Over Drive REGN**

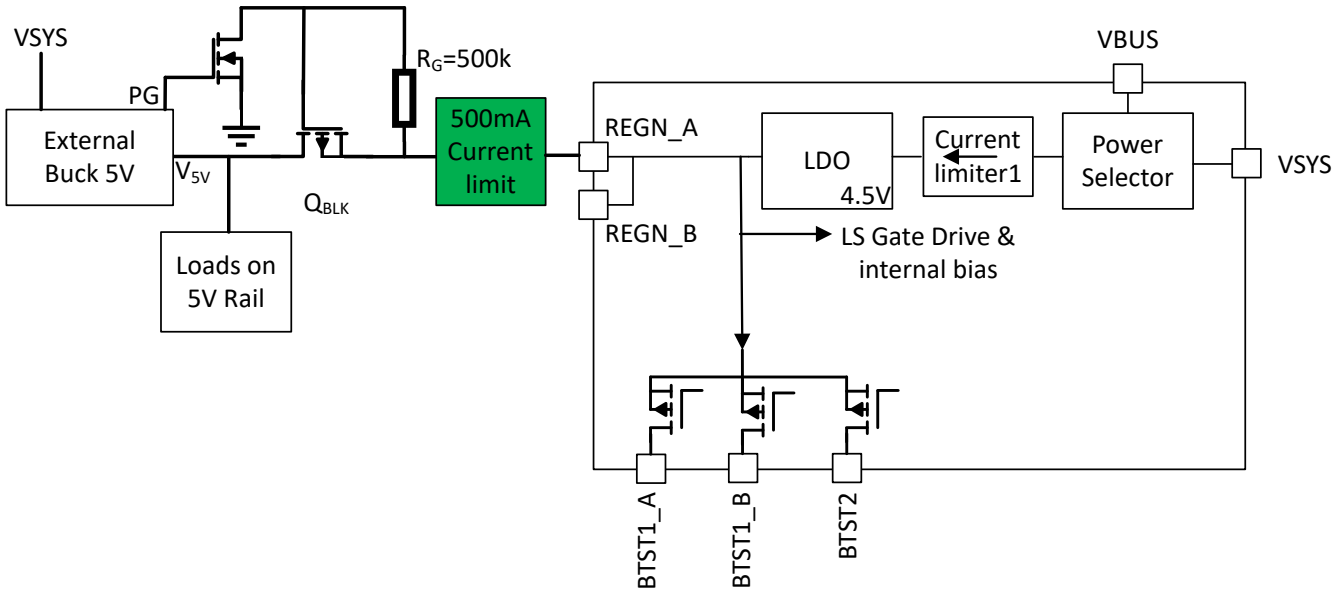


**Figure 7-2. External 5-V Source with Load Over Drive REGN**

The power dissipation for driving the gates via the REGN LDO is: $P_{REGN}$ = *(VAC -* $V_{REGN}$*)* $Q_{G(TOT)}$***$f_{SW}$ , where $Q_{G(TOT)}$ is the sum of the total gate charge for all practical switching FETs (1A,1B,2A,2B,3 and 4) and $f_{SW}$ is the programmed switching frequency.

Under battery only condition, it is flexible to configure REGN on and off through below method:


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- When charger is configured in low power mode(EN_LWPWR=1b), REGN by default is turned off(EN_REGN_LWPWR=0b). If customer needs REGN voltage to supply circuit, the charger enables REGN by setting EN_REGN_LWPWR=1b. In order to save quiescent current under low power mode, REGN current capability is scaled down to 5 mA typical and 3 mA minimum. When it receives host command to start up converter, like OTG or VAP mode is enabled, then REGN should automatically recover to full scale to support large gate drive current demand even with EN_LWPWR=1b.
- When charger is configured in performance mode(EN_LWPWR=0b), REGN should be turned on with full scale capability neglecting EN_REGN_LWPWR configuration. This is needed to support OTG, VAP, PSYS, IBAT, PROCHOT, and ADC features.

### 7.3.4 Independent Comparator Function

When CMPIN_TR pin is muxed for independent comparator input by configuring CMPIN_TR_SELECT=0b, the comparator output is low effective and the output can be latched through setting EN_CMP_LATCH =1b. Host can clear comparator output by toggling EN_CMP_LATCH bit. Comparator polarity is determined through CMP_POL bit; comparator output deglitch time is adjustable through CMP_DEG bits. With polarity HIGH (CMP_POL = 1b), there is no internal hysteresis, user can place two resistors ($R_{CMP1}$ and $R_{CMP2}$) to program hysteresis externally referring to Figure 7-3. With polarity LOW (CMP_POL = 0b), the internal hysteresis is fixed at 100 mV.

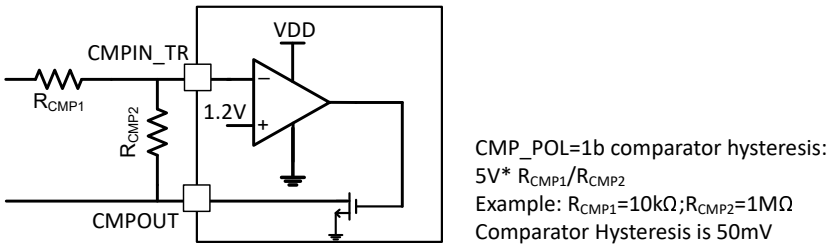


**Figure 7-3. Comparator Hysteresis External Adjustment Under CMP_POL=1b**

The comparator has a dedicated force converter off protection feature which can be triggered through external system circuit. To enable this feature, set FRC_CONV_OFF=1b. Then, when the comparator output is low, the converter will be turned off, FAULT_FRC_CONV_OFF will be set to 1b, and the CHRG_OK pin will be pulled low to inform the host EC. When the comparator output returns to high, the FAULT_FRC_OFF bit is cleared and the converter resumes switching automatically. Upon adapter removal, force converter off fault should be cleared one time, if the comparator is still triggered low then the fault should be re-triggered again to keep converter disabled.

No matter CMPIN_TR pin function selection, it always has dedicated ADC channel which can be enabled though setting EN_ADC_CMPIN=1b.

Under battery only low power mode (EN_LWPWR=1b), there is a dedicated user register bit EN_LWPWR_CMP to enable independent comparator with minimum quiescent current consumption. When EN_LWPWR_CMP=1b the independent comparator is enabled.

### 7.3.5 Battery Charging Management

The device charges 2-cell up-to 5-cell Li-Ion batteries. The charge cycle can be fully controlled by host, or it can be autonomous (requiring no host interaction).

#### *7.3.5.1 Autonomous Charging Cycle*

When autonomous battery charging is enabled (EN_AUTO_CHG=1b, CHRG_INHIBIT=0b and CHARGE_CURRENT() register is not 0 mA), the device autonomously completes a charging cycle without host involvement. The battery charging parameters can be programmed by CHARGE_VOLTAGE() and CHARGE_CURRENT(). The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers.

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**Table 7-2. Li-Ion Charging Parameter Default Settings**

| DEFAULT MODE | BQ2577x |
|---|---|
| Charge Stages | Precharge → Fast Charge (CC) → Taper Charge (CV) → Termination → Recharge |
| Cell count (n_cell) | Set by CELL_BATPRES pin |
| Charge Voltage (CHARGE_VOLTAGE()) | 4.2V / Cell |
| Charge Current(CHARGE_CURRENT()) | 0A(Need host configuration) |
| Termination Current (ITERM) | 256mA |
| Recharge Voltage (VRECHG) | CHARGE_VOLTAGE()-200mV |
| Pre-Charge Current(IPRECHG) | 384mA |
| Safety Timer | 12 hours |

An autonomous charge cycle starts when the following conditions are valid:

- Converter starts up
- Battery autonomous charge is enabled (EN_AUTO_CHG = 1b)
- CHARGE_CURRENT() register is not 0 mA
- CHRG_INHIBIT bit is not 1b
- No SYSOVP/VSYS_UVP/ACOC/TSHUT/BATOVP/BATDOC/SC_VBUSACP/Force converter off faults
- No safety timer fault

The device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device is not in DPM mode. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG[3:0] bits), the device automatically starts a new charging cycle. After the charge is terminated automatically, changing CHRG_INHIBIT bit from 1b to 0b or CHARGE_CURRENT() from 0A to non zero value can initiate a new charging cycle.

The status register (CHRG_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge (VBAT < $V_{BAT_SHORT}$)
- 010 – Pre-charge ($V_{BAT_SHORT}$ < VBAT < VSYS_MIN() setting)
- 011 – Fast-charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Reserved
- 111 – Charge Termination Done

#### *7.3.5.2 Battery Charging Profile*

The device charges the battery in four phases: trickle charge, pre-charge, constant current, constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly. If autonomous charging is enabled, automatic termination can be achieved and automatic recharge will begin when VBAT drops below certain value of CHARGE_VOLTAGE(), user registers VRECHG bits are used to configure battery re-charge threshold.

When charger is in trickle charge status (VBAT<$V_{BAT_SHORT}$) and EN_LDO=1b, charge current is upper limited by $I_{BAT_SHORT}$ to prevent battery from overcurrent charge and wake up battery pack. The practical charge current should be the lower value of CHARGE_CURRENT() and $I_{BAT_SHORT}$ to provide EC flexibility to program trickle charge current following battery package request. Note when EN_LDO=0b, $I_{BAT_SHORT}$ current clamp is not effective and provide EC flexibility to program charge current through CHARGE_CURRENT() register.

When charger is in pre-charge status ($V_{BAT_SHORT}$<VBAT<VSYS_MIN()) and EN_LDO=1b, charge current is the lower value of IPRECHG() and CHARGE_CURRENT() setting; and the maximum charge current is limited by maximum setting of IPRECHG() which is 2048mA to prevent overheat generated on BATFET. Under this condition larger VSYS_MIN() minus VBAT delta and larger charge current should generate more thermal dissipation at BATFET which should be properly limited to ensure safe operation. Therefore the device has


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additional two levels current clamp to ensure the maximum BATFET dissipation loss below 2W based on the relationship between VBAT and VSYS_MIN() setting referring to Table 7-9. Note when EN_LDO=0b, pre-charge current limit (IPRECHG()) is not effective and provide EC flexibility to program charge current through CHARGE_CURRENT() register.

**Table 7-3. Default Charging Current Setting**

| VBAT CONDITION | CHARGING CURRENT | DEFAULT SETTING | CHRG_STAT |
|---|---|---|---|
| VBAT< $V_{BAT_SHORT}$ | $I_{BAT_SHORT}$ | 128mA | 001 |
| $V_{BAT_SHORT}$<VBAT< VSYS_MIN() | $I_{PRECHG}$ | 384mA | 010 |
| VSYS_MIN()<VBAT<CHARGE_VOLTAGE() | CHARGE_CURRENT() | 0A (need host to configure based on battery request) | 011 |

If the charger device is in DPM regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as detailed in Charging Safety Timer section.

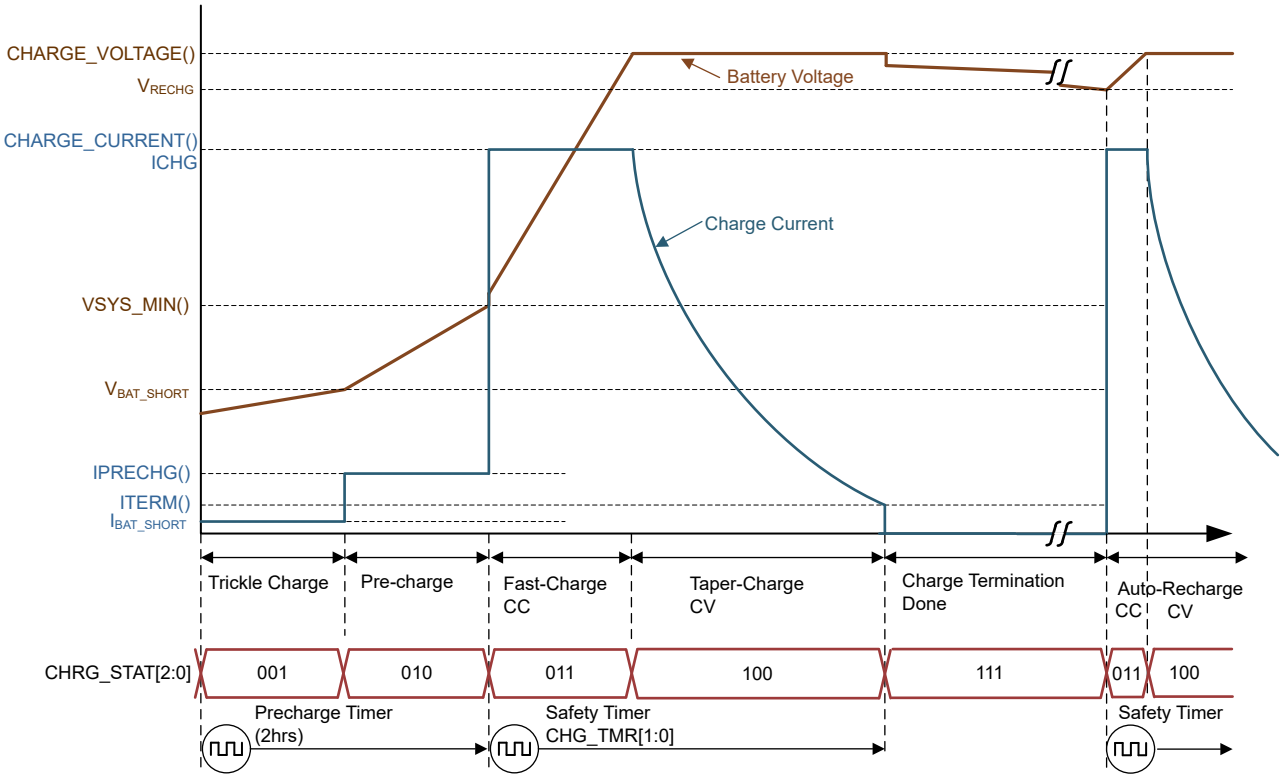


**Figure 7-4. Typical Li-Ion Battery Charging Profile**

### *7.3.5.3 Charging Termination*

When autonomous charging is not enabled (EN_AUTO_CHG=0b), the battery charging termination be can be executed when host write CHARGE_CURRENT() register to 0A or set CHRG_INHIBIT=1b based on battery gauge device request.

When autonomous charging is enabled (EN_AUTO_CHG=1b), the device terminates a charge cycle when the battery voltage is above the recharge threshold, the converter is operated in the battery constant voltage regulation loop and the current is below the termination current threshold (ITERM() register setting). After the charging cycle is completed, the CHARGE_CURRENT() register is set to 0A to terminate charge and BATFET turns off. The original CHARGE_CURRENT() register setting is logged internally and resumes it to

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CHARGE_CURRENT() when re-charge condition is detected to restart charging. The converter keeps running to power the system and the BATFET can turn on again if the supplement mode is triggered.

When termination is done, the status register CHRG_STAT is set to 111b. The charger can be configured to pull down CHRG_OK pin for minimum 256 µs to inform host that charging is terminated when CHRG_OK_INT bit is set to 1b. Termination is temporarily disabled when the charger device is in input current (IINDPM), input voltage (VINDPM) or TREG thermal regulation. The deglitch times for determining IINDPM active and VINDPM active is 1 ms, and deglitch times for determining TREG active is 10 ms.

#### *7.3.5.4 Charging Safety Timer*

The device has a built-in fast charge safety timer to prevent extended charging cycle due to abnormal battery conditions. The user can program fast charge safety timer through CHG_TMR register bits. When safety timer expires, charging should stop through setting CHARGE_CURRENT() to 0A. The status register CHG_TMR_STAT bit is set to 1 and CHRG_STAT bits will be set to 000b(not charging), and CHRG_OK pin can be configured to be pulled low for minimum 256us to inform host if CHRG_OK_INT=1b. CHG_TMR_STAT bit will keep its 1b status until safety timer gets reset. The safety timer feature can be disabled by clearing EN_CHG_TMR bit.

During IINDPM and VINDPM regulation, or TREG thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the programmed setting. For example, if the charger is in input current regulation throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer will expire in 10 hours. This half clock rate feature can be disabled by setting EN_TMR2X = 0. Changing the EN_TMR2X bit while the device is running has no effect on the safety timer count, other than forcing the timer to count at half the rate under the conditions dictated above. The deglitch times for determining IINDPM active and VINDPM active is 1ms, and deglitch times for determining TREG active is 10ms.

During faults which disable charging, timer is suspended. Since the timer is not counting in this state, the EN_TMR2X bit has no effect. Once the fault goes away, safety timer resumes. If the charging cycle is stopped and started again, the timer gets reset (toggle CHRG_INHIBIT bit restarts the timer, change CHARGE_CURRENT() register from non zero to zero and then non zero, charged battery falls below recharge threshold after termination).

The safety timer is reset for the following events:

1. Charging cycle stop and restart (toggle CHRG_INHIBIT bit, or charge-terminated battery falls below recharge threshold after termination, or change CHARGE_CURRENT() register from zero and then non zero)
2. BAT voltage changes from pre-charge to fast-charge or vice versa
3. Safety Timer (CHG_TMR[1:0]) register bits are changed
4. Toggle EN_CHG_TMR bit, when EN_CHG_TMR becomes 0b, the safety timer should be reset and count from beginning when re-enable again(EN_CHG_TMR=1b)

The pre-charge safety timer (fixed 2hr counter that runs when VBAT < VSYS_MIN()), follows the same rules as the fast-charge safety timer in terms of getting suspended, reset, and counting at half-rate when EN_TMR2X is set. Note pre-charge safety timer applies to both pre-charge and trickle charge phase.

### 7.3.6 Temperature Regulation (TREG)

In high power application, monitoring and controlling external component temperature can enhance reliability by limiting the total converter power under certain scenarios. The CMPIN_TR pin can be configured as temperature regulation feedback sensing pin when CMPIN_TR_SELECT=1b. It is the temperature feedback pin temperature regulation loop. The external voltage divider circuit is shown in Figure 7-5 consisting of $R_S$ and NTC resistor $R_{TH}$. External NTC is placed where temperature is regulated (for example charger power stage) and generates feedback voltage on CMPIN_TR pin based on temperature variation. When temperature is lower than target, the voltage should be above 1.2 V, temperature regulation is not effective and TREG_STAT=0b ; As temperature increases, CMPIN_TR pin voltage drops to $V_{TREG}$=1.2 V or lower , converter begin to reduce converter current and regulate CMPIN_TR voltage to stay at 1.2 V and set TREG_STAT=1b which is locked until host read or REG_RESET bit action.


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To enable temperature regulation feature:

- Set CMPIN_TR_SELECT=1b to configure CMPIN_TR_SELECT pin as temperature regulation feedback pin.
- Make sure AC is plugged in and charge is enabled CHARGE_CURRENT() is non-zero and CHRG_INHIBIT=0b).
- Set EN_TREG=1b to enable temperature regulation and pull CMPOUT pin to GND.

The $R_S$ and NTC resistor $R_{TH}$ network generate some quiescent current which may not be negligible under light load. In order to reduce quiescent current under light load, instead of pull down $R_{TH}$ to GND locally at power stage, we can pull down through CMPOUT pin shown in Figure 7-5. Under either TREG is enabled (CMPIN_TR_SELECT=1b & EN_TREG=1b) or thermal PROCHOT channel is enabled (CMPIN_TR_SELECT=1b & PP_THERMAL=1b), then CMPOUT pin is pulled down to GND to generate sensing voltage on CMPIN_TR pin. However under light load both TREG and PP_THERMAL can be both disabled (CMPIN_TR_SELECT=1b & EN_TREG=0b & PP_THERMAL=0b), then device will keep CMPOUT pin high impedance to reduce quiescent current flow through voltage divider network.

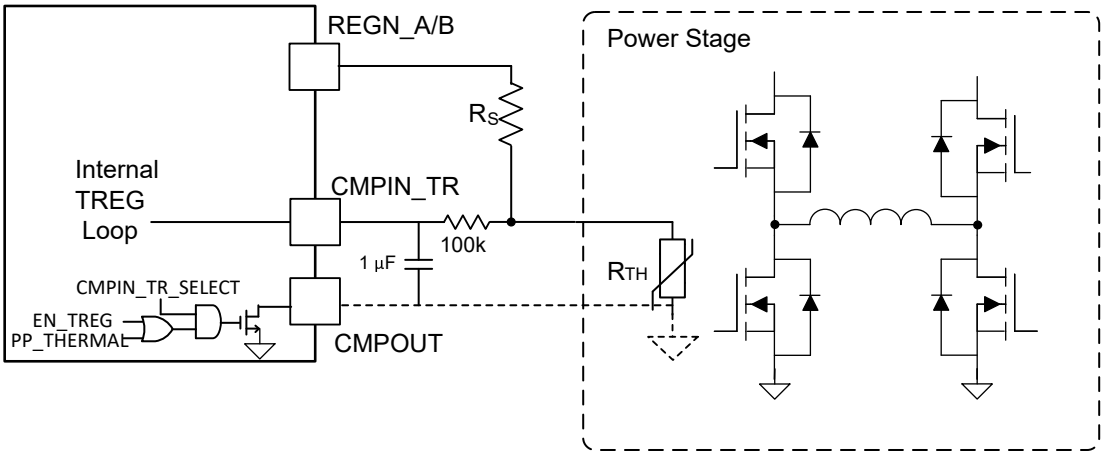


**Figure 7-5. Recommended Configuration for CMPIN_TR Temperature Regulation**

The target temperature regulation value can be chosen through configuring $R_S$ fixed resistor. A 10k NTC thermistor(ERTJ0EG103FA) is recommended in this application, corresponding $R_S$ fixed value can be calculated through equation below. The $R_S$ corresponding value at 60ºC/80ºC/100ºC TREG refers to Table 7-4. The corresponding CMPIN_TR pin voltage with swept temperature under 60ºC/80ºC/100ºC TREG configuration can be found in Figure 7-6. Based on this graph, besides temperature regulation function, the NTC temperature can also be measured through CMPIN_TR pin voltage. The device has a dedicated CMPIN_TR pin voltage ADC channel which can be enabled through setting EN_ADC_CMPIN=1b.

There is a dedicated PROCHOT profile in case regulation target gets overheat more than TREG target. The profile can enabled through setting PP_THERMAL=1b referring to Figure 7-10.

$$R_S = \frac{5V - 1.2V}{1.2V} * R_{NTC}@TREG \quad (1)$$

**Table 7-4. CMPIN_TR Pin RC Network Configuration Reference Based on ERTJ0EG103FA NTC**

| $R_S$ | TREG TEMPERATURE |
|---|---|
| 9.53kΩ | 60ºC |
| 5.23kΩ | 80ºC |
| 3.01kΩ | 100ºC |

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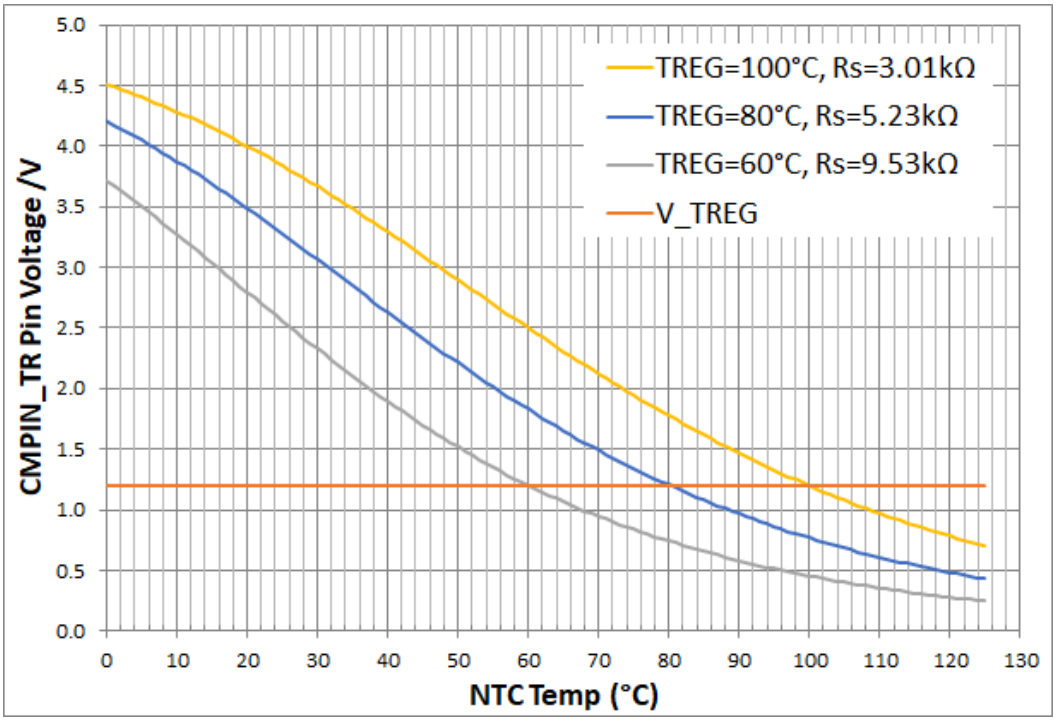


**Figure 7-6. CMPIN_TR Pin Voltage vs Temperature Under Different Regulation Target (60°C/80°C/100°C)**

### 7.3.7 Vmin Active Protection (VAP) When Battery Only Mode

When only battery is connected and adapter is removed, the system peak power pulse for a 2S or 3S system can be very high if the SoC and motherboard systems spikes coincide. These spikes are expected to be very rare, but possible. During these high power spikes, VSYS voltage could drop lower than minimum system voltage and crash the system considering the impedance of BATFET, charge sensing resistor and battery pack internal resistance. In VAP mode the charger first charges up the voltage of the input decoupling capacitors at VBUS to store a certain amount of energy. During these high system power spikes, the the energy stored in the input capacitors will supplement the system, to prevent the system voltage from dropping below the minimum system voltage and leading the system to black screen. The VAP mode can help to achieve much better Turbo performance for Intel CPU. Overall VAP mode is both a protection mechanism used to keep the system voltage from drooping below its minimum operational voltage and a method to boost Turbo performance by allowing Intel CPU to set a peak power higher than the capability of the battery.


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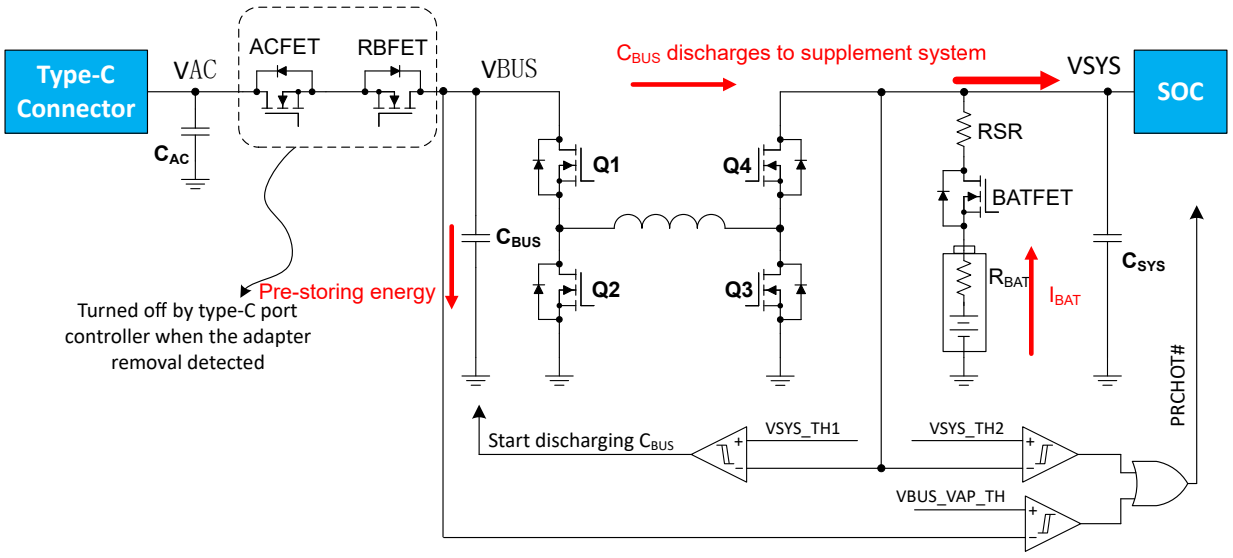


**Figure 7-7. Vmin Active Protection (VAP) Mode Operation Diagram**

To enter VAP mode follow the steps below:

- Set VAP input capacitor voltage regulation target in OTG_VOLTAGE().
- Set VAP mode loading current in OTG_CURRENT().
- Set VSYS_TH1 as the VSYS threshold to begin VAP shooting.
- Set VSYS_TH2 as the VSYS threshold to trigger $\overline{\text{PROCHOT}}$.
- Set VBUS_VAP_TH as the VBUS threshold to trigger $\overline{\text{PROCHOT}}$.
- Set OTG_VAP_MODE=0b to use EN_OTG pin to enabled/disable VAP mode.
- Remove adapter and pull up EN_OTG pin to enter VAP mode.

When an adapter is plugged in or CPU goes to sleep mode, the host can follow below steps to exit VAP mode:

- Pull down EN_OTG pin to disable VAP mode
- Set OTG_VAP_MODE=1b to use EN_OTG pin to enable/disable OTG mode.

EN_OTG pin is used as multi-function pin to enable OTG, VAP and FRS mode. In order to enter VAP mode correctly, refer to Table 7-5 case 7 for reference, note OTG_VAP_MODE=0b should be configured before EN_OTG pin is pulled high. After EN_OTG pin is pulled up, it is not recommended to change OTG_VAP_MODE bit value.

### 7.3.8 Two Level Battery Discharge Current Limit

To prevent the triggering of battery overcurrent protection and avoid battery wear-out, two battery current limit levels (IDCHG_TH1 and IDCHG_TH2) $\overline{\text{PROCHOT}}$ profiles are recommended. Define IDCHG_TH1 through REG0x34h[15:10], IDCHG_TH2 is set through REG0x36[5:3] for fixed percentage of IDCHG_TH1. There are dedicated deglitch time setting registers (IDCHG_DEG1 and IDCHG_DEG2) for both IDCHG_TH1 and IDCHG_TH2.

- When battery discharge current is continuously higher than IDCHG_TH1 for more than IDCHG_DEG1 deglitch time, $\overline{\text{PROCHOT}}$ is asserted immediately. If the discharge current reduces to lower than IDCHG_TH1, then the IDCHG_DEG1 deglitch time counter resets automatically. STAT_IDCHG1 bit will be set to 1 after $\overline{\text{PROCHOT}}$ is triggered.

  Setting PP_IDCHG1=1b to enable IDCHG_TH1 for triggering $\overline{\text{PROCHOT}}$.
- When battery discharge current is continuously higher than IDCHG_TH2 for more than IDCHG_DEG2 deglitch time, $\overline{\text{PROCHOT}}$ is asserted immediately. If the discharge current reduces to lower than IDCHG_TH2, then the IDCHG_DEG2 deglitch time counter resets automatically. STAT_IDCHG2 bit will be set to 1 after $\overline{\text{PROCHOT}}$ is triggered.

  Setting PP_IDCHG2=1b to enable IDCHG_TH2 for triggering $\overline{\text{PROCHOT}}$.

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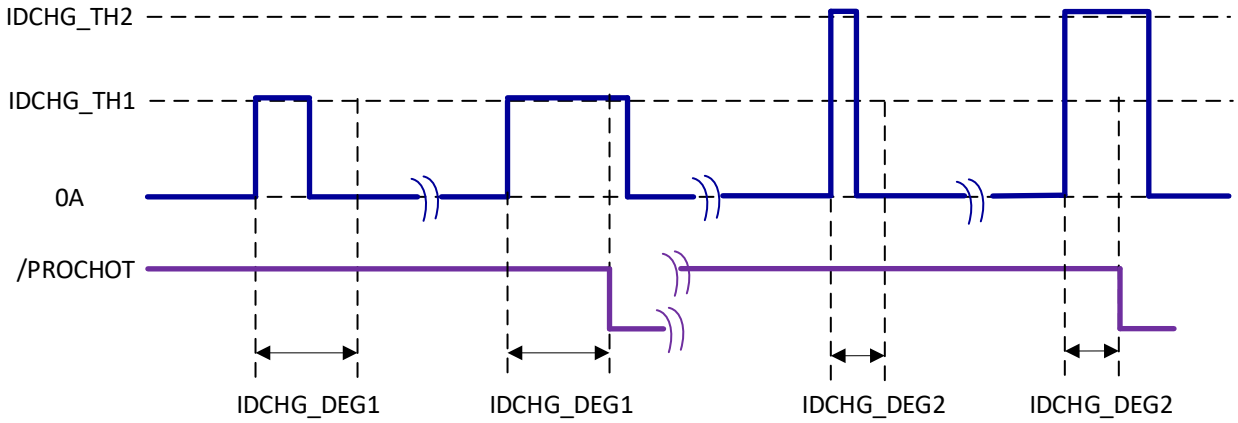


**Figure 7-8. Two Level Battery Discharging Current Trigger $\overline{\text{PROCHOT}}$ Diagram**

### 7.3.9 Fast Role Swap Feature

Fast Role Swap (FRS) means charger quickly swaps from power sink role to power source role to provide an OTG output voltage to accessories when the original power source is disconnected. This feature is defined to transfer the charger from forward mode to OTG mode quickly without dropping VBUS voltage per USB-C PD specification requirement.

To enable FRS feature, EN_FRS bit should be set to 1. When FRS is enabled (EN_FRS = 1), EN_OTG bit and converter OTG mode is only enabled after hardware EN_OTG pin is pulled up. Note when EN_FRS is reset to 0, EN_OTG bit will not be reset automatically, in order to fully exit the OTG mode operation EN_OTG bit need to be reset by the host. The steps for FRS feature operation are listed below.

- Set target IOTG current limit in OTG_CURRENT()
- Set target VOTG voltage in OTG_VOLTAGE()
- Set OTG_VAP_MODE = 1
- Enable FRS feature by setting EN_FRS = 1.
- Remove adapter and VBUS begin to drop
- USB Type-C port PD controller should pull up EN_OTG pin to enable OTG mode. If VBUS>VOTG at the beginning, the converter shuts down and waits for VBUS dropping to VOTG; as long as VBUS≤VOTG, the converter resumes switching and VOTG (CV/CC) loop takes over.

The table below compares VAP, OTG and FRS feature configuration. It is recommended to configure charger into target mode correctly before the EN_OTG pin is pulled up. After the EN_OTG pin is pulled up, it is not recommended to change the OTG_VAP_MODE and EN_FRS bits.

**Table 7-5. VAP /OTG /FRS Configuration Comparison**

| CASE # | CONFIGURATION | | | | | CHARGER STATUS |
|---|---|---|---|---|---|---|
| | EN_OTG PIN | OTG_VAP_MODE BIT | EN_OTG BIT | EN_FRS BIT | BATTERY/ ADAPTER CONFIG | |
| 1 | 0 | X | X | X | Battery only | Battery only Discharge and converter off |
| 2 | 0 | 0 | X | X | Adapter+Battery | Forward mode (without FRS) |
| 3 | 0 | 1 | X | 0 | Adapter+Battery | Forward mode (without FRS) |
| 4 | 0 | 1 | X | 1 | Adapter+Battery | Forward mode (with FRS standby) |
| 5 | 1 | 1 | 0 | X | Battery only | Battery only Discharge and converter off |
| 6 | 1 | 1 | 1 | X | Battery only | OTG mode |


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**Table 7-5. VAP /OTG /FRS Configuration Comparison (continued)**

| CASE # | CONFIGURATION | | | | | CHARGER STATUS |
|---|---|---|---|---|---|---|
| | EN_OTG PIN | OTG_VAP_MODE BIT | EN_OTG BIT | EN_FRS BIT | BATTERY/ ADAPTER CONFIG | |
| 7 | 1 | 0 | X | X | Battery only | VAP mode |

### 7.3.10 CHRG_OK Indicator

CHRG_OK is an active high open drain indicator. Under forward mode when VBUS is above $V_{VBUS_CONVEN}$ then CHRG_OK pin behavior is summarized below:

- Under non-latched faults ACOV/ACOC/TSHUT/BATOVP (only when charge is enabled)/BATDOC/ REGN_PG/force converter off, CHRG_OK will be pulled down for minimum pulse 256 µs. Even the fault is removed before 256 µs expire, the CHRG_OK pin should still be pulled down until 256 µs timer expires. When 256 µs timer expires, if the fault still exists then the CHRG_OK pin should be kept low.
- Under latched faults SYSOVP/VSYS_UVP, CHRG_OK will be pulled down and latched until EC write 0b to FAULT_SYSOVP/FAULT_VSYS_UVP bits.
- CHRG_OK pin can be also configured as interrupt source to inform host about the CHRG_STAT bits changes. To enable this, host needs to set CHRG_OK_INT bit to be 1b, then whenever there is a change in CHRG_STAT bits, CHRG_OK pin will be pulled down for 256 µs to inform the host. Note: safety timer changes the CHRG_STAT status as well when triggered, therefore when CHRG_OK_INT bit is set 1b, CHRG_OK pin is pulled down for 256 µs when safety timer triggers.

Under battery only OTG mode, if OTG_ON_CHRGOK=1b, the CHRG_OK pin should be low when converter shuts off due to faults SYSOVP/VSYS_UVP/OTG_UVP/OTG_OVP/TSHUT/BATDOC/REGN_PG/force converter off; if OTG_ON_CHRGOK=0b, the CHRG_OK pin should be always be pulled down.

### 7.3.11 Input and Charge Current Sensing

The charger supports 10 mΩ and 5 mΩ for input current sensing . By default 10 mΩ is enabled by POR setting RSNS_RAC=0b. If 5-mΩ sensing is used, configure RSNS_RAC=1b. Lower current sensing resistor can help improve overall charge efficiency especially under heavy load. At same time, PSYS/IADPT pin accuracy and IINDPM/IOTG regulation accuracy get worse due to effective signal reduction in comparison to error signal components.

The charger supports 5 mΩ and 2 mΩ for charge current sensing . By default 5 mΩ is enabled by POR setting RSNS_RSR=0b. If 2-mΩ sensing is used, configure RSNS_RSR=1b. Lower current sensing resistor can help improve overall charge efficiency especially under heavy load. At same time, PSYS/IBAT pin accuracy and ICHG/IPRECHG regulation accuracy is reduced due to effective signal reduction in comparison to error signal components.

When RSNS_RAC=RSNS_RSR=0b, 10 mΩ is used for input current sensing and 5 mΩ is used for charge current sensing, the pre-charge current upper limit is clamped at 2016 mA through IPRECHG() register, the maximum IIN_HOST setting is clamped at 8.2 A, and the maximum charge current is clamped at 16.32 A.

When RSNS_RAC=RSNS_RSR=1b, 5 mΩ is used for input current sensing and 2 mΩ is used for charge current sensing, the maximum IIN_HOST setting is clamped at 16.4 A. The maximum charge current is clamped at 30 A (with 20 mA LSB , 5DCh for CHARGE_CURRENT[13:3]). System note: Under 2-mΩ charge resistor, the pre-charge current upper limit is compensated and still clamped at 2040 mA through IPRECHG() register (66H). However $I_{BAT_SHORT}$ does not need to be compensated should increase from 128 mA (RSR=5 mΩ) to 320 mA(RSR=2 mΩ).

If PSYS function is needed, practical input current sensing and charge current sensing should be consistent with RSNS_RSR and RSNS_RAC configuration. This is necessary because of the PSYS calculation method referring to Equation 2.

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### 7.3.12 Input Current and Voltage Limit Setup

The actual input current limit being adopted by the device is the lower value of IIN_DPM and ILIM_HIZ pin. Register IIN_DPM input current limit value will be updated on below scenarios:

- IIN_DPM() will be updated based on IIN_HOST() value except ICO is executed listed below.
- When adapter is removed, IIN_HOST will be reset to 5 A, host can re-write IIN_HOST to new values after reset under battery only. If the adapter plugs back in and CHRG_OK is pulled up, IIN_HOST will not be reset again. IIN_DPM follows IIN_HOST value in this scenario.
- When input current optimization (ICO) is executed (EN_ICO_MODE=1b), the charger will automatically detect the optimized input current limit based on adapter output characteristic. The final IIN_DPM register setting could be different from IIN_HOST after ICO.

The input current limit function is enabled by default through (EN_IIN_DPM=1b), it can be disabled through setting EN_IIN_DPM=0b. Status bit IN_IIN_DPM is used to report input current under IIN_DPM() regulation.

The input voltage limit is configurable through VINDPM() register bits. Upon POR, VINDPM() default setting is A0h (3.2 V). EC host can rewrite to the target value after POR. There is also DETECT_VINDPM bit to DETECT VINDPM based on VBUS measurement result minus 1.28 V. Write 1b to DETECT_VINDPM bit to start the process, then converter shuts off to measure VBUS. After VBUS measurement is done, VINDPM() is written with value VBUS-1.28 V, DETECT_VINDPM bit goes back to 0 and converter starts up again. Status bit IN_VINDPM is used to report input voltage is under VINDPM regulation.

### 7.3.13 Battery Cell Configuration

CELL_BATPRES pin is biased with a resistor divider from REGN_A/B to GND. After REGN_A/B ramps up or CELL_BATPRES pin ramps up, the device detects the battery configuration through CELL_BATPRES pin bias voltage after 2ms delay time. No external cap is allowed at CELL_BATPRES pin. When CELL_BATPRES pin is pulled down to GND at the beginning of device start up process, CHARGE_VOLTAGE(), SYSOVP, VSYS_MIN() and VRECHG() follow battery removal row in the table below.

After device start up when battery is removed, CELL_BATPRES pin should be pulled low through external MOSFET shown in application diagram. If CELL_BATPRES pin is pulled lower than $V_{CELL_BATPRES_FALL}$ for 1ms deglitch time, then device disables charge by resetting CHARGE_CURRENT()=000h and EN_AUTO_CHG=0b; at same time, CHARGE_VOLTAGE(), SYSOVP, VSYS_MIN() and VRECHG() are not changed. When REGN_A/B voltage rises up or CELL_BATPRES pin is increased higher than $V_{CELL_BATPRES_RISE}$, the device should re-read cell configuration again with 2ms delay time: CHARGE_VOLTAGE(), SYSOVP, VSYS_MIN() and VRECHG() should be re-detected to corresponding cell setting default value if they are not changed by EC before; if any of CHARGE_VOLTAGE(), SYSOVP, VSYS_MIN() and VRECHG() are changed by EC before this re-detection then their value should not be influenced by the new detection process anymore. This is needed to avoid EC writing target value back and forth. Refer to Table 7-6 for CELL_BATPRES pin configuration typical voltage for swept cell count. Note if device is in learn mode (EN_LEARN=1b). Pulling CELL_BATPRES pin low clears EN_LEARN bit to 0b and forces device to exit learn mode.

When CELL_BATPRES pin is pulled to ground, battery removal is indicated. Since there is no battery supplement, the charger can automatically disable IIN_DPM by setting EN_IIN_DPM to 0 to minimize VSYS voltage drop. This function can be enabled through setting IIN_DPM_AUTO_DISABLE=1b. The host can re-enable IIN_DPM function later by writing EN_IIN_DPM bit to 1.

**Table 7-6. Battery Cell Configuration**

| CELL COUNT | PIN VOLTAGE w.r.t. REGN_A/B | CHARGE_VOLTAGE() | SYSOVP | VSYS_MIN | VRECHG |
|---|---|---|---|---|---|
| 5S | 100% | 21.000 V | 27V | 15.4V | 500mV |
| 4S | 75% | 16.800 V | 22 V | 12.3V | 400mV |
| 3S | 55% | 12.600 V | 17 V | 9.2V | 300mV |
| 2S | 40% | 8.400 V | 12 V | 6.6V | 200mV |
| Battery removal | 0% | 8.400 V | 27 V | 6.6V | 200mV |


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### 7.3.14 Device HIZ State

When input source is present, the charger enters HIZ mode when ILIM_HIZ pin voltage is below 0.4 V or EN_HIZ is set to 1b. During HIZ mode converter shuts off and BATFET is turned on to supplement system from battery if BATFETOFF_HIZ=0b. The BATFET can also be turned off during HIZ mode through setting BATFETOFF_HIZ=1b. In order to exit HIZ mode, ILIM_HIZ pin voltage has to be higher than 0.8 V and EN_HIZ bit has to be set to 0b. Once host clears HIZ mode, converter resumes switching and BATFET is turned off again.

### 7.3.15 USB On-The-Go (OTG)

The device supports USB OTG operation to deliver power from the battery to other portable devices through USB port. The OTG output voltage is set in OTG_VOLTAGE() register with 20 mV LSB range from 3.0 V to 5 V. The OTG output current limit is set in OTG_CURRENT() register with 50 mA LSB range from 0 A to 3 A under 10 mΩ input current sensing. Status bit IN_IIN_DPM is used to report output current is under OTG_CURRENT() regulation; status bit IN_VINDPM is used to report output voltage is under OTG_VOLTAGE() regulation. Both OTG voltage and OTG current are qualified for USB-PD programed power supply (PPS) specification in terms of resolution and accuracy. The OTG operation can be enabled if the conditions are valid:

- Set target OTG current limit in OTG_CURRENT() register.
- Set target OTG voltage in OTG_VOLTAGE() register.
- VBUS is below $V_{VBUS_CONVENZ}$.
- VBAT is higher than $V_{BAT_OTGEN}$ level.
- EN_OTG pin is HIGH, EN_OTG = 1b and OTG_VAP_MODE = 1b.
- 15 ms after the above conditions are valid, converter starts and VBUS ramps up to target voltage. CHRG_OK pin goes high if OTG_ON_CHRGOK= 1b.

EN_OTG pin is used as multi-function to enable OTG, VAP and FRS mode. In order to enable OTG mode correctly, please refer to Table 7-5 case 6. OTG_VAP_MODE=1b should be configured before EN_OTG pin pulled high. After EN_OTG pin is pulled up, it is not recommended to change OTG_VAP_MODE bit value.

### 7.3.16 Quasi Dual Phase Converter Operation

Converter can be configured under quasi dual phase buck boost operation through MODE pin referring to Table 7-1. The charger operates in buck, buck-boost and boost mode under different VBUS and VSYS combination. The buck-boost can operate seamlessly across the three operation modes. The 6 main switches operating status under continuous conduction mode (CCM) are listed below for reference.

- Buck mode operation: Q4 is constant on and two buck phases should both switching at frequency determined at PWM_FREQ bit. There should be 180 degree interleave between phase A and B to minimize inductor total ripple and finally reduce VBUS and VSYS voltage ripple. Supporting phase shedding feature, converter can automatically transit to phase A single phase operation under light load. The transition threshold is based on SINGLE_DUAL_TRANS_TH bits configuration.
- Buck-boost mode operation: Under quasi dual phase configuration, 2*Fsw switching frequency will be distributed between two buck phases and one boost phase. They should switch in sequence like SW1_A->SW2->SW1_A->SW1_B->SW2-> SW1_B->SW1_A->SW2->SW1_A... equivalent frequency of each phase can be calculated by 2*Fsw/3. For example, when PWM_FREQ=1b (600 kHz), then Phase A, Phase B and boost phase leg will be switching at 400 kHz.
- Boost mode operation: Q1_A and Q1_B should be constant on and the boost half bridge keeps switching at frequency determined at PWM_FREQ bit. Due to two buck phase inductors are in parallel to reduce total inductor current ripple, under boost mode switching frequency is doubled to 2*Fsw (MODE pin configured as quasi dual phase). There could be some CCM/PFM bounce back and force under certain load range( around 2.5A~3A). This bounce will not generate negative input current at input side but could generate some charge current ripple. Once load is higher or lower than this critical range, this issue will disappear.

**Table 7-7. MOSFET Operation**

| MODE | BUCK | BUCK-BOOST | BOOST |
|---|---|---|---|
| Q1_A | Switching at Fsw (interleave with Q1_B) | Switching (sequence with Q1_B and Q4) | ON |

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**Table 7-7. MOSFET Operation (continued)**

| MODE | BUCK | BUCK-BOOST | BOOST |
|---|---|---|---|
| Q2_A | Switching at Fsw (interleave with Q2_B) | Switching (sequence with Q2_B and Q3) | OFF |
| Q1_B | Switching at Fsw (interleave with Q1_A) | Switching (sequence with Q1_A and Q4) | ON |
| Q2_B | Switching at Fsw (interleave with Q2_A) | Switching (sequence with Q2_A and Q3) | OFF |
| Q3 | OFF | Switching (sequence with Q2_A and Q2_B) | Switching at 2*Fsw |
| Q4 | ON | Switching (sequence with Q1_A and Q1_B) | Switching at 2*Fsw |

### 7.3.17 Continuous Conduction Mode (CCM)

With sufficient charge or system current, converter operates under CCM. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM, the inductor current always flows. Having the LSFET turn-on when the HSFET is off keeps the power dissipation low and allows safe charging at high currents.

### 7.3.18 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, BQ25770G switches to PFM operation at light load. The effective switching frequency will decrease accordingly when system load decreases. The minimum frequency can be limited to 20 kHz when the OOA feature is enabled (EN_OOA=1b).

### 7.3.19 Switching Frequency and Dithering Feature

Normally, the IC switches in fixed frequency which can be adjusted through FSW_SYNC pin. The charger also supports frequency dithering function to improve EMI performance and help pass IEC-CISPR 32 specification. This function is disabled by default with setting EN_DITHER=00b. It can be enabled by setting EN_DITHER=01/10/11b, the switching frequency is not fixed when dithering is enabled, it varies within determined range by EN_DITHER setting, 01/10/11b is corresponding to ±2%/4%/6% switching frequency. The larger dithering range is selected, the smaller EMI noise peak will be, but at same time slightly larger output capacitor voltage ripple is generated. Therefore, the dithering frequency range selection is a trade-off between EMI noise peak and output voltage ripple, recommend to choose the lowest dithering range which can pass IEC-CISPR 32 specification. The patented dithering pattern can improve EMI performance from switching frequency and up to 30-MHz high frequency range which covers the entire conductive EMI noise range.

It should be noted that the Dithering feature will not work if an external clock is provided.

### 7.3.20 Current and Power Monitor

#### *7.3.20.1 High-Accuracy Current Sense Amplifier (IADPT and IBAT)*

A high-accuracy current sense amplifier (CSA) is used to monitor the input current during forward charging, or output current during OTG (IADPT) and the charge/discharge current (IBAT). IADPT voltage is 20× (IADPT_GAIN=0b) or 40× (IADPT_GAIN=1b) the differential voltage across ACP_A and ACN_A plus ACP_B and ACN_B. IBAT voltage is 8× (IBAT_GAIN=0b) or 64×(IBAT_GAIN=1b) of the differential across SRP and SRN. To lower the voltage on current monitoring, a resistor divider from IADPT/IBAT output to GND can be used, and accuracy over temperature can still be achieved. Recommend the total resistance of the divider circuit should be at least 100 kΩ to prevent crashing IADPT/IBAT pin voltage.

- $V_{IADPT}$ = 20 or 40 × ($V_{ACP_A} – V_{ACN_A}+V_{ACP_B} – V_{ACN_B}$) during forward mode and polarity is automatically flipped $V_{(IADPT)}$ = 20 or 40 × ($V_{ACN_A} – V_{ACP_A}+V_{ACN_B} – V_{ACP_B}$) during reverse OTG mode operation.
- $V_{IBAT}$ = 8 or 64 × ($V_{SRP} – V_{SRN}$) during forward mode charging. Need to configure EN_IBAT=1b and EN_ICHG_IDCHG=1b.
- $V_{IBAT}$ = 8 or 64 × ($V_{SRN} – V_{SRP}$) during forward supplement mode, reverse OTG mode and battery only discharge scenario. Need to configure EN_IBAT=1b and EN_ICHG_IDCHG=0b.


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A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional. Note that RC filtering has additional response delay. The IADPT and IBAT output voltages are clamped at 3.2 V.

#### *7.3.20.2 High-Accuracy Power Sense Amplifier (PSYS)*

The charger monitors total system power. During forward mode, the input adapter powers the system. During reverse OTG mode and battery only discharge scenario, the battery powers the system and VBUS output. The ratio of PSYS pin output current and total system power, $K_{PSYS}$, can be programmed in PSYS_RATIO register bit with default 1 μA/W. The input and charge sense resistors (RAC and RSR) are selected in RSNS_RAC bit and RSNS_RSR bit. If PSYS_CONFIG=00b then PSYS voltage can be calculated with Equation 2, where $I_{IN_A}/I_{IN_B}$ >0 when the charger is in forward charging and $I_{IN_A}/I_{IN_B}$ <0 when charger is in OTG operation; where $I_{BAT}$<0 when the battery is in charging and $I_{BAT}$>0 when battery is discharging.

$$V_{PSYS} = R_{PSYS} \cdot K_{PSYS} (V_{ACP_A} \cdot I_{IN_A} + V_{ACP_B} \cdot I_{IN_B} + V_{SYS} \cdot I_{BAT}) \quad (2)$$

For proper PSYS functionality, RAC practical value is limited to 10 mΩ or 5 mΩ and should be consistent with RSNS_RAC register setting; RSR practical value is limited to 5 mΩ or 2 mΩ and should be consistent with RSNS_RSR register setting.

Charger can block IBAT contribution to above equation by setting PSYS_CONFIG =01b in forward mode and block IBUS contribution to above equation by setting PSYS_OTG_IDCHG=1b.

To minimize the quiescent current, the PSYS function is disabled by default PSYS_CONFIG = 11b.

**Table 7-8. PSYS Configuration Table**

| CASE # | PSYS_CONFIG BITS | PSYS_OTG_IDCHG BITS | FORWARD MODE PSYS CONFIGURATION | OTG MODE PSYS CONFIGURATION |
|---|---|---|---|---|
| 1 | 00b | 0b | PSYS=PBUS+PBAT | PSYS=PBUS+PBAT |
| 2 | 00b | 1b | PSYS=PBUS+PBAT | PSYS=PBAT |
| 3 | 01b | 0b | PSYS=PBUS | PSYS=0 |
| 4 | 01b | 1b | PSYS=PBUS | PSYS=0 |
| 5 | 11b | Xb | PSYS=0(Disabled) | PSYS=0(Disabled) |

### 7.3.21 Input Source Dynamic Power Management

The charger supports Dynamic Power Management (DPM). Normally, the input power source provides power for the system load and/or charging the battery. When the input current exceeds the input current setting(IIN_DPM), or the input voltage falls below the input voltage setting(VINDPM), the charger decreases the charge current to provide priority to the system load. As the system current rises, the available charge current drops accordingly towards zero. If the system load keeps increasing after the charge current drops down to zero, the system voltage starts to drop. As the system voltage drops below the battery voltage, the battery will discharge to supply the heavy system load.

### 7.3.22 Integrated 16-Bit ADC for Monitoring

The device includes a 16-bit ADC to monitor critical system information based on the device's modes of operation. The control of the ADC is done through the ADCOption register. There are total 7 ADC channels can be enabled independently through ADCOption registers [7:0] bits. The ADC_RATE bit is used to select between continuous conversion and one-shot conversion. When continuous conversion is chosen, each enabled ADC channel will be executed one by one and continuously, the ADC cycling refresh time can be calculated by the product of enabled ADC channel count(ADCOption registers [7:0] setting) and the ADC_SAMPLE configuration (24ms/12ms/6ms). When one-shot conversion is selected, ADC_EN is used to start one-shot conversion, after a 1-shot conversion finishes, the ADC_EN bit is cleared, and must be re-asserted to start a new conversion. When ADC is under continuous mode, then ADC_EN is used to enable continuous ADC operation. To enable each channel ADC not only ADC_EN should be configured at 1b, but also need to enable the dedicated channels

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in ADCOption registers [7:0] bits. The device will immediately reset ADC_EN to 0b when all ADC channels are disabled.

The ADC is allowed to operate if either the VBUS>$V_{VBUS_CONVEN}$ or VBAT>$V_{VBAT_UVLOZ}$ is valid. If no adapter is present (VBUS<$V_{VBUS_CONVENZ}$), and the VBAT is less than $V_{VBAT_UVLO}$, the device will not perform an ADC measurement, nor update the ADC read-back values. Additionally, the device will immediately reset ADC_EN to 0b. If the charger changes mode (for example, if adapter is connected) while an ADC conversion is running, the conversion is interrupted. Once the mode change is complete, the ADC resumes conversion, starting with the channel where it was interrupted.

The ADC_SAMPLE bits control the resolution of the ADC, and also determine conversion time of $t_{ADC_CONV}$ based on resolution. The total conversion time of one cycle ADC of all channels enabled can be estimated using channel counts multiplied by the corresponding $t_{ADC_CONV}$ determined by ADC_SAMPLE setting. If an ADC channel is disabled by setting the corresponding bit, then the read-back value in the corresponding register will be from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place). If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in ADCOption register[7:0] is set to ‘1’.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN to ‘0b’ in order to disable the ADC. ADC conversion is interrupted upon adapter plug-in, and will only resume after REGN regulator is enabled from the input. ADC readings are only valid for DC states and not for transients. When host disables ADC by setting ADC_EN to 0b, the ADC stops immediately, and ADC measurement values correspond to last valid ADC reading.

If the host wants to exit continuous ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE to one-shot, and the ADC will stop at the end of a complete cycle of conversions, or
2. Disable all ADC conversion channels, and the ADC will stop at the end of the current measurement.

When system load is powered from the battery (input source is removed, or device in HIZ mode), enabling the ADC automatically powers up REGN and increases the quiescent current. To keep the battery leakage low, it is recommended to duty cycle or completely disable the ADC.

### 7.3.23 Input Current Optimizer (ICO)

Even though the IINDPM and VINDPM features are useful to keep the system load running when reaching the adapter limit. However, the adapter will overheat when keeping it running at its current and voltage limit for a long period of time. Thus it is preferred to operate the adapter under its current rating is preferred.

The charger includes innovative automatic Input Current Optimizer (ICO) to maximize the power of input source with input current limit higher than 500 mA. Below is the steps to execute ICO function:

- Make sure system can power up by the adapter and battery can be charged in CC phase
- Set VINDPM() register value to slightly below the adapter voltage with full load specification
- Set IIN_HOST() register value to the maximum amount of input current limit the user would like to sink on VBUS
- Disable external ILIM_HIZ by setting EN_EXTILIM=0b. When ICO is disabled, IIN_DPM register value should be the same as IIN_HOST.
- Set charge current in CHARGE_CURRENT register to design specification which should be high enough to support ICO evaluation
- Enable ICO test by setting EN_ICO_MODE=1b, and wait for approximately 2sec, and check the ICO_DONE status bit. If this bit goes to 1, ICO is completed
- After ICO_DONE=1b, read back ICO result in IIN_DPM register for current adapter. Value in IIN_HOST register is not changed by ICO. If the host sets EN_ICO_MODE bit back to zero, the IIN_DPM returns to the setting in IIN_HOST. To continue use the optimal input current limit identified by ICO, it is recommended to read IIN_DPM register after ICO is done and write this value back to IIN_HOST.


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### 7.3.24 Two-Level Adapter Current Limit (Peak Power Mode)

Usually adapter can supply current higher than DC rating for a few milliseconds to tens of milliseconds. The charger employs two-level input current limit, or peak power mode, to fully utilize the overloading capability and minimize battery discharge during CPU turbo mode. The level 1 current limit, or $I_{LIM1}$, is the same as adapter DC current, set in IIN_DPM register. The level 2 overloading current, or $I_{LIM2}$, is set in ILIM2_VTH, as a percentage of $I_{LIM1}$.

When the charger detects input current surge and battery discharge due to load transient (both the adapter and battery support the system together), or when the charger detects the system voltage starts to drop below VSYS_MIN register setting due to load transient (only the adapter supports the system).The charger will first apply $I_{LIM2}$ for $T_{OVLD}$ (PKPWR_TOVLD_DEG register bits), and then $I_{LIM1}$ for up to $T_{MAX}$ – $T_{OVLD}$ time. $T_{MAX}$ is programmed in PKPWR_TMAX register bits. After $T_{MAX,}$ if the load is still high, another peak power cycle starts. Charging is disabled during $T_{MAX}$; once $T_{MAX,}$ expires, charging continues. During $T_{OVLD}$ if PP_INOM=1b and input current exceed 110%*$I_{LIM1}$, the $\overline{\text{PROCHOT}}$ pin should be pulled down after INOM_DEG deglitch time expires. The details can be found in Figure 7-9.

To prepare entering peak power follow the steps below:

- Set EN_IIN_DPM=1b to enable input current dynamic power management.
- Set EN_EXTILIM=0b to disable external current limit.
- Set register IIN_HOST based on adapter output current rating as the level 1 current limit($I_{LIM1}$)
- Set register bits ILIM2_VTH according to the adapter overload capability as the level 2 current limit($I_{LIM2}$) .
- Set register bits PKPWR_TOVLD_DEG as $I_{LIM2}$ effective duration time for each peak power mode operation cycle based on adapter capability.
- Set register bits PKPWR_TMAX as each peak power mode operation cycling time based on adapter capability.

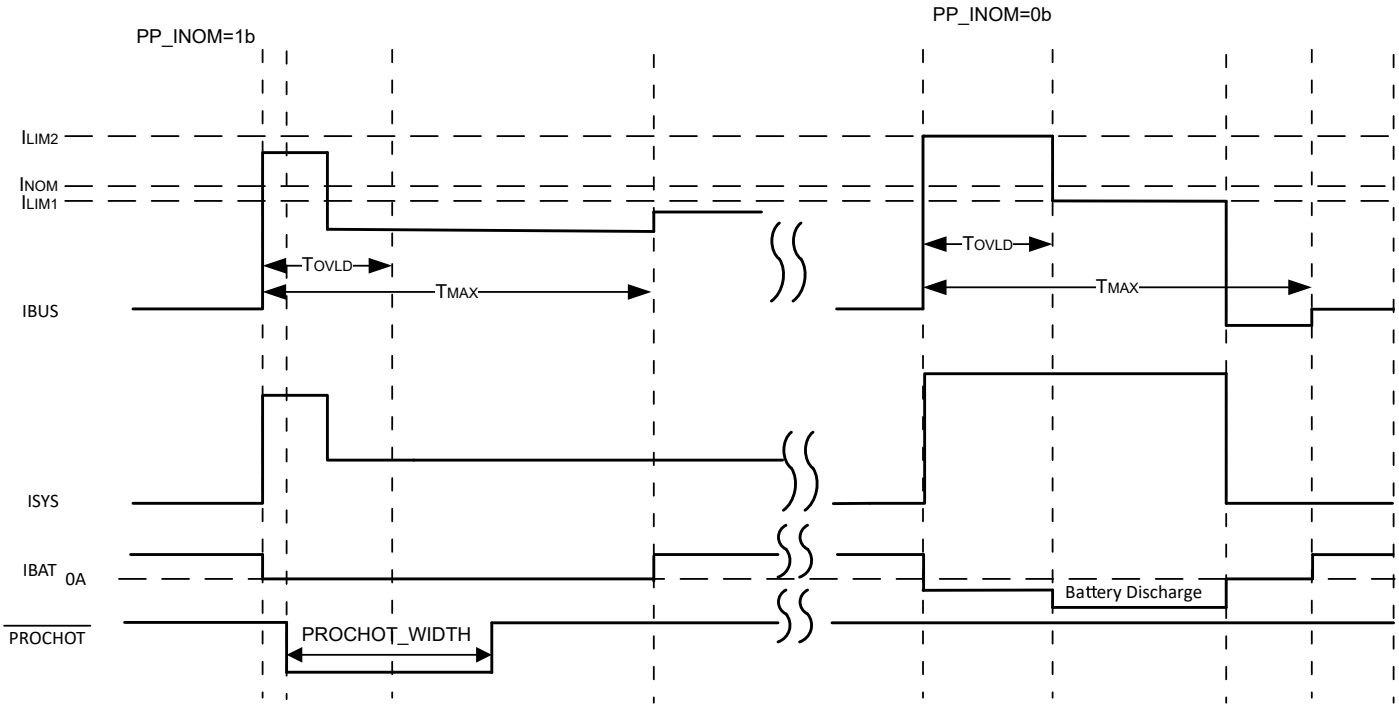


**Figure 7-9. Two-Level Adapter Current Limit Timing Diagram**

### 7.3.25 Processor Hot Indication

When CPU is running in turbo mode, the system peak power may exceed available power from adapter and battery together. The adapter current and battery discharge peak current, or system voltage drop is an indication that system power is too high. The charger processor hot function monitors these events, and $\overline{\text{PROCHOT}}$ pulse

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is asserted if the system power is too high. Once CPU receives $\overline{\text{PROCHOT}}$ pulse from charger, it slows down to reduce system power. The events monitored by the processor hot function include:

- ICRIT: adapter peak current, as 110% of $I_{LIM2}$
- INOM: adapter average current (110% of IIN_DPM)
- IDCHG1: battery discharge current level 1
- IDCHG2: battery discharge current level 2. Note that IDCHG2 threshold is always larger than IDCHG1 threshold, determined by IDCHG_TH2 register setting.
- VBUS_VAP: VBUS threshold to trigger PROCHOT in VAP mode
- VSYS: system voltage on VSYS.
- Adapter Removal: upon adapter removal ($\overline{\text{PROCHOT}}$ pin is one time falling edge trigger when VBUS falls below $V_{VBUS_CONVENZ}$ threshold and deglitch time is within 1 µs. If triggered, STAT_ADAPTER_REMOVAL bit will be set to 1b, it will be high until clear through host read or REG_RESET bit. The status bit is level trigger which means if VBUS is still below $V_{VBUS_CONVENZ}$ when status bit gets cleared, then the status bit should be triggered again immediately)
- Battery Removal: upon battery removal ($\overline{\text{PROCHOT}}$ pin is one time falling edge trigger when CELL_BATPRES pin voltage falls below $V_{CELL_BATPRES_FALL}$ and deglitch time is within 1 µs. If triggered STAT_BATTERY_REMOVAL bit will be set to 1b, it will be locked until clear through host read or REG_RESET bit. The status bit is also falling edge trigger which means if CELL_BATPRES pin is still below $V_{CELL_BATPRES_FALL}$ when status bit gets cleared, the status bit will still be cleared to 0b)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)
- VINDPM: VBUS lower than 83%/91%/100% of VINDPM setting. The effective threshold PROCHOT_VINDPM is determined by combination of register PROCHOT_VINDPM_80_90 bit and LOWER_PROCHOT_VINDPM bit:
  - PROCHOT_VINDPM=VINDPM register setting: LOWER_PROCHOT_VINDPM=0b;
  - PROCHOT_VINDPM=83% VINDPM register setting: LOWER_PROCHOT_VINDPM=1b;PROCHOT_VINDPM_80_90=0b;
  - PROCHOT_VINDPM=91% VINDPM register setting: LOWER_PROCHOT_VINDPM=1b;PROCHOT_VINDPM_80_90=1b;
- EXIT_VAP: Every time when the charger exits VAP mode.
- THERMAL: If enabled (PP_THERMAL=1b), then when the CMPIN_TR pin voltage is lower than $V_{TREG_PP}$ for 1s/100ms (THERMAL_DEG bit configurable) deglitch time. Then STAT_THERMAL will be latched until clear through host read or REG_RESET bit.

The thresholds of ICRIT, IDCHG1,IDCHG2,VSYS or VINDPM, and the deglitch times of ICRIT, INOM, IDCHG1, IDCHG2, or CMPOUT are programmable. Except for the PROCHOT_EXIT_VAP which is always enabled, the other triggering events can be individually enabled in ProchotOption1[7:0], PP_IDCHG2 and PP_VBUS_VAP. When any enabled event in $\overline{\text{PROCHOT}}$ profile is triggered, $\overline{\text{PROCHOT}}$ is asserted low for a single pulse with minimal width programmable in PROCHOT_WIDTH register bits. At the end of the single pulse, if the $\overline{\text{PROCHOT}}$ event is still active, the pulse gets extended until the event is removed.

If the $\overline{\text{PROCHOT}}$ pulse extension mode is enabled by setting EN_PROCHOT_EXT= 1b, the $\overline{\text{PROCHOT}}$ pin will be kept as low until host writes PROCHOT_CLEAR= 1b, even if the triggering event has been removed.

If the PROCHOT_VINDPM or PROCHOT_EXIT_VAP is triggered, $\overline{\text{PROCHOT}}$ pin will always stay low until the host clears it, no matter the $\overline{\text{PROCHOT}}$ is in one pulse mode or in extended mode. In order to clear PROCHOT_VINDPM, host needs to write 0 to STAT_VINDPM. In order to clear PROCHOT_EXIT_VAP, host needs to write 0 to STAT_EXIT_VAP.


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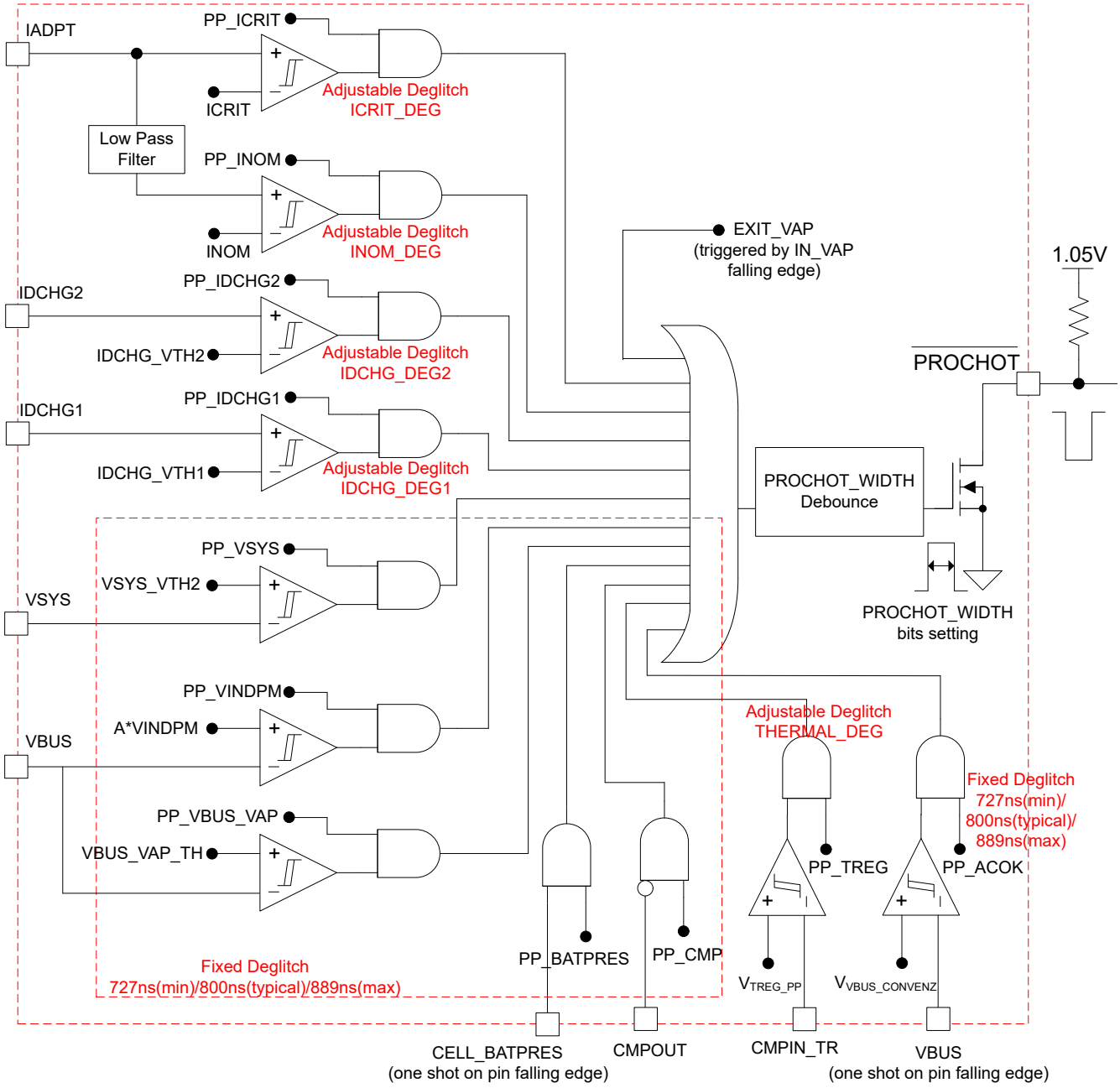


**Figure 7-10. $\overline{\text{PROCHOT}}$ Profile**

### *7.3.25.1 $\overline{\text{PROCHOT}}$ During Low Power Mode*

During low power mode (EN_LWPWR = 1), the charger offers a low power $\overline{\text{PROCHOT}}$ function with very low quiescent current consumption, which uses the independent comparator. This is commonly used to monitor the system voltage, and assert $\overline{\text{PROCHOT}}$ to CPU if the system power is too high and resulting system voltage is lower than specific threshold.

The register setting to enable $\overline{\text{PROCHOT}}$ monitoring system voltage in low power mode is listed below.

- EN_LWPWR = 1b to enable charger low power mode.
- REG0x34[7:0] = 00h
- REG0x30[6:4] = 000b
- Independent comparator threshold is always 1.2 V

- Set EN_LWPWR_CMP = 1b, CMP_POL=1b and PP_CMP=1b, charger monitors system voltage. Connect CMPIN to voltage proportional to system voltage. $\overline{\text{PROCHOT}}$ triggers from HIGH to LOW when comparator triggers low effective with VSYS falls below certain threshold .

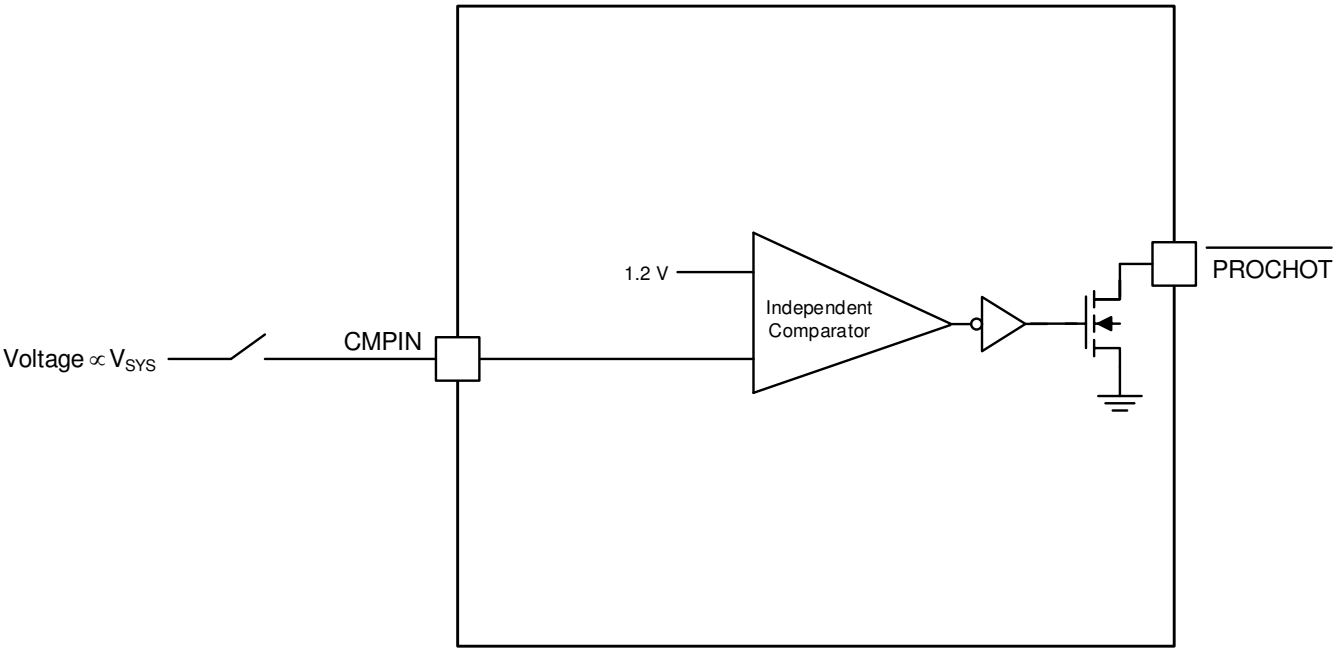


**Figure 7-11. $\overline{\text{PROCHOT}}$ Low Power Mode Implementation**

#### *7.3.25.2 $\overline{\text{PROCHOT}}$ Status*

REG0x21[8:0] reports which event in the profile triggers $\overline{\text{PROCHOT}}$ if the corresponding bit is set to 1. The status bit can be reset back to 0 after it is read by the host, when the current $\overline{\text{PROCHOT}}$ event is not active any more.

Assume there are two $\overline{\text{PROCHOT}}$ events, event A and event B. Event A triggers $\overline{\text{PROCHOT}}$ first, but event B is also active. Both status bits will be HIGH. At the end of the 10 ms $\overline{\text{PROCHOT}}$ pulse, if any of the $\overline{\text{PROCHOT}}$ event is still active (either A or B), the $\overline{\text{PROCHOT}}$ pulse is extended.

### 7.3.26 Device Protection

#### *7.3.26.1 Watchdog Timer (WD)*

The charger includes watchdog timer 175s (default value and adjustable via WDTMR_ADJ) to reset some registers including:

- Reset CHARGE_CURRENT() to 0 A to disable charge;
- Reset EN_CHG_TMR bit to 1b to re-enable CHG timer. If it is already enabled then no change.
- Reset EN_OTG bit to 0b to disable OTG operation.
- Reset ADC_EN bit 0b to disable ADC to save quiescent current.

There are four methods to reset the watchdog timer to prevent it from expiration, as long as one of them is met then watchdog timer will be reset:

- Write CHARGE_VOLTAGE() register;
- Write CHARGE_CURRENT() register;
- Write WD_RST bit to 1b, this bit will automatically to back to 0b after watchdog timer is reset.
- Update a new watchdog timer value at WDTMR_ADJ bits, then the timer is reset with new value.

Write WDTMR_ADJ = 00b to disable watchdog timer. New non-zero charge current value has to be written to charge current register CHARGE_CURRENT() to resume charging after watchdog timer expires.


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#### 7.3.26.2 Input Overvoltage Protection (ACOV)

The charger support input over voltage protection which holds ACOV threshold with hysteresis. When VBUS pin voltage is higher than $V_{ACOV_RISE}$ for more than 100 µs, it is considered as adapter over voltage. CHRG_OK pin will be pulled low by the charger, and the converter shuts down. As system falls below battery voltage, BATFET will be turned on. When VBUS pin voltage falls below $V_{ACOV_FALL}$ for more than 1 ms, it is considered as adapter voltage returns back to normal voltage. CHRG_OK pin is pulled high by external pull up resistor. The converter resumes if enable conditions are valid. When ACOV is triggered, its corresponding status bit FAULT_ACOV will be set and it can be cleared by host read.

Under different input voltage 36V EPR/ 28V EPR/20V SPR/ 15V SPR, ACOV should be adjusted accordingly to meet converter MOSFETs protection requirement. ACOV_ADJ bits are used to adjust ACOV thresholds. By default charger ACOV protection is 33 V corresponding to 28V ERP application.

#### 7.3.26.3 Input Overcurrent Protection (ACOC)

If the input current exceeds the 1.33× or 2× of ILIM2_VTH set point ACOC_TH(adjustable through ACOC_VTH), after 250us rising edge deglitch time converter stops switching because of input over current protection (ACOC). CHRG_OK pin will be pulled low by the charger when it is triggered. ACOC is a non-latch fault, if input current falls below set point, after 250 ms falling edge deglitch time converter starts switching again and CHRG_OK pin pull down will be released. ACOC is disabled by default and need to be enabled by configuring EN_ACOC=1b. When ACOC is triggered, its corresponding status bit FAULT_ACOC will be set and it can be cleared by host read.

#### 7.3.26.4 System Overvoltage Protection (SYSOVP)

When the converter starts up, the BQ25770G reads CELL_BATPRES pin configuration and sets CHARGE_VOLTAGE() and SYSOVP threshold ( 2s – 12 V, 3s – 17 V, 4s – 22 V and 5s – 27V ). Set SYSOVP_MAX=1b can force SYSOVP threshold to be maximum 27V neglecting CELL_BATPRES pin setting. Before CHARGE_VOLTAGE() is written by the host, the battery configuration will follow CELL_BATPRES pin setting. When SYSOVP happens, the device shuts off the converter. FAULT_SYSOVP status bit is set to 1 and latched to 1b. CHRG_OK pin is latched low accordingly until host clear the status bit. The user can clear this status latch-off by either writing 0 to the FAULT_SYSOVP status bit or removing and plugging in the adapter again. After latch-off is cleared, the converter starts again.

During buck HS MOSFET short, SYSOVP is the critical protection to prevent next stage VR power stage from high input voltage. This is implemented through CHRG_OK pin pull down to cut off input source after SYSOVP triggered.

#### 7.3.26.5 Battery Overvoltage Protection (BATOVP)

Battery overvoltage protection (BATOVP) can be enabled when battery is plugged in and charge is enabled in forward mode. In battery only OTG mode and charge disable forward operation this fault is neglected. The BATOVP rising threshold is 108% of regulation voltage set in CHARGE_VOLTAGE() register, and falling threshold is 106% of regulation voltage set in CHARGE_VOLTAGE() register. BATOVP protection is a non-latch fault and it is enabled by default (EN_BATOVP=1b), when BATOVP rising condition is triggered: if charge is enabled converter should shut down and CHRG_OK pin is pulled down, the charger automatically recover switching after BATOVP comparator output falls; if charge is disabled this fault should be neglected, the converter should keep operating without disturbance and CHRG_OK pin is kept high. There is dedicated user status bit FAULT_BATOVP to monitor its status. Once triggered FAULT_BATOVP status bit will be set to 1b until host read to clear it. Note VBAT voltage used for BATOVP detection is based on SRN pin measurement. When BATOVP is triggered, 20-mA discharge current is added on VSYS pin to help discharge battery voltage. The 20-mA discharge current can be disabled by setting DIS_BATOVP_20MA=1b. BATOVP protection can be disabled through setting EN_BATOVP=0b.

#### 7.3.26.6 Battery Charge Overcurrent Protection (BATCOC)

The charger monitors the battery charge current to provide the battery overcurrent charge protection(BATCOC) through voltage across SRP and SRN. BATCOC is disabled by default (BATCOC_CONFIG=00b) and can be enabled by configuring BATCOC_CONFIG=01b/10b/11b (50mV/75mV/100mV thresholds respectively).

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When the charge current is higher than the threshold after 1-µs deglitch time, BATCOC fault is triggered, CHARGE_CURRENT() register is reset back to 0A and BATFET should be turned off accordingly. Status bit FAULT_BATCOC is set and it can only be cleared by host read after 1 second latch time. The above actions are only executed one time after triggered. During this 1 second latch time, non-zero value cannot be written into CHARGE_CURRENT(). In order to recover charging, host need to re-write non-zero CHARGE_CURRENT() register value after it triggers for 1 second. Note this protection only turns off BATFET to disable charge it should not influence BATFET supplement mode turn on state machine. Also the CHRG_OK pin is not influenced under BATCOC fault to avoid unnecessary interference to customer system.

#### *7.3.26.7 Battery Discharge Overcurrent Protection (BATDOC)*

Under battery only OTG operation, the charger monitors the battery discharge current to provide the battery over current protection (BATDOC) through voltage across SRN and SRP. BATDOC can be enabled by configuring EN_BATDOC=1b. BATDOC threshold is selected either 200% of IDCHG_TH2 or 300% IDCHG_TH2 through BATDOC_VTH bit. There is also fixed low and high clamp for BATDOC threshold. When 200% of IDCHG_TH2 or 300% IDCHG_TH2 corresponding SRN-SRP voltage is below 50 mV , then BATDOC threshold will be low clamped at SRN-SRP=50 mV corresponding current; similarly if 200% of IDCHG_TH2 or 300% IDCHG_TH2 corresponding SRN-SRP voltage is above 180 mV , then BATDOC threshold will be high clamped at SRN-SRP=180 mV corresponding current.

When discharge current is higher than the threshold after 250-µs deglitch time, BATDOC fault is triggered, status bit FAULT_BATDOC is set accordingly. Converter shuts down when BATDOC is asserted to disable OTG operation and reduce discharge current. BATFET status is not impacted if need to supplement power to system.

BATDOC is not a latch fault, therefore after BATDOC fault is removed, with 250 ms relax time, converter resume switching automatically. But status bit FAULT_BATDOC is only cleared by host read.

#### *7.3.26.8 BATFET Charge Current Clamp Protection under LDO Regulation Mode*

When charger LDO mode is enabled (EN_LDO=1b) and VBAT voltage falls below VSYS_MIN() during charging, the charger should regulate system output voltage fixed at VSYS_MIN() and battery charging current is regulated by BATFET gate voltage achieving LDO mode operation. Both charger pre-charge and trickle charge status are implemented through this LDO mode operation. Under both pre-charge and trickle charge there are corresponding current limit referring to Battery Charging Profile. Under LDO mode larger VSYS_MIN() minus VBAT delta and larger charge current should generate more thermal dissipation at BATFET which should be properly limited to ensure safe operation. Therefore besides pre-charge and trickle charge current clamp mentioned above, we have additional two levels current clamp to ensure the maximum BATFET dissipation loss below 2W based on the relationship between VBAT and VSYS_MIN() setting referring to Table 7-9. The lower current clamp will dominate the final maximum charge current limit considering IPRECHG() user register upper clamp, battery short trickle charge current clamp (128 mA) and two levels BATFET current clamp below.

**Table 7-9. BATFET Charge Current Clamp Under LDO Mode**

| NAME | VBAT VS VSYS_MIN() | MAXIMUM CHARGE CURRENT CLAMP |
|---|---|---|
| $I_{BATFET_CLAMP1}$ | 1V<VSYS_MIN()-VBAT<4V | 512 mA (Internal Clamp no impact on IPRECHG() register) |
| $I_{BATFET_CLAMP2}$ | 4V<VSYS_MIN()-VBAT | 128 mA (Internal Clamp no impact on IPRECHG() register) |

When charger LDO mode is disabled (EN_LDO=0b), then BATFET will be either fully on or fully off status. When charge is disabled the system voltage is regulated at 5 V (VBAT< 5 V) or VBAT+160 mV (VBAT>5 V); however when charge is enabled then VSYS will be regulated close to VBAT to implement target charging current and VSYS_MIN regulation is not effective.

#### *7.3.26.9 Sleep Comparator Protection Between VBUS and ACP_A (SC_VBUSACP)*

Under forward mode, it is allowed to add an optional PFET or efuse between VBUS and ACP_A pin which can help shut off converter when there is dead short on Q1_A or Q1_B. Since the turn on delay on PFETs and eFuse is not fixed, sleep comparator protection is employed to ensure PFETs or eFuse is turned on when converter starts up. This sleep comparator is enabled by default (EN_SC_VBUS_ACP=1b) and can be disabled through


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EN_SC_VBUS_ACP=0b. When it is enabled, charger monitors delta voltage between VBUS and ACP_A and triggers to shuts off converter if VBUS-ACP_A is larger than $V_{SC_VBUSACP_rising}$. It is non-latch fault and in order to resume switching VBUS-ACP_A has to be smaller than $V_{SC_VBUSACP_falling}$. The comparator deglitch time is $t_{SC_VBUSACP_DEG}$ for both rising trigger and falling return. After protection is triggered converter shuts off and FAULT_SC_VBUSACP bit is set accordingly and can be cleared by a host read, note CHRG_OK pin is not pulled down during this fault, because the CHRG_OK pin needs to be high to turn on PFET or eFuse.

#### *7.3.26.10 High Duty Buck Exit Comparator Protection (HDBCP)*

Under HIGH_DUTY_BUCK=1b configuration, in order to prevent reverse boosting operation when VBUS is unplugged or reduced lower than VSYS, a dedicated comparator will force converter to exit high duty buck mode by forcing HIGH_DUTY_BUCK=0b. If VSYS is higher than 97.5% of VBUS, after 15-µs deglitch time the charger force HIGH_DUTY_BUCK back to 0b. As long as the comparator is triggered the charger should prevent HIGH_DUTY_BUCK bit from being set to 1b. HDBCP is an non-latch protection, if VSYS drops below 97.5% of VBUS minus hysteresis (80 mV), after 15-µs deglitch time HIGH_DUTY_BUCK bit is released and can be written to 1b to enter high duty buck operation.

#### *7.3.26.11 REGN Power Good Protection (REGN_PG)*

There is a dedicated REGN power good protection to guarantee converter switching under preferred gate drive voltage range. When REGN voltage is below $V_{REGN_OK_FALL}$ or above $V_{REGN_OV_RISE}$, after 100-µs deglitch time FAULT_REGN status bit will be set from 0b to 1b, converter shuts off and CHRG_OK pin is pulled down to inform host. When REGN is re-qualified above $V_{REGN_OK_RISE}$ and below $V_{REGN_OV_FALL}$ for more than 100 µs, CHRG_OK pin should also be released and converter resume switching automatically. The FAULT_REGN status bit can be cleared after host read as long as the fault condition is removed.

#### *7.3.26.12 System Under Voltage Lockout (VSYS_UVP) and Hiccup Mode*

The charger VSYS_UVP is enabled by default (VSYS_UVP_ENZ=0b) and can be disabled by writing VSYS_UVP_ENZ=1b. This protection is mainly defined to protect converter from system short circuit under both startup and steady state process. VSYS pin is used to monitor the system voltage, system under voltage lockout threshold is configurable through VSYS_UVP register bits (2.4 V upon POR), there is 2-ms deglitch time and the IIN_DPM is clamped to 0.5 A (VBUS<14.4V)/0.3A(VBUS>14.4V) to limit short circuit current. Detail protection process is slightly different based on whether hiccup mode is enabled:

If hiccup mode is enabled VSYS_UVP_NO_HICCUP = 0b, after 2-ms deglitch time, the charger should shut down for 500 ms.The charger will restart for 10 ms if VSYS is still lower than 2.4 V, the charger should shut down again. This hiccup mode will be tried continuously, if the charger restart is failed for 7 times in 90 second, the charger will be latched off. FAULT_VSYS_UVP bit will be set to 1 to report a system short fault and CHRG_OK pin is pulled accordingly. The charger only can be enabled again by writing FAULT_VSYS_UVP bit to 0b, then CHRG_OK pin can be released. Note as long as system voltage is below VSYS_UVP threshold, then IIN_DPM is also internally clamped to 0.5 A (VBUS<14.4V)/0.3A(VBUS>14.4V) to limit short circuit.

If hiccup mode is disabled VSYS_UVP_NO_HICCUP = 1b. After 2-ms deglitch time, the charger should shut down and latched off. FAULT_VSYS_UVP bit will be set to 1 to report a system short fault and CHRG_OK pin is pulled accordingly. The charger only can be enabled again once the host writes FAULT_VSYS_UVP bit to 0b, then CHRG_OK pin can be released.

#### *7.3.26.13 OTG Mode Over Voltage Protection (OTG_OVP)*

While operating in reverse direction, the device monitors the VBUS voltage. When VBUS exceeds $V_{VBUS_OTG_OV}$ there is 20-mA discharge current flow through VBUS pin. After VBUS exceeds $V_{VBUS_OTG_OV}$ for 10-ms deglitch time, the device stops switching, and and clear EN_OTG bit to 0b and exit OTG mode. When the event is triggered, the FAULT_OTG_OVP read only bit is triggered and CHRG_OK pin is pulled low if OTG_ON_CHRGOK=1b. The FAULT_OTG_OVP bit can be cleared through EC host read. In order to re-start OTG mode, EC host has to re-enable OTG mode by setting EN_OTG bit to 1b.

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#### 7.3.26.14 OTG Mode Under Voltage Protection (OTG_UVP)

While operating in reverse direction, the device monitors the VBUS voltage. When VBUS falls below $V_{VBUS_OTG_UV}$ for 10-ms deglitch time due to overloading, the device stops switching and clear EN_OTG bit to 0b and exit OTG mode. When the event is triggered, the FAULT_OTG_UVP read only bit is triggered and CHRG_OK pin is pulled low if OTG_ON_CHRGOK=1b. The FAULT_OTG_UVP bit can be cleared through EC host read. In order to re-start OTG mode, EC host has to re-enable OTG mode by setting EN_OTG bit to 1b.

#### 7.3.26.15 Thermal Shutdown (TSHUT)

The WQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature reaches the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the REGN LDO is scaled down to 35 mA and stays on. TSHUT is non-latched fault, when the temperature falls below 135°C charge can be resumed with soft start.

When thermal shut down is triggered, TSHUT status bit will be triggered. This status bit keep triggered until host read to clear it. If TSHUT is still present during host read, then this bit will try to be cleared when host read but finally keep triggered because TSHUT still exists.

## 7.4 Device Functional Modes

### 7.4.1 Forward Mode

When input source is connected to VBUS, BQ25770G is in forward mode to regulate system and charge battery.

#### 7.4.1.1 System Voltage Regulation with Narrow VDC Architecture

The device employs Narrow VDC architecture (NVDC) with BATFET separating the system from the battery. The minimum system voltage is set by VSYS_MIN(). Even with a depleted battery, the system is regulated at VSYS_ MIN() setting. To prevent inrush current from input side, when there is an step up new value written into VSYS_MIN(), the device can support soft positive slew rate DAC transition at 6.25mV/us, 3.125mV/us and 1.5625mV/us with corresponding configuration at EN_VSYS_MIN_SOFT_SR bits. The soft slew rate feature is not effective on step down direction . By default EN_VSYS_MIN_SOFT_SR=0b, there is no soft transition control for both step up and step down direction.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at VSYS_MIN register value. As the battery voltage rises above the minimum system voltage, BATFET is fully on. When in charging or in supplement mode, the voltage difference between the system and battery is the $V_{DS}$ of the BATFET. System voltage is regulated 150 mV above battery voltage when BATFET is turned off (no charging or no supplement current).

#### 7.4.1.2 Battery Charging

The BQ25770G charges cell battery in trickle charge, pre-charge, constant current (CC), and constant voltage (CV) mode. Based on CELL_BATPREZ pin setting, the charger sets default battery voltage 4.2V/cell to CHARGE_VOLTAGE(). According to battery capacity, the host programs appropriate charge current to CHARGE_CURRENT() register. When battery is full or battery is not in good condition to charge, host terminates charge by setting CHRG_INHIBIT bit to 1b, or setting CHARGE_CURRENT() to zero.

### 7.4.2 USB On-The-Go Mode

The BQ25770G supports USB OTG functionality to deliver power from the battery to other portable devices through USB port (reverse mode). The OTG output voltage is compliant with USB PD specification, including 5 V~28V. The output current regulation is compliant with USB Type-C and PD specification, including 500 mA, 1.5 A, 3 A and 5 A etc.

Similar to forward operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.


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### 7.4.3 Pass Through Mode (PTM)-Patented Technology

The charger can be operated in the pass through mode (PTM) to improve efficiency. In PTM, the Buck and Boost high-side FETs (Q1 and Q4) are both turned on, while the Buck and Boost low-side FETs are both turned off. The input power is directly passed through the charger to the system. The switching losses of MOSFETs and the inductor core loss are saved. The charger quiescent current under PTM mode is also minimized (around 2.5 mA) to increase light load efficiency.

When programmable power supply (PPS) is used as input adapter, PTM mode can also be leveraged to achieve battery flash charge under battery fast charge period. By enabling flash charge, the charge efficiency can be further improved with even higher charging current. During pre-charge and termination period the charger can go back to buck-boost mode.

The charger can exit PTM to buck-boost operation and automatically return to PTM under certain protection scenarios (TI patent).

To prevent reverse boost back after adapter removal when charger is in PTM operation before removal. There is light load PTM auto exit feature which can be enabled by configuring PTM_EXIT_LIGHT_LOAD=1b.

Charger will be transition from normal Buck-Boost operation to PTM operation by setting EN_PTM = 1b; and will transition out of PTM mode with host control by setting EN_PTM =0b.

### 7.4.4 Learn Mode

When both VBUS and VBAT exist, setting EN_LEARN=1b to enable mode to allow device to shut off converter and discharge battery to support the system. In this way it can calibrates the battery gas gauge over a complete discharge/charge cycle. When the battery voltage is below battery depletion threshold, the EC host will set EN_LEARN bit back to 0b to switch the device back in forward mode. When device is under learn mode if CELL_BATPRES pin is pulled lower than $V_{CELL_BATPRES_FALL}$ for 1ms deglitch time, then device exits LEARN mode and reset EN_LEARN bit is set back to 0 automatically.

## 7.5 Programming

The charger supports battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Section 7.5.1.1. The SMBus address is 7 bits 09h (0001001b), for 8 bits SMBus commands the last bit is read(1b)/write(0b) bit. Therefore 8 bits SMBus address command is integrated as 0b0001001_X (0x12H for write/0x13H for read).. The ManufacturerID and DeviceID registers are assigned to identify the charger device. The ManufacturerID register command always returns 40h.

### 7.5.1 SMBus Interface

The device operates as a target, receives control inputs from the embedded controller host through the SMBus interface. The device uses a simplified subset of the commands documented in *System Management Bus Specification V1.1*, which can be downloaded from www.smbus.org. The device uses the SMBus read-word and write-word protocols (shown in Table 7-10 and Table 7-11) to communicate with the smart battery. The device performs only as a SMBus target device with address 0b0001001_X (0x12H for write/0x13H for read) and does not initiate communication on the bus. In addition, the device has two identification registers, a 16-bit device ID register (0xFFH) and a 16-bit manufacturer ID register (0xFEH).

SMBus communication starts when VBUS is above $V_{VBUS_UVLO}$ or VBAT is above $V_{VBAT_UVLO}$.

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors (10 kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the host signals a start condition, which is a high-to-low transition on SDA, while SCL is high. When the host has finished communicating, the host issues a stop condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. When timeout condition is met, for example start condition is active for more than 35ms and there is no stop condition triggered, then charger SMbus communication will automatically reset and communication lines are free for another transmission. Figure 7-12 and Figure 7-13 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the start and stop conditions. The SDA

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state changes only while SCL is low, except for the start and stop conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the device because either the host or the target acknowledges the receipt of the correct byte during the ninth clock cycle. The BQ25770G supports the charger commands listed in Table 7-10.


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### 7.5.1.1 SMBus Write-Word and Read-Word Protocols

**Table 7-10. Write-Word Format**

| S (1) (2) | Target ADDRESS(1) | W (1) (3) | ACK (4) (5) | COMMAND BYTE(1) | ACK (4) (5) | LOW DATA BYTE(1) | ACK (4) (5) | HIGH DATA BYTE(1) | ACK (4) (5) | P (1) (6) |
|---|---|---|---|---|---|---|---|---|---|---|
| | 7 bits | 1b | 1b | 8 bits | 1b | 8 bits | 1b | 8 bits | 1b | |
| | MSB LSB | 0 | 0 | MSB LSB | 0 | MSB LSB | 0 | MSB LSB | 0 | |

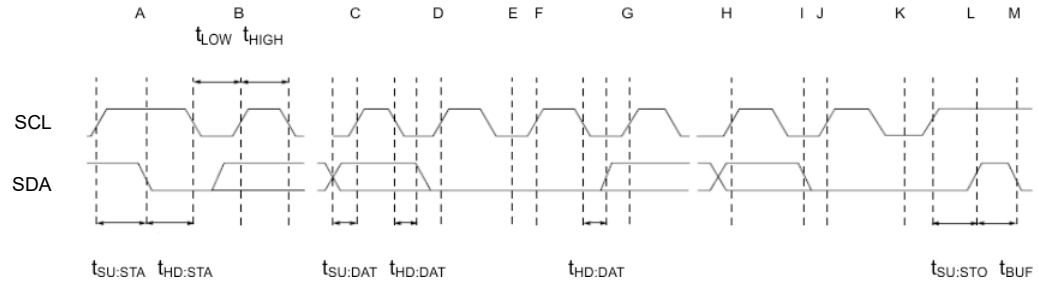
(1) Controller to target
(2) S = Start condition or repeated start condition
(3) W = Write bit (logic-low)
(4) Target to controller (shaded gray)
(5) ACK = Acknowledge (logic-low)
(6) P = Stop condition

**Table 7-11. Read-Word Format**

| S(1) (2) | Target ADDRESS(1) | W (1) (3) | ACK (4) (5) | COMMAND BYTE(1) | ACK (4) (5) | S(1) (2) | Target ADDRESS(1) | R(1) (6) | ACK (4) (5) | LOW DATA BYTE(4) | ACK (1) (5) | HIGH DATA BYTE(4) | NACK (1) (7) | P (1) (8) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 7 bits | 1b | 1b | 8 bits | 1b | | 7 bits | 1b | 1b | 8 bits | 1b | 8 bits | 1b | |
| | MSB LSB | 0 | 0 | MSB LSB | 0 | | MSB LSB | 1 | 0 | MSB LSB | 0 | MSB LSB | 1 | |

(1) Controller to target
(2) S = Start condition or repeated start condition
(3) W = Write bit (logic-low)
(4) Target to controller (shaded gray)
(5) ACK = Acknowledge (logic-low)
(6) R = Read bit (logic-high)
(7) NACK = Not acknowledge (logic-high)
(8) P = Stop condition

### 7.5.1.2 Timing Diagrams




A = Start condition
B = MSB of address clocked into target
C = LSB of address clocked into target
D = R/W bit clocked into target
E = Target pulls SMBDATA line low
F = ACKNOWLEDGE bit clocked into controller
G = MSB of data clocked into target
H = LSB of data clocked into target
I = Target pulls SMBDATA line low
J = Acknowledge clocked into controller
K = Acknowledge clock pulse
L = Stop condition, data executed by target
M = New start condition

**Figure 7-12. SMBus Write Timing**

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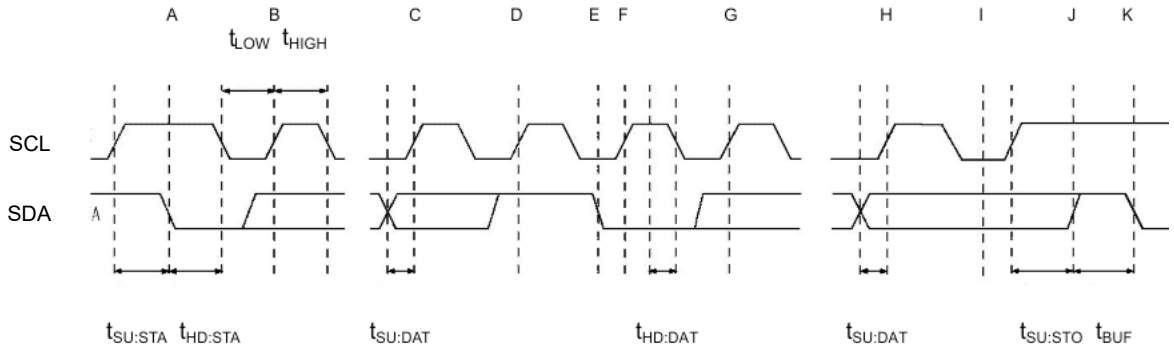


A = Start condition

B = MSB of address clocked into target

C = LSB of address clocked into target

D = R/W bit clocked into target

E = Target pulls SMBDATA line low

F = ACKNOWLEDGE bit clocked into controller

G = MSB of data clocked into controller

H = LSB of data clocked into controller

I = Acknowledge clock pulse

J = Stop condition

K = New start condition

**Figure 7-13. SMBus Read Timing**


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## 7.6 BQ25770G Registers

Table 7-12 lists the memory-mapped registers for the BQ25770G registers. All register offset addresses not listed in Table 7-12 should be considered as reserved locations and the register contents should not be modified.

**Table 7-12. BQ25770G Registers**

| Address | Acronym | Register Name | Section |
|---|---|---|---|
| 12h | REG0x12_ChargeOption0 | ChargeOption0() | Go |
| 14h | REG0x14_CHARGE_CURRENT | CHARGE_CURRENT() | Go |
| 15h | REG0x15_CHARGE_VOLTAGE | CHARGE_VOLTAGE() | Go |
| 17h | REG0x17_ChargeProfile | ChargeProfile() | Go |
| 18h | REG0x18_GateDrive | GateDrive() | Go |
| 19h | REG0x19_ChargeOption5 | ChargeOption5() | Go |
| 1Ah | REG0x1A_AutoCharge | AutoCharge() | Go |
| 1Bh | REG0x1B_ChargerStatus0 | ChargerStatus0() | Go |
| 20h | REG0x20_ChargerStatus1 | ChargerStatus1() | Go |
| 21h | REG0x21_Prochot_Status_Register | Prochot Status Register | Go |
| 22h | REG0x22_IIN_DPM | IIN_DPM() | Go |
| 23h | REG0x23_ADC_VBUS | ADC_VBUS() | Go |
| 24h | REG0x24_ADC_IBAT | ADC_IBAT() | Go |
| 25h | REG0x25_ADC_IIN | ADC_IIN() | Go |
| 26h | REG0x26_ADC_VSYS | ADC_VSYS() | Go |
| 27h | REG0x27_ADC_VBAT | ADC_VBAT() | Go |
| 28h | REG0x28_ADC_PSYS | ADC_PSYS() | Go |
| 29h | REG0x29_ADC_CMPIN_TR | ADC_CMPIN_TR() | Go |
| 30h | REG0x30_ChargeOption1 | ChargeOption1() | Go |
| 31h | REG0x31_ChargeOption2 | ChargeOption2() | Go |
| 32h | REG0x32_ChargeOption3 | ChargeOption3() | Go |
| 33h | REG0x33_ProchotOption0_Register | ProchotOption0 Register | Go |
| 34h | REG0x34_ProchotOption1 | ProchotOption1() | Go |
| 35h | REG0x35_ADCOption | ADCOption() | Go |
| 36h | REG0x36_ChargeOption4 | ChargeOption4() | Go |
| 37h | REG0x37_Vmin_Active_Protection | Vmin Active Protection() | Go |
| 3Bh | REG0x3B_OTG_VOLTAGE | OTG_VOLTAGE() | Go |
| 3Ch | REG0x3C_OTG_CURRENT | OTG_CURRENT() | Go |
| 3Dh | REG0x3D_VINDPM | VINDPM() | Go |
| 3Eh | REG0x3E_VSYS_MIN | VSYS_MIN() | Go |
| 3Fh | REG0x3F_IIN_HOST | IIN_HOST() | Go |
| 60h | REG0x60_AUTOTUNE_READ | AUTOTUNE_READ() | Go |
| 61h | REG0x61_AUTOTUNE_FORCE | AUTOTUNE_FORCE() | Go |
| 62h | REG0x62_GM_ADJUST_FORCE | GM_ADJUST_FORCE() | Go |
| FDh | REG0xFD_VIRTUAL_CONTROL | VIRTUAL_CONTROL() | Go |
| FEh | REG0xFE_Manufacture_ID | Manufacture ID | Go |
| FFh | REG0xFF_Device_ID | Device ID | Go |

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Complex bit access types are encoded to fit into small table cells. Table 7-13 shows the codes that are used for access types in this section.

**Table 7-13. BQ25770G Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |


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### 7.6.1 REG0x12_ChargeOption0 Register (Address = 12h) [Reset = E70Eh]

REG0x12_ChargeOption0 is shown in Figure 7-14 and described in Table 7-14.

Return to the Summary Table.

**Figure 7-14. REG0x12_ChargeOption0 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EN_LWPWR | WDTMR_ADJ | | IIN_DPM_AUTO_DISABLE | OTG_ON_CHRGOK | EN_OOA | PWM_FREQ | EN_BATOVP |
| R/W-1h | R/W-3h | | R/W-0h | R/W-0h | R/W-1h | R/W-1h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EN_CMP_LATCH | VSYS_UVP_ENZ | EN_LEARN | IADPT_GAIN | IBAT_GAIN | EN_LDO | EN_IIN_DPM | CHRG_INHIBIT |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-1h | R/W-1h | R/W-0h |

**Table 7-14. REG0x12_ChargeOption0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | EN_LWPWR | R/W | 1h | Reset by: REG_RESET | Low Power Mode enable<br>0b = Disable Low Power Mode. Device in performance mode with battery only. The PROCHOT, IADPT/IBAT/PSYS and comparator follow corresponding register setting, REGN should be on with full capacity.<br>1b = Enable Low Power Mode. Device in low power mode with battery only for lowest quiescent current. The PROCHOT, discharge current monitor buffer, power monitor buffer and independent comparator are disabled. ADC is not available in Low Power Mode. Independent comparator can be enabled by setting EN_LWPWR_CMP to 1b. REGN can be enabled through EN_REGN_LWPWR=1b with 5mA current capability to save quiescent current. |
| 14-13 | WDTMR_ADJ | R/W | 3h | Reset by: REG_RESET | WATCHDOG Timer Adjust<br>Set maximum delay between consecutive EC host write of charge voltage or charge current command. If device does not receive a write on the CHARGE_VOLTAGE() or the CHARGE_CURRENT() within the watchdog time period, the charger will be suspended by setting the CHARGE_CURRENT() to 0 mA. After expiration, the timer will resume upon the write of CHARGE_CURRENT(), CHARGE_VOLTAGE() ,WDTMR_ADJ or WD_RST=1b. The charger will resume if the values are valid.<br>00b = Disable<br>01b = 5 sec<br>10b = 88 sec<br>11b = 175 sec |
| 12 | IIN_DPM_AUTO_DISABLE | R/W | 0h | Reset by: REG_RESET | IIN_DPM Auto Disable<br>When CELL_BATPRES pin is LOW, the charger automatically disables the IIN_DPM function by setting EN_IIN_DPM to 0. The host can enable IIN_DPM function later by writing EN_IIN_DPM bit to 1.<br>0b = Disable<br>1b = Enable |

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**Table 7-14. REG0x12_ChargeOption0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 11 | OTG_ON_CHRGOK | R/W | 0h | Reset by:<br>REG_RESET | Add OTG to CHRG_OK<br>Drive CHRG_OK to HIGH when the device is in OTG mode.<br>0b = Disable<br>1b = Enable |
| 10 | EN_OOA | R/W | 1h | Reset by:<br>REG_RESET | Out-of-Audio Enable<br>0b = No Limit<br>1b = Set minimum PFM frequency above 20 kHz to avoid audio noise |
| 9 | PWM_FREQ | R/W | 1h | | Switching Frequency Selection: Recommend 600kHz with 2.2uH, 800 kHz with 1.5µH. After charger POR, the MODE pin programming process will make one time change on frequency selection.<br>Note: Frequency is not allowed to change on the fly has to be changed when converter is HIZ.<br>0b = 800kHz<br>1b = 600kHz |
| 8 | EN_BATOVP | R/W | 1h | Reset by:<br>REG_RESET | Enable BATOVP protection:<br>0b = Disable<br>1b = Enable |
| 7 | EN_CMP_LATCH | R/W | 0h | Reset by:<br>REG_RESET | Enable Latch of Independent Comparator. Comparator output with effective low. If enabled in PROCHOT profile PP_CMP=1b, STAT_COMP bit keep 1b after triggered until read by host and clear. host can clear CMPOUT pin by toggling this EN_CMP_LATCH bit<br>0b = No Latch<br>1b = Latch |
| 6 | VSYS_UVP_ENZ | R/W | 0h | Reset by:<br>REG_RESET | To disable system under voltage protection.<br>0b = Enable<br>1b = Disable |
| 5 | EN_LEARN | R/W | 0h | Reset by:<br>REG_RESET | LEARN mode function enable:<br>0b = Disable<br>1b = Enable |
| 4 | IADPT_GAIN | R/W | 0h | Reset by:<br>REG_RESET | IADPT Amplifier Ratio<br>The ratio of voltage on IADPT and voltage across ACP and ACN.<br>0b = 20x<br>1b = 40x |
| 3 | IBAT_GAIN | R/W | 1h | Reset by:<br>REG_RESET | IBAT Amplifier Ratio<br>The ratio of voltage on IBAT and voltage across SRP and SRN<br>0b = 8x<br>1b = 64x |
| 2 | EN_LDO | R/W | 1h | Reset by:<br>REG_RESET | LDO Mode Enable<br>When battery voltage is below VSYS_MIN(), the charger is in pre-charge with LDO mode enabled.<br>0b = Disable LDO mode, BATFET fully ON when charge is enabled and VSYS_MIN() regulation is not effective unless VBAT<5V and system is regulated at 5V. When charge is disabled, BATFET is fully off and system is regulated at VBAT+160mV.<br>1b = Enable LDO mode, Precharge current is set by the lower setting of CHARGE_CURRENT() and IPRECHG(). The system is regulated by the VSYS_MIN() register. |


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**Table 7-14. REG0x12_ChargeOption0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 1 | EN_IIN_DPM | R/W | 1h | Reset by:<br>REG_RESET | IIN_DPM Enable<br>Host writes this bit to enable IIN_DPM regulation loop. When the IIN_DPM is disabled<br>by the charger (refer to IIN_DPM_AUTO_DISABLE), this bit goes LOW. Under OTG mode, this bit is also used to enable/disable IOTG regulation.<br><br>0b = Disable<br>1b = Enable |
| 0 | CHRG_INHIBIT | R/W | 0h | Reset by:<br>REG_RESET | Charge Inhibit<br>When this bit is 0, battery charging will start with valid values in the<br>CHARGE_VOLTAGE() and CHARGE_CURRENT().<br><br>0b = Enable<br>1b = Inhibit |

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### 7.6.2 REG0x14_CHARGE_CURRENT Register (Address = 14h) [Reset = 0000h]

REG0x14_CHARGE_CURRENT is shown in Figure 7-15 and described in Table 7-15.

Return to the Summary Table.

**Figure 7-15. REG0x14_CHARGE_CURRENT Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CHARGE_CURRENT | | | | | |
| R-0h | | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHARGE_CURRENT | | | | | RESERVED | | |
| R/W-0h | | | | | R-0h | | |

**Table 7-15. REG0x14_CHARGE_CURRENT Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-14 | RESERVED | R | 0h | | Reserved |
| 13-3 | CHARGE_CURRENT | R/W | 0h | Reset by:<br>REG_RESET<br>WATCHDOG | Charge current setting with 5mΩ sense resistor (non-zero value lower than 128mA is treated as 128mA): Note when 2mΩ is chosen at RSNS_RSR=1b maximum charge current is clamped at 5DCh (30A with 20mA LSB). Under below scenarios CHARGE_CURRENT is reset to 0A:<br>1)BATCOC fault.<br>2)Charge Voltage() is written 0V<br>3)CELL_BATPRES going low(Battery removal)<br>4)STAT_AC is not valid(Adapter removal)<br>5)Watch dog event trigger<br>6) Autonomous charging get terminated (CHRG_STAT =111b)<br>7) Safety timer trigger<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br><br>POR: 0mA (0h)<br>Range: 0mA-16320mA (0h-7F8h)<br>Clamped High<br>Bit Step: 8mA |
| 2-0 | RESERVED | R | 0h | | Reserved |


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### 7.6.3 REG0x15_CHARGE_VOLTAGE Register (Address = 15h) [Reset = 0000h]

REG0x15_CHARGE_VOLTAGE is shown in Figure 7-16 and described in Table 7-16.

Return to the Summary Table.

**Figure 7-16. REG0x15_CHARGE_VOLTAGE Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | CHARGE_VOLTAGE | | | | | | |
| R-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHARGE_VOLTAGE | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

**Table 7-16. REG0x15_CHARGE_VOLTAGE Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | RESERVED | R | 0h | | Reserved |
| 14-2 | CHARGE_VOLTAGE | R/W | 0h | Write 0 to this register shall keep register value unchanged, and force CHARGE_CURRENT() to zero to disable charge.<br>Reset by:<br>REG_RESET | Charge voltage setting<br>Note: Writing non-zero value beyond clamp high/low will actually set register to the clamp high/low value. When 0V is written, it should not change CHARGE_VOLTAGE() but reset CHARGE_CURRENT() to 0A<br>POR: 0mV (0h)<br>Range: 5000mV-23000mV (4E2h-1676h)<br>Clamped Low<br>Clamped High<br>Bit Step: 4mV<br>Mode: 2s<br>8400mV<br>POR: 8400mV (834h)<br>Mode: 3s<br>12600mV<br>POR: 12600mV (C4Eh)<br>Mode: 4s<br>16800mV<br>POR: 16800mV (1068h)<br>Mode: 5s<br>21000mV<br>POR: 21000mV (1482h) |
| 1-0 | RESERVED | R | 0h | | Reserved |

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### 7.6.4 REG0x17_ChargeProfile Register (Address = 17h) [Reset = 3020h]

REG0x17_ChargeProfile is shown in Figure 7-17 and described in Table 7-17.

Return to the Summary Table.

**Figure 7-17. REG0x17_ChargeProfile Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| IPRECHG | | | | | | | |
| R/W-30h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ITERM | | | | | | | |
| R/W-20h | | | | | | | |

**Table 7-17. REG0x17_ChargeProfile Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-8 | IPRECHG | R/W | 30h | Reset by:<br>REG_RESET | Maximum precharge current clamp setting with 5mΩ sense resistor(The lower setting of CHARGE_CURRENT() and IPRECHG determine the practical precharge current when VBAT< VSYS_MIN()): Note when 2mΩ sense resistor is chosen RSNS_RSR=1b, then the IPRECHG() upper clamp should be 66H to limit BATFET thermal dissipation.<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br><br>POR: 384mA (30h)<br>Range: 128mA-2016mA (10h-FCh)<br>Clamped Low<br>Clamped High<br>Bit Step: 8mA |
| 7-0 | ITERM | R/W | 20h | Reset by:<br>REG_RESET | Termination current setting with 5mΩ sense resistor:<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br><br>POR: 256mA (20h)<br>Range: 128mA-2016mA (10h-FCh)<br>Clamped Low<br>Clamped High<br>Bit Step: 8mA |


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### 7.6.5 REG0x18_GateDrive Register (Address = 18h) [Reset = 246Ch]

REG0x18_GateDrive is shown in Figure 7-18 and described in Table 7-18.

Return to the Summary Table.

**Figure 7-18. REG0x18_GateDrive Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| HIDRV1_STAT | | | LODRV1_STAT | | | RESERVED | BATOVP_EXTEND |
| R/W-1h | | | R/W-1h | | | R-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HIDRV2_STAT | | | LODRV2_STAT | | | VSYS_REG_SLOW | RESERVED |
| R/W-3h | | | R/W-3h | | | R/W-0h | R-0h |

**Table 7-18. REG0x18_GateDrive Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-13 | HIDRV1_STAT | R/W | 1h | | HIDRV1_A and HIDRV1_B HS MOSFET gate drive strength adjustment for both turn on and turn off:<br>000b = Scale0 (Vgs=4.5V Qg range:0-5nC)<br>001b = Scale1(Vgs=4.5V Qg range:5-13nC )<br>010b = Scale2 (Vgs=4.5V Qg range:13-21nC )<br>011b = Scale3(Vgs=4.5V Qg range:21-29nC)<br>100b = Scale4 (Vgs=4.5V Qg range:29-37nC)<br>101b = Scale5(Vgs=4.5V Qg range:37-45nC)<br>110b = Scale6 (Vgs=4.5V Qg range:45-53nC)<br>111b = Scale7(Vgs=4.5V Qg range: >53nC) |
| 12-10 | LODRV1_STAT | R/W | 1h | | LODRV1_A and LODRV1_B LS MOSFET gate drive strength adjustment for both turn on and turn off:<br>000b = Scale0 (Vgs=4.5V Qg range:0-5nC)<br>001b = Scale1(Vgs=4.5V Qg range:5-13nC )<br>010b = Scale2 (Vgs=4.5V Qg range:13-21nC )<br>011b = Scale3(Vgs=4.5V Qg range:21-29nC)<br>100b = Scale4 (Vgs=4.5V Qg range:29-37nC)<br>101b = Scale5(Vgs=4.5V Qg range:37-45nC)<br>110b = Scale6 (Vgs=4.5V Qg range:45-53nC)<br>111b = Scale7(Vgs=4.5V Qg range: >53nC) |
| 9 | RESERVED | R | 0h | | Reserved |
| 8 | BATOVP_EXTEND | R/W | 0h | | Enable BATOVP for both charge enable and disable scenarios including AC+battery and battery only.<br>0b: BATOVP is only active when charge is enabled(BATFET is turned on) when EN_BATOVP=1b<br>1b: BATOVP is active as long as EN_BATOVP=1b, no matter charge is enabled or not(BATFET is on or off)<br>0b = Disable<br>1b = Enable |
| 7-5 | HIDRV2_STAT | R/W | 3h | | HIDRV2 HS MOSFET gate drive strength adjustment for both turn on and turn off:<br>000b = Scale0 (Vgs=4.5V Qg range:0-5nC)<br>001b = Scale1(Vgs=4.5V Qg range:5-13nC )<br>010b = Scale2 (Vgs=4.5V Qg range:13-21nC )<br>011b = Scale3(Vgs=4.5V Qg range:21-29nC)<br>100b = Scale4 (Vgs=4.5V Qg range:29-37nC)<br>101b = Scale5(Vgs=4.5V Qg range:37-45nC)<br>110b = Scale6 (Vgs=4.5V Qg range:45-53nC)<br>111b = Scale7(Vgs=4.5V Qg range: >53nC) |

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**Table 7-18. REG0x18_GateDrive Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 4-2 | LODRV2_STAT | R/W | 3h | | LODRV2 LS MOSFET gate drive strength adjustment for both turn on and turn off:<br><br>000b = Scale0 (Vgs=4.5V Qg range:0-5nC)<br>001b = Scale1(Vgs=4.5V Qg range:5-13nC )<br>010b = Scale2 (Vgs=4.5V Qg range:13-21nC )<br>011b = Scale3(Vgs=4.5V Qg range:21-29nC)<br>100b = Scale4 (Vgs=4.5V Qg range:29-37nC)<br>101b = Scale5(Vgs=4.5V Qg range:37-45nC)<br>110b = Scale6 (Vgs=4.5V Qg range:45-53nC)<br>111b = Scale7(Vgs=4.5V Qg range: >53nC) |
| 1 | VSYS_REG_SLOW | R/W | 0h | | System regulation loop bandwidth slow down to reduce input current overshoot during load transient:<br><br>0b = Disable<br>1b = Enable |
| 0 | RESERVED | R | 0h | | Reserved |


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### 7.6.6 REG0x19_ChargeOption5 Register (Address = 19h) [Reset = 0685h]

REG0x19_ChargeOption5 is shown in Figure 7-19 and described in Table 7-19.

Return to the Summary Table.

**Figure 7-19. REG0x19_ChargeOption5 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PTM_EXIT_LIGHT_LOAD | WD_RST | CMPIN_TR_SELECT | REGN_EXT | EN_REGN_LWPWR | BATCOC_CONFIG | | HIGH_DUTY_BUCK |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-3h | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SINGLE_DUAL_TRANS_TH | | | FORCE_SINGLE | PH_ADD_DEG | | PH_DROP_DEG | |
| R/W-4h | | | R/W-0h | R/W-1h | | R/W-1h | |

**Table 7-19. REG0x19_ChargeOption5 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | PTM_EXIT_LIGHT_LOAD | R/W | 0h | Reset by: REG_RESET | Enable PTM auto exit under light load:<br>0b = Disable<br>1b = Enable |
| 14 | WD_RST | R/W | 0h | Reset by: REG_RESET | Reset watch dog timer control:<br>0b = Normal<br>1b = Reset(bit goes back to 0 after timer reset) |
| 13 | CMPIN_TR_SELECT | R/W | 0h | Reset by: REG_RESET | CPMIN_TS pin function selection:<br>0b = CPMIN function<br>1b = TREG function |
| 12 | REGN_EXT | R/W | 0h | Reset by: REG_RESET | Enable external 5V overdrive for REGN:<br>0b = Disabled external 5V over drive<br>1b = Enable external 5V over drive |
| 11 | EN_REGN_LWPWR | R/W | 0h | Reset by: REG_RESET | Enable REGN with scale down current 5mA capability under battery only and low power mode:<br>0b = Disabled REGN under battery only low power mode<br>1b = Enable REGN under battery only low power mode |
| 10-9 | BATCOC_CONFIG | R/W | 3h | Reset by: REG_RESET | Disable BATCOC and configure BATCOC thresholds across SRP-SRN:<br>00b = Disable<br>01b = 50mV<br>10b = 75mV<br>11b = 100mV |
| 8 | HIGH_DUTY_BUCK | R/W | 0h | Reset by: REG_RESET | Enable high duty cycle buck mode to maximum buck mode operation range to keep Q4 constant on without boost switching.<br>0b = Disable<br>1b = Enable |

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**Table 7-19. REG0x19_ChargeOption5 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7-5 | SINGLE_DUAL_TRANS_TH | R/W | 4h | Reset by: REG_RESET | Buck mode single to dual phase transition threshold adjustment based on output load current: (When Quasi dual phase is chosen at MODE pin programming) Note from dual phase to single phase transition the load current threshold is 1A lower than this configuration as hysteresis.<br><br>000b = Force Dual Phase Operation<br>001b = 3A<br>010b = 4A<br>011b = 5A<br>100b = 6A<br>101b = 7A<br>110b = 8A<br>111b = 9A |
| 4 | FORCE_SINGLE | R/W | 0h | Reset by: REG_RESET | Force single phase operation under buck mode when quasi dual phase is chosen through MODE pin programming:<br><br>0b = Automatically transit to dual phase based on SINGLE_DUAL_TRANS_TH threshold option<br>1b = Force Single Phase under buck mode |
| 3-2 | PH_ADD_DEG | R/W | 1h | Reset by: REG_RESET | Adjust single phase to dual phase( phase adding transition) deglitch time:<br><br>00b = 0.727us(Min)/1.7us(Typ)/2.67us(Max)<br>01b = 2.91us(Min)/5.5us(Typ)/8us(Max)<br>10b = 11.6us(Min)/20us(Typ)/29.3us(Max)<br>11b = 46.6us(Min)/86us(Typ)/115us(Max) |
| 1-0 | PH_DROP_DEG | R/W | 1h | Reset by: REG_RESET | Adjust dual phase to single phase( phase dropping transition) deglitch time:<br><br>00b = 70us(Min)/93us(Typ)/115us(Max)<br>01b = 1.12ms(Min)/1.5ms(Typ)/1.82ms(Max)<br>10b = 8.94ms(Min)/11ms(Typ)/1.46ms(Max)<br>11b = 71.5ms(Min)/94ms(Typ)/117ms(Max) |


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### 7.6.7 REG0x1A_AutoCharge Register (Address = 1Ah) [Reset = 01C2h]

REG0x1A_AutoCharge is shown in Figure 7-20 and described in Table 7-20.

Return to the Summary Table.

**Figure 7-20. REG0x1A_AutoCharge Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EN_AUTO_CHG | CHRG_OK_INT | VRECHG | | | | CHG_TMR | |
| R/W-0h | R/W-0h | R/W-0h | | | | R/W-1h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EN_TMR2X | EN_CHG_TMR | EN_TREG | PP_THERMAL | STAT_THERMAL | THERMAL_DEG | ACOV_ADJ | |
| R/W-1h | R/W-1h | R/W-0h | R/W-0h | R-0h | R/W-0h | R/W-2h | |

**Table 7-20. REG0x1A_AutoCharge Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | EN_AUTO_CHG | R/W | 0h | Reset by: REG_RESET | Automatic charge control (recharge and terminate battery charging automatically):<br>0b = Disable<br>1b = Enable |
| 14 | CHRG_OK_INT | R/W | 0h | Reset by: REG_RESET | Enable CHRG_OK pin for interrupt function:<br>0b = Disable(CHRG_OK pin is not pulled low when CHRG_STAT bits changes)<br>1b = Enable(CHRG_OK pin is pulled low for minimum 256us when CHRG_STAT bits changes) |
| 13-10 | VRECHG | R/W | 0h | Reset by: REG_RESET | Battery automatic recharge threshold below CHARGE_VOLTAGE():<br>POR: 50mV (0h)<br>Range: 50mV-800mV (0h-Fh)<br>Bit Step: 50mV<br>Offset: 50mV<br>Mode: 2s<br>200mV<br>POR: 200mV (3h)<br>Mode: 3s<br>300mV<br>POR: 300mV (5h)<br>Mode: 4s<br>400mV<br>POR: 400mV (7h)<br>Mode: 5s<br>500mV<br>POR: 500mV (9h) |
| 9-8 | CHG_TMR | R/W | 1h | Reset by: REG_RESET | Automatic Charge Safety Timer control:<br>00b = 5hr<br>01b = 8hr<br>10b = 12hr<br>11b = 24hr |
| 7 | EN_TMR2X | R/W | 1h | Reset by: REG_RESET | Charge Safety Timer speed control: (Note changing the state of EN_TMR2X only impacts the rate at which the counter is counting and has no effect on any existing accumulated count)<br>0b = Timer always counts normally<br>1b = Timer slowed by 2x during VINDPM/IINDPM/ TREG regulation |

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**Table 7-20. REG0x1A_AutoCharge Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 6 | EN_CHG_TMR | R/W | 1h | Reset by:<br>REG_RESET<br>WATCHDOG | Enable charge safety timer:<br>0b = Disable<br>1b = Enable |
| 5 | EN_TREG | R/W | 0h | Reset by:<br>REG_RESET | Enable temperature regulation function and pull down CMPOUT pin to GND if CMPIN_TR_SELECT=1b. If CMPIN_TR_SELECT=0b, then EN_TREG will not be effective.<br>0b = Disable temperature regulation function<br>1b = Enable temperature regulation function |
| 4 | PP_THERMAL | R/W | 0h | Reset by:<br>REG_RESET | Enable temperature regulation(TREG) for PROCHOT profile.<br>0b = Disable<br>1b = Enable |
| 3 | STAT_THERMAL | R | 0h | Reset by:<br>REG_RESET | PROCHOT profile status bit for TREG thermal overheat (CMPIN_TR< 1.1V). The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 2 | THERMAL_DEG | R/W | 0h | Reset by:<br>REG_RESET | Adjust TREG thermal deglitch time to trigger prochot profile pull down pulse.<br>0b = 0.76sec(min)/0.965sec(Typ.)/1.17sec(max)<br>1b = 95.3ms(min)/121ms(Typ.)/146ms(max) |
| 1-0 | ACOV_ADJ | R/W | 2h | Reset by:<br>REG_RESET | ACOV protection threshold adjustment:<br>00b = 20V(15V SPR)<br>01b = 25V(20V SPR )<br>10b = 33V(28V EPR )<br>11b = 41V(36V EPR) |


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### 7.6.8 REG0x1B_ChargerStatus0 Register (Address = 1Bh) [Reset = 0000h]

REG0x1B_ChargerStatus0 is shown in Figure 7-21 and described in Table 7-21.

Return to the Summary Table.

ChargeStatus0()

**Figure 7-21. REG0x1B_ChargerStatus0 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CHRG_STAT | | | CHG_TMR_STAT | TREG_STAT | MODE_STAT | | |
| R-0h | | | R-0h | R-0h | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FAULT_BATOVP | RESERVED | FAULT_OCP | RESERVED | FAULT_REGN | RESERVED | | |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | | |

**Table 7-21. REG0x1B_ChargerStatus0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-13 | CHRG_STAT | R | 0h | | Charge Cycle Status<br>000b = Not Charging<br>001b = Trickle Charge (VBAT<VBAT_SHORT)<br>010b = Pre-Charge (VBAT<VSYS_MIN)<br>011b = Fast Charge(CC mode)<br>100b = Fast Charge(CV mode)<br>101b = Reserve1<br>110b = Reserve2<br>111b = Charge Termination Done |
| 12 | CHG_TMR_STAT | R | 0h | Reset by:<br>REG_RESET | Charge safety timer status<br>0b = Normal<br>1b = Charge safety timer expired |
| 11 | TREG_STAT | R | 0h | Reset by:<br>REG_RESET | Temperature regulation status<br>0b = Not in temperature regulation(TREG)<br>1b = In temperature regulation(TREG) |
| 10-8 | MODE_STAT | R | 0h | | MODE pin program status<br>000b = Quasi Dual Phase/Normal Compensation/ Fsw-600kHz<br>001b = Quasi Dual Phase/Normal Compensation/ Fsw-800kHz<br>010b = Quasi Dual Phase/Slow Compensation/ Fsw-600kHz<br>011b = Quasi Dual Phase/Slow Compensation/ Fsw-800kHz<br>100b = NA/Normal Compensation/Fsw-600kHz<br>101b = NA/Normal Compensation/Fsw-800kHz<br>110b = NA/Slow Compensation/Fsw-600kHz<br>111b = NA/Slow Compensation/Fsw-800kHz |
| 7 | FAULT_BATOVP | R | 0h | Reset by:<br>REG_RESET | The status are latched until a read from host, , if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br>0b = No Fault<br>1b = Fault |
| 6 | RESERVED | R | 0h | | Reserved |

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**Table 7-21. REG0x1B_ChargerStatus0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 5 | FAULT_OCP | R | 0h | Reset by:<br>REG_RESET | The status are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared.<br>0b = No Fault<br>1b = Fault |
| 4 | RESERVED | R | 0h | | Reserved |
| 3 | FAULT_REGN | R | 0h | Reset by:<br>REG_RESET | The status are latched until a read from host, , if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br>0b = No Fault<br>1b = Fault |
| 2-0 | RESERVED | R | 0h | | Reserved |


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### 7.6.9 REG0x20_ChargerStatus1 Register (Address = 20h) [Reset = 0000h]

REG0x20_ChargerStatus1 is shown in Figure 7-22 and described in Table 7-22.

Return to the Summary Table.

**Figure 7-22. REG0x20_ChargerStatus1 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| STAT_AC | ICO_DONE | IN_VAP | IN_VINDPM | IN_IIN_DPM | FAULT_SC_VBUSACP | FAULT_BATCOC | IN_OTG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FAULT_ACOV | FAULT_BATDOC | FAULT_ACOC | FAULT_SYSOVP | FAULT_VSYS_UVP | FAULT_FRC_CONV_OFF | FAULT_OTG_OVP | FAULT_OTG_UVP |
| R-0h | R-0h | R-0h | R/W-0h | R/W-0h | R-0h | R-0h | R-0h |

**Table 7-22. REG0x20_ChargerStatus1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | STAT_AC | R | 0h | Reset by: REG_RESET | Input source status, STAT_AC is active as long as valid VBUS source exist<br>0b = Not Present<br>1b = Present |
| 14 | ICO_DONE | R | 0h | Reset by: REG_RESET | After the ICO routine is successfully executed, the bit goes 1.<br>0b = Not Complete<br>1b = Complete |
| 13 | IN_VAP | R | 0h | Reset by: REG_RESET | Digital status bit indicates VAP has been enabled(1) or disabled(0). The enable of VAP mode only follows the host command, which is not blocked by any status of /PROCHOT. The exit of VAP mode also follows the host command, except that any faults will exit VAP mode automatically. STAT_EXIT_VAP becomes 1 which will pull low /PROCHOT until host clear.<br>The host can enable VAP by setting EN_OTG pin high and OTG_VAP_MODE=0b, disable VAP by setting either EN_OTG pin low or OTG_VAP_MOD=1b.<br>When IN_VAP bit goes 0->1, charger should disable VinDPM, IIN_DPM, ILIM pin, disable PP_ACOK if it is enabled, enable PP_VSYS if it is disabled. When IN_VAP bit goes 1->0, charger should enable VinDPM, IIN_DPM, ILIM pin<br>0b = Not Operated<br>1b = Operated |
| 12 | IN_VINDPM | R | 0h | Reset by: REG_RESET | VINDPM/ VOTG Status<br>0b = Charger is not in VINDPM during forward mode, or voltage regulation during OTG mode<br>1b = Charger is in VINDPM during forward mode, or voltage regulation during OTG mode |
| 11 | IN_IIN_DPM | R | 0h | Reset by: REG_RESET | IIN_DPM / IOTG Status<br>0b = Not In IIN_DPM<br>1b = In IIN_DPM |

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**Table 7-22. REG0x20_ChargerStatus1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 10 | FAULT_SC_VBUSACP | R | 0h | Reset by:<br>REG_RESET | The faults are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br><br>0b = No Fault<br>1b = Fault |
| 9 | FAULT_BATCOC | R | 0h | Reset by:<br>REG_RESET | The faults are latched until a read from host after 1 second after triggering. To recover charge, EC also need to re-write non zero value into CHARGE_CURRENT() register.<br><br>0b = No Fault<br>1b = Fault |
| 8 | IN_OTG | R | 0h | Reset by:<br>REG_RESET | OTG<br><br>0b = Not In OTG<br>1b = In OTG |
| 7 | FAULT_ACOV | R | 0h | Reset by:<br>REG_RESET | The faults are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br><br>0b = No Fault<br>1b = Fault |
| 6 | FAULT_BATDOC | R | 0h | Reset by:<br>REG_RESET | The faults are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br><br>0b = No Fault<br>1b = Fault |
| 5 | FAULT_ACOC | R | 0h | Reset by:<br>REG_RESET | The faults are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br><br>0b = No Fault<br>1b = Fault |
| 4 | FAULT_SYSOVP | R/W | 0h | Reset by:<br>REG_RESET | SYSOVP fault status and Clear<br>When the SYSOVP occurs, this bit is set HIGH. As long as this bit is high, the converter is disabled. After the SYSOVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the SYSOVP condition to enable the converter again.<br><br>0b = No Fault<br>1b = Fault |
| 3 | FAULT_VSYS_UVP | R/W | 0h | Reset by:<br>REG_RESET | VSYS_UVP fault status and clear. It is latched until a clear from host by writing this bit to 0.<br>As long as this bit is high, the converter is disabled. After the VSYS_UVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the VSYS_UVP condition to enable the converter again.<br><br>0b = No Fault<br>1b = Fault |


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**Table 7-22. REG0x20_ChargerStatus1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 2 | FAULT_FRC_CONV_OFF | R | 0h | Reset by:<br>REG_RESET | Force converter off when independent comparator is triggered low effective. The faults are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br><br>0b = No Fault<br>1b = Fault |
| 1 | FAULT_OTG_OVP | R | 0h | Reset by:<br>REG_RESET | The faults are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way hos<br><br>0b = No Fault<br>1b = Fault |
| 0 | FAULT_OTG_UVP | R | 0h | Reset by:<br>REG_RESET | The faults are latched until a read from host, if the fault still exist during host read this bit should be kept at 1b. However after host read fault status one time, this bit will be automatically reset when the original fault is cleared. In this way host doesn't need to read again to clear this fault bit after fault is removed.<br><br>0b = No Fault<br>1b = Fault |

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### 7.6.10 REG0x21_Prochot_Status_Register (Address = 21h) [Reset = 3800h]

REG0x21_Prochot_Status_Register is shown in Figure 7-23 and described in Table 7-23.

Return to the Summary Table.

**Figure 7-23. REG0x21_Prochot_Status_Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | EN_PROCHOT_EXT | PROCHOT_WIDTH | | PROCHOT_CLEAR | TSHUT | STAT_VAP_FAIL | STAT_EXIT_VAP |
| R-0h | R/W-0h | R/W-3h | | R/W-1h | R-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STAT_VINDPM | STAT_COMP | STAT_ICRIT | STAT_INOM | STAT_IDCHG1 | STAT_VSYS | STAT_BATTERY_REMOVAL | STAT_ADAPTER_REMOVAL |
| R/W-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

**Table 7-23. REG0x21_Prochot_Status_Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | RESERVED | R | 0h | | Reserved |
| 14 | EN_PROCHOT_EXT | R/W | 0h | Reset by: REG_RESET | PROCHOT Pulse Extension Enable. When pulse extension is enabled, keep the PROCHOT pin voltage LOW until host writes PROCHOT_CLEAR= 0b.<br>0b = Disable<br>1b = Enable |
| 13-12 | PROCHOT_WIDTH | R/W | 3h | Reset by: REG_RESET | PROCHOT Pulse Width when EN_PROCHOT_EXT = 0b<br>00b = 83ms(min)/100ms(Typ.)/117ms(max)<br>01b = 42ms(min)/50ms(Typ.)/58ms(max)<br>10b = 5ms(min)/6.15ms(Typ.)/7.3ms(max)<br>11b = 10ms(min)/12.5ms(Typ.)/15ms(max) |
| 11 | PROCHOT_CLEAR | R/W | 1h | Reset by: REG_RESET | PROCHOT Pulse Clear.<br>Clear PROCHOT pulse when EN_PROCHOT_EXT=0b.<br>0b = Clear PROCHOT pulse and drive /PROCHOT pin HIGH<br>1b = Idle |
| 10 | TSHUT | R | 0h | Reset by: REG_RESET | TSHUT trigger<br>0b = Not Triggered<br>1b = Triggered |
| 9 | STAT_VAP_FAIL | R/W | 0h | Reset by: REG_RESET | This status bit reports a failure to load VBUS 7 consecutive times in VAP mode, which indicates the battery voltage might be not high enough to enter VAP mode, or the VAP loading current settings are too high.<br>0b = Not is VAP failure<br>1b = In VAP failure, the charger exits VAP mode, and latches off until the host writes this bit to 0. |
| 8 | STAT_EXIT_VAP | R/W | 0h | Reset by: REG_RESET | When the charger is operated in VAP mode, it can exit VAP by either being disabled through host, or there is any charger faults.<br>0b = PROCHOT_EXIT_VAP is not active<br>1b = PROCHOT_EXIT_VAP is active, PROCHOT pin is low until host writes this status bit to 0 |
| 7 | STAT_VINDPM | R/W | 0h | Reset by: REG_RESET | PROCHOT Profile VINDPM status bit, once triggered 1b, PROCHOT pin is low until host writes this status bit to 0b when PP_VINDPM = 1b.<br>0b = Not Triggered<br>1b = Triggered |


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**Table 7-23. REG0x21_Prochot_Status_Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 6 | STAT_COMP | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 5 | STAT_ICRIT | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 4 | STAT_INOM | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 3 | STAT_IDCHG1 | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 2 | STAT_VSYS | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 1 | STAT_BATTERY_REMOVAL | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 0 | STAT_ADAPTER_REMOVAL | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |

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### 7.6.11 REG0x22_IIN_DPM Register (Address = 22h) [Reset = 0320h]

REG0x22_IIN_DPM is shown in Figure 7-24 and described in Table 7-24.

Return to the Summary Table.

**Figure 7-24. REG0x22_IIN_DPM Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | IIN_DPM | |
| R-0h | | | | | | R-C8h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IIN_DPM | | | | | | RESERVED | |
| R-C8h | | | | | | R-0h | |

**Table 7-24. REG0x22_IIN_DPM Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-11 | RESERVED | R | 0h | | Reserved |
| 10-2 | IIN_DPM | R | C8h | Reset by:<br>REG_RESET | Input current setting with 10mΩ sense resistor:<br>POR: 5000mA (C8h)<br>Range: 400mA-8200mA (10h-148h)<br>Clamped Low<br>Clamped High<br>Bit Step: 25mA |
| 1-0 | RESERVED | R | 0h | | Reserved |


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### 7.6.12 REG0x23_ADC_VBUS Register (Address = 23h) [Reset = 0000h]

REG0x23_ADC_VBUS is shown in Figure 7-25 and described in Table 7-25.

Return to the Summary Table.

**Figure 7-25. REG0x23_ADC_VBUS Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_VBUS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_VBUS | | | | | | | |
| R-0h | | | | | | | |

**Table 7-25. REG0x23_ADC_VBUS Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-0 | ADC_VBUS | R | 0h | Reset by:<br>REG_RESET | VBUS ADC reading:<br>(Note: When VBUS plugged in before converter starts up , VBUS ADC channel should execute one time to read the no-load VBUS voltage and save the value into ADC_VBUS())<br>POR: 0mV (0h)<br>Format: 2s Complement<br>Range: 0mV-65534mV (0h-7FFFh)<br>Clamped Low<br>Bit Step: 2mV |

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### 7.6.13 REG0x24_ADC_IBAT Register (Address = 24h) [Reset = 0000h]

REG0x24_ADC_IBAT is shown in Figure 7-26 and described in Table 7-26.

Return to the Summary Table.

**Figure 7-26. REG0x24_ADC_IBAT Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_IBAT | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_IBAT | | | | | | | |
| R-0h | | | | | | | |

**Table 7-26. REG0x24_ADC_IBAT Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-0 | ADC_IBAT | R | 0h | Reset by:<br>REG_RESET | IBAT ADC reading with 5mΩ sense resistor: Note the charger only measures discharging current (negative voltage) under battery only or OTG modes, and only measure charging current(positive voltage) when valid adapter is plugged in<br><br>POR: 0mA (0h)<br>Format: 2s Complement<br>Range: -32768mA-32767mA (8000h-7FFFh)<br>Bit Step: 1mA |


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### 7.6.14 REG0x25_ADC_IIN Register (Address = 25h) [Reset = 0000h]

REG0x25_ADC_IIN is shown in Figure 7-27 and described in Table 7-27.

Return to the Summary Table.

**Figure 7-27. REG0x25_ADC_IIN Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_IIN | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_IIN | | | | | | | |
| R-0h | | | | | | | |

**Table 7-27. REG0x25_ADC_IIN Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-0 | ADC_IIN | R | 0h | Reset by:<br>REG_RESET | IIN ADC reading with 10mΩ sense resistor: current flowing from the adapter to the converter (like in forward mode) is represented as positive and current flowing to the adapter (like in OTG mode) is negative.<br><br>POR: 0mA(0h)<br>Format: 2s Complement<br>Range: -16384mA - 16383.5mA (8000h-7FFFh)<br>Bit Step: 0.5mA |

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### 7.6.15 REG0x26_ADC_VSYS Register (Address = 26h) [Reset = 0000h]

REG0x26_ADC_VSYS is shown in Figure 7-28 and described in Table 7-28.

Return to the Summary Table.

**Figure 7-28. REG0x26_ADC_VSYS Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_VSYS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_VSYS | | | | | | | |
| R-0h | | | | | | | |

**Table 7-28. REG0x26_ADC_VSYS Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-0 | ADC_VSYS | R | 0h | Reset by:<br>REG_RESET | VSYS ADC reading:<br><br>POR: 0mV (0h)<br>Format: 2s Complement<br>Range: 0mV-65534mV (0h-7FFFh)<br>Clamped Low<br>Bit Step: 2mV |


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### 7.6.16 REG0x27_ADC_VBAT Register (Address = 27h) [Reset = 0000h]

REG0x27_ADC_VBAT is shown in Figure 7-29 and described in Table 7-29.

Return to the Summary Table.

**Figure 7-29. REG0x27_ADC_VBAT Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_VBAT | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_VBAT | | | | | | | |
| R-0h | | | | | | | |

**Table 7-29. REG0x27_ADC_VBAT Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-0 | ADC_VBAT | R | 0h | Reset by:<br>REG_RESET | VBAT ADC reading:<br><br>POR: 0mV (0h)<br>Format: 2s Complement<br>Range: 0mV-32767mV (0h-7FFFh)<br>Clamped Low<br>Bit Step: 1mV |

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### 7.6.17 REG0x28_ADC_PSYS Register (Address = 28h) [Reset = 0000h]

REG0x28_ADC_PSYS is shown in Figure 7-30 and described in Table 7-30.

Return to the Summary Table.

**Figure 7-30. REG0x28_ADC_PSYS Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_PSYS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_PSYS | | | | | | | |
| R-0h | | | | | | | |

**Table 7-30. REG0x28_ADC_PSYS Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-0 | ADC_PSYS | R | 0h | Clamp at 3.2V<br>Reset by:<br>REG_RESET | System Power PSYS ADC reading:<br>POR: 0mV (0h)<br>Range: 0mV-8191mV (0h-1FFFh)<br>Clamped High<br>Bit Step: 1mV |


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### 7.6.18 REG0x29_ADC_CMPIN_TR Register (Address = 29h) [Reset = 0000h]

REG0x29_ADC_CMPIN_TR is shown in Figure 7-31 and described in Table 7-31.

Return to the Summary Table.

**Figure 7-31. REG0x29_ADC_CMPIN_TR Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_CMPIN_TR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_CMPIN_TR | | | | | | | |
| R-0h | | | | | | | |

**Table 7-31. REG0x29_ADC_CMPIN_TR Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-0 | ADC_CMPIN_TR | R | 0h | Pin abs max = 5.5V<br>Reset by:<br>REG_RESET | CMPIN_TR pin voltage ADC reading:<br>POR: 0mV (0h)<br>Range: 0mV-8191mV (0h-1FFFh)<br>Clamped High<br>Bit Step: 1mV |

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### 7.6.19 REG0x30_ChargeOption1 Register (Address = 30h) [Reset = 3201h]

REG0x30_ChargeOption1 is shown in Figure 7-32 and described in Table 7-32.

Return to the Summary Table.

**Figure 7-32. REG0x30_ChargeOption1 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EN_IBAT | EN_LWPWR_CMP | PSYS_CONFIG | | RSNS_RAC | RSNS_RSR | PSYS_RATIO | EN_OTG_BIG_CAP |
| R/W-0h | R/W-0h | R/W-3h | | R/W-0h | R/W-0h | R/W-1h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SYSOVP_MAX | CMP_POL | CMP_DEG | | FRC_CONV_OFF | EN_PTM | EN_SHIP_DCHG | EN_SC_VBUSACP |
| R/W-0h | R/W-0h | R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-1h |

**Table 7-32. REG0x30_ChargeOption1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | EN_IBAT | R/W | 0h | Reset by:<br>REG_RESET | IBAT Enable<br>Enable the IBAT output buffer. In low power mode (EN_LWPWR=1b), IBAT<br>buffer is always disabled regardless of this bit value.<br>0b = Disable<br>1b = Enable |
| 14 | EN_LWPWR_CMP | R/W | 0h | Reset by:<br>REG_RESET | Independent Comparator Enable<br>Enable independent comparator under battery only low power mode(EN_LWPWR=1b)<br>0b = Disable<br>1b = Enable |
| 13-12 | PSYS_CONFIG | R/W | 3h | Reset by:<br>REG_RESET | PSYS Enable and Definition Register<br>Enable PSYS sensing circuit and output buffer (whole PSYS circuit). In low power mode (EN_LWPWR=1b), PSYS sensing and buffer are always disabled regardless of this bit value.<br>00b = PBUS+PBAT<br>01b = PBUS<br>10b = RESERVED<br>11b = OFF |
| 11 | RSNS_RAC | R/W | 0h | Reset by:<br>REG_RESET | Input sense resistor RAC.Not recommend change this value during IINDPM/IOTG regulation: Under adapter plugged in: make changes right after converter starts up with light loading and before charge is enabled.<br>With battery only : make changes before EN_OTG pin is pulled up.<br>0b = 10 mOhms<br>1b = 5 mOhms |
| 10 | RSNS_RSR | R/W | 0h | Reset by:<br>REG_RESET | Charge sense resistor RSR. Not recommend change this value during ICHG/IPRECHG/BATFET_CLAMP1/ BATFET_CLAMP2/BAT_SHORT regulation:<br>Under adapter plugged in: make changes right after converter starts up with light loading and before charge is enabled.<br>With battery only : make changes before EN_OTG pin is pulled up.<br>0b = 5 mOhms<br>1b = 2 mOhms |


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**Table 7-32. REG0x30_ChargeOption1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 9 | PSYS_RATIO | R/W | 1h | Reset by:<br>REG_RESET | PSYS Gain<br>Ratio of PSYS output current vs total input and battery power.<br>0b = 0p25uAperW<br>1b = 1p00uAperW |
| 8 | EN_OTG_BIG_CAP | R/W | 0h | Reset by:<br>REG_RESET | Enable OTG compensation for VBUS effective capacitance larger than<br>60uF<br>0b = Disable OTG large VBUS capacitance compensation(Recommended<br>for VBUS effective capacitance smaller than 60uF effective capacitance)<br>1b = Enable OTG large VBUS capacitance compensation(Recommended<br>for VBUS effective capacitance larger than 60uF effective capacitance) |
| 7 | SYSOVP_MAX | R/W | 0h | Reset by:<br>REG_RESET | Force SYSOVP protection threshold to 27V neglecting CELL_BATPRES pin configuration<br>0b = Disable<br>1b = Enable |
| 6 | CMP_POL | R/W | 0h | Reset by:<br>REG_RESET | Independent Comparator output Polarity<br>0b = When CMPIN_TR is above internal threshold, CMPOUT is LOW (internal<br>hysteresis)<br>1b = When CMPIN_TR is below internal threshold, CMPOUT is LOW (external<br>hysteresis) |
| 5-4 | CMP_DEG | R/W | 0h | Reset by:<br>REG_RESET | Independent comparator deglitch time, only applied to the falling edge of<br>CMPOUT (HIGH to LOW).<br>00b = 1us(Not in battery only low power mode)/ 40us(Battery only low power mode)<br>01b = 2.05ms~2.73ms<br>10b = 20.85ms~27.31ms<br>11b = 5.34s~6.99s |
| 3 | FRC_CONV_OFF | R/W | 0h | Reset by:<br>REG_RESET | Force Power Path Off<br>When independent comparator triggers, charger turns off Q1 and Q4 (same as<br>disable converter) so that the system is disconnected from the input source. At<br>the same time, CHRG_OK signal goes to LOW to notify the system. It should be effective during forward mode with AC plugged in or battery only performance mode. Both FRC_CONV_OFF and CMP_EN should be 1b to enable this feature. No need for EN_LWPWR, EN_LWPWR_CMP to be high which are employed under battery only low power mode.<br>0b = Disable<br>1b = Enable |
| 2 | EN_PTM | R/W | 0h | Reset by:<br>REG_RESET | PTM enable register bit, it will automatically reset to zero<br>0b = Disable<br>1b = Enable |

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**Table 7-32. REG0x30_ChargeOption1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 1 | EN_SHIP_DCHG | R/W | 0h | Reset by:<br>REG_RESET | Discharge SRN for Shipping Mode<br>Used to discharge SRN pin capacitor voltage which is necessary for battery gauge device shipping mode. When this bit is 1, discharge SRN pin down in 340 ms with around 20mA current flowing through VSYS pin. When 340 ms is over, this bit is reset to 0 automatically. If this bit is written to 0b by host before 340ms expires, VSYS pin should stop discharging immediately. After SRN is discharged to 0V the discharge current will shut off automatically in order to get rid of any negative voltage on SRN pin. Note if after 340ms SRN voltage is still not low enough for battery gauge device entering ship mode, the host may need to write this bit to 1b again to start a new 340ms discharge cycle.<br>0b = Disable<br>1b = Enable |
| 0 | EN_SC_VBUSACP | R/W | 1h | Reset by:<br>REG_RESET | SC_VBUSACP protection enable register bit<br>0b = Disable<br>1b = Enable |


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### 7.6.20 REG0x31_ChargeOption2 Register (Address = 31h) [Reset = 00B7h]

REG0x31_ChargeOption2 is shown in Figure 7-33 and described in Table 7-33.

Return to the Summary Table.

**Figure 7-33. REG0x31_ChargeOption2 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PKPWR_TOVLD_DEG | | EN_PKPWR_IIN_DPM | EN_PKPWR_VSYS | STAT_PKPWR_OVLD | STAT_PKPWR_RELAX | PKPWR_TMAX | |
| R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EN_EXTILIM | EN_ICHG_IDCHG | OCP_SW2_HIGH_RANGE | OCP_SW1X_HIGH_RANGE | EN_ACOC | ACOC_VTH | EN_BATDOC | BATDOC_VTH |
| R/W-1h | R/W-0h | R/W-1h | R/W-1h | R/W-0h | R/W-1h | R/W-1h | R/W-1h |

**Table 7-33. REG0x31_ChargeOption2 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-14 | PKPWR_TOVLD_DEG | R/W | 0h | Reset by: REG_RESET | Input Overload time in Peak Power Mode<br>00b = 1ms<br>01b = 2ms<br>10b = 5ms<br>11b = 10ms |
| 13 | EN_PKPWR_IIN_DPM | R/W | 0h | Reset by: REG_RESET | Enable Peak Power Mode triggered by input current overshoot. If EN_PKPWR_IIN_DPM and EN_PKPWR_VSYS are 0b, peak power mode is disabled. Upon adapter removal, this bits is reset to 0b.<br>0b = Disable<br>1b = Enable |
| 12 | EN_PKPWR_VSYS | R/W | 0h | Reset by: REG_RESET | Enable Peak Power Mode triggered by system voltage under-shoot. If EN_PKPWR_IIN_DPM and EN_PKPWR_VSYS are 0b, peak power mode is disabled. Upon adapter removal, this bits is reset to 0b.<br>0b = Disable<br>1b = Enable |
| 11 | STAT_PKPWR_OVLD | R/W | 0h | Reset by: REG_RESET | Indicator that the device is in overloading cycle. Write 0 to get out of overloading cycle.<br>0b = Not In Peak<br>1b = In Peak |
| 10 | STAT_PKPWR_RELAX | R/W | 0h | Reset by: REG_RESET | Indicator that the device is in relaxation cycle. Write 0 to get out of relaxation cycle.<br>0b = Not In Relaxation<br>1b = In Relaxation |
| 9-8 | PKPWR_TMAX | R/W | 0h | Reset by: REG_RESET | Peak power mode overload and relax cycle time.<br>00b = 20ms<br>01b = 40ms<br>10b = 80ms<br>11b = 1s |
| 7 | EN_EXTILIM | R/W | 1h | Reset by: REG_RESET | Enable ILIM_HIZ pin to set input current limit<br>0b = Disable(Input current limit is set by IIN_HOST())<br>1b = Enable(Input current limit is set by the lower value of ILIM_HIZ pin and IIN_HOST()) |

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**Table 7-33. REG0x31_ChargeOption2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 6 | EN_ICHG_IDCHG | R/W | 0h | Reset by:<br>REG_RESET | IBAT pin monitor selection for discharge current and charge current<br><br>0b = IBAT pin as Discharge Current<br>1b = IBAT pin as Charge Current |
| 5 | OCP_SW2_HIGH_RANGE | R/W | 1h | Reset by:<br>REG_RESET | Over current protection threshold by sensing Q4 Vds. When this fault is continuously triggered 1 switching cycle, converter will be latched off. To re-enable converter, need to toggle EN_HIZ bit from 0 to 1 and back to 0.<br><br>0b = 150mV<br>1b = 260mV |
| 4 | OCP_SW1X_HIGH_RANGE | R/W | 1h | Reset by:<br>REG_RESET | Over current protection threshold by sensing RAC resistor across voltage, When this fault is continuously triggered 1 switching cycle, converter will be latched off. To re-enable converter, need to toggle EN_HIZ bit from 0 to 1 and back to 0.<br><br>0b = 300 mV (150mV under VSYS_UVP) for Q1_A and Q1_B<br>1b = 450 mV (300mV under VSYS_UVP) for Q1_A and Q1_B |
| 3 | EN_ACOC | R/W | 0h | Reset by:<br>REG_RESET | ACOC Enable<br>Input overcurrent (ACOC) protection by sensing the voltage across ACP_A and ACN_A plus ACP_B and ACN_B. Upon ACOC (after 250-µs blank-out time), converter is disabled.<br><br>0b = Disable<br>1b = Enable |
| 2 | ACOC_VTH | R/W | 1h | Reset by:<br>REG_RESET | ACOC Limit<br>Set ACOC threshold as percentage of ILIM2_VTH with current sensed from RAC.<br><br>0b = 1.33<br>1b = 2 |
| 1 | EN_BATDOC | R/W | 1h | Reset by:<br>REG_RESET | BATDOC Enable<br>Battery discharge overcurrent (BATDOC) protection by sensing the voltage across SRN and SRP. Upon BATDOC, converter is disabled.<br><br>0b = Disable<br>1b = Enable |
| 0 | BATDOC_VTH | R/W | 1h | Reset by:<br>REG_RESET | Set battery discharge overcurrent threshold as percentage of<br>PROCHOT battery discharge current limit.<br><br>0b = 2<br>1b = 3 |


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### 7.6.21 REG0x32_ChargeOption3 Register (Address = 32h) [Reset = 0534h]

REG0x32_ChargeOption3 is shown in Figure 7-34 and described in Table 7-34.

Return to the Summary Table.

**Figure 7-34. REG0x32_ChargeOption3 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EN_HIZ | REG_RESET | DETECT_VINDPM | EN_OTG | EN_ICO_MODE | EN_PORT_CTRL | EN_VSYS_MIN_SOFT_SR | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-1h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BATFET_ENZ | RESERVED | OTG_VAP_MODE | IL_AVG | | CMP_EN | BATFETOFF_HIZ | PSYS_OTG_IDCHG |
| R/W-0h | R-0h | R/W-1h | R/W-2h | | R/W-1h | R/W-0h | R/W-0h |

**Table 7-34. REG0x32_ChargeOption3 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | EN_HIZ | R/W | 0h | Reset by:<br>REG_RESET | Device Hi-Z Mode Enable<br>When the charger is in Hi-Z mode, the device draws minimal quiescent current. With VBUS above UVLO. REGN LDO stays on, and system powers from battery.<br>0b = Disable<br>1b = Enable |
| 14 | REG_RESET | R/W | 0h | Reset by:<br>REG_RESET | Reset Registers<br>All the R/W and R registers go back to the default setting except: CHRG_STAT, MODE_STAT, HIDRV1_STAT, LODRV1_STAT, HIDRV2_STAT, LODRV2_STAT, PWM_FREQ<br>0b = Idle<br>1b = Reset |
| 13 | DETECT_VINDPM | R/W | 0h | Reset by:<br>REG_RESET | Set VINDPM threshold based on VBUS measurement result minus 1.28V, Converter is disabled to measure VBUS. After VBUS measurement is done, VINDPM() is written with value VBUS-1.28V. Then this bit goes back to 0 and converter starts.<br>0b = Idle<br>1b = Measure VIN, write VIN-1.28V to VINDPM |
| 12 | EN_OTG | R/W | 0h | Reset by:<br>REG_RESET<br>WATCHDOG | OTG Mode Enable<br>Enable device in OTG mode when EN_OTG pin is HIGH.<br>0b = Disable<br>1b = Enable |
| 11 | EN_ICO_MODE | R/W | 0h | Reset by:<br>REG_RESET | Enable ICO Algorithm<br>0b = Disable<br>1b = Enable |
| 10 | EN_PORT_CTRL | R/W | 1h | Reset by:<br>REG_RESET | Enable BATFET control for dual port application:<br>0b = Disable BATFET control by HIZ BATDRV pin<br>1b = Enable BATFET control by active BATDRV pin |
| 9-8 | EN_VSYS_MIN_SOFT_SR | R/W | 1h | Reset by:<br>REG_RESET | VSYS_MIN soft slew rate control for VSYS_MIN step up transition. Note for step down doesn't need the soft transition.<br>00b = Disable<br>01b = 6.25mV/us<br>10b = 3.125mV/us<br>11b = 1.5625mV/us |

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**Table 7-34. REG0x32_ChargeOption3 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | BATFET_ENZ | R/W | 0h | Reset by:<br>REG_RESET | Turn off BATFET under battery only low power mode. When not in low power mode like OTG or with AC plugged in, the bit configuration is neglected and not effective.<br>0b = Not force turn off BATFET<br>1b = Force turn off BATFET |
| 6 | RESERVED | R | 0h | | Reserved |
| 5 | OTG_VAP_MODE | R/W | 1h | Reset by:<br>REG_RESET | The selection of the external EN_OTG pin control.<br>0b = VAP Mode<br>1b = OTG Mode |
| 4-3 | IL_AVG | R/W | 2h | Reset by:<br>REG_RESET | 4 levels inductor average current clamp.<br>00b = 10A<br>01b = 18A<br>10b = 24A<br>11b = Disable(internal 30A limit) |
| 2 | CMP_EN | R/W | 1h | Reset by:<br>REG_RESET | Enable Independent Comparator with effective low.<br>0b = Disable<br>1b = Enable |
| 1 | BATFETOFF_HIZ | R/W | 0h | Reset by:<br>REG_RESET | Turn off BATFET during HIZ mode.<br>0b = On<br>1b = Off |
| 0 | PSYS_OTG_IDCHG | R/W | 0h | Reset by:<br>REG_RESET | PSYS definition during OTG mode.<br>0b = PSYS as battery discharge power minus OTG output power<br>1b = PSYS as battery discharge power only |


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### 7.6.22 REG0x33_ProchotOption0_Register (Address = 33h) [Reset = 4A39h]

REG0x33_ProchotOption0_Register is shown in Figure 7-35 and described in Table 7-35.

Return to the Summary Table.

**Figure 7-35. REG0x33_ProchotOption0_Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ILIM2_VTH | | | | | ICRIT_DEG | | PROCHOT_VINDPM_80_90 |
| R/W-9h | | | | | R/W-1h | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSYS_TH1 | | | | | | INOM_DEG | LOWER_PROCHOT_VINDPM |
| R/W-Eh | | | | | | R/W-0h | R/W-1h |

**Table 7-35. REG0x33_ProchotOption0_Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-11 | ILIM2_VTH | R/W | 9h | Add notes here to describe<br>Reset by:<br>REG_RESET | ILIM2 Threshold<br><br>00000b = OutOfRange_0x00<br>00001b = 110_percent<br>00010b = 115_percent<br>00011b = 120_percent<br>00100b = 125_percent<br>00101b = 130_percent<br>00110b = 135_percent<br>00111b = 140_percent<br>01000b = 145_percent<br>01001b = 150_percent<br>01010b = 155_percent<br>01011b = 160_percent<br>01100b = 165_percent<br>01101b = 170_percent<br>01110b = 175_percent<br>01111b = 180_percent<br>10000b = 185_percent<br>10001b = 190_percent<br>10010b = 195_percent<br>10011b = 200_percent<br>10100b = 205_percent<br>10101b = 210_percent<br>10110b = 215_percent<br>10111b = 220_percent<br>11000b = 225_percent<br>11001b = 230_percent<br>11010b = 250_percent<br>11011b = 300_percent<br>11100b = 350_percent<br>11101b = 400_percent<br>11110b = 450_percent<br>11111b = OutOfRange_0x1F |
| 10-9 | ICRIT_DEG | R/W | 1h | Reset by:<br>REG_RESET | ICRIT deglitch time to trigger PROCHOT<br><br>00b = 12us(Min)/14.5us(Typ.)/17us(Max)<br>01b = 93us(Min)/111us(Typ.)/129us(Max)<br>10b = 372us(Min)/443us(Typ.)/513us(Max)<br>11b = 745us(Min)/873us(Typ.)/1000us(Max) |
| 8 | PROCHOT_VINDPM_80_90 | R/W | 0h | Reset by:<br>REG_RESET | Lower threshold of the PROCHOT_VINDPM comparator.<br>When LOWER_PROCHOT_VINDPM=1, the threshold of PROCHOT_VINDPM is determined by this setting.<br><br>0b = 83% of VINDPM<br>1b = 91% of VINDPM |

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**Table 7-35. REG0x33_ProchotOption0_Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7-2 | VSYS_TH1 | R/W | Eh | Reset by:<br>REG_RESET | VSYS threshold to trigger discharging VBUS in VAP mode.<br><br>POR: 6400mV (Eh)<br>Range: 5000mV-11300mV (0h-3Fh)<br>Bit Step: 100mV<br>Offset: 5000mV |
| 1 | INOM_DEG | R/W | 0h | Reset by:<br>REG_RESET | INOM deglitch time<br><br>0b = 0.84ms (min)/0.988ms (typ.)/1.14ms (max)<br>1b = 54ms (min)/64ms (typ.)/73ms (max) |
| 0 | LOWER_PROCHOT_VINDPM | R/W | 1h | Reset by:<br>REG_RESET | Enable lower threshold of PROCHOT_VINDPM comparator:<br><br>0b = PROCHOT_VINDPM follows VINDPM REG0x3D setting<br>1b = PROCHOT_VINDPM is lowered and determined by PROCHOT_VINDPM_80_90 bit setting |


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### 7.6.23 REG0x34_ProchotOption1 Register (Address = 34h) [Reset = 41A0h]

REG0x34_ProchotOption1 is shown in Figure 7-36 and described in Table 7-36.

Return to the Summary Table.

**Figure 7-36. REG0x34_ProchotOption1 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| IDCHG_TH1 | | | | | | IDCHG_DEG1 | |
| R/W-10h | | | | | | R/W-1h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PP_VINDPM | PP_CMP | PP_ICRIT | PP_INOM | PP_IDCHG1 | PP_VSYS | PP_BATPRES | PP_ACOK |
| R/W-1h | R/W-0h | R/W-1h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7-36. REG0x34_ProchotOption1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-10 | IDCHG_TH1 | R/W | 10h | Reset by:<br>REG_RESET | IDCHG level 1 Threshold<br>6 bit, range, range 1500A to 33A(5mΩ RSR), step 500 mA. There is a 1500 mA offset for all code<br>Measure current between SRN and SRP.<br>Trigger when the discharge current is above the threshold.<br>If the value is programmed to 000000b PROCHOT is always triggered.<br>Default: 9500 mA or 010000b<br><br>POR: 9500mA (10h)<br>Range: 1500mA-33000mA (0h-3Fh)<br>Bit Step: 500mA<br>Offset: 1500mA |
| 9-8 | IDCHG_DEG1 | R/W | 1h | Reset by:<br>REG_RESET | IDCHG Deglitch Time<br><br>00b = 69ms(min)/78ms(Typ.)/93.6ms(max)<br>01b = 1.1sec(min)/1.25sec(Typ.)/1.4sec(max)<br>10b = 4.4sec(min)/5sec(Typ.)/5.6sec(max)<br>11b = 17.5sec(min)/20sec(Typ.)/22.3sec(max) |
| 7 | PP_VINDPM | R/W | 1h | Reset by:<br>REG_RESET | VINDPM PROCHOT profile enable<br><br>0b = Disable<br>1b = Enable |
| 6 | PP_CMP | R/W | 0h | Reset by:<br>REG_RESET | COMP PROCHOT profile enable<br><br>0b = Disable<br>1b = Enable |
| 5 | PP_ICRIT | R/W | 1h | Reset by:<br>REG_RESET | ICRIT PROCHOT profile enable<br><br>0b = Disable<br>1b = Enable |
| 4 | PP_INOM | R/W | 0h | Reset by:<br>REG_RESET | INOM PROCHOT profile enable<br><br>0b = Disable<br>1b = Enable |
| 3 | PP_IDCHG1 | R/W | 0h | Reset by:<br>REG_RESET | IDCHG1 PROCHOT profile enable<br><br>0b = Disable<br>1b = Enable |
| 2 | PP_VSYS | R/W | 0h | Reset by:<br>REG_RESET | VSYS PROCHOT profile enable<br><br>0b = Disable<br>1b = Enable |

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**Table 7-36. REG0x34_ProchotOption1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 1 | PP_BATPRES | R/W | 0h | Reset by:<br>REG_RESET | Battery removal PROCHOT profile enable<br>If PP_BATPRES is enabled in PROCHOT after the battery is removed, it will immediately send out one-shot PROCHOT pulse.<br>0b = Disable<br>1b = Enable |
| 0 | PP_ACOK | R/W | 0h | Reset by:<br>REG_RESET | Adapter removal PROCHOT profile enable.<br>If PP_ACOK is enabled in PROCHOT after the adapter is removed, it will be pulled low.<br>0b = Disable<br>1b = Enable |


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### 7.6.24 REG0x35_ADCOption Register (Address = 35h) [Reset = 9000h]

REG0x35_ADCOption is shown in Figure 7-37 and described in Table 7-37.

Return to the Summary Table.

**Figure 7-37. REG0x35_ADCOption Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADC_RATE | ADC_EN | ADC_SAMPLE | | ADC_AVG | ADC_AVG_INIT | RESERVED | |
| R/W-1h | R/W-0h | R/W-1h | | R/W-0h | R/W-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EN_ADC_CMPIN | EN_ADC_VBUS | EN_ADC_PSYS | EN_ADC_IIN | RESERVED | EN_ADC_IBAT | EN_ADC_VSYS | EN_ADC_VBAT |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7-37. REG0x35_ADCOption Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | ADC_RATE | R/W | 1h | Reset by:<br>REG_RESET | ADC conversion type selection<br>Typical conversion time is determined by resolution accuracy.<br>0b = Continuous update. Cycling set of conversion updates to ADC registers without break. The total period of whole set is determined by the ADC channel enabled count times conversion time for each channel determined by ADC_SAMPLE setting.<br>1b = One-shot update. Do one set of conversion updates to ADC registers after ADC_START =1. The total period of whole set is determined by the ADC channel enabled count times conversion time for each channel determined by ADC_SAMPLE setting. |
| 14 | ADC_EN | R/W | 0h | Reset by:<br>REG_RESET<br>WATCHDOG | ADC conversion enable command.<br>Under one-shot ADC configuration ADC_RATE=0b, After the one-shot update is complete, this bit automatically resets to zero<br>0b = Idle<br>1b = Start |
| 13-12 | ADC_SAMPLE | R/W | 1h | Reset by:<br>REG_RESET | ADC sample resolution selection, each channel conversion time is also determined based on resolution.<br>00b = 15 bits effective resolution(24ms conversion time per channel)<br>01b = 14 bits effective resolution(12ms conversion time per channel)<br>10b = 13 bits effective resolution(6ms conversion time per channel)<br>11b = Reserved |
| 11 | ADC_AVG | R/W | 0h | Reset by:<br>REG_RESET | ADC average control<br>0b = Single Value<br>1b = Running average |
| 10 | ADC_AVG_INIT | R/W | 0h | Reset by:<br>REG_RESET | ADC average initial value control<br>0b = Start average using existing register value<br>1b = Start average using new ADC conversion |
| 9-8 | RESERVED | R | 0h | | Reserved |
| 7 | EN_ADC_CMPIN | R/W | 0h | Reset by:<br>REG_RESET | Enable CMPIN_TR pin Voltage ADC Channel<br>0b = Disable<br>1b = Enable |

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**Table 7-37. REG0x35_ADCOption Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 6 | EN_ADC_VBUS | R/W | 0h | Reset by:<br>REG_RESET | Enable VBUS pin Voltage ADC Channel<br>0b = Disable<br>1b = Enable |
| 5 | EN_ADC_PSYS | R/W | 0h | Reset by:<br>REG_RESET | Enable PSYS pin Voltage ADC Channel<br>0b = Disable<br>1b = Enable |
| 4 | EN_ADC_IIN | R/W | 0h | Reset by:<br>REG_RESET | Enable IIN ADC Channel<br>0b = Disable<br>1b = Enable |
| 3 | RESERVED | R | 0h | | Reserved |
| 2 | EN_ADC_IBAT | R/W | 0h | Reset by:<br>REG_RESET | Enable ICHG ADC Channel<br>0b = Disable<br>1b = Enable |
| 1 | EN_ADC_VSYS | R/W | 0h | Reset by:<br>REG_RESET | Enable VSYS pin Voltage ADC Channel<br>0b = Disable<br>1b = Enable |
| 0 | EN_ADC_VBAT | R/W | 0h | Reset by:<br>REG_RESET | Enable SRN pin Voltage ADC Channel<br>0b = Disable<br>1b = Enable |


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### 7.6.25 REG0x36_ChargeOption4 Register (Address = 36h) [Reset = 0048h]

REG0x36_ChargeOption4 is shown in Figure 7-38 and described in Table 7-38.

Return to the Summary Table.

**Figure 7-38. REG0x36_ChargeOption4 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| VSYS_UVP | | | EN_DITHER | | VSYS_UVP_NO_HICCUP | PP_VBUS_VAP | STAT_VBUS_VAP |
| R/W-0h | | | R/W-0h | | R/W-0h | R/W-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IDCHG_DEG2 | | IDCHG_TH2 | | | PP_IDCHG2 | STAT_IDCHG2 | STAT_PTM |
| R/W-1h | | R/W-1h | | | R/W-0h | R-0h | R-0h |

**Table 7-38. REG0x36_ChargeOption4 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-13 | VSYS_UVP | R/W | 0h | Reset by: REG_RESET | VSYS Under Voltage Lock Out After UVP is triggered the charger enters hiccup mode, and then the charger is latched off if the restart fails 7 times in 90s The hiccup mode during the UVP can be disabled by setting VSYS_UVP_NO_HICCUP=1b.<br>000b = 2.4V<br>001b = 3.2V<br>010b = 4.0V<br>011b = 4.8V<br>100b = 5.6V<br>101b = 6.4V<br>110b = 7.2V<br>111b = 8.0V |
| 12-11 | EN_DITHER | R/W | 0h | Reset by: REG_RESET | Frequency Dither configuration<br>00b = Disable<br>01b = 1X<br>10b = 2X<br>11b = 3X |
| 10 | VSYS_UVP_NO_HICCUP | R/W | 0h | Reset by: REG_RESET | Disable VSYS_UVP Hiccup mode operation:<br>0b = Hiccup Mode Enabled<br>1b = Hiccup Mode Disabled |
| 9 | PP_VBUS_VAP | R/W | 0h | Reset by: REG_RESET | Enable VBUS_VAP PROCHOT Profile<br>0b = Disable<br>1b = Enable |
| 8 | STAT_VBUS_VAP | R | 0h | Reset by: REG_RESET | STAT_VBUS_VAP<br>0b = Not Triggered<br>1b = Triggered |
| 7-6 | IDCHG_DEG2 | R/W | 1h | Reset by: REG_RESET | Battery discharge current limit 2 deglitch time<br>00b = 81us(min)/98us(Typ.)/115us(max)<br>01b = 1.3ms(min)/1.55ms(Typ.)/1.8ms(max)<br>10b = 5.2ms(min)/6.25ms(Typ.)/7.3ms(max)<br>11b = 10.4ms(min)/12.5ms(Typ.)/14.6ms(max) |

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**Table 7-38. REG0x36_ChargeOption4 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 5-3 | IDCHG_TH2 | R/W | 1h | Reset by:<br>REG_RESET | Battery discharge current limit2 based on percentage of IDCHG_TH1. Note IDCHG_TH2 setting higher than 40A should lose accuracy derating between target value and 40A.<br>000b = 125%*IDCHG_TH1<br>001b = 150%*IDCHG_TH1<br>010b = 175%*IDCHG_TH1<br>011b = 200%*IDCHG_TH1<br>100b = 250%*IDCHG_TH1<br>101b = 300%*IDCHG_TH1<br>110b = 350%*IDCHG_TH1<br>111b = 400%*IDCHG_TH1 |
| 2 | PP_IDCHG2 | R/W | 0h | Reset by:<br>REG_RESET | Enable IDCHG_TH2 PROCHOT Profile<br>0b = Disable<br>1b = Enable |
| 1 | STAT_IDCHG2 | R | 0h | Reset by:<br>REG_RESET | The status is latched until a read from host.<br>0b = Not Triggered<br>1b = Triggered |
| 0 | STAT_PTM | R | 0h | Reset by:<br>REG_RESET | PTM operation status bit monitor<br>0b = Not Active<br>1b = Active |


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### 7.6.26 REG0x37_Vmin_Active_Protection Register (Address = 37h) [Reset = 0024h]

REG0x37_Vmin_Active_Protection is shown in Figure 7-39 and described in Table 7-39.

Return to the Summary Table.

**Figure 7-39. REG0x37_Vmin_Active_Protection Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| VBUS_VAP_TH | | | | | | | DIS_BATOVP_20MA |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSYS_TH2 | | | | | | EN_VSYSTH2_FOLLOW_VSYSTH1 | EN_FRS |
| R/W-9h | | | | | | R/W-0h | R/W-0h |

**Table 7-39. REG0x37_Vmin_Active_Protection Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-9 | VBUS_VAP_TH | R/W | 0h | Reset by: REG_RESET | VAP Mode2 VBUS /PROCHOT trigger voltage threshold<br>POR: 3200mV (0h)<br>Range: 3200mV-15900mV (0h-7Fh)<br>Bit Step: 100mV<br>Offset: 3200mV |
| 8 | DIS_BATOVP_20MA | R/W | 0h | Reset by: REG_RESET | Disable BATOVP 20mA discharge current through VSYS pin<br>0b = Discharge 20mA under BATOVP<br>1b = Not discharge 20mA under BATOVP |
| 7-2 | VSYS_TH2 | R/W | 9h | Reset by: REG_RESET | VAP Mode2 VBUS /PROCHOT trigger voltage threshold<br>POR: 5900mV (9h)<br>Range: 5000mV-11300mV (0h-3Fh)<br>Bit Step: 100mV<br>Offset: 5000mV |
| 1 | EN_VSYSTH2_FOLLOW_VSYSTH1 | R/W | 0h | Reset by: REG_RESET | Enable internal VSYS_TH2 follow VSYS_TH1 setting neglecting register VSYS_TH2 setting<br>0b = Disable<br>1b = Enable |
| 0 | EN_FRS | R/W | 0h | Reset by: REG_RESET | Fast Role Swap Feature Enable<br>0b = Disable<br>1b = Enable |

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### 7.6.27 REG0x3B_OTG_VOLTAGE Register (Address = 3Bh) [Reset = 03E8h]

REG0x3B_OTG_VOLTAGE is shown in Figure 7-40 and described in Table 7-40.

Return to the Summary Table.

**Figure 7-40. REG0x3B_OTG_VOLTAGE Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | OTG_VOLTAGE | | | | |
| R-0h | | | R/W-FAh | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTG_VOLTAGE | | | | | | RESERVED | |
| R/W-FAh | | | | | | R-0h | |

**Table 7-40. REG0x3B_OTG_VOLTAGE Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-13 | RESERVED | R | 0h | | Reserved |
| 12-2 | OTG_VOLTAGE | R/W | FAh | Reset by:<br>REG_RESET | OTG output voltage regulation:<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br>POR: 5000mV (FAh)<br>Range: 3000mV-5000mV (96h-FAh)<br>Clamped Low<br>Clamped High<br>Bit Step: 20mV |
| 1-0 | RESERVED | R | 0h | | Reserved |


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### 7.6.28 REG0x3C_OTG_CURRENT Register (Address = 3Ch) [Reset = 01E0h]

REG0x3C_OTG_CURRENT is shown in Figure 7-41 and described in Table 7-41.

Return to the Summary Table.

**Figure 7-41. REG0x3C_OTG_CURRENT Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | OTG_CURRENT | | |
| R-0h | | | | | R/W-78h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTG_CURRENT | | | | | | RESERVED | |
| R/W-78h | | | | | | R-0h | |

**Table 7-41. REG0x3C_OTG_CURRENT Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-11 | RESERVED | R | 0h | | Reserved |
| 10-2 | OTG_CURRENT | R/W | 78h | Reset by:<br>REG_RESET | OTG output current limit with 10mΩ Rac current sense:<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br>POR: 3000mA (78h)<br>Range: 100mA-3000mA (4h-78h)<br>Clamped Low<br>Clamped High<br>Bit Step: 25mA |
| 1-0 | RESERVED | R | 0h | | Reserved |

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### 7.6.29 REG0x3D_VINDPM Register (Address = 3Dh) [Reset = 0280h]

REG0x3D_VINDPM is shown in Figure 7-42 and described in Table 7-42.

Return to the Summary Table.

**Figure 7-42. REG0x3D_VINDPM Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | VINDPM | | | | |
| R-0h | | | R/W-A0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VINDPM | | | | | | RESERVED | |
| R/W-A0h | | | | | | R-0h | |

**Table 7-42. REG0x3D_VINDPM Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-13 | RESERVED | R | 0h | | Reserved |
| 12-2 | VINDPM | R/W | A0h | Reset by:<br>REG_RESET | Input voltage limit:<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br>POR: 3200mV (A0h)<br>Range: 3200mV-27000mV (A0h-546h)<br>Clamped Low<br>Clamped High<br>Bit Step: 20mV |
| 1-0 | RESERVED | R | 0h | | Reserved |


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### 7.6.30 REG0x3E_VSYS_MIN Register (Address = 3Eh) [Reset = 0528h]

REG0x3E_VSYS_MIN is shown in Figure 7-43 and described in Table 7-43.

Return to the Summary Table.

**Figure 7-43. REG0x3E_VSYS_MIN Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | VSYS_MIN | | | | |
| R-0h | | | R/W-528h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSYS_MIN | | | | | | | |
| R/W-528h | | | | | | | |

**Table 7-43. REG0x3E_VSYS_MIN Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-13 | RESERVED | R | 0h | | Reserved |
| 12-0 | VSYS_MIN | R/W | 528h | Reset by:<br>REG_RESET | Minimum system voltage configuration register<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br><br>POR: 6600mV (528h)<br>Range: 5000mV-21000mV (3E8h-1068h)<br>Clamped Low<br>Clamped High<br>Bit Step: 5mV<br>Mode: 2s<br>6600mV<br><br>Mode: 3s<br>9200mV<br>POR: 9200mV (730h)<br><br>Mode: 4s<br>12300mV<br>POR: 12300mV (99Ch)<br><br>Mode: 5s<br>15400mV<br>POR: 15400mV (C08h) |

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### 7.6.31 REG0x3F_IIN_HOST Register (Address = 3Fh) [Reset = 0320h]

REG0x3F_IIN_HOST is shown in Figure 7-44 and described in Table 7-44.

Return to the Summary Table.

**Figure 7-44. REG0x3F_IIN_HOST Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | IIN_HOST | |
| R-0h | | | | | | R/W-C8h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IIN_HOST | | | | | | RESERVED | |
| R/W-C8h | | | | | | R-0h | |

**Table 7-44. REG0x3F_IIN_HOST Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-11 | RESERVED | R | 0h | | Reserved |
| 10-2 | IIN_HOST | R/W | C8h | Reset by:<br>REG_RESET | Maximum input current limit with 10mΩ sense resistor:<br>Note: Writing value beyond clamp high/low will actually set register to the clamp high/low value .<br>POR: 5000mA (C8h)<br>Range: 400mA-8200mA (10h-148h)<br>Clamped Low<br>Clamped High<br>Bit Step: 25mA |
| 1-0 | RESERVED | R | 0h | | Reserved |


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### 7.6.32 REG0x60_AUTOTUNE_READ Register (Address = 60h) [Reset = 0000h]

REG0x60_AUTOTUNE_READ is shown in Figure 7-45 and described in Table 7-45.

Return to the Summary Table.

**Figure 7-45. REG0x60_AUTOTUNE_READ Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| AUTOTUNE_A | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUTOTUNE_B | | | | | | | |
| R-0h | | | | | | | |

**Table 7-45. REG0x60_AUTOTUNE_READ Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-8 | AUTOTUNE_A | R | 0h | | Phase A inductor time constant L(uH)/DCR(mΩ) value: AUTOTUNE_A= 256-265*L(uH)/DCR(mΩ). When converter shuts off these bits are set back to 0. |
| 7-0 | AUTOTUNE_B | R | 0h | | Phase B inductor time constant L(uH)/DCR(mΩ) value: AUTOTUNE_A= 256-265*L(uH)/DCR(mΩ). When converter shuts off these bits are set back to 0. |

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### 7.6.33 REG0x61_AUTOTUNE_FORCE Register (Address = 61h) [Reset = A8A8h]

REG0x61_AUTOTUNE_FORCE is shown in Figure 7-46 and described in Table 7-46.

Return to the Summary Table.

**Figure 7-46. REG0x61_AUTOTUNE_FORCE Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| FORCE_AUTOTUNE_A | | | | | | | |
| R/W-A8h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FORCE_AUTOTUNE_B | | | | | | | |
| R/W-A8h | | | | | | | |

**Table 7-46. REG0x61_AUTOTUNE_FORCE Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-8 | FORCE_AUTOTUNE_A | R/W | A8h | | Force value for phase A inductor time constant L(uH)/DCR(mΩ) : FORCE_AUTOTUNE_A= 256-265*L(uH)/DCR(mΩ). Default 0xA8 refers to 0.211 uH/mΩ |
| 7-0 | FORCE_AUTOTUNE_B | R/W | A8h | | Force value for phase B inductor time constant L(uH)/DCR(mΩ): FORCE_AUTOTUNE_B= 256-265*L(uH)/DCR(mΩ) Default 0xA8 refers to 0.211 uH/mΩ |


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### 7.6.34 REG0x62_GM_ADJUST_FORCE Register (Address = 62h) [Reset = 00C7h]

REG0x62_GM_ADJUST_FORCE is shown in Figure 7-47 and described in Table 7-47.

Return to the Summary Table.

**Figure 7-47. REG0x62_GM_ADJUST_FORCE Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| GM_ADJUST | | | | | | FORCE_UPDATE | RESERVED |
| R-0h | | | | | | R/W-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FORCE_GM_ADJUST | | | | | | FORCE_GM_ADJUST_EN | FORCE_AUTOTUNE_EN |
| R/W-31h | | | | | | R/W-1h | R/W-1h |

**Table 7-47. REG0x62_GM_ADJUST_FORCE Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-10 | GM_ADJUST | R | 0h | | Auto adaptive adjustment value for inductor DCR. This value is 0 when converter shuts off. If converter starts switching and FORCE_GM_ADJUST_EN=1b then GM_ADJUST=FORCE_GM_ADJUST+1 as fixed value. |
| 9 | FORCE_UPDATE | R/W | 0h | | Update FORCE_AUTOTUNE_A, FORCE_AUTOTUNE_B, FORCE_GM_ADJUST value to be effective for inductor DCR current sense. Converter will automatically shuts off and restart when this bit is written from 0b to 1b to login new force values. After one time update completes, the converter automatically recovers switching and reset this bit to 0b.<br>0b = Idle<br>1b = Update FORCE_AUTOTUNE_A,FORCE_AUTOTUNE_B, FORCE_GM_ADJUST values to converter |
| 8 | RESERVED | R | 0h | | Reserved |
| 7-2 | FORCE_GM_ADJUST | R/W | 31h | | Force GM adjustment value for inductor DCR: GM_ADJUST= 71.25-272/DCR(mΩ) Default value 0x31 refers to 12.2mΩ |
| 1 | FORCE_GM_ADJUST_EN | R/W | 1h | | Enable FORCE_GM_ADJUST effective for inductor DCR current sense. Converter will automatically shuts off and restart when FORCE_UPDATE bit is written from 0b to 1b to update these force values. When converter restarts from other reason, as long as this bit is 1b, converter will force GM_ADJUST = FORCE_GM_ADJUST+1 as fixed value<br>0b = Disable FORCE_GM_ADJUST<br>1b = Enable FORCE_GM_ADJUST |

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**Table 7-47. REG0x62_GM_ADJUST_FORCE Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 0 | FORCE_AUTOTUNE_EN | R/W | 1h | | Enable FORCE_AUTOTUNE_A, FORCE_AUTOTUNE_B effective for inductor DCR current sense. Converter will automatically shuts off and restart when FORCE_UPDATE bit is written from 0b to 1b to update these force values. When converter restarts from other reasons, as long as this bit is 1b, converter will follow the FORCE_AUTO_TUNE_A/B value and there is no auto calibration at beginning anymore.<br>0b = Disable FORCE_AUTOTUNE_A,FORCE_AUTOTUNE_B<br>1b = Enable FORCE_AUTOTUNE_A,FORCE_AUTOTUNE_B |


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### 7.6.35 REG0xFD_VIRTUAL_CONTROL Register (Address = FDh) [Reset = 0013h]

REG0xFD_VIRTUAL_CONTROL is shown in Figure 7-48 and described in Table 7-48.

Return to the Summary Table.

**Figure 7-48. REG0xFD_VIRTUAL_CONTROL Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EN_AUTO_CHG | RESERVED | | | | | | EN_OTG |
| R/W-0h | R-0h | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REG_RESET | RESERVED | | EN_EXTILIM | RESERVED | WD_RST | WDTMR_ADJ | |
| R/W-0h | R-0h | | R/W-1h | R-0h | R/W-0h | R/W-3h | |

**Table 7-48. REG0xFD_VIRTUAL_CONTROL Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | EN_AUTO_CHG | R/W | 0h | Reset by:<br>REG_RESET | Automatic charge control(recharge and terminate battery charging automatically):<br>0b = Disable<br>1b = Enable |
| 14-9 | RESERVED | R | 0h | | Reserved |
| 8 | EN_OTG | R/W | 0h | Reset by:<br>REG_RESET<br>WATCHDOG | OTG Mode Enable<br>Enable device in OTG mode when EN_OTG pin is HIGH.<br>0b = Disable<br>1b = Enable |
| 7 | REG_RESET | R/W | 0h | Reset by:<br>REG_RESET | Reset Registers<br>All the R/W and R registers go back to the default setting except: CHRG_STAT, MODE_STAT, HIDRV1_STAT, LODRV1_STAT, HIDRV2_STAT, LODRV2_STAT<br>0b = Idle<br>1b = Reset |
| 6-5 | RESERVED | R | 0h | | Reserved |
| 4 | EN_EXTILIM | R/W | 1h | Reset by:<br>REG_RESET | Enable ILIM_HIZ pin to set input current limit<br>0b = Disable(Input current limit is set by IIN_HOST())<br>1b = Enable(Input current limit is set by the lower value of ILIM_HIZ pin and IIN_HOST()) |
| 3 | RESERVED | R | 0h | | Reserved |
| 2 | WD_RST | R/W | 0h | Reset by:<br>REG_RESET | Reset watch dog timer control:<br>0b = Normal<br>1b = Reset(bit goes back to 0 after timer reset) |

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**Table 7-48. REG0xFD_VIRTUAL_CONTROL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 1-0 | WDTMR_ADJ | R/W | 3h | Reset by:<br>REG_RESET | WATCHDOG Timer Adjust<br>Set maximum delay between consecutive EC host write of charge voltage or charge current command. If device does not receive a write on the CHARGE_VOLTAGE() or the CHARGE_CURRENT() within the watchdog time period, the charger will be suspended by setting the CHARGE_CURRENT() to 0 mA. After expiration, the timer will resume upon the write of CHARGE_CURRENT(), CHARGE_VOLTAGE() ,WDTMR_ADJ or WD_RST=1b. The charger will resume if the values are valid.<br>00b = Disable<br>01b = 5 sec<br>10b = 88 sec<br>11b = 175 sec |


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### 7.6.36 REG0xFE_Manufacture_ID Register (Address = FEh) [Reset = 0040h]

REG0xFE_Manufacture_ID is shown in Figure 7-49 and described in Table 7-49.

Return to the Summary Table.

**Figure 7-49. REG0xFE_Manufacture_ID Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MANUFACTURE_ID | | | | | | | |
| R-40h | | | | | | | |

**Table 7-49. REG0xFE_Manufacture_ID Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-8 | RESERVED | R | 0h | | Reserved |
| 7-0 | MANUFACTURE_ID | R | 40h | | Manufacture ID : 40h |

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### 7.6.37 REG0xFF_Device_ID Register (Address = FFh) [Reset = 000Ah]

REG0xFF_Device_ID is shown in Figure 7-50 and described in Table 7-50.

Return to the Summary Table.

**Figure 7-50. REG0xFF_Device_ID Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEVICE_ID | | | | | | | |
| R-Ah | | | | | | | |

**Table 7-50. REG0xFF_Device_ID Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15-8 | RESERVED | R | 0h | | Reserved |
| 7-0 | DEVICE_ID | R | Ah | | Device ID<br>BQ25776: 00 001 100(0Ah) |


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The BQ25770EVM evaluation module (EVM) is a complete charger module for evaluating the BQ25770G. The application curves were taken using the BQ25770EVM.

## 8.2 Typical Application

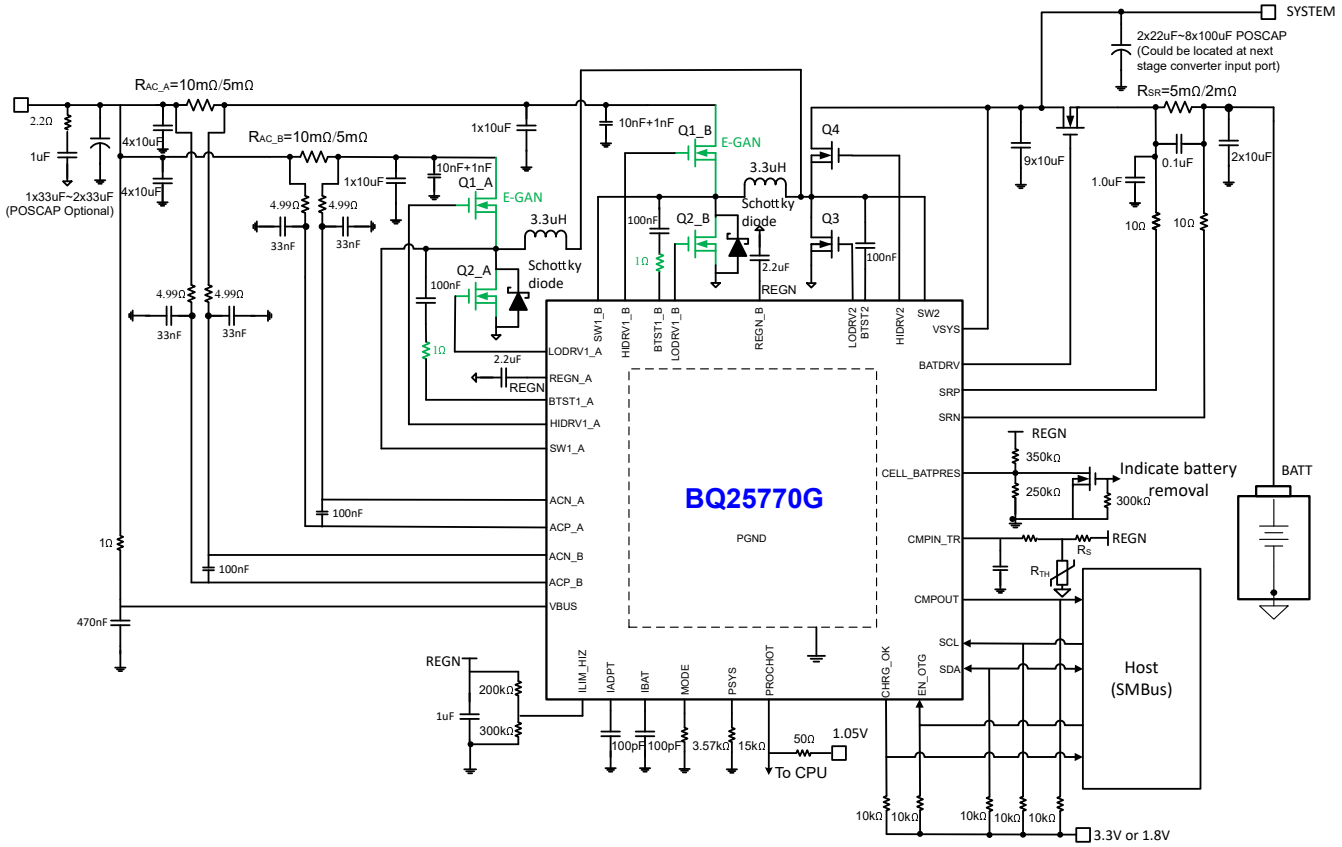


**Figure 8-1. Application Diagram of BQ25770G**

### 8.2.1 Design Requirements

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input Voltage(2) | 3.5 V < Adapter Voltage < 40 V |
| Input Current Limit (2) | 5 A for 28 V 140W adapter |
| Battery Charge Voltage(1) | 16800 mV for 4s battery |
| Battery Charge Current(1) | 8192 mA for 4s battery |
| Minimum System Voltage(1) | 12300 mV for 4s battery |

(1) Refer to battery specification for settings.
(2) Refer to adapter specification for settings for Input Voltage and Input Current Limit.

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### 8.2.2 Detailed Design Procedure

The parameters are configurable using the evaluation software. The simplified application circuit (see Figure 8-1, as the application diagram) shows the minimum component requirements. Inductor, capacitor, and MOSFET selection are explained in the rest of this section. Refer to the EVM user's guide for the complete application schematic.

#### *8.2.2.1 ACP-ACN Input Filter*

The BQ25770G input current sensing through ACP_A-ACN_A and ACP_B-ACN_B are critical to ensure IINDPM/IOTG regulation stability. Parasitic inductance on board will generate high frequency ringing on ACP_A-ACN_A and ACP_B-ACN_B which overwhelms converter sensed inductor current information. Larger parasitic inductance will generate larger sense current ringing which could cause the average current control loop to go into oscillation. Therefore ACP_A-ACN_A and ACP_B-ACN_B sensing information need to be conditioned.

For real system board condition, we suggest using below circuit design to get best result and filter noise induced from different PCB parasitic factor. The filter is effective and the delay of on the sensed signal is small, therefore there is no concern for average current mode control. On ACN_A and ACN_B side the maximum capacitance is 1*10-µF MLCC shown below, the 10 nF + 1 nF EMI filtering capacitance can be neglected comparing to the 10-µF MLCC. When the 10-µF MLCC is used on ACN_A and ACN_B, then differential 100-nF ~ 220-nF filter capacitors are recommended for ACP_A-ACN_A and ACP_B-ACN_B to prevent pulse reverse current through RAC.

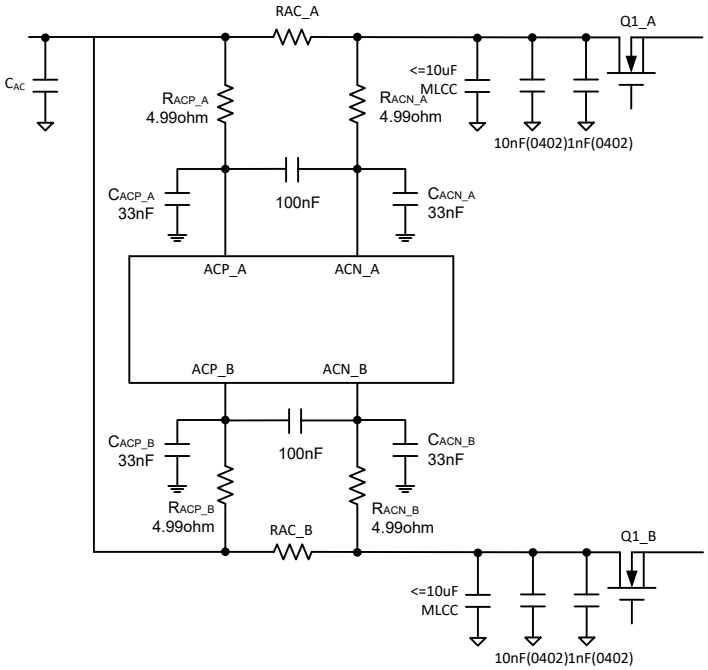


**Figure 8-2. ACN-ACP Input Filter**

#### *8.2.2.2 Inductor Selection*

The BQ25770G has two selectable fixed switching frequency 600 kHz/800 kHz. Higher switching frequency allows the use of smaller inductance. Inductor saturation current should be higher than the charging current ($I_{CHG}$) plus half the ripple current ($I_{RIPPLE}$):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (3)$$

The inductor ripple current in buck operation depends on input voltage ($V_{IN}$), duty cycle ($D_{BUCK} = V_{OUT}/V_{IN}$), switching frequency ($f_S$) and inductance (L):


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$$I_{RIPPLE_BUCK} = V_{IN} \times D_{BUCK} \times (1-D_{BUCK}) / (f_S \times L) \quad (4)$$

During boost operation, the duty cycle is:

$D_{BOOST} = 1 – (V_{IN}/V_{BAT})$

and the ripple current is:

$I_{RIPPLE_BOOST} = (V_{IN} \times D_{BOOST}) / (f_S \times L)$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 12 V to 16.8 V for 4-cell battery pack. For 28-V adapter voltage, 14-V battery voltage gives the maximum inductor ripple current.

The recommended inductor DCR range is 5 mΩ ~ 25 mΩ for each phase. Inductor DCR beyond this range may hold system stability risk which is not recommended. Upon different switching frequency and VBUS input voltage recommended inductance are summarized in Table 8-1. Inductance lower than the recommendation could result in large inductor ripple and high inductor core loss which is not preferred.

**Table 8-1. Inductance Selection Recommendation**

| | VBUS = 20 V | VBUS = 28 V | VBUS = 36 V |
|---|---|---|---|
| Fsw=600 kHz | 2.2 µH | 2.2 µH | 3.3 µH |
| Fsw=800 kHz | 1.5 µH | 1.5 µH | 2.2 µH |

#### *8.2.2.3 Input Capacitor*

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current (plus system current there is any system load) when duty cycle is 0.5 in buck mode. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 5:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed in front of RAC current sensing and as close as possible to the power stage half bridge MOSFETs. Capacitance after RAC before power stage half bridge should be limited to10µF+10nF+1nF referring to Figure 8-2 diagram. Voltage rating of the capacitor must be higher than normal input voltage level, 35 V rating or higher capacitor is preferred for 28 V input voltage. Minimum 10 pieces of 10-µF 0603 size capacitors are suggested for 28V/140 W adapter design. 50-V rating or higher capacitor is preferred for 36-V input voltage. Minimum 10*10µF 0805 capacitors are needed when power reaches 36 V/180 W. Under different input voltage the minimum input capacitance requirement is summarized in Table 8-2, Table 8-3 and Table 8-4. For quasi dual phase it is recommended to spread the MLCC caps before RAC_A and RAC_B. 1*10nF+1nF 0402 package MLCC capacitors (EMI filter purpose) are recommended to be placed as close as possible to both phase A and phase B half bridge MOSFETs.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required capacitance value at the operating point. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which is recommended especially for 28-V and 36-V higher power application.

**Table 8-2. Input Capacitance Requirement for 20-V/100-W System**

| 20-V/100-W SYSTEM | MINIMUM | TYPICAL | MAXIMUM |
|---|---|---|---|
| Effective input capacitance | 4 µF (MLCC) OTG is not needed<br>8 µF (MLCC) OTG is needed | 4 µF (MLCC) + 15 µF (POSCAP) | 4 µF (MLCC) + 2*33 µF (POSCAP) |

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**Table 8-2. Input Capacitance Requirement for 20-V/100-W System (continued)**

| 20-V/100-W SYSTEM | MINIMUM | TYPICAL | MAXIMUM |
|---|---|---|---|
| Practical input capacitors configuration | 4*10 µF OTG is not needed (0603 35 V MLCC derating to around 10% under 20-V bias voltage) | 4*10 µF (0603 35 V MLCC derating to around 10% under 20-V bias voltage)<br>1*15 µF (2917 35 V POSCAP) | 4*10 µF (0603 35 V MLCC derating to around 10% under 20-V bias voltage)<br>2*33 µF (2917 35 V POSCAP) |

**Table 8-3. Input Capacitance Requirement for 28-V/140-W System**

| 28-V/140-W SYSTEM | MINIMUM | TYPICAL | MAXIMUM |
|---|---|---|---|
| Effective input capacitance | 6 µF (MLCC) OTG is not needed<br>8 µF (MLCC) OTG is needed | 6 µF (MLCC) + 15 µF (POSCAP) | 6 µF (MLCC) + 2*33 µF (POSCAP) |
| Practical input capacitors configuration | 10*10 µF OTG is not needed (0603 35 V MLCC derating to around 6% under 28-V bias voltage) | 10*10 µF (0603 35 V MLCC derating to around 6% under 28-V bias voltage )<br>1*15 µF (2917 35 V POSCAP) | 10*10 µF (0603 35 V MLCC derating to around 6% under 28-V bias voltage )<br>2*33 µF (2917 35 V POSCAP) |

**Table 8-4. Input Capacitance Requirement for 36-V/180-W System**

| 36-V/180-W SYSTEM | MINIMUM | TYPICAL | MAXIMUM |
|---|---|---|---|
| Effective input capacitance | 8 µF (MLCC) | 8 µF (MLCC) + 15 µF (POSCAP) | 8 µF (MLCC) + 2*33 µF (POSCAP) |
| Practical input capacitors configuration | 10*10 µF (0805 50 V MLCC derating to around 8% under 36-V bias voltage) | 10*10 µF (0805 50 V MLCC derating to around 8% under 36-V bias voltage)<br>1*15 µF (2917 50 V POSCAP) | 10*10 µF (0805 50 V MLCC derating to around 8% under 36-V bias voltage)<br>2*33 µF (2917 50 V POSCAP) |

#### *8.2.2.4 Output Capacitor*

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The preferred ceramic capacitor is 35-V X7R or X5R for output capacitor. Minimum 7 pieces of 10-µF 0603 size capacitor is suggested to be placed as close as possible to Q3&Q4 half bridge (between Q4 drain and Q3 source terminal), when the power reaches 140 W/180 W 2 more 0603 MLCC are recommended at system output. Recommend to place minimum 2*10 µF after the charge current sense resistor for best stability. The overall minimum VSYS effective capacitance should be 50 µF including all the capacitance distributed along the VSYS output line like input capacitance on the next stage VRs referring to Table 8-5.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required capacitance value at the operating point.

**Table 8-5. Minimum Output Capacitance Requirement**

| OUTPUT CAPACITORS vs TOTAL INPUT POWER | 100 W | 140 W | 180 W |
|---|---|---|---|
| Minimum Effective Output Capacitance | 50 µF | 50 µF | 50 µF |
| Minimum output capacitors at charger VSYS output terminal | 7*10 µF (0603 35 V MLCC) | 9*10 µF (0603 35 V MLCC) | 9*10 µF (0603 35 V MLCC) for VBUS<=28 V<br>9*10 µF (0805 50 V MLCC) for VBUS=36 V |


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**Table 8-5. Minimum Output Capacitance Requirement (continued)**

| OUTPUT CAPACITORS vs TOTAL INPUT POWER | 100 W | 140 W | 180 W |
|---|---|---|---|
| Minimum additional output capacitors along VSYS distribution line, input cap of next stage converter can also be counted. | 2*22 µF (2917 35 V POSCAP with <100 mΩ ESR for each) | 2*22 µF (2917 35 V POSCAP with <100 mΩ ESR for each) | 2*22 µF (2917 35 V POSCAP with <100 mΩ ESR for each) VBUS<=28 V<br>2*22 µF (2917 50 V POSCAP with <100 mΩ ESR for each) VBUS=36 V |

It is common under higher system power the total next stage (Vcore) input capacitance could be increased accordingly. These capacitance are also counted as charger system output capacitance. When these capacitance is too large it could also influence controller stability and maximum effective output capacitance are listed below for reference.

**Table 8-6. Maximum Output Capacitance Requirement**

| OUTPUT CAPACITORS vs TOTAL INPUT POWER | 100 W | 140 W | 180 W |
|---|---|---|---|
| Maximum Effective Output Capacitance | 500 µF | 800 µF | 800 µF |
| Maximum output capacitors along VSYS distribution line, input cap of next stage converter can also be counted. | 5*100 µF (2917 35 V POSCAP with <100 mΩ ESR for each) | 8*100 µF (2917 35 V POSCAP with <100 mΩ ESR for each) | 8*100 µF (2917 35 V POSCAP with <100 mΩ ESR for each) VBUS<=28 V<br>8*100 µF (2917 50 V POSCAP with <100 mΩ ESR for each) VBUS=36 V |

#### *8.2.2.5 Power MOSFETs Selection*

Six external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are integrated into the IC with 5 V of gate drive voltage. MOSFET breakdown voltage ($BV_{DSS}$) rating refers to Table 8-7 based on different input voltage and application position. 5mm*6mm package MOSFET is preferred for better thermal performance and 3.3mm*3.3mm package MOSFET is preferred for higher power density design.

**Table 8-7. MOSFET Voltage Rating Recommendation**

| | 20 V/100 W | 28 V/140 W | 36 V/180 W |
|---|---|---|---|
| Buck Half bridge (Q1_A,Q2_A,Q1_B,Q2_B) | $BV_{DSS}$=30 V or higher | $BV_{DSS}$=40 V or higher | $BV_{DSS}$=60 V or higher |
| Boost Half bridge (Q3,Q4) and BATFET (Q5) | $BV_{DSS}$=30 V or higher | $BV_{DSS}$=30 V or higher | $BV_{DSS}$=40 V or higher (for Buck HS short fault condition safety) |

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, $Q_{GD}$. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, $Q_G$.

$$FOM_{top} = R_{DS(on)} \cdot Q_{GD};\ FOM_{bottom} = R_{DS(on)} \cdot Q_G \quad (6)$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. Taking buck mode operation as an example the power loss is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current ($I_{CHG}$), MOSFET's on-resistance ($R_{DS(ON)_top}$), input voltage ($V_{IN}$), switching frequency ($f_S$), turn-on time ($t_{on}$) and turn-off time ($t_{off}$):

$$P_{top} = P_{con_top} + P_{sw_top} \quad (7)$$

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$$P_{con_top} = D \cdot I_{L_RMS}^{2} \cdot R_{DS(on)_top}; \quad (8)$$

$$I_{L_RMS}^{2} = I_{L_DC}^{2} + I_{ripple}^{2}/12 \quad (9)$$

- $I_{L_DC}$ is the average inductor DC current under buck mode;
- $I_{ripple}$ is the inductor current ripple peak-to-peak value;

$$P_{sw_top} = P_{IV_top} + P_{Qoss_top} + P_{Gate_top}; \quad (10)$$

The first item $P_{con_top}$ represents the conduction loss which is straight forward. The second term $P_{sw_top}$ represents the multiple switching loss items in top MOSFET including voltage and current overlap losses ($P_{IV_top}$), MOSFET parasitic output capacitance loss ($P_{Qoss_top}$) and gate drive loss ($P_{Gate_top}$). To calculate voltage and current overlap losses ($P_{IV_top}$):

$$P_{IV_top} = 0.5x\ V_{IN} \cdot I_{valley} \cdot t_{on} \cdot f_S + 0.5x\ V_{IN} \cdot I_{peak} \cdot t_{off} \cdot f_S \quad (11)$$

$$I_{valley} = I_{L_DC} - 0.5 \cdot I_{ripple} \text{ (inductor current valley value)}; \quad (12)$$

$$I_{peak} = I_{L_DC} + 0.5 \cdot I_{ripple} \text{ (inductor current peak value)}; \quad (13)$$

- $t_{on}$ is the MOSFET turn-on time that $V_{DS}$ falling time from $V_{IN}$ to almost zero (MOSFET turn on conduction voltage);
- $t_{off}$ is the MOSFET turn-off time that $I_{DS}$ falling time from $I_{peak}$ to zero;

The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \quad (14)$$

where $Q_{sw}$ is the switching charge, $I_{on}$ is the turn-on gate driving current, and $I_{off}$ is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge ($Q_{GD}$) and gate-to-source charge ($Q_{GS}$):

$$Q_{sw} = Q_{GD} + Q_{GS} \quad (15)$$

Gate driving current can be estimated by REGN voltage ($V_{REGN}$), MOSFET plateau voltage ($V_{plt}$), total turn-on gate resistance ($R_{on}$), and turn-off gate resistance ($R_{off}$) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (16)$$

To calculate top MOSFET parasitic output capacitance loss ($P_{Qoss_top}$):

$$P_{Qoss_top} = 0.5 \cdot V_{IN} \cdot Q_{oss} \cdot f_S \quad (17)$$

- $Q_{oss}$ is the MOSFET parasitic output charge which can be found in MOSFET data sheet;

To calculate top MOSFET gate drive loss ($P_{Gate_top}$):

$$P_{Gate_top} = V_{IN} \cdot Q_{Gate_top} \cdot f_S \quad (18)$$

- $Q_{Gate_top}$ is the top MOSFET gate charge which can be found in MOSFET data sheet;
- Note here $V_{IN}$ is used instead of real gate drive voltage 6 V because, the gate drive 6 V is generated based on LDO from $V_{IN}$ under buck mode, the total gate drive related loss are all considered when $V_{IN}$ is used for gate drive loss calculation .

The bottom-side MOSFET loss also includes conduction loss and switching loss:

$$P_{bottom} = P_{con_bottom} + P_{sw_bottom} \quad (19)$$


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$$P_{con_bottom} = (1 - D) \cdot I_{L_RMS}^{2} \cdot R_{DS(on)_bottom}; \quad (20)$$

$$P_{sw_bottom} = P_{RR_bottom} + P_{Dead_bottom} + P_{Gate_bottom}; \quad (21)$$

The first item $P_{con_bottom}$ represents the conduction loss which is straight forward. The second term $P_{sw_bottom}$ represents the multiple switching loss items in bottom MOSFET including reverse recovery losses ($P_{RR_bottom}$), Dead time body diode conduction loss ($P_{Dead_bottom}$) and gate drive loss ($P_{Gate_bottom}$). The detail calculation can be found below:

$$P_{RR_bottom} = V_{IN} \cdot Q_{rr} \cdot f_S \quad (22)$$

- $Q_{rr}$ is the bottom MOSFET reverse recovery charge which can be found in MOSFET data sheet;

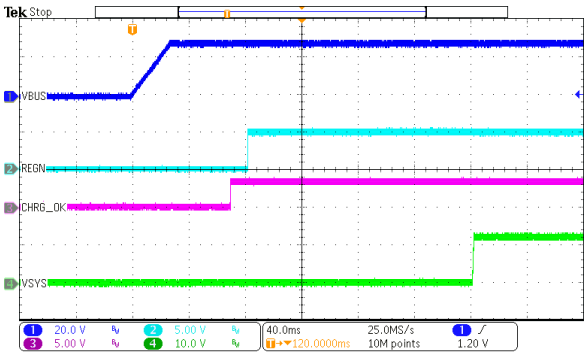
$$P_{Dead_bottom} = V_F \cdot I_{valley} \cdot f_S \cdot t_{dead_rise} + V_F \cdot I_{peak} \cdot f_S \cdot t_{dead_fall} \quad (23)$$

- $V_F$ is the body diode forward conduction voltage drop;
- $t_{dead_rise}$ is the SW rising edge deadtime between top and bottom MOSFETs which is around 20 ns;
- $t_{dead_fall}$ is the SW falling edge deadtime between top and bottom MOSFETs which is around 20 ns;

$P_{Gate_bottom}$ can follow the same method as top MOSFET gate drive loss calculation approach refer to Equation 18.

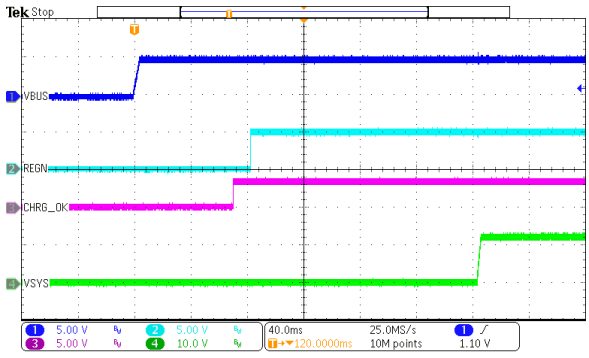
N-channel MOSFETs is used for battery charging BATFET. The gate drivers are internally integrated into the IC with 5V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred , the Ciss of N-channel MOSFET should be chosen less than 6 nF.

### 8.2.3 Application Curves



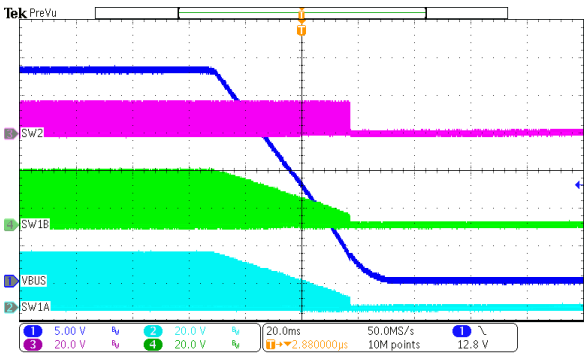

VBUS = 28 V VSYS_MIN=12.3V ISYS=0A

**Figure 8-3. Power Up From 28 V**



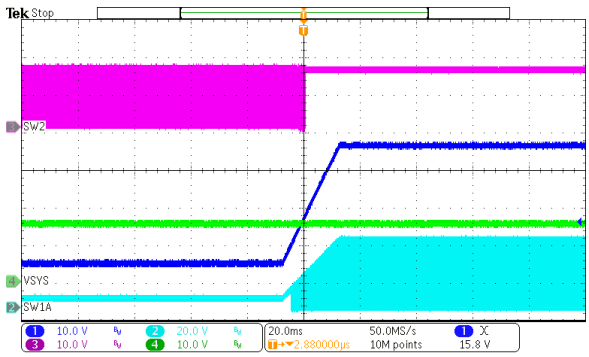

VBUS = 5 V VSYS_MIN=12.3V ISYS=0A

**Figure 8-4. Power Up From 5 V**




VBUS = 28V->0V VBAT=14.8V
VSYS_MIN=12.3V ISYS=100mA

**Figure 8-5. Power Off From 28 V**




VBUS = 10V->20V VBAT=14.8V
VSYS_MIN=12.3V ISYS=3A

**Figure 8-6. Line Regulation**

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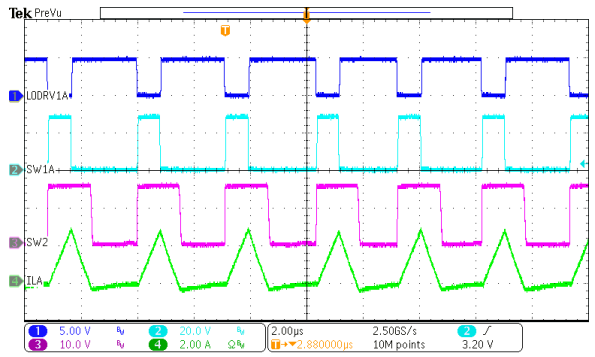
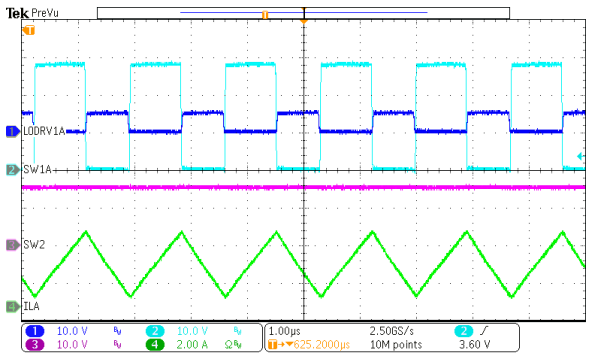


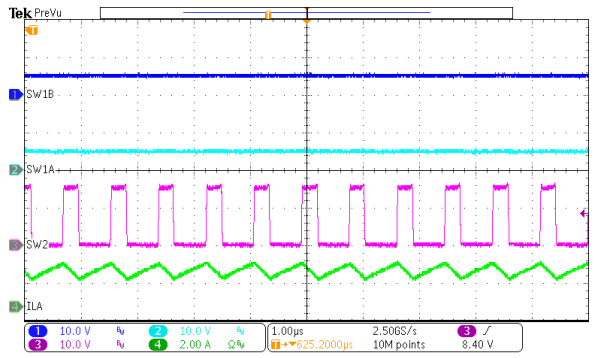

VBUS = 28V VBAT=14.8V
VSYS_MIN=12.3V ISYS=100mA

**Figure 8-7. PFM Operation**



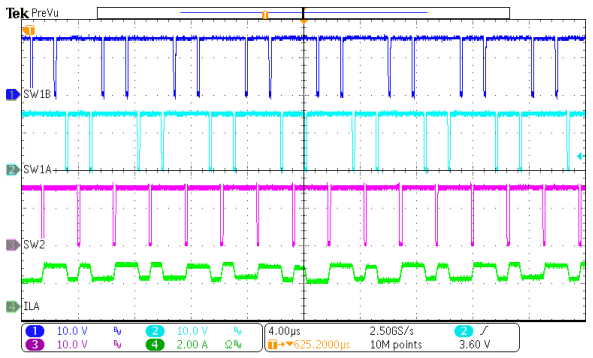

VBUS = 28V VBAT=14.8V
VSYS_MIN=12.3V ISYS=2A

**Figure 8-8. PWM Operation**



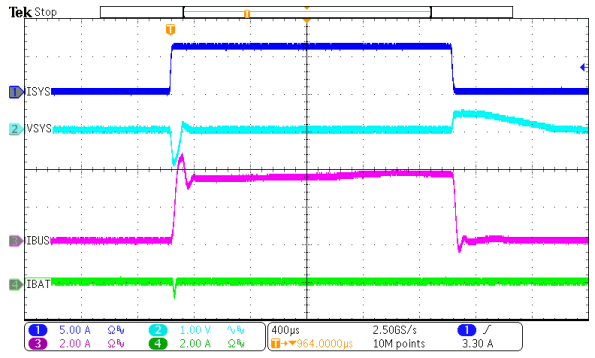

VBUS = 5V VBAT=14.8V
VSYS_MIN=12.3V ISYS=1A

**Figure 8-9. Switching During Boost Mode**



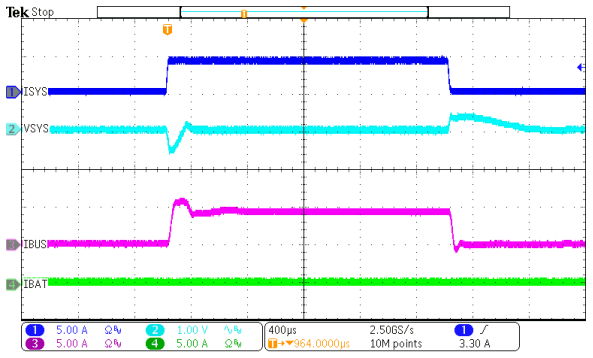

VBUS = 15V VBAT=14.8V
VSYS_MIN=12.3V ISYS=3A

**Figure 8-10. Switching During Buck Boost Mode**




VBUS = 28V VBAT=14.8V ISYS=0~6A

**Figure 8-11. System Regulation in Buck Mode**




VBUS = 15V VBAT=14.8V ISYS=0~4A

**Figure 8-12. System Regulation in Buck Boost Mode**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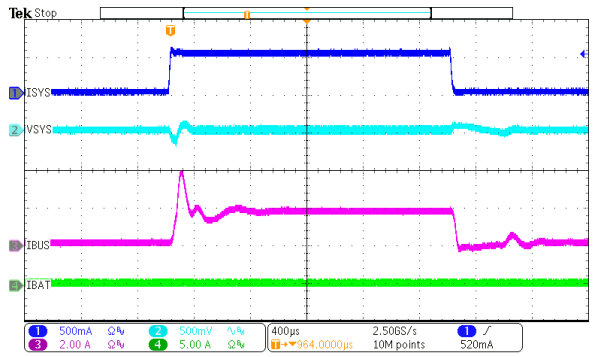
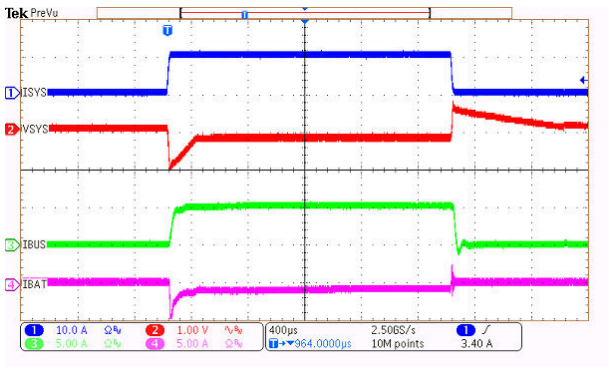


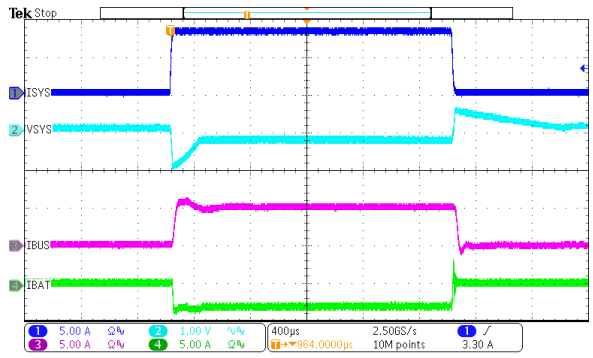

VBUS = 5V VBAT=14.8V ISYS=0~0.5A

**Figure 8-13. System Regulation in Boost Mode**



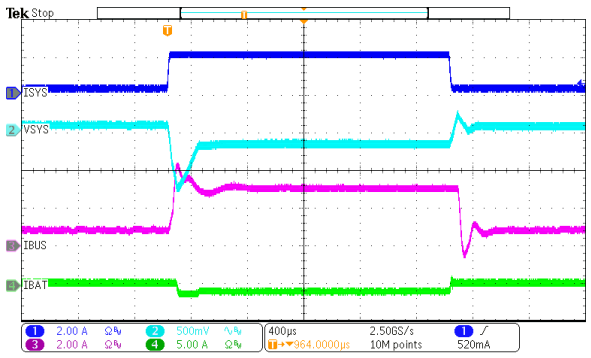

VBUS = 28V VBAT=14.8V IINDPM=5A ISYS=0~10A

**Figure 8-14. Input Current Regulation in Buck Mode**



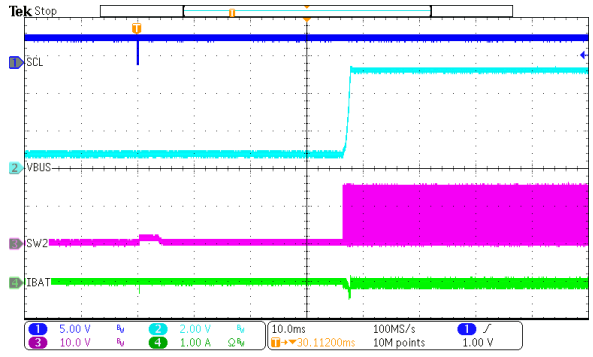

VBUS = 15V VBAT=14.8V IINDPM=5A ISYS=0~8A

**Figure 8-15. Input Current in Buck Boost Mode**



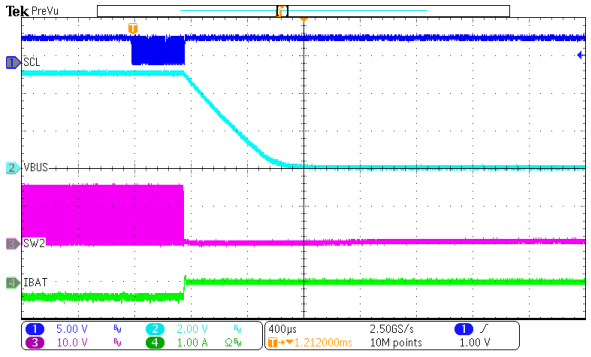

VBUS = 5V VBAT=14.8V IINDPM=3A ISYS=0~2A

**Figure 8-16. Input Current in Boost Mode**




VOTG= 5V VBAT=14.8V IOTG=3A IBUS=1A

**Figure 8-17. OTG Voltage Ramp Up After Enable**




VOTG= 5V VBAT=14.8V IOTG=3A IBUS=1A

**Figure 8-18. OTG Voltage Power Off After Disable**

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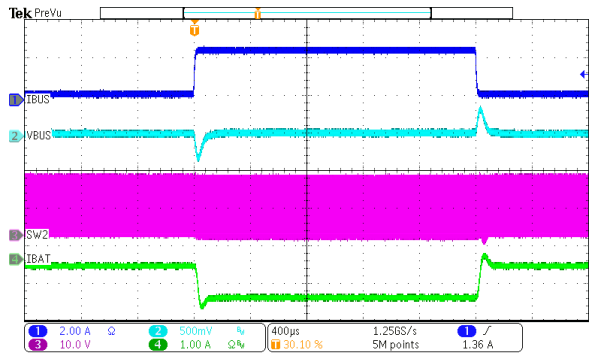
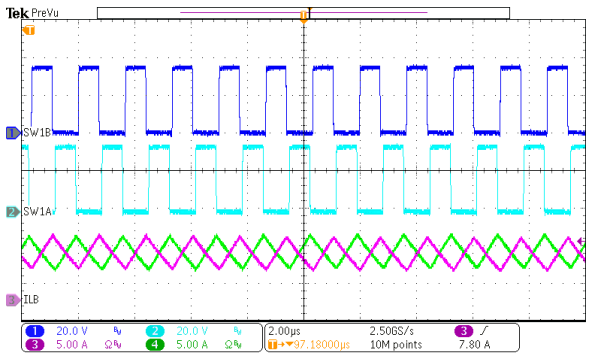


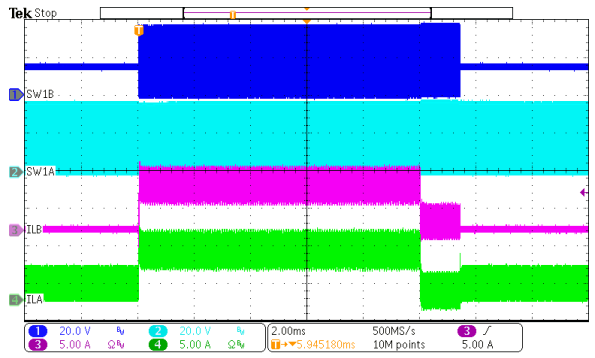

VOTG= 5V VBAT=14.8V IOTG=5A IBUS=0.3~2.7A

**Figure 8-19. OTG Load Transient**



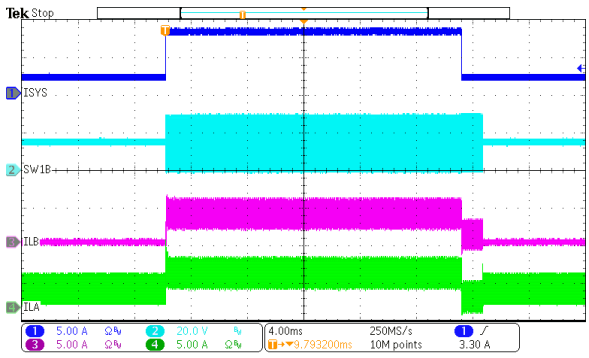

VBUS= 36V VBAT=14.8V ISYS=12.2A

**Figure 8-20. Dual Phase Current Balance at 36 V 180 W**



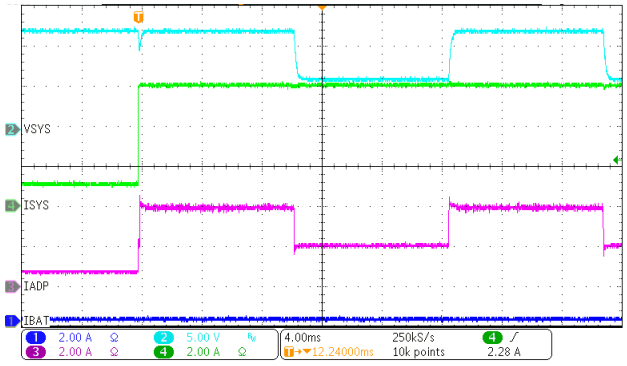

VBUS= 36V ISYS=2~12A
SINGLE_DUAL_TRANS_TH=6A PH_DROP_DEG=1ms

**Figure 8-21. Automatic Second Phase Adding and Dropping Under 36-V VBUS**



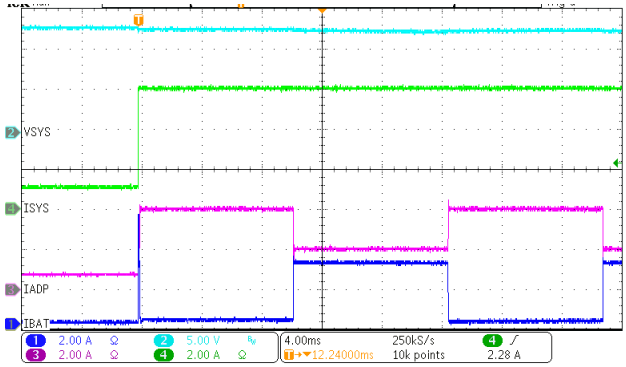

VBUS= 28V ISYS=2~8A
SINGLE_DUAL_TRANS_TH=5A PH_DROP_DEG=1ms

**Figure 8-22. Automatic Second Phase Adding and Dropping Under 28-V VBUS**




VBUS = 28 V IIN_DPM=2A ILIM2_VTH=200%
$T_{MAX}$=20ms $T_{OVLD}$=10ms ISYS=1~6A

**Figure 8-23. Peak Power Mode VSYS Trigger**




VBUS = 28 V IIN_DPM=2A ILIM2_VTH=200%
$T_{MAX}$=20ms $T_{OVLD}$=10ms ISYS=1~6A

**Figure 8-24. Peak Power Mode IBUS Trigger**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# 9 Power Supply Recommendations

The valid adapter range is from 3.5 V ($V_{VBUS_CONVEN}$) to 40 V with at least 500-mA current rating. When CHRG_OK goes HIGH, the system is powered from adapter through the charger. When adapter is removed, the system is connected to battery through BATFET. Typically the battery depletion threshold should be greater than the VSYS_MIN so that the battery capacity can be fully utilized for maximum battery run time.

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# 10 Layout

## 10.1 Layout Guidelines

Proper layout of the components to minimize high frequency current path loop (see Section 10.2) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

**Table 10-1. PCB Layout Guidelines**

| RULES | COMPONENTS | FUNCTION | IMPACT | GUIDELINES |
|---|---|---|---|---|
| 1 | | PCB layer stack up | Thermal, efficiency, signal integrity | Multi- layer PCB is suggested. Allocate at least one ground layer. The BQ2577xG EVM uses a 6-layer PCB (top layer, ground layer, signal layer and bottom layer). |
| 2 | CBUS, RAC_A, RAC_B, Q1_A, Q1_B, Q2_A, Q2_B | Input loop | High frequency noise, ripple | VBUS capacitors, RAC_A, RAC_B, Q1_A, Q1_B and Q2_A, Q2_B form two small loops 1 and 2. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CBUS to the other side of PCB for high density design. After RAC_A, RAC_B before Q1_A, Q1_B and Q2_A, Q2_B power stage recommend to put 10uF(0603/0805 package)+10nF+1nF(0402 package) decoupling capacitors as close as possible to IC to decoupling switching loop high frequency noise. |
| 3 | RAC_A, RAC_B, Q1_A, Q1_B, L1, Q4 | Current path | Efficiency | The current path from VBUS to VSYS, through RAC_A, RAC_B, Q1_A, Q1_B, L1, Q4, has low impedance. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1~2A/via for a 10mil via with 1 oz copper thickness. |
| 4 | CSYS, Q3, Q4 | Output loop | High frequency noise, ripple | VSYS capacitors, Q3 and Q4 form a small loop 3. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CSYS to the other side of PCB for high density design. |
| 5 | QBAT, RSR | Current path | Efficiency, battery voltage detection | Place QBAT and RSR near the battery terminal. The current path from VBAT to VSYS, through RSR and QBAT, has low impedance. Pay attention to via resistance if they are not on the same side. The device detects the battery voltage through SRN near battery terminal. |
| 6 | Q1_A, Q1_B, Q2_A, Q2_B, L1, Q3, Q4 | Power stage | Thermal, efficiency | Place Q1_A and Q2_A, Q1_B and Q2_B, L1, Q3 and Q4 next to each other. Allow enough copper area for thermal dissipation. The copper area is suggested to be 2x~4x of the pad size. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat. |
| 7 | RAC_A, RAC_B, RSR | Current sense | Regulation accuracy | Use Kelvin-sensing technique for RAC_A, RAC_B and RSR current sense resistors. Connect the current sense RAC_A, RAC_B to the center of the pads, and run current sense traces as differential pairs. |
| 8 | Small capacitors | IC bypass caps | Noise, jittering, ripple | Place VBUS cap, VCC cap, REGN caps near IC. |


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**Table 10-1. PCB Layout Guidelines (continued)**

| RULES | COMPONENTS | FUNCTION | IMPACT | GUIDELINES |
|---|---|---|---|---|
| 9 | BTST capacitors | HS gate drive | High frequency noise, ripple | Place HS MOSFET boost strap circuit capacitor close to IC and on the same side of PCB board. Capacitors SW1_A/SW1_B/2 nodes are recommended to use wide copper polygon to connect to power stage and capacitors BTST1_A/BTST1_B/BTST2 node are recommended to use at least 8mil trace to connected to IC BTST1_A/BTST1_B/BTST2 pins. |
| 10 | | Ground partition | Measurement accuracy, regulation accuracy, jitters, ripple | Separate analog ground(AGND) and power grounds(PGND) is preferred. PGND should be used for all power stage related ground net. AGND should be used for all sensing, compensation and control network ground for example ACP_A/ACN_A/ACP_B/ ACN_B/CMPIN_TR/CMPOUT/IADPT/IBAT/PSYS. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. If possible, use dedicated AGND traces. Connect analog ground and power ground together using power pad as the single ground connection point. |

## 10.2 Layout Example

### 10.2.1 Layout Example Reference Top View

Based on the above layout guidelines, the quasi dual phase buck-boost charger layout example top view is shown below including all the key power components. Also the top layer PCB is shown separately to illustrate top layer PCB routing, main power flow and key optimization parasitic loop1-3.

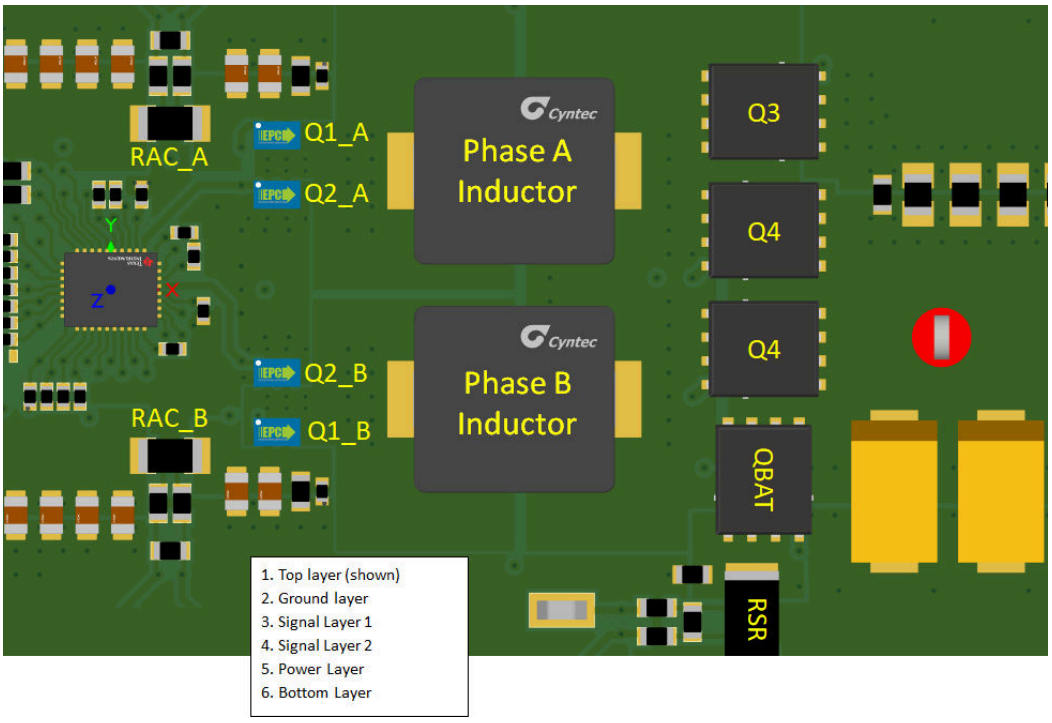


**Figure 10-1. Quasi Dual Phase Buck-Boost Charger Layout Reference Example Top View**

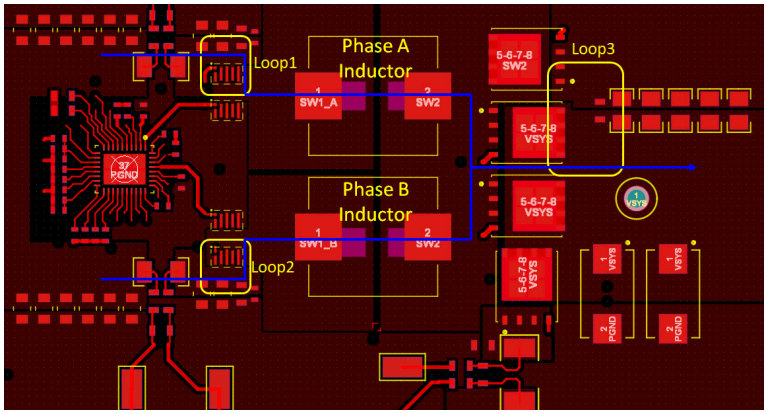


**Figure 10-2. Quasi Dual Phase Buck-Boost Charger Top Layer PCB Overview**


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# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics* Application Report SPRA953
- *BQ2571x Evaluation Module* User's Guide SLUUBT8
- *QFN/SON PCB Attachment* Application Report SLUA271

## 11.3 Receiving Notification of Documentation Updates

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## 11.4 Support Resources

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| April 2024 | * | Initial Release |

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## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| BQ25770GREER | Active | Production | WQFN (REE) \| 36 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | Q25770G |
| BQ25770GREER.A | Active | Production | WQFN (REE) \| 36 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | Q25770G |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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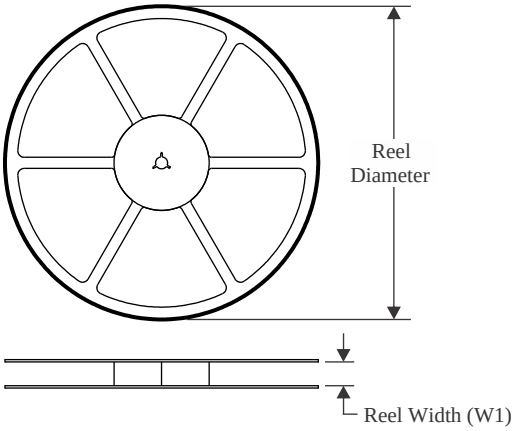
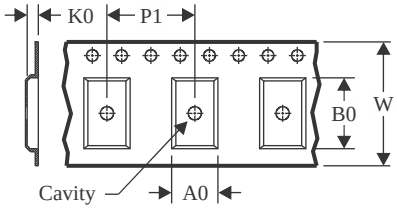
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

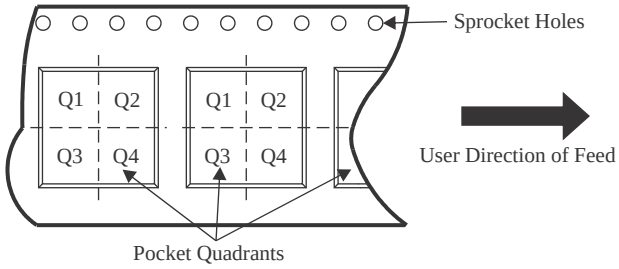



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

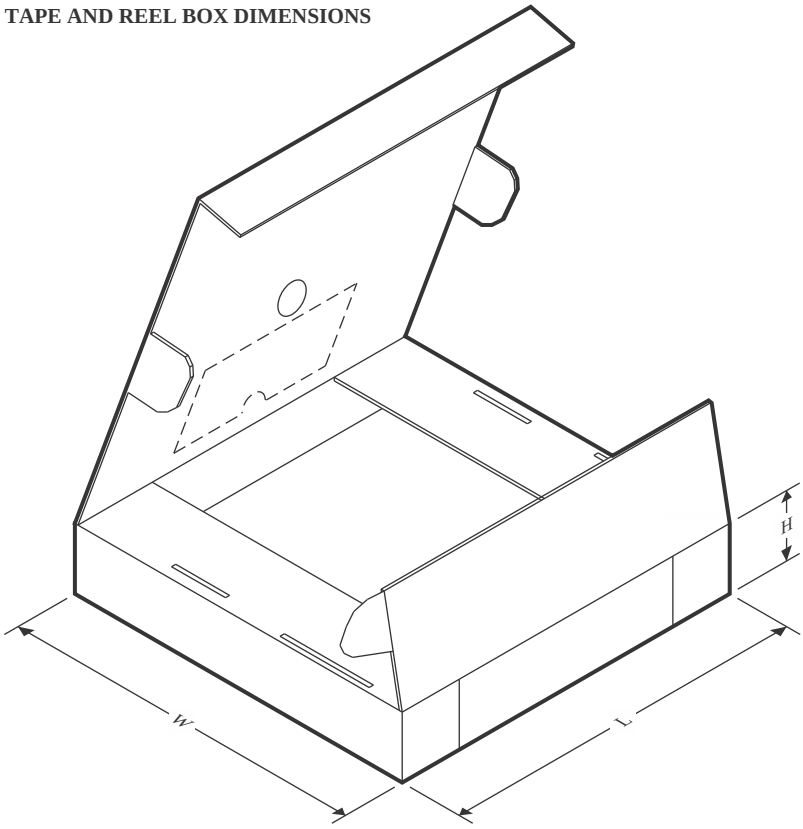
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ25770GREER | WQFN | REE | 36 | 3000 | 330.0 | 12.4 | 4.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

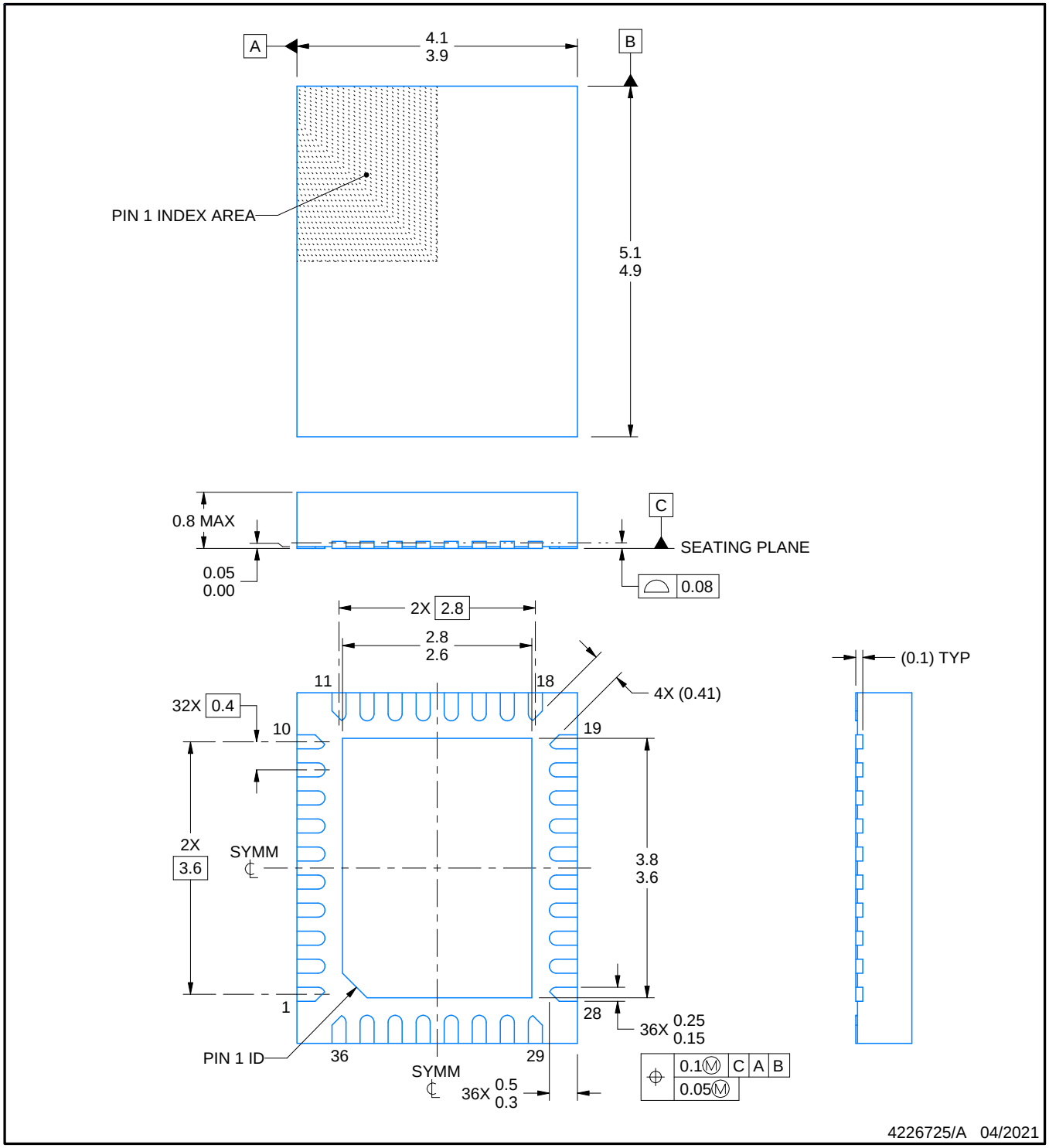
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ25770GREER | WQFN | REE | 36 | 3000 | 360.0 | 360.0 | 36.0 |

# REE0036A

# PACKAGE OUTLINE

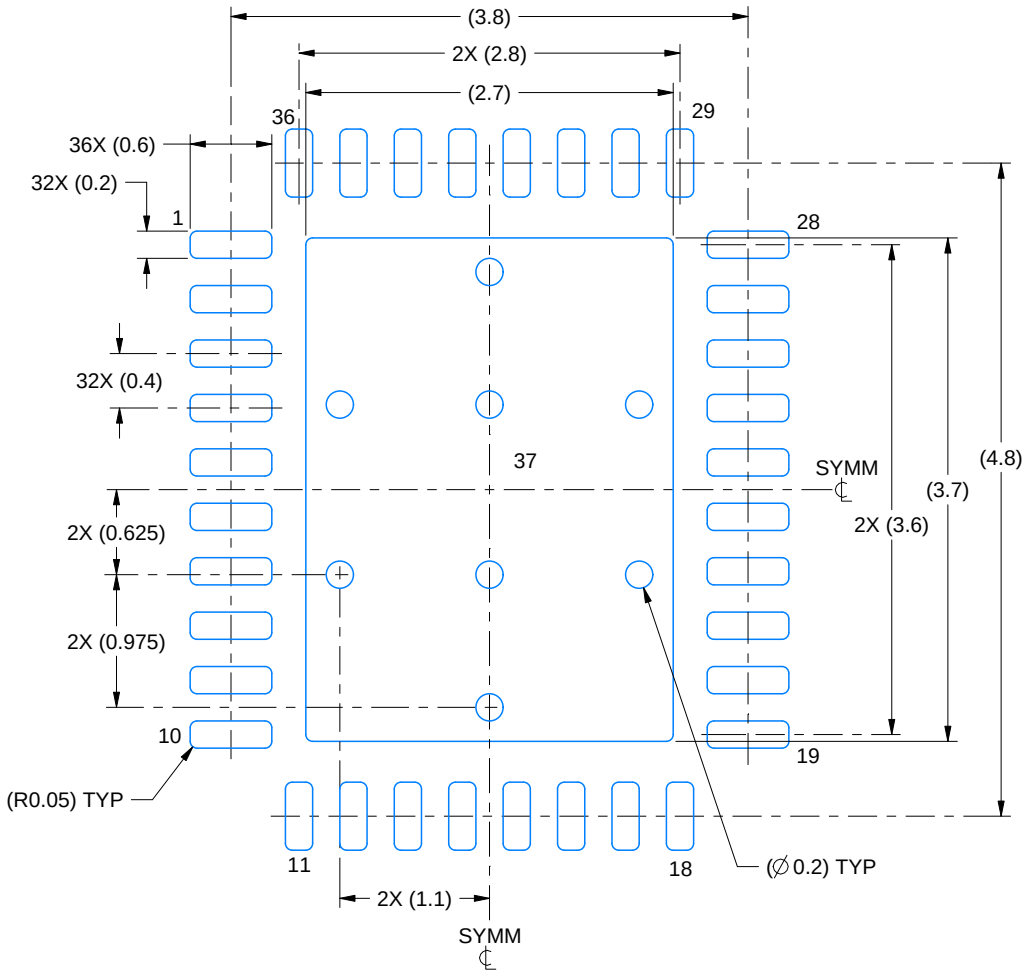
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

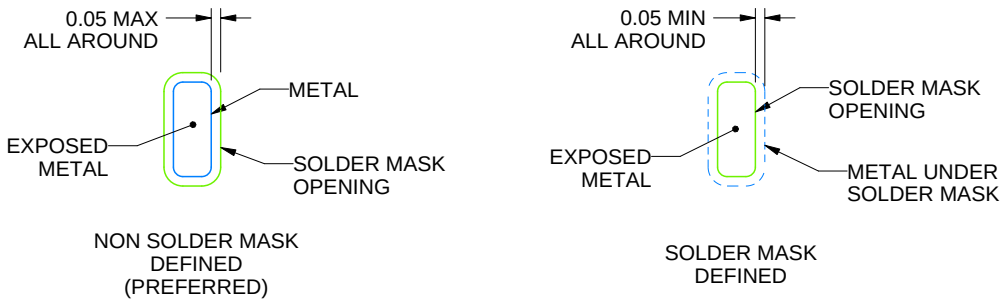



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

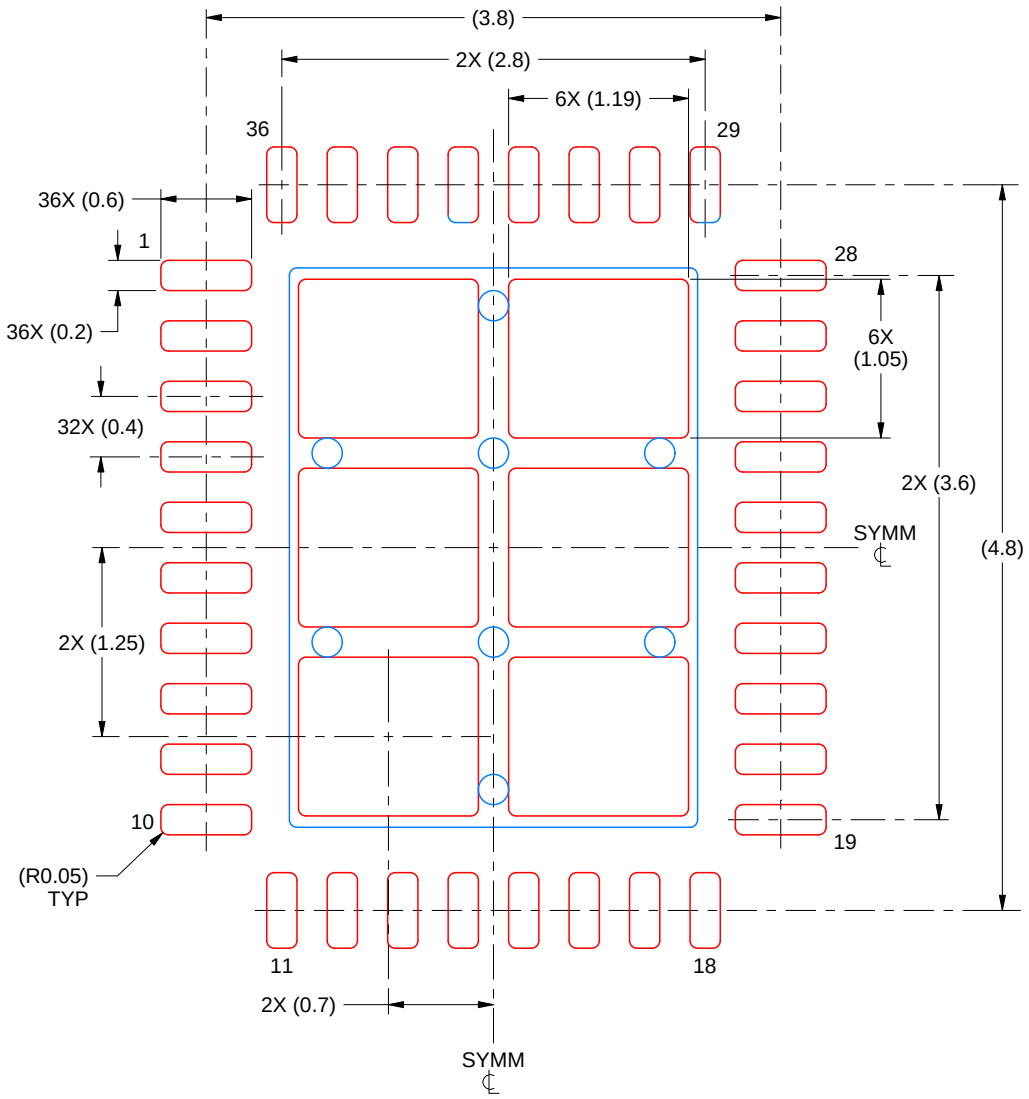



SOLDER MASK DETAILS

4226725/A 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4226725/A 04/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025

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