TEXAS INSTRUMENTS
BQ25723
SLUSE64 – MAY 2021

BQ25723 I²C 1- to 4-Cell Narrow VDC Buck-Boost Battery Charge Controller With System Power Monitor and Processor Hot Monitor

1 Features

- Pin-to-pin compatible to BQ25713
- Buck-boost narrow voltage DC (NVDC) charger for USB-C Power Delivery (PD) interface platform
  - 3.5-V to 26-V input range to charge 1- to 4-cell battery
  - Charge current up to 16.2 A/8.1 A with 128-mA/64-mA resolution based on 5-mΩ/10-mΩ sensing resistor
  - Input current limit up to 10 A/6.35 A with 100-mA/50-mA resolution based on 5-mΩ/10-mΩ sensing resistor
  - Support USB 2.0, USB 3.0, USB 3.1 and USB Power Delivery (PD)
  - Input Current Optimizer (ICO) to extract max input power without overloading the adapter
  - Integrated Fast Role Swap (FRS) feature following USB-PD specification
  - Seamless transition between buck, buck-boost, and boost operations
  - Input current and voltage regulation (IINDPM and VINDPM) against source overload
- TI patented switching frequency dithering pattern for EMI noise reduction
- TI patented Pass Through Mode (PTM) for system power efficiency improvement and battery fast charging achieving 99% efficiency.
- IMVP8/IMVP9 compliant system features for Intel platform
  - Enhanced Vmin Active Protection (VAP) mode supplements battery from input capacitors during system peak power spike following latest Intel specification
  - Comprehensive $\overline{\text{PROCHOT}}$ profile
  - Two level discharge current limit $\overline{\text{PROCHOT}}$ profile to avoid battery wire-out
  - System power monitor
- Input and battery current monitor through dedicated pins
- Integrated 8-bit ADC to monitor voltage, current and power
- Battery MOSFET ideal diode operation in supplement mode to support system when adapter is fully loaded
- Power up USB port from battery (USB OTG)
  - 3-V to 24-V OTG with 8-mV resolution
  - Output current limit up to 12.7 A/6.35 A with 100-mA/50-mA resolution based on 5-mΩ/10-mΩ sensing resistor
- 800-kHz/1.2-MHz programmable switching frequency with 2.2-µH/1.0-µH inductor
- I²C host control interface for flexible system configuration
- High accuracy for the regulation and monitor
  - ±0.5% Charge voltage regulation
  - ±3% Charge current regulation
  - ±2.5% Input current regulation
  - ±2% Input/charge current monitor
- Safety
  - Thermal shutdown
  - Input, system, battery overvoltage protection
  - Input, MOSFET, inductor overcurrent protection
- Package: 32-Pin 4.0 mm × 4.0 mm WQFN

2 Applications

- Standard notebook PC,Chromebook
- Tablet (multimedia), wireless speaker
- Ultrasound scanner, ventilators

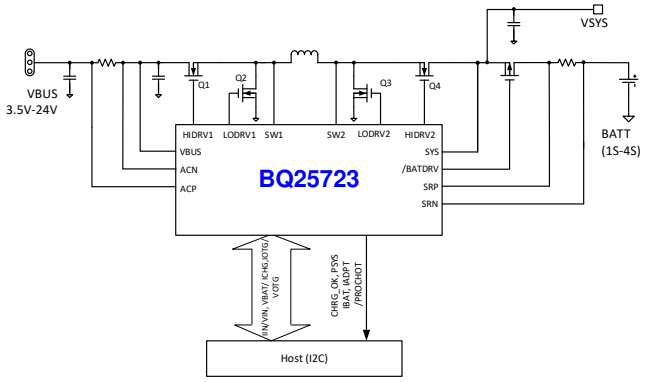
3 Description

The BQ25723 is a synchronous NVDC buck-boost battery charge controller to charge a 1- to 4-cell battery from a wide range of input sources including USB adapter, high voltage USB-C Power Delivery (PD) sources, and traditional adapters.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
BQ25723	WQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Description (continued)....3
6 Device Comparison Table....4
7 Pin Configuration and Functions....5
8 Specifications....8
8.1 Absolute Maximum Ratings....8
8.2 ESD Ratings....8
8.3 Recommended Operating Conditions....8
8.4 Thermal Information....9
8.5 Electrical Characteristics....9
8.6 Timing Requirements....20
8.7 Typical Characteristics....21
9 Detailed Description....24
9.1 Overview....24
9.2 Functional Block Diagram....25
9.3 Feature Description....26
9.4 Device Functional Modes....37
9.5 Programming....38
9.6 Register Map....43
10 Application and Implementation....86
10.1 Application Information....86
10.2 Typical Application....86
11 Power Supply Recommendations....96
12 Layout....97
12.1 Layout Guidelines....97
12.2 Layout Example....98
13 Device and Documentation Support....100
13.1 Device Support....100
13.2 Documentation Support....100
13.3 Receiving Notification of Documentation Updates....100
13.4 Support Resources....100
13.5 Trademarks....100
13.6 Electrostatic Discharge Caution....100
13.7 Glossary....100
14 Mechanical, Packaging, and Orderable Information....101

4 Revision History

DATE	REVISION	NOTES
May 2021	*	Initial release.

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5 Description (continued)

The NVDC configuration allows the system to be regulated based on battery voltage, but not drop below system minimum voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds input source rating, the battery goes into supplement mode and prevents the system from crashing.

During power up, the charger sets the converter to a buck, boost, or buck-boost configuration based on the input source and battery conditions. The charger seamlessly transitions between the buck, boost, and buck-boost operation modes without host control.

In the absence of an input source, the BQ25723 supports the USB On-the-Go (OTG) function from a 1- to 4-cell battery to generate an adjustable 3-V to 24-V output on VBUS with 8-mV resolution. The OTG output voltage transition slew rate can be configured to comply with the USB-PD 3.0 PPS specification.

When only a battery powers the system and no external load is connected to the USB OTG port, the BQ25723 implements the latest Intel Vmin Active Protection (VAP) feature, in which the device charges up the VBUS voltage from the battery to store some energy in the input decoupling capacitors. During a system peak power spike, the energy stored in the input capacitors supplements the system, to prevent the system voltage from dropping below the minimum system voltage and causing a system crash.

The BQ25723 monitors adapter current, battery current, and system power. The flexibly programmed $\overline{\text{PROCHOT}}$ output goes directly to the CPU for throttle back when needed.

The latest version of the USB-C PD specification includes Fast Role Swap (FRS) to ensure power role swapping occurs in a timely fashion so that the device(s) connected to the dock can avoid experiencing momentary power loss or glitching. This device integrates FRS in compliance with the PD specification.

TI patented switching frequency dithering pattern can significantly reduce EMI noise over the whole conductive EMI frequency range (150 kHz to 30 MHz). Multiple dithering scale options are available to provide flexibility for different applications to simplify EMI noise filter design.

The charger can be operated in the TI patented Pass Through Mode (PTM) to improve efficiency over the full load range. In PTM, input power is directly passed through the charger to the system. Switching losses of the MOSFETs and inductor core loss can be saved for high efficiency operation.

The BQ25723 is available in a 32-pin 4 mm × 4 mm WQFN package.

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6 Device Comparison Table

	BQ25710	BQ25713	BQ25720	BQ25723	BQ25730	BQ25731
Interface	SMBus	I^2C	SMBus	I^2C	I^2C	I^2C
Device Address	09h	6Bh	09h	6Bh	6Bh	6Bh
Maximum Charge Current	8.128 A	8.128 A	16.256 A	16.256 A	16.256 A	16.256 A
Switching Frequency (Hz)	800 k/1.2 M	800 k/1.2 M	800 k/1.2 M	800 k/1.2 M	400 k/800 k	400 k/800 k
Cell Count	1s to 4s	1s to 4s	1s to 4s	1s to 4s	1s to 5s	1s to 5s
Input Current Sense Resistor	10 mΩ/20 mΩ	10 mΩ/20 mΩ	5 mΩ/10 mΩ	5 mΩ/10 mΩ	5 mΩ/10 mΩ	5 mΩ/10 mΩ
Independent Comparator Latch	Non Latch	Non Latch	Latch/Non latch (default)	Latch/Non latch (default)	Latch/Non latch (default)	Latch/Non latch (default)
VSYS_UVP	2.4 V	2.4 V	2.4 V ~ 8.0 V (0.8-V step size) Default: 2.4 V	2.4 V ~ 8.0 V (0.8-V step size) Default: 2.4 V	2.4 V ~ 8.0 V (0.8-V step size) Default: 2.4 V	1.6 V
OTG Voltage Range	3.0 V to 20.8 V	3.0 V to 20.8 V	3.0 V to 24 V	3.0 V to 24 V	3.0 V to 24 V	3.0 V to 24 V
Frequency Dithering	No	No	Yes	Yes	Yes	Yes
BATFET Power Path	Yes	Yes	Yes	Yes	Yes	No
Pre-charge LDO Mode	Yes	Yes	Yes	Yes	Yes	No

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7 Pin Configuration and Functions

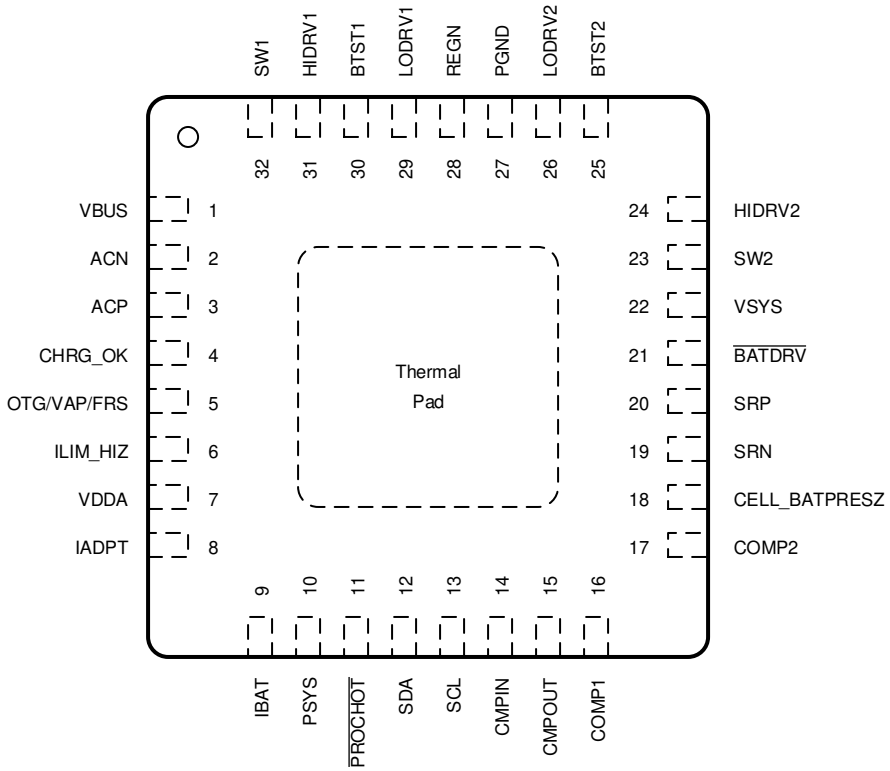

Figure 7-1. RSN Package 32-Pin WQFN Top View

Table 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
ACN	2	PWR	Input current sense amplifier negative input. The leakage on ACP and ACN are matched. A RC low-pass filter is required to be placed between the sense resistor and the ACN pin to suppress the high frequency noise in the input current signal. Refer to Section 10.2.2.1 for ACP/ACN filter design.
ACP	3	PWR	Input current sense amplifier positive input. The leakage on ACP and ACN are matched. A RC low-pass filter is required to be placed between the sense resistor and the ACP pin to suppress the high frequency noise in the input current signal. Refer to Section 10.2.2.1 for ACP/ACN filter design.
$\overline{\text{BATDRV}}$	21	O	P-channel battery FET (BATFET) gate driver output. It is shorted to VSYS to turn off the BATFET. It goes 10 V below VSYS to fully turn on BATFET. BATFET is in linear mode to regulate VSYS at minimum system voltage when battery is depleted. BATFET is fully on during fast charge and works as an ideal-diode in supplement mode.
BTST1	30	PWR	Buck mode high-side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW1 and BTST1. The bootstrap diode between REGN and BTST1 is integrated.
BTST2	25	PWR	Boost mode high-side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW2 and BTST2. The bootstrap diode between REGN and BTST2 is integrated.
CELL_BATPRESZ	18	I	Battery cell selection pin for 1- to 4- cell battery setting. CELL_BATPRESZ pin is biased from VDDA through a resistor divider. CELL_BATPRESZ pin also sets SYSOVP thresholds to 5 V for 1-cell, 12 V for 2-cell and 19.5 V for 3-cell/4-cell. CELL_BATPRESZ pin is pulled below $V_{CELL_BATPRESZ_FALL}$ to indicate battery removal. After battery is removed the charge voltage register REG0x05/04h() goes back to default. No external cap is allowed at CELL_BATPRESZ pin. The device exits LEARN mode and disables charge when CELL_BATPRESZ pin is pulled low (upon battery removal).

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Table 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CHRG_OK	4	O	Open drain active high indicator to inform the system good power source is connected to the charger input. Connect to the pullup rail via 10-kΩ resistor. When VBUS rises above 3.5 V and falls below 25.8 V, CHRG_OK is HIGH after 50-ms deglitch time. When VBUS falls below 3.2 V or rises above 26.8 V, CHRG_OK is LOW. When one of SYSOVP, SYSUVP, ACOC, TSHUT, BATOVP, BATOC or force converter off faults occurs, CHRG_OK is asserted LOW.
CMPIN	14	I	Input of independent comparator. The independent comparator compares the voltage sensed on CMPIN pin with internal reference, and its output is on CMPOUT pin. Internal reference, output polarity and deglitch time is selectable by the host. With polarity HIGH (CMP_POL = 1b), place a resistor between CMPIN and CMPOUT to program hysteresis. With polarity LOW (CMP_POL = 0b), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN to ground.
CMPOUT	15	O	Open-drain output of independent comparator. Place a pullup resistor from CMPOUT to pullup supply rail. Internal reference, output polarity and deglitch time are selectable by the host. If the independent comparator is not in use, float CMPOUT pin.
COMP2	17	I	Buck boost converter compensation pin 2. Refer to Section 9.3.13 for COMP2 pin RC network.
COMP1	16	I	Buck boost converter compensation pin 1. Refer to Section 9.3.13 for COMP1 pin RC network.
OTG/VAP/FRS	5	I	Active HIGH to enable OTG, VAP or FRS modes. 1) When OTG_VAP_MODE=1b and EN_OTG=1b, pulling high this pin can enable OTG mode. 2) When OTG_VAP_MODE=1b and EN_FRS=1b, pulling high this pin can enable FRS mode in forward operation. 3) When OTG_VAP_MODE=0b, pulling high OTG/VAP/FRS pin is to enable VAP mode.
HIDRV1	31	O	Buck mode high-side power MOSFET (Q1) driver. Connect to high-side n-channel MOSFET gate.
HIDRV2	24	O	Boost mode high-side power MOSFET(Q4) driver. Connect to high-side n-channel MOSFET gate.
IADPT	8	O	The adapter current monitoring output pin. V_{IADPT} = 20 or 40 × (V_{ACP} – V_{ACN}) with ratio selectable through IADPT_GAIN bit. This pin is also used to program the inductance used in the application. Refer to Section 9.3.12 for selecting resistor from the IADPT pin to ground . For a 2.2-µH inductance, the resistor is 137 kΩ. Place a 100-pF or less ceramic decoupling capacitor from IADPT pin to ground. IADPT output voltage is clamped below 3.3 V.
IBAT	9	O	The battery current monitoring output pin. V_{IBAT} = 8 or 16 × (V_{SRP} – V_{SRN}) for charge current, or V_{IBAT} = 8 or 16 × (V_{SRN} – V_{SRP}) for discharge current, with ratio selectable through IBAT_GAIN bit. Place a 100-pF or less ceramic decoupling capacitor from IBAT pin to ground. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V.
ILIM_HIZ	6	I	Input current limit setting pin. Program ILIM_HIZ voltage by connecting a resistor divider from VDDA rail to ground. The pin voltage is calculated as: $V_{(ILIM_HIZ)}$ = 1 V + 40 × IDPM × Rac, in which IDPM is the target input current limit. When EN_EXTILIM = 1b the input current limit used by the charger is the lower setting of ILIM_HIZ pin and IIN_HOST register. When EN_EXTILIM = 0b input current limit is only determined by IIN_HOST register. When the pin voltage is below 0.4 V, the device enters high impedance (HIZ) mode with low quiescent current. When the pin voltage is above 0.8 V, the device is out of HIZ mode. The ILIM_HIZ pin voltage is continuous read and used for updating current limit setting (If EN_EXTILIM=1b), this allows dynamic change input current limit setting by adjusting this pin voltage.
LODRV1	29	O	Buck mode low side power MOSFET (Q2) driver. Connect to low side n-channel MOSFET gate.
LODRV2	26	O	Boost mode low side power MOSFET (Q3) driver. Connect to low side n-channel MOSFET gate.
PGND	27	GND	Device power ground.
$\overline{\text{PROCHOT}}$	11	O	Active low open drain output indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the $\overline{\text{PROCHOT}}$ profile is triggered, a pulse is asserted. The minimum pulse width is adjustable through PROCHOT_WIDTH bits.

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Table 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
PSYS	10	O	Current mode system power monitor. The output current is proportional to the total power from the adapter and the battery. The gain is selectable through . Place a resistor from PSYS to ground to generate output voltage. This pin can be floating if not in use. Its output voltage is clamped at 3.3 V. Place a capacitor in parallel with the resistor for filtering.
REGN	28	PWR	6-V linear regulator output supplied from VBUS or VSYS. The LDO is active when VBUS above V_{VBUS_CONVEN}. Connect a 2.2- or 3.3-μF ceramic capacitor from REGN to power ground. REGN pin output is for power stage gate drive.
SCL	13	I	clock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to specifications.
SDA	12	I/O	open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to specifications.
SRN	19	PWR	Charge current sense amplifier negative input. SRN pin is for battery voltage sensing as well. Connect a 0.1-μF filter cap cross battery charging sensing resistor and use 10-Ω contact resistor between SRN pin and battery charging sensing resistor. The leakage current on SRP and SRN are matched.
SRP	20	PWR	Charge current sense amplifier positive input. Connect a 0.1-μF filter cap cross battery charging sensing resistor and use 10-Ω contact resistor between SRP pin and battery charging sensing resistor. The leakage current on SRP and SRN are matched.
SW1	32	PWR	Buck mode switching node. Connect to the source of the buck half bridge high side n-channel MOSFET.
SW2	23	PWR	Boost mode switching node. Connect to the source of the boost half bridge high side n-channel MOSFET.
VBUS	1	PWR	Charger input voltage. An input low pass filter of 1 Ω and 0.47 μF (minimum) is recommended.
VDDA	7	PWR	Internal reference bias pin. Connect a 10-Ω resistor from REGN to VDDA and a 1-μF ceramic capacitor from VDDA to power ground.
VSYS	22	PWR	Charger system voltage sensing. The system voltage regulation maximum limit is programmed in ChargeVoltage register plus 150 mV and regulation minimum limit is programmed in VSYS_MIN register.
Thermal pad	–	–	Exposed pad beneath the IC. Always solder thermal pad to the board, and have vias on the thermal pad plane connecting to power ground planes. It serves as a thermal pad to dissipate the heat.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	SRN, SRP, ACN, ACP, VBUS, VSYS	–0.3	32	V
	SW1, SW2	–2	32	
	BTST1, BTST2, HIDRV1, HIDRV2, $\overline{\text{BATDRV}}$	–0.3	38	
	LODRV1, LODRV2 (25nS)	–4	7	
	HIDRV1, HIDRV2 (25nS)	–4	38	
	SW1, SW2 (25nS)	–4	32	
	SDA, SCL, REGN, PSYS, CHRG_OK, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP2, CMPIN, CMPOUT,OTG/VAP/FRS,	–0.3	7	
	$\overline{\text{PROCHOT}}$	–0.3	5.5	
	IADPT, IBAT, COMP1	–0.3	3.6	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	–0.3	7	V
	SRP-SRN, ACP-ACN	–0.5	0.5	
Temperature	Junction temperature range, T_J	–40	150	°C
Temperature	Storage temperature, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	ACN, ACP, VBUS	0		26	V
	SRN, SRP, VSYS	0		19.2	
	SW1, SW2	–2		26	
	BTST1, BTST2, HIDRV1, HIDRV2, $\overline{\text{BATDRV}}$	0		32	
	SDA, SCL, REGN, PSYS, CHRG_OK, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP2, CMPIN, CMPOUT,OTG/VAP/FRS	0		6.5	
	$\overline{\text{PROCHOT}}$	0		5.3	
	IADPT, IBAT, COMP1	0		3.3	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	0		6.5	V
	SRP-SRN, ACP-ACN	–0.5		0.5	
	BATDRV-VSYS	0		10.8	

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8.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature	Junction temperature range, T_J	–20		125	°C
	Storage temperature, T_{stg}	–20		85	

8.4 Thermal Information

THERMAL METRIC[1]		BQ25723 RSN (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INPUT_OP}	Input voltage operating range		3.5		26	V
MAX SYSTEM VOLTAGE REGULATION						
V_{SYSMAX_RNG}	System Voltage Regulation, measured on V_{SYS} (charge disabled)		1.024		19.2	V
V_{SYSMAX_ACC}	System voltage regulation accuracy (charge disabled and EN_OOA=0b)	REG0x05/04() = 0x41A0H (16.800 V)		V_{SRN} + 150 mV		V
			–2%		2%	
		REG0x05/04() = 0x3138H (12.600 V)		V_{SRN} + 150 mV		V
			–2%		2%	
		REG0x05/04() = 0x20D0H (8.400 V)		V_{SRN} + 150 mV		V
			–3%		3%	
		REG0x05/04() = 0x1068H (4.200 V)		V_{SRN} + 150 mV		V
			–3%		3%	
MINIMUM SYSTEM VOLTAGE REGULATION						
$V_{SYS_MIN_RNG}$	System Voltage Regulation, measured on V_{SYS}		1.00		19.2	V

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SYS_MIN_REG_ACC}$	Minimum System Voltage Regulation Accuracy (VBAT below REG0x0D/0C() setting, EN_OOA=0b)	REG0x0D/0C() = 0x7B00H		12.30		V
			–2%		–2%	
		REG0x0D/0C() = 0x5C00H		9.20		V
			–2%		–2%	
		REG0x0D/0C() = 0x4200H		6.60		V
			–3%		–3%	
		REG0x0D/0C() = 0x2400H		3.60		V
			–3%		–3%	
CHARGE VOLTAGE REGULATION						
V_{BAT_RNG}	Battery voltage regulation		1.024		19.2	V
$V_{BAT_REG_ACC}$	Battery voltage regulation accuracy (charge enable) (0°C to 85°C)	REG0x05/04() = 0x41A0H		16.8		V
			–0.5%		0.5%	
		REG0x05/04() = 0x3138H		12.6		V
			–0.5%		0.5%	
		REG0x05/04() = 0x20D0H		8.4		V
			–0.6%		0.6%	
		REG0x05/04() = 0x1068H		4.2		V
			–1.1%		1.2%	
CHARGE CURRENT REGULATION IN FAST CHARGE						
$V_{IREG_CHG_RNG}$	Charge current regulation differential voltage range	V_{IREG_CHG} = V_{SRP} – V_{SRN}	0		81.28	mV
$I_{CHRG_REG_ACC}$	Charge current regulation accuracy 10-mΩ sensing resistor, VBAT above 0x0D/0C() setting (0°C to 85°C)	REG0x03/02() = 0x1000H		4096		mA
			–3.0%		2.0%	
		REG0x03/02() = 0x0800H		2048		mA
			–4.0%		3.0%	
		REG0x03/02() = 0x0400H		1024		mA
			–5.0%		6.0%	
		REG0x03/02() = 0x0200H		512		mA
			–12.0%		12.0%	
CHARGE CURRENT REGULATION IN LDO MODE						
I_{CLAMP}	Pre-charge current clamp	CELL(≥2 S) VSRN < VSYS_MIN		384		mA
		CELL 1 S, VSRN < 3 V		384		mA
		CELL 1 S, 3 V < VSRN < VSYS_MIN		2		A

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PRECHRG_REG_ACC}$	Pre-charge current regulation accuracy with 10-mΩ SRP/SRN series resistor, VBAT below VSYS_MIN(REG0x0D/0C()) setting (0°C to 85°C)	REG0x03/02() = 0x0180H		384		mA
		≥2S	–15.0%		15.0%	
		1S	–25.0%		25.0%	
		REG0x03/02() = 0x0100H		256		mA
		≥2S	–20.0%		20.0%	
		1S	–35.0%		35.0%	
		REG0x03/02() = 0x00C0H		192		mA
		≥2S	–25.0%		25.0%	
		1S	–50.0%		50.0%	
		REG0x03/02() = 0x0080H		128		mA
		≥2S	–30.0%		30.0%	
$I_{LEAK_SRP_SRN}$	SRP, SRN leakage current mismatch (0°C to 85°C)		–13.5		10.0	µA
INPUT CURRENT REGULATION						
$V_{IREG_DPM_RNG}$	Input current regulation differential voltage range with 10-mΩ ACP/ACN series resistor	V_{IREG_DPM} = V_{ACP} – V_{ACN}	0.5		64	mV
$I_{IIN_DPM_REG_ACC}$	Input current regulation accuracy (-40°C to 105°C) with 10-mΩ ACP/ACN series resistor	REG0x0F/0E() = 0x4E00H	3800	3900	4000	mA
		REG0x0F/0E() = 0x3A00H	2800	2900	3000	mA
		REG0x0F/0E() = 0x1C00H	1300	1400	1500	mA
		REG0x0F/0E() = 0x0800H	300	400	500	mA
$I_{LEAK_ACP_ACN}$	ACP, ACN leakage current mismatch		–21		10	µA
$V_{IREG_DPM_RNG_ILIM}$	Voltage range for input current regulation (ILIM_HIZ Pin)		1.15		4	V
$I_{IIN_DPM_REG_ACC_ILIM}$	Input Current Regulation Accuracy on ILIM_HIZ pin V_{ILIM_HIZ} = 1 V + 40 × I_{DPM} × R_{AC}, with 10-mΩ ACP/ACN series resistor	V_{ILIM_HIZ} = 2.6 V	3800	4000	4200	mA
		V_{ILIM_HIZ} = 2.2 V	2800	3000	3200	mA
		V_{ILIM_HIZ} = 1.6 V	1300	1500	1700	mA
		V_{ILIM_HIZ} = 1.2 V	300	500	700	mA
I_{LEAK_ILIM}	ILIM_HIZ pin leakage current		–1		1	µA
INPUT VOLTAGE REGULATION						
V_{DPM_RNG}	Input voltage regulation range	Voltage on VBUS	3.2		19.52	V
$V_{DPM_REG_ACC}$	Input voltage regulation accuracy	REG0x0B/0A()=0x3C80H		18688		mV
			–3%		2%	
		REG0x0B/0A()=0x1E00H		10880		mV
			–4%		2.5%	
		REG0x0B/0A()=0x0500H		4480		mV
					5.0%	
OTG CURRENT REGULATION						

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8.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IOTG_REG_RNG}$	OTG output current regulation differential voltage range	$V_{IOTG_REG} = V_{ACP} – V_{ACN}$	0		81.28	mV
I_{OTG_ACC}	OTG output current regulation accuracy with 50-mA LSB and 10-mΩ ACP/ACN series resistor	REG0x09/08() = 0x3C00H	2800	3000	3200	mA
		REG0x09/08() = 0x1E00H	1300	1500	1700	mA
		REG0x09/08() = 0x0A00H	300	500	700	mA
OTG VOLTAGE REGULATION						
$V_{OTG_REG_RNG}$	OTG voltage regulation range(OOA disabled)	Voltage on VBUS	3		24.00	V
$V_{OTG_REG_ACC}$	OTG voltage regulation accuracy(OOA disabled)	REG0x07/06()=0x2CEC		23.00		V
			–2%		2%	
		REG0x07/06()=0x1770H		12.00		V
			–2%		2%	
		REG0x07/06()=0x09C4H		5.00		V
			–3%		3%	
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage (0 mA – 60 mA)	V_{VBUS} = 10 V	5.7	6	6.3	V
$V_{DROPOUT}$	REGN voltage in drop out mode	V_{VBUS} = 5 V, I_{LOAD} = 20 mA	3.8	4.3	4.6	V
$I_{REGN_LIM_Charging}$	REGN current limit when converter is enabled	V_{VBUS} = 10 V, force V_{REGN} =4 V	50	65		mA
QUIESCENT CURRENT						
$I_{BAT_BATFET_ON}$	System powered by battery. BATFET on. $I_{SRN} + I_{SRP} + I_{SW2} + I_{BTST2} + I_{SW1} + I_{BTST1} + I_{ACP} + I_{ACN} + I_{VBUS} + I_{VSYS}$	VBAT = 18 V, REG0x01[7] = 1,REG0x31[6] = 0b, in low-power mode, Disable PSYS		22	45	µA
		VBAT = 18 V, REG0x01[7] = 1, REG0x31[6] = 1b, REG0x31[5:4] = 11b,REGN off, Disable PSYS, Enable low power $\overline{\text{PROCHOT}}$		35	60	µA
		VBAT = 18 V, REG0x01[7]= 0,REG0x31[5:4]= 11b, REGN on, Disable PSYS, In performance mode		880	1170	µA
		VBAT = 18 V, REG0x01[7] = 0, REG0x31[5:4] = 00b, REGN on, Enable PSYS, In performance mode		980	1270	µA
$I_{AC_SW_LIGHT_buck}$	Input current during PFM in buck mode, no load, $I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST} + I_{SW2} + I_{BTST2}$	VIN = 20 V, VBAT = 12.6 V, 3s, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.2		mA
$I_{AC_SW_LIGHT_boost}$	Input current during PFM in boost mode, no load, $I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}$	VIN = 5 V, VBAT = 8.4 V, 2s, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.7		mA

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{AC_SW_LIGHT_buckboost}$	Input current during PFM in buck boost mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	VIN = 12 V, VBAT = 12 V, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.4		mA
$I_{OTG_STANDBY}$	Quiescent current during PFM in OTG mode I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}	VBAT = 8.4 V, VBUS = 5 V, 800 kHz switching frequency, MOSFET Qg = 4nC		3		mA
		VBAT = 8.4 V, VBUS = 12 V, 800 kHz switching frequency, MOSFET Qg = 4nC		4.2		mA
		VBAT = 8.4 V, VBUS = 20 V, 800 kHz switching frequency, MOSFET Qg = 4nC		6.2		mA
CURRENT SENSE AMPLIFIER						
$V_{ACP_ACN_OP}$	Input common mode range	Voltage on ACP/ACN	3.8		26	V
V_{IADPT_CLAMP}	I_{ADPT} output clamp voltage		3.1	3.2	3.3	V
I_{IADPT}	I_{ADPT} output current				1	mA
A_{IADPT}	Input current sensing gain	$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x00[4] = 0		20		V/V
		$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x00[4] = 1		40		V/V
V_{IADPT_ACC}	Input current monitor accuracy	$V_{(ACP-ACN)}$ = 40.96 mV	–2%		2%	
		$V_{(ACP-ACN)}$ = 20.48 mV	–3%		3%	
		$V_{(ACP-ACN)}$ =10.24 mV	–6%		6%	
		$V_{(ACP-ACN)}$ = 5.12 mV	–10%		10%	
C_{IADPT_MAX}	Maximum capacitance at IADPT Pin				100	pF
$V_{SRP_SRN_OP}$	Battery common mode range	Voltage on SRP/SRN	2.5		19.2	V
V_{IBAT_CLAMP}	IBAT output clamp voltage		3.05	3.2	3.3	V
I_{IBAT}	IBAT output current				1	mA
A_{IBAT}	Charge and discharge current sensing gain on IBAT pin	$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x00[3] = 0,		8		V/V
		$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x00[3] = 1,		16		V/V
$I_{IBAT_CHG_ACC}$	Charge and discharge current monitor accuracy on IBAT pin	$V_{(SRN-SRP)}$ = 40.96 mV	–2%		2%	
		$V_{(SRN-SRP)}$ = 20.48 mV	–4%		4%	
		$V_{(SRN-SRP)}$ =10.24 mV	–7%		7%	
		$V_{(SRN-SRP)}$ = 5.12 mV	–15%		15%	
C_{IBAT_MAX}	Maximum capacitance at IBAT Pin				100	pF
SYSTEM POWER SENSE AMPLIFIER						
V_{PSYS}	PSYS output voltage range		0		3.3	V
I_{PSYS}	PSYS output current		0		160	µA
A_{PSYS}	PSYS system gain	$I_{(PSYS)}$ / ($P_{(IN)}$ +$P_{(BAT)}$), REG0x31[5:4] = 00b;REG0x31[1] = 1b		1		µA/W
A_{PSYS}	PSYS system gain	$I_{(PSYS)}$ / $P_{(IN)}$, REG0x31[5:4]= 01b;REG0x31[1] = 1b		1		µA/W

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PSYS_ACC}	PSYS gain accuracy (REG0x30[13:12] = 00b)	Adapter only with system power = 19.5 V / 45 W, TA = 0 to 85°C	–4%		4%	
		Battery only with system power = 11 V / 44 W, TA = 0 to 85°C	–3%		3%	
	PSYS gain accuracy (REG0x30[13:12] = 01b)	Adapter only with system power = 19.5 V / 45 W, TA = 0 to 85°C	–4%		4%	
V_{PSYS_CLAMP}	PSYS clamp voltage		3		3.3	V
VMIN ACTIVE PROTECTION(VAP) PROCHOT COMPARATOR						
V_{SYS_TH1Z}	VAP VSYS rising threshold 1	VSYS_TH1 rising	6.4	6.6	6.75	V
V_{SYS_TH1}	VAP VSYS falling threshold 1	VSYS_TH1 falling REG36<7:2>=100010b	6.3	6.5	6.65	V
$V_{SYS_TH1_HYST}$	VAP VSYS threshold 1 hysteresis			100		mV
$t_{SYS_TH1_falling_DEG}$	VSYS threshold 1 falling deglitch for VAP shooting			4		us
V_{SYS_TH2Z}	VAP VSYS rising threshold 2	VSYS_TH2 rising	6.1	6.3	6.45	V
V_{SYS_TH2}	VAP VSYS falling threshold 2	VSYS_TH2 falling REG3E<7:2>=011111b	6.0	6.2	6.35	V
$V_{SYS_TH2_HYST}$	VAP VSYS threshold 2 hysteresis			100		mV
$t_{SYS_TH2_falling_DEG}$	VSYS threshold 2 falling deglitch for throttling			4		us
$V_{BUS_VAP_THZ}$	VAP mode VBUS rising threshold	VBUS_VAP_TH rising	3.15	3.35	3.50	V
$V_{BUS_VAP_TH}$	VAP mode VBUS falling threshold	VBUS_VAP_TH falling REG3F<7:1>=0000000b	3.0	3.2	3.35	V
$V_{BUS_VAP_TH_HYST}$	VAP mode VBUS threshold hysteresis			150		mV
$t_{BUS_VAP_TH_falling_DEG}$	VBUS falling deglitch for throttling			4		us
VSYS UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{SYS_UVLOZ}	VSYS undervoltage rising threshold(≥1S)	VSYS rising	2.3	2.5	2.65	V
V_{SYS_UVLO}	VSYS undervoltage falling threshold(≥1S)	VSYS falling REG3D<7:5>=000b	2.2	2.4	2.55	V
$V_{SYS_UVLO_HYST}$	VSYS undervoltage hysteresis(≥1S)			100		mV
VBUS UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBUS_UVLOZ}	VBUS undervoltage rising threshold	VBUS rising	2.35	2.55	2.80	V
V_{VBUS_UVLO}	VBUS undervoltage falling threshold	VBUS falling	2.2	2.4	2.6	V
$V_{VBUS_UVLO_HYST}$	VBUS undervoltage hysteresis			150		mV
V_{VBUS_CONVEN}	VBUS converter enable rising threshold	VBUS rising	3.2	3.5	3.9	V

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VBUS_CONVENZ}$	VBUS converter enable falling threshold	VBUS falling	2.9	3.2	3.5	V
$V_{VBUS_CONVEN_HYST}$	VBUS converter enable hysteresis			300		mV
BATTERY UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBAT_UVLOZ}	VBAT undervoltage rising threshold	VSRN rising	2.35	2.55	2.80	V
V_{VBAT_UVLO}	VBAT undervoltage falling threshold	VSRN falling	2.2	2.4	2.6	V
$V_{VBAT_UVLO_HYST}$	VBAT undervoltage hysteresis			150		mV
V_{VBAT_OTGEN}	VBAT OTG enable rising threshold	VSRN rising	3.25	3.55	3.85	V
V_{VBAT_OTGENZ}	VBAT OTG enable falling threshold	VSRN falling	2.15	2.4	2.65	V
$V_{VBAT_OTGEN_HYST}$	VBAT OTG enable hysteresis			1150		mV
VBUS UNDER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS_OTG_UV}$	VBUS undervoltage falling threshold	As percentage of REG0x07/06()		85%		
$t_{VBUS_OTG_UV}$	VBUS time undervoltage deglitch			7		ms
VBUS OVER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS_OTG_OV}$	VBUS overvoltage rising threshold	As percentage of REG0x07/06()		110%		
$t_{VBUS_OTG_OV}$	VBUS Time Overvoltage Deglitch			10		ms
PRE-CHARGE to FAST CHARGE TRANSITION(For ≥2S)						
$V_{BAT_VSYS_MIN_RISE}$	LDO mode to fast charge mode threshold, VSRN rising	as percentage of 0x0D/0C()	98%	100%	102%	
$V_{BAT_VSYS_MIN_FALL}$	LDO mode to fast charge mode threshold, VSRN falling	as percentage of 0x0D/0C()		97.5%		
$V_{BAT_VSYS_MIN_HYST}$	Fast charge mode to LDO mode threshold hysteresis	as percentage of 0x0D/0C()		2.5%		
BATTERY LOWV COMPARATOR (Pre-charge to Fast Charge Threshold for 1S)						
V_{BATLV_FALL}	BATLOWV falling threshold			2.8		V
V_{BATLV_RISE}	BATLOWV rising threshold			3		V
V_{BATLV_RHYST}	BATLOWV hysteresis			200		mV
INPUT OVER-VOLTAGE COMPARATOR (ACOV)						
V_{ACOV_RISE}	VBUS overvoltage rising threshold	VBUS rising	26.0	26.8	27.7	V
V_{ACOV_FALL}	VBUS overvoltage falling threshold	VBUS falling	25.0	25.8	26.7	V

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ACOV_HYST}	VBUS overvoltage hysteresis			1.0		V
$t_{ACOV_RISE_DEG}$	VBUS deglitch overvoltage rising	VBUS converter rising to stop converter		100		us
$t_{ACOV_FALL_DEG}$	VBUS deglitch overvoltage falling	VBUS converter falling to start converter		1		ms
INPUT OVER CURRENT COMPARATOR (ACOC)						
V_{ACOC}	ACP to ACN rising threshold, w.r.t. ILIM2 in REG0x33[15:11]	Voltage across input sense resistor rising, Reg0x32[2]= 1	180%	200%	220%	
V_{ACOC_FLOOR}	Measure between ACP and ACN	Set IIN_DPM to minimum	44	50	56	mV
$V_{ACOC_CEILING}$	Measure between ACP and ACN	Set IIN_DPM to maximum	172	180	188	mV
$t_{ACOC_DEG_RISE}$	Rising deglitch time	Deglitch time to trigger ACOC		250		us
t_{ACOC_RELAX}	Relax time	Relax time before converter starts again		250		ms
SYSTEM OVER-VOLTAGE COMPARATOR (SYSOVP)						
V_{SYSOVP_RISE}	System overvoltage rising threshold to turnoff converter	1 s	5.8	6	6.1	V
		2 s	11.7	12	12.2	V
		3 s	19	19.5	20	V
		4 s	19	19.5	20	V
V_{SYSOVP_FALL}	System overvoltage falling threshold	1 s		5.5		V
		2 s		11.7		V
		3 s		19.3		V
		4 s		19.3		V
I_{SYSOVP}	Discharge current when SYSOVP stop switching was triggered	on VSYS pin		20		mA
BAT OVER-VOLTAGE COMPARATOR (BATOVP)						
V_{BATOVP_RISE}	Overvoltage rising threshold as percentage of VBAT_REG in REG0x15()	1 s, 4.2 V	102.5%	104%	106%	
		≥2 s	102.5%	104%	105%	
V_{BATOVP_FALL}	Overvoltage falling threshold as percentage of VBAT_REG in REG0x15()	1 s	100%	102%	104%	
		≥2 s	100%	102%	103%	
V_{BATOVP_HYST}	Overvoltage hysteresis as percentage of VBAT_REG in REG0x15()	1 s		2%		
		≥2 s		2%		
I_{BATOVP}	Discharge current during BATOVP	Discharge current through VSYS pin		40		mA
CONVERTER OVER-CURRENT COMPARATOR (Q2)						
$V_{OCP_limit_Q2}$	Converter Over-Current Limit across Q2 MOSFET drain to source voltage	Reg0x32[5]=1		150		mV
		Reg0x32[5]=0		210		mV

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OCP_limit_SYSSHORT_Q2}$	System Short or SRN < 2.4 V	Reg0x32[5]=1		45		mV
		Reg0x32[5]=0		60		mV
CONVERTER OVER-CURRENT COMPARATOR (ACX)						
$V_{OCP_limit_ACX}$	Converter Over-Current Limit across ACP-ACN input current sensing resistor	Reg0x32[4]=1; RSNS_RAC=0b		150		mV
		Reg0x32[4]=0;RSNS_RAC=0b		280		mV
$V_{OCP_limit_SYSSHORT_ACX}$	System Short or SRN < 2.4 V	Reg0x32[4]=1		90		mV
		Reg0x32[4]=0		150		mV
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT_RISE}	Thermal shutdown rising temperature	Temperature increasing		155		°C
T_{SHUTF_FALL}	Thermal shutdown falling temperature	Temperature reducing		135		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			20		°C
t_{SHUT_RDEG}	Thermal deglitch shutdown rising			100		us
t_{SHUT_FHYS}	Thermal deglitch shutdown falling			12		ms
ICRIT PROCHOT COMPARATOR						
I_{ICRIT_PRO}	Input current rising threshold for throttling as 10% above ILIM2 (REG0x33[15:11])	Only when ILIM2 setting is higher than 2A	105%	110%	117%	
INOM PROCHOT COMPARATOR						
I_{INOM_PRO}	INOM rising threshold as 10% above IIN_DPM (REG0x22[15:8])		105%	110%	116%	
BATTERY DISCHARGE CURRENT LIMIT PROCHOT COMPARATOR(IDCHG)						
I_{DCHG_TH1}	IDCHG threshold1 for throttling CPU	Reg0x39<7:2>=010000b, with 10mΩ SRP/SRN current sensing resistor		8192		mA
			96%		103%	
I_{DCHG_DEG1}	IDCHG threshold1 deglitch time	Reg0x39h<1:0>=01b		1.25		sec
I_{DCHG_TH2}	IDCHG threshold2 for throttling CPU	Reg0x39<7:2>=010000b 3C<5:3>=001b,with 10mΩ SRP/SRN current sensing resistor		12288		mA
			96%		103%	
t_{DCHG_DEG2}	IDCHG threshold2 deglitch time	Reg0x3C<7:6>=01b		1.6		ms
INDEPENDENT COMPARATOR						
V_{INDEP_CMP}	Independent comparator threshold	Reg0x30h<7>= 1, CMPIN falling	1.17	1.2	1.23	V
		Reg0x30h<7>= 0, CMPIN falling	2.27	2.3	2.33	V
$V_{INDEP_CMP_HYS}$	Independent comparator hysteresis	CMPIN falling		100		mV
POWER MOSFET DRIVER						
PWM OSCILLATOR AND RAMP						
F_{SW}	PWM switching frequency	Reg0x01[1] = 0	1020	1200	1380	kHz

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW}	PWM switching frequency	Reg0x01[1] = 1	680	800	920	kHz
BATFET GATE DRIVER (BATDRV)						
V_{BATDRV_ON}	Gate drive voltage on BATFET		8.5	10	11.5	V
V_{BATDRV_DIODE}	Drain-source voltage on BATFET during ideal diode operation			30		mV
R_{BATDRV_ON}	Measured by sourcing 10 µA current to BATDRV		3	4	6	kΩ
R_{BATDRV_OFF}	Measured by sinking 10 µA current from BATDRV			1.2	2.1	kΩ
PWM HIGH SIDE DRIVER (HIDRV Q1)						
$R_{DS_HI_ON_Q1}$	High-side driver (HSD) turnon resistance	V_{BTST1} - V_{SW1} = 5 V		6		Ω
$R_{DS_HI_OFF_Q1}$	High-side driver turnoff resistance	V_{BTST1} - V_{SW1} = 5 V		1.3	2.2	Ω
$V_{BTST1_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST1} - V_{SW1} when low-side refresh pulse is requested	3.2	3.7	4.6	V
PWM HIGH SIDE DRIVER (HIDRV Q4)						
$R_{DS_HI_ON_Q4}$	High-side driver (HSD) turnon resistance	V_{BTST2} - V_{SW2} = 5 V		6		Ω
$R_{DS_HI_OFF_Q4}$	High-side driver turnoff resistance	V_{BTST2} - V_{SW2} = 5 V		1.5	2.4	Ω
$V_{BTST2_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST2} - V_{SW2} when low-side refresh pulse is requested	3.3	3.7	4.6	V
PWM LOW SIDE DRIVER (LODRV Q2)						
$R_{DS_LO_ON_Q2}$	Low-side driver (LSD) turnon resistance	V_{BTST1} - V_{SW1} = 5.5 V		6		Ω
$R_{DS_LO_OFF_Q2}$	Low-side driver turnoff resistance	V_{BTST1} - V_{SW1} = 5.5 V		1.7	2.6	Ω
PWM LOW SIDE DRIVER (LODRV Q3)						
$R_{DS_LO_ON_Q3}$	Low-side driver (LSD) turnon resistance	V_{BTST2} - V_{SW2} = 5.5 V		7.6		Ω
$R_{DS_LO_OFF_Q3}$	Low-side driver turnoff resistance	V_{BTST2} - V_{SW2} = 5.5 V		2.9	4.6	Ω
INTERNAL SOFT START During Charge Enable						
SS_{STEP_SIZE}	Charge current soft-start step size			64		mA
SS_{STEP_TIME}	Charge current soft-start duration time for each step			8		us
INTEGRATED BTST DIODE (D1)						
V_{F_D1}	Forward bias voltage	IF = 20 mA at 25°C		0.8		V
V_{R_D1}	Reverse breakdown voltage	IR = 2 µA at 25°C			20	V

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTEGRATED BTST DIODE (D2)						
V_{F_D2}	Forward bias voltage	IF = 20 mA at 25°C		0.8		V
V_{R_D2}	Reverse breakdown voltage	IR = 2 µA at 25°C			20	V
INTERFACE						
LOGIC INPUT (SDA, SCL)						
V_{IN_LO}	Input low threshold	I2C			0.4	V
V_{IN_HI}	Input high threshold	I2C	1.3			V
LOGIC OUTPUT OPEN DRAIN (SDA, CHRG_OK, CMPOUT)						
V_{OUT_LO}	Output saturation voltage	5 mA drain current			0.4	V
V_{OUT_LEAK}	Leakage current	Voltage = 7 V	–1		1	µA
LOGIC INPUT (OTG/VAP/FRS pin)						
$V_{IN_LO_OTG}$	Input low threshold				0.4	V
$V_{IN_HI_OTG}$	Input high threshold		1.3			V
LOGIC OUTPUT OPEN DRAIN SDA						
$V_{OUT_LO_SDA}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT_LEAK_SDA}$	Leakage Current	Voltage = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN CHRG_OK						
$V_{OUT_LO_CHRG_OK}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT_LEAK_CHRG_OK}$	Leakage Current	Voltage = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN CMPOUT						
$V_{OUT_LO_CMPOUT}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT_LEAK_CMPOUT}$	Leakage Current	Voltage = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN ($\overline{\text{PROCHOT}}$)						
$V_{OUT_LO_PROCHOT}$	Output saturation voltage	50 Ω pullup to 1.05 V / 5-mA			300	mV
$V_{OUT_LEAK_PROCHOT}$	Leakage current	Voltage = 5.5 V	–1		1	µA
ANALOG INPUT (ILIM_HIZ)						
V_{HIZ_LO}	Voltage to get out of HIZ mode	ILIM_HIZ pin rising	0.8			V
V_{HIZ_HIGH}	Voltage to enable HIZ mode	ILIM_HIZ pin falling			0.4	V
ANALOG INPUT (CELL_BATPRESZ)						
V_{CELL_4S}	4S setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	68.4%	75%	81.5%	
V_{CELL_3S}	3S setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	51.7%	55%	65%	
V_{CELL_2S}	2S setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	35%	40%	48.5%	
V_{CELL_1S}	1S setting	CELL_BATPRESZ pin voltage as percentage of REGN = 6 V	18.4%	25%	31.6%	
$V_{CELL_BATPRESZ_RISE}$	Battery is present	CELL_BATPRESZ rising	18%			
$V_{CELL_BATPRESZ_FALL}$	Battery is removed	CELL_BATPRESZ falling			15%	
ANALOG INPUT (COMP1, COMP2)						

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8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV_FALL}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK_COMP1}	COMP1 Leakage		–120		120	nA
I_{LEAK_COMP2}	COMP2 Leakage		–120		120	nA

8.6 Timing Requirements

		MIN	NOM	MAX	UNIT
TIMING CHARACTERISTICS					
t_r	SCL/SDA rise time			300	ns
t_f	SCL/SDA fall time			300	ns
t_{HIGH}	SCL pulse width high	0.6		50	µs
t_{LOW}	SCL pulse width low	1.3			µs
$t_{SU:STA}$	Setup time for START condition	0.6			µs
$t_{HD:STA}$	Start condition hold time after which first clock pulse is generated	0.6			µs
$t_{SU:DAT}$	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	300			ns
$t_{SU:STO}$	Set up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between START and STOP conditions	1.3			µs
f_{SCL}	Clock frequency	10		400	kHz
HOST COMMUNICATION FAILURE					
$t_{TIMEOUT}$	bus release timeout(1)	25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal	10			ms
t_{WDI}	Watchdog timeout period, REG0x01[6:5]=01	4	5.5	7	s
	Watchdog timeout period, REG0x01[6:5]=10	70	88	105	s
	Watchdog timeout period, REG0x01[6:5]=11	140	175	210	s

(1) Devices participating in a transfer timeout when any clock low exceeds the 25-ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35-ms maximum timeout period. Both a host and a target must adhere to the maximum value specified because it incorporates the cumulative stretch limit for both a host (10 ms) and a target (25 ms).

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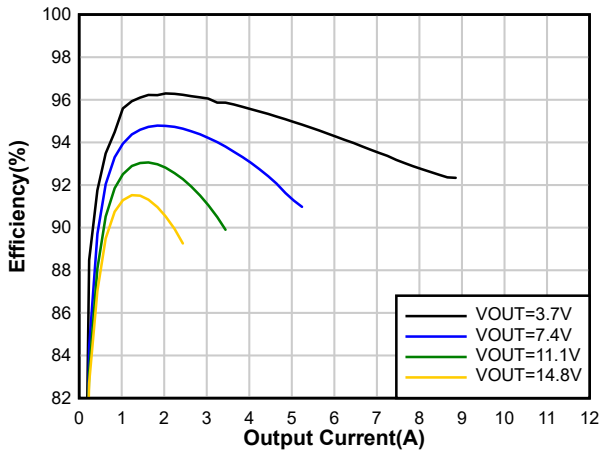
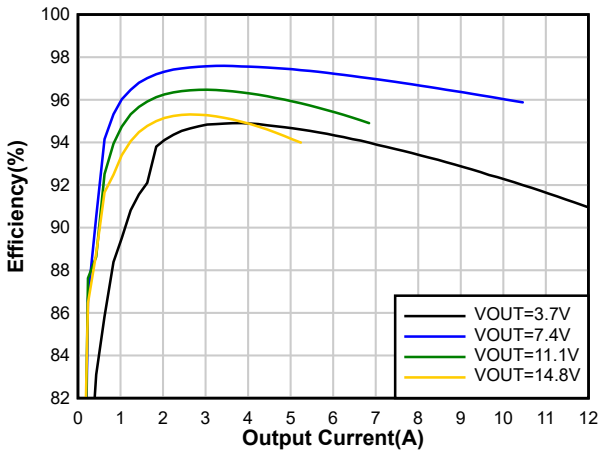
8.7 Typical Characteristics

R_{AC} = 5 mΩ, R_{SR} = 5 mΩ, Inductance = 2.2 µH, CCM Frequency = 800 kHz



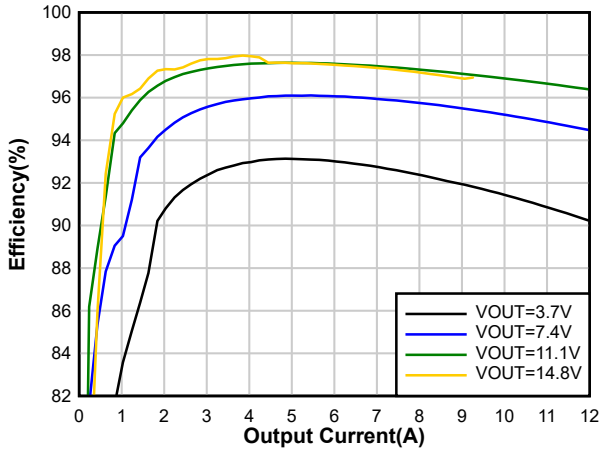
VIN = 5 V CCM 800 kHz VOUT = System voltage

Figure 8-1. System Efficiency



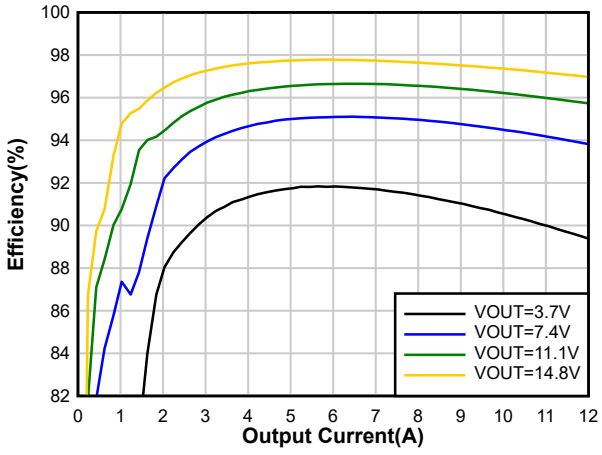
VIN = 9 V CCM 800 kHz VOUT = System voltage

Figure 8-2. System Efficiency



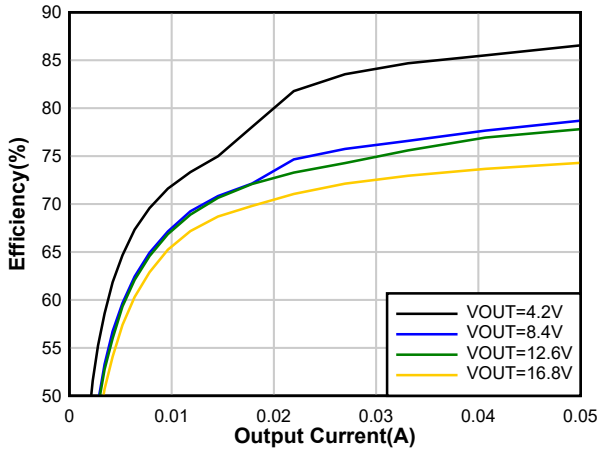
VIN = 15 V CCM 800 kHz VOUT = System voltage

Figure 8-3. System Efficiency



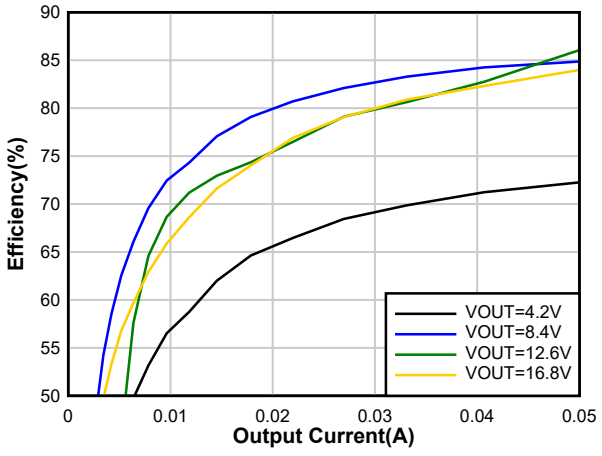
VIN = 20 V CCM 800 kHz VOUT = System voltage

Figure 8-4. System Efficiency



VIN = 5 V EN_OOA = 0b VOUT = System voltage

Figure 8-5. Light Load System Efficiency



VIN = 12 V EN_OOA = 0b VOUT = System voltage

Figure 8-6. Light Load System Efficiency

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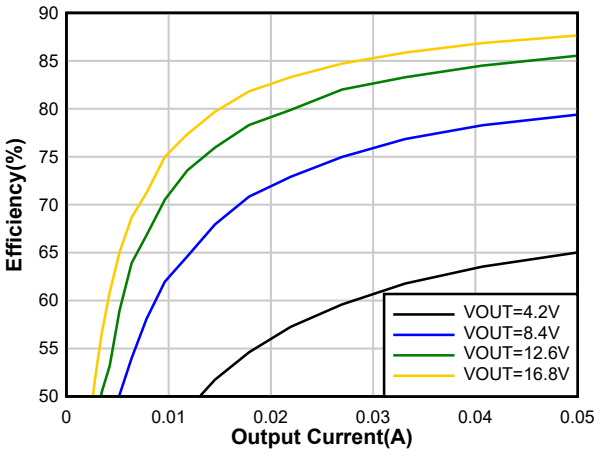
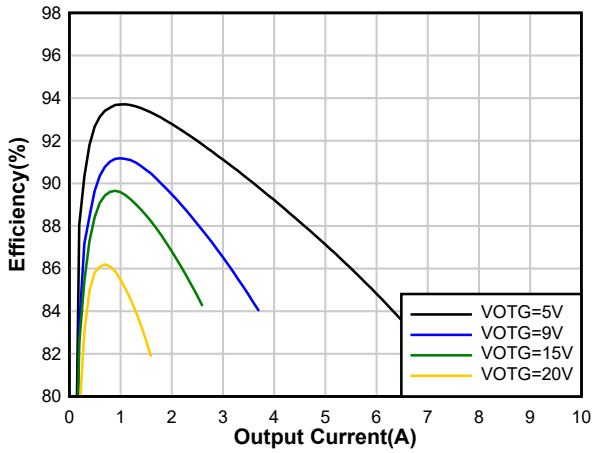
8.7 Typical Characteristics (continued)



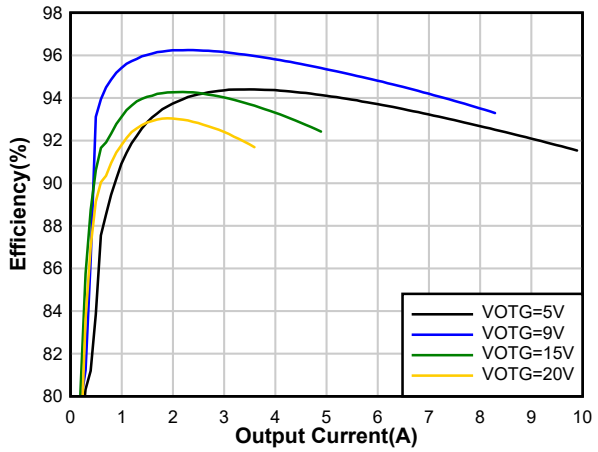
VIN = 20 V EN_OOA = 0b VOUT = System voltage

Figure 8-7. Light Load System Efficiency



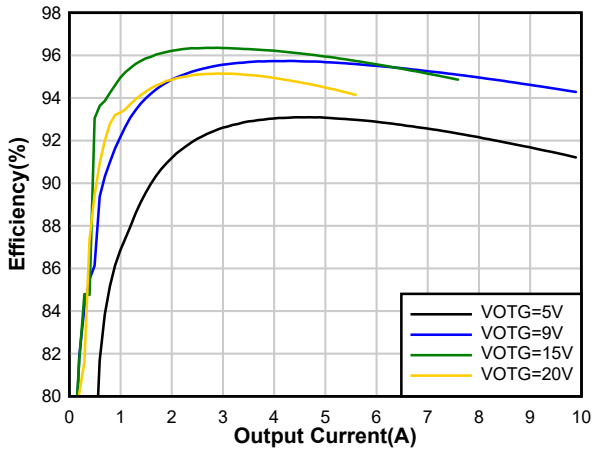
VBAT = 4 V CCM 800 kHz

Figure 8-8. OTG Efficiency with 1S Battery



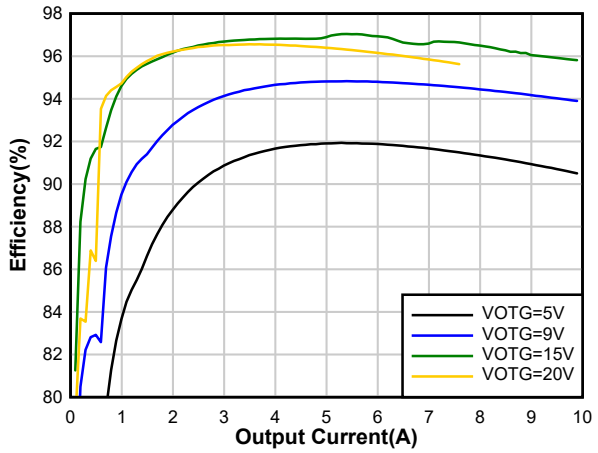
VBAT = 8 V CCM 800 kHz

Figure 8-9. OTG Efficiency with 2S Battery



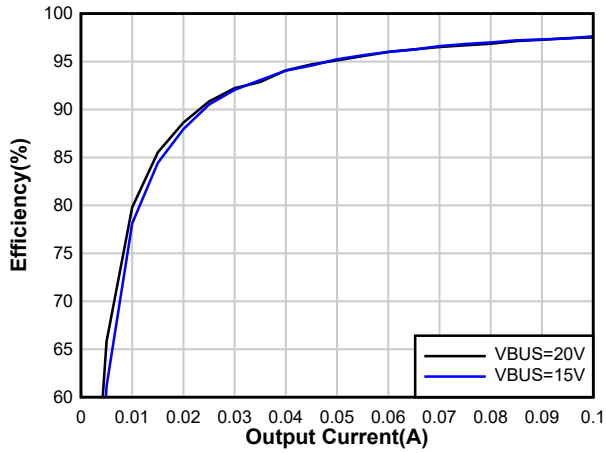
VBAT = 12 V CCM 800 kHz

Figure 8-10. OTG Efficiency with 3S Battery



VBAT = 16 V CCM 800 kHz

Figure 8-11. OTG Efficiency with 4S Battery



VBAT = 8.4 V VOUT = VBUS

Figure 8-12. PTM Mode Ligh Load System Efficiency

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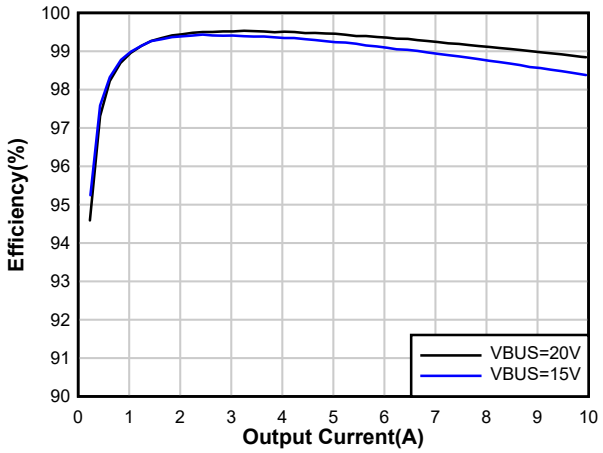
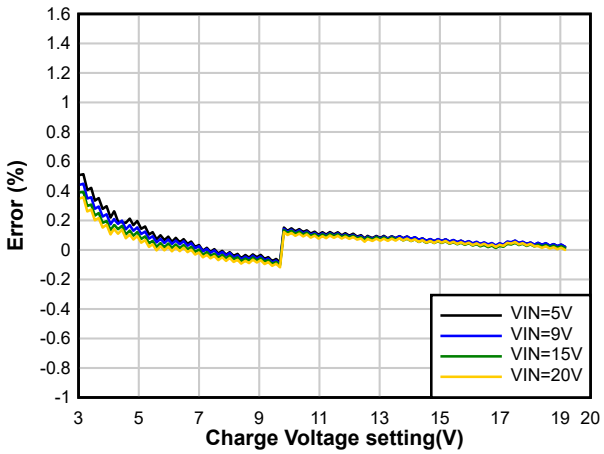
8.7 Typical Characteristics (continued)



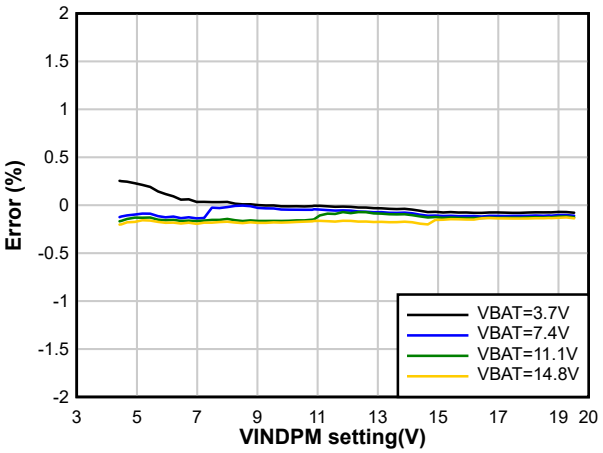
VBAT = 8.4 V VOUT = VBUS

Figure 8-13. PTM Mode Heavy Load System Efficiency



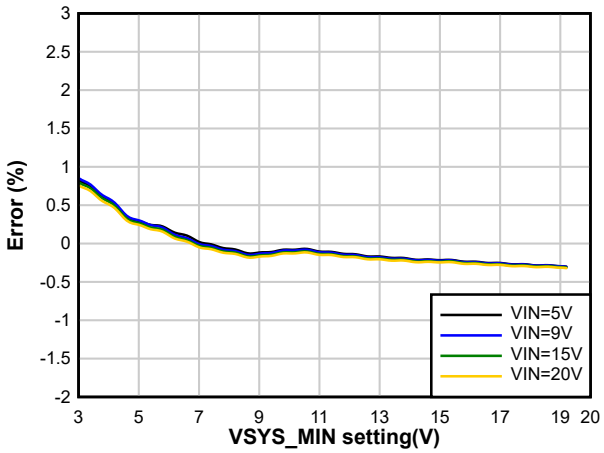
ICHG = 1024 mA CCM 800 kHz

Figure 8-14. Battery Voltage Regulation Accuracy



ICHG = 1024 mA CCM 800 kHz IBUS = 100 mA

Figure 8-15. Input Voltage(VINDPM) Regulation Accuracy



VBAT = 0.5 V CCM 800 kHz EN_OOA = 0b

Figure 8-16. Minimum System Voltage Regulation Accuracy

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9 Detailed Description

9.1 Overview

The BQ25723 is a narrow VDC buck-boost charger controller for portable electronics such as notebook, detachable, ultrabook, tablet, and other mobile devices with rechargeable batteries. It provides seamless transition between different converter operation modes (buck, boost, or buck-boost), fast transient response, and high light load efficiency.

The BQ25723 supports a wide range of power sources, including USB-C PD ports, legacy USB ports, traditional AC-DC adapters, and so forth. It takes input voltage from 3.5 V to 26 V and charges a battery of 1 to 4 cells in series. In the absence of an input source, the BQ25723 supports the USB On-the-Go (OTG) function from a 1- to 4-cell battery to generate an adjustable 3 V to 24 V at the USB port with 8-mV resolution.

When only the battery powers the system and no external load is connected to the USB OTG port, the BQ25723 provides the Vmin Active Protection (VAP) feature. In VAP operation, the BQ25723 first charges up the voltage of the input decoupling capacitors at VBUS to store a certain amount of energy. During the system peak power spike, the huge current drawn from the battery introduces a larger voltage drop across the impedance from the battery to the system. The energy stored in the input capacitors will supplement the system, to prevent the system voltage from dropping below the minimum system voltage and leading the system to a black screen. This VAP is designed to absorb system power peaks during the periods of high demand to improve system turbo performance, which is highly recommended by Intel for the platforms with a 1S~2S battery.

The BQ25723 features Dynamic Power Management (DPM) to limit input power and avoid AC adapter overloading. During battery charging, as system power increases, charging current is reduced to maintain total input current below adapter rating. If system power demand temporarily exceeds adapter rating, the BQ25723 supports the NVDC architecture to allow battery discharge energy to supplement system power.

The BQ25723 monitors adapter current, battery current, and system power. The flexibility of the programmable $\overline{\text{PROCHOT}}$ output goes directly to the CPU for throttling back when needed.

The latest version of the USB-C PD specification includes Fast Role Swap (FRS) to ensure power role swapping occurs in a timely fashion so that the device(s) connected to the dock never experience momentary power loss or glitching. The device integrates FRS with compliance to the USB-C PD specification.

The TI patented switching frequency dithering pattern can significantly reduce EMI noise over the entire conductive EMI frequency range (150 kHz to 30 MHz). Multiple dithering scale options are available to provide flexibility for different applications to simplify EMI noise filter design.

In order to be compliant with Intel IMVP8 / IMVP9, the BQ25723 includes a PSYS function to monitor the total platform power from the adapter and battery. Besides PSYS, it provides both an independent input current buffer (IADPT) and a battery current buffer (IBAT) with highly accurate current sense amplifiers. If the platform power exceeds the available power from the adapter and battery, a $\overline{\text{PROCHOT}}$ signal is asserted to the CPU so that the CPU optimizes its performance to the power available to the system.

The host controls input current, charge current, and charge voltage registers with high resolution, high accuracy regulation limits. It also sets the $\overline{\text{PROCHOT}}$ timing and threshold profile to meet system requirements.

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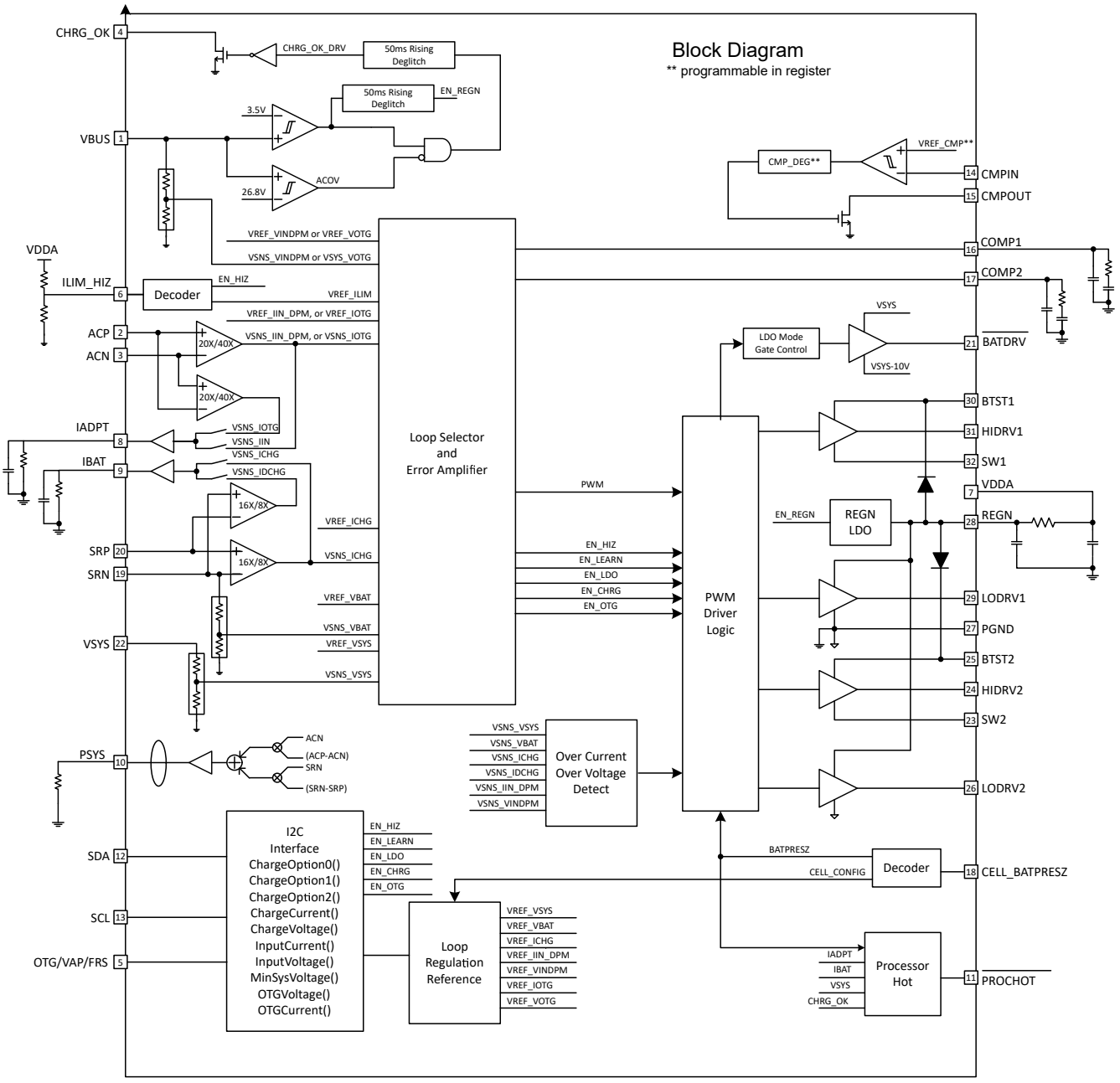
9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Up Sequence

The device powers up from the higher voltage of VBUS or VBAT through integrated power selector. The charger starts POR (power on reset) when VBUS exceeds V_{VBUS_UVLOZ} or VBAT exceeds V_{VBAT_UVLOZ}. 5 ms after either VBUS or VBAT becomes valid, the charger resets all the registers to the default state. Another 5 ms later, the user registers become accessible to the host.

Power up sequence when the charger is powered up from VBUS:

- After VBUS above V_{VBUS_UVLOZ}, enable 6-V LDO REGN pin and VDDA pin voltage increase accordingly. CHRG_OK pin goes HIGH and the AC_STAT is configured to 1.
- After passing VBUS qualification, the REGN voltage is setup. VINDPM is detected in VBUS steady state voltage and IIN_DPM is detected at ILIM_HIZ pin steady state voltage.
- Battery CELL configuration is read at CELL_BATPRESZ pin voltage and compared to VDDA to determine cell configuration. Corresponding the default value of ChargeVoltage register (REG0x05/04()), ChargeCurrent register (Reg0x03/02), VSYS_MIN register (Reg0x0D/0C) and SYSOVP threshold are loaded.
- Converter powers up.

Power up sequence when the charger is powered up from VBAT:

- If only battery is present and the voltage is above V_{VBAT_UVLOZ} , charger wakes up and the BATFET is turned on and connecting the battery to system.
- By default, the charger is in low power mode (EN_LWPWR = 1b) with lowest quiescent current. The REGN LDO stays off. The Quiescent current is minimized. $\overline{\text{PROCHOT}}$ is available through the independent comparator by setting EN_PROCHOT_LPWR=1b.
- The adapter present comparator is activated, to monitor the VBUS voltage.
- SDA and SDL lines stand by waiting for host commands.
- Device can move to performance mode by configuring EN_LWPWR = 0b. The host can enable IBAT buffer through setting EN_IBAT=1b to monitor discharge current. The PSYS, $\overline{\text{PROCHOT}}$ or the independent comparator also can be enabled by the host.
- In performance mode, the REGN LDO is always available to provide an accurate reference and gate drive voltage for the converter.

9.3.2 Vmin Active Protection (VAP) with Battery only

When operating in battery only mode, high system peak power can cause the VSYS to drop below the minimum system voltage due to impedance of battery pack, charging sense resistor and BATFET. Device incorporates VAP mode to help supplement the system during high peak power events by releasing energy previously stored in the input capacitor. While the system is operating with normal power loads, the charger can be configured to store energy in the input capacitors by charging them up to a programamble voltage level. During these high system power spikes, the energy stored in the input capacitors will supplement the system, to prevent the system voltage from dropping below the minimum system voltage. The VAP mode can help achieve much better Turbo performance for Intel CPU under battery only condition. Please contact factory for more detail information about VAP mode.

9.3.3 Two-Level Battery Discharge Current Limit

To prevent the triggering of battery overcurrent protection and avoid battery wear-out, two battery current limit levels (IDCHG_TH1 and IDCHG_TH2) $\overline{\text{PROCHOT}}$ profiles are recommended to be enabled. Define IDCHG_TH1 through REG0x39h[7:2], IDCHG_TH2 is set through REG0x3Ch[5:3] for fixed percentage of IDCHG_TH1. There are dedicated de-glitch time setting registers(IDCHG_DEG1 and IDCHG_DEG2) for both IDCHG_TH1 and IDCHG_TH2.

- When battery discharge current is continuously higher than IDCHG_TH1 for more than IDCHG_DEG1 de-glitch time, $\overline{\text{PROCHOT}}$ is asserted immediately. If the discharge current reduces to lower than IDCHG_TH1, then the time counter resets automatically. STAT_IDCHG1 bit will be set to 1 after $\overline{\text{PROCHOT}}$ is triggered.

  Set PP_IDCHG1=1b to enable IDCHG_TH1 for triggering $\overline{\text{PROCHOT}}$.

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- When battery discharge current is continuously higher than IDCHG_TH2 for more than IDCHG_DEG2 de-glitch time, $\overline{\text{PROCHOT}}$ is asserted immediately. If the discharge current reduces to lower than IDCHG_TH2, then the time counter resets automatically. STAT_IDCHG2 bit will be set to 1 after $\overline{\text{PROCHOT}}$ is triggered.

  Set PP_IDCHG2=1b to enable IDCHG_TH2 for triggering $\overline{\text{PROCHOT}}$.

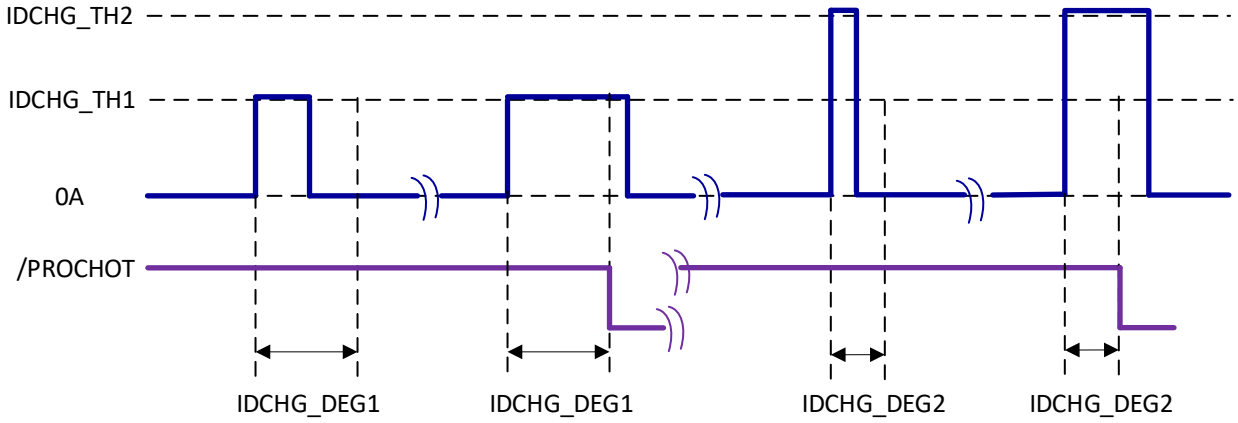

Figure 9-1. Two-Level Battery Discharging Current Trigger $\overline{\text{PROCHOT}}$ Diagram

9.3.4 Fast Role Swap Feature

Fast Role Swap (FRS) means charger quickly swaps from power sink role to power source role to provide an OTG output voltage to accessories when the original power source is disconnected. This feature is defined to transfer the charger from forward mode to OTG mode quickly without dropping VBUS voltage per USB-C PD specification requirement.Please contact factory for more detail information about FRS mode.

9.3.5 CHRG_OK Indicator

CHRG_OK is an active HIGH open drain indicator. It indicates the charger is in normal operation when the following conditions are valid:

- VBUS is above V_{VBUS_CONVEN}
- VBUS is below V_{ACOV_FALL}
- No faults triggered such as: SYSOVP/SYSUVP/ACOC/TSHUT/BATOVP/BATOC/force converter off.

9.3.6 Input and Charge Current Sensing

The charger supports 10 mΩ and 5 mΩ for both input current sensing and charge current sensing. By default, 10 mΩ is enabled by POR setting RSNS_RAC=0b and RSNS_RSR=0b, if 5 mΩ sensing is used please configure RSNS_RAC=1b and RSNS_RSR=1b. Lower current sensing resistor can help improve overall charge efficiency especially under heavy load. At same time PSYS,IADPT,IBAT pin accuracy and IINDPM/ICHG/IOTG regulation accuracy get worse due to effective signal reduction in comparison to error signal components.

When RSNS_RAC=RSNS_RSR=0b and 10 mΩ is used for both input and charge current sensing, the pre-charge current clamp is 384 mA (2 A for 1S if VSYS_MIN>VBAT>3 V), the maximum IIN_HOST setting is clamped at 6.35 A, and the maximum charge current is clamped at 8.128 A.

When RSNS_RAC=RSNS_RSR=1b and 5 mΩ is used for both input and charge current sensing, the charger will internally compensate pre-charge current clamp to be 384 mA (2 A for 1S if VSYS_MIN>VBAT>3 V) under 5-mΩ current sensing which keeps consistent between 10 mΩ and 5 mΩ. Under 5-mΩ current sensing application charge current range is doubled to 16.256 A. Based on EN_FAST_5MOHM register bit status and IADPT pin resistor the maximum input current can be configured referring to Table 9-1:

For defined current sense resistors (10 mΩ/5 mΩ), PSYS function is still valid when unsymmetrical input current sense and charge current sense resistors are used. But RSNS_RAC and RSNS_RSR bit status have to be consistent with practical resistors used in the system.

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Table 9-1. Maximum Input Current Limit Configuration Table

INDUCTANCE (IADPT Pin Resistance)	EN_FAST_5MOHM	RSR_RAC BIT	MAXIMUM INPUT CURRENT LIMIT (IINDPM)
1.0 uH(90.9 kΩ) 1.5 uH(121 kΩ) 2.2 uH(137 kΩ)	Xb	RSNS_RAC=0b	6.35 A
	1b	RSNS_RAC=1b	6.35 A
	0b	RSNS_RAC=1b	10 A
3.3 uH(169 kΩ)	Xb	RSNS_RAC=0b	6.35 A
	Xb	RSNS_RAC=1b	10 A

9.3.7 Input Voltage and Current Limit Setup

The actual input current limit being adopted by the device is the lower setting of IIN_DPM and ILIM_HIZ pin. Register IIN_DPM input current limit setting will reset for below scenarios:

- When adapter is removed (CHRG_OK is not valid). Note when adapter is removed IIN_HOST will be reset one time to 3.25 A, under battery only host is still able to overwrite IIN_HOST register with a new value. If the adapter plug back in and CHRG_OK is pulled up, IIN_HOST will not be reset again.
- When input current optimization (ICO) is executed (EN_ICO_MODE=1b), the charger will automatically detect the optimized input current limit based on adapter output characteristic. The final IIN_DPM register setting could be different from IIN_HOST after ICO.

The voltage regulation loop of the charger regulates the input voltage to prevent the input adapter collapsing. The VINDPM threshold should be configured based on no load input voltage level.Charger initiates a VBUS voltage measurement without any load (VBUS at no load) right before the converter is enabled. The default VINDPM threshold is VBUS at no load – 1.28 V. Host can adjust VINDPM threshold after device POR through InputVoltage register(0x0B/0Ah[]), range from 3.2V to 19.52V with LSB 64mV.

After input current and voltage limits are set, the charger device is ready to power up. The host can always program the input current and voltage limit after the charger being powered up based on the input source type.

9.3.8 Battery Cell Configuration

CELL_BATPRESZ pin is biased with a resistor divider from VDDA to GND. After REGN LDO is activated (VDDA rise up), the device detects the battery configuration through CELL_BATPRESZ pin bias voltage. No external cap is allowed at CELL_BATPRESZ pin. When CELL_BATPRESZ pin is pulled down to GND (because of battery removal) at the beginning of startup process, VSYS_MIN = 3.6 V and SYS_OVP = 25 V and Maximum charge voltage (REG0x15) follow 1 cell default setting 4.2 V. . Refer to Table 9-2 for CELL_BATPRESZ pin configuration typical voltage for swept cell count.

Table 9-2. Battery Cell Configuration

CELL COUNT	PIN VOLTAGE w.r.t. VDDA	CHARGEVOLTAGE (REG0x05/04h)	SYSOVP	VSYS_MIN	VSYS/VBAT ADC OFFSET
4S	75%	16.800 V	19.5 V	12.3 V	2.88 V
3S	55%	12.600 V	19.5 V	9.2 V	2.88 V
2S	40%	8.400 V	12 V	6.6 V	2.88 V
1S	25%	4.200 V	6 V	3.6 V	2.88 V
Battery removal	0%	4.200 V	25 V	3.6 V	2.88 V

9.3.9 Device HIZ State

When input source is present, the charger can enter HIZ mode (converter shuts off) when ILIM_HIZ pin voltage is below 0.4 V or EN_HIZ is set to 1b. The charger is in the low quiescent current mode with REGN LDO enabled, ADC circuits are disactivated to reduce quiescent current. In order to exit HIZ mode, ILIM_HIZ pin voltage has to be higher than 0.8 V and EN_HIZ bit has to be set to 0b.

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9.3.10 USB On-The-Go (OTG)

The device supports USB OTG operation to deliver power from the battery to other portable devices through USB port. The OTG mode output voltage is set in OTGVoltage register REG0x07/06() with 8-mV LSB range from 3.0 V to 24 V. The OTG mode output current is set in OTGCurrent register REG0x09() with 50-mA LSB range from 0 A to 6.35 A under 10-mΩ input current sensing. Both OTG voltage and OTG current are qualified for USB-C™ programed power supply (PPS) specification in terms of resolution and accuracy. The OTG mode can be enabled following below steps:

- Set target OTG current limit in OTGCurrent register, VBUS is below $V_{VBUS_CONVENZ}$.
- Set OTG_VAP_MODE = 1b and EN_OTG = 1b.
- OTG/VAP/FRS pin is pulled high.
- 15 ms after the above conditions are valid, converter starts and VBUS ramps up to target voltage. CHRG_OK pin goes HIGH if OTG_ON_CHRGOK= 1b.

OTG/VAP/FRS pin is used as multi-function to enable OTG, VAP and FRS mode.

9.3.11 Converter Operation

The charger operates in buck, buck-boost and boost mode under different VBUS and VSYS combination. The buck-boost can operate seamlessly across the three operation modes. The 4 main switches operating status under continuous conduction mode (CCM) are listed below for reference.

Table 9-3. MOSFET Operation

MODE	BUCK	BUCK-BOOST	BOOST
Q1	Switching	Switching	ON
Q2	Switching	Switching	OFF
Q3	OFF	Switching	Switching
Q4	ON	Switching	Switching

9.3.12 Inductance Detection Through IADPT Pin

The charger reads the inductance value through the resistance tied to IADPT pin before the converter starts up. The resistances recommended for 1-µH (1200 kHz), 2.2-µH (800 kHz), and 3.3-µH (800 kHz) inductance are 90.9 kΩ, 137 kΩ, 169 kΩ, respectively. A surface mount chip resistor with ±2% or better tolerance must to be used for an accurate inductance detection. In order to detect the correct IADPT pin pull down resistance and get rid of disturbance from external circuit, before converter startup all the additional sensing circuit connecting to IADPT pin should be high impedance.

Table 9-4. Inductor Detection through IADPT Resistance

INDUCTOR IN USE	RESISTOR ON IADPT PIN
1 µH (recommended for 1200 kHz)	90.9 kΩ
1.5 µH (recommended for 800 kHz)	121 kΩ
2.2 µH (recommended for 800 kHz)	137 kΩ or 140 kΩ
3.3 µH (recommended for 800 kHz)	169 kΩ

9.3.13 Converter Compensation

The charger employs two compensation pins COMP1 and COMP2 for converter compensation purpose, appropriate RC network is needed to guarantee converter steady state and transient operation. Under different operation frequency corresponding RC network value needs to be configured respectively as shown in below table. The definition of these RC components can be referred to Figure 9-2. It is not recommended to change the compensation network value due to the complexity of various operation modes.

Table 9-5. Compensation Configuration

COMPONENT VALUE	INDUCTOR	COMP1 R1	COMP1 C11	COMP1 C12	COMP2 R2	COMP2 C21	COMP2 C22
800 kHz	3.3 µH	16.9 kΩ	3.3 nF	33 pF	15 kΩ	1200 pF	15 pF

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Table 9-5. Compensation Configuration (continued)

COMPONENT VALUE	INDUCTOR	COMP1 R1	COMP1 C11	COMP1 C12	COMP2 R2	COMP2 C21	COMP2 C22
800 kHz	2.2 µH	16.9 kΩ	3.3 nF	33 pF	10 kΩ	1200 pF	15 pF
800 kHz	1.5 µH	16.9 kΩ	3.3 nF	33 pF	6.8 kΩ	1200 pF	15 pF
1200 kHz	1.0 µH	16.9 kΩ	3.3 nF	33 pF	5 kΩ	1200 pF	15 pF

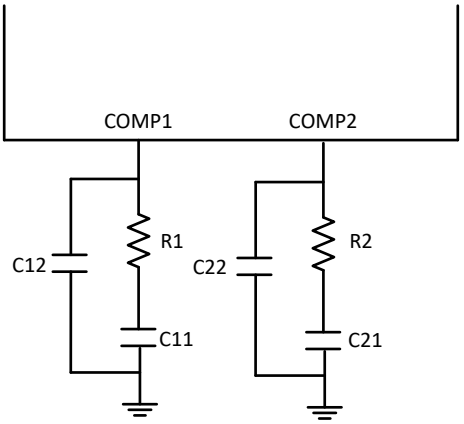

Figure 9-2. Compensation RC Network

9.3.14 Continuous Conduction Mode (CCM)

With sufficient charge or system current, the inductor current does not cross 0 A, which is defined as CCM. The controller starts a new cycle with ramp coming up from 200 mV. As long as the error amplifier output voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds error amplifier output voltage, HSFET turns off and low-side MOSFET (LSFET) turns on. At the end of the cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM, the inductor current always flows. Having the LSFET turn-on when the HSFET is off keeps the power dissipation low and allows safe charging at high currents.

9.3.15 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, BQ25723 switches to PFM operation at light load. The effective switching frequency will decrease accordingly when system load decreases. The minimum frequency can be limited to 25 kHz when the OOA feature is enabled (EN_OOA=1b) to avoid audible noise.

9.3.16 Switching Frequency and Dithering Feature

Normally, the IC switches in fixed frequency which can be adjusted through PWM_FREQ register bit. The Charger also support frequency dithering function to improve EMI performance. This function is disabled by default with setting EN_DITHER=00b. It can be enabled by setting EN_DITHER=01/10/11b, the switching frequency is not fixed when dithering is enabled. It varies within determined range by EN_DITHER setting, 01/10/11b is corresponding to ±2%/4%/6% switching frequency. Please contact factory for more detail information.

9.3.17 Current and Power Monitor

9.3.17.1 High-Accuracy Current Sense Amplifier (IADPT and IBAT)

A high-accuracy current sense amplifier (CSA) is used to monitor the input current during forward charging, or output current during OTG (IADPT) and the charge/discharge current (IBAT). IADPT voltage is 20× or 40× the differential voltage across ACP and ACN. IBAT voltage is 8×/16× of the differential across SRP and SRN. After input voltage or battery voltage is above UVLO, IADPT output becomes valid. To lower the voltage on current

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monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

- V_{IADPT} = 20 or 40 × (V_{ACP} – V_{ACN}) during forward mode, or 20 or 40 × (V_{ACN} – V_{ACP}) during reverse OTG mode.
- V_{IBAT} = 8 or 16 × (V_{SRP} – V_{SRN}) during forward charging mode.
- V_{IBAT} = 8 or 16 × (V_{SRN} – V_{SRP}) during forward supplement mode, reverse OTG mode and battery only discharge scenario.

A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional. Note that RC filtering has additional response delay. The CSA output voltage is clamped at 3.3 V.

9.3.17.2 High-Accuracy Power Sense Amplifier (PSYS)

The charger monitors total system power. During forward mode, the input adapter powers the system. During reverse OTG mode and battery only discharge scenario, the battery powers the system and VBUS output. The ratio of PSYS pin output current and total system power, K_{PSYS}, can be programmed in PSYS_RATIO register bit with default 1 µA/W. The input and charge sense resistors (R_{AC} and R_{SR}) are selected in RSNS_RAC bit and RSNS_RSR bit. By default, PSYS_CONFIG=00b and PSYS voltage can be calculated with Equation 1, where I_{IN}>0 when the charger is in forward charging and I_{IN}<0 when charger is in OTG operation; where I_{BAT}>0 when the battery is in charging and I_{BAT}<0 when battery is discharging.

$$V_{PSYS} = R_{PSYS} \cdot K_{PSYS} (V_{ACP} \cdot I_{IN} + V_{SYS} \cdot I_{BAT}) \quad (1)$$

R_{AC} and R_{SR} values are not limited to symmetrical both 5 mΩ or both 10 mΩ. For defined current sense resistors (10 mΩ/5 mΩ), PSYS function is still valid when R_{AC}=5 mΩ(RSNS_RAC=1b) and R_{SR}=10 mΩ(RSNS_RAC=0b), vice versa. As long as RSNS_RAC and RSNS_RSR bit status are consistent with practical resistors used in the system.

Charger can block IBAT contribution to above equation by setting PSYS_CONFIG =01b in forward mode and block IBUS contribution to above equation by setting PSYS_OTG_IDCHG=1b in OTG mode.

To minimize the quiescent current, the PSYS function is disabled by default PSYS_CONFIG = 11b.

Table 9-6. PSYS Configuration Table

CASE #	PSYS_CONFIG BITS	PSYS_OTG_IDCHG BITS	FORWARD MODE PSYS CONFIGURATION	OTG MODE PSYS CONFIGURATION
1	00b	0b	PSYS = PBUS+PBAT	PSYS = PBUS + PBAT
2	00b	1b	PSYS = PBUS+PBAT	PSYS =PBAT
3	01b	Xb	PSYS = PBUS	PSYS = 0
4	11b	Xb	PSYS = 0 (Disabled)	PSYS = 0 (Disabled)
5 (Reserved)	10b	Xb	PSYS = 0 (Reserved)	PSYS = 0 (Reserved)

9.3.18 Input Source Dynamic Power Management

The charger supports Dynamic Power Management (DPM). Normally, the input power source provides power for the system load and/or charging the battery. When the input current exceeds the input current setting (IIN_DPM), or the input voltage falls below the input voltage setting (VINDPM), the charger decreases the charge current to provide priority to the system load. As the system current rises, the available charge current drops accordingly towards zero. If the system load keeps increasing after the charge current drops down to zero, the system voltage starts to drop. As the system voltage drops below the battery voltage, the battery will discharge to supplement the heavy system load.

9.3.19 Input Current Optimizer (ICO)

For a recognized input adapter, IINDPM can be configured precisely to prevent adapter collapasing. When a third party unknown adapter is used, then input voltage regulation (VINDPM) feature can be leveraged to prevent

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input crash. With the increasing of input current, voltage drops along the input cable also increases and voltage measured it charger input port decreases accordingly. VINDPM feature can limit input power from adapter by regulating VBUS at certain value configured at InputVoltage register(0x0Bh/0Ah[]). However, the adapter may still overheat when it is kept running at its voltage limit for a long period of time. Therefore, it is preferred to operate the third party adapter slightly under its current rating. The Input Current Optimizer (ICO) feature can automatically maximize the power of unknown input adapter without continuously working under VINDPM. Note the ICO feature can only be employed when the adapter input current limit is at least 500 mA. Please contact factory for more detail information about ICO feature.

9.3.20 Two-Level Adapter Current Limit (Peak Power Mode)

Usually adapter can supply current higher than DC rating for a few milliseconds to tens of milliseconds. The charger employs two-level input current limit, or peak power mode, to fully utilize the overloading capability and minimize battery discharge during system load transient. The level 1 current limit, or I_{LIM1}, is the same as adapter DC current, set in IIN_DPM register. The level 2 overloading current, or I_{LIM2}, is set in ILIM2_VTH, as a percentage of I_{LIM1}.

When the charger detects input current surge and battery discharge due to load transient (both the adapter and battery support the system together), or when the charger detects the system voltage starts to drop below VSYS_MIN setting due to load transient (only the adapter supports the system), the charger will first apply I_{LIM2} for T_{OVLD} (PKPWR_TOVLD_DEG register bits), and then I_{LIM1} for up to $T_{MAX} – T_{OVLD}$ time. T_{MAX} is programmed in PKPWR_TMAX register bits. After $T_{MAX,}$ if the load is still high, another peak power cycle starts. Charging is disabled during T_{MAX} and T_{OVLD} already expires; once $T_{MAX,}$ expires, a new cycle starts and resumes charging automatically.

To prepare entering peak power follow below steps:

- Set EN_IIN_DPM=1b to enable input current dynamic power management.
- Set EN_EXTILIM=0b to disable external current limit.
- Set register IIN_HOST based on adapter output current rating as the level 1 current limit(I_{LIM1})
- Set register bits ILIM2_VTH according to the adapter overload capability as the level 2 current limit(I_{LIM2}) .
- Set register bits PKPWR_TOVLD_DEG as I_{LIM2} effective duration time for each peak power mode operation cycle based on adapter capability.
- Set register bits PKPWR_TMAX as each peak power mode operation cycling time based on adapter capability.

Depends on the battery existence and charge status peak power mode can be finally enabled with two different approaches:

- When battery is depleted in which VBAT is lower than VSYS_MIN setting or battery is removed, host need to set EN_PKPWR_VSYS=1b to enable peak power mode triggered by system voltage undershoot. The under-shoot threshold is the VSYS_MIN register setting which is the system regulation point before load transient happens. Typical application waveform refer to Figure 10-21.
- When battery is not depleted in which VBAT is higher than VSYS_MIN setting, host need to set EN_PKPWR_IIN_DPM=1b to enable peak power mode triggered by input current overshoot. The overshoot threshold is IIN_DPM register which is same as the level 1 current limit (I_{LIM1}). Typical application waveform refer to Figure 10-22.

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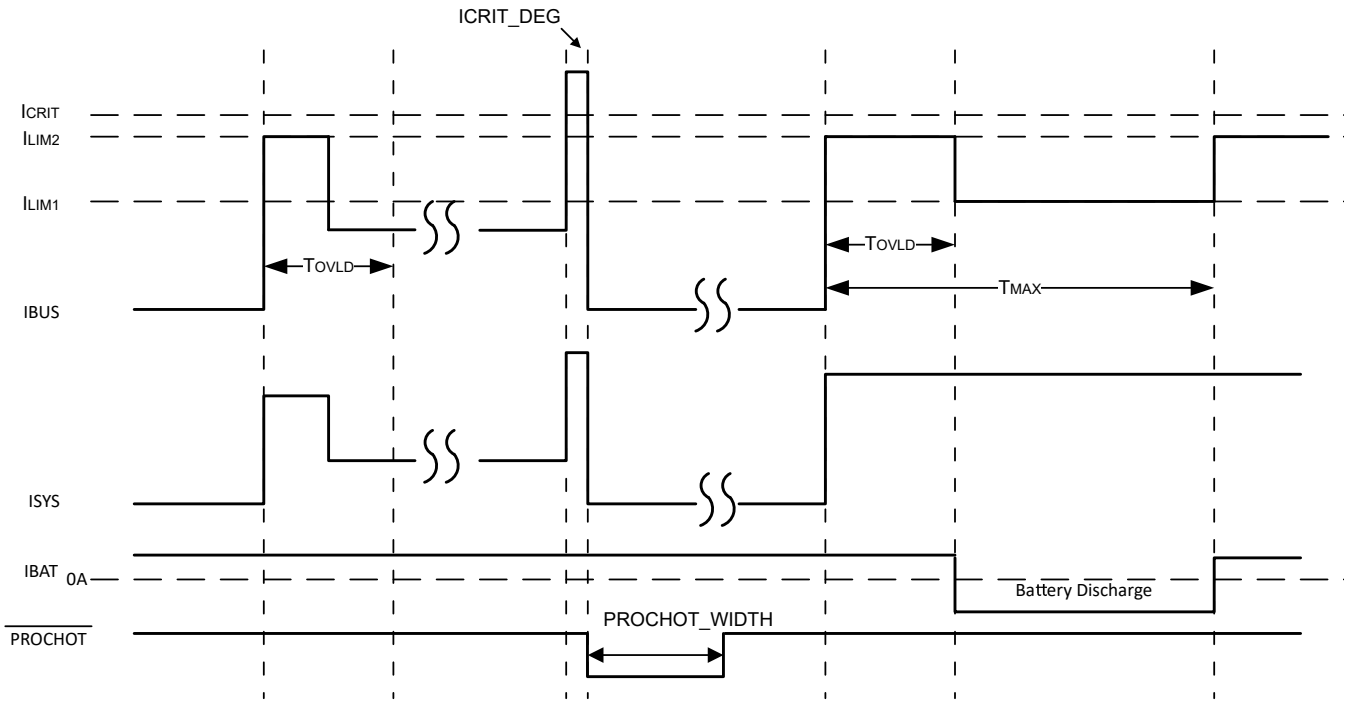

Figure 9-3. Two-Level Adapter Current Limit Timing Diagram

9.3.21 Processor Hot Indication

When CPU is running turbo mode, the system peak power may exceed available power from adapter and battery together. The adapter current and battery discharge peak current, or system voltage drop is an indication that system power is too high. The charger processor hot function monitors these events, and $\overline{\text{PROCHOT}}$ pulse is asserted if the system power is too high. Once CPU receives $\overline{\text{PROCHOT}}$ pulse from charger, it slows down to reduce system power. The events monitored by the processor hot function includes:

- ICRIT: adapter peak current, as 110% of I_{LIM2}
- INOM: adapter average current (110% of IIN_DPM)
- IDCHG1: battery discharge current level 1
- IDCHG2: battery discharge current level 2, note IDCHG2 threshold is always larger than IDCHG1 threshold determined by IDCHG_TH2 register setting.
- VBUS_VAP: VBUS threshold to trigger PROCHOT in VAP mode 2 and 3.
- VSYS: system voltage on VSYS pin
- Adapter Removal: upon adapter removal (VBUS is lower than ACOK_TH=3.2 V same as $V_{VBUS_CONVENZ}$ threshold)
- Battery Removal: upon battery removal (CELL_BATPRESZ pin goes LOW)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)
- VINDPM: VBUS lower than 83%/91%/100% of VINDPM setting. The effective threshold PROCHOT_VINDPM is determined by combination of register PROCHOT_VINDPM_80_90 bit and LOWER_PROCHOT_VINDPM bit:
  - PROCHOT_VINDPM=VINDPM register setting: LOWER_PROCHOT_VINDPM=0b;
  - PROCHOT_VINDPM=83% VINDPM register setting: LOWER_PROCHOT_VINDPM=1b;PROCHOT_VINDPM_80_90=0b;
  - PROCHOT_VINDPM=91% VINDPM register setting: LOWER_PROCHOT_VINDPM=1b;PROCHOT_VINDPM_80_90=1b;
- EXIT_VAP: Every time when the charger exits VAP mode.

The threshold of ICRIT, IDCHG1,IDCHG2,VSYS or VINDPM, and the deglitch time of ICRIT, INOM, IDCHG1, IDCHG2, or CMPOUT are programmable through I^2C register bits. Except the PROCHOT_EXIT_VAP is always enabled, the other triggering events can be individually enabled in ProchotOption1[7:0], PP_IDCHG2 and

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PP_VBUS_VAP. When any enabled event in $\overline{\text{PROCHOT}}$ profile is triggered, $\overline{\text{PROCHOT}}$ is asserted low for a single pulse with minimal width programmable in PROCHOT_WIDTH register bits. At the end of the single pulse, if the $\overline{\text{PROCHOT}}$ event is still active, the pulse gets extended until the event is removed.

If the $\overline{\text{PROCHOT}}$ pulse extension mode is enabled by setting EN_PROCHOT_EXT= 1b, the $\overline{\text{PROCHOT}}$ pin will be kept low until host writes PROCHOT_CLEAR= 0b, even if the triggering event has been removed.

If the PROCHOT_VINDPM or PROCHOT_EXIT_VAP is triggered, $\overline{\text{PROCHOT}}$ pin will always stay low until the host clears it, no matter the $\overline{\text{PROCHOT}}$ is in one pulse mode or in extended mode. In order to clear PROCHOT_VINDPM, host needs to write 0 to STAT_VINDPM. In order to clear PROCHOT_EXIT_VAP, host needs to write 0 to STAT_EXIT_VAP.

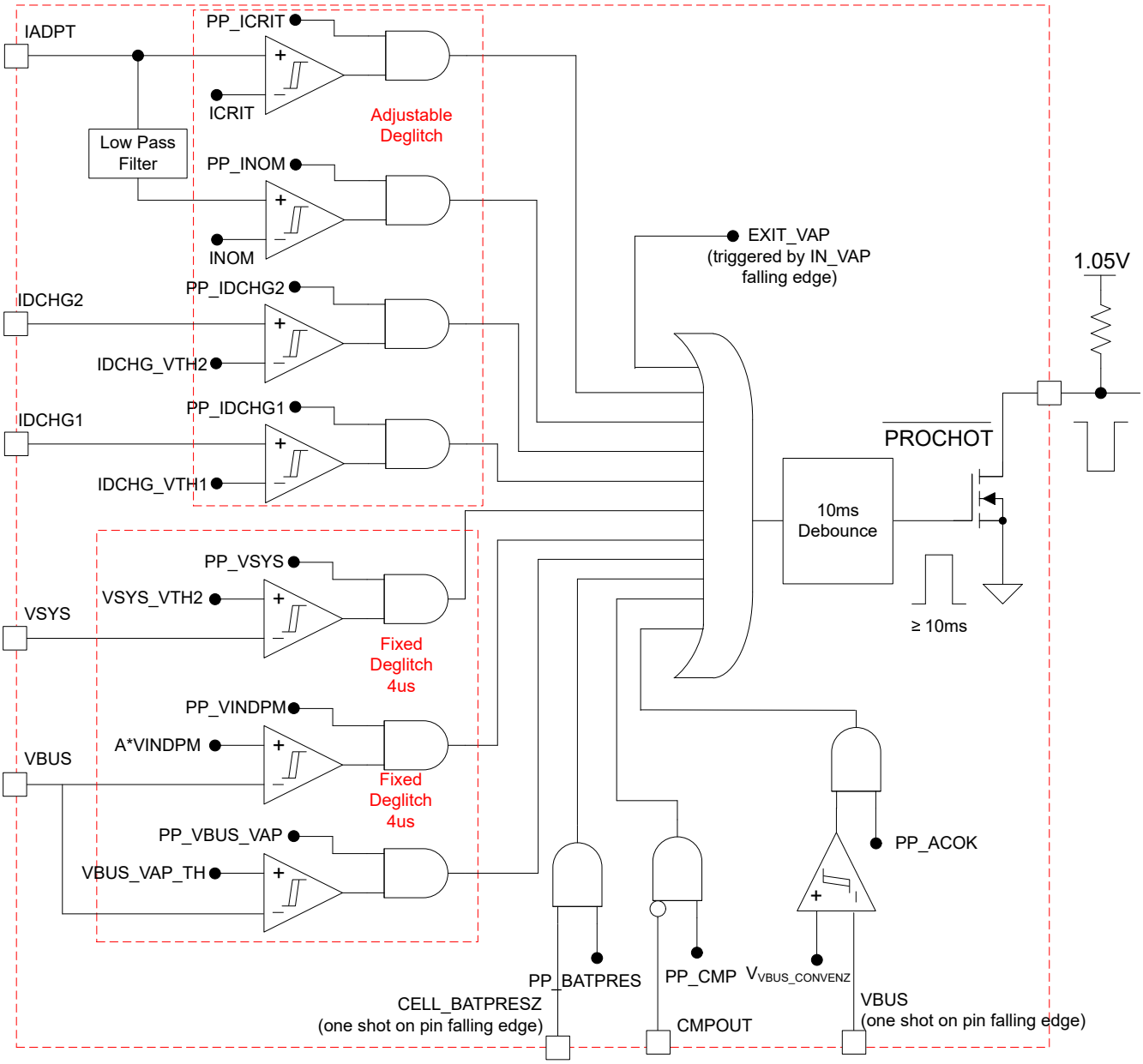

Figure 9-4. $\overline{\text{PROCHOT}}$ Profile

9.3.21.1 $\overline{\text{PROCHOT}}$ During Low Power Mode

During low power mode (EN_LWPWR = 1), the charger offers a low power $\overline{\text{PROCHOT}}$ function with very low quiescent current consumption (~35 µA), which uses the independent comparator to monitor the system voltage,

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and assert $\overline{\text{PROCHOT}}$ to CPU if the system power is too high and resulting system voltage is lower than specific threshold.

Below lists the register setting to enable $\overline{\text{PROCHOT}}$ monitoring system voltage in low power mode.

- EN_LWPWR = 1b to enable charger low power mode.
- REG0x34[7:0] = 00h
- REG0x30[6:4] = 000b
- Independent comparator threshold is always 1.2 V
- When EN_PROCHOT_LPWR = 1b, charger monitors system voltage. Connect CMPIN to voltage proportional to system voltage. $\overline{\text{PROCHOT}}$ triggers from HIGH to LOW when CMPIN voltage rises above 1.2 V.

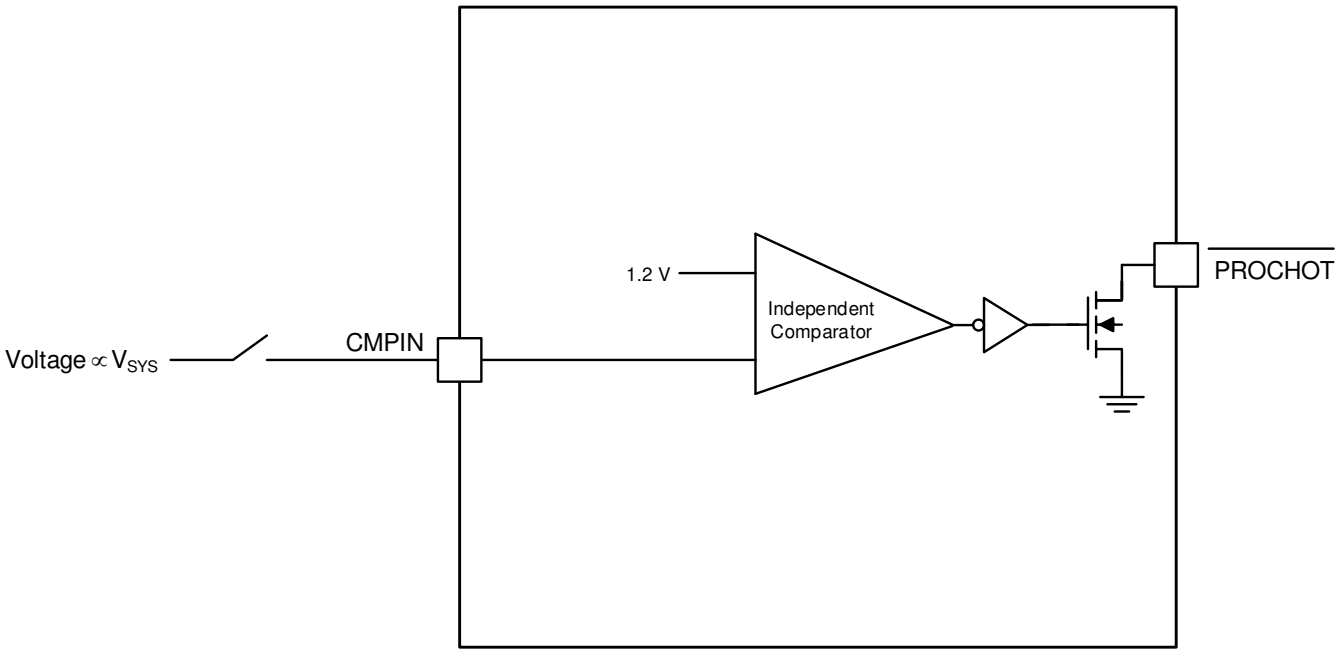

Figure 9-5. $\overline{\text{PROCHOT}}$ Low Power Mode Implementation

9.3.21.2 $\overline{\text{PROCHOT}}$ Status

REG0x22[7:0] and REG0x23[0] report which event in the profile triggers $\overline{\text{PROCHOT}}$ if the corresponding bit is set to 1. The status bit can be reset back to 0 after it is read by the host, when the current $\overline{\text{PROCHOT}}$ event is not active any more.

Assume there are two $\overline{\text{PROCHOT}}$ events, event A and event B. Event A triggers $\overline{\text{PROCHOT}}$ first, but event B is also active. Both status bits will be HIGH. At the end of the 10-ms $\overline{\text{PROCHOT}}$ pulse, if any of the $\overline{\text{PROCHOT}}$ event is still active (either A or B), the $\overline{\text{PROCHOT}}$ pulse is extended.

9.3.22 Device Protection

9.3.22.1 Watchdog Timer

The charger includes a watchdog timer to terminate charging if the charger does not receive a write ChargeVoltage() or write ChargeCurrent() command within 175s (default value and adjustable via WDTMR_ADJ). When watchdog timeout occurs, all register values are kept unchanged except ChargeCurrent() resets to 0 A . Write ChargeVoltage() or write ChargeCurrent() commands must be resent to reset watchdog timer. Writing WDTMR_ADJ = 00b to disable watchdog timer or update new watchdog timer values can also reset watchdog timer. New non-zero charge current value has to be written to ChargeCurrent() register to resume charging after watchdog timer expires.

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9.3.22.2 Input Overvoltage Protection (ACOV)

The charger has fixed ACOV voltage threshold with hysteresis. When VBUS pin voltage is higher than V_{ACOV_RISE} for more than 100 µs, it is considered as adapter overvoltage. CHRG_OK pin will be pulled low by the charger, and the converter will be disabled. As system falls below battery voltage, BATFET will be turned on. When VBUS pin voltage falls below V_{ACOV_FALL} for more than 1 ms, it is considered as adapter voltage returns back to normal voltage. CHRG_OK pin is pulled high by external pull-up resistor. The converter resumes if enable conditions are valid.

9.3.22.3 Input Overcurrent Protection (ACOC)

If the input current exceeds the 1.33× or 2× of ILIM2_VTH set point ACOC_TH (adjustable through ACOC_VTH), after 250-µs rising edge de-glitch time converter stops switching because of input overcurrent protection (ACOC). ACOC is a non-latch fault, if input current falls below set point, after 250-ms falling edge de-glitch time converter starts switching again. ACOC is disabled by default and need to be enabled by configuring EN_ACOC=1b. When ACOC is triggered, its corresponding status bit Fault ACOC will be set and it can be cleared by host read.

9.3.22.4 System Overvoltage Protection (SYSOVP)

When the converter starts up, the BQ25723 reads CELL_BATPRESZ pin configuration and sets ChargeVoltage() and SYSOVP threshold (1s – 6 V, 2s – 12 V, 3s/4s – 19.5 V). Before ChargeVoltage() is written by the host, the battery configuration will change with CELL pin voltage. When SYSOVP happens, the device latches off the converter. Fault SYSOVP status bit is set to 1. The user can clear latch-off by either writing 0 to the Fault SYSOVP status bit or removing and plugging in the adapter again. After latch-off is cleared, the converter starts again.

9.3.22.5 Battery Overvoltage Protection (BATOVP)

Battery overvoltage may happen when user plugs in a wrong battery or a wrong regulation voltage is written into ChargeVoltage() register. The BATOVP rising threshold is 104% of regulation voltage set in ChargeVoltage() register, and falling threshold is 102% of regulation voltage set in ChargeVoltage() register. When BATOVP rising condition is triggered: if charge is enabled (charge current is not 0A) converter should shut down with both HS MOSFET and LS MOSFET turned off; if charge is disabled the converter should keep operating without disturbance until battery rise up system voltage to be high enough trigger SYSOVP. There is no user status bit to monitor. Note VBAT voltage used for BATOVP detection is based on SRN pin measurement. When BATOVP is triggered with charge enabled, 40-mA discharge current is added on VSYS pin will help discharge battery voltage.

9.3.22.6 Battery Discharge Overcurrent Protection (BATOC)

The charger monitors the battery discharge current to provide the battery overcurrent protection (BATOC) through voltage across SRN and SRP. BATOC can be enabled by configuring EN_BATOC=1b. BATOC threshold is selected either 133% of IDCHG_TH2 or 200% IDCHG_TH2 through BATOC_VTH bit. The threshold is also clamped between 100 mV and 360 mV SRN-SRP cross voltage.

When discharge current is higher than the threshold after 250-µs deglitch time, BATOC fault is triggered, status bit Fault BATOC is set accordingly. Converter shuts down when BATOC is asserted to disable OTG operation and reduce discharge current. BATFET status is not impacted if need to supplement power to system.

BATOC is not a latch fault, therefore after BATOC fault is removed, with 250-ms relax time, converter resume switching automatically. But status bit Fault BATOC is only cleared by host read.

9.3.22.7 Battery Short Protection (BATSP)

For multicell operation, if BAT voltage falls below VSYS_MIN during charging, the maximum charger current is limited to 384 mA. For single-cell operation, if BAT voltage falls below 3.0 V during charging, the maximum charge current is limited to 384 mA; if BAT voltage is between 3.0 V and VSYS_MIN then maximum charge current is limited to 2 A. Note VBAT voltage used for battery short detection is based on SRN pin measurement.

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9.3.22.8 System Undervoltage Lockout (VSYS_UVP) and Hiccup Mode

The charger VSYS_UVP is enabled by POR (VSYS_UVP_ENZ=0b) and can be disabled by writing VSYS_UVP_ENZ=1b. This protection is mainly defined to protect converter from system short circuit under both startup and steady state process. VSYS pin is used to monitor the system voltage, when VSYS is lower than 2.4 V (configurable through VSYS_UVP register bits), there is 2-ms deglitch time, the IIN_DPM is clamped to 0.5 A by the charger itself.

If hiccup mode is enabled with VSYS_UVP_NO_HICCUP = 0b, after 2-ms deglitch time, the charger should shut down for 500 ms.The charger will restart for 10 ms if VSYS is still lower than 2.4 V, the charger should shut down again. This hiccup mode will be tried continuously, if the charger restart failed for 7 times in 90 second, the charger will be latched off. Fault VSYS_UVP bit will be set to 1 to report a system short fault. The charger only can be enabled again by writing Fault VSYS_UVP bit to 0b.

If hiccup mode is disabled VSYS_UVP_NO_HICCUP = 1b. After 2-ms deglitch time, the charger should shut down and latched off. Fault VSYS_UVP bit will be set to 1 to report a system short fault. The charger only can be enabled again once the host writes Fault VSYS_UVP bit to 0b.

9.3.22.9 Thermal Shutdown (TSHUT)

The WQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature reaches the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the REGN LDO current limit is reduced to 16 mA and stays on. When the temperature falls below 135°C, charge can be resumed with soft start.

When thermal shut down is triggered, TSHUT status bit will be triggered. This status bit keep triggered until host read to clear it. If TSHUT is still present during host read, then this bit will try to be cleared when host read but finally keep triggered because TSHUT still exists.

9.4 Device Functional Modes

9.4.1 Forward Mode

When input source is connected to VBUS, BQ25723 is in forward mode to regulate system and charge battery.

9.4.1.1 System Voltage Regulation with Narrow VDC Architecture

The device employs Narrow VDC architecture (NVDC) with BATFET separating the system from the battery. The minimum system voltage is set by VSYS_MIN register REG0x0D/0C(). Even with a depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at VSYS_MIN register value. As the battery voltage rises above the minimum system voltage, system voltage is regulated 150 mV above battery voltage when BATFET is turned off (no charging or no supplement current). When in charging or in supplement mode, the voltage difference between the system and battery is the V_{DS} of the BATFET and the BATFET is fully on.

9.4.1.2 Battery Charging

The BQ25723 charges 1- to 4-cell battery in constant current (CC), and constant voltage (CV) mode. Based on CELL_BATPREZ pin setting, the charger sets default battery voltage 4.2 V/cell to ChargeVoltage(). According to battery capacity, the host programs appropriate charge current to ChargeCurrent() register. When battery is full or battery is not in good condition to charge, host terminates charge by setting CHRG_INHIBIT bit to 1b, or setting ChargeCurrent() to zero.

9.4.2 USB On-The-Go

The BQ25723 supports USB OTG functionality to deliver power from the battery to other portable devices through USB port (reverse mode). The OTG output voltage is compliant with USB-C PD specification, including 5 V, 9 V, 15 V, and 20 V. The output current regulation is compliant with USB-C PD specification, including 500 mA, 1.5 A, 3 A and 5 A, and so forth.

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Similar to forward operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

9.4.3 Pass Through Mode (PTM)-Patented Technology

The charger can be operated in the pass through mode (PTM) to improve efficiency. In PTM, the Buck and Boost high-side FETs (Q1 and Q4) are both turned on, while the Buck and Boost low-side FETs are both turned off. The input power is directly passed through the charger to the system. The switching losses of MOSFETs and the inductor core loss are saved. The charger quiescent current under PTM mode is also minimized to further increase light load efficiency. Charger will be transition from normal Buck-Boost operation to PTM operation by setting EN_PTM = 1b; and will transition out of PTM mode with host control by setting EN_PTM =0b. Please contact factory for more detail information about PTM mode.

9.5 Programming

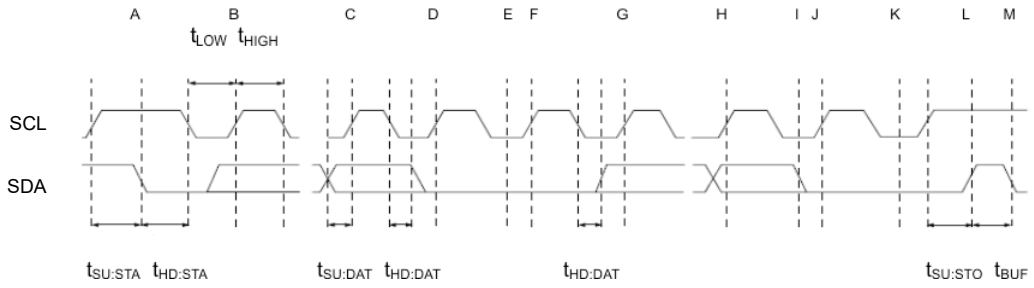
The charger supports battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Section 9.5.1.7. The I^{2}C address is 6Bh(0b1101011) consist of 7 bits. Adding read(1b) and write(0b) to the end of address 7bits, the total 8bits data format address should be D6h (1101011_0 for write)/ D7h(1101011_1 for read). The ManufacturerID and DeviceID registers are assigned to identify the charger device. The ManufacturerID register command always returns 40h.

9.5.1 I^{2}C Serial Interface

The BQ25723 uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^{2}C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as host or target when performing data transfers. A host is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target device.

The device operates as a target device with address D6h, receiving control inputs from the host device like micro controller or a digital signal processor through REG00-REG3F. The I^{2}C interface supports both standard mode (up to 100 kHz), and fast mode (up to 400 kHz). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

9.5.1.1 Timing Diagrams



A = Start condition

B = MSB of address clocked into target

C = LSB of address clocked into target

D = R/W bit clocked into target

E = Target pulls SDA line low

F = ACKNOWLEDGE bit clocked into host

G = MSB of data clocked into target

H = LSB of data clocked into target

I = Target pulls SDA line low

J = Acknowledge clocked into host

K = Acknowledge clock pulse

L = Stop condition, data executed by target

M = New start condition

Figure 9-6. I^{2}C Write Timing

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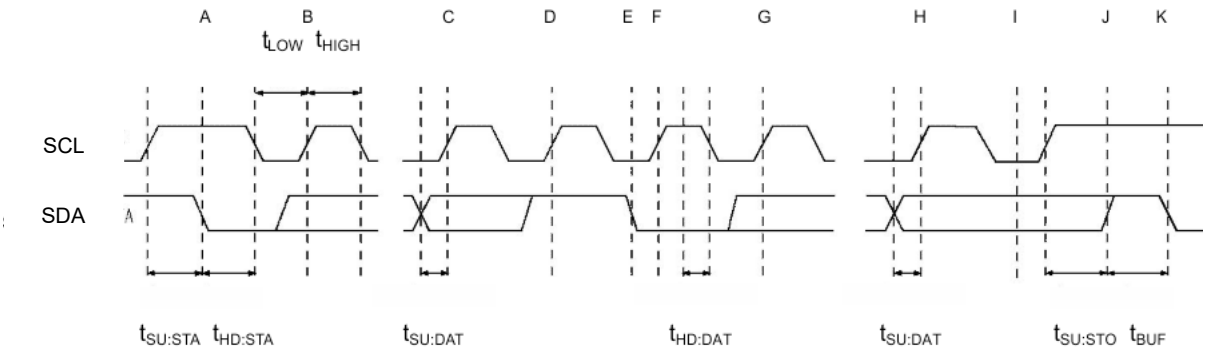

A = Start condition

B = MSB of address clocked into target

C = LSB of address clocked into target

D = R/W bit clocked into target

E = Target pulls SDA line low

F = ACKNOWLEDGE bit clocked into host

G = MSB of data clocked into host

H = LSB of data clocked into host

I = Acknowledge clock pulse

J = Stop condition

K = New start condition

Figure 9-7. I²C Read Timing

9.5.1.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

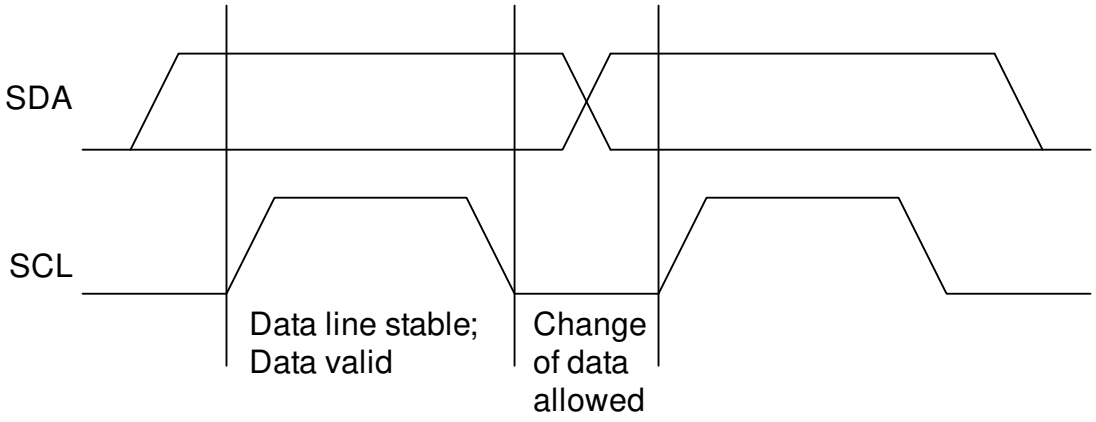

Figure 9-8. Bit Transfer on the I²C Bus

9.5.1.3 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

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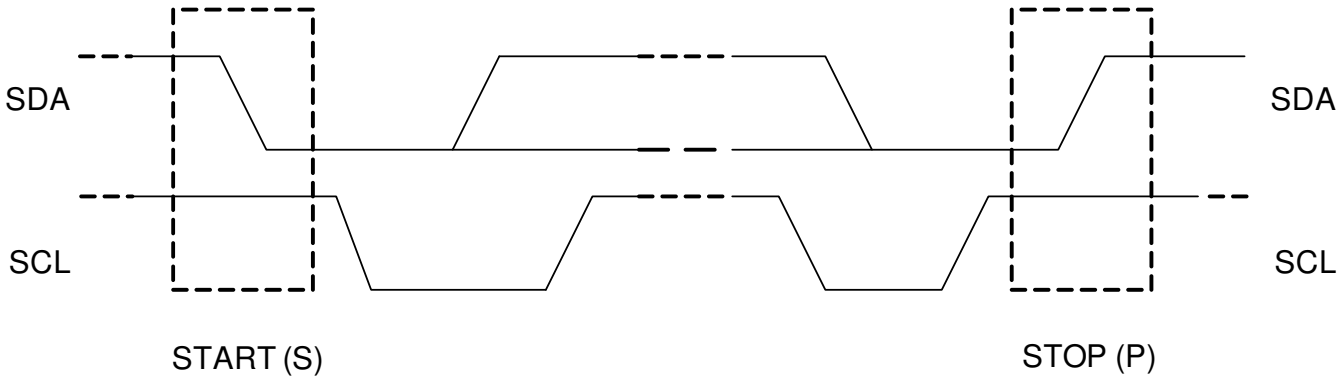

Figure 9-9. START and STOP Conditions

9.5.1.4 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

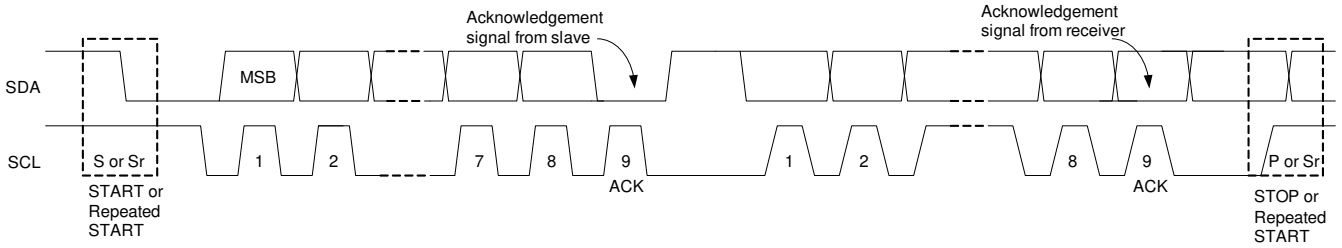

Figure 9-10. Data Transfer on the I²C Bus

9.5.1.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

9.5.1.6 Target Address and Data Direction Bit

After the START, a target address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

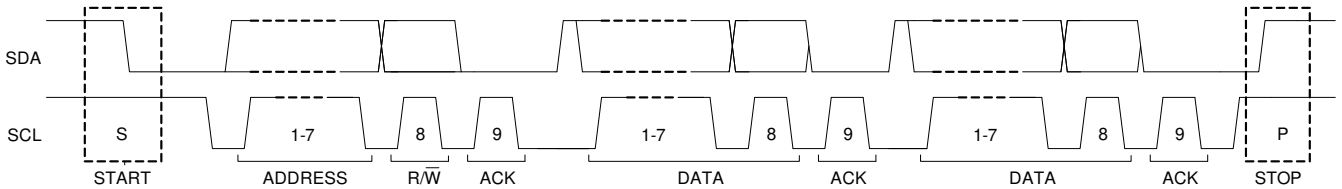

Figure 9-11. Complete Data Transfer

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9.5.1.7 Single Read and Write

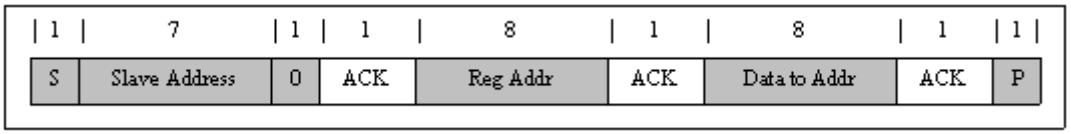

Figure 9-12. Single Write

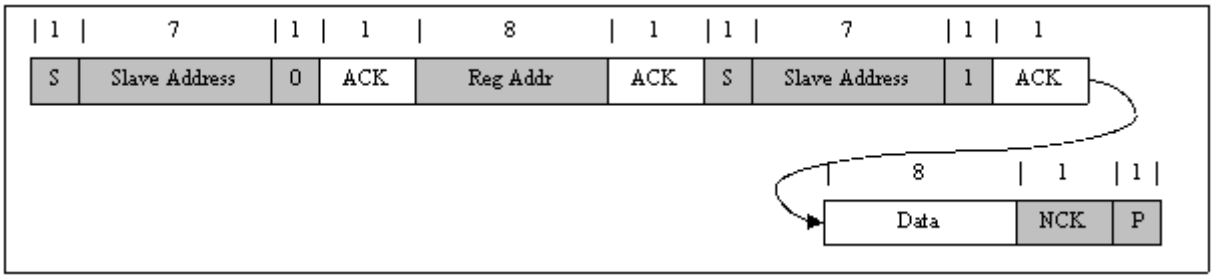

Figure 9-13. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.5.1.8 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

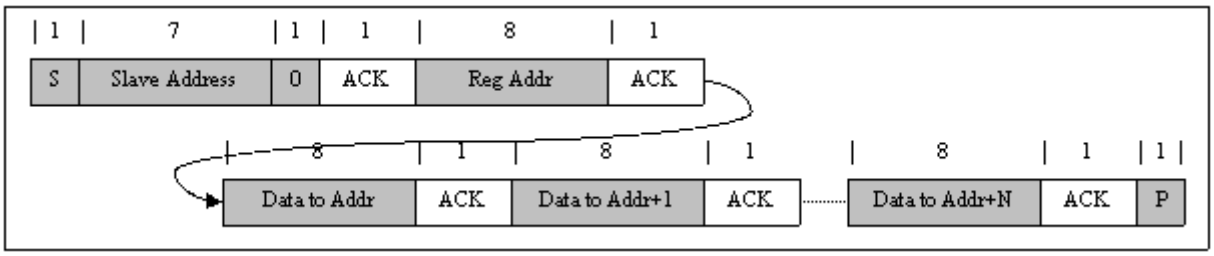

Figure 9-14. Multi Write

Figure 9-15. Multi Read



9.5.1.9 Write 2-Byte I²C Commands

A few I²C commands combine two 8-bit registers together to form a complete value. These commands include:

- ChargeCurrent()
- ChargeVoltage()
- IIN_DPM()
- OTGVoltage()
- InputVoltage()

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Host has to write LSB bit first and then move on to MSB bit. No other command can be inserted in between these two writes. The charger waits for the complete write to the two registers to decide whether to accept or ignore the new value.

After the completion of LSB and MSB bytes, the two bytes will be updated at the same time. If host writes MSB byte first, the command will be ignored. If the time between write of LSB and MSB bytes exceeds watchdog timer, both the LSB and MSB commands will be ignored.

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9.6 Register Map

Table 9-7. Charger Command Summary

I²C ADDR (MSB/LSB)	REGISTER NAME	TYPE	DESCRIPTION	LINKS
01/00h	ChargeOption0()	R/W	Charge Option 0	Go
03/02h	ChargeCurrent()	R/W	7-bit charge current setting LSB 64 mA, Range 0 mA - 8128 mA	Go
05/04h	ChargeVoltage()	R/W	12-bit charge voltage setting LSB 8 mV, Default: 1S-4200mV, 2S-8400mV, 3S-12600mV, 4S-16800mV	Go
07/06h	OTGVoltage()	R/W	12-bit OTG voltage setting LSB 8 mV, Range: 3000 mV – 24000 mV	Go
09/08h	OTGCurrent()	R/W	7-bit OTG output current setting LSB 50 mA, Range: 0 A – 6350 mA	Go
0B/0Ah	InputVoltage()	R/W	8-bit input voltage setting LSB 64 mV, Range: 3200 mV – 19520 mV	Go
0D/0Ch	VSYS_MIN()	R/W	8-Bit minimum system voltage setting LSB: 100 mV, Range: 1000 mV - 23000 mV Default: 1S-3.6V, 2S-6.6V, 3S-9.2V, 4S-12.3V	Go
0F/0Eh	IIN_HOST()	R/W	7-bit Input current limit set by host LSB: 50 mA, Range: 50 mA - 6350 mA	Go
21/20h	ChargerStatus()	R with R/W bits	Charger Status	Go
23/22h	ProchotStatus()	R and R/W bits	Prochot Status	Go
25/24h	IIN_DPM()	R	7-bit input current limit in use LSB: 50 mA, Range: 50 mA - 6350 mA	Go
27/26h	ADCVBUS/PSYS()	R	8-bit digital output of input voltage, 8-bit digital output of system power PSYS: Full range: 3.06 V, LSB: 12 mV VBUS: Full range: 0 V - 24.48 V, LSB 96 mV	Go
29/28h	ADCIBAT()	R	7-bit digital output of battery charge current, 7-bit digital output of battery discharge current ICHG: Full range 8.128 A, LSB 64 mA IDCHG: Full range: 32.512 A, LSB: 256 mA	Go
2B/2Ah	ADCIINCMPIN()	R	8-bit digital output of input current, 8-bit digital output of CMPIN voltage POR State - IIN: Full range: 12.75 A, LSB 50 mA CMPIN: Full range 3.06 V, LSB: 12 mV	Go
2D/2Ch	ADCVSYSVBAT()	R	8-bit digital output of system voltage, 8-bit digital output of battery voltage VSYS: Full range: 2.88 V - 19.2 V, LSB: 64 mV (1S-4S) VBAT: Full range : 2.88 V - 19.2 V, LSB 64 mV (1S-4S)	Go
2Eh	ManufacturerID()	R	Manufacturer ID - 0x0040H	Go
2Fh	DeviceID()	R	Device ID	Go
31/30h	ChargeOption1()	R/W	Charge Option 1	Go
33/32h	ChargeOption2()	R/W	Charge Option 2	Go
35/34h	ChargeOption3()	R/W	Charge Option 3	Go
37/36h	ProchotOption0()	R/W	$\overline{\text{PROCHOT}}$ Option 0	Go
39/38h	ProchotOption1()	R/W	$\overline{\text{PROCHOT}}$ Option 1	Go
3B/3Ah	ADCOption()	R/W	ADC Option	Go
3D/3Ch	ChargeOption4()	R/W	Charge Option 4	Go
3F/3Eh	Vmin Active Protection()	R/W	Vmin Active Protection	Go

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9.6.1 ChargeOption0 Register (I²C address = 01/00h) [reset = E70Eh]

Figure 9-14. ChargeOption0 Register (I²C address = 01/00h) [reset = E70Eh]

7	6	5	4	3	2	1	0
EN_LWPWR	WDTMR_ADJ		IIN_DPM_AUTO_DISABLE	OTG_ON_CHRGOK	EN_OOA	PWM_FREQ	DIS_STRGRV
R/W	R/W		R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
EN_CMP_LATCH	VSYS_UVP_ENZ	EN_LEARN	IADPT_GAIN	IBAT_GAIN	EN_LDO	EN_IIN_DPM	CHRG_INHIBIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-8. ChargeOption0 Register (I²C address = 01h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_LWPWR	R/W	1b	Low Power Mode Enable, under low power mode lowest quiescent current is achieved when only battery exist. It is not recommended to enable low power mode when adapter present. 0b: Disable Low Power Mode. Device in performance mode with battery only. The $\overline{\text{PROCHOT}}$, current/power monitor buffer and comparator follow register setting. 1b: Enable Low Power Mode. Device in low power mode with battery only for lowest quiescent current. The REGN is off. The $\overline{\text{PROCHOT}}$, discharge current monitor buffer, power monitor buffer and independent comparator are disabled. ADC is not available in Low Power Mode. Independent comparator and its low power mode $\overline{\text{PROCHOT}}$ profile can be enabled by setting EN_PROCHOT_LPWR bit to 1b. <default at POR>
6-5	WDTMR_ADJ	R/W	11b	WATCHDOG Timer Adjust Set maximum delay between consecutive Host write of charge voltage or charge current command. If device does not receive a write on the REG0x15() or the REG0x14() within the watchdog time period, the charger will be suspended by setting the REG0x14() to 0 mA . After expiration, the timer will resume upon the write of REG0x14(), REG0x15() or REG0x12[14:13]. 00b: Disable Watchdog Timer 01b: Enabled, 5 sec 10b: Enabled, 88 sec 11b: Enable Watchdog Timer, 175 sec <default at POR>
4	IIN_DPM_AUTO_DISABLE	R/W	0b	IIN_DPM Auto Disable When CELL_BATPRESZ pin is LOW, the charger automatically disables the IIN_DPM function by setting EN_IIN_DPM (REG0x12[1]) to 0. The host can enable IIN_DPM function later by writing EN_IIN_DPM bit (REG0x12[1]) to 1. 0b: Disable this function. IIN_DPM is not disabled when CELL_BATPRESZ goes LOW. <default at POR> 1b: Enable this function. IIN_DPM is disabled when CELL_BATPRESZ goes LOW.
3	OTG_ON_CHRGOK	R/W	0b	Add OTG to CHRG_OK Drive CHRG_OK to HIGH when the device is in OTG mode. 0b: Disable <default at POR> 1b: Enable

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Table 9-8. ChargeOption0 Register (I²C address = 01h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2	EN_OOA	R/W	1b	Out-of-Audio Enable In both forward mode and OTG mode, switching frequency reduces with diminishing load, under extreme light load condition the switching frequency could be lower than 25 kHz which is already in audible frequency range. By configuring EN_OOA=1b, the minimum PFM burst frequency is clamped at around 25 kHz to avoid any audible noise. 0b: No limit of PFM burst frequency 1b: Set minimum PFM burst frequency to above 25 kHz to avoid audio noise <default at POR>
1	PWM_FREQ	R/W	1b	Switching Frequency Selection: Recommend 1200 kHz with 1 µH, 800 kHz with 2.2 µH. 0b: 1200 kHz 1b: 800 kHz<default at POR>
0	DIS_STRGRV	R/W	1b	Switching HS MOSFET turn on gate drive strength. 0b: Enable HS MOSFET strong turn on gate drive strength 1b: Disable HS MOSFET strong turn on gate drive strength <default at POR>

Table 9-9. ChargeOption0 Register (I²C address = 00h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_CMP_LATCH	R/W	0b	The EN_CMP_LATCH bit, will latch the independent comparator output after it is triggered at low state. If enabled in PROCHOT profile REG34H[6]=1 , STAT_COMP bit REG0x21[6] keep 1b after triggered until read by host and clear 0b: Independent comparator output will not latch when it is low<default at POR> 1b: Independent comparator output will latch when it is low, host can clear CMPOUT pin by toggling this REG0x12[7] bit.
6	VSYS_UVP_ENZ	R/W	0b	To disable system under voltage protection. 0b: VSYS under voltage protection is enabled <default at POR> 1b: VSYS under voltage protection is disabled
5	EN_LEARN	R/W	0b	LEARN mode allows the battery to discharge and converter to shut off while the adapter is present . It calibrates the battery gas gauge over a complete discharge/charge cycle. When the host determines the battery voltage is below battery depletion threshold, the host switch the system back to adapter input by writing this bit back to 0b. 0b: Disable LEARN Mode <default at POR> 1b: Enable LEARN Mode
4	IADPT_GAIN	R/W	0b	IADPT Amplifier Ratio The ratio of voltage on IADPT and voltage across ACP and ACN. 0b: 20× <default at POR> 1b: 40×
3	IBAT_GAIN	R/W	1b	IBAT Amplifier Ratio The ratio of voltage on IBAT and voltage across SRP and SRN 0b: 8× 1b: 16× <default at POR>

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Table 9-9. ChargeOption0 Register (I^2C address = 00h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2	EN_LDO	R/W	1b	LDO Mode Enable When battery voltage is below minimum system voltage (REG0x3E()), the charger is in pre-charge with LDO mode enabled. 0b: Disable LDO mode, BATFET fully ON. Precharge current is set by battery pack internal resistor. The system is regulated by the MaxChargeVoltage register. 1b: Enable LDO mode, Precharge current is set by the ChargeCurrent register and clamped below 384 mA (2 cell – 4 cell, 1cell VBAT<3.0V) or 2A (1cell 3.0V<VBAT<3.6V). The system is regulated by the VSYS_MIN register. <default at POR>
1	EN_IIN_DPM	R/W	1b	IIN_DPM Enable Host writes this bit to enable IIN_DPM regulation loop. When the IIN_DPM is disabled by the charger (refer to IIN_DPM_AUTO_DISABLE), this bit goes LOW. 0b: IIN_DPM disabled 1b: IIN_DPM enabled <default at POR>
0	CHRG_INHIBIT	R/W	0b	Charge Inhibit When this bit is 0, battery charging will start with valid values in the ChargeVoltage() register and the ChargeCurrent register. 0b: Enable Charge <default at POR> 1b: Inhibit Charge

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9.6.2 ChargeCurrent Register (I²C address = 03/02h) [reset = 0000h]

To set the charge current, write 16-bit ChargeCurrent() command (REG0x03/02h()) using the data format listed Figure 9-15.

With 5-mΩ sense resistor, the charger provides charge current range of 0 A to 16.256 A, with a 128-mA step resolution. With 10-mΩ sense resistor, the charger provides charge current range of 0 A to 8.128 A, with a 64-mA step resolution.

Upon POR, ChargeCurrent() is 0 A. Below scenarios will also reset Charge current to zero:

- CELL_BATPRESZ going LOW (battery removal).
- STAT_AC is not valid(Adapter removal).
- RESET_REG is asserted and reset all registers.
- Charge voltage is written to be 0 V.
- Watch dog event is triggered.

Charge current is not reset in force converter latch off fault (REG0x20[2]), and ACOC/TSHUT/SYSOVP/ACOV/ VSYS_UVP/BATOVP/BATOC faults.

Figure 9-15. ChargeCurrent Register (I²C address = 03/02h) [reset = 0000h]

7	6	5	4	3	2	1	0
Reserved			Charge Current, bit 6	Charge Current, bit 5	Charge Current, bit 4	Charge Current, bit 3	Charge Current, bit 2
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Charge Current, bit 1	Charge Current, bit 0	Reserved	Reserved				
R/W	R/W	R/W	R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-10. Charge Current Register with 10-mΩ Sense Resistor (I²C address = 03h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-5	Reserved	R/W	000b	Not used. 1 = invalid write.
4	Charge Current, bit 6	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 4096 mA of charger current.
3	Charge Current, bit 5	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 2048 mA of charger current.
2	Charge Current, bit 4	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 1024 mA of charger current.
1	Charge Current, bit 3	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 512 mA of charger current.
0	Charge Current, bit 2	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 256 mA of charger current.

Table 9-11. Charge Current Register with 10-mΩ Sense Resistor (I²C address = 02h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Charge Current, bit 1	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 128 mA of charger current.
6	Charge Current, bit 0	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 64 mA of charger current.
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

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9.6.2.1 Battery Pre-Charge Current Clamp

During pre-charge, BATFET works in linear mode (LDO mode) (default EN_LDO= 1b). For 2-4 cell battery, the system is regulated at VSYS_MIN register and the pre-charge current is clamped at 384 mA. For 1 cell battery, the pre-charge to fast charge threshold is 3 V, and the pre-charge current is clamped at 384 mA. However, the BATFET stays in LDO mode operation untill battery voltage is above minimum system voltage (~3.6 V). During battery voltage from 3 V to 3.6 V, the fast charge current is clamped at 2 A.

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9.6.3 ChargeVoltage Register (I²C address = 05/04h) [reset value based on CELL_BATPRESZ pin setting]

To set the output charge voltage, write a 16-bit ChargeVoltage register command (REG0x05/04h()) using the data format listed in Figure 9-16, Table 9-12, and Table 9-13. The charger provides charge voltage range from 1.024 V to 19.200 V, with 8-mV step resolution. Any write below 1.024 V or above19.200 V is ignored

Upon POR, ChargeVoltage() is by default set as 4200 mV for 1 s, 8400 mV for 2 s, 12600 mV for 3 s or 16800 mV for 4 s. After CHRG_OK goes high, the charge will start when the host writes the charging current to ChargeCurrent() register, the default charging voltage is used if ChargeVoltage() is not programmed. If the battery is different from 4.2 V/cell, the host has to write to ChargeVoltage() before ChargeCurrent() register for correct battery voltage setting. Writing ChargeVoltage() to 0 should keep ChargeVoltage() value unchanged, and force ChargeCurrent() register to zero to disable charge.

The SRN pin senses the battery voltage for voltage regulation and should be connected as close to the battery as possible.

Figure 9-16. ChargeVoltage Register (I²C address = 05/04h) [reset value based on CELL_BATPRESZ pin setting]

7	6	5	4	3	2	1	0
Reserved	Charge Voltage, bit 11	Charge Voltage, bit 10	Charge Voltage, bit 9	Charge Voltage, bit 8	Charge Voltage, bit 7	Charge Voltage, bit 6	Charge Voltage, bit 5
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Charge Voltage, bit 4	Charge Voltage, bit 3	Charge Voltage, bit 2	Charge Voltage, bit 1	Charge Voltage, bit 0	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-12. ChargeVoltage Register (I²C address = 05h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Charge Voltage, bit 11	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16384 mV of charger voltage.
5	Charge Voltage, bit 10	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 8192 mV of charger voltage
4	Charge Voltage, bit 9	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 4096 mV of charger voltage.
3	Charge Voltage, bit 8	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 2048 mV of charger voltage.
2	Charge Voltage, bit 7	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 1024 mV of charger voltage.
1	Charge Voltage, bit 6	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 512 mV of charger voltage.
0	Charge Voltage, bit 5	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 256 mV of charger voltage.

Table 9-13. ChargeVoltage Register (I²C address = 04h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Charge Voltage, bit 4	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 128 mV of charger voltage.
6	Charge Voltage, bit 3	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 64 mV of charger voltage.

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Table 9-13. ChargeVoltage Register (I^2C address = 04h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
5	Charge Voltage, bit 2	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 32 mV of charger voltage.
4	Charge Voltage, bit 1	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16 mV of charger voltage.
3	Charge Voltage, bit 0	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 8 mV of charger voltage.
2-0	Reserved	R/W	000b	Not used. Value Ignored.

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9.6.4 ChargerStatus Register (I²C address = 21/20h) [reset = 0000h]

Figure 9-17. ChargerStatus Register (I²C address = 21/20h) [reset = 0000h]

7	6	5	4	3	2	1	0
STAT_AC	ICO_DONE	IN_VAP	IN_VINDPM	IN_IIN_DPM	IN_FCHRG	IN_PCHRG	IN_OTG
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Fault ACOV	Fault BATOC	Fault ACOC	FAULT SYSOVP	Fault VSYS _UVP	Fault Force_Converte r_Off	Fault_OTG _OVP	Fault_OTG _UVP
R	R	R	R/W	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-14. ChargerStatus Register (I²C address = 21h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	STAT_AC	R	0b	Input source status. STAT_AC is valid as long as VBUS go within 3.5-V to 26-V range. It is different from CHRG_OK bit, When CHRG_OK is valid, STAT_AC must be valid, but if STAT_AC is valid, it is not necessary CHRG_OK is valid. There are Force converter off, ACOC, TSHUT , SYSOVP, VSYS_UVP, BATOVP can pull low CHRG_OK. 0b: Input not present 1b: Input is present
6	ICO_DONE	R	0b	After the ICO routine is successfully executed, the bit goes 1. 0b: ICO is not complete 1b: ICO is complete
5	IN_VAP	R	0b	0b: Charger is not operated in VAP mode 1b: Charger is operated in VAP mode Digital status bit indicates VAP has enabled(1) or disabled(0). The enable of VAP mode only follows the host command, which is not blocked by any status of /PROCHOT. The exit of VAP mode also follows the host command, except that any faults will exit VAP mode automatically. STAT_EXIT_VAP (REG0x21[8]) becomes 1 which will pull low /PROCHOT until host clear. The host can enable VAP by setting OTG/VAP/FRS pin high and 0x32[5]=0, disable VAP by setting either OTG/VAP/FRS pin low or 0x32[5]=1. Any faults in VAP When IN_VAP bit goes 0->1, charger should disable VINDPM, IIN_DPM, ICRIT, ILIM pin, disable PP_ACOK if it is enabled, enable PP_VSYS if it is disabled. When IN_VAP bit goes 1->0, charger should enable VINDPM, IIN_DPM, ICRIT, ILIM pin function.
4	IN_VINDPM	R	0b	0b: Charger is not in VINDPM during forward mode, or voltage regulation during OTG mode 1b: Charger is in VINDPM during forward mode, or voltage regulation during OTG mode
3	IN_IIN_DPM	R	0b	0b: Charger is not in IIN_DPM during forward mode. 1b: Charger is not in IIN_DPM during forward mode.
2	IN_FCHRG	R	0b	0b: Charger is not in fast charge 1b: Charger is in fast charger
1	IN_PCHRG	R	0b	0b: Charger is not in pre-charge 1b: Charger is in pre-charge

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Table 9-14. ChargerStatus Register (I²C address = 21h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
0	IN_OTG	R	0b	0b: Charger is not in OTG 1b: Charge is in OTG

Table 9-15. ChargerStatus Register (I²C address = 20h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Fault ACOV	R	0b	The status are latched if triggered until a read from host. 0b: No fault 1b: ACOV
6	Fault BATOC	R	0b	The status is latched if triggered until a read from host. Fault indicator for BATOC only during normal operation. However, in PTM mode when EN_BATOC=1b, this status bit is fault indicator for both BATOVP and BATOC; when EN_BATOC=0b, this status bit is not effective. 0b: No fault 1b: BATOC is triggered
5	Fault ACOC	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: ACOC
4	Fault SYSOVP	R/W	0b	SYSOVP Status and Clear. SYSOVP fault is latched until a clear from host by writing this bit to 0. When the SYSOVP occurs, this bit is HIGH. During the SYSOVP, the converter is disabled. After the SYSOVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the SYSOVP condition to enable the converter again. 0b: Not in SYSOVP <default at POR> 1b: In SYSOVP. When SYSOVP is removed, write 0 to clear the SYSOVP latch.
3	Fault VSYS_UVP	R/W	0b	VSYS_UVP fault status and clear. VSYS_UVP fault is latched until a clear from host by writing this bit to 0. 0b: No fault <default at POR> 1b: When system voltage is lower than VSYS_UVP, then 7 times restart tries are failed.
2	Fault Force_Converter_Off	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: Force converter off triggered (when FORCE_CONV_OFF (REG0x30[3])=1b)
1	Fault_OTG_OVP	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: OTG OVP fault is triggered
0	Fault_OTG_UVP	R	0b	The status is latched if triggered until a read from host. 0b: No fault 1b: OTG UVP fault is triggered

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9.6.5 ProchotStatus Register (I²C address = 23/22h) [reset = B800h]

All the status bits in REG0x23[7,2],REG0x23[6:0] will be cleared after host read.

Figure 9-18. ProchotStatus Register (I²C address = 23/22h) [reset = B800h]

7	6	5	4	3	2	1	0
Reserved	EN_PROCHOT _EXT	PROCHOT_WIDTH		PROCHOT_CLEAR	Reserved	STAT_VAP_FAIL	STAT_EXIT_VAP
R	R/W	R/W		R/W	R	R/W	R/W
7	6	5	4	3	2	1	0
STAT_VINDPM	STAT_COMP	STAT_ICRIT	STAT_INOM	STAT_IDCHG1	STAT_VSYS	STAT_BAT_Removal	STAT_ADPT_Removal
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-16. ProchotStatus Register (I²C address = 23h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	1b	Reserved
6	EN_PROCHOT _EXT	R/W	0b	$\overline{\text{PROCHOT}}$ Pulse Extension Enable. When pulse extension is enabled, keep the $\overline{\text{PROCHOT}}$ pin voltage LOW until host writes PROCHOT _CLEAR = 0b. 0b: Disable pulse extension <default at POR> 1b: Enable pulse extension
5-4	PROCHOT _WIDTH	R/W	11b	$\overline{\text{PROCHOT}}$ Pulse Width Minimum $\overline{\text{PROCHOT}}$ pulse width when EN_PROCHOT _EXT = 0b 00b: 100 us 01b: 1 ms 10b: 5 ms 11b: 10 ms <default at POR>
3	PROCHOT _CLEAR	R/W	1b	$\overline{\text{PROCHOT}}$ Pulse Clear. Clear $\overline{\text{PROCHOT}}$ pulse when EN_PROCHOT _EXT = 1b. 0b: Clear $\overline{\text{PROCHOT}}$ pulse and drive $\overline{\text{PROCHOT}}$ pin HIGH 1b: Idle <default at POR>
2	TSHUT	R	0b	TSHUT trigger: 0b: TSHUT is not triggered 1b: TSHUT is triggered
1	STAT_VAP_FAIL	R/W	0b	This status bit reports a failure to load VBUS 7 consecutive times in VAP mode, which indicates the battery voltage might be not high enough to enter VAP mode, or the VAP loading current settings are too high. 0b: Not is VAP failure <default at POR> 1b: In VAP failure, the charger exits VAP mode, and latches off until the host writes this bit to 0.
0	STAT_EXIT_VAP	R/W	0b	When the charger is operated in VAP mode, it can exit VAP by either being disabled through host, or there are ACOV/ACOC/ SYSOVP/BATOVP/VSYS_UVP faults. 0b: PROCHOT_EXIT_VAP is not active <default at POR> 1b: PROCHOT_EXIT_VAP is active, $\overline{\text{PROCHOT}}$ pin is low until host writes this status bit to 0.

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Table 9-17. ProchotStatus Register (I^2C address = 22h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	STAT_VINDPM	R/W	0b	$\overline{\text{PROCHOT}}$ Profile VINDPM status bit 0b: Not triggered 1b: Triggered, $\overline{\text{PROCHOT}}$ pin is low until host writes this status bit to 0 when PP_VINDPM = 1b
6	STAT_COMP	R	0b	$\overline{\text{PROCHOT}}$ Profile CMPOUT status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
5	STAT_ICRIT	R	0b	$\overline{\text{PROCHOT}}$ Profile ICRIT status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
4	STAT_INOM	R	0b	$\overline{\text{PROCHOT}}$ Profile INOM status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
3	STAT_IDCHG1	R	0b	$\overline{\text{PROCHOT}}$ Profile IDCHG1 status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
2	STAT_VSYS	R	0b	$\overline{\text{PROCHOT}}$ Profile VSYS status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
1	STAT_Battery_Removal	R	0b	$\overline{\text{PROCHOT}}$ Profile Battery Removal status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered
0	STAT_Adapter_Removal	R	0b	$\overline{\text{PROCHOT}}$ Profile Adapter Removal status bit. The status is latched until a read from host. 0b: Not triggered 1b: Triggered

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9.6.6 IIN_DPM Register (I²C address = 25/24h) [reset = 4100h]

IIN_DPM register reflects the actual input current limit programmed in the register, either from IIN_HOST register or from ICO.

After ICO, the current limit used by DPM regulation may differ from the IIN_HOST register settings. The actual DPM limit is reported in IIN_DPM register.

To read the nominal or typical input current limit

- When using a 10-mΩ sense resistor (RSNS_RAC=0b). There is 50-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes.
- When using a 5-mΩ sense resistor (RSNS_RAC=1b). There is 100-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes.

To read the maximum input current limit, need to add 100 mA/200 mA offset based on above nominal input current limit reading approach.

- When using a 10-mΩ sense resistor (RSNS_RAC=0b). There is 150-mA offset at code 0 and this 150 mA offset is only applied to code 0, 100-mA offset should be added for all other non-zero codes.
- When using a 5-mΩ sense resistor (RSNS_RAC=1b). There is 300-mA offset at code 0 and this 300 mA offset is only applied to code 0, 200-mA offset should be added for all other non-zero codes

Figure 9-19. IIN_DPM Register with 10-mΩ Sense Resistor (I²C address = 25/24h) [reset = 4100h]

7	6	5	4	3	2	1	0
Reserved	Input Current in DPM, bit 6	Input Current in DPM, bit 5	Input Current in DPM, bit 4	Input Current in DPM, bit 3	Input Current in DPM, bit 2	Input Current in DPM, bit 1	Input Current in DPM, bit 0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-18. IIN_DPM Register with 10-mΩ Sense Resistor (I²C address = 25h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	0b	Not used. 1 = invalid write.
6	Input Current in DPM, bit 6	R	0b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
5	Input Current in DPM, bit 5	R	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
4	Input Current in DPM, bit 4	R	0b	0 = Adds 0 mA of input current. 1 = Adds 800mA of input current
3	Input Current in DPM, bit 3	R	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
2	Input Current in DPM, bit 2	R	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.
1	Input Current in DPM, bit 1	R	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.
0	Input Current in DPM, bit 0	R	0b	0 = Adds 0 mA of input current. 1 = Adds 50 mA of input current.

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Table 9-19. IIN_DPM Register with 10-mΩ Sense Resistor (I^2C address = 24h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

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9.6.7 ADCVBUS/PSYS Register (I²C address = 27/26h)

- PSYS: Full range: 3.06 V, LSB: 12 mV (ADC_FULLSCALE=1b)
- PSYS: Full range: 2.04 V, LSB: 8 mV (ADC_FULLSCALE=0b)
- VBUS: Full range: 0 mV to 24480 mV, LSB: 96 mV

Figure 9-20. ADCVBUS/PSYS Register (I²C address = 27/26h)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-20. ADCVBUS Register (I²C address = 27h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Voltage

Table 9-21. ADCPSYS Register (I²C address = 26h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of System Power

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9.6.8 ADCIBAT Register (I²C address = 29/28h)

- ICHG: Full range when using a 10-mΩ sense resistor (RSNS_RSR=0b):8.128 A, LSB: 64 mA.
- ICHG: Full range when using a 5-mΩ sense resistor (RSNS_RSR=1b):16.256A,LSB: 128 mA.
- IDCHG: Full range when using a 10-mΩ sense resistor (RSNS_RSR=0b):32.512 A, LSB: 256 mA. Note when discharge current is higher than 32.512 A, the ADC will report 32.512 A
- IDCHG: Full range when using a 5-mΩ sense resistor (RSNS_RSR=1b):65.024A,LSB: 512 mA. Note when discharge current is higher than 65.024 A, the ADC will report 65.024 A

Figure 9-21. ADCIBAT Register (I²C address = 29/28h)

7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-22. ADCICHG Register (I²C address = 29h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Charge Current

Table 9-23. ADCIDCHG Register (I²C address = 28h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Discharge Current

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9.6.9 ADCIIN/CMPIN Register (I²C address = 2B/2Ah)

- IIN Full range: When using a 10-mΩ sense resistor (RSNS_RAC=0b): 12.75 A, LSB: 50 mA.
- IIN Full range: When using a 5-mΩ sense resistor (RSNS_RAC=1b): 25.5A, LSB:100 mA.
- CMPIN Full range: 3.06 V, LSB: 12 mV (ADC_FULLSCALE=1b)
- CMPIN Full range: 2.04 V, LSB: 8 mV (ADC_FULLSCALE=0b)

Figure 9-22. ADCIIN/CMPIN Register (I²C address = 2B/2Ah)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-24. ADCIIN Register (I²C address = 2Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Current

Table 9-25. ADCCMPIN Register (I²C address = 2Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of CMPIN voltage

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9.6.10 ADCVSYS/VBAT Register (I²C address = 2D/2Ch)

- VSYS: Full range: 2.88 V to 19.2 V, LSB: 64 mV (1S-4S)
- VBAT: Full range: 2.88 V to 19.2 V, LSB: 64 mV (1S-4S)

Figure 9-23. ADCVSYS/VBAT Register (I²C address = 2D/2Ch)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-26. ADCVSYS Register (I²C address = 2Dh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of System Voltage

Table 9-27. ADCVSYSVBAT Register (I²C address = 2Ch) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Battery Voltage

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9.6.11 ChargeOption1 Register (I²C address = 31/30h) [reset = 3300h]

Figure 9-24. ChargeOption1 Register (I²C address = 31/30h) [reset = 3300h]

7	6	5	4	3	2	1	0
EN_IBAT	EN_PROCHOT_LPWR	PSYS_CONFIG		RSNS_RAC	RSNS_RSR	PSYS_RATIO	EN_FAST_5MOHM
R/W	R/W	R/W		R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
CMP_REF	CMP_POL	CMP_DEG		FORCE_CONV_OFF	EN_PTM	EN_SHIP_DCHG	AUTO_WAKEUP_EN
R/W	R/W	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-28. ChargeOption1 Register (I²C address = 31h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_IBAT	R/W	0b	IBAT Enable Enable the IBAT output buffer. In low power mode (EN_LWPWR=1b), IBAT buffer is always disabled regardless of this bit value. 0b Turn off IBAT buffer to minimize Iq <default at POR> 1b: Turn on IBAT buffer
6	EN_PROCHOT_LPWR	R/W	0b	Enable $\overline{\text{PROCHOT}}$ during battery only low power mode With battery only, enable VSYS in $\overline{\text{PROCHOT}}$ with low power consumption. Do not enable this function with adapter present. Refer to Section 9.3.21.1 for more details. 0b: Disable Independent Comparator low power $\overline{\text{PROCHOT}}$ <default at POR> 1b: Enable Independent Comparator low power $\overline{\text{PROCHOT}}$
5-4	PSYS_CONFIG	R/W	11b	PSYS Enable and Definition Register Enable PSYS sensing circuit and output buffer (whole PSYS circuit). In low power mode (EN_LWPWR=1b), PSYS sensing and buffer are always disabled regardless of this bit value. 00b: PSYS=PBUS+PBAT 01b: PSYS=PBUS 10b: Reserved 11b: Turn off PSYS buffer to minimize Iq<default at POR>
3	RSNS_RAC	R/W	0b	Input sense resistor R_{AC} 0b: 10 mΩ <default at POR> 1b: 5 mΩ
2	RSNS_RSR	R/W	0b	Charge sense resistor R_{SR} 0b: 10 mΩ <default at POR> 1b: 5 mΩ
1	PSYS_RATIO	R/W	1b	PSYS Gain Ratio of PSYS output current vs total system power 0b: 0.25 µA/W 1b: 1 µA/W <default at POR>

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Table 9-28. ChargeOption1 Register (I²C address = 31h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
0	EN_FAST_5MOHM	R/W	1b	Enable fast compensation to increase bandwidth under 5 mΩ RAC (RSNS_RAC=1b) for input current up to 6.4-A application (the fast compensation will only work when IADPT pin is configured less than 160 kΩ) 0b: Turn off bandwidth promotion under RSNS_RAC=1b (Note when this bit configured as 0b, IIN_HOST DAC can be extended up to 10 A, writing IIN_HOST value higher than 10 A will be neglected, the ICHG regulation loop will be slower to guarantee stability under 6.4-A to 10-A input current range) 1b: Turn on bandwidth promotion under RSNS_RAC=1b <default at POR> (Note when this bit configured as 1b, IIN_HOST DAC is clamped at 6.4 A, writing IIN_HOST value higher than 6.4 A will be neglected, the ICHG regulation loop will be faster within 6.4-A input current range)

Table 9-29. ChargeOption1 Register (I²C address = 30h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CMP_REF	R/W	0b	Independent Comparator internal Reference 0b: 2.3 V <default at POR> 1b: 1.2 V
6	CMP_POL	R/W	0b	Independent Comparator output Polarity 0b: When CMPIN is above internal threshold, CMPOUT is LOW (internal hysteresis) <default at POR> 1b: When CMPIN is below internal threshold, CMPOUT is LOW (external hysteresis)
5-4	CMP_DEG	R/W	00b	Independent comparator deglitch time, only applied to the falling edge of CMPOUT (HIGH → LOW). 00b: Independent comparator is enabled with output deglitch time 5 µs <default at POR> 01b: Independent comparator is enabled with output deglitch time of 2 ms 10b: Independent comparator is enabled with output deglitch time of 20 ms 11b: Independent comparator is enabled with output deglitch time of 5 sec
3	FORCE_CONV_OFF	R/W	0b	Force Converter Off function When independent comparator triggers, (CMPOUT pin pulled down) converter latches off, at the same time, CHRG_OK signal goes LOW to notify the system. Charge current is also set to zero internally, but charge current register setting keeps the same. To get out of converter latches off, firstly the CMPOUT should be released to high and secondly FORCE_CONV_OFF bit should be cleared (=0b). 0b: Disable this function <default at POR> 1b: Enable this function
2	EN_PTM	R/W	0b	PTM enable register bit, it will automatically reset to zero 0b: disable PTM. <default at POR> 1b: enable PTM.

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Table 9-29. ChargeOption1 Register (I²C address = 30h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1	EN_SHIP_DCHG	R/W	0b	Discharge SRN for Shipping Mode. Used to discharge VBAT pin capacitor voltage which is necessary for battery gauge device shipping mode. When this bit is 1, discharge SRN pin down in 140 ms 20 mA. When 140 ms is over, this bit is reset to 0b automatically. If this bit is written to 0b by host before 140 ms expires, VSYS should stop discharging immediately. Note if after 140-ms SRN voltage is still not low enough for battery gauge device entering ship mode, the host may need to start a new 140-ms discharge cycle. 0b: Disable shipping mode <default at POR> 1b: Enable shipping mode
0	AUTO_WAKEUP_EN	R/W	0b	Auto Wakeup Enable When this bit is HIGH, if the battery is below VSYS_MIN , the device should automatically enable 128-mA charging current for 30 mins. When the battery is charged up above minimum system voltage, charge will terminate and the bit is reset to LOW. The charger will also exit auto wake up if host write a new charge current value to charge current register Reg0x14(). 0b: Disable <default at POR> 1b: Enable

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9.6.12 ChargeOption2 Register (I²C address = 33/32h) [reset = 00B7]

Figure 9-25. ChargeOption2 Register (I²C address = 33/32h) [reset = 00B7]

7	6	5	4	3	2	1	0
PKPWR_TOVLD_DEG		EN_PKPWR_IIN_DPM	EN_PKPWR_VSYS	PKPWR_OVLD_STAT	PKPWR_RELAX_STAT	PKPWR_TMAX[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	
7	6	5	4	3	2	1	0
EN_EXTILIM	EN_ICHG_IDCHG	Q2_OCP	ACX_OCP	EN_ACOC	ACOC_VTH	EN_BATOC	BATOC_VTH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-30. ChargeOption2 Register (I²C address = 33h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	PKPWR_TOVLD_DEG	R/W	00b	Input Overload time in Peak Power Mode 00b: 1 ms <default at POR> 01b: 2 ms 10b: 5 ms 11b: 10 ms
5	EN_PKPWR_IIN_DPM	R/W	0b	Enable Peak Power Mode triggered by input current overshoot If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by input current overshoot <default at POR> 1b: Enable peak power mode triggered by input current overshoot.
4	EN_PKPWR_VSYS	R/W	0b	Enable Peak Power Mode triggered by system voltage under-shoot If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by system voltage under-shoot <default at POR> 1b: Enable peak power mode triggered by system voltage under-shoot.
3	STAT_PKPWR_OVLD	R/W	0b	Indicator that the device is in overloading cycle. Write 0 to get out of overloading cycle. 0b: Not in peak power mode. <default at POR> 1b: In peak power mode.
2	STAT_PKPWR_RELAX	R/W	0b	Indicator that the device is in relaxation cycle. Write 0 to get out of relaxation cycle. 0b: Not in relaxation cycle. <default at POR> 1b: In relaxation mode.
1-0	PKPWR_TMAX[1:0]	R/W	00b	Peak power mode overload and relax cycle time. 00b: 20 ms <default at POR> 01b: 40 ms 10b: 80 ms 11b: 1 sec

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Table 9-31. ChargeOption2 Register (I^2C address = 32h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_EXTILIM	R/W	1b	Enable ILIM_HIZ pin to set input current limit 0b: Input current limit is set by IIN_DPM register.. 1b: Input current limit is set by the lower value of ILIM_HIZ pin and IIN_DPM register.. <default at POR>
6	EN_ICHG_IDCHG	R/W	0b	0b: IBAT pin as discharge current. <default at POR> 1b: IBAT pin as charge current.
5	Q2_OCP	R/W	1b	Q2 OCP threshold by sensing Q2 VDS 0b: 210 mV 1b: 150 mV <default at POR>
4	ACX_OCP	R/W	1b	Fixed Input current OCP threshold by sensing ACP-ACN, converter is disabled immediately when triggered non latch protection resume switching automatically after ACX comparator release. 0b: 280 mV(RSNS_RAC=0b)/200 mV(RSNS_RAC=1b) 1b: 150 mV(RSNS_RAC=0b)/100 mV(RSNS_RAC=1b) <default at POR>
3	EN_ACOC	R/W	0b	ACOC Enable Configurable Input overcurrent (ACOC) protection by sensing the voltage across ACP and ACN. Upon ACOC (after 250-µs blank-out time), converter is disabled. Non latch fault, after 250-ms falling edge de-glitch time converter starts switching automatically. 0b: Disable ACOC <default at POR> 1b: ACOC threshold 133% or 200% ILIM2
2	ACOC_VTH	R/W	1b	ACOC Limit Set MOSFET OCP threshold as percentage of IIN_DPM with current sensed from $R_{AC.}$ 0b: 133% of ILIM2 1b: 200% of ILIM2 <default at POR>
1	EN_BATOC	R/W	1b	BATOC Battery discharge overcurrent (BATOC) protection by sensing the voltage across SRN and SRP. Upon BATOC, converter is disabled. 0b: Disable BATOC 1b: Enable BATOC threshold 133% or 200% $\overline{\text{PROCHOT}}$ IDCHG_TH2 <default at POR>
0	BATOC_VTH	R/W	1b	Set battery discharge overcurrent threshold as percentage of $\overline{\text{PROCHOT}}$ battery discharge current limit. Note when SRN and SRP common voltage is low for 1S application, the BATOC threshold could be derating. 0b: 133% of $\overline{\text{PROCHOT}}$ IDCHG_TH2 1b: 200% of $\overline{\text{PROCHOT}}$ IDCHG _TH2<default at POR>

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9.6.13 ChargeOption3 Register (I²C address = 35/34h) [reset = 0434h]

Figure 9-26. ChargeOption3 Register (I²C address = 35/34h) [reset = 0434h]

7	6	5	4	3	2	1	0
EN_HIZ	RESET_REG	RESET_VINDPM	EN_OTG	EN_ICO_MODE	EN_PORT_CTRL	EN_VSYS_MIN_SOFT_SR	EN_OTG_BIGCAP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
BATFET_ENZ	EN_VBUS_VAP	OTG_VAP_MODE	IL_AVG		CMP_EN	BATFETOFF_HIZ	PSYS_OTG_IDCHG
R/W	R/W	R/W	R/W		R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-32. ChargeOption3 Register (I²C address = 35h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_HIZ	R/W	0b	Device HIZ Mode Enable When the charger is in HIZ mode, the device draws minimal quiescent current. With VBUS above UVLO. REGN LDO stays on, and system powers from battery. 0b: Device not in HIZ mode <default at POR> 1b: Device in HIZ mode
6	RESET_REG	R/W	0b	Reset Registers All the registers are reset to POR default setting except the VINDPM register. 0b: Idle <default at POR> 1b: Reset all the registers to default values. After reset, this bit goes back to 0.
5	RESET_VINDPM	R/W	0b	Reset VINDPM Threshold 0b: Idle 1b: Converter is disabled to measure VINDPM threshold. After VINDPM measurement is done, this bit goes back to 0 and converter starts. (When battery voltage is lower than VSYS_MIN this function is not recommended due to potential risk to crash system during VINDPM measurement .)
4	EN_OTG	R/W	0b	OTG Mode Enable Enable device in OTG mode when OTG/VAP/FRS pin is HIGH. 0b: Disable OTG <default at POR> 1b: Enable OTG mode to supply VBUS from battery.
3	EN_ICO_MODE	R/W	0b	Enable ICO Algorithm 0b: Disable ICO algorithm. <default at POR> 1b: Enable ICO algorithm.
2	EN_PORT_CTRL	R/W	1b	Enable BATFET control 0b: Disable BATFET control pin by HIZ $\overline{\text{BATDRV}}$ pin 1b: Enable BATFET control pin by activate $\overline{\text{BATDRV}}$ pin
1	EN_VSYS_MIN_SOFT_SR	R/W	0b	Enable VSYS_MIN soft slew rate transition 0b: Disable VSYS_MIN soft slew rate transition <default at POR> 1b:Enable VSYS_MIN soft slew rate transition (1LSB/8μs=12.5mV/μs)

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Table 9-32. ChargeOption3 Register (I²C address = 35h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
0	EN_OTG_BIGCAP	R/W	0b	Enable OTG compensation for VBUS effective capacitance larger than 33 µF 0b: Disable OTG large VBUS capacitance compensation (Recommended for VBUS effective capacitance smaller than 33 µF) <default at POR> 1b: Enable OTG large VBUS capacitance compensation (Recommended for VBUS effective capacitance larger than 33 µF)

Table 9-33. ChargeOption3 Register (I²C address = 34h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	BATFET_ENZ	R/W	0b	Turn off BATFET under battery only mode. If charger is not in battery only mode this bit is not allowed to be written to 1. Under battery only OTG mode, this bit is forced to be 0b. 0b: Not force turn off BATFET <default at POR> 1b: Force turn off BATFET
6	EN_VBUS_VAP	R/W	0b	Enable the VBUS VAP for VAP operation mode 2&3 0b: Disabled <default at POR> 1b: Enabled
5	OTG_VAP_MODE	R/W	1b	The selection of the external OTG/VAP/FRS pin control. Don't recommend to change pin control after OTG/VAP/FRS pin is pulled high. 0b: the external OTG/VAP/FRS pin controls the EN/DIS VAP mode 1b: the external OTG/VAP/FRS pin controls the EN/DIS OTG mode <default at POR>
4-3	IL_AVG	R/W	10b	Converter inductor average current clamp. It is recommended to choose the smallest option which is higher than maximum possible converter average inductor current. 00b: 6A 01b: 10A 10b: 15A <default at POR> 11b: Disabled
2	CMP_EN	R/W	1b	Enable Independent Comparator with effective low. 0b: Disabled 1b: Enabled <default at POR>
1	BATFETOFF_HIZ	R/W	0b	Control BATFET on/off during charger HIZ mode. 0b: BATFET on during charger HIZ mode <default at POR> 1b: BATFET off during charger HIZ mode
0	PSYS_OTG_IDCHG	R/W	0b	PSYS function during OTG mode. 0b: PSYS as battery discharge power minus OTG output power <default at POR> 1b: PSYS as battery discharge power only

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9.6.14 ProchotOption0 Register (I²C address = 37/36h) [reset = 4A81h(2S~4s) 4A09(1S)]

To set VSYS_TH1 threshold to trigger discharging VBUS in VAP mode, write a 6-bit Vmin Active Protection register command (REG0x37<7:2>()) using the data format listed in Figure 9-27, Table 9-34, and Table 9-35. The charger Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. The threshold range from 3.2 V (000000b) to 9.5 V (111111b) for 2s~4s and 3.2 V (000000b) to 3.9 V (000111b) for 1S, with 100-mV step resolution. There is a fixed DC offset which is 3.2 V. Under 1S application writing beyond 3.9 V will be ignored. For example 000111b and xxx111b result in same VSYS_TH1 setting 3.9 V. Upon POR, the VSYS_TH1 threshold to trigger VBUS discharge in VAP mode is 3.4 V (000010b) for 1S and 6.400 V (100000b) for 2s~4s.

Figure 9-27. ProchotOption0 Register (I²C address = 37/36h) [reset = 4A81h(2S~4s) 4A09(1S)]

7	6	5	4	3	2	1	0
ILIM2_VTH					ICRIT_DEG		PROCHOT_VINDPM_80_90
R/W	R/W	R/W	R/W	R/W	R/W		R/W
7	6	5	4	3	2	1	0
VSYS_TH1						INOM_DEG	LOWER_PROCHOT_VINDPM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-34. ProchotOption0 Register (I²C address = 37h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-3	ILIM2_VTH	R/W	01001b	I_{LIM2} Threshold 5 bits, percentage of IIN_DPM in 0x22H. Measure current between ACP and ACN. Trigger when the current is above this threshold: 00001b - 11001b: 110% - 230%, step 5% 11010b - 11110b: 250% - 450%, step 50% 11111b: Out of Range (Ignored) Default 150%, or 01001
2-1	ICRIT_DEG	R/W	01b	ICRIT Deglitch time ICRIT threshold is set to be 110% of I_{LIM2}. Typical ICRIT deglitch time to trigger $\overline{PROCHOT}$. 00b: 15 µs 01b: 100 µs <default at POR> 10b: 400 µs (max 500 µs) 11b: 800 µs (max 1 ms)
0	PROCHOT_VINDPM_80_90	R/W	0b	Lower threshold of the PROCHOT_VINDPM comparator When REG0x33[0]=1, the threshold of the PROCHOT_VINDPM comparator is determined by this bit setting. 0b: 83% of VinDPM threshold <default at POR>. 1b: 91% of VinDPM threshold

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Table 9-35. ProchotOption0 Register (I²C address = 36h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	VSYS_TH1	R/W	100000b(2S~4s) 000010b(1S)	VSYS Threshold to trigger discharging VBUS in VAP mode. Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. There is a fixed DC offset which is 3.2 V. 2S - 4s battery (Default: 6.4 V) 000000b- 111111b: 3.2 V - 9.5 V with 100-mV step size. 1S battery (Default: 3.4 V) XXX000b - XXX111b: 3.2 V - 3.9 V with 100-mV step size.
1	INOM_DEG	R/W	0b	INOM Deglitch Time INOM is always 10% above IIN_DPM register setting. Measure current between ACP and ACN. Trigger when the current is above this threshold. 0b: 1 ms(max) <default at POR> 1b: 60 ms(max)
0	LOWER_PROCHOT_VINDPM	R/W	1b	Enable the lower threshold of the PROCHOT_VINDPM comparator 0b: the threshold of the PROCHOT_VINDPM comparator follows the same VINDPM REG0x3D() setting. 1b: the threshold of the PROCHOT_VINDPM comparator is lower and determined by PROCHOT_VINDPM_80_90 bit setting. <default at POR>

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9.6.15 ProchotOption1 Register (I²C address = 39/38h) [reset = 41A0h]

Figure 9-28. ProchotOption1 Register (I²C address = 39/38h) [reset = 41A0h]

7	6	5	4	3	2	1	0
IDCHG_TH1						IDCHG_DEG1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
PP_VINDPM	PP_COMP	PP_ICRIT	PP_INOM	PP_IDCHG1	PP_VSYS	PP_BATPRES	PP_ACOK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When the REG0x38h[7:0] are set to be disabled, the $\overline{\text{PROCHOT}}$ event associated with that bit will not be reported in the $\overline{\text{PROCHOT}}$ status register REG0x22h[7:0] any more, and the $\overline{\text{PROCHOT}}$ pin will not be pulled low any more if the event happens.

Table 9-36. ProchotOption1 Register (I²C address = 39h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	IDCHG_TH1	R/W	010000b	IDCHG level 1 Threshold 6 bit, range, range 0 A to 32256 mA, step 512 mA. Measure current between SRN and SRP. Trigger when the discharge current is above the threshold. If the value is programmed to 000000b $\overline{\text{PROCHOT}}$ is always triggered. Default: 8192 mA or 010000b
1-0	IDCHG_DEG1	R/W	00b	IDCHG level 1 Deglitch Time 00b: 78 ms 01b: 1.25s <default at POR> 10b: 5s 11b: 20s

Table 9-37. ProchotOption1 Register (I²C address = 38h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	PP_VINDPM	R/W	1b	VINDPM $\overline{\text{PROCHOT}}$ Profile When all the REG0x38[7:0] , REG0x3D[1], REG0x3C[2]bits are 0, $\overline{\text{PROCHOT}}$ function is disabled. 0b: disable 1b: enable<default at POR>
6	PP_COMP	R/W	0b	Independent comparator $\overline{\text{PROCHOT}}$ Profile When not in low power mode(Battery only), use this bit to control independent comparator PROCHOT profiles. When in low power mode(Battery only), this bit will lose controllability to independent comparator PROCHOT profiles. Need to use EN_PROCHOT_LPWR to enable independent comparator and its PROCHOT profile. 0b: disable <default at POR> 1b: enable
5	PP_ICRIT	R/W	1b	ICRIT $\overline{\text{PROCHOT}}$ Profile 0b: disable 1b: enable <default at POR>
4	PP_INOM	R/W	0b	INOM $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable

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Table 9-37. ProchotOption1 Register (I^2C address = 38h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	PP_IDCHG1	R/W	0b	IDCHG1 $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable
2	PP_VSYS	R/W	0b	VSYS $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable
1	PP_BATPRES	R/W	0b	Battery removal $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable (one-shot falling edge triggered) If BATPRES is enabled in $\overline{\text{PROCHOT}}$ after the battery is removed, it will immediately send out one-shot $\overline{\text{PROCHOT}}$ pulse.
0	PP_ACOK	R/W	0b	Adapter removal $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable EN_LWPWR= 0b to assert $\overline{\text{PROCHOT}}$ pulse after adapter removal. If PP_ACOK is enabled in $\overline{\text{PROCHOT}}$ after the adapter is removed, it will be pulled low.

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9.6.16 ADCOption Register (I²C address = 3B/3Ah) [reset = 2000h]

Figure 9-29. ADCOption Register (I²C address = 3B/3Ah) [reset = 2000h]

7	6	5	4	3	2	1	0
ADC_CONV	ADC_START	ADC_FULLSCALE	Reserved				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
EN_ADC_CMPIN	EN_ADC_VBUS	EN_ADC_PSYS	EN_ADC_IIN	EN_ADC_IDCHG	EN_ADC_ICHG	EN_ADC_VSYS	EN_ADC_VBAT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The ADC registers are read in the following order: VBAT, VSYS, ICHG, IDCHG, IIN, PSYS, VBUS, CMPIN. ADC is disabled in low power mode. Before enabling ADC, low power mode should be disabled first.

Table 9-38. ADCOption Register (I²C address = 3Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ADC_CONV	R/W	0b	Typical each ADC channel conversion time is 25 ms maximum. Total ADC conversion time is the product of 25 ms and enabled channel counts. 0b: One-shot update. Do one set of conversion updates to registers REG0x29/28(), REG0x27/26(), REG0x2B/2A(), and REG0x2D/2C() after ADC_START = 1. 1b: Continuous update. Do a set of conversion updates to registers REG0x29/28(), REG0x27/26(), REG0x2B/2A(), and REG0x2D/2C()every 1 sec.
6	ADC_START	R/W	0b	0b: No ADC conversion 1b: Start ADC conversion. After the one-shot update is complete, this bit automatically resets to zero
5	ADC_FULLSCALE	R/W	1b	ADC input voltage range adjustment for PSYS and CMPIN ADC Channels. 2.04-V full scale holds 8 mV/LSB resolution and 3.06-V full scale holds 12 mV/LSB resolution 0b: 2.04 V 1b: 3.06 V <default at POR>(Not accurate for REGN<6-V application (VBUS & VSYS< 6V))
4-0	Reserved	R/W	00000b	Reserved

Table 9-39. ADCOption Register (I²C address = 3Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_ADC_CMPIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
6	EN_ADC_VBUS	R/W	0b	0b: Disable <default at POR> 1b: Enable
5	EN_ADC_PSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
4	EN_ADC_IIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
3	EN_ADC_IDCHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
2	EN_ADC_ICHG	R/W	0b	0b: Disable <default at POR> 1b: Enable

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Table 9-39. ADCOption Register (I^2C address = 3Ah) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1	EN_ADC_VSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
0	EN_ADC_VBAT	R/W	0b	0b: Disable <default at POR> 1b: Enable

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9.6.17 ChargeOption4 Register (I²C address = 3D/3Ch) [reset = 0048h]

Figure 9-30. ChargeOption4 Register (I²C address = 3D/3Ch) [reset = 0048h]

7	6	5	4	3	2	1	0
VSYS_UVP			EN_Dither		VSYS_UVP_NO_HICCUP	PP_VBUS_VAP	STAT_VBUS_VAP
R/W			R/W		R/W	R/W	R
7	6	5	4	3	2	1	0
IDCHG_DEG2		IDCHG_TH2			PP_IDCHG2	STAT_IDCHG2	STAT_PTM
R/W		R/W			R/W	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-40. ChargeOption4 Register (I²C address = 3Dh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-5	VSYS_UVP	R/W	000b	VSYS Under Voltage Lock Out After UVP is triggered the charger enters hiccup mode, and then the charger is latched off if the restart fails 7 times in 90s The hiccup mode during the UVP can be disabled by setting 0x37[10]=1.
				VSYS_UVP | 1S~ 4s | VSYS_UVP | 1S~ 4s 000b | 2.4 V(Default) | 100b | 5.6 V 001b | 3.2 V | 101b | 6.4 V 010b | 4.0 V | 110b | 7.2 V 011b | 4.8 V | 111b | 8.0 V
4-3	EN_DITHER	R/W	00b	Frequency Dither configuration 00b: Disable Dithering<default at POR> 01b: Dither 1X (±2% Fs dithering range) 10b: Dither 2X (±4% Fs dithering range) 11b: Dither 3X (±6% Fs dithering range)
2	VSYS_UVP_NO_HICCUP	R/W	0b	Disable VSYS_UVP Hiccup mode operation: 0b: Enable VSYS_UVP Hiccup mode <default at POR> 1b: Disable VSYS_UVP Hiccup mode
1	PP_VBUS_VAP	R/W	0b	VBUS_VAP $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 0b: enable
0	STAT_VBUS_VAP	R	0b	$\overline{\text{PROCHOT}}$ profile VBUS_VAP status bit. The status is latched until a read from host. 0b: Not triggered <default at POR> 1b: Triggered

Table 9-41. ChargeOption4 Register (I²C address = 3Ch) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	IDCHG_DEG2	R/W	01b	Battery discharge current limit 2 deglitch time(minimum value) 00b: 100 µs 01b: 1.6 ms <default at POR> 10b: 6 ms 11b: 12 ms

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Table 9-41. ChargeOption4 Register (I²C address = 3Ch) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
5-3	IDCHG_TH2	R/W	001b	Battery discharge current limit2 based on percentage of IDCHG_TH1. Note IDCHG_TH2 setting higher than 32256 mA should lose accuracy de-rating between target value and 32256 mA. (Recommend not to set higher than 20 A for 1S OTG boost operation) 000b: 125% IDCHG_TH1 001b: 150% IDCHG_TH1 <default at POR> 010b: 175% IDCHG_TH1 011b: 200% IDCHG_TH1 100b: 250% IDCHG_TH1 101b: 300% IDCHG_TH1 110b: 350% IDCHG_TH1 111b: 400% IDCHG_TH1
2	PP_IDCHG2	R/W	0b	IDCHG2 $\overline{\text{PROCHOT}}$ Profile 0b: disable <default at POR> 1b: enable
1	STAT_IDCHG2	R	0b	The status is latched until a read from host. 0b: Not triggered <default at POR> 1b: Triggered
0	STAT_PTM	R	0b	PTM operation status bit monitor 0b: Not in PTM Operation <default at POR> 1b: In PTM Operation

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9.6.18 Vmin Active Protection Register (I²C address = 3F/3Eh) [reset = 006Ch(2s~4s)/0004h(1S)]

To set the VAP VBUS $\overline{\text{PROCHOT}}$ trigger threshold, write a 7-bit Vmin Active Protection register command (REG0x3F[7:1]) using the data format listed in Figure 9-31 and Table 9-42. The charger provides VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger threshold range from 3.2 V (0000000b) to 15.9 V (1111111b), with 100-mV step resolution. There is a fixed offset of 3.2 V. Upon POR, the VBUS $\overline{\text{PROCHOT}}$ trigger threshold is 3.2 V (0000000b).

To set VSYS_TH2 Threshold to assert STAT_VSYS, write a 6-bit Vmin Active Protection register command (REG0x3E[7:2]) using the data format listed in Figure 9-31 and Table 9-43. The charger Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. The threshold range from 3.2 V (000000b) to 9.5 V (111111b) for 2s~4s and 3.2 V (000000b) to 3.9 V (000111b) for 1S, with 100-mV step resolution. There is a fixed DC offset which is 3.2 V. Under 1S application writing beyond 3.9 V will be ignored. For example, xxx111b and 000111b result in same VSYS_TH2 setting 3.9 V. Upon POR, the VSYS $\overline{\text{PROCHOT}}$ trigger threshold is 3.2 V (000000b) for 1S and 5.9 V (011011b) for 2s~ 4s.

Figure 9-31. Vmin Active Protection Register (I²C address = 3F/3Eh) [reset = 0070h/0004h]

7	6	5	4	3	2	1	0
VBUS_VAP_TH Bit6	VBUS_VAP_TH Bit5	VBUS_VAP_TH Bit4	VBUS_VAP_TH Bit3	VBUS_VAP_T H Bit2	VBUS_VAP_TH Bit1	VBUS_VAP_TH Bit0	Reserved
R/W							R/W
7	6	5	4	3	2	1	0
VSYS_TH2 Bit6	VSYS_TH2 Bit5	VSYS_TH2 Bit4	VSYS_TH2 Bit3	VSYS_TH2 Bit2	VSYS_TH2 Bit1	EN_TH2_FOLL OW_TH1	EN_FRS
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-42. Vmin Active Protection Register (I²C address = 3Fh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	VBUS_VAP_TH, Bit6	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 6400 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
6	VBUS_VAP_TH, Bit5	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 3200 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
5	VBUS_VAP_TH, Bit4	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 1600 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
4	VBUS_VAP_TH, Bit3	R/W	0b	0 = Adds 0 mV of VAP Mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 800 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
3	VBUS_VAP_TH, Bit2	R/W	0b	0 = Adds 0 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 400 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
2	VBUS_VAP_TH, Bit1	R/W	0b	0 = Adds 0 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 200 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
1	VBUS_VAP_TH, Bit0	R/W	0b	0 = Adds 0 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 100 mV of VAP mode VBUS $\overline{\text{PROCHOT}}$ trigger voltage threshold
0	Reserve	R/W	0b	Reserve

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Table 9-43. Vmin Active Protection Register (I²C address = 3Eh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	VSYS_TH2, Bit5	R/W	0b	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 3200 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
6	VSYS_TH2, Bit4	R/W	1b(2S~4s) 0b(1S)	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 1600 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
5	VSYS_TH2, Bit3	R/W	1b(2S~4s) 0b(1S)	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 800 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
4	VSYS_TH2, Bit2	R/W	0b	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 400 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
3	VSYS_TH2, Bit1	R/W	0b(1S) 1b(2S~4s)	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 200 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
2	VSYS_TH2, Bit0	R/W	1b	0 = Adds 0 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold 1 = Adds 100 mV of VAP mode VSYS $\overline{\text{PROCHOT}}$ trigger voltage threshold
1	EN_VSYSTH2_FOLLOW_VSYSTH1	R/W	0b	Enable internal VSYS_TH2 follow VSYS_TH1 setting neglecting register REG37[7:2] setting 0b: disable <default at POR> 1b: enable
0	EN_FRS	R/W	0b	Fast Role Swap feature enable (note not recommend to change EN_FRS during OTG operation, the FRS bit from 0 to 1 change will disable power stage for about 50 µs (Fs = 800 kHz). HIZ mode holds higher priority, If EN_HIZ=1b, this EN_FRS bit should be forced to 0b. 0b: disable <default at POR> 1b: enable

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9.6.19 OTGVoltage Register (I²C address = 07/06h) [reset = 09C4h]

To set the OTG output voltage limit, write to REG0x07/06h() using the data format listed in Figure 9-32, Table 9-44, and Table 9-45.

The DAC is clamped in digital core at minimal 3 V and maximum 24.0 V during normal OTG operation. Any register writing lower than the minimal or higher than the maximum will be ignored.

Figure 9-32. OTGVoltage Register (I²C address = 07/06h) [reset = 09C4h]

7	6	5	4	3	2	1	0
Reserved		OTG Voltage, bit 11	OTG Voltage, bit 10	OTG Voltage, bit 9	OTG Voltage, bit 8	OTG Voltage, bit 7	OTG Voltage, bit 6
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
OTG Voltage, bit 5	OTG Voltage, bit 4	OTG Voltage, bit 3	OTG Voltage, bit 2	OTG Voltage, bit 1	OTG Voltage, bit 0	Reserved	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-44. OTGVoltage Register (I²C address = 07h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	Reserved	R/W	00b	Not used. 1 = invalid write.
13	OTG Voltage, bit 11	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 16384 mV of OTG voltage.
12	OTG Voltage, bit 10	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 8192 mV of OTG voltage.
11	OTG Voltage, bit 9	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 4096 mV of OTG voltage.
10	OTG Voltage, bit 8	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 2048 mV of OTG voltage.
9	OTG Voltage, bit 7	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 1024 mV of OTG voltage.
8	OTG Voltage, bit 6	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 512 mV of OTG voltage.

Table 9-45. OTGVoltage Register (I²C address = 06h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	OTG Voltage, bit 5	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 256 mV of OTG voltage.
6	OTG Voltage, bit 4	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 128 mV of OTG voltage.
5	OTG Voltage, bit 3	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 64 mV of OTG voltage.
4	OTG Voltage, bit 2	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 32 mV of OTG voltage.
3	OTG Voltage, bit 1	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 16 mV of OTG voltage.
2	OTG Voltage, bit 0	R/W	1b	0 = Adds 0 mV of OTG voltage. 1 = Adds 8 mV of OTG voltage.

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Table 9-45. OTGVoltage Register (I^2C address = 06h) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1-0	Reserved	R/W	00b	Not used. Value Ignored.

9.6.20 OTGCurrent Register (I²C address = 09/08h) [reset = 3C00h]

To set the OTG output current limit, write to REG0x09() using the data format listed in Figure 9-33 and Table 9-46.

Figure 9-33. OTGCurrent Register (I²C address = 09/08h) [reset = 3C00h]

7	6	5	4	3	2	1	0
Reserved	OTG Current set by host, bit 6	OTG Current set by host, bit 5	OTG Current set by host, bit 4	OTG Current set by host, bit 3	OTG Current set by host, bit 2	OTG Current set by host, bit 1	OTG Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-46. OTGCurrent Register (I²C address = 09h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	OTG Current set by host, bit 6	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 3200 mA of OTG current.
5	OTG Current set by host, bit 5	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 1600 mA of OTG current.
4	OTG Current set by host, bit 4	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 800 mA of OTG current.
3	OTG Current set by host, bit 3	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 400 mA of OTG current.
2	OTG Current set by host, bit 2	R/W	1b	0 = Adds 0 mA of OTG current. 1 = Adds 200 mA of OTG current.
1	OTG Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 100 mA of OTG current.
0	OTG Current set by host, bit 0	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 50 mA of OTG current.

Table 9-47. OTGCurrent Register (I²C address = 08h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R/W	00000000b	Not used. Value Ignored.

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9.6.21 InputVoltage(VINDPM) Register (I²C address = 0B/0Ah) [reset =VBUS-1.28V]

To set the input voltage limit, write a 16-bit InputVoltage register command (REG0x0B/0A()) using the data format listed in Figure 9-34, Table 9-48, and Table 9-49.

If the input voltage drops more than the InputVoltage register allows, the device enters VINDPM and reduces the charge current. The default setting is 1.28 V below the no-load VBUS voltage. There is a fixed DC offset 3.2 V for all codes.

Figure 9-34. InputVoltage Register (I²C address = 0B/0Ah) [reset = VBUS-1.28V]

7	6	5	4	3	2	1	0
Reserved		Input Voltage, bit 7	Input Voltage, bit 6	Input Voltage, bit 5	Input Voltage, bit 4	Input Voltage, bit 3	Input Voltage, bit 2
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Input Voltage, bit 1	Input Voltage, bit 0	Reserved					
R/W	R/W	R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-48. InputVoltage Register (I²C address = 0Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	Input Voltage, bit 7	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 8192 mV of input voltage.
4	Input Voltage, bit 6	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 4096 mV of input voltage.
3	Input Voltage, bit 5	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 2048 mV of input voltage.
2	Input Voltage, bit 4	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 1024 mV of input voltage.
1	Input Voltage, bit 3	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 512 mV of input voltage.
0	Input Voltage, bit 2	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 256 mV of input voltage.

Table 9-49. InputVoltage Register (I²C address = 0Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Input Voltage, bit 1	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 128 mV of input voltage.
6	Input Voltage, bit 0	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 64 mV of input voltage
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

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9.6.22 VSYS_MIN Register (I²C address = 0D/0Ch) [reset value based on CELL_BATPRESZ pin setting]

To set the minimum system voltage, write a 16-bit VSYS_MIN register command (REG0x3E()) using the data format listed in Figure 9-35, Table 9-50 , and Table 9-51 . The charger provides minimum system voltage range from 1.0V to 19.2V, with 100-mV step resolution. Any write below 1.0V or above 19.2V is ignored. Upon POR, the VSYS_MIN register is 3.6 V for 1 S, 6.6V for 2 S and 9.2 V for 3 S, and 12.3 V for 4 S. Writing VSYS_MIN to 0 will set it to the default value based on CELL_BATPRESZ pin.

Figure 9-35. VSYS_MIN Register (I²C address = 0D/0Ch) [reset value based on CELL_BATPRESZ pin setting]

7	6	5	4	3	2	1	0
VSYS_MIN, bit 7	VSYS_MIN, bit 6	VSYS_MIN, bit 5	VSYS_MIN, bit 4	VSYS_MIN, bit 3	VSYS_MIN, bit 2	VSYS_MIN, bit 1	VSYS_MIN, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-50. VSYS_MIN Register (I²C address = 0Dh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Min System Voltage, bit 7	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 12800 mV of system voltage.
6	Min System Voltage, bit 6	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 6400mV of system voltage.
5	Min System Voltage, bit 5	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 3200 mV of system voltage.
4	Min System Voltage, bit 4	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 1600 mV of system voltage.
3	Min System Voltage, bit 3	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 800 mV of system voltage.
2	Min System Voltage, bit 2	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 400 mV of system voltage.
1	Min System Voltage, bit 1	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 200 mV of system voltage.
0	Min System Voltage, bit 0	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 100 mV of system voltage.

Table 9-51. VSYS_MIN Register (I²C address = 0Ch) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R/W	00000000b	Not used. Value Ignored.

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9.6.23 IIN_HOST Register (I²C address = 0F/0Eh) [reset = 4100h]

To set the nominal or typical input current limit based on the adapter rated current. Write a 7-bit IIN_HOST register command using the data format listed below.

When using a 10-mΩ sense resistor (RSNS_RAC=0b), the charger provides a nominal input-current limit range of 50 mA to 6350 mA, with 50-mA resolution. The upper boundary is implemented through DAC clamp, writing value higher than limitation will be neglected. The lower boundary is implemented through 50-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes. The default nominal input current limit is 3.25 A. Upon adapter removal, the input current limit is reset to the default value of 3.25 A.

When using a 5-mΩ sense resistor (RSNS_RAC=1b) referring to Section 9.3.6, the input-current limit range can be found under certain IADPT pin, EN_FAST_5MOHM bit status. The lower boundary is implemented through 100-mA offset at code 0. Note this offset is only applied to code 0, not applied to other codes. The default current limit is 3.2 A. Due to the USB current setting requirement, the register setting specifies the maximum current instead of the typical current. Upon adapter removal, the nominal input current limit is reset to the default value of 3.2 A.

To set the maximum input current limit based on adapter rated current. Additional 100-mA (10-mΩ sense resistor)/200-mA (5-mΩ sense resistor) offset should be added based on above nominal input current limit to obtain the maximum input current limit.

The ACP and ACN pins are used to sense R_{AC} with the default value of 10 mΩ. For a 5-mΩ sense resistor, a smaller sense voltage is given and worse regulation accuracy, but at the benefit of lower conduction loss.

Instead of using the internal IIN_DPM loop, the user can build up an external input current regulation loop and have the feedback signal on the ILIM_HIZ pin.

In order to disable ILIM_HIZ pin, the host can write EN_EXTILIM=0b to disable ILIM_HIZ pin, or pull ILIM_HIZ pin above 4.0 V.

Figure 9-36. IIN_HOST Register (I²C address = 0F/0Eh) [reset = 4100h]

7	6	5	4	3	2	1	0
Reserved	Input Current set by host, bit 6	Input Current set by host, bit 5	Input Current set by host, bit 4	Input Current set by host, bit 3	Input Current set by host, bit 2	Input Current set by host, bit 1	Input Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-52. IIN_HOST Register With 10-mΩ Sense Resistor (I²C address = 0Fh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Input Current set by host, bit 6	R/W	1b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
5	Input Current set by host, bit 5	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
4	Input Current set by host, bit 4	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 800 mA of input current.
3	Input Current set by host, bit 3	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
2	Input Current set by host, bit 2	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.

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Table 9-52. IIN_HOST Register With 10-mΩ Sense Resistor (I^2C address = 0Fh) Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1	Input Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.
0	Input Current set by host, bit 0	R/W	1b	0 = Adds 0 mA of input current. 1 = Adds 50 mA of input current.

Table 9-53. IIN_HOST Register With 10-mΩ Sense Resistor (I^2C address = 0Eh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

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9.6.24 ID Registers

9.6.24.1 ManufactureID Register (I²C address = 2Eh) [reset = 40h]

Figure 9-37. ManufactureID Register (I²C address = 2Eh) [reset = 40h]

7-0
Manufacturer ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-54. ManufactureID Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION (READ ONLY)
7-0	MANUFACTURE_ID	R	40h	40h

9.6.24.2 Device ID (DeviceAddress) Register (I²C address = 2Fh) [reset = E0h]

Figure 9-38. Device ID (DeviceAddress) Register (I²C address = 2Fh) [reset = E0h]

7-0
DEVICE_ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-55. Device ID (DeviceAddress) Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	DEVICE_ID	R	BQ25723: 11 01 0000b (E0h)	BQ25723: 11 01 0000b (E0h)

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The BQ2572xEVM evaluation module (EVM) is a complete charger module for evaluating the BQ25723. The application curves were taken using the BQ2572xEVM.

At the VBUS input with a 2.2-µH or smaller inductor, a minimum 4 µF effective (4 × 10-µF MLCC) is suggested for a 45-W to 65-W adapter, and two more 10-µF MLCC capacitors are needed when power reaches 90 W. Note when VAP feature is employed, 1 × 33-µF POSCAP is recommended to be added to improve VAP feature performance and finally system CPU performance.

At the charger VSYS output terminal, a minimum 7 µF effective (7 × 10-µF 0805 package MLCC) is suggested for a 45-W to 65-W adapter, and two more 10-µF MLCC capacitors are needed when power reaches 90 W. Overall 50-µF effective distributed capacitance on VSYS net is necessary (POSCAP is preferred), these capacitors do not have to be placed at the charger VSYS output terminal, all capacitors connected to VSYS net can be counted including the input capacitor of the next stage converters.

10.2 Typical Application

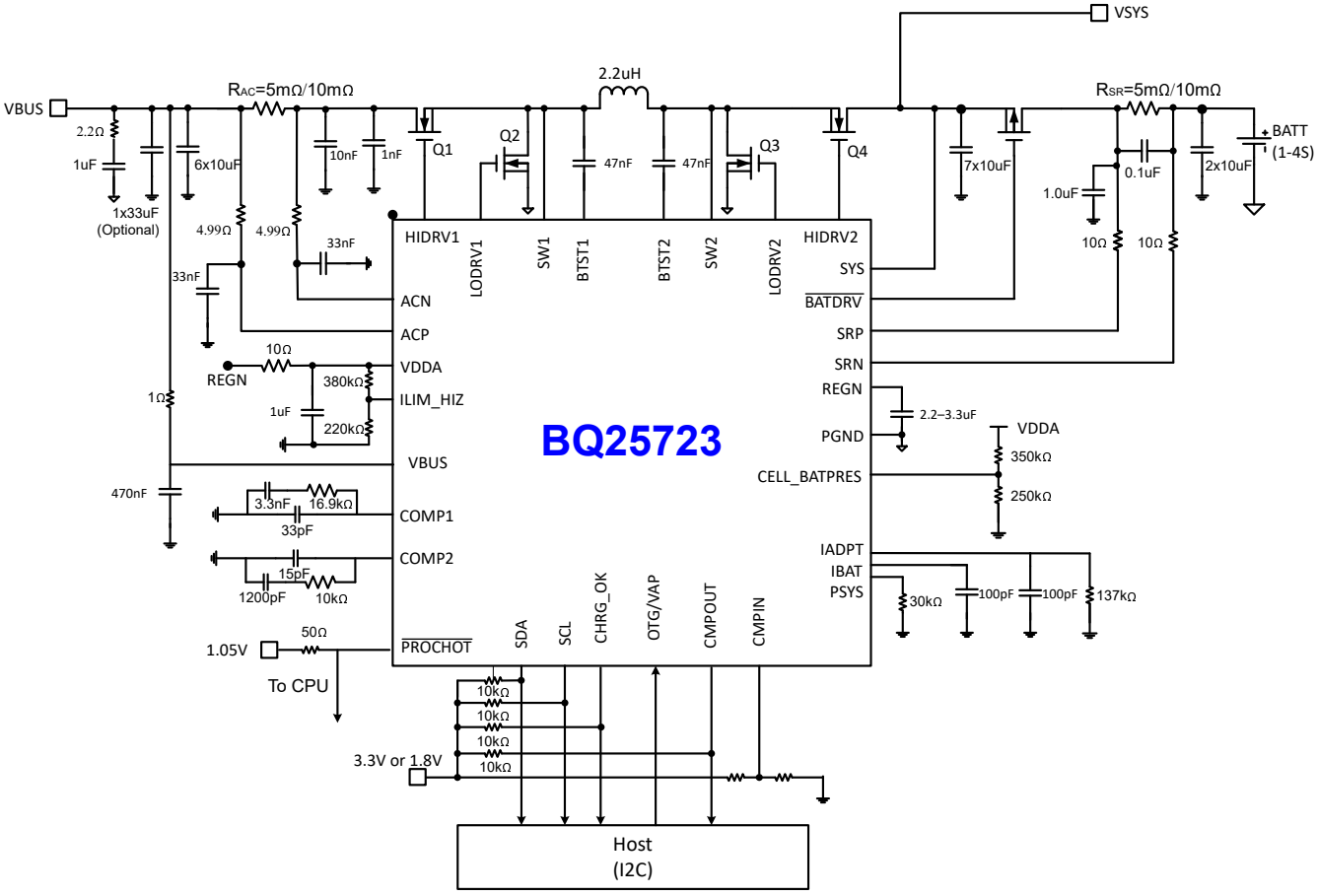

Figure 10-1. Application Diagram of BQ25723

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10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage(2)	3.5 V < Adapter Voltage < 26V
Input Current Limit (2)	3.2 A for 65-W adapter
Battery Charge Voltage(1)	8400 mV for 2s battery
Battery Charge Current(1)	3072 mA for 2s battery
Minimum System Voltage(1)	6600 mV for 2s battery

(1) Refer to battery specification for settings.
(2) Refer to adapter specification for settings for Input Voltage and Input Current Limit.

10.2.2 Detailed Design Procedure

The parameters are configurable using the evaluation software. The simplified application circuit (see Figure 10-1, as the application diagram) shows the minimum component requirements. Inductor, capacitor, and MOSFET selection are explained in the rest of this section. Refer to the EVM user's guide for the complete application schematic.

10.2.2.1 ACP-ACN Input Filter

The BQ25723 has average current mode control. The input current sensing through ACP/ACN is critical to recover inductor current ripple. Parasitic inductance on board will generate high frequency ringing on ACP-ACN which overwhelms converter sensed inductor current information. It is also difficult to manage parasitic inductance created based on different PCB layout. Larger parasitic inductance will generate larger sense current ringing which could cause the average current control loop to go into oscillation. Therefore ACP-ACN sensing information need to be conditioned.

For real system board condition, we suggest using below circuit design to get best result and filter noise induced from different PCB parasitic factor. With time constant of filter from 47 ns to 200 ns, the filter is effective and the delay of on the sensed signal is small, therefore there is no concern for average current mode control.

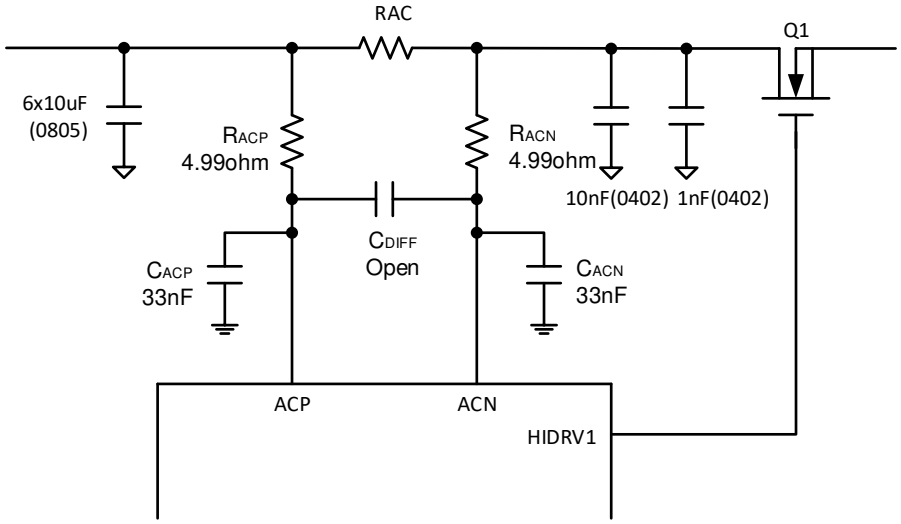

Figure 10-2. ACN-ACP Input Filter

10.2.2.2 Inductor Selection

The BQ25723 has two selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (2)$$

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The inductor ripple current in buck operation depends on input voltage (V_{IN}), duty cycle ($D_{BUCK} = V_{OUT}/V_{IN}$), switching frequency ($f_S$) and inductance (L):

$$I_{RIPPLE_BUCK} = V_{IN} \times D_{BUCK} \times (1-D_{BUCK}) / (f_S \times L) \quad (3)$$

During boost operation, the duty cycle is:

$D_{BOOST} = 1 – (V_{IN}/V_{BAT})$

and the ripple current is:

$I_{RIPPLE_BOOST} = (V_{IN} \times D_{BOOST}) / (f_S \times L)$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9 V to 12.6 V for 3-cell battery pack. For 20-V adapter voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12 V to 16.8 V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

10.2.2.3 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current (plus system current there is any system load) when duty cycle is 0.5 in buck mode. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 4:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (4)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed in front of R_{AC} current sensing and as close as possible to the power stage half bridge MOSFETs. Capacitance after R_{AC} before power stage half bridge should be limited to 10 nF + 1 nF referring to Figure 10-2 diagram. Because too large capacitance after R_{AC} could filter out R_{AC} current sensing ripple information. Voltage rating of the capacitor must be higher than normal input voltage level, 25-V rating or higher capacitor is preferred for 19-V to 20-V input voltage. The minimum input effective capacitance recommendation based on refers to Table 10-1.

Ceramic capacitors (MLCC) show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required effective capacitance value at the operating point. Considering the 25 V 0603 package MLCC capacitance derating under 19-V to 20-V input voltage, the recommended practical capacitors configuration can also be found in Table 10-1. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which is recommended for 90 W to 130 W higher power application.

Table 10-1. Minimum Input Capacitance Requirement

INPUT CAPACITORS vs TOTAL INPUT POWER	65 W	90 W	130 W
Minimum effective input capacitance	4 µF	6 µF	13 µF
Minimum practical input capacitors configuration	4*10 µF (0603 25 V MLCC)	6*10 µF (0603 25 V MLCC)	3*10 µF (0603 25 V MLCC) 1* 10 µF (25 V to 35 V POSCAP)

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10.2.2.4 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25-V X7R or X5R for output capacitor. Minimum 7 pcs of 10-µF 0603 package capacitor is suggested to be placed as close as possible to Q3&Q4 half bridge (between Q4 drain and Q3 source terminal). Total minimum output effective capacitance along VSYS distribution line is 50 µF refers to Table 10-2. Recommend to place minimum 20-µF MLCC capacitors after the charge current sense resistor for best stability.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required capacitance value at the operating point. Considering the 25-V 0603 package MLCC capacitance derating under 21-V to 23-V output voltage, the recommended practical capacitors configuration at VSYS output terminal can also be found in Table 10-2. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which are recommend to be used along VSYS output distribution line to meet total minimum effective output capacitance requirement.

Table 10-2. Minimum Output Capacitance Requirement

OUTPUT CAPACITORS vs TOTAL INPUT POWER	65 W	90 W	130 W
Minimum Effective Output Capacitance	50 µF	50 µF	50 µF
Minimum output capacitors at charger VSYS output terminal	7*10 µF (0603 25 V MLCC)	9*10 µF (0603 25 V MLCC)	9*10 µF (0603 25 V MLCC)
Additional output capacitors along VSYS distribution line	2*22 µF (25 V~35 V POSCAP)	2*22 µF (25 V~35 V POSCAP)	2*22 µF (25 V~35 V POSCAP)

10.2.2.5 Power MOSFETs Selection

Four external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are integrated into the IC with 6 V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred for 19-V to 20-V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \cdot Q_{GD};\ FOM_{bottom} = R_{DS(on)} \cdot Q_G \quad (5)$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. Taking buck mode operation as an example the power loss is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ($R_{DS(ON)_top}$), input voltage (V_{IN}), switching frequency (f_S), turn-on time (t_{on}) and turn-off time (t_{off}):

$$P_{top} = P_{con_top} + P_{sw_top} \quad (6)$$

$$P_{con_top} = D \cdot I_{L_RMS}^{\ 2} \cdot R_{DS(on)_top}; \quad (7)$$

$$I_{L_RMS}^{\ 2} = I_{L_DC}^{\ 2} + I_{ripple}^{\ 2}/12 \quad (8)$$

- I_{L_DC} is the average inductor DC current under buck mode;
- I_{ripple} is the inductor current ripple peak-to-peak value;

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$$P_{sw_top} = P_{IV_top} + P_{Qoss_top} + P_{Gate_top}; \quad (9)$$

The first item P_{con_top} represents the conduction loss which is straight forward. The second term P_{sw_top} represents the multiple switching loss items in top MOSFET including voltage and current overlap losses (P_{IV_top}), MOSFET parasitic output capacitance loss (P_{Qoss_top}) and gate drive loss (P_{Gate_top}). To calculate voltage and current overlap losses (P_{IV_top}):

$$P_{IV_top} = 0.5x\ V_{IN} \cdot I_{valley} \cdot t_{on} \cdot f_S + 0.5x\ V_{IN} \cdot I_{peak} \cdot t_{off} \cdot f_S \quad (10)$$

$$I_{valley} = I_{L_DC} - 0.5 \cdot I_{ripple} \text{ (inductor current valley value)}; \quad (11)$$

$$I_{peak} = I_{L_DC} + 0.5 \cdot I_{ripple} \text{ (inductor current peak value)}; \quad (12)$$

- t_{on} is the MOSFET turn-on time that V_{DS} falling time from V_{IN} to almost zero (MOSFET turn on conduction voltage);
- t_{off} is the MOSFET turn-off time that I_{DS} falling time from I_{peak} to zero;

The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \quad (13)$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current, and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{sw} = Q_{GD} + Q_{GS} \quad (14)$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}), and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (15)$$

To calculate top MOSFET parasitic output capacitance loss (P_{Qoss_top}):

$$P_{Qoss_top} = 0.5 \cdot V_{IN} \cdot Q_{oss} \cdot f_S \quad (16)$$

- Q_{oss} is the MOSFET parasitic output charge which can be found in MOSFET datasheet;

To calculate top MOSFET gate drive loss (P_{Gate_top}):

$$P_{Gate_top} = V_{IN} \cdot Q_{Gate_top} \cdot f_S \quad (17)$$

- Q_{Gate_top} is the top MOSFET gate charge which can be found in MOSFET datasheet;
- Note here V_{IN} is used instead of real gate drive voltage 6 V because, the gate drive 6 V is generated based on LDO from V_{IN} under buck mode, the total gate drive related loss are all considered when V_{IN} is used for gate drive loss calculation .

The bottom-side MOSFET loss also includes conduction loss and switching loss:

$$P_{bottom} = P_{con_bottom} + P_{sw_bottom} \quad (18)$$

$$P_{con_bottom} = (1 - D) \cdot I_{L_RMS}^{\ 2} \cdot R_{DS(on)_bottom}; \quad (19)$$

$$P_{sw_bottom} = P_{RR_bottom} + P_{Dead_bottom} + P_{Gate_bottom}; \quad (20)$$

The first item P_{con_bottom} represents the conduction loss which is straight forward. The second term P_{sw_bottom} represents the multiple switching loss items in bottom MOSFET including reverse recovery losses (P_{RR_bottom}),

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Dead time body diode conduction loss (P_{Dead_bottom}) and gate drive loss (P_{Gate_bottom}). The detail calculation can be found below:

$$P_{RR_bottom}=V_{IN} \cdot Q_{rr} \cdot f_S \quad (21)$$

- Q_{rr} is the bottom MOSFET reverse recovery charge which can be found in MOSFET data sheet;

$$P_{Dead_bottom}=V_F \cdot I_{valley} \cdot f_S \cdot t_{dead_rise}+V_F \cdot I_{peak} \cdot f_S \cdot t_{dead_fall} \quad (22)$$

- V_F is the body diode forward conduction voltage drop;
- t_{dead_rise} is the SW rising edge deadtime between top and bottom MOSFETs which is around 40 ns;
- t_{dead_fall} is the SW falling edge deadtime between top and bottom MOSFETs which is around 30 ns;

P_{Gate_bottom} can follow the same method as top MOSFET gate drive loss calculation approach refer to Equation 17.

P-channel MOSFETs is used for battery charging BATFET. The gate drivers are internally integrated into the IC with 10 V of gate drive voltage. 20 V or higher voltage rating MOSFETs are preferred for 1- to 4-cell battery application, the Ciss of P-channel MOSFET should be chosen less than 5 nF.

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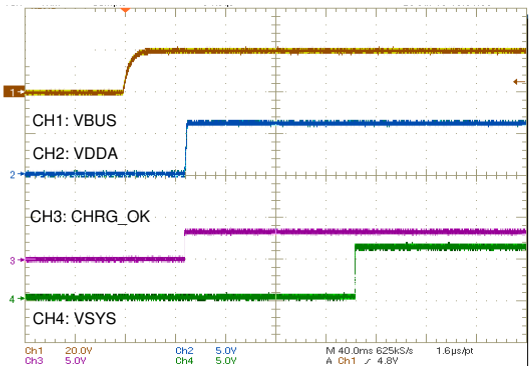
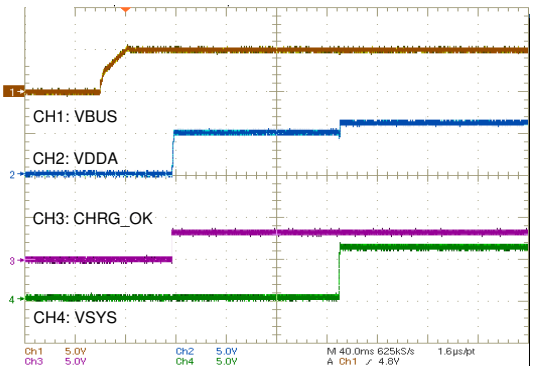
10.2.3 Application Curves



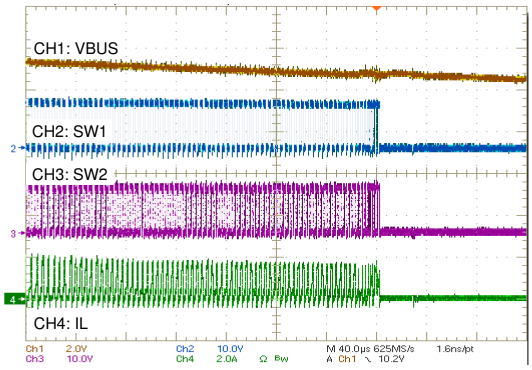
2-cell without battery

Figure 10-3. Power Up From 20 V



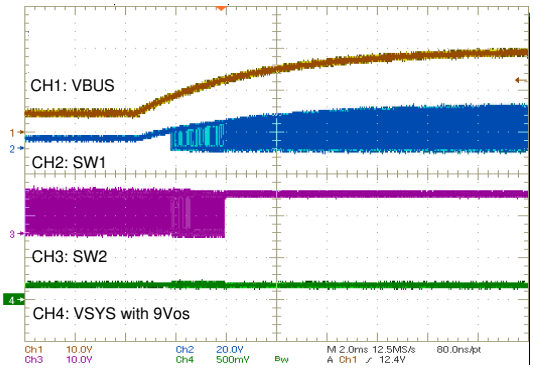
2-cell without battery

Figure 10-4. Power Up From 5 V



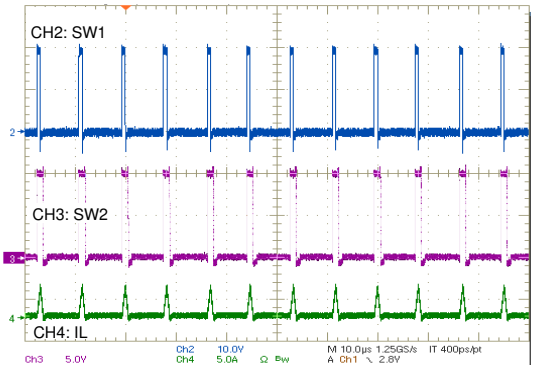
3-cell VBAT = 10 V

Figure 10-5. Power Off From 12 V



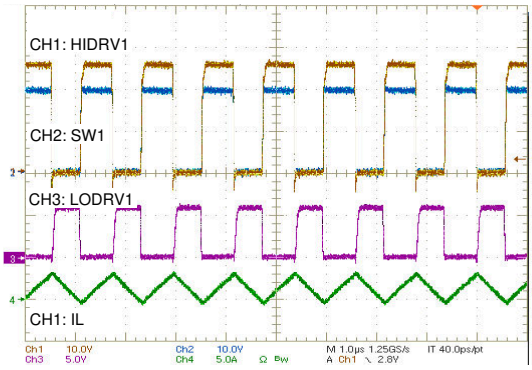
VBUS 5 V to 20 V

Figure 10-6. Line Regulation



VBUS = 20 V, VSYS = 10 V, ISYS = 200 mA

Figure 10-7. PFM Operation



VBUS = 20 V, VSYS = 10 V, ISYS = 2 A

Figure 10-8. PWM Operation

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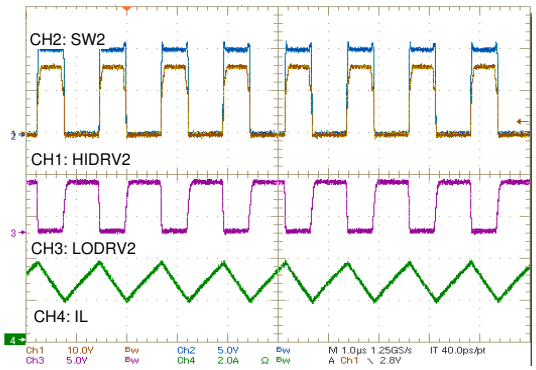
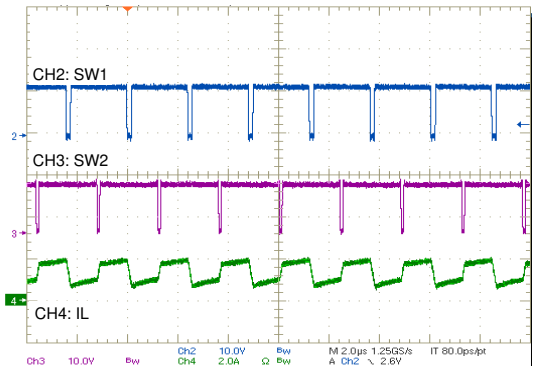


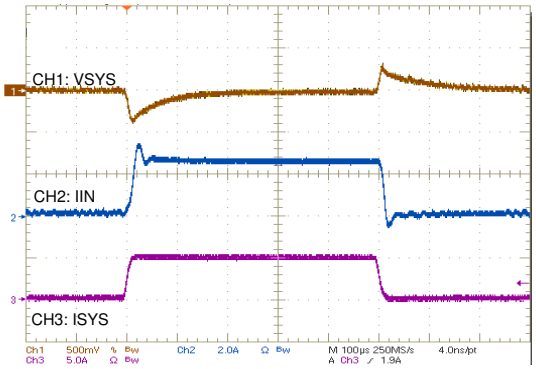
VBUS = 5 V, VBAT = 10 V

Figure 10-9. Switching During Boost Mode



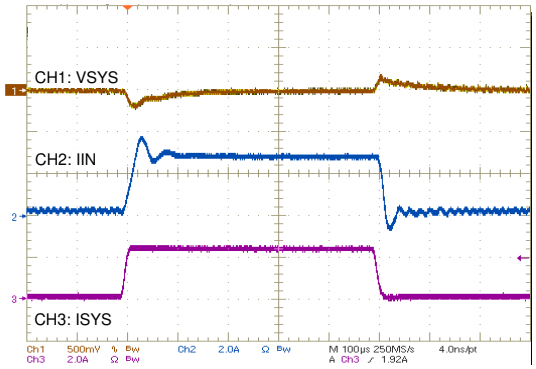
VBUS = 12 V, VBAT = 12 V

Figure 10-10. Switching During Buck Boost Mode



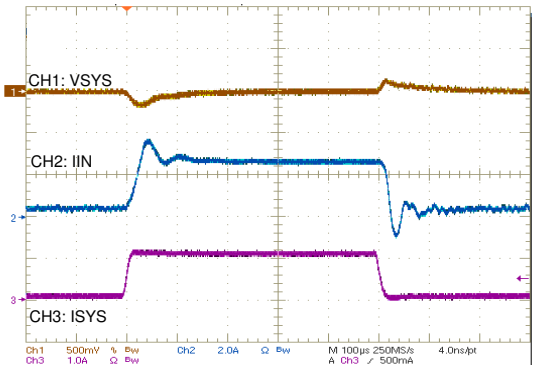
VBUS = 12 V/3.25 A, 3-cell, VSYS = 9 V, Without battery

Figure 10-11. System Regulation in Buck Mode



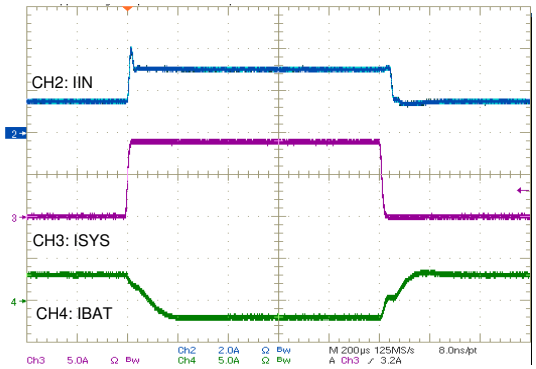
VBUS = 9 V/3.25 A, 3-cell, VSYS = 9 V, Without battery

Figure 10-12. System Regulation in Buck Boost Mode



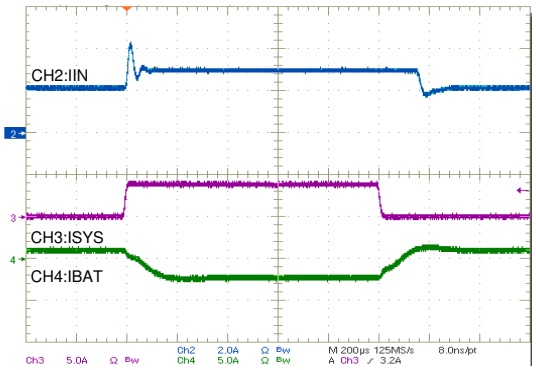
VBUS = 5 V/3.25 A, 3-cell, VSYS = 9 V, Without battery

Figure 10-13. System Regulation in Boost Mode



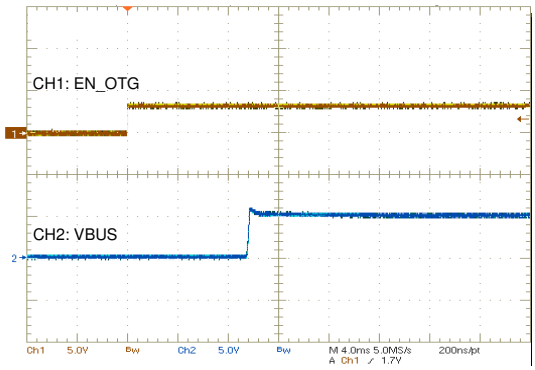
VBUS = 20 V/3.25 A, VBAT = 7.5 V

Figure 10-14. Input Current Regulation in Buck Mode



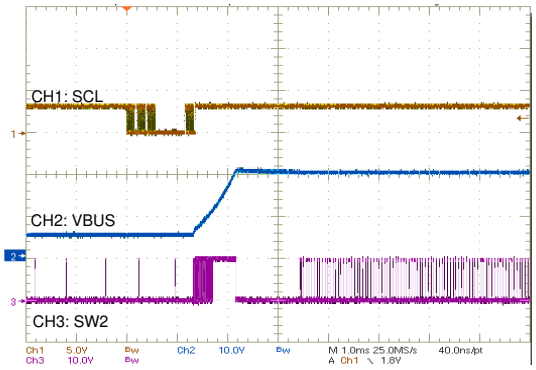
VBUS = 5 V/3.25 A, VBAT = 7.5 V

Figure 10-15. Input Current in Boost Mode



VBUS = 5 V

Figure 10-16. OTG Power Up from 8-V Battery



VBAT = 10 V, VBUS 5 V to 20 V, IOTG = 500 mA

Figure 10-17. OTG Voltage Ramp Up

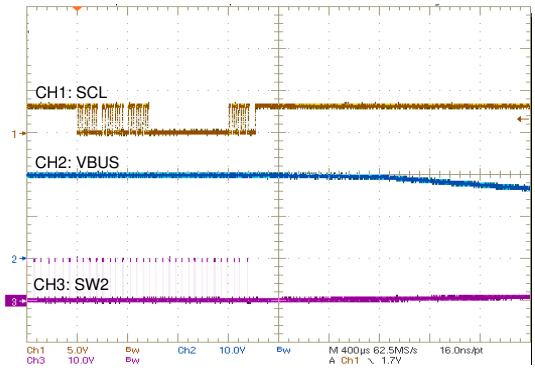
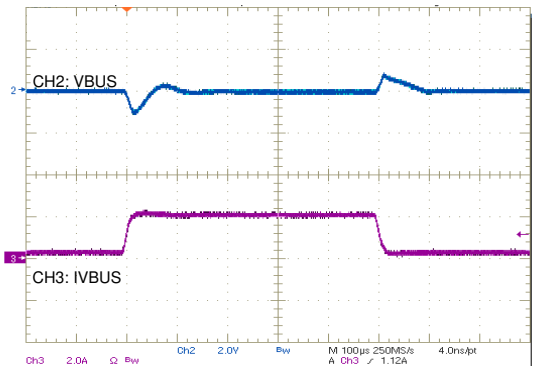
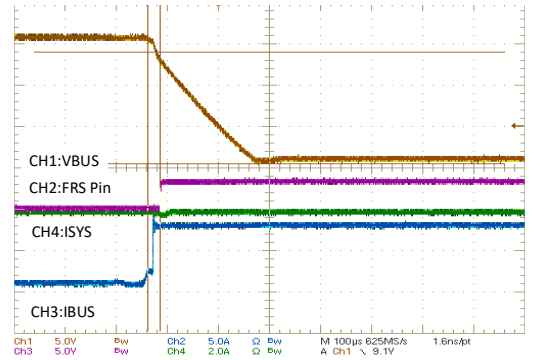


Figure 10-18. OTG Power Off



VBAT = 10 V, VBUS = 20 V

Figure 10-19. OTG Load Transient



VBUS = 20 V, VOTG = 5 V, ISYS = 5 A,VBAT = 14.8 V

Figure 10-20. FRS Transition Waveform

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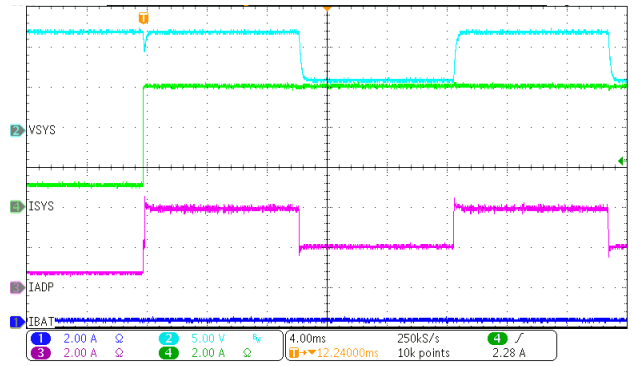
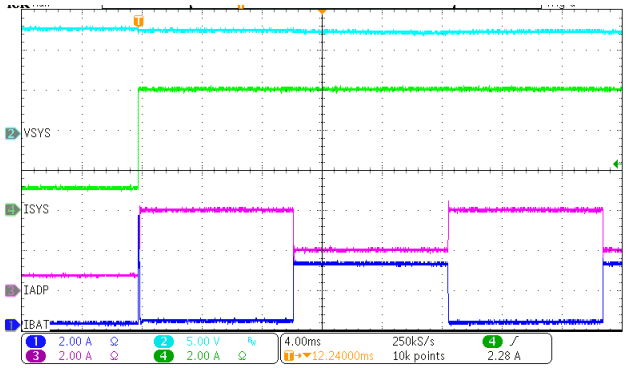


VBUS = 20 V
T_{MAX} = 20 ms
ISYS = 1 to 6 A
IIN_DPM = 2 A
T_{OVLD} = 10 ms
ICHG = 0 A
ILIM2_VTH = 200%
VSYS_MIN = 12.3 V

Figure 10-21. Peak Power Mode VSYS Trigger



VBUS = 20 V
T_{MAX} = 20 ms
ISYS = 1 to 6 A
IIN_DPM = 2 A
T_{OVLD} = 10 ms
ICHG = 0 A
ILIM2_VTH = 200%
VBAT = 12.8 V

Figure 10-22. Peak Power Mode IBUS Trigger

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11 Power Supply Recommendations

The valid adapter range is from 3.5 V (V_{VBUS_CONVEN}) to 26 V with at least 500-mA current rating. When CHRG_OK goes HIGH, the system is powered from adapter through the charger. When adapter is removed, the system is connected to battery through BATFET. Typically the battery depletion threshold should be greater than the VSYS_MIN so that the battery capacity can be fully utilized for maximum battery run time.

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12 Layout

12.1 Layout Guidelines

Proper layout of the components to minimize high frequency current path loop (see Section 12.2) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

Table 12-1. PCB Layout Guidelines

RULES	COMPONENTS	FUNCTION	IMPACT	GUIDELINES
1		PCB layer stack up	Thermal, efficiency, signal integrity	Multi- layer PCB is suggested. Allocate at least one ground layer. The BQ257XXEVM uses a 4-layer PCB (top layer, ground layer, signal layer and bottom layer).
2	CBUS, RAC, Q1, Q2	Input loop	High frequency noise, ripple	VBUS capacitors, RAC, Q1 and Q2 form a small loop 1. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CBUS to the other side of PCB for high density design. After RAC before Q1 and Q2 power stage recommend to put 10 nF + 1 nF (0402 package) decoupling capacitors as close as possible to IC to decoupling switching loop high frequency noise.
3	R_{AC}, Q1, L1, Q4	Current path	Efficiency	The current path from VBUS to VSYS, through R_{AC}, Q1, L1, Q4, has low impedance. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1 to 2A/via for a 10-mil via with 1 oz. copper thickness.
4	CSYS, Q3, Q4	Output loop	High frequency noise, ripple	VSYS capacitors, Q3 and Q4 form a small loop 2. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CSYS to the other side of PCB for high density design.
5	QBAT, R_{SR}	Current path	Efficiency, battery voltage detection	Place QBAT and R_{SR} near the battery terminal. The current path from VBAT to VSYS, through R_{SR} and QBAT, has low impedance. Pay attention to via resistance if they are not on the same side. The device detects the battery voltage through SRN near battery terminal.
6	Q1, Q2, L1, Q3, Q4	Power stage	Thermal, efficiency	Place Q1, Q2, L1, Q3 and Q4 next to each other. Allow enough copper area for thermal dissipation. The copper area is suggested to be 2x to 4x of the pad size. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
7	R_{AC}, R_{SR}	Current sense	Regulation accuracy	Use Kelvin-sensing technique for R_{AC} and R_{SR} current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs.
8	Small capacitors	IC bypass caps	Noise, jittering, ripple	Place VBUS cap, VCC cap, REGN caps near IC.
9	BST capacitors	HS gate drive	High frequency noise, ripple	Place HS MOSFET boost strap circuit capacitor close to IC and on the same side of PCB board. Capacitors SW1/2 nodes are recommended to use wide copper polygon to connect to power stage and capacitors BST1/2 node are recommended to use at least 8mil trace to connected to IC BST1/2 pins.

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Table 12-1. PCB Layout Guidelines (continued)

RULES	COMPONENTS	FUNCTION	IMPACT	GUIDELINES
10		Ground partition	Measurement accuracy, regulation accuracy, jitters, ripple	Separate analog ground(AGND) and power grounds(PGND) is preferred. PGND should be used for all power stage related ground net. AGND should be used for all sensing, compensation and control network ground for example ACP/ACN/COMP1/ COMP2/CMPIN/CMPOUT/IADPT/IBAT/PSYS. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. If possible, use dedicated COMP1, COMP2 AGND traces. Connect analog ground and power ground together using power pad as the single ground connection point.

12.2 Layout Example

12.2.1 Layout Example Reference Top View

Based on the above layout guidelines, the buck-boost charger layout example top view is shown below including all the key power components.

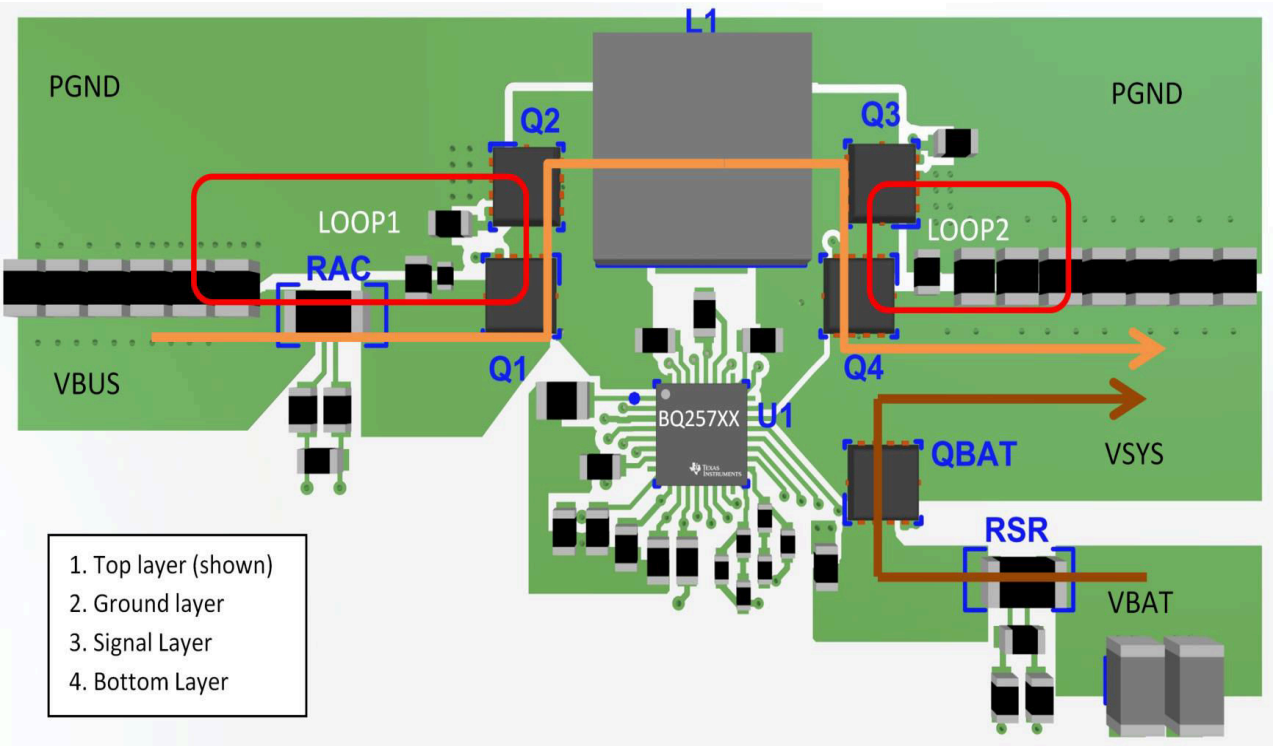

Figure 12-1. Buck-Boost Charger Layout Reference Example Top View

12.2.2 Inner Layer Layout and Routing Example

For both input sensing resistor and charging current sensing resistor, differential sensing and routing method are suggested and highlighted in below figure. Use wide trace for gate drive traces, minimum 15 mil trace width. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. Suggest using dedicated COMP1, COMP2 analog ground traces shown in below figure.

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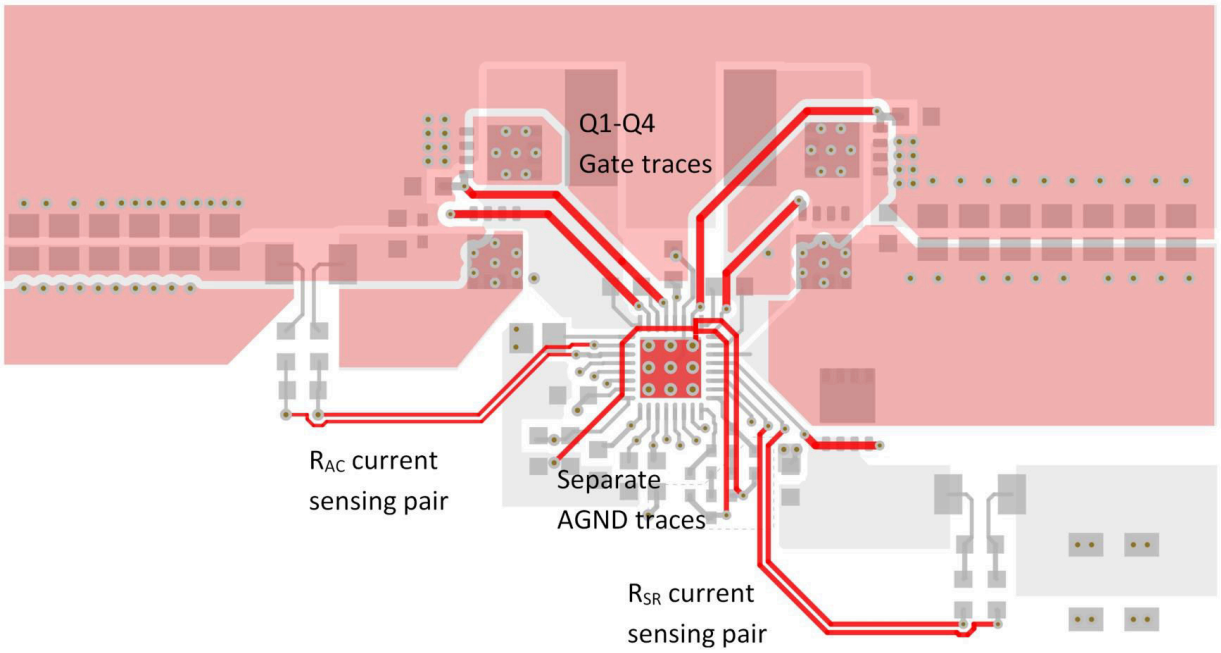

Figure 12-2. Buck-Boost Charger Gate Drive/Current Sensing/AGND Signal Layer Routing Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics Application Report*
- *BQ2571x Evaluation Module User's Guide*
- *QFN/SON PCB Attachment Application Report*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25723RSNR	Active	Production	QFN (RSN) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQ25723
BQ25723RSNR.A	Active	Production	QFN (RSN) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQ25723

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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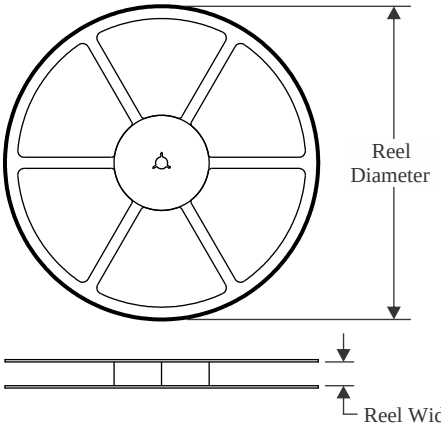
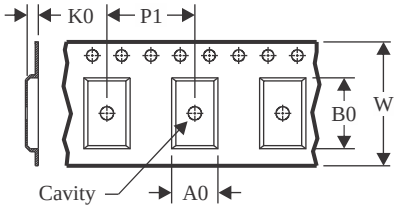
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

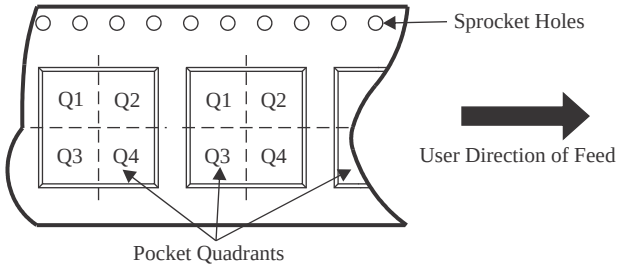


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

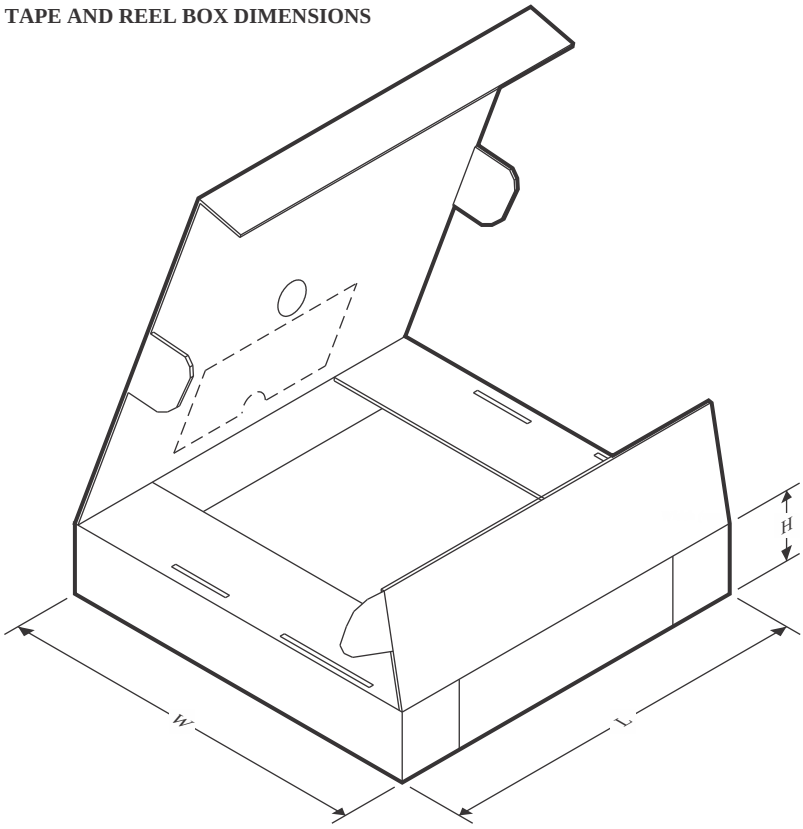
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25723RSNR	QFN	RSN	32	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25723RSNR	QFN	RSN	32	3000	356.0	356.0	36.0

GENERIC PACKAGE VIEW

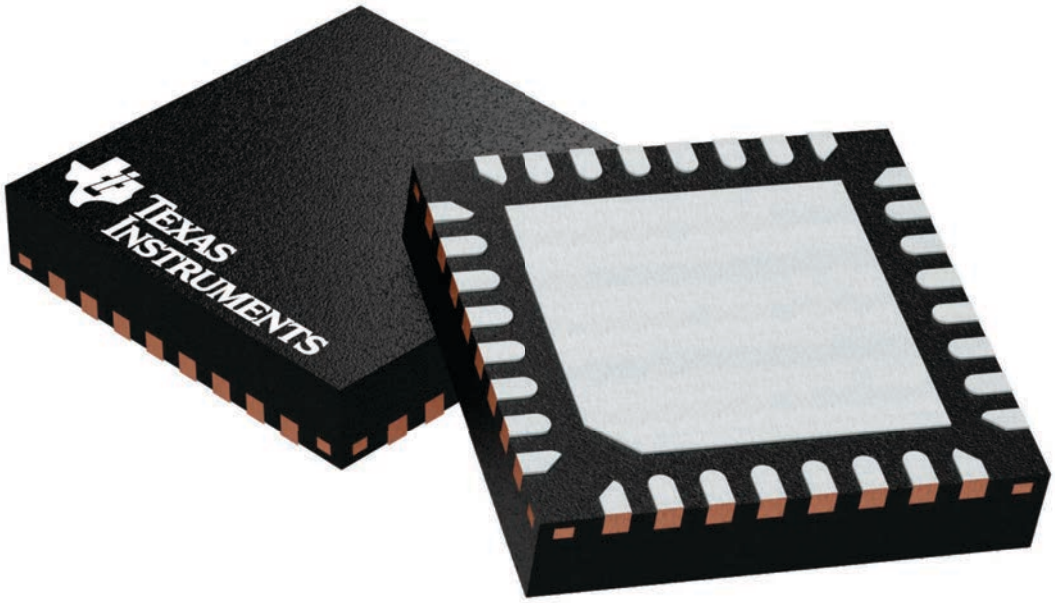
RSN 32

WQFN - 0.8 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



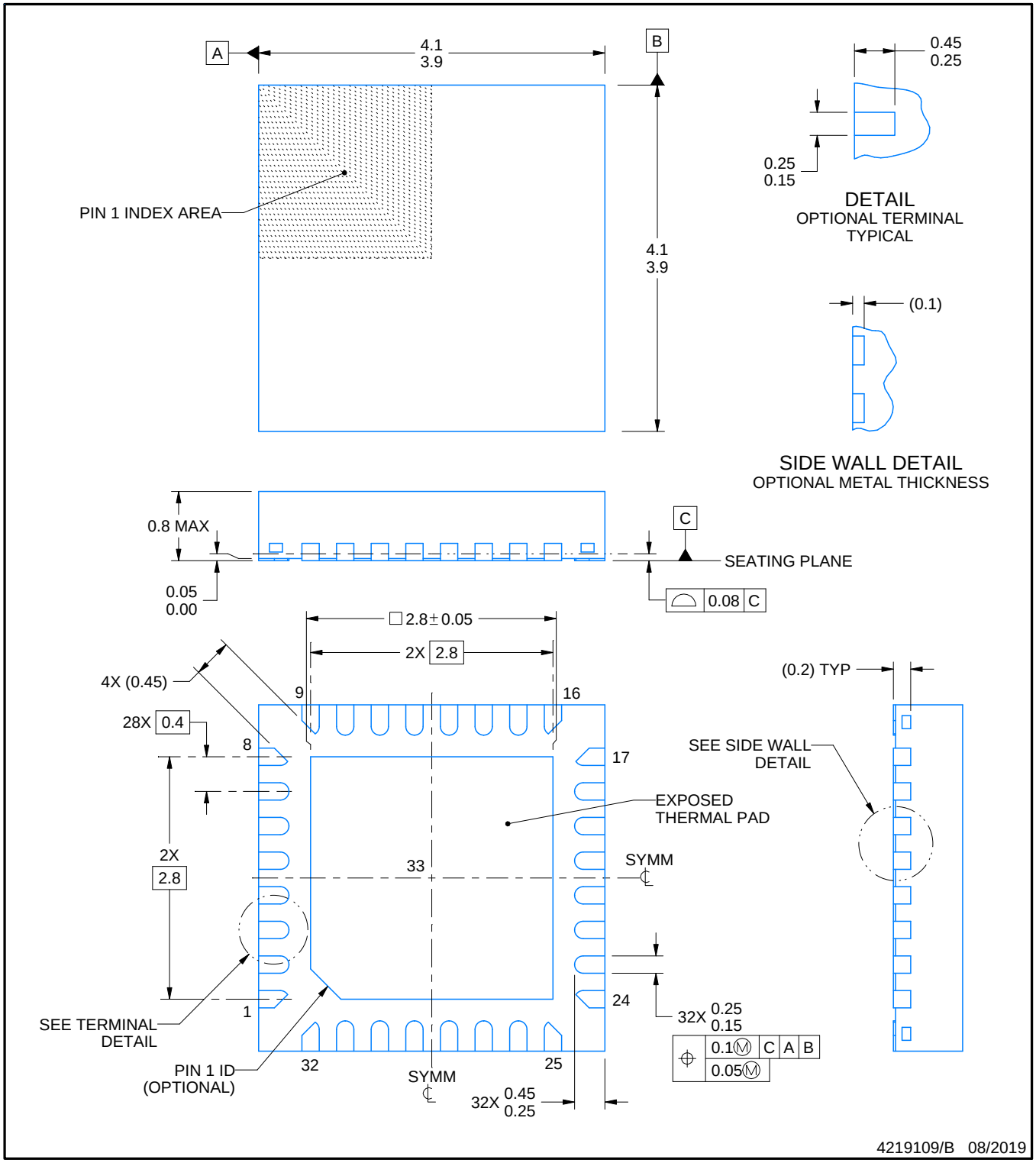
4225265/A

PACKAGE OUTLINE

RSN0032B

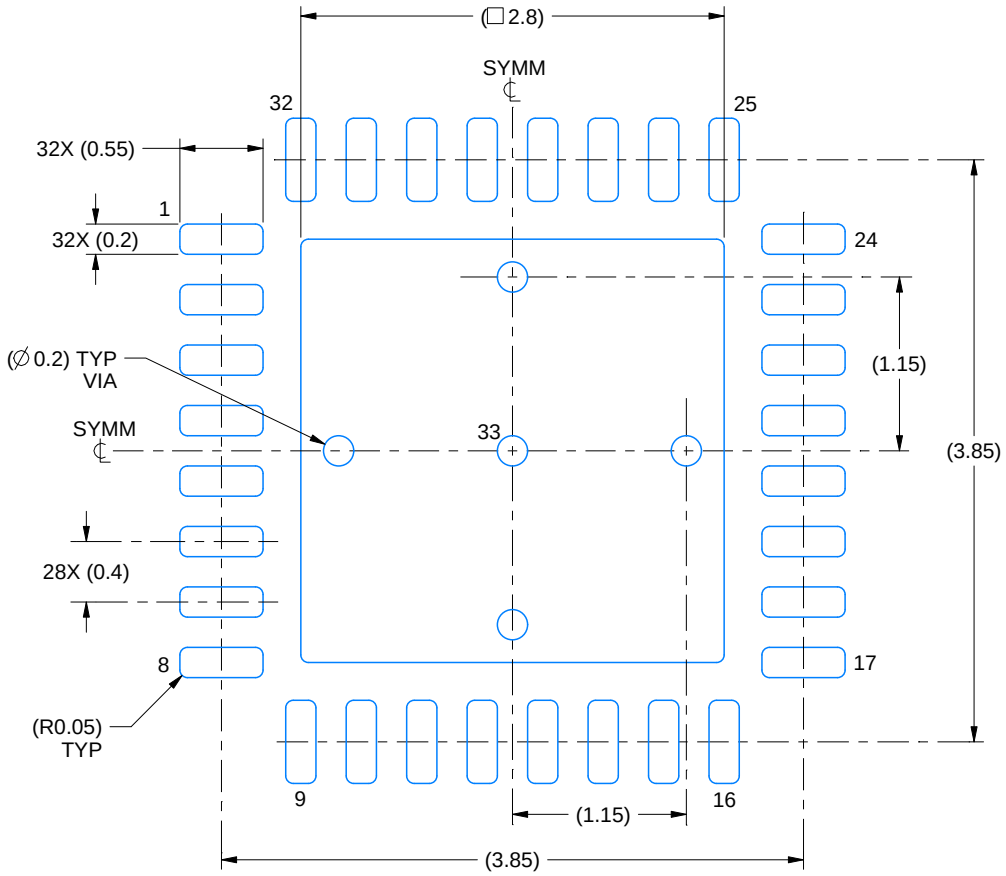
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

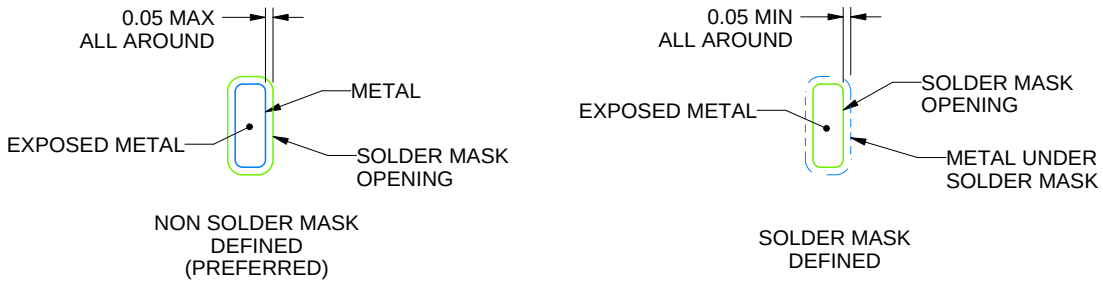


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

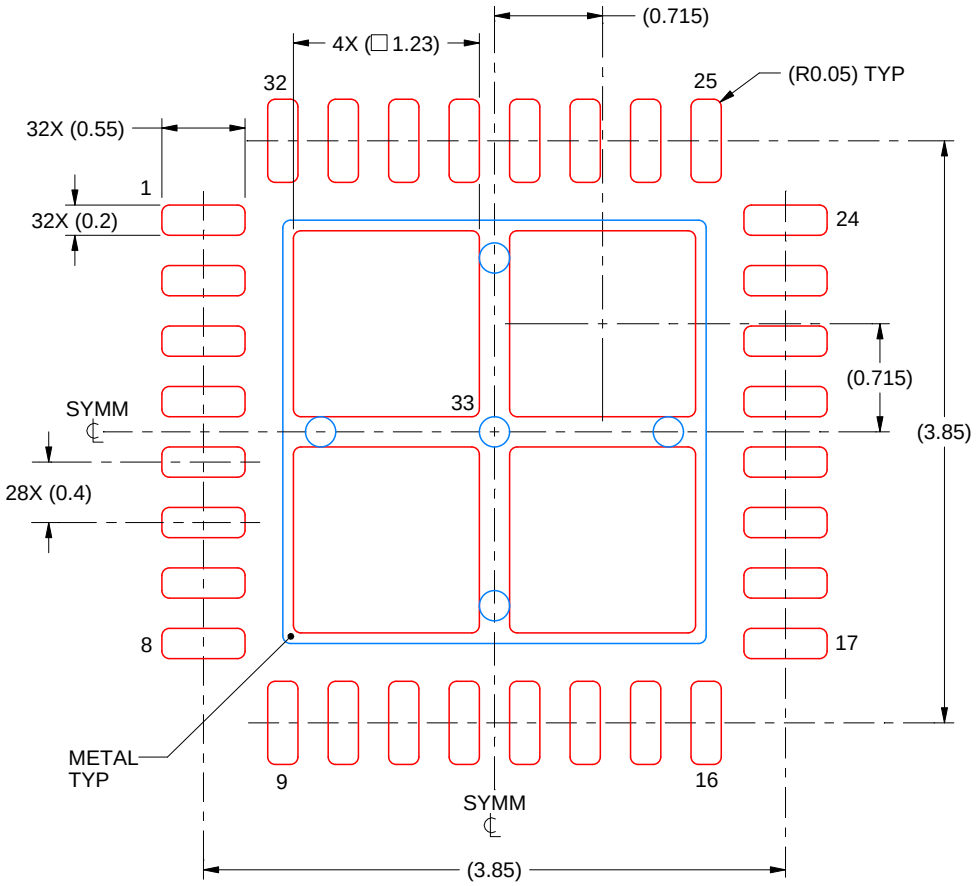


SOLDER MASK DETAILS

4219109/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219109/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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