BQ25690: Standalone/I²C Controlled, 34V, 1- to 7-Cell Li-Ion, 3A Buck-Boost Bidirectional NVDC Battery Charger with Bypass Mode and USB-PD OTG Output

1 Features

- High integration buck-boost forward (sink) mode charger for 1- to 7cell Li-Ion batteries supporting USB PD profile with integrated switching MOSFETs and loop compensation
- Highly efficient
  - Programmable switching frequency from 450kHz to 1.2MHz
  - Bypass mode for >98.0% efficiency USB-PD PPS direct battery charging at 20V, 3A
  - Selectable PFM with out-of-audio (OOA) operation for light load efficiency improvement
- Supports a wide range of input sources with 2.5V to 34V operating range and 45V absolute maximum rating
  - Support V_{IN} down to 2.5V with V_{BAT} > 3.2V
  - USB-PD input
  - Input voltage dynamic power management (VINDPM) up to 34V to avoid input crashing
  - Optional input current dynamic power management (IINDPM) up-to 3.3A for maximum power limit
- Optional Narrow voltage DC (NVDC) power path management
  - System instant-on with depleted or no battery
  - Battery supplements system when the adapter is fully loaded
- I2C controlled for optimal system performance with resistor-programmable option
  - Hardware selectable default cell count, charge voltage, input and charge current limits
  - 3.3A charging current with 20mA resolution
- Reverse/OTG (source) mode powers input port from battery
  - 3.5V to 34V reverse output voltage with 20mV resolution to support USB-PD PPS
  - Up-to 3.3A reverse output current regulation with 20mA resolution to support USB-PD PPS
- Low quiescent current
  - 6.5µA for battery only operation
  - 700µA for converter switching operation
- High accuracy
  - ±0.5% charge voltage regulation
  - ±5% input/output current regulation
- Safety
  - Input and battery OVP
  - Thermal regulation and thermal shutdown
  - Converter MOSFETs OCP
  - Charging safety timer

2 Applications

- Video doorbell, Smart home control
- Data concentrators, Wireless speaker, Appliances
- Smart trackers, Smart speaker
- Multiparameter patient monitor, Electrocardiogram (ECG), Ultrasound smart probe

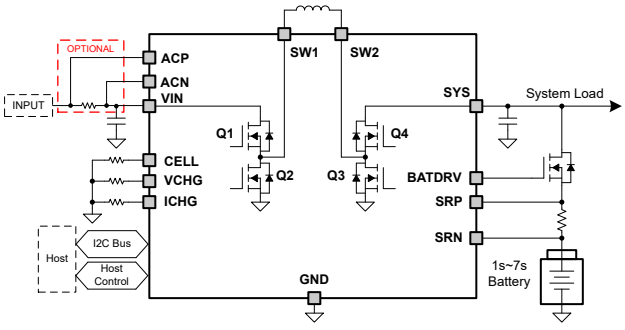
3 Description

The BQ25690 is a fully integrated, switch-mode buck-boost charger for 1 cell to 7cell Li-ion or Li-polymer batteries. The wide input voltage range from 2.5V to 34V supports applications powered from batteries, standard USB-PD adapters, and high voltage dedicated DC adapters. The device integrates 4 switching MOSFETs (Q_1, Q_2, Q_3, Q_4) and all the loop compensation of the buck-boost converter for small solution size with simple design. The device uses NVDC power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. When system power exceeds the input source rating, battery supplement mode supports the system without overloading the input source. The device also supports the full input (sink) and output (reverse or source mode) voltage ranges for USB Type-C and USB power delivery (USB-PD) applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
BQ25690RBAR	RBA (WQFN, 26)	4.0mm × 3.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

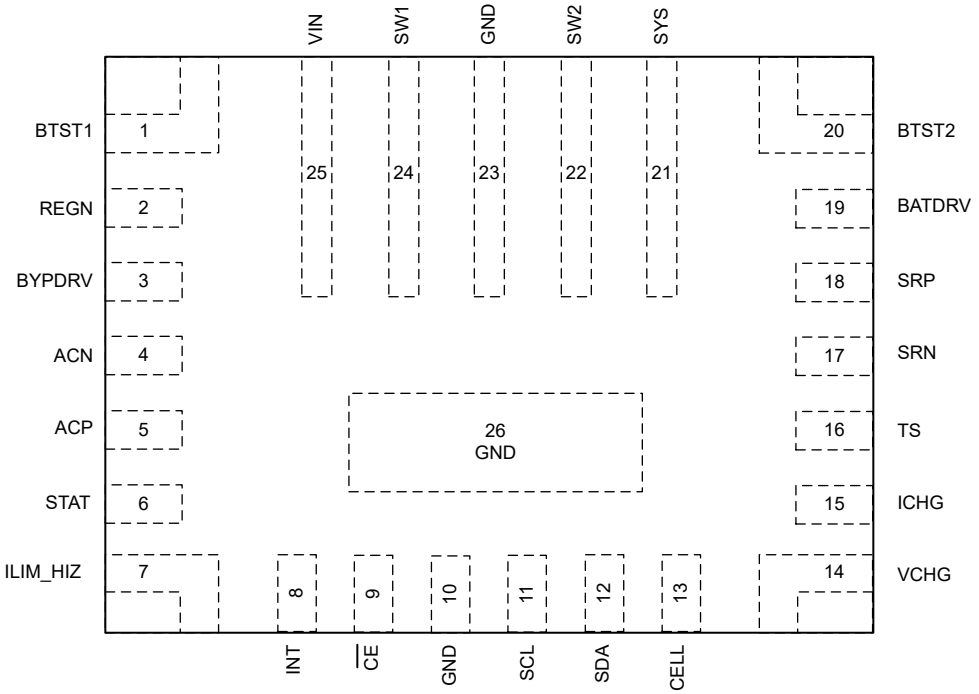


Figure 4-1. BQ25690 RBA Package 26-Pin WQFN Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ACN	4	AI	**Adapter Current-Sense Resistor, Negative Input –** A 0.1µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 33nF ceramic capacitor is placed from the ACN pin to GND for common-mode filtering. If input current sensing is not used, tie directly to VIN.
ACP	5	AI	**Adapter Current-Sense Resistor, Positive Input –** A 0.1µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 33nF ceramic capacitor is placed from the ACP pin to GND for common-mode filtering. If input current sensing is not used, tie directly to VIN.
BATDRV	19	P	**N-Channel Battery FET Gate Drive –** Connect directly to the BATFET gate. Pin is driven 5V above SRP to fully turn on BATFET. BATFET is in linear mode to regulate VSYS at VSYSMIN when battery is depleted below VSYSMIN setting. BATFET is fully on during fast charge, supplement and battery-only modes.
BTST1	1	P	**Buck High-Side Power MOSFET Gate Driver Power Supply –** Connect a 47nF ceramic capacitor and 2.2Ω resistor between BTST1 and SW1 for driving the high-side buck MOSFET (Q1). The bootstrap diode between REGN and BTST1 is integrated.
BTST2	20	P	**Boost High-Side Power MOSFET Gate Driver Power Supply –** Connect a 47nF ceramic capacitor and 2.2Ω resistor between BTST2 and SW2 for driving the high-side boost MOSFET (Q4). The bootstrap diode between REGN and BTST2 is integrated.
BYPDRV	3	P	**Bypass FET Gate Drive –** Connect directly to the back-to-back external bypass FETs gates. Pin drives the gate with 5V relative to SRN to turn on external bypass FETs when the EN_BYPASS = 1 and EN_EXT_BYPASS = 1. Connect a 15V zener diode from BYPDRV to the common source of the external bypass FETs. If external bypass is unused, this pin can be left floating.
$\overline{CE}$	9	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating.
CELL	13	AI	**Cell Count Program –** At power up, the charger detects the resistance tied to CELL pin to determine the default battery cell count and set the corresponding VSYSMIN and charge voltage. The surface mount resistor with ±1% or ±2% tolerance is recommended.

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Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	10	P	**Ground Return**
GND	23	P	**Ground Return**
ICHG	15	AI	**Charge Current Program –** At power up, the charger detects the resistance tied to ICHG pin to determine the default battery charge current. The surface mount resistor with ±1% or ±2% tolerance is recommended.
ILIM_HIZ	7	AI	**Input Current Limit Setting –** ILIM_HIZ pin sets the maximum input current, can be used to monitor the input current and can be puled HIGH to force the device into HIZ mode. A programming resistor to GND is used to set the input current limit as $I_{IN_MAX} = K_{ILIM} / R_{ILIM}$. When the device is under input current regulation, the voltage at ILIM_HIZ pin is 1V. When ILIM pin voltage (V_{ILIM}) is less than 1V, the actual input current can be calculated as: IIN = K_{ILIM} x V_{ILIM} / (R_{ILIM} x 1V). The actual input current limit is the lower of the limits set by ILIM_HIZ pin or the IINDPM register bits. This pin function can be disabled when EN_EXTILIM bit is 0. If ILIM_HIZ pin is not used, pull this pin to GND, do not leave floating.
$\overline{INT}$	8	DO	**Open Drain Interrupt Output –** Connect the $\overline{INT}$ pin to a logic rail using a 10kΩ resistor. The $\overline{INT}$ pin sends an active low, 256µs pulse to host to report the charger device status and faults.
REGN	2	P	**Charger Internal Linear Regulator Output –** Connect a 4.7µF ceramic capacitor from REGN to ground. The REGN LDO output is used for the internal MOSFETs gate driving voltage and the voltage bias for TS pin resistor divider.
SCL	11	DI	**I2C Interface Clock –** Connect SCL to the logic rail through a 10kΩ resistor.
SDA	12	DIO	**I2C Interface Data –** Connect SDA to the logic rail through a 10kΩ resistor.
SRN	17	AI	**Charge Current-Sense Resistor, Negative Input –** A 0.1µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 33nF ceramic capacitor is placed from the SRN pin to GND for common-mode filtering.
SRP	18	AI	**Charge Current-Sense Resistor, Positive Input –** A 0.1µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 33nF ceramic capacitor is placed from the SRP pin to GND for common-mode filtering.
STAT	6	DO	**Open Drain Status Output –** Connect to the pull up rail using a 10kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. The STAT pin function can be disabled when DIS_STAT_PIN bit is set to 1.
SW1	24	P	**Buck Side Half Bridge Switching Node –** Inductor connection to mid point of Q1 and Q2 switches.
SW2	22	P	**Boost Side Half Bridge Switching Node –** Inductor connection to mid point of Q3 and Q4 switches.
SYS	21	P	**Charger Output Voltage to System –** The internal N-channel high side MOSFET (Q4) has drain connected to SYS and source connected to SW2. This is the output of the switching converter, and must be decoupled with ceramic capacitors as close to the pin as possible. Use a combination of 0.1µF with higher value capacitance to achieve low impedance connection from SYS to GND.
Thermal Pad	26	–	**Exposed pad beneath the IC –** Always solder the thermal pad to the board and connect to GND and the power ground plane with multiple vias. The exposed pad serves to dissipate heat.
TS	16	AI	**Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. Recommend 103AT-2 10kΩ thermistor.
VCHG	14	AI	**Charge Voltage Program –** At power up, the charger detects the resistance tied to VCHG pin to determine the default battery charge voltage. The surface mount resistor with ±1% or ±2% tolerance is recommended.
VIN	25	P	**Charger Input Voltage –** The internal N-channel high side MOSFET (Q1) has drain connected to VIN and source connected to SW1. This is the input of the switching converter, and must be decoupled with ceramic capacitors as close to the pin as possible. Use a combination of 0.1µF with higher value capacitance to achieve low impedance connection from VIN to GND.

(1) AI = Analog input, AIO = Analog input/output, DI = Digital input, DO = Digital output, DIO = Digital input/output, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN, ACP, ACN, BATDRV, SYS, SRP, SRN	-0.3	45	V
	SW1, SW2	-0.3	45	V
	SW1, SW2 (50ns transient)	-2	45	V
	BYPDRV	-0.3	45	V
	BTST1 with respect to SW1	-0.3	6	V
	BTST2 with respect to SW2	-0.3	6	V
	REGN	-0.3	6	V
	BATDRV with respect to SRP	-0.3	10	V
	ACP with respect to ACN, SRP with respect to SRN	-0.3	0.3	V
	CELL, /CE, ICHG, ILIM_HIZ, /INT, SCL, SDA, STAT, TS, VCHG	-0.3	6	V
Output Sink Current	/CE, STAT		5	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		34	V
V_{BAT}	Battery voltage	0		33	V
V_{I2C}	SCL and SDA pullup voltage VDD	1.8		5V	V
F_{SW}	Switching Frequency	450		1,200	kHz
C_{VIN}	VIN total capacitance (minimum value after derating) (C_{VIN} = C_{VIN_ACN} + C_{VIN_ACP}) ($C_{VIN_ACP} \geq C_{VIN_ACN}$)	10			µF
C_{VIN_ACN}	C_{VIN_ACN} capacitance (minimum value after derating)	100			nF
C_{SYS}	SYS capacitance (minimum value after derating)	15			µF
C_{SYS_1s-2s}	SYS capacitance (1s,2s) (minimum value after derating)	15			µF
C_{SYS_3s-7s}	SYS capacitance (3s-7s) (minimum value after derating)	8			µF
C_{BAT}	BAT capacitance (minimum value after derating)	5			µF
L	Recommended Inductor for f_{SW}: 450kHz - 500kHz	6.8		15	µH
	Recommended Inductor for f_{SW}: 550kHz - 700kHz	4.7		10	µH
	Recommended Inductor for f_{SW} >700kHz	2.2		4.7	µH
R_{AC_SNS}	Input current sense resistor	0	5	10	mΩ

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over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
R_{BAT_SNS}	Battery current sense resistor		5	10	mΩ
R_{CELL}	CELL pulldown resistor	4.6		27.4	kΩ
R_{VCHG}	VCHG pulldown resistor	4.6		27.4	kΩ
R_{ICHG}	ICHG pulldown resistor	4.6		27.4	kΩ
R_{ILIM_HIZ}	ILIM_HIZ pulldown resistor	0.0		33	kΩ
T_A	Ambient temperature	-40		105	°C
T_J	Junction temperature	-40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		BQ25690 RBA (QFN) 26-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (EVM(2))	22.9	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC(1))	37.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Measured on 70µm thick copper, 4-layer board.

5.5 Electrical Characteristics

$V_{VIN_UVLOZ} < V_{VIN} < V_{VIN_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current (I_{SRN} + I_{SRP} + I_{SYS})	V_{SRP} = V_{SRN} = V_{SYS} = 20V, VIN = 0V, BATFET_CTRL = 1, T_J < 105°C		6.5	16	µA
		V_{SRP} = V_{SRN} = V_{SYS} = 20V, VIN = 0V, BATFET_CTRL = 0, T_J < 105°C		6.5	20	µA
I_{HIZ_VIN}	HIZ mode input current (IACP + IACN + IVIN)	EN_HIZ = 1, VIN = 24V		11		µA
I_{Q_VIN}	Quiescent input current (IACP + IACN + IVIN)	Not switching		250	300	µA
		Switching, ISYS = ICHG = 0A		700		µA
I_{Q_REV}	Quiescent battery current in reverse mode (I_{SRN} + I_{SRP} + I_{SYS})	Not switching		320	370	µA
		Switching		700		µA
VIN / VBAT SUPPLY						
V_{VIN_OP}	VIN operating range	VBAT >3.2V	2.5		34	V
		VBAT <3.2V	3.2		34	V
V_{VIN_OK}	VIN converter enable threshold	VIN rising, no battery	2.9			V
V_{VIN_OKZ}	VIN converter disable threshold	VIN falling, no battery			2.35	V
$V_{VIN\ _OVP}$	VIN over-voltage rising threshold	VIN rising	35.5	36.3	37	V
	VIN internal over-voltage falling threshold	VIN falling	33.8	34.5	35.2	V

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V_{VIN_UVLOZ} < V_{VIN} < V_{VIN_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_OK}	Battery voltage to allow OTG operation	V_{SRN} rising, no input		2.8		V
	Battery voltage to enable BATFET	V_{SRN} rising, no input	2.4			V
V_{BAT_OKZ}	Battery voltage to disable OTG operation	V_{SRN} falling, no input			2.4	V
	Battery voltage to disable BATFET	V_{SRN} falling, no input			1.9	V
POWER-PATH MANAGEMENT						
V_{SYSMIN_RANGE}	Minimum System Voltage regulation range		3.0		28	V
V_{SYSMIN_STEP}	Typical VSYS_MIN regulation step size			20		mV
V_{SYSMIN_REG}	Default System Regulation Voltage when VBAT < VSYS_MIN	1s battery, ISYS = 0A, Charge Disabled	3.5	3.7		V
		2s-7s battery, ISYS = 0A, Charge Disabled. Offset voltage above VSYS_MIN (3.1V/cell)		200		mV
	System Regulation Voltage when VBAT < VSYS_MIN. VBAT = 2.5V/cell	2s battery, ISYS = 0A, Charge Disabled	6.2	6.4		V
		3s battery, ISYS = 0A, Charge Disabled	9.3	9.5		V
		4s battery, ISYS = 0A, Charge Disabled	12.4	12.6		V
		5s battery, ISYS = 0A, Charge Disabled	15.5	15.7		V
		6s battery, ISYS = 0A, Charge Disabled	18.5	18.8		V
		7s battery, ISYS = 0A, Charge Disabled	21.6	21.9		V
V_{SYSMAX_REG}	Default System Regulation Voltage when VBAT > VSYS_MIN	1s-7s battery, ISYS = 0A, Charge Disabled, PFM disabled. Offset voltage above VBAT		200		mV
	System Regulation Voltage when VBAT > VSYS_MIN. VBAT = 3.8V/cell.	1s, ISYS = 0A, Charge Disabled, PFM Disabled		4.000	4.1	V
		3s, ISYS = 0A, Charge Disabled, PFM Disabled		11.600	11.7	V
		7s, ISYS = 0A, Charge Disabled, PFM Disabled		26.800	27.0	V
V_{SYS_OVP}	VSYS overvoltage protection	VSYS rising to stop switching, as percentage of system regulation voltage	104	106	110	%
		VSYS falling to start switching, as percentage of system regulation voltage	98	100	104	%
V_{SYS_SHORT}	VSYS short voltage rising threshold		2.085	2.2	2.3	V
	VSYS short voltage falling threshold		1.9	2.0	2.1	V
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		2.4		33.0	V
V_{REG_STEP}	Typical charge voltage step			10		mV

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V_{VIN_UVLOZ} < V_{VIN} < V_{VIN_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG_ACC}	Charge voltage regulation accuracy	1s to 7s battery, T_J = 0°C to 85°C	-0.55		0.5	%
		1s to 7s battery, T_J = -40°C to 125°C	-1.15		0.9	%
	Charge voltage regulation accuracy, 4.2V/cell	1s, TJ = 0°C to 85°C	4.1769	4.2	4.221	V
		2s, TJ = 0°C to 85°C	8.358	8.4	8.442	V
		3s, TJ = 0°C to 85°C	12.537	12.6	12.663	V
		4s, TJ = 0°C to 85°C	16.716	16.8	16.884	V
		5s,TJ = 0°C to 85°C	20.895	21.0	21.105	V
		6s, TJ = 0°C to 85°C	25.074	25.2	25.326	V
		7s, TJ = 0°C to 85°C	29.253	29.4	29.547	V
I_{CHG_RANGE}	Typical charge current regulation range		40		3300	mA
I_{CHG_STEP}	Typical charge current step			20		mA
I_{CHG_ACC}	Charge current regulation accuracy (VBAT > VSYS_MIN), VBAT = 4V/cell, R_{BAT_SNS} = 10mΩ	VBAT = 12V, 20V, 28V. ICHG = 1.5A	1425	1500	1575	mA
		VBAT = 12V, 20V, 28V. ICHG = 0.5A	450	500	550	mA
I_{CHG_ACC}	Charge current regulation accuracy (VBAT < VSYS_MIN), VBAT = 3V/cell, R_{BAT_SNS} = 10mΩ	VBAT = 9V, 15V, 21V. ICHG = 1.5A	1425	1500	1575	mA
		VBAT = 9V, 15V, 21V. ICHG = 0.5A	450	500	550	mA
I_{TERM_RANGE}	Typical termination current range		20		620	mA
I_{TERM_STEP}	Typical termination current step			20		mA
I_{TERM_ACC}	Termination current accuracy, VBAT = 4.2V/cell, R_{BAT_SNS} = 10mΩ	VBAT = 12.6V, 21V, 29.4V. ITERM = 160mA	140	160	176	mA
		VBAT = 12.6V, 21V, 29.4V. ITERM = 80mA	60	80	120	mA
I_{PRECHG}	Typical pre-charge current range	VBAT < VBAT_LOWV	20		620	mA
I_{PRECHG_STEP}	Typical pre-charge current step			20		mA
I_{PRECHG_ACC}	Precharge current accuracy, VBAT = 2.5V/cell, R_{BAT_SNS} = 10mΩ	VBAT = 7.5V, 12.5V, 17.5V. IPRECHG = 300mA	250	300	330	mA
		VBAT = 7.5V, 12.5V, 17.5V. IPRECHG = 160mA	110	160	190	mA
I_{BAT_SHORT}	Trickle charge current accuracy for Li-Ion batteries	VBAT < V_{BAT_SHORT}		100		mA
V_{BAT_SHORT}	Trickle charge to pre-charge transition (1s-2s)	VBAT rising, threshold per cell		2.15		V
	Pre-charge to trickle charge transition (1s-2s)	VBAT falling, threshold per cell		1.85		V
	Trickle charge to pre-charge transition (3s-7s)	VBAT rising, threshold per cell		2.2		V
	Pre-charge to trickle charge transition (3s-7s)	VBAT falling, threshold per cell		2.0		V
V_{BAT_LOWV}	Pre-charge to fast-charge transition	VBAT rising, as percentage of VREG, VBAT_LOWV[2:0] = 3	69.0	71.4	73.8	%
		VBAT rising, as percentage of VREG, VBAT_LOWV[2:0] = 2	64.3	66.7	69.0	%
		VBAT rising, as percentage of VREG, VBAT_LOWV[2:0] = 1	52	55	58	%
		VBAT rising, as percentage of VREG, VBAT_LOWV[2:0] = 0	27	30	33	%
$V_{BAT_LOWV_HYS}$	BAT_LOWV hysteresis			5		%

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V_{VIN_UVLOZ} < V_{VIN} < V_{VIN_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RECHG}	Battery recharge threshold	VBAT falling, as percentage of VREG, VRECHG[1:0] = 3		97		%
		VBAT falling, as percentage of VREG, VRECHG[1:0] = 2		95.5		%
		VBAT falling, as percentage of VREG, VRECHG[1:0] = 1		94.1		%
		VBAT falling, as percentage of VREG, VRECHG[1:0] = 0		92.7		%
I_{SYS_LOAD}	System (SYS) discharge load current	FORCE_ISYS_DSCHG = 1	20			mA
I_{VIN_LOAD}	Input (VIN) discharge load current	FORCE_VIN_DSCHG = 1	20			mA
BATFET CONTROL						
V_{BATDRV_REG}	BATFET drive voltage	V_{BATDRV} - V_{SRP}, VIN < VBAT		5		V
I_{BATDRV_REG}	BATFET charge pump current limit	V_{BATDRV} - V_{SRP} = 5V, VIN = 0V		50		µA
BATTERY PROTECTIONS						
V_{BAT_OVP}	Battery over-voltage threshold	VBAT rising, as percentage of VREG	102	104	105.5	%
		VBAT falling, as percentage of VREG	100	102	103.5	%
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Input voltage DPM regulation range		2.5		34	V
V_{INDPM_STEP}	Typical input voltage DPM regulation step			20		mV
V_{INDPM_ACC}	Input voltage DPM regulation accuracy	VINDPM = 20V	19.6	20	20.4	V
		VINDPM = 12V	11.76	12	12.24	V
		VINDPM = 4.3V	4.17	4.3	4.43	V
		VINDPM = 3V	2.85	3	3.15	V
I_{INDPM_RANGE}	Input current DPM regulation range		40		3300	mA
I_{INDPM_STEP}	Typical input current DPM regulation step			20		mA
I_{INDPM_ACC}	Input current DPM regulation accuracy	IINDPM = 3000mA	2700	2850	3000	mA
		IINDPM = 1500mA	1350	1425	1500	mA
		IINDPM = 900mA	810	855	900	mA
		IINDPM = 500mA	450	475	500	mA
K_{ILIM}	Input current limit scale factor (IIN_MAX = KILIM / RILIM)	IIN_MAX = 1.6A, 1A, 0.5A	2890	3333	3780	A x Ω
$V_{IH_ILIM_HIZ}$	ILIM_HIZ input high threshold to enter HIZ mode	V_{ILIM_HIZ} rising	1.77			V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation	TREG = 120°C		120		°C
		TREG = 80°C		80		°C
T_{SHUT}	Thermal shutdown rising threshold	Temperature rising		165		°C
T_{SHUTZ}	Thermal shutdown falling threshold	Temperature falling		130		°C
SWITCHING CONVERTER						

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V_{VIN_UVLOZ} < V_{VIN} < V_{VIN_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW}	Switching frequency	FSW = b001	382.5	450	517.5	kHZ
		FSW = b010	425	500	575	kHZ
		FSW = b011	467.5	550	632.5	kHZ
		FSW = b100	510	600	690	kHZ
		FSW = b101	595	700	805	kHZ
		FSW = b110	1020	1200	1380	kHZ
R_{Q1_ON}	VIN to SW1 MOSFET on resistance			37	67	mΩ
R_{Q2_ON}	SW1 to GND MOSFET on resistance			77	140	mΩ
R_{Q3_ON}	SW2 to GND MOSFET on resistance			77	140	mΩ
R_{Q4_ON}	SYS to SW2 MOSFET on resistance			37	67	mΩ
BYPASS MODE						
V_{BYPDRV_REG}	External BYPASS FET drive voltage	VIN = 4V, V_{BYP_DRV} - V_{SRN}, VIN > VBAT, EN_BYPASS = 1, EN_EXT_BYPASS = 1		4.18		V
I_{BYPDRV_REG}	External BYPASS FET charge pump current limit	V_{BYPDRV} - V_{SYS} = 5V	16	23		µA
I_{BYPDRV_OFF}	External BYPASS FET turn off current			460		µA
I_{EXTBYP_OCP}	External bypass overcurrent limit to exit bypass mode	EN_BYPASS = 1, EN_EXT_BYPASS = 1. R_{AC_SNS} = 10mΩ	5.35	5.5		A
I_{BYP_OCP}	Internal bypass overcurrent limit to exit bypass mode.	EN_BYPASS = 1, EN_EXT_BYPASS = 0, percentage above IINDPM setting. R_{AC_SNS} = 10mΩ		15		%
I_{BYP_LL}	Bypass light-load current limit to exit bypass mode	EN_BYPASS = 1, current falling. R_{AC_SNS} = 10mΩ		130		mA
$I_{REV_EXTBYP_OCP}$	External reverse bypass overcurrent limit to exit bypass mode	EN_REV = 1, EN_BYPASS = 1, EN_EXT_BYPASS = 1. R_{AC_SNS} = 10mΩ	5.35	5.5		A
$I_{REV_BYP_OCP}$	Internal reverse bypass overcurrent limit to exit bypass mode	EN_REV = 1, EN_BYPASS = 1, EN_EXT_BYPASS = 0, percentage above IIN_REV setting. R_{AC_SNS} = 10mΩ		15		%
$I_{REV_BYP_LL}$	Reverse bypass light-load current limit to exit bypass mode	EN_BYPASS = 1, EN_EXT_BYPASS = 0, reverse current falling. R_{AC_SNS} = 10mΩ		122		mA
REVERSE MODE VOLTAGE AND CURRENT REGULATION						
V_{INREV_RANGE}	Reverse mode voltage regulation range at VIN		3.5		34	V
V_{INREV_STEP}	Reverse mode voltage regulation step at VIN			20		mV
V_{INREV_ACC}	Reverse mode voltage regulation at VIN:	VIN_REV = 20V	19.8	20	20.2	V
		VIN_REV = 15V	14.8	15	15.2	V
		VIN_REV = 9V	8.8	9	9.2	V
		VIN_REV = 5V	4.8	5	5.2	V
V_{INREV_BACKUP}	VIN falling threshold to trigger reverse backup mode. Defined as percentage of VINDPM	VIN_BACKUP = 100%, VINDPM = 15V	93.5	100	106.5	%
		VIN_BACKUP = 80%, VINDPM = 15V	75	80	85	%
		VIN_BACKUP = 60%, VINDPM = 15V	56	60	64	%
		VIN_BACKUP = 50%, VINDPM = 15V	46	50	54	%
I_{INREV_RANGE}	Reverse mode current regulation range across ACP/ACN		40		3300	mA

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V_{VIN_UVLOZ} < V_{VIN} < V_{VIN_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{INREV_STEP}	Reverse mode current regulation step across ACP/ACN			20		mA
I_{INREV_ACC}	Reverse mode current regulation accuracy across ACP/ACN	IIN_REV = 3000mA	2680	2850	3000	mA
		IIN_REV = 1500mA	1300	1425	1500	mA
		IIN_REV = 900mA	750	855	930	mA
		IIN_REV = 500mA	380	475	560	mA
I_{BATREV_ACC}	Reverse mode battery discharging current regulation accuracy across SRP/SRN	IBAT_REV = 3.56A	3410	3560	3710	mA
		IBAT_REV = 2.28A	2130	2280	2430	mA
		IBAT_REV = 1A	850	1000	1150	mA
V_{INREV_OV}	Reverse mode VIN rising threshold	VIN rising as percentage of VIN_REV	110			%
V_{INREV_UV}	Reverse mode VIN falling threshold to stop converter	VIN falling			2.95	V
BATTERY PACK NTC MONITOR (CHARGE MODE)						
V_{T1_RISE}	TS pin voltage rising T1 threshold, charge suspended above this voltage.	As Percentage to REGN, TS_TH1=0°C w/ 103AT	72.0	73.3	74.2	%
V_{T1_FALL}	TS pin voltage falling T1 threshold, charge re-enabled below this voltage.	As Percentage to REGN, TS_TH1=0°C w/ 103AT	71.0	72	73.5	%
V_{T2_RISE}	TS pin voltage rising T2 threshold, charge back to reduced ICHG above this voltage	As Percentage to REGN, TS_TH2=10°C w/ 103AT	67.0	68.25	69.25	%
V_{T2_FALL}	TS pin voltage falling T2 threshold. Charge back to normal below this voltage	As Percentage to REGN, TS_TH2=10°C w/ 103AT	66.0	66.95	68.5	%
V_{T3_FALL}	TS pin voltage falling T3 threshold, reduced VREG below this voltage.	As Percentage to REGN, TS_TH3=45°C w/ 103AT	43.75	44.75	45.75	%
V_{T3_RISE}	TS pin voltage rising T3 threshold. Charge back to normal above this voltage.	As Percentage to REGN, TS_TH3=45°C w/ 103AT	45.0	46.05	46.55	%
V_{T5_FALL}	TS pin voltage falling T5 threshold, charge suspended below this voltage	As Percentage to REGN, TS_TH5=60°C w/ 103AT	33.5	34.375	34.875	%
V_{T5_RISE}	TS pin voltage rising T5 threshold. Charge with reduced VREG above this voltage.	As Percentage to REGN, TS_TH5=60°C w/ 103AT	34.5	35.5	36	%
BATTERY PACK NTC MONITOR (REVERSE MODE)						
$V_{TS_REV_COLD_RISE}$	TS pin voltage rising TS COLD threshold. Reverse mode suspended above this voltage	As Percentage to REGN (TS_REV_COLD = –20°C w/ 103AT)	78.0	80	81.0	%
		As Percentage to REGN (TS_REV_COLD= –10°C w/ 103AT)	75.0	77.15	78.0	%
$V_{TS_REV_COLD_FALL}$	TS pin voltage falling TS COLD threshold. Reverse mode resumes below this voltage	As Percentage to REGN (TS_REV_COLD= –20°C w/ 103AT)	77.5	78.7	80.0	%
		As Percentage to REGN (TS_REV_COLD= –10°C w/ 103AT)	74.5	75.6	77.0	%
$V_{TS_REV_HOT_FALL}$	TS pin voltage falling TS HOT threshold. Reverse mode suspended below this voltage	As Percentage to REGN, (TS_REV_HOT= 55°C w/ 103AT)	36.5	37.7	38.2	%
		As Percentage to REGN, (TS_REV_HOT= 60°C w/ 103AT)	33.5	34.375	34.875	%
		As Percentage to REGN, (TS_REV_HOT= 65°C w/ 103AT)	30.5	31.25	31.75	%

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V_{VIN_UVLOZ} < V_{VIN} < V_{VIN_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TS_REV_HOT_RISE}$	TS pin voltage rising TS HOT threshold. Reverse mode resumes above this voltage	As Percentage to REGN, (TS_REV_HOT= 55°C w/ 103AT)	38.5	39	39.95	%
		As Percentage to REGN, (TS_REV_HOT= 60°C w/ 103AT)	34.5	35.5	36	%
		As Percentage to REGN, (TS_REV_HOT= 65°C w/ 103AT)	31.5	32.5	33	%
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{IN} = 5V, I_{REGN} = 20mA	4.6	4.8		V
		V_{IN} = 15V, I_{REGN} = 20mA	4.8	5	5.2	V
I_{REGN}	REGN LDO current limit	V_{IN} = 5V, V_{REGN} = 4.5V	26			mA
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
V_{OL}	SDA Output low threshold level				0.4	V
I_{IN_BIAS}	High level leakage current				1	µA
LOGIC INPUT PIN ($\overline{CE}$)						
V_{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
I_{IN_BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC OUTPUT PIN ($\overline{INT}$, STAT)						
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{OUT_BIAS}	High-level leakage current	Pull up rail 1.8V			2	µA

5.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
BATTERY CHARGER						
t_{TOP_OFF}	Top-off timer accuracy	TOPOFF_TMR[1:0] = b01	12	15	18	min
		TOPOFF_TMR[1:0] = b10	24	30	36	min
		TOPOFF_TMR[1:0] = b11	36	45	54	min
t_{SAFETY_PRECHG}	Charge safety timer in pre-charge	PRECHG_TMR = b0	1.8	2	2.2	hr
t_{SAFETY}	Charge safety timer accuracy	CHG_TMR[1:0] = b00	4.5	5	5.5	hr
		CHG_TMR[1:0] = b01	7.2	8	8.8	hr
		CHG_TMR[1:0] = b10	10.8	12	13.2	hr
		CHG_TMR[1:0] = b11	21.6	24	26.4	hr
tCV_TMR	CV timer accuracy	CV_TMR = b1010	8.5	10	11.5	hr
t_{TS_DGL}	Deglitch time for TS threshold crossing			30		ms
I2C INTERFACE						
f_{SCL}	SCL clock frequency				1000	kHZ
t_r	Rise time of SDA signal	f_{SCL} = 1MHz			120	ns
t_r	Rise time of SDA signal	f_{SCL} = 400kHz			300	ns
t_r	Rise time of SDA signal	f_{SCL} = 100kHz			1000	ns
C_b	Capacitive load for each bus line				550	pF
WATCHDOG TIMER						
t_{LP_WDT}	Watchdog reset time	EN_HIZ = 1, WATCHDOG = 160s	100	160		s

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PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{WDT}	Watchdog reset time	EN_HIZ = 0, WATCHDOG = 160s	136	160		s

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5.7 Typical Characteristics

C_{VIN} = 10*4.7µF, C_{SYS}= 6*4.7µF, C_{BAT} = 4*4.7µF, L1 = 10µH (SRP5050FA-100M)

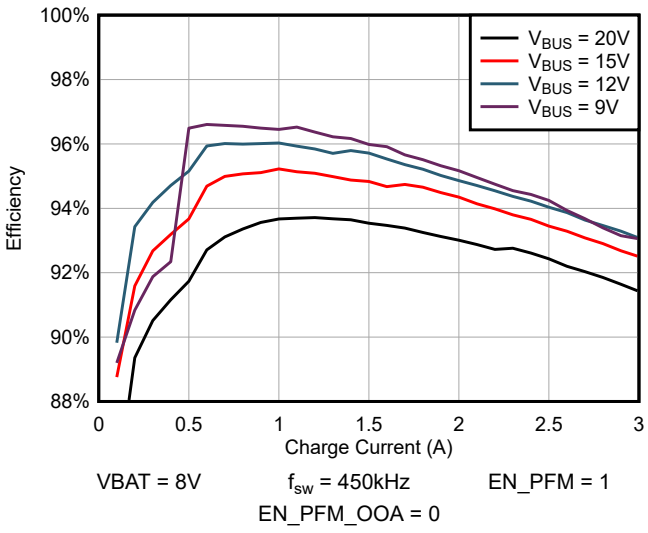


Figure 5-1. 2S Battery Charge Efficiency vs. Charge Current

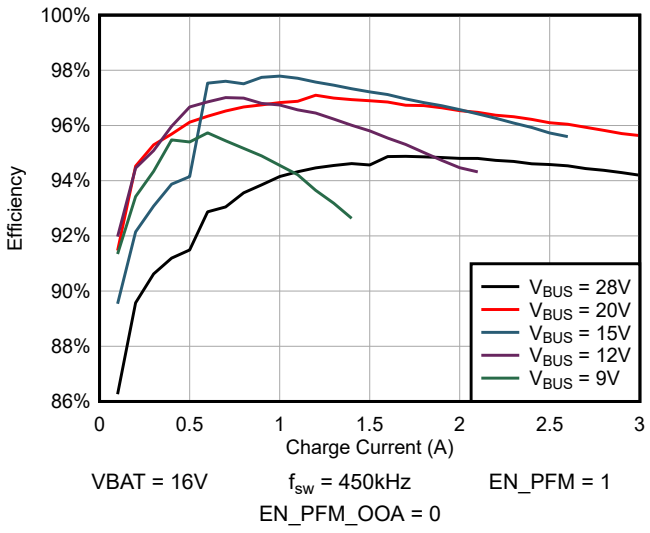


Figure 5-2. 4S Battery Charge Efficiency vs. Charge Current

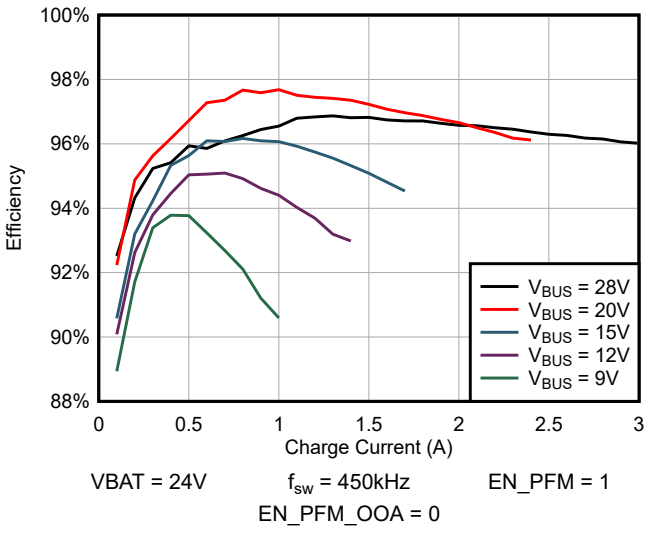


Figure 5-3. 6S Battery Charge Efficiency vs. Charge Current

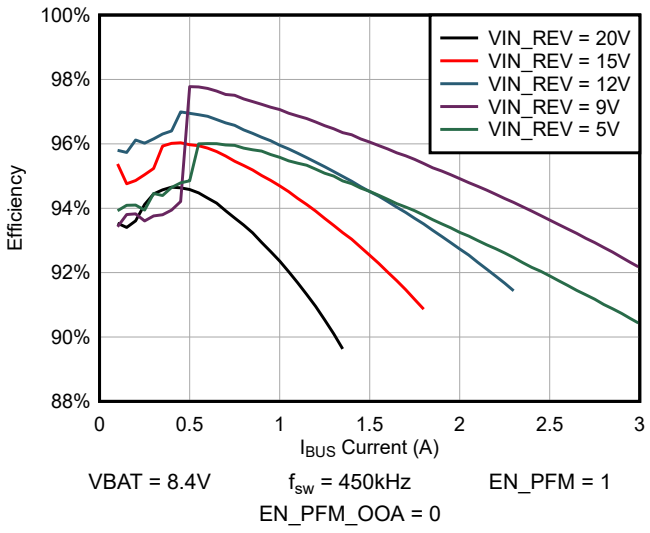


Figure 5-4. 2S Battery OTG Efficiency vs. OTG Current

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5.7 Typical Characteristics (continued)

C_{VIN} = 10*4.7µF, C_{SYS}= 6*4.7µF, C_{BAT} = 4*4.7µF, L1 = 10µH (SRP5050FA-100M)

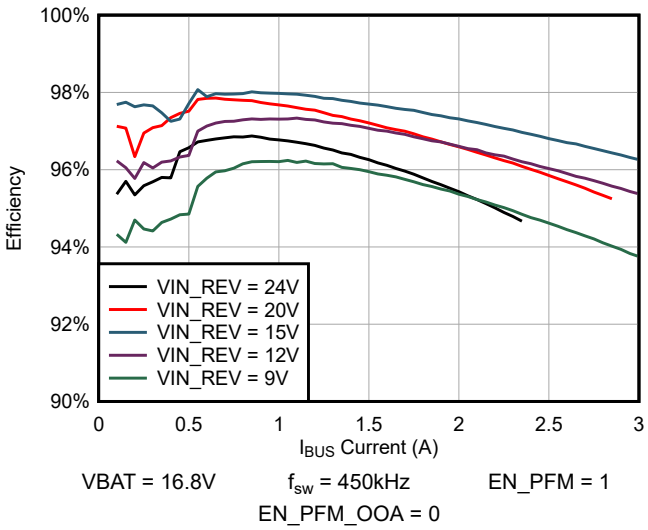


Figure 5-5. 4S Battery OTG Efficiency vs. OTG Current

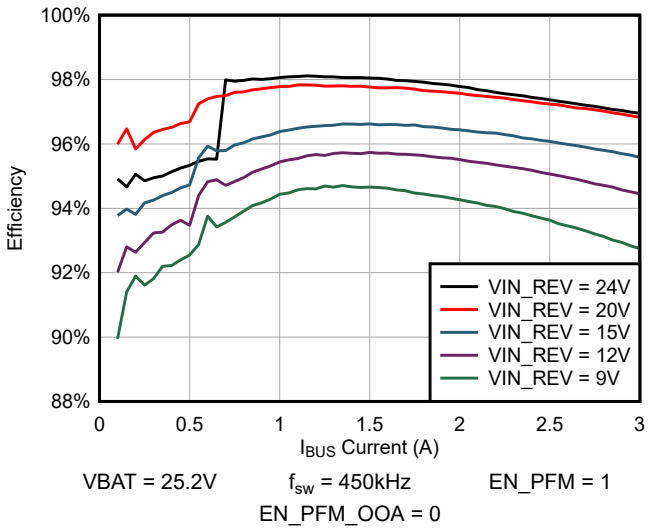


Figure 5-6. 6S Battery OTG Efficiency vs. OTG Current

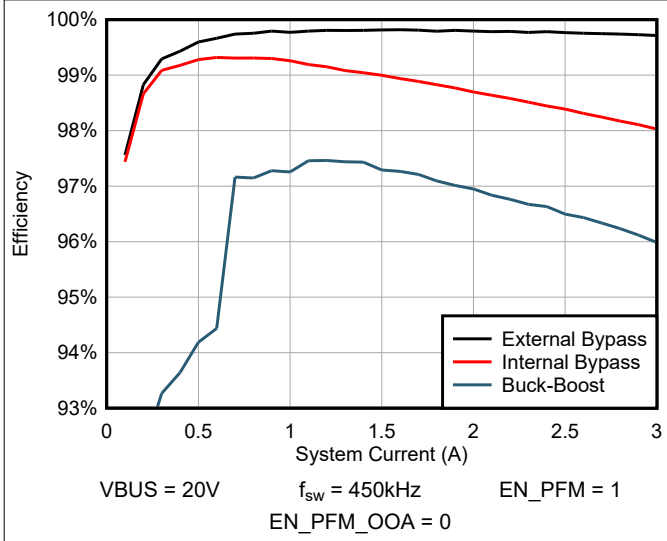


Figure 5-7. Bypass Mode Efficiency vs. System Current

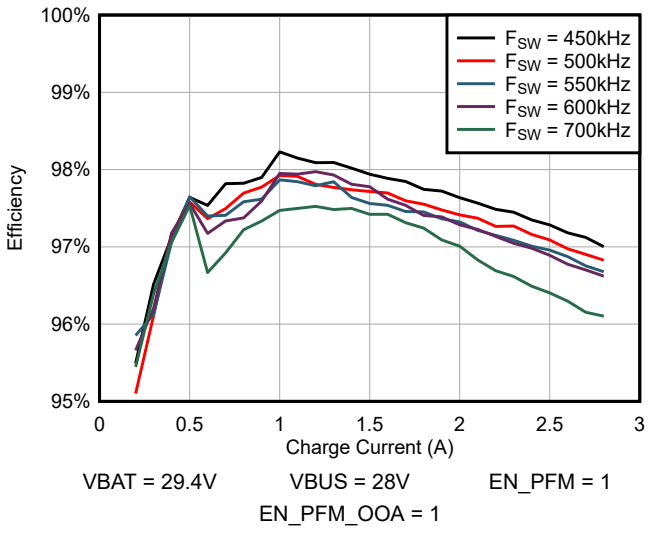


Figure 5-8. 7S Battery Charge Efficiency vs. Charge Current Across Switching Frequency

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5.7 Typical Characteristics (continued)

C_{VIN} = 10*4.7µF, C_{SYS}= 6*4.7µF, C_{BAT} = 4*4.7µF, L1 = 10µH (SRP5050FA-100M)

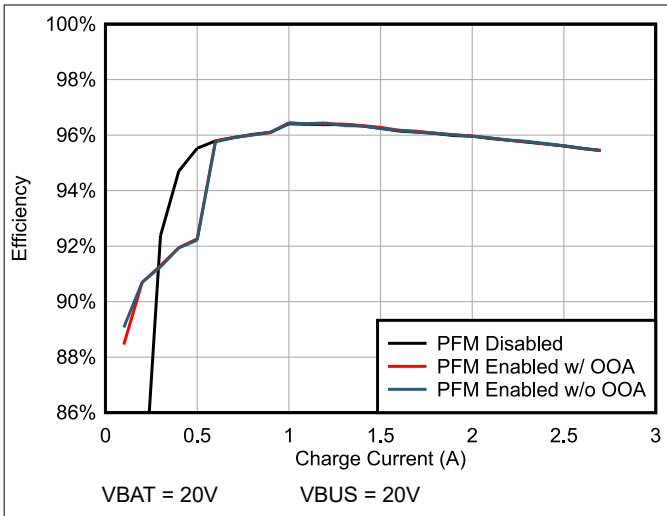


Figure 5-9. 5S Battery Charge Efficiency vs. Charge Current Across PWM/PFM/OOA Modes

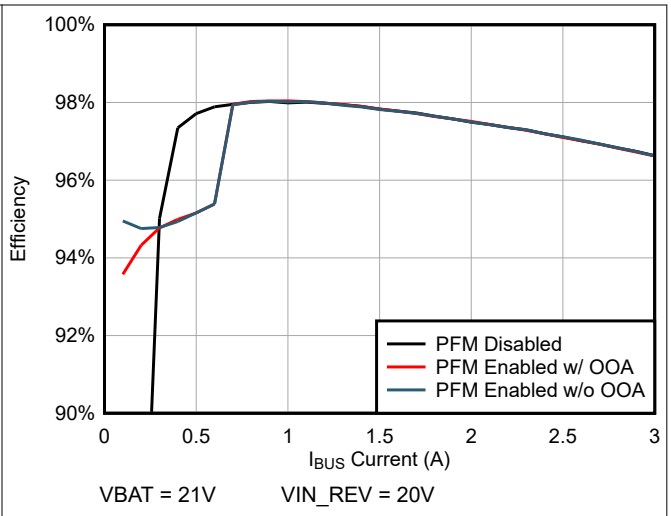


Figure 5-10. 5S Battery OTG Efficiency vs. Charge Current Across PWM/PFM/OOA Modes

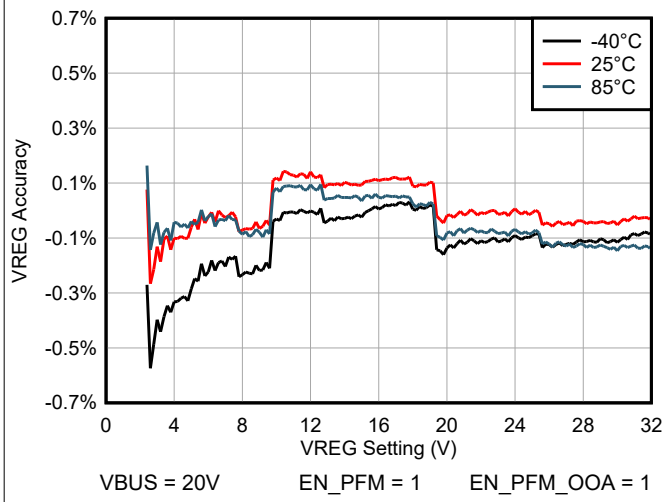


Figure 5-11. Charge Voltage Accuracy

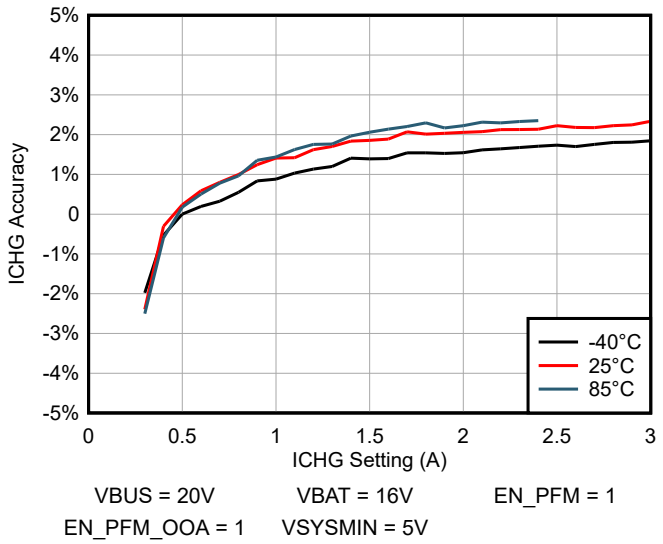


Figure 5-12. Charge Current Accuracy (VBAT > VSYSMIN)

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5.7 Typical Characteristics (continued)

C_{VIN} = 10*4.7µF, C_{SYS}= 6*4.7µF, C_{BAT} = 4*4.7µF, L1 = 10µH (SRP5050FA-100M)

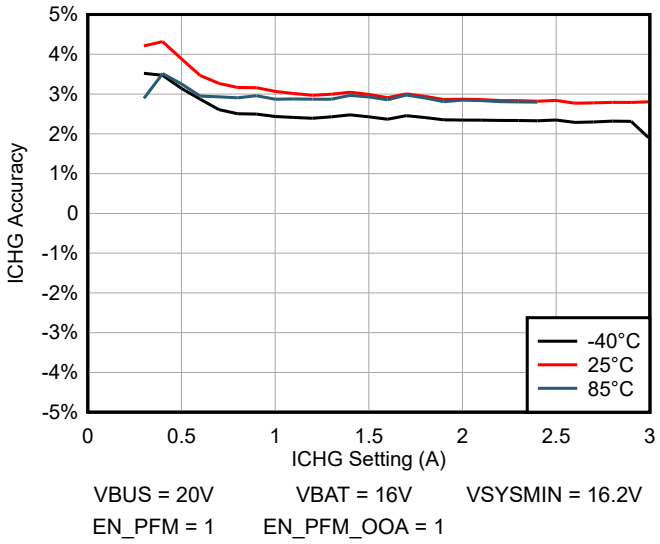


Figure 5-13. Charge Current Accuracy (VBAT < VSYSMIN)

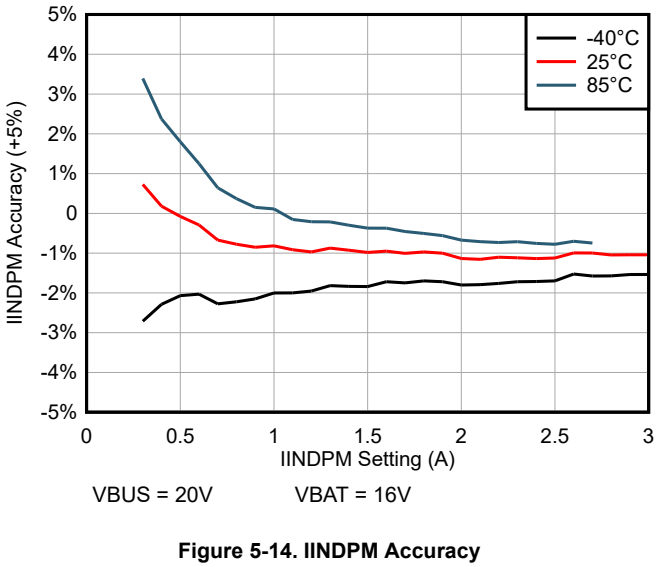


Figure 5-14. IINDPM Accuracy

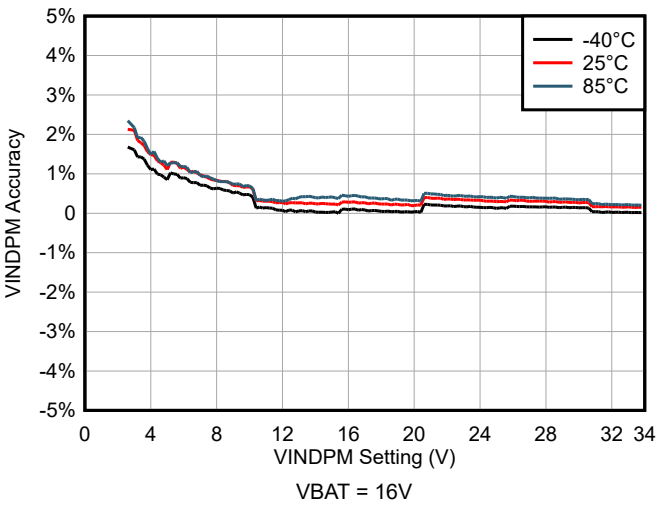


Figure 5-15. VINDPM Accuracy

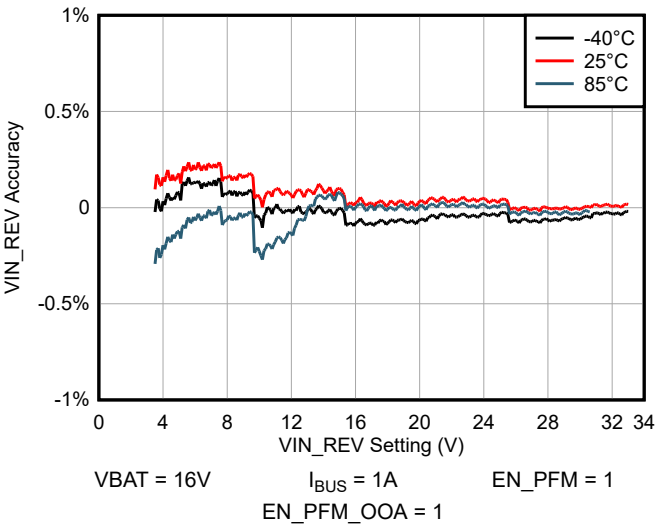


Figure 5-16. VIN_REV Accuracy

5.7 Typical Characteristics (continued)

C_{VIN} = 10*4.7µF, C_{SYS}= 6*4.7µF, C_{BAT} = 4*4.7µF, L1 = 10µH (SRP5050FA-100M)

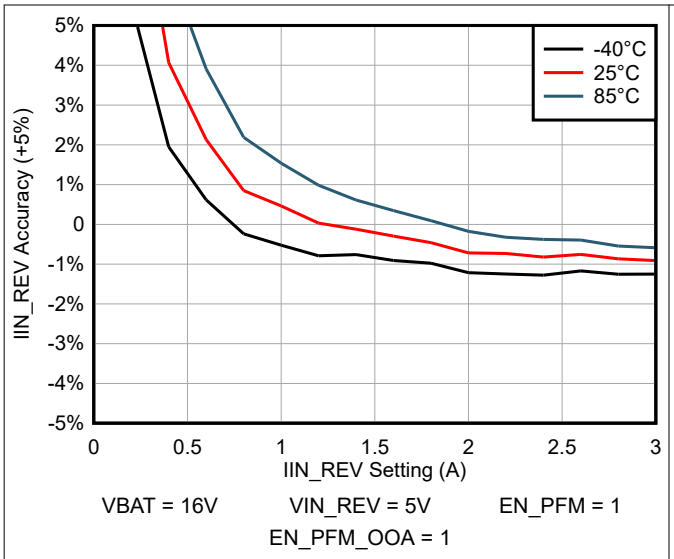


Figure 5-17. IIN_REV Accuracy

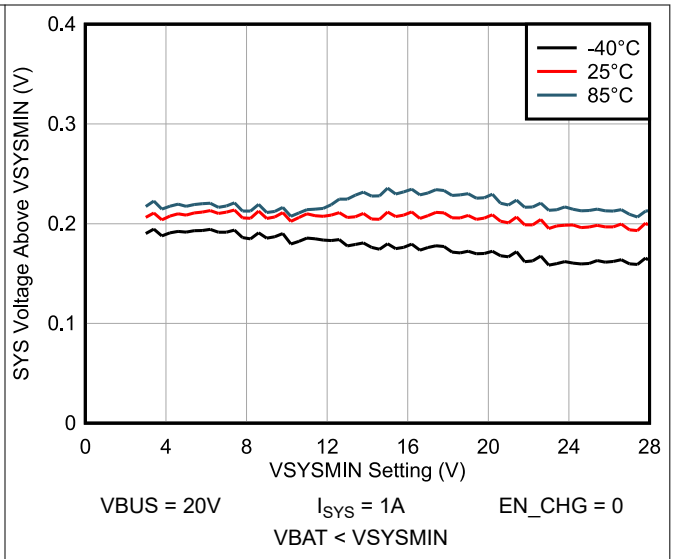


Figure 5-18. VSYSMIN Regulation

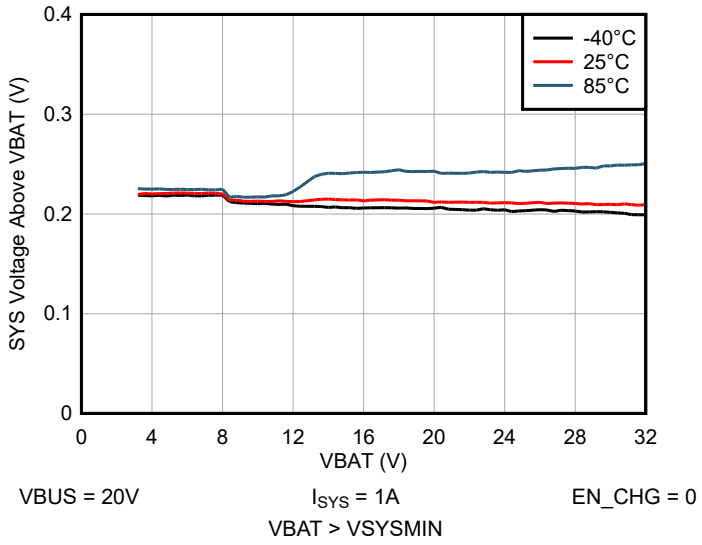


Figure 5-19. VSYSMAX Regulation

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6 Detailed Description

6.1 Overview

The BQ25690 is a fully integrated, switch-mode buck-boost charger for 1 cell to 7cell Li-ion or Li-polymer batteries. The wide input voltage range from 2.5V to 34V supports applications powered from batteries, standard USB-PD adapters, and high voltage dedicated DC adapters. The device integrates 4 switching MOSFETs (Q_1, Q_2, Q_3, Q_4) and all the loop compensation of the buck-boost converter for small solution size with simple design. BQ25690 is compliant with USB power delivery (USB-PD) power specifications with input current and voltage regulation. In addition, the input current optimizer (ICO) supports the detection of maximum power of the input source without overload. The device can also operate in reverse mode, providing power from the battery to the input port with USB-PD power profile compatibility.

BQ25690 uses narrow VDC (NVDC) power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. This architecture maintains system operation even when the battery is completely discharged or removed. When the input current limit or input voltage limit is reached, the power path management automatically reduces the charge current. If system load continues to increase, the power path discharges the battery until the system power requirement is met. This supplement mode prevents overloading the input source.

The device initiates and completes a charging cycle without host control. At start-up, the device reads the resistor value on CELL, VCHG and ICHG pins to determine the correct settings for the charge profile, and the register settings are updated accordingly. The device then proceeds to charge the battery in four different phases, according to the sensed battery voltage: trickle charge, pre-charge, constant current (CC) charge and constant voltage (CV) charge. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset threshold and the battery voltage is higher than the recharge threshold. Termination is supported for TS pin COOL, NORMAL, and WARM temperature zones. When the full battery voltage falls below the programmable recharge threshold, the charger automatically starts a new charging cycle. The charger seamlessly transitions between buck, boost and buck-boost modes based on input voltage and battery voltage without host control.

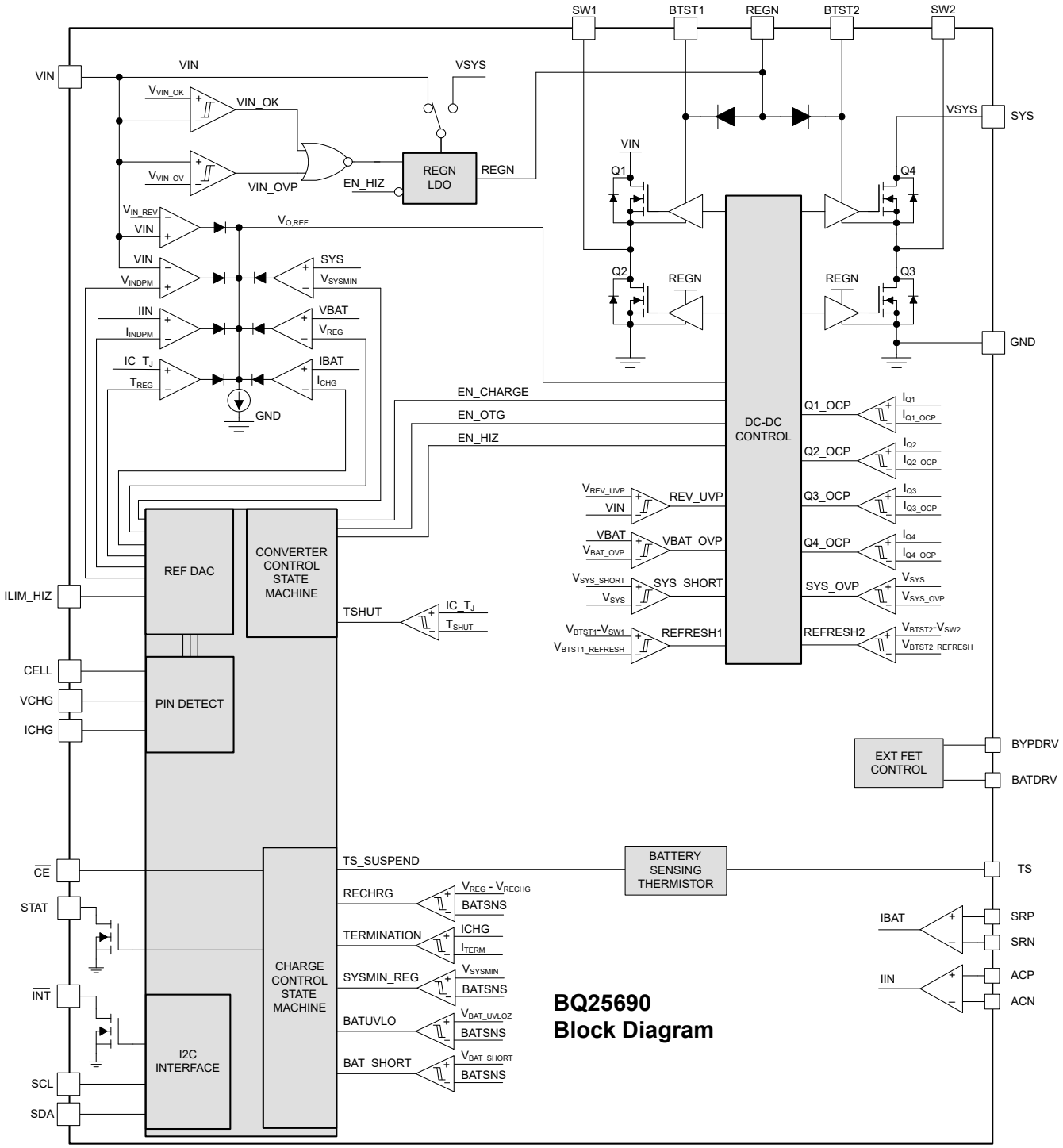
In the absence of input sources, BQ25690 supports reverse mode operation, discharging the battery to generate an adjustable 3.5V to 34V output voltage on VIN with 20mV step size. The adjustable output voltage is compliant with the USB PD 3.0 specification defined PPS feature. The BQ25690 also supports a backup feature using the same mechanism in which a system load connected at VIN can be supplied with the adjustable reverse mode voltage when the adapter is removed. Once configured, the integrated backup comparator automatically triggers the converter to discharge the battery, holding up the VIN node and transitioning into backup mode without host intervention.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor (NTC) monitoring, trickle charge, pre-charge and fast-charge timers, and over-voltage and over-current protections on the battery and the charger power input pin. The thermal regulation reduces charge current when the die temperature exceeds a programmable threshold. The STAT output of the device reports the charging status and any fault conditions. The $\overline{\text{INT}}$ pin immediately notifies the host when a fault occurs or the status changes.

The device is available in a WQFN 4mm × 3.5mm 26-pin package.

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6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Power-On-Reset

Either V_{IN} or the battery connected at SRN power the internal bias circuits of the charger. Verify that the valid voltage to power up the device is greater than V_{VIN_OK} when powering from VIN or V_{BAT_OK} when powering from the battery.

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6.3.2 Battery Only Power Up State

The charger enters Battery Only mode when there is no valid input source at VIN. The device is ready for I^2C communication, and the converter is ready to operate in reverse mode. The charger is in a low quiescent current mode with BATFET turned on to support the system load, and with REGN turned off.

6.3.3 Device HIZ State

The HIZ state is state refers to a charger state in which the REGN LDO is off, and the converter stops switching, even if a valid adapter is present. The device draws I_{HIZ_VIN} from the input supply, and the system load is provided by the battery.

The device enters HIZ mode when EN_HIZ bit is set to 1 or the ILIM_HIZ pin is pulled above $V_{IH_ILIM_HIZ}$ (refer to ILIM_HIZ Pin).

If the device is operating in reverse mode with the converter turned on and enters HIZ mode (EN_HIZ bit is set to 1 or ILIM_HIZ pin is pulled above $V_{IH_ILIM_HIZ}$), switching stops. Once the host clears the HIZ mode condition, the device resumes reverse mode operation.

The device exits HIZ Mode when the EN_HIZ bit clears to 0 and the ILIM_HIZ pin is no longer pulled high. Once device exits HIZ mode through the ILIM_HIZ pin, the CELL, ICHG and VCHG pin values update, allowing for standalone charger settings updated by toggling the ILIM_HIZ pin.

6.3.4 Power Up REGN LDO

When the device powers up from VIN, the LDO turns on when V_{VIN_OK} < VIN < V_{VIN_OVP} and the charger is not in HiZ mode due to EN_HIZ bit =1. When the device is powered from battery only, the LDO is turned on only when operating in reverse mode to minimize battery quiescent current and extend battery life.

The REGN LDO supplies internal bias circuits and the MOSFETs gate drivers. The pull-up rails of TS and STAT can connect to REGN. Use the $\overline{INT}$ pin pull-up rail as an external voltage source, rather than REGN. This is because at battery only condition, REGN output is not available.

6.3.5 Default VINDPM Setting

The device supports wide range of input voltage limit (2.5V – 34V) for high voltage charging and provides two methods to set input voltage limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM (FORCE_VINDPM = 1)
   Setting FORCE_VINPM = 1 disables the VINDPM threshold setting algorithm. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.
2. Relative VINDPM based on the unloaded VIN voltage (FORCE_VINDPM = 0)

When FORCE_VINDPM = 0, the VINDPM threshold setting algorithm is enabled, and VINDPM limit is automatically changed during following conditions:

- Adapter Plug-in (V_{VIN} > V_{IN_OK})
- Exiting the HIZ mode with EN_HIZ register bit

The charger automatically sets the default VINDPM threshold as:

- 84.375% of unloaded VIN when VIN ≤ 6V (5V input sets a 4.2V VINDPM)
- 87.5% of unloaded VIN when VIN > 6V (20V input sets a 17.5V VINDPM)

The unloaded VIN is remeasured when the EN_HIZ bit is toggled. This causes the converter to stop switching, and the VINDPM register field is updated. To maintain the system voltage during the HIZ toggle event, the host must verify that a battery is present.

When the unloaded VIN is out of the VINDPM register range, the changer sets the VINDPM register to the minimum value (2.5V) or maximum (34V) value, as appropriate.

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6.3.6 Default Charge Profile Setting With CELL, ICHG and VCHG Pins

The device offers standalone charge profile programming using the CELL, ICHG, and VCHG pins. The resistance on these pins is read at start-up and the value is used to determine the default charge voltage (CELL and VREG registers) and charge current (ICHG register) for the device. Once the device exits HIZ mode using the ILIM_HIZ pin, the CELL, ICHG, and VCHG pin values update, allowing for standalone charger settings update by toggling ILIM_HIZ pin.

The Pin Detection Status registers bits (VCHG_PIN, CELL_PIN, ICHG_PIN) store the result of the pin detection.

Table 6-1. CELL Pin Detection

CELL RESISTOR (kΩ)	CELL_PIN	CELL COUNT	VSYSMIN REGISTER DEFAULT
<3.8	0	FAULT, no charge	FAULT, no charge
4.64	1	1s	3.5V
6.04	2	2s	6.2V
8.25	3	3s	9.3V
10.5	4	4s	12.4V
13.7	5	5s	15.5V
16.9	6	6s	18.6V
27.4	7	7s	21.7V
>46.8	0	FAULT, no charge	FAULT, no charge

Table 6-2. VCHG Pin Detection

VCHG RESISTOR (kΩ)	VCHG_PIN	CHARGE VOLTAGE (VREG)
<3.8	0	FAULT, no charge
4.64	1	3.5V × CELL COUNT
6.04	2	3.6V × CELL COUNT
8.25	3	4.0V × CELL COUNT
10.5	4	4.1V × CELL COUNT
13.7	5	4.2V × CELL COUNT
16.9	6	4.3V × CELL COUNT
27.4	7	4.35V × CELL COUNT
>46.8	0	FAULT, no charge

Table 6-3. ICHG Pin Detection

ICHG RESISTOR (kΩ)	ICHG_PIN	CHARGE CURRENT (ICHG)	PRECHARGE AND TERMINATION (IPRECHG / ITERM)
<3.8	0	FAULT, no charge	FAULT, no charge
4.64	1	0.1A	40mA / 40mA
6.04	2	0.5A	60mA / 60mA
8.25	3	1.0A	100mA / 100mA
10.5	4	1.5A	160mA / 160mA
13.7	5	2.0A	200mA / 200mA
16.9	6	2.5A	260mA / 260mA
27.4	7	3.3A	340mA / 340mA
>46.8	0	FAULT, no charge	FAULT, no charge

The ICHG pin setting is referenced to a 10mΩ sense resistor. Use a 5mΩ sense resistor for better efficiency. Use the R_{BAT_SNS} register bit to change the sense resistor value to 5mΩ. Setting R_{BAT_SNS} register bit to 1 scales the internal values to provide the same programmed ICHG while using a 5mΩ sense resistor.

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The CELL pin and VCHG pin results combine to program the charge voltage at VREG register. For example, if CELL pin and VCHG pin resistors are both 13.7kΩ, the resulting VREG voltage is: 4.2V/cell × 5cell = 21V.

The CELL pin is also used to program the VSYSMIN register. For 1s detection, VSYSMIN is programmed at 3.5V, while all higher cell counts are programmed with 3.1V/cell. Returning to the 13.7kΩ example from before, the resulting VSYSMIN value is 15.5V.

The CELL detected value is stored in the register map at the CELL_PIN, the ICHG detected value is stored in the register map at the ICHG_PIN, and the VCHG detected value is stored in the register map at the VCHG_PIN registers. After detection, the value in the ICHG and VREG registers updates, and the detected value becomes the upper clamp. For example, if ICHG pin resistor is set to 1.0A, an I^2C write to the ICHG register requesting >1.0A is ignored. To overwrite the clamp, the ICHG_PIN_OVERRIDE register must first be written to 1, then the ICHG register takes the full range of values. The requirement is similar for VREG: to write higher values than the result from pin detection, the VCHG_PIN_OVERRIDE registers must be written to 1, then the VREG and VSYSMIN can be updated. Even though VCHG_PIN_OVERRIDE=1, VREG still is clamped based on CELL_PIN based on the following table:

Table 6-4. VREG Upper Clamp VCHG_PIN_OVERRIDE = 1

CELL_PIN	VREG UPPER CLAMP
1s	4.8V
2s	9.6V
3s - 4s	19.2V
5s - 7s	33V

To change the CELL count and/or increase charge voltage (VREG) after POR, the following sequence is recommended:

1. Disable charge (EN_CHG = 0)
2. Set CELL_PIN_OVERRIDE = 1
3. Change CELL_PIN register to appropriate value for desired cell count
   a. Note, VREG register is automatically updated based on CELL_PIN selection
   b. Note, SYSMIN register is automatically updated based on CELL_PIN selection
4. Set VCHG_PIN_OVERRIDE = 1
5. Change VREG to appropriate value
   a. Note, VREG is still clamped based on CELL_PIN selection with VCHG_PIN_OVERRIDE = 1
6. Change VSYSMIN to appropriate value

As an example, if POR detections are 5s (CELL Resistor = 13.7kΩ) charging at 4.0V/cell (VCHG Resistor = 8.25kΩ), and changing to 4s charging at 4.2V/cell is desired, the following table shows the sequence of commands:

Table 6-5. I^2C command Sequence Needed For Updating CELL

REGISTER	PREVIOUS VALUE	NEW VALUE
EN_CHG	1	0
CELL_PIN_OVERRIDE	0	1
CELL_PIN	5	4
VCHG_PIN_OVERRIDE	0	1
VREG	16.0V (4.0V/cell)	16.8V (4.2V/cell)
VSYSMIN	12.4V (3.1V/cell)	12.8V (3.2V/cell)
EN_CHG	0	1

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If a fault is detected on any of the three pins, the device does not automatically start a charge cycle (EN_CHG cleared to 0 by the device). Recover the fault by overriding the pin detection status using the CELL_PIN_OVERRIDE, VCHG_PIN_OVERRIDE, or ICHG_PIN_OVERRIDE bits. A host is required to program the desired charge profile registers to the appropriate values. Finally, set the EN_CHG bit back to 1. The converter remains on and regulates SYS to VSYSMIN after pin fault is detected.

As an example, the following sequence is presented to recover from a CELL pin fault to charge a 5s battery:

1. Set CELL_PIN_OVERRIDE bit to 1
2. Set CELL_PIN register to 5
3. Set VSYSMIN register to 15.5V
4. Set VREG to desired charge voltage (for 4.2V charge voltage, use VREG = 21V)
5. Set EN_CHG = 1

6.3.7 Buck-Boost Converter Operation

The charger employs a synchronous, 4-switch buck-boost converter that allows forward (sink) operation with input power at VIN and output power at SYS, reverse (source) operation with input power from a battery at SRN and output power at VIN or bypass mode which connects the VIN and SYS.

In forward and reverse modes, the charger operates as a buck, buck-boost, or boost converter based on different input voltage and output voltage combinations. The converter seamlessly transitions the buck, buck-boost, and boost operating regions. During buck-boost mode, the converter alternates a SW1 pulse with a SW2 pulse, with effective switching frequency interleaved among these pulses for highest efficiency operation. The transition from buck or boost to buck-boost operation is a propriety function of duty cycle and load current. For the charger to provide full support for the charge current and system load, the average inductor current must not be expected to exceed 4A.

6.3.7.1 Pulse Frequency Modulation (PFM)

To improve converter light-load efficiency in either forward or reverse operation, the device switches to pulse frequency modulation (PFM) control at light load when the EN_PFM bit is set to 1. The effective switching frequency decreases accordingly when system load decreases. Disable PFM operation by setting EN_PFM = 0, in which case the converter stays at PWM mode switching frequency, and transitions to DCM operation at light load condition. Limit the minimum effective switching frequency in PFM to 25kHz to eliminate the audible noise concern if the out of audio (OOA) feature is enabled by setting EN_PFM_OOA = 1.

6.3.7.2 Switching Frequency and Dithering Feature

Typically, the device switches with a fixed frequency. The charger also supports a frequency dithering function to improve EMI performance and help pass IEC-CISPR 22 specification. This dithering function is disabled by default with setting EN_DITHER=00b. Enable the function by setting EN_DITHER=01/10/11b. The switching frequency is not fixed when dithering is enabled. The switching frequency varies within determined range by EN_DITHER setting, 01/10/11b is corresponding to ±2%/4%/6% switching frequency. The larger the selected dithering range, the smaller the EMI noise peak; however, a slightly larger VIN/VSYS capacitor voltage ripple generates. Therefore, the dithering frequency range selection is a trade-off between EMI noise peak and VIN/VSYS voltage ripple. Select the lowest dithering range which can pass IEC-CISPR 22 specification. The patented dithering pattern can improve EMI performance from switching frequency and up to 30MHz high frequency range which covers the entire conductive EMI noise range.

6.3.8 Forward (Sink) Operation

With input power at VIN in forward (sink) operation, the charger's converter regulates SYS to V_{SYSMIN_REG} and provides the load current the system at SYS pin. If a battery is attached to SRN, the charger provides current first to the SYS load and then to charge the battery. Once the battery voltage reaches the VSYSMIN voltage, the SYS voltage follows the battery voltage up to regulation.

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6.3.8.1 Power Path Management

The device accommodates a wide range of input voltage range from 2.5V to 34V supporting applications powered from battery, standard USB-PD adapters, and high voltage dedicated DC adapters. The device provides automatic power path selection to supply the system from input source, battery or both, while preventing input source collapse.

6.3.8.1.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYSMIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage. The default minimum system voltage at POR is determined according to the CELL pin configuration resistor.

The NVDC architecture also provides charging termination when the battery is fully charged. By turning off the BATFET, the adapter power is prioritized to support the system, which avoids having the battery continuously charged and discharged by the system load even if the adapter is present. This is important for extending the battery life time.

When the battery voltage is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at around 200mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the $R_{DS(ON)}$ of the BATFET multiplied by the charging current. When battery charging is disabled and battery voltage is above the minimum system voltage setting or charging is terminated, the system is regulated at 200mV (typical) above battery voltage.

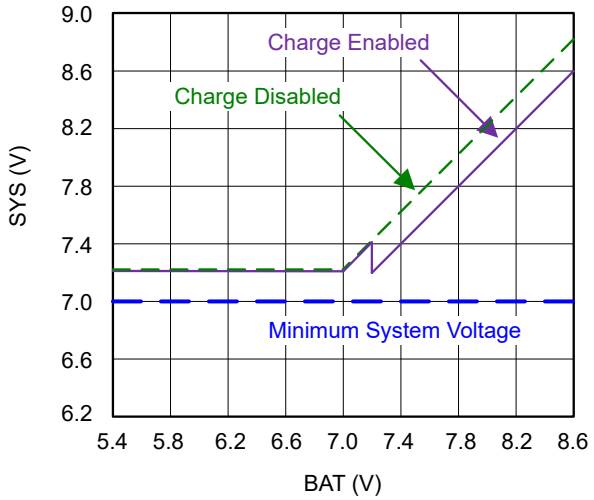


Figure 6-1. Typical System Voltage vs Battery Voltage for a 2S Battery Configuration

6.3.8.1.2 Dynamic Power Management

To use the maximum available current from the input power source without overloading the adapter, the charger features dynamic power management (DPM). DPM continuously monitors the input current and input voltage. When the input power (P_{IN}) is lower than the demanded output power (P_{SYS} + P_{BAT}), the charger engages either IINDPM to limit the input current or VINDPM to prevent further reduction in VIN pin voltage.

When the system voltage is regulated at VSYSMIN and SYS voltage temporarily drops lower than VSYSMIN, the VSYSMIN loop reduces charging current so that the SYS voltage remains at the VSYSMIN level. If the charge current falls to zero, but the input source is still overloaded, the SYS voltage drops. Once the SYS voltage falls below the battery voltage, the device automatically enters supplement mode and the battery FET turns on. The battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VINDPM_STAT and/or IINDPM_STAT go high. Figure 6-2 shows the DPM response with 5V/3A adapter, 6.4V battery, 1.5A charge current and 6.8V minimum system voltage setting.

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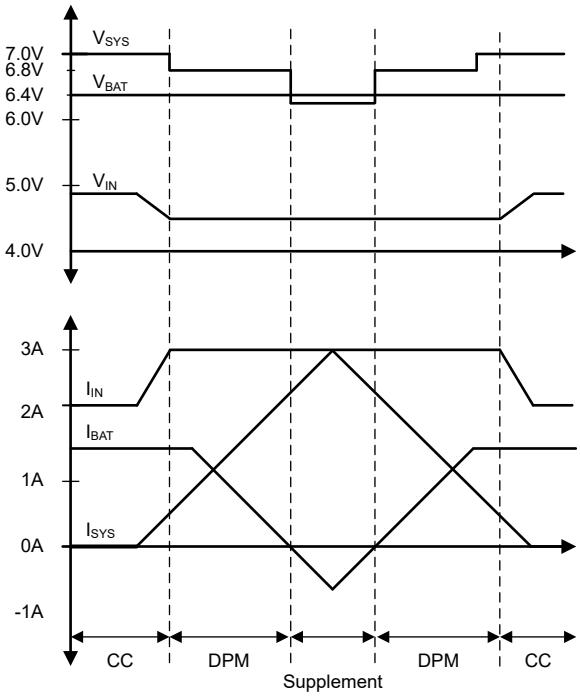


Figure 6-2. DPM Response

6.3.8.1.2.1 ILIM_HIZ Pin

Use a pulldown resistor to GND to set the maximum input current using the ILIM_HIZ pin. When using a 10mΩ R_{AC_SNS} resistor, the input current limit is controlled by:

$$I_{IN_MAX} = K_{ILIM} \div R_{ILIM} \quad (1)$$

The actual input current limit is the lower value between ILIM_HIZ pin setting and register setting (IINDPM). For example, if the register setting is 3.3A, and ILIM_HIZ pin has a 6.04kΩ resistor to ground for 0.551A, the actual input current limit is 0.551A. Use the ILIM_HIZ pin to set the input current limit when the EN_EXTILIM bit is set to 1.

Use the ILIM_HIZ pin to monitor the input current. The voltage on ILIM_HIZ pin (V_{ILIM_HIZ}) is proportional to the input current. Pin voltage can be used to monitor input current with the following relationship:

$$IIN = K_{ILIM} \times V_{ILIM_HIZ} / (R_{ILIM} \times 1V) \quad (2)$$

For example, if the pin is set with 3.32kΩ resistor, and the pin voltage is 0.5V, the actual input current is between 451mA to 552mA (based on K_{ILIM} specified).

As the input current rises, then pin voltage rises proportionally up to 1V. Once the device enters input current regulation, the ILIM pin voltage clamps to 1V. Entering input current regulation through the pin sets the IINDPM_STAT and FLAG bits, and produces an interrupt to host. The interrupt can be masked through the IINDPM_MASK bit.

If ILIM_HIZ pin shorts to ground, the IINDPM register sets the input current limit. If the hardware input current limit function is not needed, short this pin to GND. If ILIM_HIZ pin is pulled above $V_{IH_ILIM_HIZ}$, the device enters HIZ mode (refer to Device HIZ State). Disable the ILIM_HIZ pin function by setting the EN_EXTILIM bit to 0. When the pin is disabled, input current limit and monitoring functions, as well as HIZ mode control through the pin, are not available.

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K_{ILIM} is referenced to a 10mΩ sense resistor. Use a 5mΩ sense resistor for better efficiency. Use the R_{AC_SNS} register bit to change the sense resistor value to 5mΩ. Setting the R_{AC_SNS} register bit to 1 scales the internal values to provide the same A × Ω, while using a 5mΩ sense resistor.

6.3.8.1.2.2 Input Current Optimizer (ICO)

The device provides input current optimizer (ICO) to identify the input sources maximum power point to avoid overloading the input source. The algorithm automatically identifies maximum input current limit of an unknown power source and sets the charger IINDPM register properly, to prevent from entering the charger input voltage (VINDPM) regulation. This feature is controlled with the EN_ICO register bit.

The actual input current limit used by the dynamic power management is reported in the ICO_IINDPM register whether set by ICO if enabled or IINDPM register if not. In addition, ILIM_HIZ pin resistor setting clamps the maximum current limit to disable the ILIM_HIZ pin function, unless the EN_EXTILIM bit is 0. The IINDPM register does not report the clamp value.

When V(BAT) > VSYSMIN, the ICO algorithm starts with the maximum allowed input current set to 500mA then continually increases this limit until the optimal limit is found. When VBAT < VSYSMIN, the battery voltage can be too low to supplement a large system load if the converter is limited to 500mA and then ramped up by the ICO algorithm. Therefore, when a VBAT < VSYSMIN, the ICO algorithm starts with the maximum allowed input current in the IINDPM register and then continually decreases this limit until the optimal input current limit is found.

Once the optimal input current is identified, the ICO_STAT and ICO_FLAG bits are set. The actual input current is reported in the ICO_IINDPM register and does not change unless the algorithm is triggered again by the following events:

1. A new input source is plugged-in, or EN_HIZ bit is toggled
2. IINDPM register is changed
3. VINDPM register is changed
4. FORCE_ICO bit is set to 1
5. VIN_OVP event

These events also reset the ICO_STAT[1:0] bits to 01

If the optimal current is not identified (for example, if output power < maximum input power), the ICO routine is suspended until more power is needed from the input. In this case, the ICO_STAT bits are set to 0b11.

6.3.8.2 Battery Charging Management

The device charges 1S to 7S Li-Ion batteries with up to 3.3A charge current for high capacity cells. The battery charging in different stages is controlled internally according to the battery voltage. The low external BATFET improves charging efficiency and minimizes the voltage drop during discharging.

6.3.8.2.1 Battery Detection

For applications with removable battery, the device includes a battery detection routine which aims to maintain a steady system voltage while checking for the battery to be applied again.

If VBAT < V_{BAT_SHORT} at startup, the device uses trickle charge current to charge the SRN pin to V_{BAT_DET} (programmable via I^2C). Subsequently, SRN is allowed to discharge by 200mV. If the SRN pin successfully moves between V_{BAT_DET} and V_{BAT_DET}-200mV, a battery is not present, and the BAT_FAULT_STAT is set to 01. During battery detection, the converter continues to regulate SYS to V_{BAT_DET} + 400mV or V_{SYSMIN} + 200mV, whichever is higher, allowing uninterrupted system operation even with an absent battery. If at any point the SRN pin does not charge to VBAT_DET or discharge to VBAT_DET-200mV within 2 seconds, a battery has been plugged in. Once the battery plugin is detected, charging resumes normally, the internal regulation target is moved up to VREG and the BAT_FAULT_STAT is set to 00.

If the battery is removed during a charge cycle, the device continues to charge the SRN pin up to VREG and terminate very quickly. If the device detects 4 termination events within 20 seconds, a no battery condition is assumed on the 4th termination, and the BAT_FAULT_STAT is set to 01. The device then returns to the

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operation outlined above, charging and discharging the SRN pin voltage between V_{BAT_DET} and V_{BAT_DET} - 200mV. At the same time, the converter regulates SYS to V_{BAT_DET} + 400mV or V_{SYSMIN} + 200mV, whichever is higher.

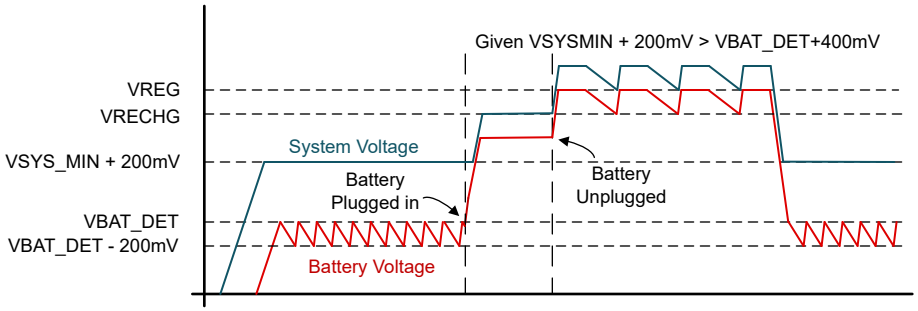


Figure 6-3. Battery Detection

Disable the battery detection function by setting EN_BAT_DETECT = 0.

6.3.8.2.2 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit =1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 6-6. The host controls the charging operation and optimizes the charging parameters by writing to the corresponding registers through I^2C.

Table 6-6. Charging Parameter Default Settings

DEFAULT MODE	BQ25690
Charging voltage (VREG)	Based on the resistance on VCHG pin and CELL pin
Recharging voltage threshold (VRECHG)	95.5% × VREG (≅190mV/cell for Li-Ion)
Precharge to fast charge voltage threshold (VBAT_LOWV)	71.4% × VREG (≅3V/cell for Li-Ion)
Fast charge current (ICHG)	Based on the resistance on ICHG pin
Pre-charge current (IPRECHG)	Based on the resistance on ICHG pin
Trickle charge current (fixed value)	100mA
Termination current (ITERM)	Based on the resistance on ICHG pin
Temperature profile	JEITA
Fast charge safety timer (CHG_TMR)	12 hours
Pre-charge safety Timer (PRECHG_TMR)	2 hours

A new charge cycle starts when the following conditions are valid:

- VIN > V_{VIN_OK}
- VBAT < V_{RECHG}
- Battery charging enables by setting register bit EN_CHG = 1 and $\overline{CE}$ pin LOW
- No thermistor fault on TS pin
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and the device is not in DPM mode or thermal regulation. When a fully charged battery voltage is discharged below recharge threshold, the device automatically starts a new charging cycle. After the charging terminates, toggling either $\overline{CE}$ pin or EN_CHG bit initiates a new charging cycle. In addition, the device offers a dedicated CV timer to stop the charging after a programmable period (CV_TMR bits) in CV mode, regardless of the charge current value.

The Charge status register (CHARGE_STAT) indicates the different charging phases as:

- 000 – Not Charging

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- 001 – Trickle Charge (VBAT < V_{BAT_SHORT})
- 010 – Pre-charge (V_{BAT_SHORT} < VBAT < V_{BAT_LOWV})
- 011 – Fast Charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the charger transitions to any of these states, including when the charge cycle completes, an $\overline{INT}$ is asserted to notify the host.

6.3.8.2.3 Battery Charging Profile

The device charges the battery in five phases:

1. Trickle charge
2. Pre-charge
3. Constant current
4. Constant voltage
5. Top-off trickle charging (optional)

At the beginning of a charging cycle, the device checks the battery voltage and accordingly regulates the current and voltage.

Table 6-7. Default Charging Current Setting

VBAT	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHARGE_STAT
< V_{BAT_SHORT}	I_{BAT_SHORT}	100mA (fixed value)	001
V_{BAT_SHORTZ} to V_{BAT_LOWV}	I_{PRECHG}	Based on resistance on ICHG pin	010
> V_{BAT_LOWV}	ICHG	Based on resistance on ICHG pin	011

If the charger is in DPM regulation or thermal regulation during charging, the actual charging current is less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in Charging Safety Timer.

During VSYSMIN regulation with BATFET LDO operation, charge current is limited in accordance with Table 6-8. This helps protect the BATFET from excessive power dissipation. The actual value of the ICHG register is not modified when this clamp is enabled.

Table 6-8. VSYSMIN Battery Charging Current Clamp

VSYSMIN - V_{BAT}	ICHG CLAMP	IPRECHG CLAMP
<0.6V	3.3A	0.62A
>0.6V, <1.6V	1.26A	0.62A
> 1.6V	0.3A	0.3A

V_{BAT_SHORTZ} is the battery voltage threshold for the transition from trickle charge to precharge, which is 2.2V/cell. When the battery is below V_{BAT_SHORTZ}, the VSYSMIN is clamped to protect the BATFET from high power dissipation.

Table 6-9. VSYSMIN Clamp vs CELL Count When V_{BAT}<V_{BAT_SHORTZ}

CELL	VSYSMIN UPPER CLAMP
1s - 2s	5V per cell
3s	4.4V per cell
4s	3.9V per cell
5s - 7s	3.2V per cell

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V_{BAT_LOWV} is the battery voltage threshold for the transition from pre-charge to fast charge. V_{BAT_LOWV} is a ratio of battery voltage regulation limit (VREG).

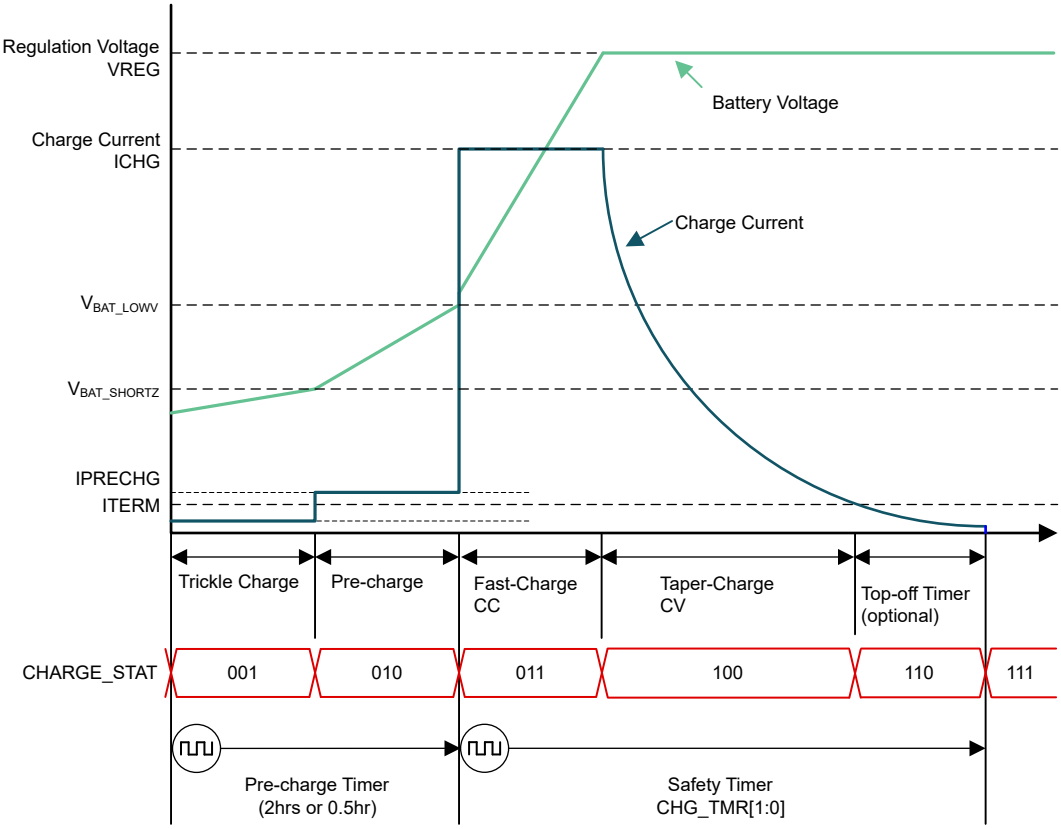


Figure 6-4. Battery Charging Profile

6.3.8.2.4 Charging Termination

The device terminates a charge cycle when the battery voltage is above the recharge threshold, the converter operates in the battery constant voltage regulation loop and the charge current is below the set termination current (ITERM). After the charging cycle completes, the BATFET turns off. The converter keeps running to power the system. If the supplement mode triggers, the BATFET turns on again.

When termination is done, the status register CHARGE_STAT is set to 111 and an $\overline{INT}$ pulse is asserted to the host. Termination temporarily disables when the charger device is in input current (IINDPM), input voltage (VINDPM), or thermal (TREG) regulation. Permanently disable termination by writing 0 to EN_TERM bit prior to charging termination. Writing 0 to EN_TERM when the termination has already occurred or in the top-off charging stage does not disable termination, until the next charging cycle restarts. If termination is enabled by setting EN_TERM = 1 during an active charging cycle, the change is applied immediately.

At low termination currents (< 160mA), due to the comparator offset, the actual termination current can be up to ≅20% to ≅40% higher than the termination target. To compensate for the comparator offset, activate a programmable top-off timer (default disabled) after termination. While the top-off timer is running, the device continues to charge the battery in constant voltage mode (BATFET stays on) until the top-off time expires. The top-off timer follows safety timer constraints, such that if the safety timer is suspended, so is the top-off timer, and if the safety timer is doubled, so is the top-off timer. CHARGE_STAT reports whether the top off timer is active through the 110 code. Once the top-off timer expires, charging terminates, the CHARGE_STAT register is set to 111 and an $\overline{INT}$ pulse is asserted to the host.

The top-off timer resets (set to 0 and counting resumes when appropriate) for any of the following conditions:

1. Charge disable to enable

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2. Termination status low to high
3. REG_RST register bit is set (disables top-off timer)

Once the charger detects termination, the charger reads the top-off timer (TOPOFF_TMR) settings. Programming the top-off timer value after termination resets the timer. The top-off timer only starts to count when the termination criteria of the charger are met. If EN_TERM = 0, the charger never terminates charging, so the top-off timer does not start counting, even if the timer is enabled. An $\overline{INT}$ is asserted to the host when the top-off timer starts counting as well as when the top-off timer expires. The CHG_MASK bit can mask all charge-cycle related $\overline{INT}$ pulses (including top-off timer $\overline{INT}$ pulse).

6.3.8.2.5 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The user can program fast charge safety timer through I^2C (CHG_TMR bits). When safety timer expires, the fault register CHG_TMR_STAT bit is set to 1, and an INT pulse is asserted to the host. Disable the safety timer feature by clearing EN_CHG_TMR bit.

During input voltage, input current, or thermal regulation, the safety timer counts at half clock rate, as the actual charge current is likely to be below the programmed setting. For example, if the charger is in input current regulation (IINDPM_STAT=1) throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer expires in 10 hours. Set EN_TMR2X = 0 to disable the half clock rate feature.

During faults which disable charging, the timer is suspended. Once the fault goes away, the safety timer resumes. If the charging cycle is stopped and started again, the timer is reset (toggle $\overline{CE}$ pin or EN_CHG bit restarts the timer).

The pre-charge safety timer runs when VBAT < V_{BAT_LOWV}. Program the timer duration using PRECHG_TMR bits as 30 minutes or 2 hours. The pre-charge safety timer follows the same rules as the fast-charge safety timer, in terms of suspension and count resetting. However, the pre-charge safety timer is unaffected by the EN_TMR2X bit, and always counts for fixed time (30min or 2hrs). The pre-charge safety timer is disabled when EN_PRECHG bit is 0.

6.3.8.2.6 CV Timer

In some applications, such as batteries with high-leakage or batteries in parallel with a system load, the battery current does not always reach the ITERM threshold while in CV mode. The device offers a dedicated CV timer to control the amount of time the charger stays in CV mode.

The CV timer begins counting when the device enters the CV mode, and the timer duration can be programmed through the CV_TMR register bits. Note that CV_TMR = 0 disables the timer altogether. The CV timer is an absolute timer, and the EN_TMR2X register bit has no effect on the timer.

During faults which disable charging or when device falls out of CV regulation due to IAC_DPM or VAC_DPM, the CV timer is suspended. Once the device return to CV mode, the CV timer resumes. If the charging cycle is stopped and started again, the timer resets (toggle $\overline{CE}$ pin or EN_CHG bit restarts the timer).

An INT is asserted to the host when CV timer expires. Mask the INT using the CV_TMR_MASK bit.

6.3.8.2.7 Thermistor Qualification

The charger device provides a single thermistor input to monitor battery temperature.

6.3.8.2.7.1 JEITA Guideline Compliance in Charge Mode

JEITA guideline from April 20, 2007 highlights information for improving the safety of charging Li-ion batteries. The guideline emphasizes the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, verify that the voltage on TS pin is within the VT1 to VT5 thresholds. If TS voltage exceeds the T1 – T5 range, the controller suspends charging and waits until the battery temperature is within the T1 – T5 range. At cool temperature (T1 – T2), JEITA recommends reducing the charge current to half of the

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charge current or lower. At warm temperature (T3 – T5), JEITA recommends charging the voltage less than 4.1V per cell.

At cool temperature T1 – T2, JEITA recommends reducing the charge current to lower than half of the charge current at normal temperature T2 – T3. The device provides the programmability of the charge current at T1 – T2 an 20%, 40% or 100% of the charge current at T2 – T3 or charge suspend, which is controlled by the register bits JEITA_ISETC.

At warm temperature T3 – T5, JEITA recommends charge voltage less than 4.1V / cell. The device provides the programmability of the charge voltage at T3 – T5, to be with a voltage offset less than charge voltage at T2 – T3 or charge suspend, which is controlled by the register bits JEITA_VSET.

The charger also provides flexible voltage/current settings beyond the JEITA requirements. The charge current setting at warm temperature T3 – T5 can be configured to be 40%, or 100% of the programmed charge current or charge suspend, which is programmed by the register bit JEITA_ISETH.

The default charging profile for JEITA is shown in the figure below, in which the blue line is the default setting and the red dash line is the programmable options.

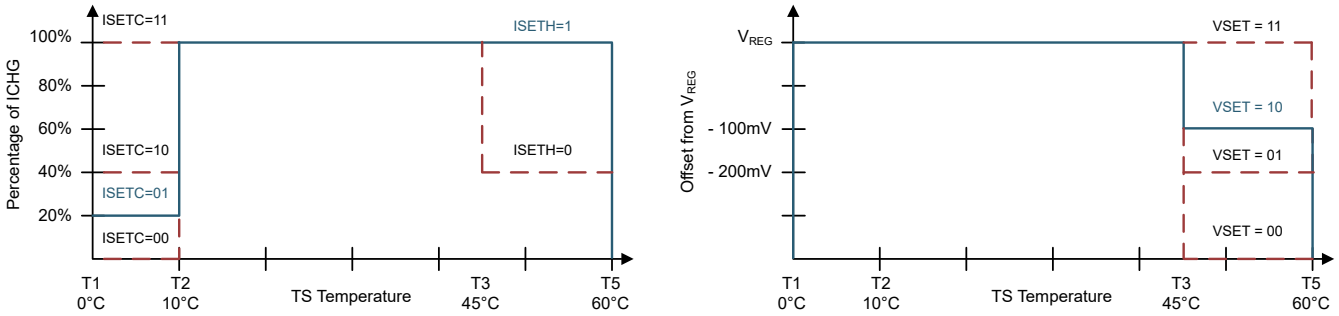


Figure 6-5. TS Charging Values

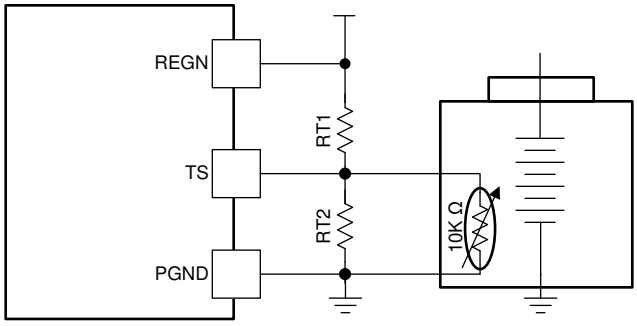


Figure 6-6. TS Resistor Network

Assuming a 103AT NTC thermistor on the battery pack as shown above, the value of RT1 and RT2 can be determined by:

$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{1}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{1}{VT1} - 1\right)} \quad (3)$$

$$RT1 = \frac{\frac{1}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (4)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

- RTH_{T1} = 27.28kΩ

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- RTH_{T5} = 3.02kΩ
- RT1 = 5.36kΩ
- RT2 = 41.2kΩ

The device also offers programmability for all the thresholds using the TS charging threshold control register. This flexibility can help to change the operating window of the charger in software.

Disable the JEITA profile by clearing the EN_JEITA register bit. In this case, the device still limits the charging window from T1 – T5, but no special charge profile is employed within the Cool (T1 – T2) or Warm (T3 – T5) regions.

Disable the NTC monitoring window by clearing the EN_TS register bit. In this case, the TS pin voltage is ignored, and the device always reports normal TS status.

6.3.8.2.7.2 Cold/Hot Temperature Window in Reverse Mode

For battery protection during reverse or backup modes of operation, the device monitors the battery temperature to be within the TS COLD to TS HOT thresholds. When temperature is outside of the thresholds, the reverse mode is suspended, and the converter stops switching. The TS_STAT is reported (TS Cold or TS Hot). Completely disable the temperature protection in reverse mode by clearing the EN_TS bit to 0. The device automatically resumes reverse mode operation when the fault condition clears. During a TS fault, REGN remains on.

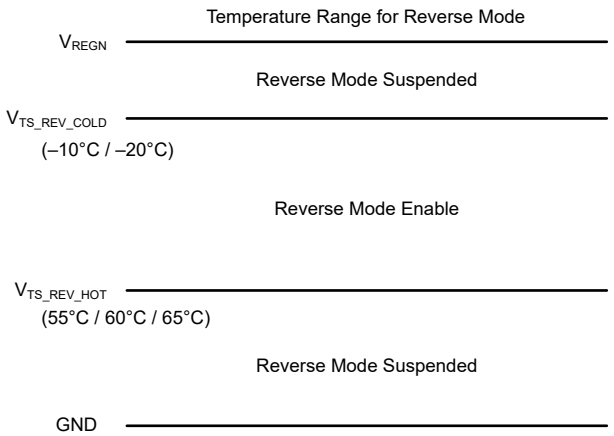


Figure 6-7. TS Pin Thermistor Sense Threshold in Reverse Mode

6.3.8.3 Bypass Mode

The device supports bypass mode to allow VSYS = VIN without regulation and highest efficiency. In this operating mode, the buck and boost high-side FETs (Q1 and Q4) are both turned on, while the Buck and Boost low-side FETs (Q2 and Q3) remain off. The input power directly passes through the power stage to the output. The switching losses of MOSFETs and the inductor core loss are eliminated, thereby providing highest efficiency. Enable the bypass mode by setting the EN_BYPASS register bit to 1. Bypass mode requires the R_{AC_SNS} resistor to sense for overcurrent and light-load conditions.

When using USB-PD programmable power supply (PPS) as input adapter, bypass mode can be leveraged to achieve flash charge under the battery fast charging period. By enabling flash charge, this further improves the charge efficiency with an even higher charge current. During pre-charge and CV charging phases, the charger can go back to buck-boost mode.

While device is in bypass mode, the current through R_{AC_SNS} is monitored and compared against the IINDPM register setting. If the input current exceeds I_{BYP_OCP} (15% above IINDPM setting) for t_{BYP_OCP}, the device automatically exits bypass mode and returns to PWM regulation mode (switching power stage enabled). The EN_BYPASS bit is cleared back to 0, BYPASS_FLAG bit is set, and an INT pulse is asserted to signal the host if BYPASS_MASK is cleared.

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Enter bypass mode when VSYS is within 0.5V of VIN to avoid inrush current false tripping the bypass over-current protection. Typical use case is to first change the VSYSMIN setting to achieve a condition of VSYS approximately equal to VIN, then set EN_BYPASS = 1.

While device is in bypass mode, the BATFET operates in linear regulation mode to control the charging current into the battery, if battery charging is enabled. For Q1 and Q4 to be held on continuously, SRN/SRP voltage must be within approximately 2V of VIN/VSYS. If VSYS-VBAT > 2V then bootstrap refreshes occurs.

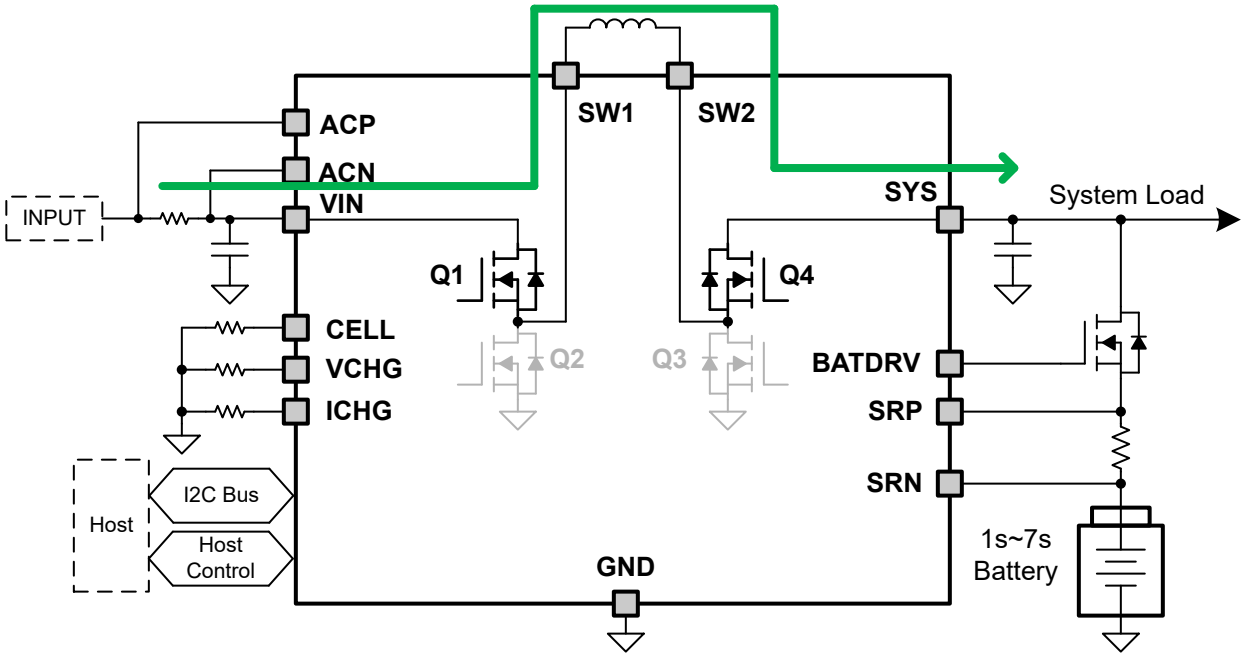


Figure 6-8. Internal Bypass Mode

In addition to the internal bypass mode, the device offers external bypass mode for highest efficiency with up to 5A current. In this case, the BYPDRV pin drives external back-to-back MOSFET to directly connect the VIN to SYS. The external bypass mode is enabled by setting EN_EXT_BYPASS = 1, as well as EN_BYPASS = 1. If EN_EXT_BYPASS = 1 while EN_BYPASS = 0, then bypass is not entered. The EN_BYPASS bit determines if bypass mode is enabled. EN_EXT_BYPASS determines if external bypass is enabled while EN_BYPASS = 1. Set EN_EXT_BYPASS before or after the device enters bypass mode through EN_BYPASS.

While device is in external bypass mode, the current through R_{AC_SNS} is monitored. If the R_{AC_SNS} current exceeds I_{EXTBYP_OCP} for t_{BYP_OCP}, the device automatically exits external bypass mode and returns to PWM regulation mode (switching power stage enabled). The EN_BYPASS bit is cleared back to 0, BYPASS_FLAG bit is set, and an INT pulse is asserted to signal the host if BYPASS_MASK is cleared. Note, the EN_EXT_BYPASS bit is not changed.

To prevent reverse boost-back after input source removal when charger is in bypass mode, there is light-load bypass auto exit feature. The charger monitors for the input current dropping below I_{BYP_LL}, at which point the charger automatically exits bypass mode and returns to PWM regulation mode. This protection is active during both internal and external bypass modes. Disable the protection by setting EN_BYPASS_LL_EXIT = 0. The EN_BYPASS bit is cleared back to 0, BYPASS_FLAG bit is set, and an INT pulse is asserted to signal the host if BYPASS_MASK is cleared.

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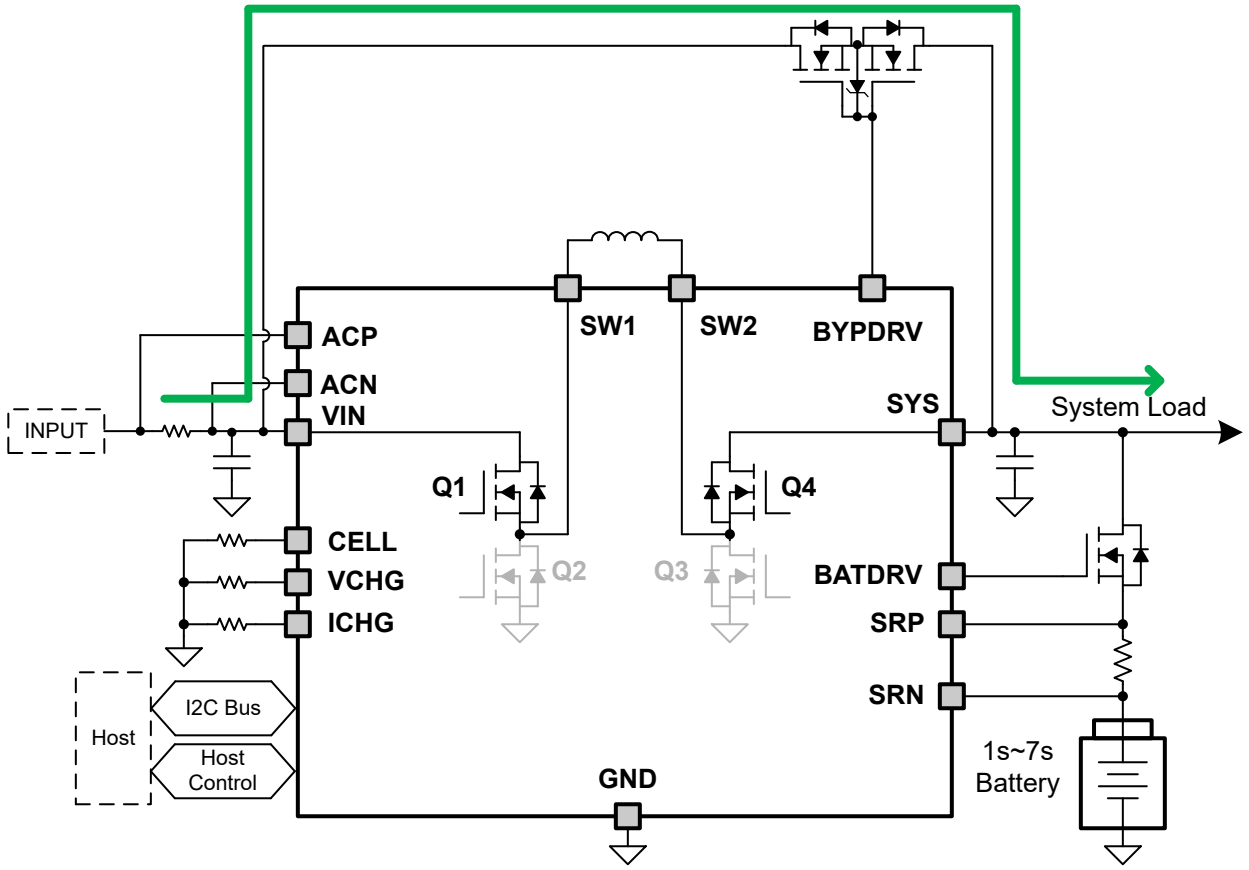


Figure 6-9. External Bypass Mode

6.3.9 Reverse (Source) Mode (USB On-The-Go)

6.3.9.1 Reverse (Source) Mode Operation

The device supports reverse mode operation to deliver regulated power from the battery to other devices connected to the input port. The reverse mode voltage regulation (CV) target is set in VIN_REV register bits. The reverse mode R_{AC_SNS} current regulation (CC) target is set in IIN_REV register bits. To enable reverse mode operation, the following conditions have to be valid:

- The battery voltage is above V_{BAT_OK}
- The VIN is below V_{VIN_OK}
- The voltage at TS pin is within the range configured by TS_REV_HOT and TS_REV_COLD register bits
- Battery detection is disabled (EN_BAT_DETECT = 0)

The device regulates the VIN reverse mode voltage when the R_{AC_SNS} reverse mode current is below the IIN_REV register bits. When the demanded load increases above the IIN_REV register, the device regulates the current through R_{AC_SNS} (CC mode), and the output voltage at VIN drops. The REV_STAT bits are set to 0x2, and an $\overline{INT}$ pulse is asserted. If the VIN voltage drops below V_{INREV_UV}, the device exits reverse mode, clears EN_REV to 0 and sets REV_STAT bits to 0x3 until the charger changes state, for example, until reverse mode is re-enabled by the host setting EN_REV=1 or the input source is attached for forward/charge mode. Also, an $\overline{INT}$ pulse is asserted.

The charger can regulate the battery discharging current during reverse mode. When battery current rises higher than the IBAT_REV register setting, the charger reduces the battery discharge current through the converter and prioritizes the system load current if there is any. The IINDPM_STAT and IINDPM_FLAG bits are set to 1 and an $\overline{INT}$ pulse is asserted if the IINDPM_MASK is set to 0. If the battery discharge regulation loop reduces the reverse mode input current to zero and the system load pulls even more current, the charger can no longer limit the battery discharging current.

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The charger can achieve more aggressive transient response in reverse mode via the EN_FAST_VOTG_RESPONSE bit. When EN_FAST_VOTG_RESPONSE=1 the converter achieves a faster transient response; however, the inductance and capacitance recommended operating conditions required are:

Table 6-10. EN_FAST_VOTG_RESPONSE = 1 Inductor and Capacitance Requirements

EN_FAST_VOTG_RESPONSE = 1		MIN	MAX	UNIT
CIN	VIN total capacitance (minimum value after derating)	20		µF
L	Recommended Inductor for f_{SW} ≤ 700kHz	4.7	10	µH
	Recommended Inductor for f_{SW} > 700kHz	2.2	3	µH

To prevent a small IIN_REV load current from depleting the battery while in reverse mode, there is a light load status indication when operating in reverse mode, REV_TERM_STAT. The light load status indication threshold is user controlled via the ITERM register and trips when reverse current through RAC_SNS drops below 2x ITERM. An $\overline{INT}$ pulse is asserted when the threshold is crossed, and the REV_FLAG is set to 1 if REV_MASK = 0. EN_TERM=0 disables the status.

6.3.9.2 Backup Power Supply Mode

By utilizing the charger reverse buck-boost operation, BQ25690 supports the backup power supply mode. In this mode, the charger discharges the energy stored in the battery or the capacitors to hold the VIN voltage for certain amount of time after the adapter is disconnected. The backup mode only can be enabled when VIN is high, by setting EN_BACKUP = 1. When VIN becomes low, the charger resets EN_BACKUP bit to 0.

A comparator is monitoring the VIN voltage. Once the adapter is disconnected, and the VIN drops lower than the VIN_BACKUP threshold, the charger terminates the forward charging mode, forces EN_REV = 1, starts discharging the battery or supercapacitor to regulate the VIN voltage at the VIN_REV register setting. After the charger enters backup mode, the REV_STAT is changed accordingly. At the same time, an $\overline{INT}$ pulse is asserted and the REV_FLAG is set to 1, if REV_MASK = 0.

The comparator threshold monitoring VIN to trigger backup mode is programmed in the VIN_BACKUP register bits, as a ratio of VINDPM values. Only when EN_BACKUP = 1 and VIN drops lower than the threshold, the charger forces EN_REV = 1 to enter the backup mode.

If the charger is running in backup mode, any of the following conditions force the charger to exit the backup operation:

- The battery or the supercapacitor voltage discharges lower than V_{BAT_OKZ}
- The host sets the EN_REV bit from 1 to 0
- Other faults exit reverse mode (refer to Reverse (Source) Mode Operation)
- VIN is above the regulation window during reverse mode of VIN_REV + 6%

While charger is in backup mode, comparators are active on the VIN to check for an adapter reconnection. If VIN is above the regulation window of VIN_REV + 6%, the device automatically exits backup mode and resumes forward charging. For example, if VIN_REV = 15V and converter is operating in backup mode and 20V adapter is plugged in: VIN rises above 15.9V, triggering device to exit backup mode and proceed with normal power up routine normally.

Because VIN is not measured during the re-arming sequence, the VINDPM is not updated. In most applications, the device is expected to support a single adapter so that the previously-set VINDPM value is still accurate. For those applications where different adapter voltages are possible, the user can manually set the VINDPM value.

The battery discharge current is limited during backup mode if IBAT_REV is enabled (Set to 0, 1 or 2). Set IBAT_REV = 0x3 (Disabled) when using backup mode for the best response. Depending on the loading at VIN, additional low ESR capacitance up to 200µF can be necessary to prevent VIN dropping below the VINDPM set point.

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6.3.9.3 Reverse Bypass Mode

The device supports reverse bypass mode to allow VIN = VSYS without regulation and highest efficiency. In reverse bypass mode operating mode, the buck and boost high-side FETs (Q1 and Q4) are both turned on, while the Buck and Boost low-side FETs (Q2 and Q3) remain off. The battery power directly passes through the power stage to the input. The switching losses of MOSFETs and the inductor core loss are eliminated, thereby providing highest efficiency. Enable the reverse bypass mode by setting the EN_REV and EN_BYPASS register bits to 1. Reverse bypass mode requires the R_{AC_SNS} resistor to sense for overcurrent and light-load conditions.

While the device is in reverse bypass mode, the current through R_{AC_SNS} is monitored and compared against the IIN_REV register setting. If the input current exceeds $I_{REV_BYP_OCP}$ (15% above IIN_REV setting) for t_{BYP_OCP}, the device automatically exits bypass mode and returns to PWM regulation mode (switching power stage enabled). The EN_BYPASS bit is cleared back to 0, BYPASS_FLAG bit is set, and an INT pulse is asserted to signal the host if BYPASS_MASK is cleared.

To avoid inrush current false tripping the bypass over-current protection, enter bypass mode when VIN is within 0.5V of VSYS. A typical use case is to first make sure EN_BAT_DETECT = 0, then enable reverse mode (EN_REV = 1), then change the VIN_REV setting to achieve a condition of VIN approximately equal to VSYS, then set EN_BYPASS = 1.

While device is in bypass mode, the system load is prioritized. The BATFET shall remain on if bypass mode is exited due to $I_{REV_BYP_OCP}$.

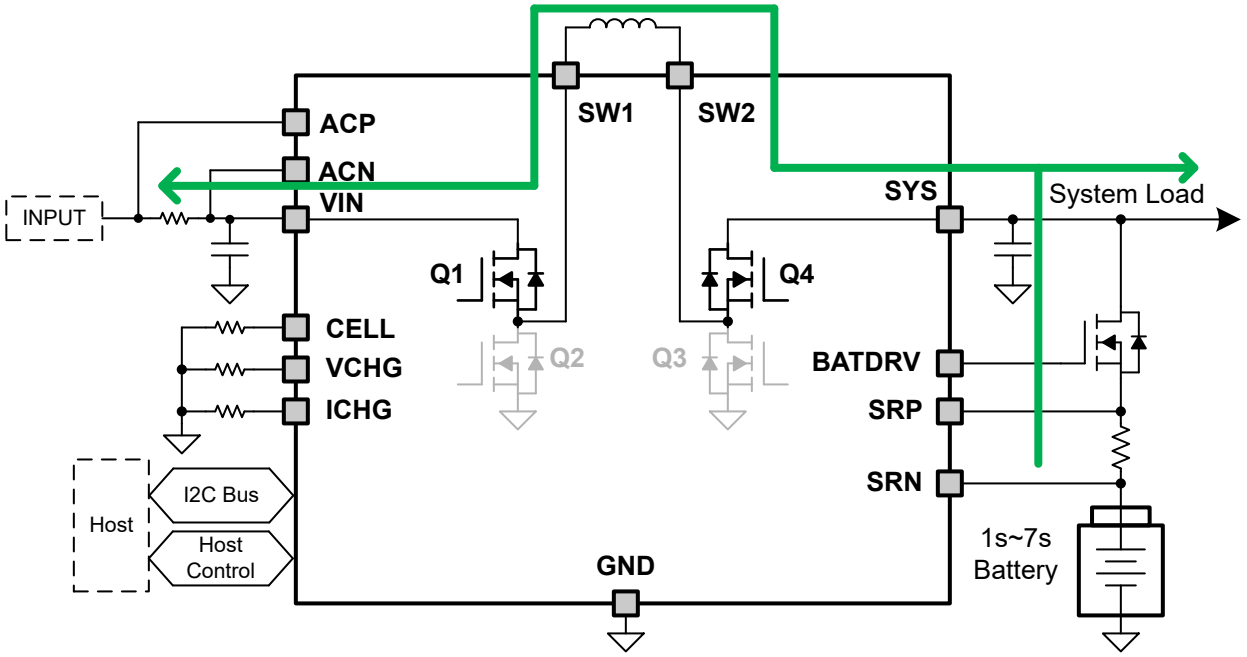


Figure 6-10. Internal Reverse Bypass Mode

In addition to the internal reverse bypass mode, the device offers external reverse bypass mode for highest efficiency with up-to 5A current. In this case, the BYPDRV pin drives external back-to-back MOSFET to connect VIN directly to SYS. The external reverse bypass mode is enabled by setting EN_REV = EN_EXT_BYPASS = EN_BYPASS = 1. If EN_REV = EN_EXT_BYPASS = 1 while EN_BYPASS = 0, then reverse bypass is not entered. The EN_BYPASS bit determines if bypass mode is enabled. EN_EXT_BYPASS determines if external reverse bypass is enabled while EN_REV = EN_BYPASS = 1. Set EN_EXT_BYPASS before or after the device enters bypass mode through EN_BYPASS.

While device is in external reverse bypass mode, the current through R_{AC_SNS} is monitored. If the R_{AC_SNS} current exceeds $I_{REV_EXTBYP_OCP}$ for t_{BYP_OCP}, the device automatically exits external reverse bypass mode and returns to PWM regulation mode (switching power stage enabled). The EN_BYPASS bit is cleared back to 0,

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BYPASS_FLAG bit is set, and an INT pulse is asserted to signal the host if BYPASS_MASK is cleared. Note, the EN_EXT_BYPASS bit is not changed.

To avoid inrush current false tripping the bypass over-current protection, enter reverse bypass mode when VIN is within 0.5V of VSYS. Typical use case is to first make sure EN_BAT_DETECT = 0, then enable reverse mode (EN_REV = 1), then change the VIN_REV setting to achieve a condition of VIN approximately equal to VSYS, then set EN_EXT_BYPASS = EN_BYPASS = 1.

A light-load bypass auto exit feature prevents reverse current direction flow during reverse bypass mode. The charger monitors for the input current dropping below $I_{REV_BYP_LL}$, at which point the charger automatically exits bypass mode and returns to PWM regulation mode. This protection is active during both internal and external bypass modes, but can be disabled by setting EN_BYPASS_LL_EXIT = 0. The EN_BYPASS bit is cleared back to 0, BYPASS_FLAG bit is set, and an INT pulse is asserted to signal the host if BYPASS_MASK is cleared.

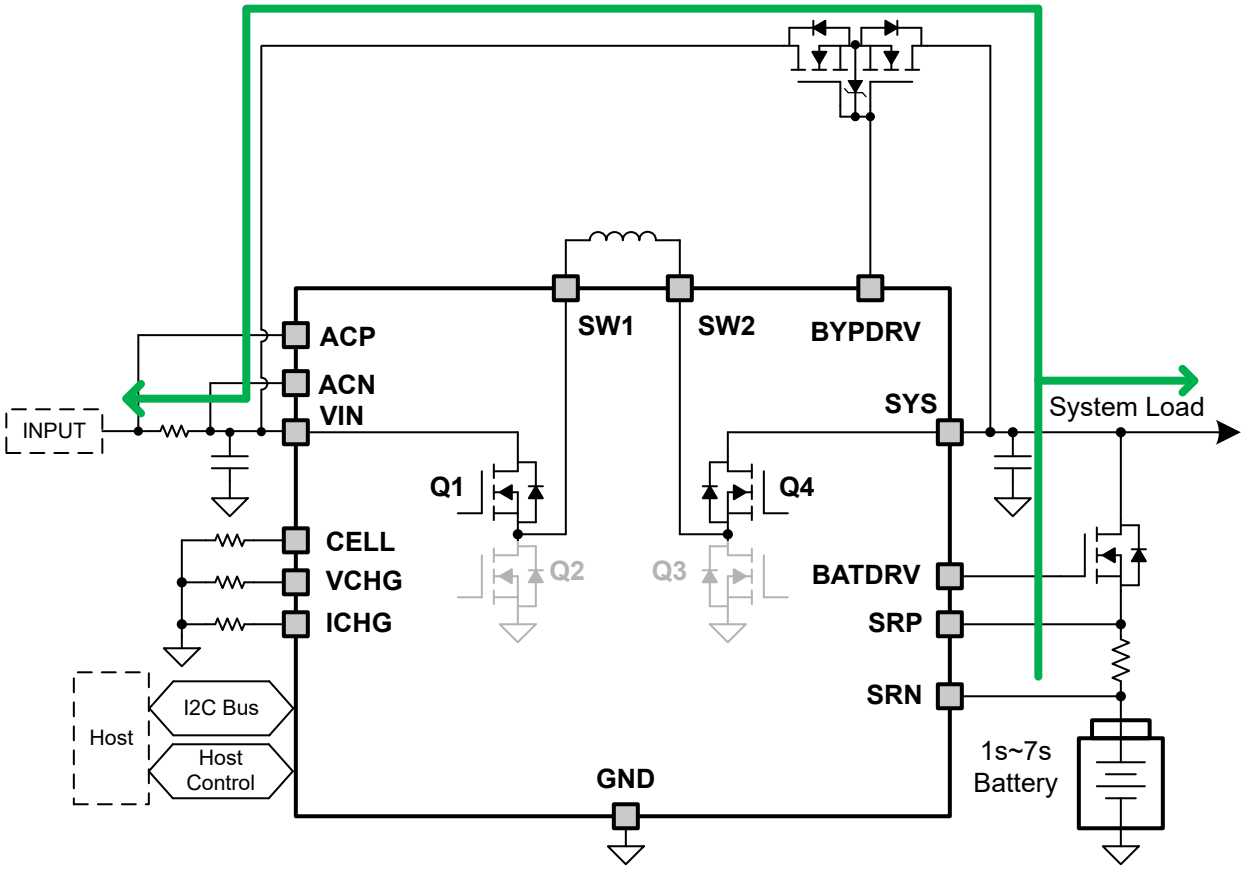


Figure 6-11. External Reverse Bypass Mode

6.3.10 Status Outputs (STAT and $\overline{INT}$)

6.3.10.1 Power Good Indicator (PG_STAT)

The power good status register is set to 1 once a good input source qualifies. The PG_STAT and PG_FLAG change to 1 to indicate a good input source. An $\overline{INT}$ asserts low to alert the host, unless masked by PG_MASK when the following conditions are met:

1. VIN above V_{VIN_UVLOZ}
2. VIN below the V_{VIN_OVP} threshold

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6.3.10.2 Charging Status Indicator (STAT Pin)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. Disable the STAT pin function using the DIS_STAT bit.

Table 6-11. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge and charging in top-off timer)	LOW
Charging complete	HIGH
HIZ mode, charge disable	HIGH
Battery only mode and OTG mode	HIGH
Charge suspend (a fault condition which disable charging)	Blinking at 1Hz

6.3.10.3 Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor charger operation. The $\overline{INT}$ pin notifies the system host on the device operation. By default, the following events generate an active-low, 256µs $\overline{INT}$ pulse.

1. Detection of a good input source
   - V_{VIN} < V_{VIN_OVP} threshold
   - V_{VIN} > V_{VIN_OK} threshold
2. Removal of a good input source
3. Entering IINDPM regulation
4. Entering VINDPM regulation
5. Entering IC junction temperature regulation (TREG)
6. Expiration of a I^2C Watchdog timer
   - At initial power up, $\overline{INT}$ asserts to signal that I^2C is ready for communication
7. Charger status changes state (CHARGE_STAT value change), including Charge Complete
8. TS_STAT changes state (TS_STAT any bit change)
9. Detection of VIN over-voltage (VIN_OVP)
10. Junction temperature shutdown (TSHUT)
11. Detection of battery over-voltage (BATOVP)
12. Expiration of charge safety timer, including trickle charge and pre-charge and fast charge safety timer expired
13. A rising edge on any of the other *_STAT bits

Mask off each one of the $\overline{INT}$ sources to prevent sending out $\overline{INT}$ pulses when the pulses occur. Three bits exist for each one of the pulse events:

- The STAT bit holds the *current status* of each $\overline{INT}$ source.
- The FLAG bit holds information on which source produced an $\overline{INT}$, regardless of the *current status.*
- The MASK bit is used to prevent the device from sending out $\overline{INT}$ for each particular event.

When one of the above conditions occurs (a rising edge on any of the *_STAT bits), the device sends out an $\overline{INT}$ pulse and keeps track of which source generates the $\overline{INT}$ through the FLAG registers. The FLAG register bits automatically reset to zero after being read by the host, and a new edge on STAT bit is required to re-assert the FLAG. This sequence is illustrated in Figure 6-12.

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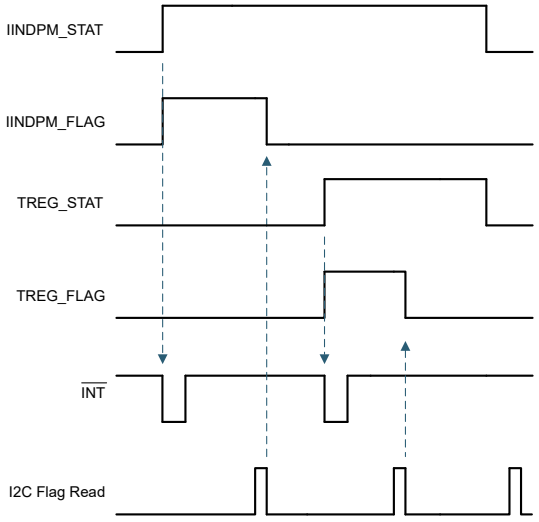


Figure 6-12. INT Generation Behavior Example

6.3.11 Serial Interface

The device uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^{2}C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Consider the devices as controllers or targets when performing data transfers. A controller is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The device operates as a target device with address 0x6A, receiving control inputs from the controller device like a micro-controller or digital signal processor through the registers defined in Register Map. Registers read outside those defined in the map, return 0xFF. The I2C interface supports standard mode (up to 100kbits/s), fast mode (up to 400kbits/s), and fast mode plus (up to 1Mbit/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage using a current source or pull-up resistor.

System Note: All 16-bit registers are defined as Little Endian, with the most-significant byte allocated to the higher address. 16-bit register writes must be done sequentially and programming using the multi-write approach described in Multi-Write and Multi-Read is recommended.

6.3.11.1 Data Validity

Verify that the data on the SDA line is stable during the HIGH period of the clock. The HIGH or LOW state of the data line only changes when the clock signal on SCL line is LOW. One clock pulse generates for each data bit transferred.

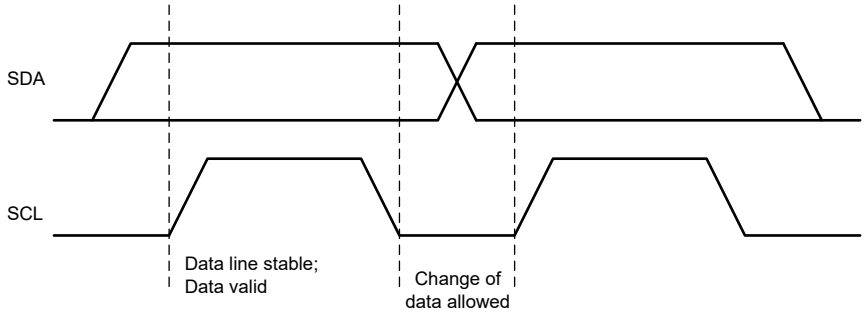


Figure 6-13. Bit Transfers on the I^{2}C Bus

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6.3.11.2 START and STOP Conditions

All transactions begin with a START (S) and terminate with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition. When timeout condition is met, for example START condition is active for more than 2 seconds and there is no STOP condition triggered, the charger I^2C communication automatically resets and communication lines are free for another transmission.

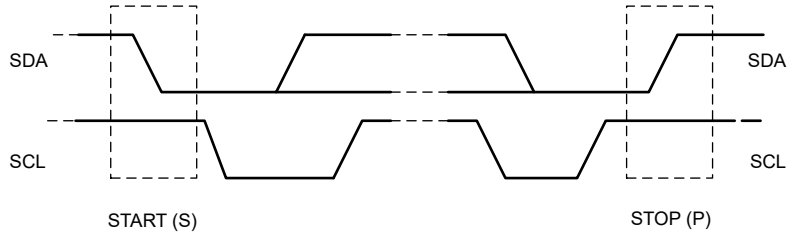


Figure 6-14. START and STOP Conditions on the I^2C Bus

6.3.11.3 Byte Format

Verify that every byte on the SDA line is 8 bits long. The number of bytes transmitted per transfer is unrestricted. An ACKNOWLEDGE (ACK) bit must follow each byte. Data is transferred with the Most Significant Bit (MSB) first. If the target device cannot receive or transmit another complete byte of data until the target device performs some other function, the target device can hold the SCL line low to force the controller into a wait state (clock stretching). Data transfer then continues when the target device is ready for another byte of data and releases the SCL line.

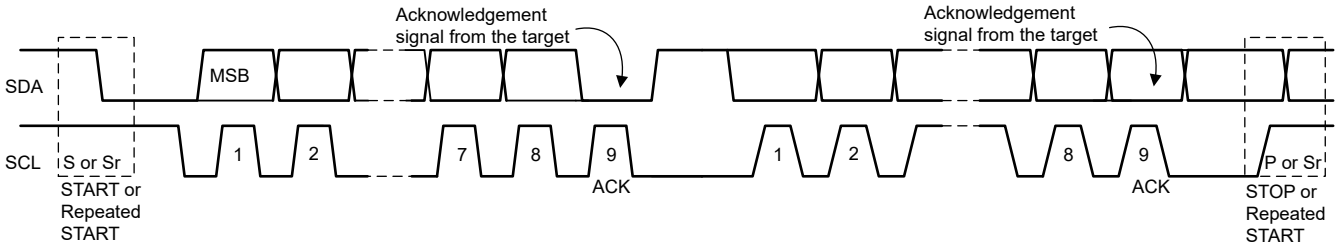


Figure 6-15. Data Transfer on the I^2C Bus

6.3.11.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the receiver to signal the controller that the byte is successfully received and another byte can be sent. The controller generates all clock pulses, including the acknowledge 9th clock pulse.

The controller releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and the line remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK signals when the SDA line remains HIGH during the 9th clock pulse. The controller then generates either a STOP to abort the transfer or a repeated START to start a new transfer.

6.3.11.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 010' (0x6A).

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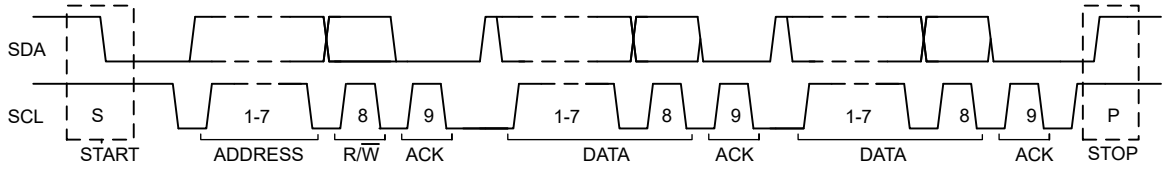


Figure 6-16. Complete Data Transfer on the I²C Bus

6.3.11.6 Single Write and Read

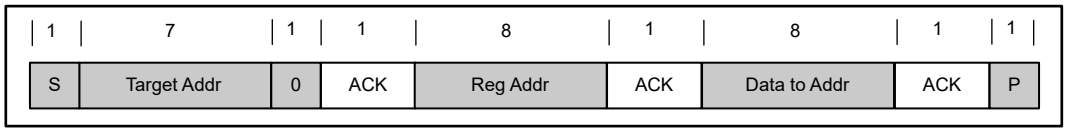


Figure 6-17. Single Write

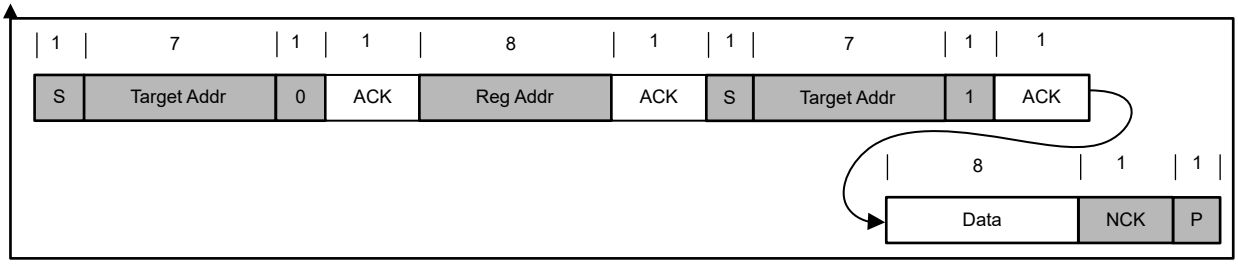
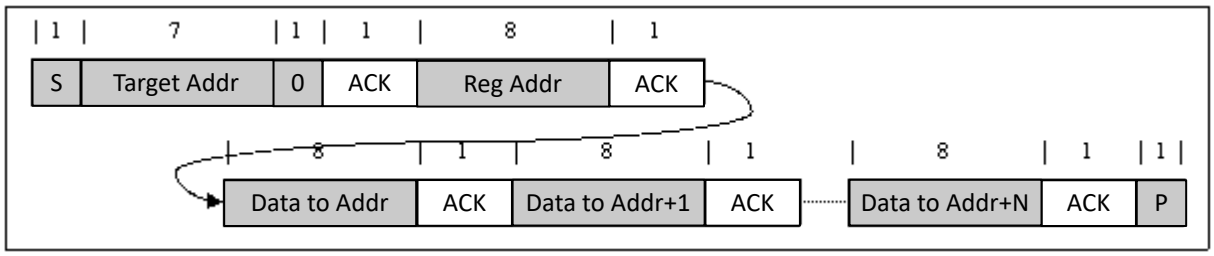


Figure 6-18. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

6.3.11.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers.



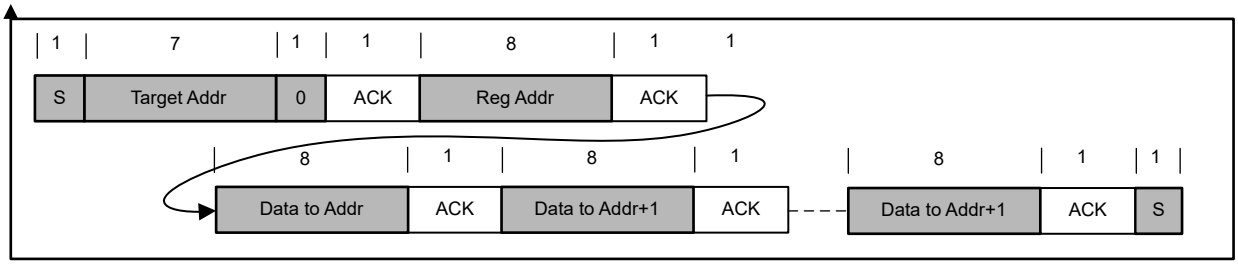


Figure 6-19. Multi-Write

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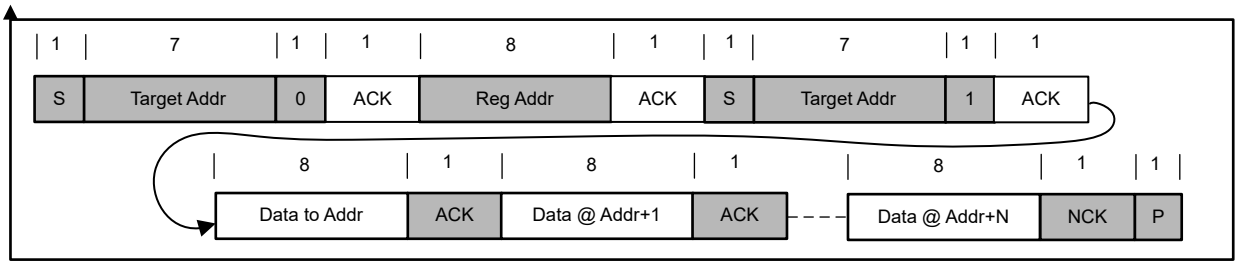


Figure 6-20. Multi-Read

6.4 Device Functional Modes

6.4.1 Host Mode and Default Mode

The device is a host controlled charger, but the device can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit is read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default charging safety timers. At the end of the safety timer expiration, the charging is stopped and the buck-boost converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and all registers are reset to default values except the ones described in the Register Map. The watchdog timer is reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK).

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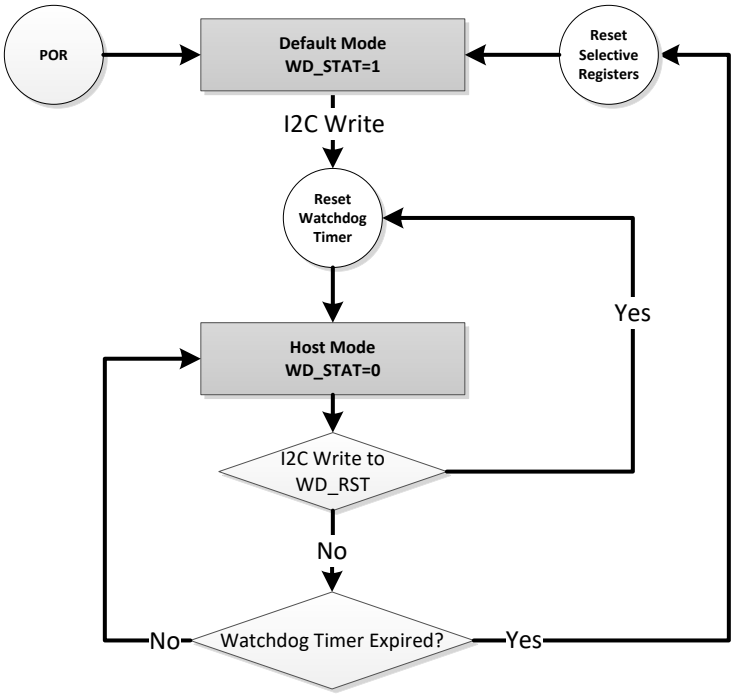


Figure 6-21. Watchdog Timer Flow Chart

6.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer can be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit goes back from 1 to 0 automatically.

The register reset by the REG_RST bit does not initiate the CELL, ICHG and VCHG pin detection, which is only done at the charger first time POR. In addition, if the charger is in the process of forced ICO, set the REG_RST to 1 terminates this process.

6.5 Register Map

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6.5.1 BQ25690 Registers

Table 6-12 lists the memory-mapped registers for the BQ25690 registers. All register offset addresses not listed in Table 6-12 should be considered as reserved locations and the register contents should not be modified.

Table 6-12. BQ25690 Registers

Address	Acronym	Register Name	Section
0x0	REG0x00_Minimal_System_Voltage	Minimal System Voltage	Go
0x2	REG0x02_Charge_Current_Limit	Charge Current Limit	Go
0x4	REG0x04_Charge_Voltage_Limit	Charge Voltage Limit	Go
0x6	REG0x06_Input_Current_Limit	Input Current Limit	Go
0x8	REG0x08_Input_Voltage_Limit	Input Voltage Limit	Go
0xA	REG0x0A_Reverse_Mode_Input_Current_Regulation	Reverse Mode Input Current Regulation	Go
0xC	REG0x0C_Reverse_Mode_Input_Voltage_Regulation	Reverse Mode Input Voltage Regulation	Go
0xE	REG0x0E_Precharge_Control	Precharge Control	Go
0xF	REG0x0F_Termination_Control	Termination Control	Go
0x10	REG0x10_Precharge_and_Termination_Control	Precharge and Termination Control	Go
0x11	REG0x11_Timer_Control	Timer Control	Go
0x12	REG0x12_Charger_Control_1	Charger Control 1	Go
0x13	REG0x13_Charger_Control_2	Charger Control 2	Go
0x14	REG0x14_Charger_Control_3	Charger Control 3	Go
0x15	REG0x15_Charger_Control_4	Charger Control 4	Go
0x16	REG0x16_Converter_Control_1	Converter Control 1	Go
0x17	REG0x17_MPPT_Control	MPPT Control	Go
0x18	REG0x18_TS_Charging_Threshold_Control	TS Charging Threshold Control	Go
0x19	REG0x19_TS_Charging_Behavior_Control	TS Charging Behavior Control	Go
0x1A	REG0x1A_TS_Reverese_Mode_Threshold_Control	TS Reverese Mode Threshold Control	Go
0x1B	REG0x1B_Pin_Detection_Status_1	Pin Detection Status 1	Go
0x1C	REG0x1C_Pin_Detection_Status_2	Pin Detection Status 2	Go
0x1D	REG0x1D_Charger_Status_1	Charger Status 1	Go
0x1E	REG0x1E_Charger_Status_2	Charger Status 2	Go
0x1F	REG0x1F_FAULT_Status	FAULT Status	Go
0x20	REG0x20_Charger_Flag	Charger Flag	Go
0x21	REG0x21_FAULT_Flag	FAULT Flag	Go
0x22	REG0x22_Charger_Mask	Charger Mask	Go
0x23	REG0x23_FAULT_Mask	FAULT Mask	Go
0x24	REG0x24_ICO_Current_Limit	ICO Current Limit	Go
0x26	REG0x26_Part_Information	Part Information	Go

Complex bit access types are encoded to fit into small table cells. Table 6-13 shows the codes that are used for access types in this section.

Table 6-13. BQ25690 Access Type Codes

Access Type	Code	Description
Read Type		

Table 6-13. BQ25690 Access Type Codes (continued)

Access Type	Code	Description
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.5.1.1 REG0x00_Minimal_System_Voltage Register (Address = 0x0) [Reset = 0xXXX0]

REG0x00_Minimal_System_Voltage is shown in Table 6-14.

Return to the Summary Table.

Table 6-14. REG0x00_Minimal_System_Voltage Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15	RESERVED	R	0x0		Reserved
14:4	VSYSMIN	R/W	X	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Minimal system voltage: After POR, the device reads the resistance on CELL pin to set the default VSYSMIN value: 1s: 3.5V 2s ~ 7s: 3.1V/cell Range: 3000mV-28000mV (96h-578h) Clamped Low Clamped High Bit Step: 20mV
3:0	RESERVED	R	0x0		Reserved

6.5.1.2 REG0x02_Charge_Current_Limit Register (Address = 0x2) [Reset = 0x0XX0]

REG0x02_Charge_Current_Limit is shown in Table 6-15.

Return to the Summary Table.

Table 6-15. REG0x02_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:4	ICHG	R/W	X	This 16-bit register follows the little-endian convention. Reset by: REG_RESET	Charge current regulation limit: After POR, the device reads the resistance on ICHG pin to set the maximum ICHG clamp: Range: 40mA-3300mA (2h-A5h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

6.5.1.3 REG0x04_Charge_Voltage_Limit Register (Address = 0x4) [Reset = 0xXXXX]

REG0x04_Charge_Voltage_Limit is shown in Table 6-16.

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Table 6-16. REG0x04_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15	RESERVED	R	0x0		Reserved
14:3	VREG	R/W	X	This 16-bit register follows the little-endian convention. VREG is clamped based on CELL_PIN register value Reset by: REG_RESET	Battery voltage regulation limit: After POR, the device reads the resistance on CELL and VCHG pins to set the maximum VREG clamp: Range: 2400mV-33000mV (F0h-CE4h) Clamped Low Clamped High Bit Step: 10mV
2:0	RESERVED	R	0x0		Reserved

6.5.1.4 REG0x06_Input_Current_Limit Register (Address = 0x6) [Reset = 0x0A50]

REG0x06_Input_Current_Limit is shown in Table 6-17.

Return to the Summary Table.

Table 6-17. REG0x06_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:4	IINDPM	R/W	0xA5	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Input current regulation limit: POR: 3300mA (A5h) Range: 40mA-3300mA (2h-A5h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

6.5.1.5 REG0x08_Input_Voltage_Limit Register (Address = 0x8) [Reset = 0x0910]

REG0x08_Input_Voltage_Limit is shown in Table 6-18.

Return to the Summary Table.

Table 6-18. REG0x08_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15	RESERVED	R	0x0		Reserved
14:4	VINDPM	R/W	0x91	This 16-bit register follows the little-endian convention	Absolute input voltage regulation limit: POR: 2900mV (91h) Range: 2500mV-34000mV (7Dh-6A4h) Clamped Low Clamped High Bit Step: 20mV
3:0	RESERVED	R	0x0		Reserved

6.5.1.6 REG0x0A_Reverse_Mode_Input_Current_Regulation Register (Address = 0xA) [Reset = 0x0A50]

REG0x0A_Reverse_Mode_Input_Current_Regulation is shown in Table 6-19.

Return to the Summary Table.

Table 6-19. REG0x0A_Reverse_Mode_Input_Current_Regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved

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Table 6-19. REG0x0A_Reverse_Mode_Input_Current_Regulation Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
11:4	IIN_REV	R/W	0xA5	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Reverse mode current regulation across ACP/ACN: POR: 3300mA (A5h) Range: 40mA-3300mA (2h-A5h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

6.5.1.7 REG0x0C_Reverse_Mode_Input_Voltage_Regulation Register (Address = 0xC) [Reset = 0x0FA0]

REG0x0C_Reverse_Mode_Input_Voltage_Regulation is shown in Table 6-20.

Return to the Summary Table.

Table 6-20. REG0x0C_Reverse_Mode_Input_Voltage_Regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15	RESERVED	R	0x0		Reserved
14:4	VIN_REV	R/W	0xFA	This 16-bit register follows the little-endian convention Reset by: REG_RESET	Reverse mode voltage regulation at VIN: POR: 5000mV (FAh) Range: 3500mV-34000mV (AFh-6A4h) Clamped Low Clamped High Bit Step: 20mV
3:0	RESERVED	R	0x0		Reserved

6.5.1.8 REG0x0E_Precharge_Control Register (Address = 0xE) [Reset = 0x05]

REG0x0E_Precharge_Control is shown in Table 6-21.

Return to the Summary Table.

Table 6-21. REG0x0E_Precharge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved
5:0	IPRECHG	R/W	0x5	Note: 20mA setting only recommended when using 10mOhm RBAT_SNS Reset by: REG_RESET	Pre-charge current regulation limit: POR: 100mA (5h) Range: 20mA-620mA (1h-1Fh) Clamped Low Clamped High Bit Step: 20mA

6.5.1.9 REG0x0F_Termination_Control Register (Address = 0xF) [Reset = 0x05]

REG0x0F_Termination_Control is shown in Table 6-22.

Return to the Summary Table.

Table 6-22. REG0x0F_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved

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Table 6-22. REG0x0F_Termination_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
5:0	ITERM	R/W	0x5	Note: 20mA setting only recommended when using 10mOhm RBAT_SNS Reset by: REG_RESET	Termination current threshold: POR: 100mA (5h) Range: 20mA-620mA (1h-1Fh) Clamped Low Clamped High Bit Step: 20mA

6.5.1.10 REG0x10_Precharge_and_Termination_Control Register (Address = 0x10) [Reset = 0x2F]

REG0x10_Precharge_and_Termination_Control is shown in Table 6-23.

Return to the Summary Table.

Table 6-23. REG0x10_Precharge_and_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0x0	Reset by: REG_RESET	Reset registers to default values and reset timer Bit resets to 0 after reset completes. 0b = Not reset 1b = Reset
6	DIS_STAT	R/W	0x0	Reset by: REG_RESET	Disable the STAT pin output: 0b = Enable 1b = Disable
5:4	VRECHG	R/W	0x2	Reset by: REG_RESET	Battery auto-recharge threshold, as percentage of VREG: 00b = 92.7% x VREG (~260mV/cell for LiFePO4) 01b = 94.1% x VREG (~210mV/cell for LiFePO4) 10b = 95.5% x VREG (~190mV/cell for LiIon) 11b = 97% x VREG (~130mV/cell for LiIon)
3	EN_TERM	R/W	0x1	Reset by: REG_RESET	Termination control: 0b = Disable 1b = Enable
2:1	VBAT_LOWV	R/W	0x3	Reset by: REG_RESET	Battery threshold for precharge to fast charge transition, as percentage of VREG: 00b = 30% x VREG 01b = 55% x VREG 10b = 66.7% x VREG 11b = 71.4% x VREG
0	EN_PRECHG	R/W	0x1	Reset by: REG_RESET	Enable precharge and BAT_SHORT functions: 0b = Disable 1b = Enable

6.5.1.11 REG0x11_Timer_Control Register (Address = 0x11) [Reset = 0x1D]

REG0x11_Timer_Control is shown in Table 6-24.

Return to the Summary Table.

Table 6-24. REG0x11_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TOPOFF_TMR	R/W	0x0	Reset by: REG_RESET	Top-off timer control: 00b = Disable 01b = 15 mins 10b = 30 mins 11b = 45 mins

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Table 6-24. REG0x11_Timer_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
5:4	WATCHDOG	R/W	0x1	Reset by: REG_RESET	Watchdog timer setting: 00b = Disable 01b = 40s 10b = 80s 11b = 160s
3	EN_CHG_TMR	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable precharge and fast charge safety timers: 0b = Disable 1b = Enable
2:1	CHG_TMR	R/W	0x2	Reset by: REG_RESET	Fast charge safety timer setting: 00b = 5hr 01b = 8hr 10b = 12hr 11b = 24hr
0	EN_TMR2X	R/W	0x1	Reset by: REG_RESET	Enable 2x mode for charging safety timer: 0b = Safety timers NOT slowed by 2x during input DPM or thermal regulation 1b = Safety timers slowed by 2x during input DPM or thermal regulation

6.5.1.12 REG0x12_Charger_Control_1 Register (Address = 0x12) [Reset = 0x80]

REG0x12_Charger_Control_1 is shown in Table 6-25.

Return to the Summary Table.

Table 6-25. REG0x12_Charger_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	IBAT_REV	R/W	0x2	Reset by: REG_RESET	Reverse mode Battery discharging current regulation across SRP/SRN: 00b = 1A 01b = 2.28A 10b = 3.56A 11b = Disable
5	RBAT_SNS	R/W	0x0	Reset by: REG_RESET	Battery current sense resistor value: 0b = 10mOhm 1b = 5mOhm
4	EN_BYPASS	R/W	0x0	If EN_EXT_BYPASS = 1, this bit controls the external bypass path. If EN_EXT_BYPASS = 0, this bit enables the internal bypass path. This bit is cleared when EN_HIZ goes to 1 or when EN_REV goes to 0. Reset by: REG_RESET WATCHDOG	Bypass mode control: 0b = Disable 1b = Enable
3	EN_EXT_BYPASS	R/W	0x0	Reset by: REG_RESET	External bypass mode control: 0b = Disable 1b = Enable
2	WD_RST	R/W	0x0	Reset by: REG_RESET WATCHDOG	I2C Watchdog timer reset: 0b = Normal 1b = Reset (this bit goes back to 0 after timer resets)

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Table 6-25. REG0x12_Charger_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1	STOP_WD_CHG	R/W	0x0		Defines whether a WD timer expiration disables charging: 0b = WD timer expiration keeps existing EN_CHG setting 1b = WD timer expiration sets EN_CHG = 0
0	PRECHG_TMR	R/W	0x0	Reset by: REG_RESET	Precharge safety timer setting: 0b = 2hrs 1b = 0.5hrs

6.5.1.13 REG0x13_Charger_Control_2 Register (Address = 0x13) [Reset = 0xA0]

REG0x13_Charger_Control_2 is shown in Table 6-26.

Return to the Summary Table.

Table 6-26. REG0x13_Charger_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_AUTO_DSCHG	R/W	0x1	Reset by: REG_RESET	Enable the auto discharge during OVP - ISYS_LOAD during forward mode OVP and IVIN_LOAD during reverse mode OVP faults: 0b = Charger will NOT apply discharging ISYS_LOAD nor IVIN_LOAD current during converter OVP 1b = Charger will apply discharging ISYS_LOAD or IVIN_LOAD current during converter OVP
6	FORCE_ISYS_DSCHG	R/W	0x0	Reset by: REG_RESET WATCHDOG	Force a system discharging current (ISYS_LOAD): 0b = Disable 1b = Enable ISYS_LOAD
5	EN_CHG	R/W	0x1	Reset by: REG_RESET WATCHDOG	Charge enable control: 0b = Disable charge 1b = Enable charge
4	EN_HIZ	R/W	0x0	Reset by: REG_RESET WATCHDOG Adapter Plug In	Enable HIZ mode: 0b = Disable HIZ 1b = Enable HIZ
3	FORCE_VIN_DSCHG	R/W	0x0	Reset by: REG_RESET WATCHDOG	Force an input discharging current (IVIN_LOAD): 0b = Disable 1b = Enable IVIN_LOAD
2	RAC_SNS	R/W	0x0	Reset by: REG_RESET	Input current sense resistor value: 0b = 10mOhm 1b = 5mOhm
1	EN_REV	R/W	0x0	Reset by: REG_RESET WATCHDOG	Enabling reverse mode must be done after disabling EN_BAT_DETECT (Reg0x14[3]=0) Reverse mode control: 0b = Disable 1b = Enable
0	EN_BACKUP	R/W	0x0	This bit can only be enabled when a valid input source is present; ignored in battery-only mode Reset by: REG_RESET WATCHDOG	Backup mode control: 0b = Disable 1b = Enable

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6.5.1.14 REG0x14_Charger_Control_3 Register (Address = 0x14) [Reset = 0x28]

REG0x14_Charger_Control_3 is shown in Table 6-27.

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Table 6-27. REG0x14_Charger_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	VIN_BACKUP	R/W	0x0	Reset by: REG_RESET	VIN falling threshold to trigger backup mode, defined as ratio of VINDPM 00b = 50% x VINDPM 01b = 60% x VINDPM 10b = 80% x VINDPM 11b = 100% x VINDPM
5	EN_EXTILIM	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable external ILIM_HIZ pin for input current regulation: 0b = Disable 1b = Enable
4	BATFET_CTRL	R/W	0x0	Reset by: REG_RESET WATCHDOG	Force BATFET turn off: 0b = Disable (BATFET can turn on) 1b = Enable (BATFET forced off)
3	EN_BAT_DETECT	R/W	0x1	Reset by: REG_RESET	Enabling battery detection can only be done if reverse mode is disabled (Reg0x13[1]=0) Enable Battery Detection Routine: 0b = Disable (no battery detection) 1b = Enable
2	FORCE_VINDPM	R/W	0x0	Reset by: REG_RESET WATCHDOG	VINDPM threshold setting method: 0b = Run relative VINDPM threshold 1b = Run absolute VINDPM threshold
1	FORCE_ICO	R/W	0x0	Reset by: REG_RESET	Force Start Input Current Optimizer (ICO): Note: This bit can only be set and always returns to 0 after ICO starts. This bit is only valid when EN_ICO = 1 0b = Do not force ICO 1b = Force ICO start
0	EN_ICO	R/W	0x0	Reset by: REG_RESET	Input Current Optimizer (ICO) control: 0b = Disable 1b = Enable

6.5.1.15 REG0x15_Charger_Control_4 Register (Address = 0x15) [Reset = 0x00]

REG0x15_Charger_Control_4 is shown in Table 6-28.

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Table 6-28. REG0x15_Charger_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:4	RESERVED	R	0x0		Reserved
3	EN_FAST_VOTG_RESPONSE	R/W	0x0	See Reverse (Source) Mode Operation section for constraints Reset by: REG_RESET	Faster reverse (source) (OTG) transient response: 0b = Disable 1b = Enable
2	RESERVED	R	0x0		Reserved

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Table 6-28. REG0x15_Charger_Control_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1:0	VBAT_DETECT	R/W	0x0	Reset by: REG_RESET	Battery detection high regulation setpoint, voltage per cell: 00b = 2.8 01b = 3 10b = 3.1 11b = 3.3

6.5.1.16 REG0x16_Converter_Control_1 Register (Address = 0x16) [Reset = 0xE1]

REG0x16_Converter_Control_1 is shown in Table 6-29.

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Table 6-29. REG0x16_Converter_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_PFM	R/W	0x1	Reset by: REG_RESET	Enable PFM mode: 0b = Disable 1b = Enable
6	EN_PFM_OOA	R/W	0x1	Only valid if EN_PFM = 1 Reset by: REG_RESET	Enable PFM Out Of Audio (OOA) mode: 0b = Disable 1b = Enable
5	TREG	R/W	0x1	Reset by: REG_RESET	Thermal regulation limit: 0b = 80°C 1b = 120°C
4:3	EN_DITHER	R/W	0x0	Reset by: REG_RESET	Switching frequency dithering configuration: 00b = Disable 01b = 1X 10b = 2X 11b = 3X
2:0	FSW	R/W	0x1	Reset by: REG_RESET	Switching frequency configuration: 001b = 450kHz 010b = 500kHz 011b = 550kHz 100b = 600kHz 101b = 700kHz 110b = 1.2MHz

6.5.1.17 REG0x17_MPPT_Control Register (Address = 0x17) [Reset = 0xAA]

REG0x17_MPPT_Control is shown in Table 6-30.

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Table 6-30. REG0x17_MPPT_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:5	VOC_PCT	R/W	0x5	Reset by: REG_RESET	Sets the input operating voltage (VINDPM), as percentage of open-circuit voltage (VOC): 000b = 62.5% x VOC 001b = 68.75% x VOC 010b = 75% x VOC 011b = 78.125% x VOC 100b = 81.25% x VOC 101b = 84.375% x VOC 110b = 87.5% x VOC 111b = 93.75% x VOC

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Table 6-30. REG0x17_MPPT_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
4:3	VOC_DLY	R/W	0x1	Reset by: REG_RESET	Time delay before making VOC measurement after converter stops: 00b = 50ms 01b = 300ms 10b = 2s 11b = 5s
2:1	VOC_RATE	R/W	0x1	Reset by: REG_RESET	Time interval between two VOC measurements: 00b = 30s 01b = 2min 10b = 10min 11b = 30min
0	EN_MPPT	R/W	0x0	Reset by: REG_RESET	Enable MPPT routine: 0b = Disable 1b = Enable

6.5.1.18 REG0x18_TS_Charging_Threshold_Control Register (Address = 0x18) [Reset = 0x95]

REG0x18_TS_Charging_Threshold_Control is shown in Table 6-31.

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Table 6-31. REG0x18_TS_Charging_Threshold_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_TH5	R/W	0x2	Using 103AT NTC thermistor with RT1=5.36kOhm and RT2=41.2kOhm Reset by: REG_RESET	TS TH5 (HOT) threshold control: 00b = 41.2% (50°C) 01b = 37.7% (55°C) 10b = 34.375% (60°C) 11b = 31.25% (65°C)
5:4	TS_TH3	R/W	0x1	Using 103AT NTC thermistor with RT1=5.36kOhm and RT2=41.2kOhm Reset by: REG_RESET	TS TH3 (WARM) threshold control: 00b = 48.4% (40°C) 01b = 44.75% (45°C) 10b = 41.2% (50°C) 11b = 37.7% (55°C)
3:2	TS_TH2	R/W	0x1	Using 103AT NTC thermistor with RT1=5.36kOhm and RT2=41.2kOhm Reset by: REG_RESET	TS TH2 (COOL) threshold control: 00b = 70.9% (5°C) 01b = 68.25% (10°C) 10b = 65.35% (15°C) 11b = 62.25% (20°C)
1:0	TS_TH1	R/W	0x1	Using 103AT NTC thermistor with RT1=5.36kOhm and RT2=41.2kOhm Reset by: REG_RESET	TS TH1 (COLD) threshold control: 00b = 77.15% (-10°C) 01b = 75.32% (-5°C) 10b = 73.3% (0°C) 11b = 70.9% (5°C)

6.5.1.19 REG0x19_TS_Charging_Behavior_Control Register (Address = 0x19) [Reset = 0xD7]

REG0x19_TS_Charging_Behavior_Control is shown in Table 6-32.

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Table 6-32. REG0x19_TS_Charging_Behavior_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_BYPASS_LL_EXIT	R/W	0x1		Enable auto exit bypass mode when light-load is detected: 0b = Disabled 1b = Enabled
6:5	JEITA_VSET	R/W	0x2	Reset by: REG_RESET	JEITA Warm (T3 < TS < T5) battery voltage regulation setting: 00b = Charge Suspend 01b = VREG - 250mV/cell 10b = VREG - 100mV/cell 11b = VREG
4	JEITA_ISETH	R/W	0x1	Reset by: REG_RESET	JEITA Warm (T3 < TS < T5) battery current regulation setting, as percentage of ICHG: 0b = 40% x ICHG 1b = 100% x ICHG
3:2	JEITA_ISETC	R/W	0x1	Reset by: REG_RESET	JEITA Cool (T1 < TS < T2) battery current regulation setting, as percentage of ICHG: 00b = Charge Suspend 01b = 20% x ICHG 10b = 40% x ICHG 11b = 100% x ICHG
1	EN_JEITA	R/W	0x1	Reset by: REG_RESET	JEITA profile control: 0b = Disable JEITA (COLD/HOT control only) 1b = Enable JEITA (COLD/COOL/WARM/HOT control)
0	EN_TS	R/W	0x1	Reset by: REG_RESET	TS pin function control (applies to forward charging and reverse discharging modes): 0b = Disable (ignore TS pin) 1b = Enable

6.5.1.20 REG0x1A_TS_Reverese_Mode_Threshold_Control Register (Address = 0x1A) [Reset = 0x40]

REG0x1A_TS_Reverese_Mode_Threshold_Control is shown in Table 6-33.

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Table 6-33. REG0x1A_TS_Reverese_Mode_Threshold_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_REV_HOT	R/W	0x1	Reset by: REG_RESET	Reverse Mode TS HOT temperature threshold control: 00b = 37.7% (55°C) 01b = 34.2% (60°C) 10b = 31.25%(65°C) 11b = Disable
5	TS_REV_COLD	R/W	0x0	Reset by: REG_RESET	Reverse Mode TS COLD temperature threshold control: 0b = 77.15% (-10°C) 1b = 80% (-20°C)
4	RESERVED	R	0x0		Reserved
3:0	CV_TMR	R/W	0x0	Reset by: REG_RESET	CV timer setting: 0000b = disable 0001b = 1hr 0010b = 2hr ... = ... 1110b = 14hr 1111b = 15hr

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6.5.1.21 REG0x1B_Pin_Detection_Status_1 Register (Address = 0x1B) [Reset = 0x00]

REG0x1B_Pin_Detection_Status_1 is shown in Table 6-34.

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Table 6-34. REG0x1B_Pin_Detection_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VCHG_PIN_OVERRIDE	R/W	0x0	Reset by: REG_RESET WATCHDOG	Enable VCHG register to exceed clamp value from VCHG pin detection: 0b = Disable 1b = Enable
6	CELL_PIN_OVERRIDE	R/W	0x0	Reset by: REG_RESET WATCHDOG	Enable host to write to CELL_PIN register: 0b = Disable 1b = Enable
5:3	VCHG_PIN	R	0x0	Use VCHG_PIN_OVERRIDE to program VREG above the value detected by VCHG pin	VCHG pin detection result: 000b = Fault 001b = 3.5V/cell 010b = 3.6V/cell 011b = 4V/cell 100b = 4.1V/cell 101b = 4.2V/cell 110b = 4.3V/cell 111b = 4.35V/cell
2:0	CELL_PIN	R/W	0x0	Must change this register before changing VREG, VSYSMIN regulation targets	CELL pin detection result: 000b = Fault 001b = 1s 010b = 2s 011b = 3s 100b = 4s 101b = 5s 110b = 6s 111b = 7s

6.5.1.22 REG0x1C_Pin_Detection_Status_2 Register (Address = 0x1C) [Reset = 0x00]

REG0x1C_Pin_Detection_Status_2 is shown in Table 6-35.

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Table 6-35. REG0x1C_Pin_Detection_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:4	RESERVED	R	0x0		Reserved
3	ICHG_PIN_OVERRIDE	R/W	0x0	Reset by: REG_RESET WATCHDOG	Enable ICHG register to exceed clamp value from ICHG_PIN detection: 0b = Disable 1b = Enable
2:0	ICHG_PIN	R	0x0	Use ICHG_PIN_OVERRIDE to program ICHG above the value detected by ICHG pin	ICHG pin detection resulting ICHG register clamp: 000b = Fault 001b = 0.1A 010b = 0.5A 011b = 1A 100b = 1.5A 101b = 2A 110b = 2.5A 111b = 3.3A

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6.5.1.23 REG0x1D_Charger_Status_1 Register (Address = 0x1D) [Reset = 0x08]

REG0x1D_Charger_Status_1 is shown in Table 6-36.

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Table 6-36. REG0x1D_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_STAT	R	0x0		Input Power Good status: 0b = Not Power Good 1b = Power Good
6	IINDPM_STAT	R	0x0		Input current regulation status in forward mode or Battery current regulation status in reverse mode: 0b = Normal 1b = Device in current regulation
5	VINDPM_STAT	R	0x0		Input voltage regulation status (forward mode): 0b = Normal 1b = Device in input voltage regulation
4	TREG_STAT	R	0x0		IC Thermal regulation status (forward or reverse mode): 0b = Normal 1b = Device in thermal regulation
3	WD_STAT	R	0x1		I2C watch dog timer status: 0b = Normal 1b = WD timer expired
2:0	CHARGE_STAT	R	0x0		Charge cycle status: 000b = Not charging 001b = Trickle Charge (VBAT < VBAT_SHORT) 010b = Pre-Charge (VBAT < VBAT_LOWV) 011b = Fast Charge (CC mode) 100b = Taper Charge (CV mode) 101b = Reserved 110b = Top-off Timer Charge 111b = Charge Termination Done

6.5.1.24 REG0x1E_Charger_Status_2 Register (Address = 0x1E) [Reset = 0x00]

REG0x1E_Charger_Status_2 is shown in Table 6-37.

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Table 6-37. REG0x1E_Charger_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6:5	ICO_STAT	R	0x0		Input Current Optimizer (ICO) Status: 00b = ICO Disabled 01b = ICO Optimization in Progress 10b = Maximum input current detected 11b = ICO Routine Suspended
4:3	REV_STAT	R	0x0		Reverse Mode status: 00b = Reverse Mode Disabled 01b = Reverse Mode CV 10b = Reverse Mode CC 11b = Reverse Mode Fault

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Table 6-37. REG0x1E_Charger_Status_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
2:0	TS_STAT	R	0x0		TS (battery NTC) status: 000b = Normal 001b = TS Cold (forward or reverse mode) 010b = TS Hot (forward or reverse mode) 011b = TS Cool (forward mode) 100b = TS Warm (forward mode)

6.5.1.25 REG0x1F_FAULT_Status Register (Address = 0x1F) [Reset = 0x00]

REG0x1F_FAULT_Status is shown in Table 6-38.

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Table 6-38. REG0x1F_FAULT_Status Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VIN_OVP_STAT	R	0x0		VIN over-voltage status: 0b = Normal 1b = Device in input over voltage protection
6:5	BAT_FAULT_STAT	R	0x0		Battery fault status: 00b = Normal 01b = Battery missing 10b = Over-voltage battery detected 11b = Dead battery detected
4	CHG_TMR_STAT	R	0x0		Charge safety timer status: 0b = Normal 1b = Charge safety timer expired
3	CV_TMR_STAT	R	0x0		CV timer status: 0b = Normal 1b = CV Timer Expired
2	TSHUT_STAT	R	0x0		IC temperature shutdown status: 0b = Normal 1b = Device in thermal shutdown protection
1	RESERVED	R	0x0		Reserved
0	REV_TERM_STAT	R	0x0		Reverse mode termination status: 0b = Reverse mode current is greater than 2x ITERM 1b = Reverse mode current is less than or equal to 2x ITERM

6.5.1.26 REG0x20_Charger_Flag Register (Address = 0x20) [Reset = 0x08]

REG0x20_Charger_Flag is shown in Table 6-39.

Return to the Summary Table.

Table 6-39. REG0x20_Charger_Flag Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_FLAG	R	0x0		Input Power Good flag: Access: R (ClearOnRead) 0b = Normal 1b = PG status changed

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Table 6-39. REG0x20_Charger_Flag Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
6	IINDPM_FLAG	R	0x0		Input current regulation flag in forward mode or Battery current regulation flag in reverse mode: Access: R (ClearOnRead) 0b = Normal 1b = Device entered current regulation
5	VINDPM_FLAG	R	0x0		Input voltage regulation flag (forward mode): Access: R (ClearOnRead) 0b = Normal 1b = Device entered input voltage regulation
4	TREG_FLAG	R	0x0		IC Thermal regulation flag (forward or reverse mode): Access: R (ClearOnRead) 0b = Normal 1b = Device entered thermal regulation
3	WD_FLAG	R	0x1		I2C watchdog timer flag: Access: R (ClearOnRead) 0b = Normal 1b = WD timer signal rising edge detected
2	ICO_FLAG	R	0x0		Input Current Optimizer (ICO) flag: Access: R (ClearOnRead) 0b = Normal 1b = ICO_STAT changed (transition to any state)
1	TS_FLAG	R	0x0		TS (battery NTC) flag: Access: R (ClearOnRead) 0b = Normal 1b = TS_STAT changed (transitioned to any state)
0	CHARGE_FLAG	R	0x0		Charge cycle flag: Access: R (ClearOnRead) 0b = Normal 1b = CHARGE_STAT changed (transition to any state)

6.5.1.27 REG0x21_FAULT_Flag Register (Address = 0x21) [Reset = 0x00]

REG0x21_FAULT_Flag is shown in Table 6-40.

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Table 6-40. REG0x21_FAULT_Flag Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VIN_OVP_FLAG	R	0x0		VIN over-voltage flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered VIN OVP
6	BAT_FAULT_FLAG	R	0x0		Battery fault flag: Access: R (ClearOnRead) 0b = Normal 1b = BAT_FAULT_STAT changed (transition to any state)
5	CHG_TMR_FLAG	R	0x0	Applies to both fast charge and pre-charge safety timers	Charge safety timer flag: Access: R (ClearOnRead) 0b = Normal 1b = Charge Safety timer expired rising edge detected

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Table 6-40. REG0x21_FAULT_Flag Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
4	CV_TMR_FLAG	R	0x0		CV timer flag: Access: R (ClearOnRead) 0b = Normal 1b = CV timer expired rising edge detected
3	TSHUT_FLAG	R	0x0		IC thermal shutdown flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered thermal shutdown protection
2	BYPASS_FLAG	R	0x0		Bypass mode fault flag: Access: R (ClearOnRead) 0b = Normal 1b = Bypass exit due to fault
1	RESERVED	R	0x0		Reserved
0	REV_FLAG	R	0x0		Reverse Mode flag: Access: R (ClearOnRead) 0b = Normal 1b = REV_STAT changed (transitioned to any state)

6.5.1.28 REG0x22_Charger_Mask Register (Address = 0x22) [Reset = 0x00]

REG0x22_Charger_Mask is shown in Table 6-41.

Return to the Summary Table.

Table 6-41. REG0x22_Charger_Mask Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_MASK	R/W	0x0	Reset by: REG_RESET	Input Power Good mask: 0b = PG toggle produces INT pulse 1b = PG toggle does not produce INT pulse
6	IINDPM_MASK	R/W	0x0	Reset by: REG_RESET	Input current regulation mask in forward mode or Battery current regulation mask in reverse mode: 0b = Enter current regulation toggle produces INT 1b = Enter current regulation toggle does not produce INT
5	VINDPM_MASK	R/W	0x0	Reset by: REG_RESET	Input voltage regulation mask (forward mode): 0b = Enter input voltage regulation toggle produces INT 1b = Enter input voltage regulation toggle does not produce INT
4	TREG_MASK	R/W	0x0	Reset by: REG_RESET	IC Thermal regulation mask (forward or reverse mode): 0b = Enter TREG produces INT 1b = Enter TREG does not produce INT
3	WD_MASK	R/W	0x0	Reset by: REG_RESET	I2C watchdog timer mask: 0b = WD expiration produces INT 1b = WD expiration does not produce INT
2	ICO_MASK	R/W	0x0	Reset by: REG_RESET	Input Current Optimizer (ICO) mask: 0b = ICO_STAT change produces INT 1b = ICO_STAT change does not produce INT
1	TS_MASK	R/W	0x0	Reset by: REG_RESET	TS (battery NTC) mask: 0b = TS_STAT change produces INT 1b = TS_STAT change does not produce INT

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Table 6-41. REG0x22_Charger_Mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	CHARGE_MASK	R/W	0x0	Reset by: REG_RESET	Charge cycle mask: 0b = CHARGE_STAT change produces INT 1b = CHARGE_STAT change does not produce INT

6.5.1.29 REG0x23_FAULT_Mask Register (Address = 0x23) [Reset = 0x00]

REG0x23_FAULT_Mask is shown in Table 6-42.

Return to the Summary Table.

Table 6-42. REG0x23_FAULT_Mask Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VIN_OVP_MASK	R/W	0x0	Reset by: REG_RESET	VIN over-voltage mask: 0b = Input overvoltage produces INT 1b = Input overvoltage does not produce INT
6	BAT_FAULT_MASK	R/W	0x0	Reset by: REG_RESET	Battery fault mask: 0b = BAT_FAULT_STAT produces INT 1b = BAT_FAULT_STAT does not produce INT
5	CHG_TMR_MASK	R/W	0x0	Applies to both fast charge and pre-charge safety timers Reset by: REG_RESET	Charge safety timer mask: 0b = Charge timer expiration produces INT 1b = Charge timer expiration does not produce INT
4	CV_TMR_MASK	R/W	0x0	Reset by: REG_RESET	CV timer mask: 0b = CV timer expiration produces INT 1b = CV timer expiration does not produce INT
3	TSHUT_MASK	R/W	0x0	Reset by: REG_RESET	IC thermal shutdown mask: 0b = Enter TSHUT produces INT 1b = Enter TSHUT does not produce INT
2	BYPASS_MASK	R/W	0x0	Reset by: REG_RESET	Bypass mode fault mask: 0b = BYPASS_FLAG produces INT 1b = BYPASS_FLAG does not produce INT
1	RESERVED	R	0x0		Reserved
0	REV_MASK	R/W	0x0	Reset by: REG_RESET	Reverse Mode mask: 0b = REV_STAT change produces INT 1b = REV_STAT change does not produce INT

6.5.1.30 REG0x24_ICO_Current_Limit Register (Address = 0x24) [Reset = 0x0A50]

REG0x24_ICO_Current_Limit is shown in Table 6-43.

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Table 6-43. REG0x24_ICO_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0x0		Reserved
11:4	ICO_IINDPM	R	0xA5	This 16-bit register follows the little-endian convention	Optimized Input Current Limit when ICO is enabled: POR: 3300mA (A5h) Range: 0mA-3300mA (0h-A5h) Clamped High Bit Step: 20mA
3:0	RESERVED	R	0x0		Reserved

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6.5.1.31 REG0x26_Part_Information Register (Address = 0x26) [Reset = 0x05]

REG0x26_Part_Information is shown in Table 6-44.

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Table 6-44. REG0x26_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved
5:2	PN	R	0x1		Device Part number
1:0	DEV_REV	R	0x1		Device Revision

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

A typical application consists of the device paired with an I^2C host and software to charge a multi-cell Li-Ion and Li-polymer batteries. Charging other battery chemistries such as NiMH is allowed but requires host software to change the Li battery based default regulation and termination settings. The charger integrates the switching MOSFETs(Q_1 to Q_4) for the buck-boost converter. The device uses external sense resistors for input current and charging current sensing circuits.

In either forward (charge or sink) or reverse (OTG or source) mode, the converter operates in buck mode if the input voltage (V_{IN}) is above the output (V_{OUT}), buck-boost mode if the input voltage is close to the output voltage or boost mode if the input voltage is below the output voltage. At high output current (I_{OUT}) when in continuous conduction mode (CCM), the average (DC) inductor current of the converter is equal to either the converter output current in buck mode or the input current in boost mode. The expected average inductor current of the converter must not exceed 4A so that the full IINDPM range can be used. Using efficiency estimates from the data sheet efficiency curves, use a power balance shown in Equation 5 to compute the required input current (I_{IN}) for boost mode and to confirm that the adapter voltage and IINDPM setting are high enough for the desired charge current and system load.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \tag{5}$$

The design example equations use the generic converter variables below.

Table 7-1. Equation Variables For Forward/Charge/Sink and Reverse/OTG/Source Converter Operation

EQUATION VARIABLE	FORWARD OPERATION	REVERSE OPERATION
V_{IN}	Minimum or maximum V(ADAPTER or USB) voltage	Minimum or maximum battery voltage at V(SRN)
I_{IN}	Input current estimate from equation above ≤ min current allowed from ADAPTER, USB or IINDPM	Input current estimate from equation above < min of pack protector max discharge current or IBAT_REV limit
V_{OUT}	battery regulation voltage per VREG	Input regulation voltage per VIN_REV
I_{OUT}	Maximum battery charge current ICHG + maximum system load current ISYS	Maximum reverse current < IIN_REV

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7.2 Typical Application Design Example

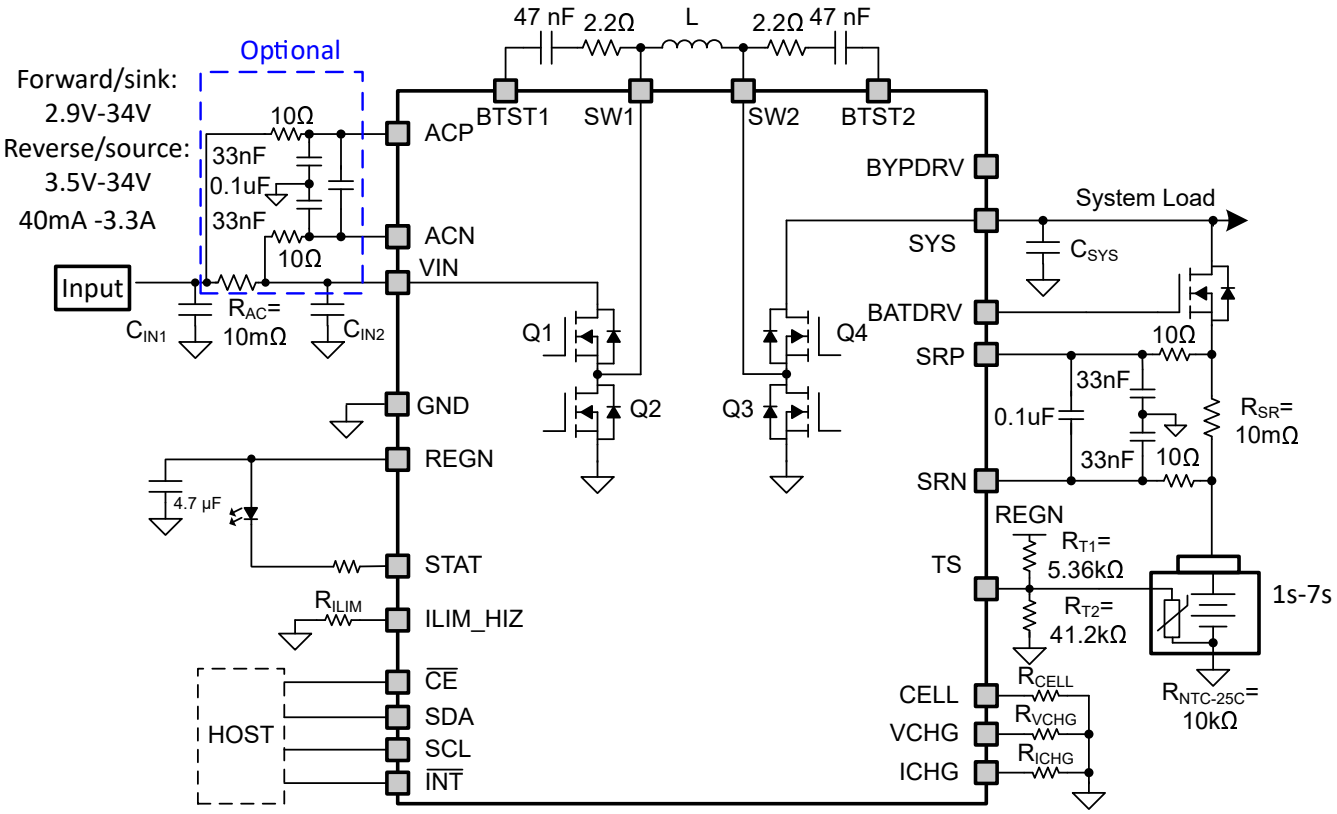


Figure 7-1. BQ25690 Typical Application Diagram

Table 7-2. BQ25690 BOM for Design Example 1

SCHEMATIC COMPONENT OR I²C SETTING	VALUE	COMMENT
f_{SW}	450kHz (default)	REG0x16[4:0]
L	10uH	
C_{IN1}+C_{IN2}	10x 4.7uF	Required: 4x C_{IN1} > C_{IN2}
C_{SYS}	6x 4.7uF	
R_{ILIM}	2.2kΩ	1.5A default
R_{CELL}	6.04kΩ	2S default
R_{VCHG}	14.0kΩ	4.2/cell default
R_{ICHG}	8.25kΩ	1A default
Q_{BATFET}	TPN3R704PL	Rdson = 3.7mΩ in 3.1mm × 3.1mm package

1. Required <<0.1uF noise filtering capacitors at VIN and SYS pins not shown for simplicity
2. Additional C_{IN} or C_{SYS} can be required to mitigate long line inductance effects especially during line or load transients

7.2.1 Design Requirements

Table 7-3. Design Example 1 Parameters

PARAMETER	VALUE	COMMENT
VIN voltage range	5V to 20V	
Input current limit (IINDPM in REG0x06)	3.0A	

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Table 7-3. Design Example 1 Parameters (continued)

PARAMETER	VALUE	COMMENT
Fast charge current limit (ICHG in REG0x02)	3.3A	Clamped by input current limit during boost mode
Max system load current excluding ICHG (ISYS)	1A	
Battery regulation voltage (VREG in REG0x04)	8.4V	
Reverse mode voltage (VIN_REV in REG0x0C)	5V	
Reverse mode minimum battery discharge voltage	6V	Must be > V_{BAT_OKZ} = 2.5V
Reverse mode max discharge current	3A	Clamped by IBAT_REV in REG0x12
Reverse mode output current limit	3.3A	Clamped by IIN_REV in REG0x0A

7.2.2 Detailed Design Procedure

7.2.2.1 Inductor Selection

The DC/DC converter of the charger has an adjustable switching frequency. For small signal stability, the select an inductance within the switching frequency ranges below.

Table 7-4. Inductor Selection per Switching Frequency

SWITCHING FREQUENCY (kHz)	INDUCTANCE - L (µH)
450 - 500	6.8 - 15
550 - 700	4.7 to 10
1200	2.2 - 4.7

To reduce EMI, a shielded inductor is highly recommended. The inductor's saturation current (I_{SAT}) is recommend as at least 20% higher than the larger value of the input current (I_{IN}) in boost mode or the output current (I_{OUT}) in buck mode plus one half the inductor ripple current (I_{RIPPLE}):

$$I_{SAT} \geq MAX\left[\left(I_{IN} + \frac{I_{RIPPLE}}{2}\right), \left(I_{IOUT} + \frac{I_{RIPPLE}}{2}\right)\right] \quad (6)$$

I_{RIPPLE} depends on V_{IN}, V_{OUT}, the switching frequency (F_{SW}), and the inductance (L). Select a larger inductor for the given range of inductances per F_{SW} to minimize I_{RIPPLE}. For a given output current, I_{RIPPLE} is highest when the duty cycle is at 50%. If I_{L_PK} reaches the cycle-by-cycle current limit of 7A, the converters output current is limited. The peak to peak inductor ripple current I_{RIPPLE} of the converter needs to be at least ±10% but no higher than ±20% of I_{L_AVG}. There are some input to output voltage combinations where the charger is not always able to reach 3.3A output current. The inductor current ripple calculations for buck mode and boost mode, as well as the peak inductor current are calculated below:

$$I_{RIPPLE_BUCK} \geq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad (7)$$

$$I_{RIPPLE_BOOST} \geq \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times L} \quad (8)$$

$$I_{L_PK} = I_{L_AVG} + \frac{I_{RIPPLE}}{2} \quad (9)$$

7.2.2.2 Capacitors

Low ESR ceramic capacitors such as X7R or X5R are preferred for the decoupling capacitors and must be placed close to the converter VIN, SYS or SRN and GND pins. To account for the de-rating due to temperature and applied voltage of a ceramic capacitor, the voltage rating of the selected ceramic capacitor must be higher

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than the normal input voltage level. For example, a capacitor with 35V or higher voltage rating is preferred for up to 24V input voltage. Non-ceramic capacitors can be used if the ESR is less than 50mΩ. C_{VIN_ACP} + C_{VIN_ACP} must be at least 10µF after derating with C_{VIN_ACN} < 4×C_{VIN_ACP}. For 1S-2S applications, C_{SYS} must be at least 15µF. For 3S-7S applications, C_{SYS} must be at least 8µF after derating. C_{BAT}, the bulk capacitance close to SRN and GND pins in parallel with the battery pack, must be at least 5µF after derating. The following sections explain how to size the derated capacitance value for the desired steady state voltage ripple. Voltage ripple is the highest for the input of a buck converter and the output of a boost converter. At the start and release of a load transient step, additional capacitance can be required to reduce voltage dips and overshoot, respectively, for a buck, boost or buck-boost converter's output.

7.2.2.3 Buck Mode Input (V_{IN}) Capacitor

In the buck mode operation, the input current is discontinuous, which dominates the input RMS ripple current and input voltage ripple. The converter input capacitors must have enough ripple current rating (i.e. low ESR) to absorb the input AC current and have large enough capacitance to maintain the small input voltage ripple. For buck mode operation, the input RMS ripple current and input voltage ripple are calculated by the equations below, where D = V_{OUT} / V_{IN}.

$$I_{CIN-BUCK} = I_{OUT} \times \sqrt{D \times (1-D)} \tag{10}$$

$$\Delta V_{IN-BUCK} \geq \frac{D \times (1-D) \times I_{OUT}}{C_{IN-BUCK} \times f_{SW}} \tag{11}$$

The worst case input RMS ripple current and input voltage ripple both occur at 0.5 duty cycle condition.

7.2.2.4 Boost Mode Output (V_{OUT}) Capacitor

In the boost mode operation, the output current is discontinuous, which dominates the output RMS ripple current and output voltage ripple. The output capacitors must have enough ripple current rating to absorb the output AC current (meaning low enough ESR) and have large enough capacitance to maintain the small output voltage ripple.For boost mode operation, the output RMS ripple current and the output voltage ripple are calculated by the equations below, where D = (1 - V_{IN} / V_{OUT}).

$$I_{COUT-BOOST} = I_{OUT} \times \sqrt{\frac{D}{(1-D)}} \tag{12}$$

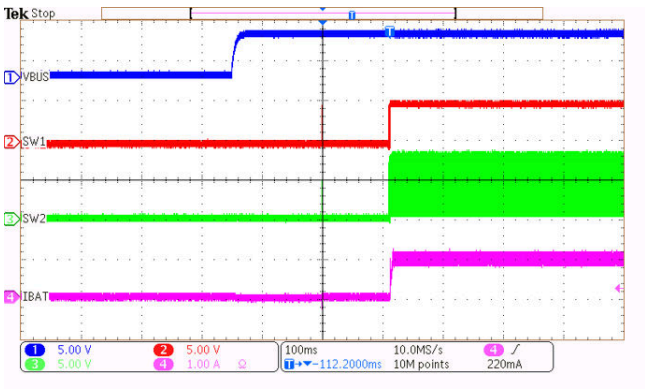
$$\Delta V_{OUT-BOOST} \geq \frac{D \times I_{OUT}}{C_{OUT-BOOST} \times f_{SW}} \tag{13}$$

The worst case output RMS ripple current and output voltage ripple both occur at the lowest V_{IN} input voltage of the converter. Additional capacitance can be required for large, fast load transients.

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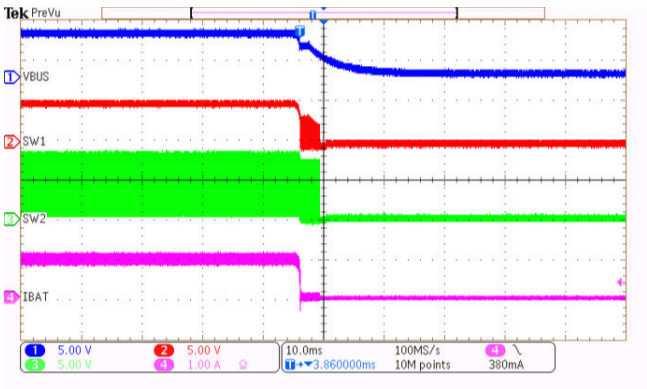
7.2.3 Application Curves

C_{VIN} = 10*4.7µF, C_{SYS} = 6*4.7µF, C_{BAT} = 4*4.7µF, L1 = 10µH (SRP5050FA-100M), Fsw = 450kHz.



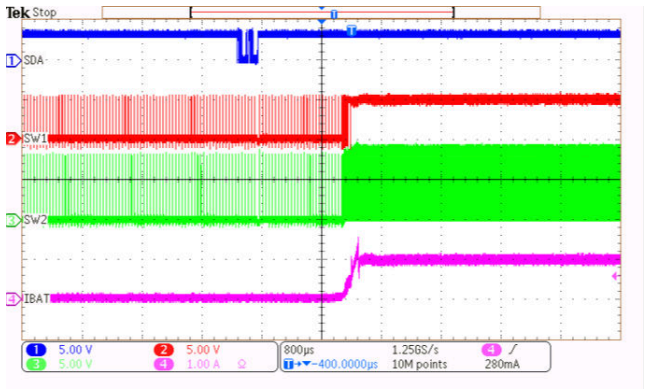
VBUS = 5V VBAT = 7.4V ICHG = 1A

Figure 7-2. Adapter Plug In with Charge Enabled



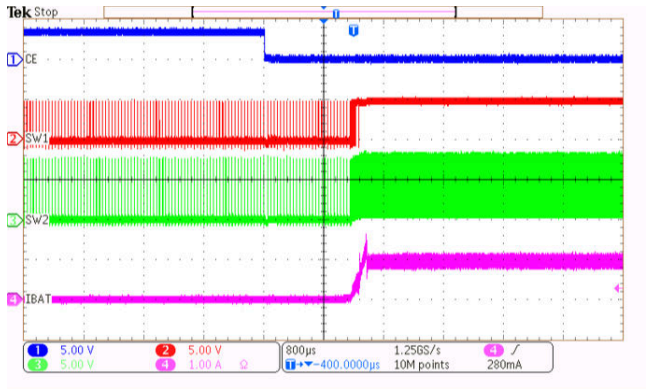
VBUS = 5V VBAT = 7.4V ICHG = 1A

Figure 7-3. Adapter Unplug with Charge Enabled



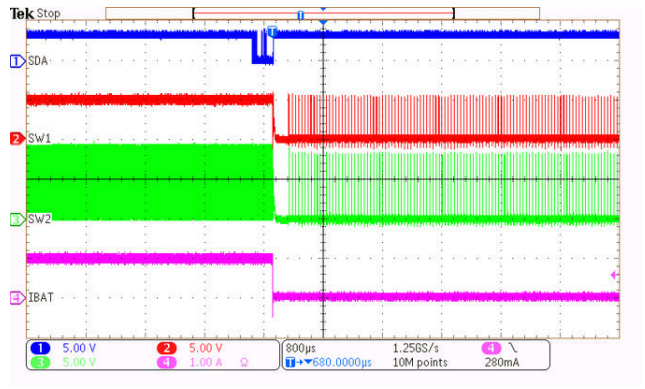
VBUS = 5V VBAT = 7.4V ICHG = 1A

Figure 7-4. Enable Charge with I²C



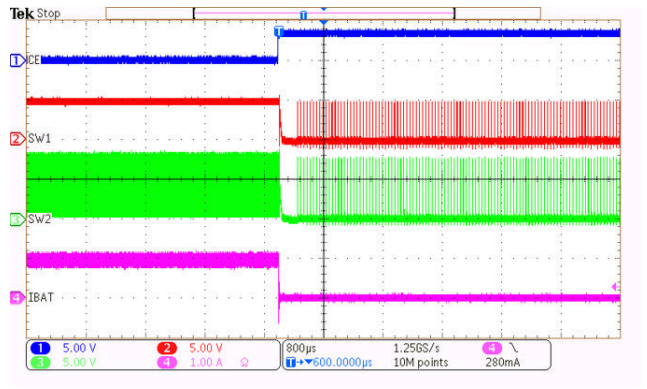
VBUS = 5V VBAT = 7.4V ICHG = 1A

Figure 7-5. Enable Charge with $\overline{CE}$ Pin



VBUS = 5V VBAT = 7.4V ICHG = 1A

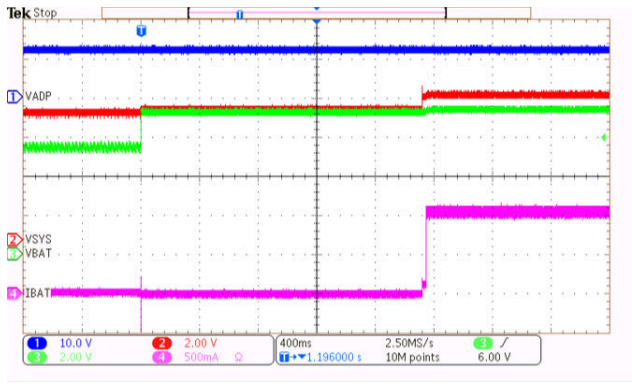
Figure 7-6. Disable Charge with I²C



VBUS = 5V VBAT = 7.4V ICHG = 1A

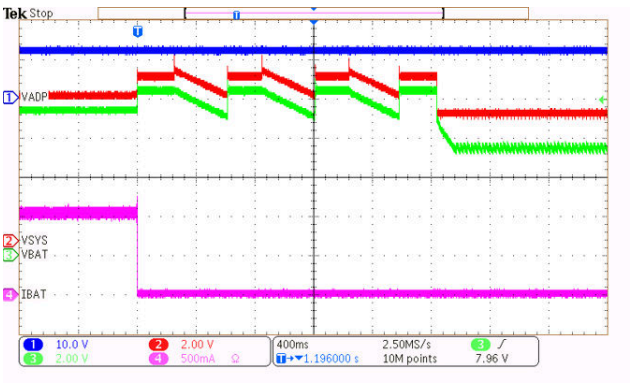
Figure 7-7. Disable Charge with $\overline{CE}$ Pin

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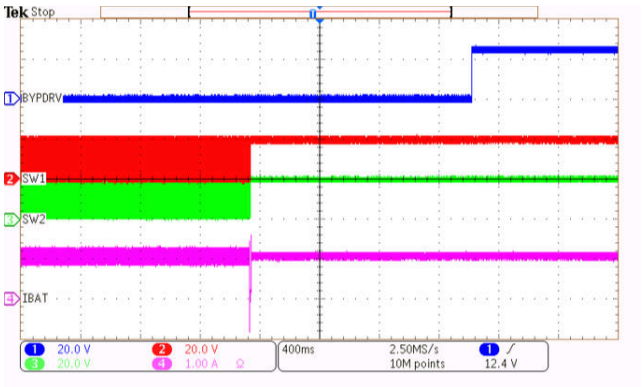
VBUS = 12V VBAT = 7.4V ICHG = 1A
VSYSMIN = 6.2V VBAT_DETECT = 2.8V

Figure 7-8. Battery Plug In Detection



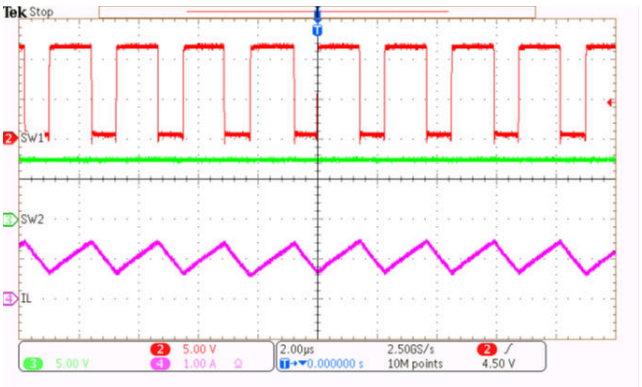
VBUS = 12V VBAT = 7.4V ICHG = 1A
VSYSMIN = 6.2V VBAT_DETECT = 2.8V

Figure 7-9. Battery Unplug Detection



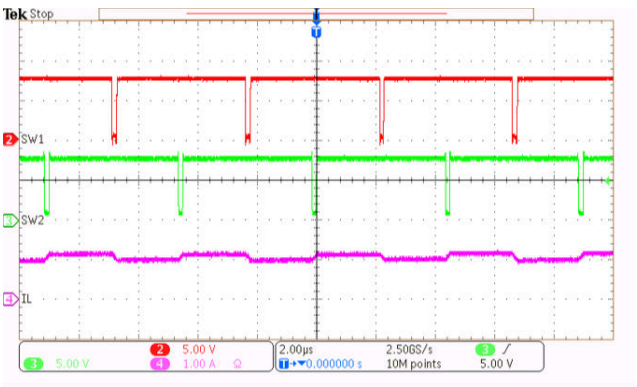
VBUS = 20V VBAT = 20V ICHG = 1A

Figure 7-10. Buck-Boost to Internal Bypass to External Bypass Transition



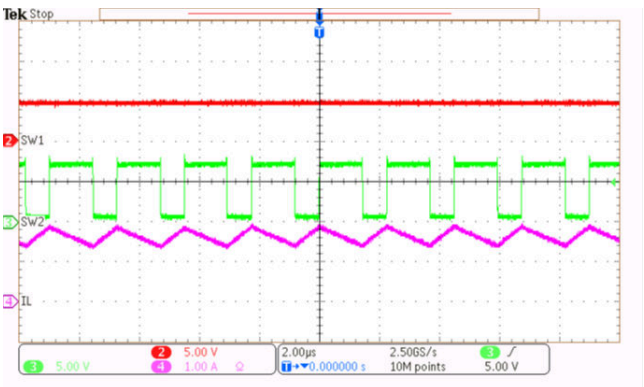
VBUS = 12V VBAT = 7.4V ICHG = 1A

Figure 7-11. Forward Buck Mode CCM



VBUS = 8V VBAT = 7.4V ICHG = 1A

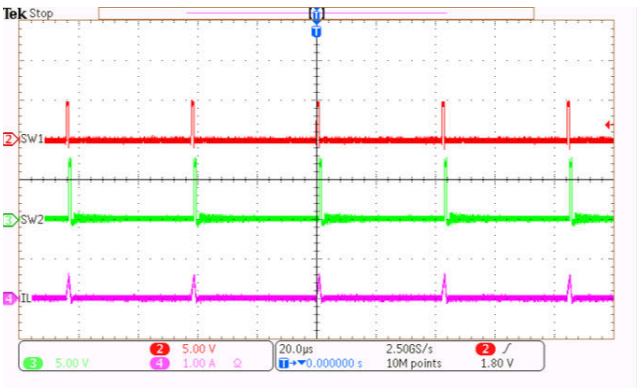
Figure 7-12. Forward Buck-Boost Mode CCM



VBUS = 5V VBAT = 7.4V ICHG = 1A

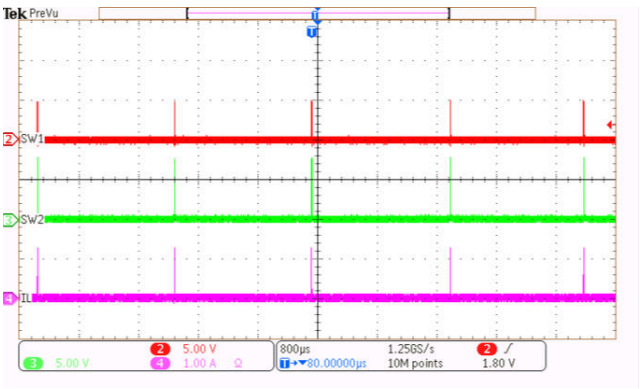
Figure 7-13. Forward Boost Mode CCM

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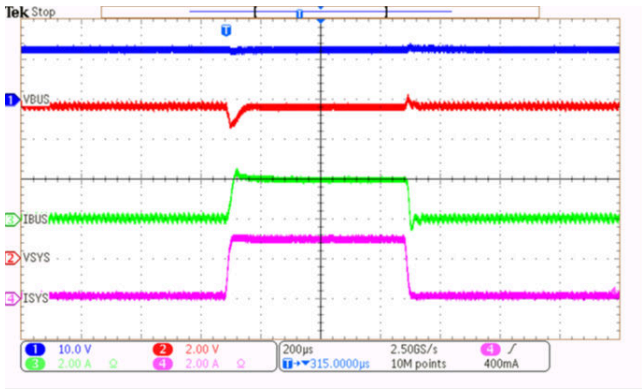
VBUS = 5V VBAT = 7.4V No Load

Figure 7-14. Forward Boost Mode PFM with OOA



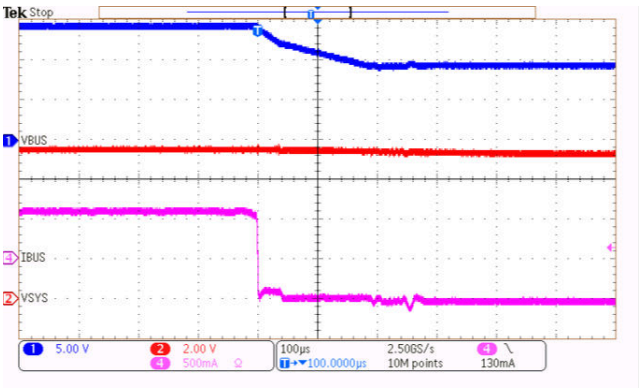
VBUS = 5V VBAT = 7.4V No Load

Figure 7-15. Forward Boost Mode PFM without OOA



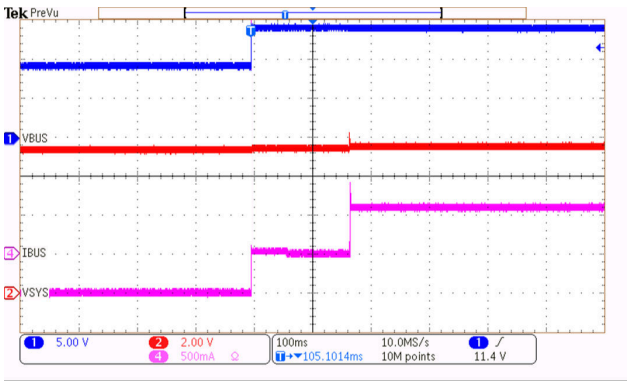
VBUS = 12V VBAT = 7.4V Charge Disabled
I_{SYS} = 0.1A to 3A to 0.1A

Figure 7-16. Forward Mode I_{SYS} Transient Response



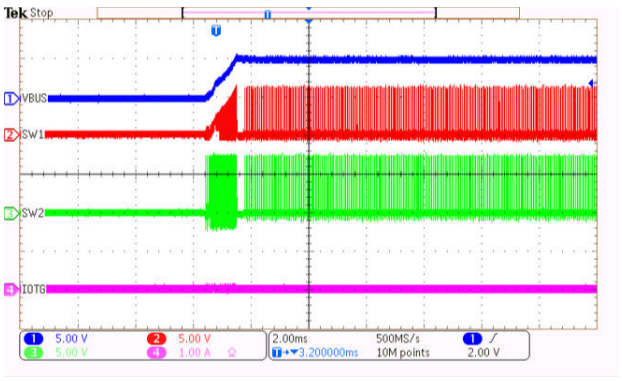
VBUS = 14V VBAT = 7.4V ICHG = 1A
VINDPM = 12V VIN_REV = 9V
VIN_BACKUP = 100% VINDPM

Figure 7-17. Backup Mode Entry



VBUS = 14V VBAT = 7.4V ICHG = 1A
VINDPM = 12V VIN_REV = 9V
VIN_BACKUP = 100% VINDPM

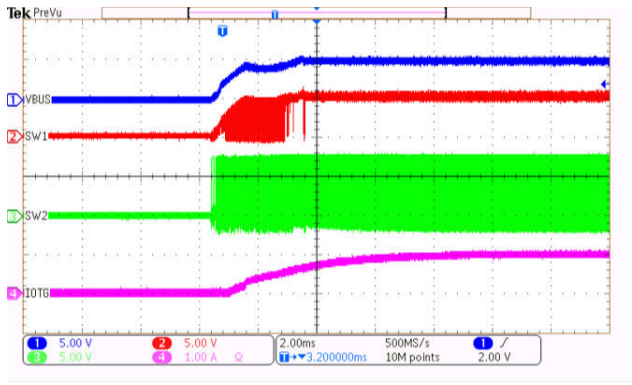
Figure 7-18. Backup Mode Exit



VIN_REV = 5V VBAT = 7.4V I_{OTG} = 0A

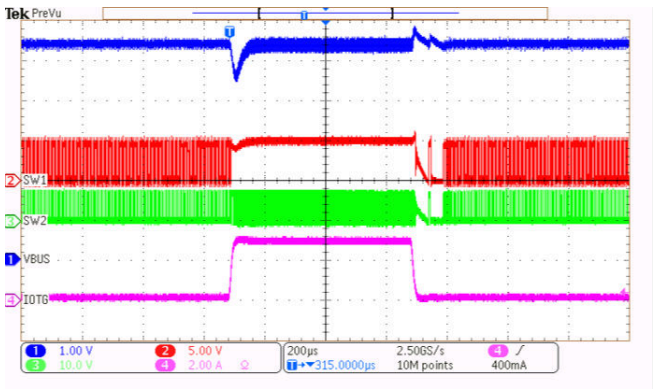
Figure 7-19. Enable Reverse Mode with No OTG Load

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VIN_REV = 5V VBAT = 7.4V I_{OTG} = 1A

Figure 7-20. Enable Reverse Mode with 1A OTG Load



VBUS = 5V VBAT = 7.4V VIN_REV = 5V
I_{OTG} = 0.1A to 3A to 0.1A

Figure 7-21. Reverse Mode I_{OTG} Transient Response

7.3 Power Supply Recommendations

To provide an output voltage on SYS, the device requires a power supply between 2.5V and 34V input with recommended >200mA current rating connected to VBUS or a 1s to 7s Li-Ion battery with voltage higher than V_{BAT_OK} connected to BAT. The source current rating needs to be at least 3.3A for the converter of the charger to provide maximum output power to SYS.

7.4 Layout

7.4.1 Layout Guidelines

The switching nodes rising and falling times must be minimized for minimal switching losses. Proper layout of the components to minimize the high frequency current path loops (shown in the figure below) is important to minimize switching noise coupling, electrical and magnetic field radiation and high frequency resonant problems. Below is a PCB layout list in order of priority.

1. Place the SYS capacitors as close to SYS and GND pins as possible with vias. Place a 0.1µF small footprint capacitor and at least one of the bulk capacitors closer than the other capacitors. The positive and negative terminals of these two capacitors must be connected on the same layer as the IC without vias.
2. Place the VIN capacitors as close to VIN and GND as possible. Place a 0.1µF small footprint capacitor and at least one of the bulk capacitors closer than the other capacitors. The positive and negative terminals of these two capacitors must be connected on the same layer as the IC without vias.
3. Place one inductor terminal to SW1 and the other terminal to SW2 as close as possible to IC pins. Rules 1 and 2 require that the SWx copper traces be routed under the IC where a via is placed to the inductor. Verify that the traces are wide enough to carry the inductor current but small enough to minimize EMI. Minimize parasitic capacitance from these traces by cutting out ground pours or planes on neighboring layers.
4. Place the REGN capacitor close to the REGN and GND pins using vias if necessary. The bootstrap capacitors can be placed close to the BTSTx pins and GND using vias if necessary.
5. Place the battery capacitors close to SRN and GND.
6. Route ACP, ACN, SRP, SRN, TS traces and filter capacitor GND away from switching nodes such as SW1 and SW2.
7. Place at least 3 thermal vias directly under the power pad, connecting to copper on other layers.
8. Via size and number must be enough for a given current path.

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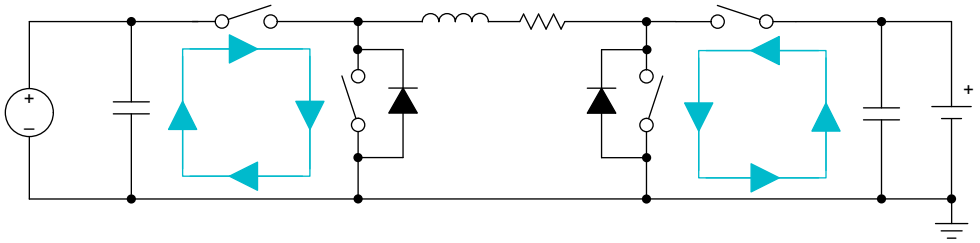


Figure 7-22. Converter High Frequency Current Path

7.4.2 Layout Example

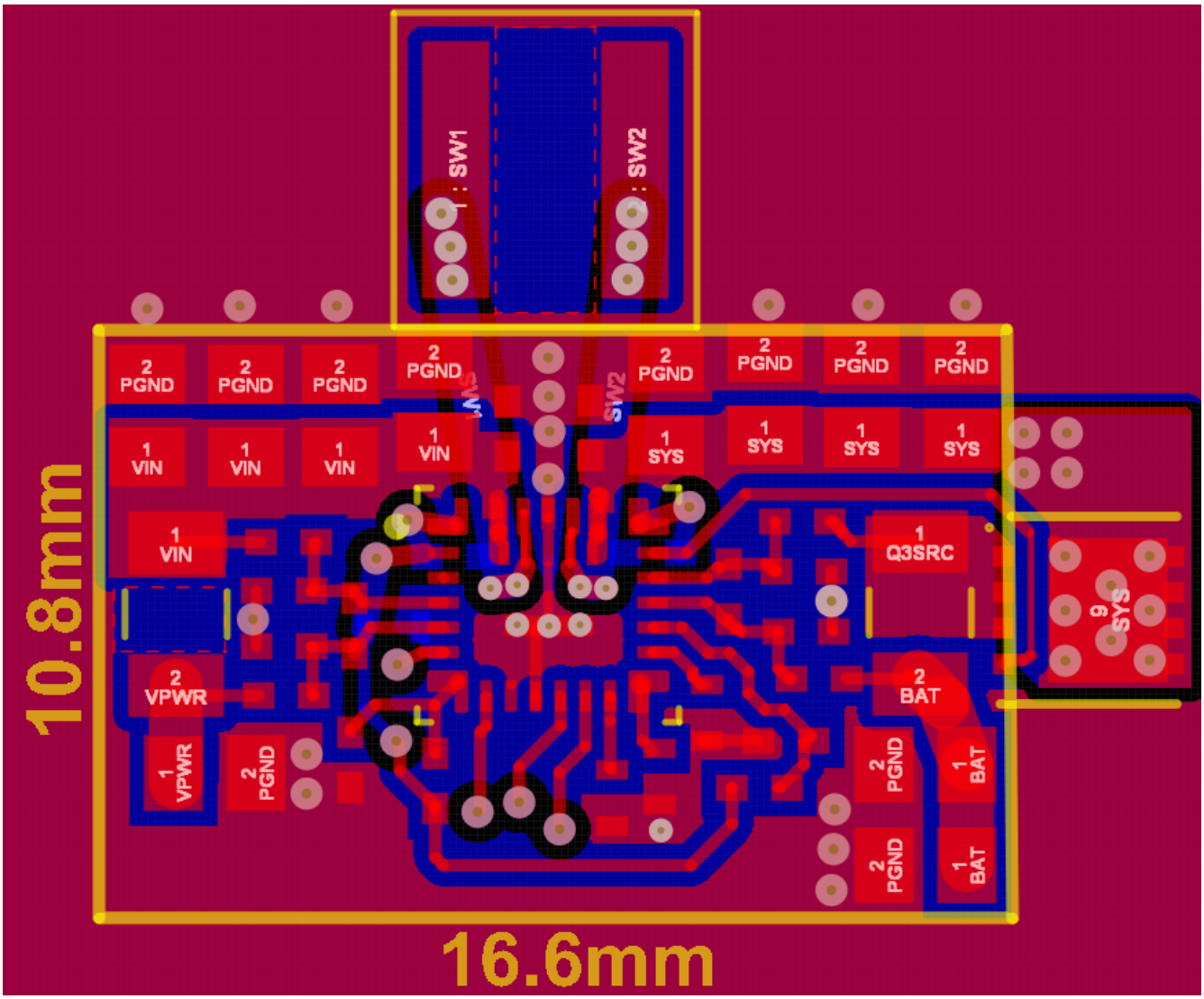


Figure 7-23. Top Layer of 2 Layer PCB Layout Example - Red is Ground

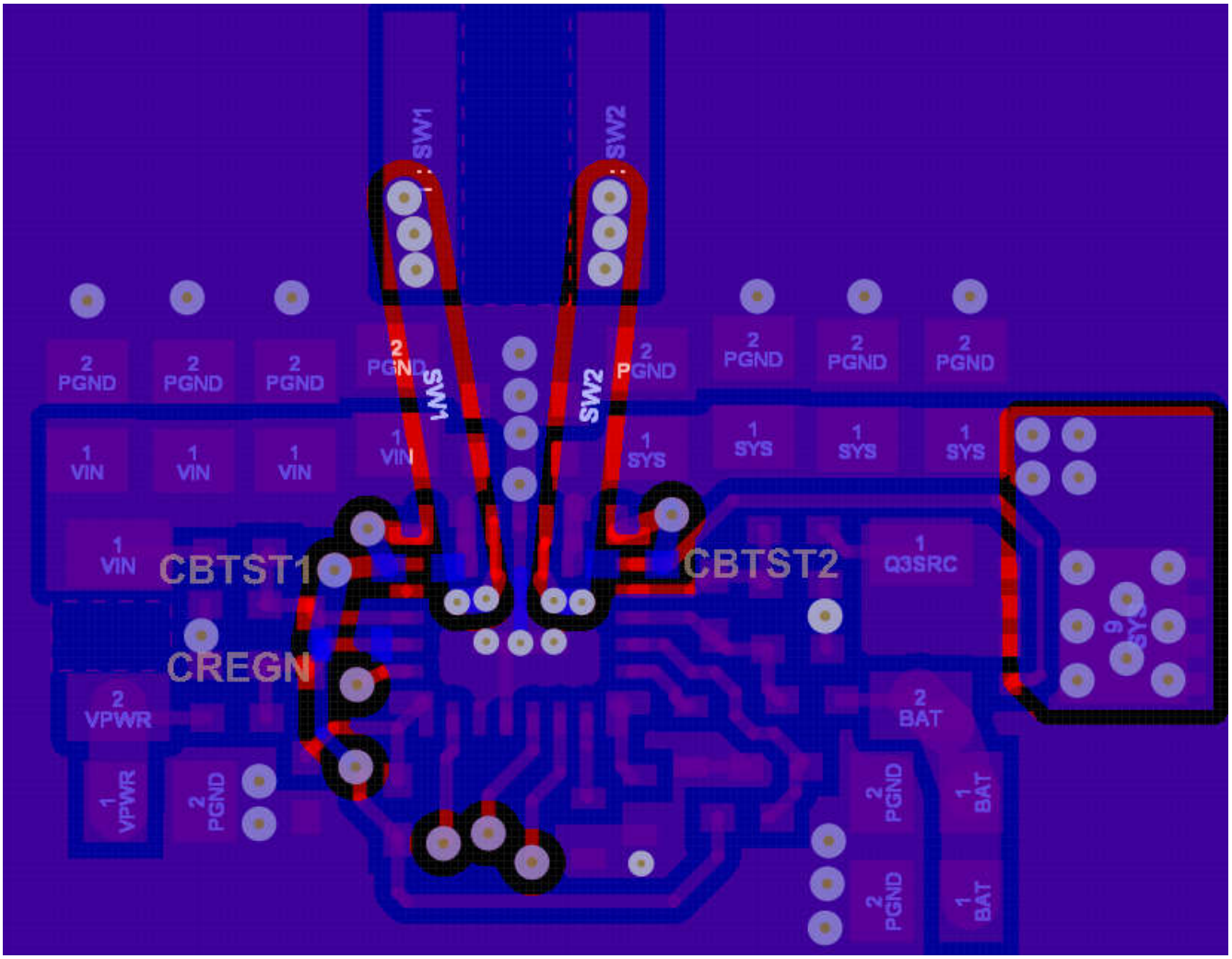


Figure 7-24. Bottom Layer of 2 Layer PCB Layout Example - Blue/Purple is GND

Figure 7-23 shows the recommended placement and routing of external components for 2 layer board. For a prioritized list of component placement, please refer to Layout Guidelines

1. For maximum power dissipation, using a 4 layer board with 1 internal layer as GND and redundant power pin pours/planes are recommended . See the EVM layout as an example.
2. For minimum board space, the inductor can be placed on the bottom layer under the IC.

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (December 2025)	Page
• Changed the device status from Advanced to Production Data	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
BQ25690RBAR	Active	WQFN-HR	RBA	26	3000	RoHS & Green	Matte Tin	MSL2	-40 to 125	B690

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

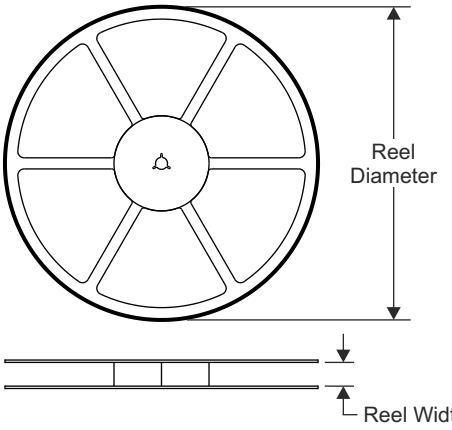
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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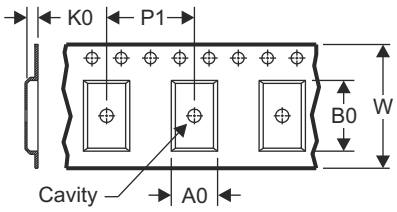
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10.2 Tape and Reel Information

REEL DIMENSIONS

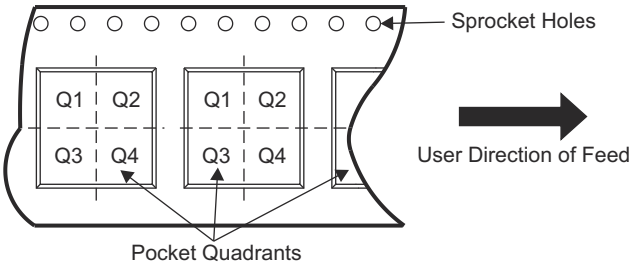


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

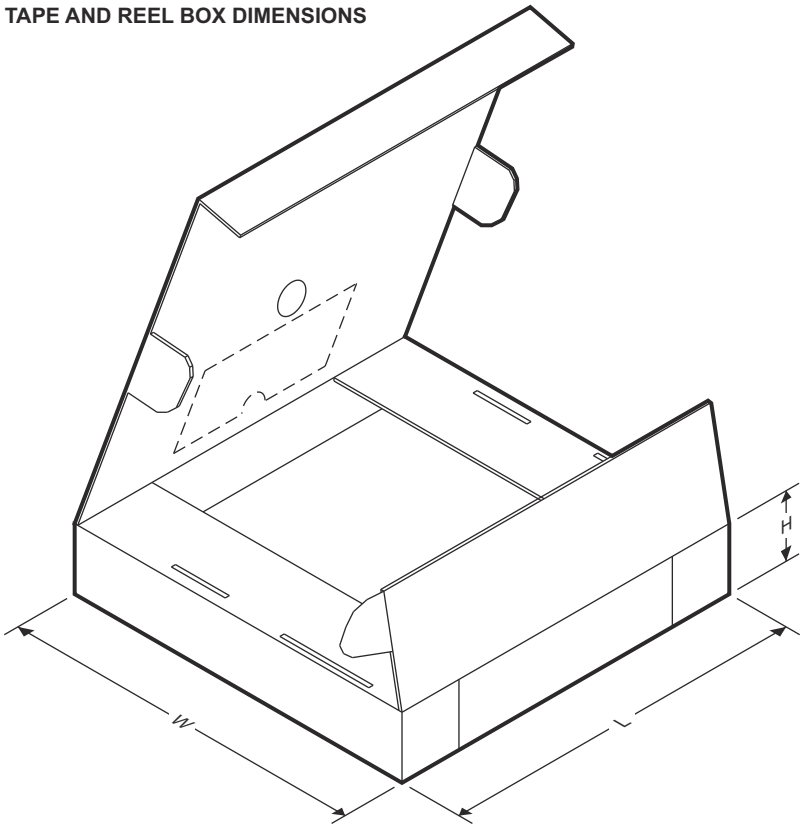
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25690RBAR	WQFN-HR	RBA	26	3000	330	12.4	3.8	4.3	1.5	8.0	12.0	Q2

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25690RBAR	WQFN-HR	RBA	26	3000	367.0	367.0	35.0

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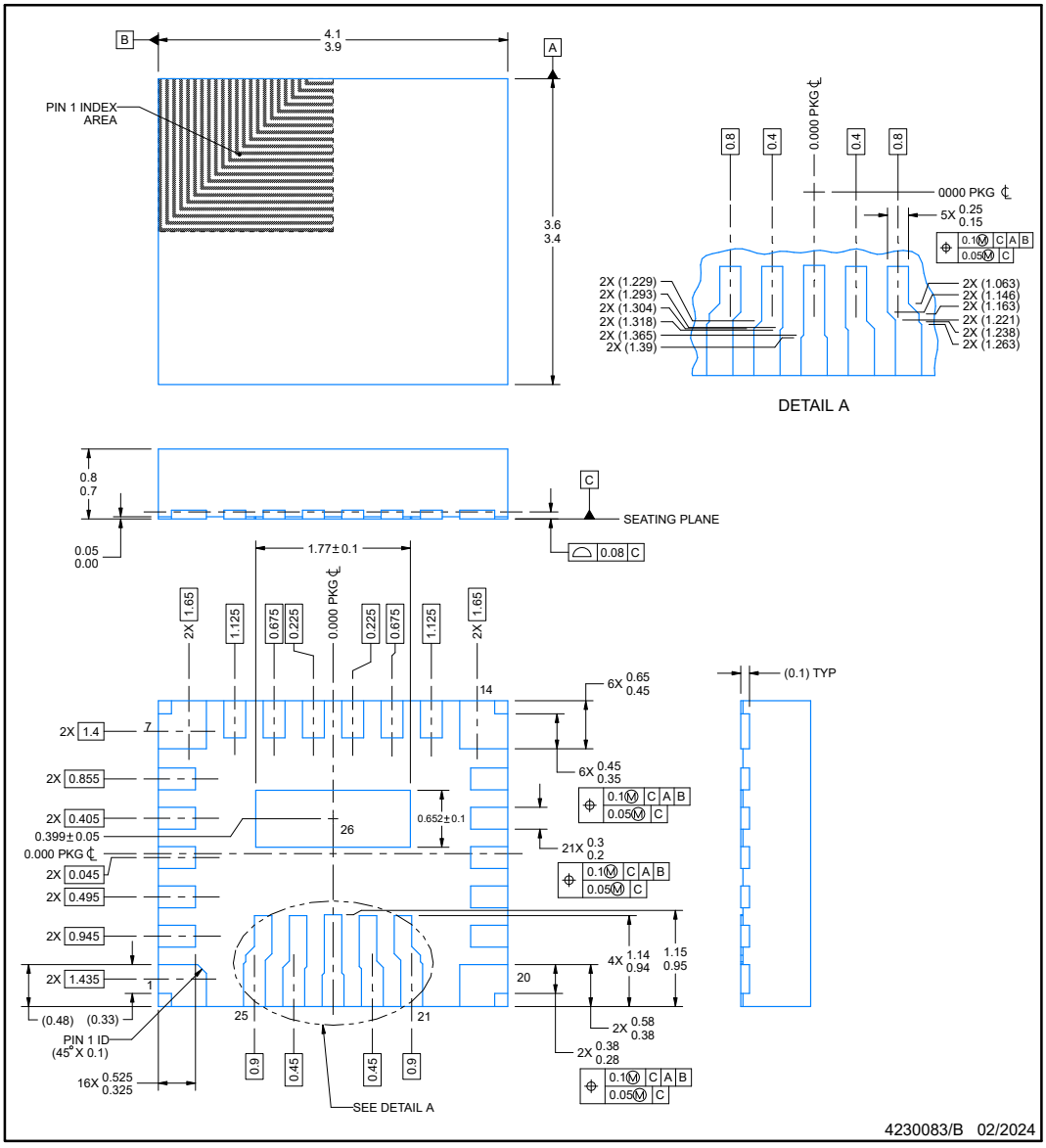
10.3 Mechanical Data

RBA0026A

PACKAGE OUTLINE

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

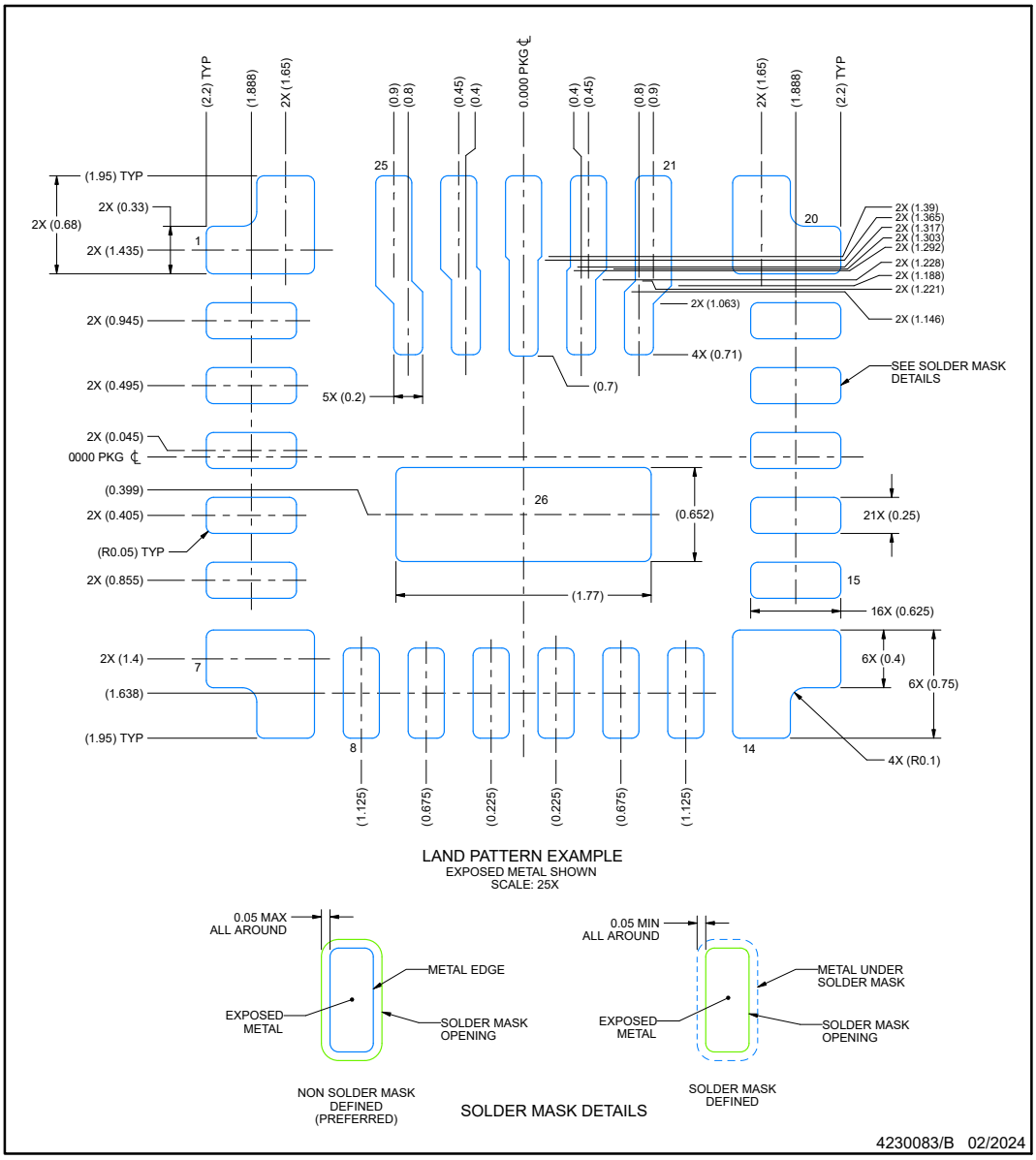
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EXAMPLE BOARD LAYOUT

RBA0026A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

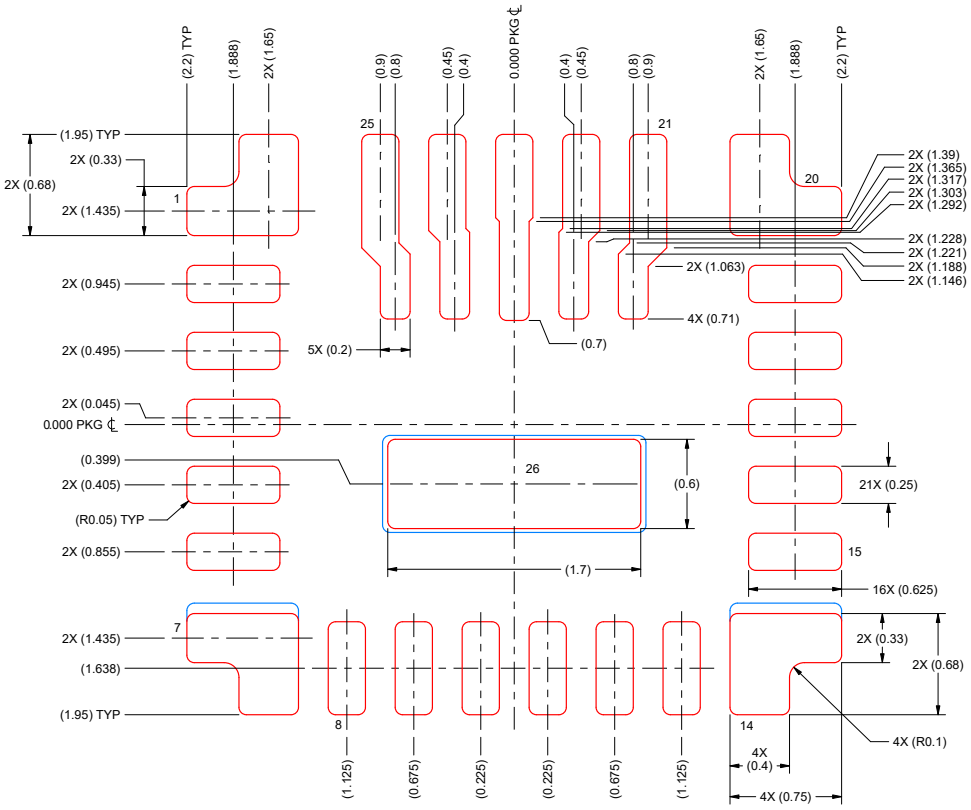
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RBA0026A — **WQFN-HR - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 7, 14 & 26: 88%

4230083/B 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25690RBAR	Active	Production	WQFN-HR (RBA) | 26	3000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	-40 to 125	B690

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

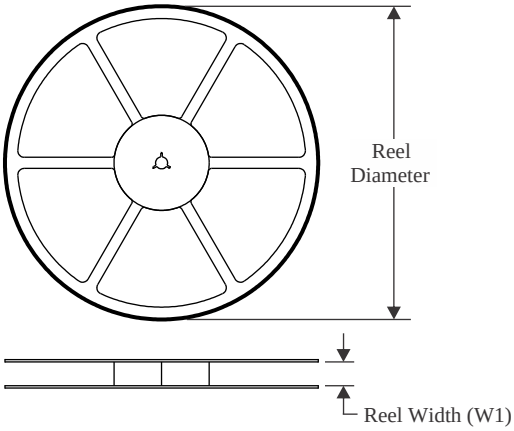
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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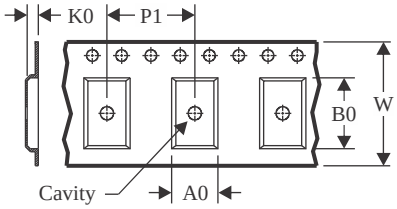
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

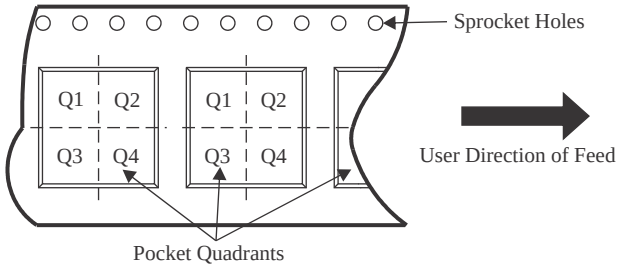


TAPE DIMENSIONS



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B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

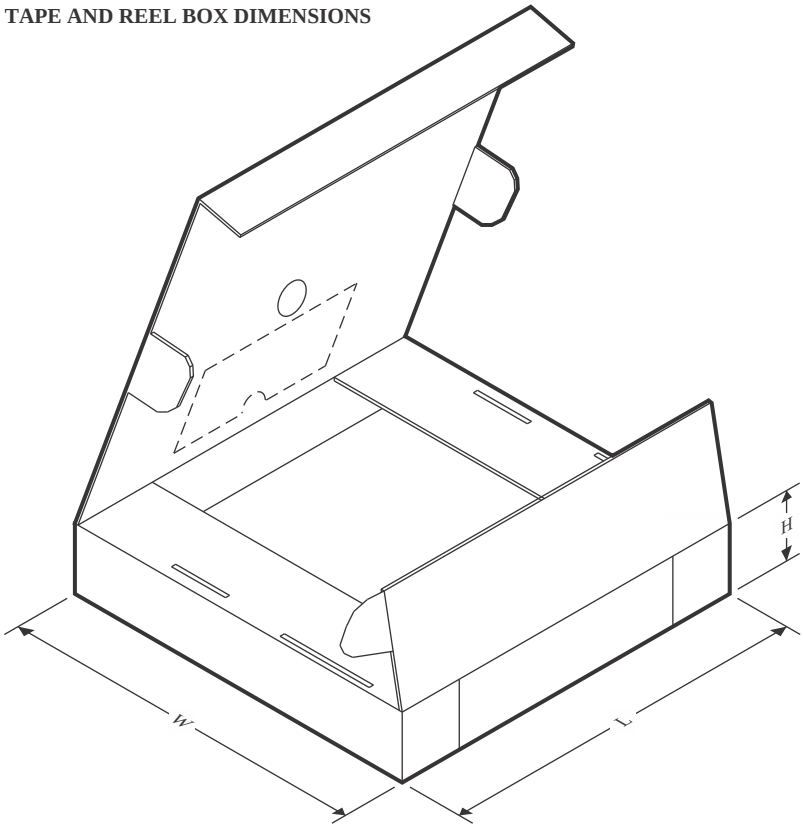
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25690RBAR	WQFN-HR	RBA	26	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25690RBAR	WQFN-HR	RBA	26	3000	360.0	360.0	36.0

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