# BQ25180 I²C Controlled, 1-Cell, 1-A Linear Battery Charger with Power Path and Ship Mode

## 1 Features

- 1-A Power path linear battery charger
  - 3.0-V to 5.9-V input voltage operating range optimized for battery to battery charging and USB adapter
  - 25-V tolerant input voltage
  - Configurable battery regulation voltage with 0.5% accuracy from 3.6 V to 4.65 V in 10-mV steps
  - 5-mA to 1-A configurable fast charge current
  - 55-mΩ battery FET ON resistance
  - Up to 2.5-A discharge current to support high system loads
  - Configurable termination current down to 0.5 mA
  - Configurable NTC charging profile thresholds including JEITA support
  - Power cycle and advanced reset mechanisms to recover system
- Power path management for powering the system and charging the battery
  - Regulated system voltage (SYS) ranging from 4.4 V to 4.9 V in addition to battery voltage tracking and input pass-though options
  - Configurable input current limit
  - Selectable adapter or battery power for system
  - Dynamic power path management optimizes charging from weak adapters
- Ultra low quiescent current modes
  - 15-nA Shutdown mode
  - 3.2-µA Ship mode with button press wake
  - 3 µA in Battery Only mode
  - 30-µA input adapter Iq in Sleep mode
- One push-button wake-up and reset input
- Integrated fault protection
  - Input overvoltage protection ($V_{IN_OVP}$)
  - Battery undervoltage protection ($V_{BUVLO}$)
  - Battery short protection (BATSC)
  - Battery overcurrent protection (BATOCP)
  - Input current limit protection (ILIM)
  - Thermal regulation (TREG) and thermal shutdown (TSHUT)
  - Battery thermal fault protection (TS)
  - Watchdog and safety timer fault
  - System short protection
  - System overvoltage protection

## 2 Applications

- TWS headset and charging case
- Smart glasses, AR and VR
- Smart watches and other wearable devices
- Retail automation and payment
- Building automation

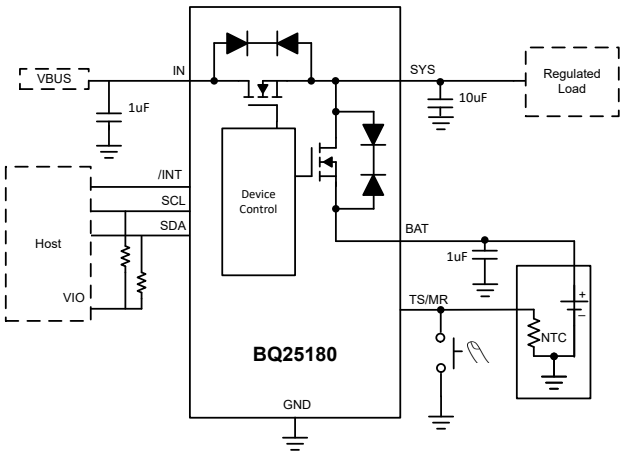
## 3 Description

The BQ25180 is a linear battery charger IC focusing on small solution size and low quiescent current for extending battery life. The device is available in an 8-ball chipscale package which does not need HDI PCB process for fabrication thereby reducing the PCB cost. The device can support up to 1-A charging and system loads of up to 2.5 A.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| BQ25180 | DSBGA (8) | 1.6 mm x 1.1 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Simplified Schematic**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (January 2022) to Revision C (January 2023) | Page |
|---|---|
| • Removed figure from Section 8.3.1 | 16 |

| Changes from Revision A (December 2021) to Revision B (January 2022) | Page |
|---|---|
| • Removed operating ambient | 5 |
| • Removed OTP_VLOWV | 6 |
| • Removed Standalone | 6 |
| • Removed /PG Isink | 6 |
| • Removed $t_{HW_RESET}$ and $F_{I2C_CLK}$ | 10 |
| • Updated conditions for Typical Characteristics | 11 |
| • Added legend for Figure 7-1 | 11 |
| • Changed Figure 8-4 and Figure 8-5 | 21 |
| • Changed MR input to Pushbutton input in Table 8-6 | 25 |
| • Updated Section 8.5 Register Maps reset values | 26 |
| • Changed Device_ID description in the Table 8-21 | 26 |

| Changes from Revision * (September 2021) to Revision A (December 2021) | Page |
|---|---|
| • Changed from Advance Information to Production Data | 1 |


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## 5 Description (continued)

The battery is charged using a standard Li-ion or LiFePO4 charge profile with three phases: precharge, constant current and constant voltage. Thermal regulation provides the maximum charge current while managing the device temperature. The charger is also optimized for battery to battery charging with 3-V minimum input voltage operation and can withstand 25-V absolute maximum line transients. The device integrates a single push-button input and reset circuitry to reduce the total solution footprint.

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# 6 Pin Configuration and Functions

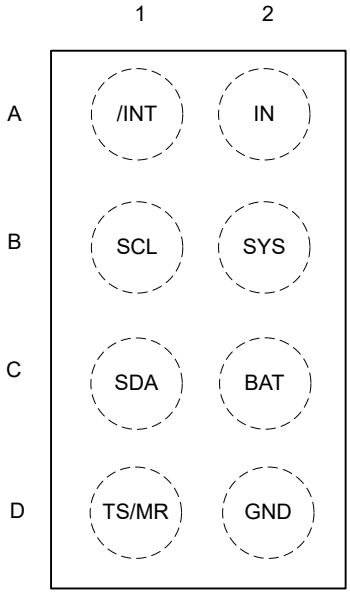



**Figure 6-1. YBG Package 8-Pin DSBGA (Top View)**

**Table 6-1. Pin Functions**

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN | A2 | P | DC Input Power Supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1 µF of capacitance using a ceramic capacitor. |
| SYS | B2 | P | Regulated System Output. Connect at least 10-µF ceramic capacitor (at least >1 µF of ceramic capacitance with DC bias derating) from SYS to GND as close to the SYS and GND pins as possible. |
| BAT | C2 | P | Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1 µF of ceramic capacitance. |
| GND | D2 | - | Ground connection. Connect to the ground plane of the circuit. |
| SCL | B1 | I/O | $I^2C$ Interface Clock. Connect SCL to the logic rail through a 10-kΩ pullup resistor. |
| SDA | C1 | I/O | $I^2C$ Interface Data. Connect SDA to the logic rail through a 10-kΩ pullup resistor. |
| /INT | A1 | O | INT is an open-drain output that signals fault interrupts. When a fault occurs, a 128-µs active low pulse is sent out as an interrupt for the host. INT is enabled/disabled using the MASK_INT bit in the control register. Can be pulled up to the logic rail through a 1-kΩ to 20-kΩ resistor. |
| TS/MR | D1 | I/O | Manual Reset Input/ NTC thermistor pin. TS/MR is a general purpose input that must be held low for greater than $t_{LPRESS}$ to go into Ship mode or perform a hardware reset. It can also be used to detect shorter button press durations such as $t_{WAKE1}$ and $t_{WAKE2}$ TSMR may be driven by a momentary push-button or a MOS switch. The TSMR pin can also have an NTC thermistor connected on to it. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input Voltage | IN | -0.3 | 25 | V |
| Voltage | All other pins | -0.3 | 5.5 | V |
| Input Current (DC) | IN | | 1.1 | A |
| SYS Discharge Current(DC) | SYS | | 1.5 | A |
| SYS Discharge Current (tpulse <20ms) | SYS | | 2.5 | A |
| Output Sink Current | /INT | | 20 | mA |
| $T_J$ | Junction temperature | -40 | 150 | °C |
| $T_{stg}$ | Storage temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1) | ±2500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Thermal Information

| THERMAL METRIC | | BQ25180 YBG (DSBGA) 8 PIN | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (EVM(2)) | 65 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (JEDEC(1)) | 107.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 30.3 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 30.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) 1oz Copper, 2-layer board

## 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VBAT | Battery Voltage Range | 2.2 | | 4.6 | V |
| VIN | Input Voltage Range | 2.7 | | 5.5 | V |

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## 7.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| IIN | Input Current Range (IN to SYS) | | | 1.1 | A |
| IBAT | Battery Discharge Current (BAT to SYS) | | | 1.5 | A |
| TJ | Operating Junction Temperature Range | -40 | | 125 | °C |

## 7.5 Electrical Characteristics

VIN = 5V, VBAT = 3.6V. -40°C < TJ < 125°C unless otherwise noted. Typical data at TJ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CURRENTS** | | | | | | |
| $I_{Q_IN}$ | Input supply quiescent current | VBAT = 3.6V, VIN = 5V, Charge enabled, ICHG = 0mA, SYSREG = 4.5V | | 0.75 | 1 | mA |
| $I_{Q_IN}$ | Input supply quiescent current | VBAT = 3.6V, VIN = 5V, Charge enabled, ICHG = 0mA, SYSREG = Passthrough | | 0.660 | 0.850 | mA |
| $I_{SLEEP_IN}$ | SLEEP input current | VIN = 3.6V, VBAT = 3.7V | | 30 | | µA |
| $I_{Q_BAT}$ | Battery quiescent current | $V_{IN}$ <$V_{UVLO}$ or floating, Watchdog disabled, Push button disabled, I2C functional. VBAT =3.6V $T_J$ = 25°C | | 3 | 3.5 | µA |
| $I_{Q_BAT}$ | Battery quiescent current | $V_{IN}$ <$V_{UVLO}$ , VBAT =3.6V, Push-button function enabled, 0°C < $T_J$ < 85°C | | 4 | 5 | µA |
| $I_{BAT_SHUTDOWN}$ | Battery discharge current in Ship Mode | VIN = 0V, Ship Mode, VBAT = 3.6V, Adapter Sense wake enabled. | | 15 | | nA |
| $I_{BAT_SHIP}$ | Battery discharge current in Ship Mode | VBAT = 3.6V, Push button function enabled (average current), 0°C < $T_J$ < 85°C | | 3.2 | 4.5 | µA |
| **POWER-PATH MANAGEMENT AND INPUT** | | | | | | |
| $V_{IN_OP}$ | Input voltage operating range | | 3 | | 5.5 | V |
| $V_{IN_UVLOZ}$ | Exit IN undervoltage lock-out | IN rising | | | 3 | V |
| $V_{IN_UVLO}$ | Enter IN undervoltage lock-out | IN falling | | | 2.7 | V |
| $V_{IN_LOWV}$ | IN voltage to start charging | IN rising | | 3 | 3.15 | V |
| $V_{IN_LOWVZ}$ | IN voltage to stop charging | IN falling | | 2.95 | 3.1 | V |
| $V_{IN_PORZ}$ | IN voltage threshold to enter shipmode | IN falling | 1.09 | 1.3 | 1.66 | V |
| $V_{SLEEPZ}$ | Exit sleep mode threshold | IN rising, VIN - VBAT, VBAT= 4V | 100 | 135 | 185 | mV |
| $V_{SLEEP}$ | Sleep mode threshold hysteresis | IN falling, VIN - VBAT, VBAT= 4V | | 72 | | mV |
| $V_{IN_OVP}$ | VIN overvoltage rising threshold | IN rising | 5.5 | 5.7 | 5.9 | V |
| $V_{IN_OV_HYS}$ | IN overvoltage hysteresis | IN falling | | 125 | | mV |
| $I_{BAT_OCP}$ | BATOCP(Reverse OCP only) | VBAT = 3.6V, IBAT_OCP= 00 | | 0.5 | | A |
| | | VBAT = 3.6V, IBAT_OCP= 01 | | 1 | | A |
| | | VBAT = 3.6V, IBAT_OCP= 10 | | 1.5 | | A |
| | | VBAT = 3.6V, IBAT_OCP= 11 | | Disabled | | A |
| VBSUP1 | Enter supplement mode threshold | VBAT = 3.6V, VBAT > $V_{BUVLO}$, VSYS< VBAT-VBSUP1 | | 40 | | mV |
| VBSUP2 | Exit supplement mode threshold | $V_{BAT}$ > $V_{BUVLO}$, VSYS>VBAT-VBSUP2 | | 20 | | mV |


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## 7.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. -40°C < TJ < 125°C unless otherwise noted. Typical data at TJ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ILIM | Input Current Limit | VIN = 5V, ILIM =50mA | 40 | 50 | 60 | mA |
| | | VIN = 5V, ILIM =100mA | 80 | 90 | 98 | mA |
| | | VIN = 5V, ILIM= 200mA | 180 | 200 | 220 | mA |
| | | VIN = 5V, ILIM= 300mA | 270 | 300 | 330 | mA |
| | | VIN = 5V, ILIM= 380mA | 360 | 380 | 400 | mA |
| | | VIN = 5V, ILIM= 500mA | 450 | 475 | 498 | mA |
| | | VIN = 5V, ILIM =665mA | 630 | 665 | 700 | mA |
| | | VIN = 5V, ILIM= 1050mA | 995 | 1050 | 1100 | mA |
| $V_{INDPM_ACC}$ | VINDPM accuracy | VINDPM target is not disabled | -3 | | 3 | % |
| $V_{INDPM}$ | Input voltage threshold when input current is reduced | VINDPM target =4.2V | | 4.2 | | V |
| | Input voltage threshold when input current is reduced | VINDPM target =4.5V | | 4.5 | | V |
| | Input voltage threshold when input current is reduced | VINDPM target =4.7V | | 4.7 | | V |
| $V_{DPPM}$ | SYS voltage threshold when charge current is reduced | VBAT = 3.6V, VSYS = $V_{DPPM}$ + VBAT before charge current is reduced. | | 0.1 | | V |
| $V_{SYS_REG_ACCURACY}$ | Programmable SYS voltage regulation accuracy | VIN = 5V, VBAT = 3.6V, RSYS = 100ohm, SYS regulation target = 4.4V to 4.9V | -2 | | 2 | % |
| $V_{MINSYS}$ | Minimum SYS voltage when in battery tracking mode | VBAT < 3.6V | | 3.8 | | V |
| $V_{SYS_TRACK}$ | Voltage regulation threshold for SYS when VBAT >3.6V in battery tracking mode | VBAT = 4V, VSYS = VBAT + $V_{SYS_TRACK}$ | | 225 | | mV |
| $R_{SYS_PD}$ | SYS pull down resistance | $V_{SYS}$ = 3.6V | | 25 | | Ω |
| **BATTERY CHARGER** | | | | | | |
| $R_{ON_BAT}$ | Battery FET on-resistance | VBAT = 4.5V, IBAT =500mA | | 55 | 90 | mΩ |
| $R_{ON_IN}$ | Input FET on-resistance | IN = 5V, IIN = 1A | | 270 | 470 | mΩ |
| $V_{REG_RANGE}$ | Typical BAT charge voltage regulation range | 10mV steps, programmabe through $I^2C$ | 3.5 | | 4.65 | V |
| $V_{REG_ACC}$ | BAT charge voltage accuracy, summary for all settings | All VBATREG settings, typical measurement at VBATREG = 4.2V | –0.5 | | 0.5 | % |
| $I_{CHG_RANGE}$ | Typical charge current regulation range | $V_{OUT}$ > $V_{LOWV}$ | 5 | | 1000 | mA |
| $I_{CHG_ACC}$ | Charge current accuracy | VIN = 5V, Fastcharge >=40mA | –10 | | 10 | % |
| $I_{CHG_ACC}$ | Charge current accuracy | Fastcharge current = 40mA | 36 | 40 | 44 | mA |
| $I_{CHG_ACC}$ | Charge current accuracy | Fastcharge current = 630mA | 567 | 630 | 693 | mA |
| $I_{PRECHG}$ | Typical pre-charge current, as percentage of ICHG | $V_{OUT}$ < $V_{LOWV}$ | | 20 | | % |
| $I_{PRECHG_ACC}$ | Precharge current accuracy | Fastcharge current >=40mA | –10 | | 10 | % |
| $I_{TERM}$ | Typical termination current, as percentage of ICHG | $V_{OUT}$ = VBATREG | | 10 | | % of Icharge |
| $I_{TERM_ACC}$ | Termination current accuracy | IBAT = 3mA (IFCHG = 30mA) Tj = 25°C | –10 | | 10 | % |
| $I_{TERM_ACC}$ | Termination current accuracy | IBAT = 3mA (IFCHG = 30mA) Tj = 25°C | 2.7 | | 3.3 | mA |

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## 7.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. -40°C < TJ < 125°C unless otherwise noted. Typical data at TJ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{LOWV}$ | Pre-charge to fast-charge transition threshold | VLOWVSEL = 3.0V, VBAT rising | 2.9 | 3 | 3.1 | V |
| $V_{LOWV}$ | Pre-charge to fast-charge transition threshold | VLOWVSEL = 2.8V, VBAT rising | 2.7 | 2.8 | 2.9 | V |
| $V_{LOWV_HYS}$ | Battery LOWV hysteresis | All settings | | 100 | | mV |
| $V_{BUVLO}$ | Battery UVLO, VBAT falling | BUVLO setting = b000 | | 3 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b011 | | 2.8 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b100 | | 2.6 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b101 | | 2.4 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b110 | | 2.2 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b111 | | 2.0 | | V |
| $V_{BUVLO_HYS}$ | Battery UVLO hysteresis, VBAT rising | Any BUVLO Setting, value above VBAT, VIN = 5V | 110 | 150 | 190 | mV |
| $V_{BATPOR}$ | Battery only power up voltage, VBAT rising | -40C < Tj < 125C | 3.08 | 3.21 | 3.46 | V |
| $V_{RCH}$ | | BAT falling, VRCH bit = 0 | 75 | 100 | 130 | mV |
| | | BAT falling, VRCH bit = 1 | 175 | 200 | 230 | mV |
| $V_{BATSC}$ | Short on battery threshold for trickle charge, VBAT rising | | 1.6 | 1.8 | 2.0 | V |
| $V_{BATSC_HYS}$ | Battery short circuit voltage hysteresis | | | 200 | | mV |
| $I_{BATSC}$ | Trickle Charge Current | VBAT<$V_{BATSC}$ | | 8 | | mA |
| **TERMPERATURE REGULATION AND TEMPERATURE SHUTDOWN** | | | | | | |
| $T_{REG}$ | Typical junction temperature regulation | THERM_REG = 00 | | 100 | | °C |
| $T_{REG}$ | Typical junction temperature regulation | THERM_REG = 11 | | Disabled | | |
| $T_{SHUT_RISING}$ | Thermal shutdown rising threshold | Temperature increasing | | 150 | | °C |
| $T_{SHUT_FALLING}$ | Thermal shutdown falling threshold | Temperature decreasing | | 135 | | °C |
| **BATTERY NTC MONITOR** | | | | | | |
| $I_{TS_BIAS}$ | TS nominal bias current | | 36.5 | 38 | 39.5 | µA |
| $V_{T1_Entry}$ | Cold - 00 @ Approx. 0°C, default | VIN = 5V | 0.9575 | 1.0075 | 1.0575 | V |
| $V_{T2_Entry}$ | Cold - 01 @ Approx. 3°C | VIN = 5V | 0.8450 | 0.8900 | 0.9325 | V |
| $V_{T3_Entry}$ | Cold - 10 @ Approx. 5°C | VIN = 5V | 0.7775 | 0.8200 | 0.8600 | V |
| $V_{T4_Entry}$ | Cold - 11 @ Approx. -3°C | VIN = 5V | 1.0850 | 1.1425 | 1.2000 | V |
| $V_{T5_Entry}$ | Cool - 00 @ Approx. 10°C, default | VIN = 5V | 0.6350 | 0.6700 | 0.7025 | V |
| $V_{T6_Entry}$ | Warm - 00 @ Approx. 45°C, default | VIN = 5V | 0.1730 | 0.1850 | 0.198 | V |
| $V_{T7_Entry}$ | Hot - 00 @ Approx. 60°C, default | VIN = 5V | 0.1050 | 0.1150 | 0.1250 | V |
| $V_{T8_Entry}$ | Hot - 01 @ Approx. 65°C | VIN = 5V | 0.0875 | 0.0975 | 0.1075 | V |
| $V_{T9_Entry}$ | Hot - 10 @ Approx. 50°C | VIN = 5V | 0.1475 | 0.1575 | 0.1675 | V |
| $V_{T10_Entry}$ | Hot - 11 @ Approx. 45°C | VIN = 5V | 0.1750 | 0.1850 | 0.1950 | V |
| $V_{T1_Exit}$ | Cold - 00 @ Approx. 5°C, default | VIN = 5V | 0.7775 | 0.8200 | 0.8600 | V |
| $V_{T2_Exit}$ | Cold - 01 @ Approx. 8°C | VIN = 5V | 0.6875 | 0.7250 | 0.7600 | V |
| $V_{T3_Exit}$ | Cold - 10 @ Approx. 10°C | VIN = 5V | 0.6350 | 0.6700 | 0.7025 | V |
| $V_{T4_Exit}$ | Cold - 11 @ Approx. 2°C | VIN = 5V | 0.8800 | 0.9275 | 0.9725 | V |
| $V_{T5_Exit}$ | Cool - 00 @ Approx. 15°C, default | VIN = 5V | 0.5225 | 0.5500 | 0.5775 | V |


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## 7.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. -40°C < TJ < 125°C unless otherwise noted. Typical data at TJ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{T6_Exit}$ | Warm - 00 @ Approx. 41°C, default | VIN = 5V | 0.2080 | 0.2200 | 0.235 | V |
| $V_{T7_Exit}$ | Hot - 00 @ Approx. 55°C, default | VIN = 5V | 0.1250 | 0.1350 | 0.1450 | V |
| $V_{T8_Exit}$ | Hot - 01 @ Approx. 60°C | VIN = 5V | 0.1050 | 0.1150 | 0.1250 | V |
| $V_{T9_Exit}$ | Hot - 10 @ Approx. 45°C | VIN = 5V | 0.1750 | 0.1850 | 0.1950 | V |
| $V_{T10_Exit}$ | Hot - 11 @ Approx. 40°C | VIN = 5V | 0.2100 | 0.2200 | 0.23 | V |
| $V_{TS_ENZ}$ | TS monitoring enable threshold VTSMR<VTS_ENZ for TS function to be enabled | TS Rising, VIN = 5V | 1.8 | 2.1 | 2.8 | V |
| $V_{TS_CLAMP}$ | TS maximum voltage clamp | TS open-circuit (float), VIN = 5V | 2.2 | 2.8 | 3.3 | V |
| **PUSH BUTTON TIMERS AND THRESHOLDS** | | | | | | |
| $I_{TSMR}$ | Adapter present | | 36.5 | 38 | 39.5 | µA |
| $I_{TSMR}$ | Battery only mode | | | 60 | | µA |
| $V_{TSMR}$ | TSMR voltage to detect a button press event, battery only mode | | | | 90 | mV |
| $V_{TSMR}$ | TSMR voltage to detect a button press event, adapter present | | | | 90 | mV |
| $t_{WAKE1}$ | WAKE1 Timer. Time from TSMR low detection | MR_WAKE1_TIMER = 0 | | 300 | | ms |
| | | MR_WAKE1_TIMER = 1 | | 1 | | s |
| $t_{WAKE2}$ | WAKE2 Timer. Time from TSMR low detection | MR_WAKE2_TIMER = 0 | | 2 | | s |
| | | MR_WAKE2_TIMER = 1 | | 3 | | s |
| $t_{RESET_WARN}$ | RESET_WARN Timer. Time prior to HW RESET | MR_RESET_WARN = 0 | 0.9 | 1 | 1.1 | s |
| $t_{LPRESS}$ | Long Press timer. Time from button press detection to long press action. | MR_LPRESS = 00 | 4.5 | 5 | 5.5 | s |
| | | MR_LPRESS = 01 | 9 | 10 | 11 | s |
| | | MR_LPRESS = 10 | 13.5 | 15 | 16.5 | s |
| | | MR_LPRESS = 11 | 18 | 20 | 22 | s |
| $t_{RESTART(AUTOWAKE)}$ | RESTART Timer. Time from HW Reset to SYS power up | AUTOWAKE = 00 | | 0.5 | | s |
| | | AUTOWAKE = 01 | | 1 | | s |
| | | AUTOWAKE = 10 | | 2 | | s |
| | | AUTOWAKE = 11 | | 4 | | s |
| **BATTERY CHARGING TIMERS** | | | | | | |
| $t_{MAXCHG}$ | Charge safety timer | Programmable range | 180 | | 720 | min |
| $t_{PRECHG}$ | Precharge safety timer | | | 0.25 * $t_{MAXCHG}$ | | |
| **I2C INTERFACE** | | | | | | |
| $V_{IL}$ | Input low threshold level | VPULLUP = 1.8V, SDA and SCL | | | 0.4 | V |
| $V_{IH}$ | Input high threshold level | VPULLUP = 1.8V, SDA and SCL | 1.3 | | | V |
| $V_{OL}$ | Output low threshold level | IL = 5mA, sink current, $V_{PULLUP}$ =1.8V | | | 0.4 | V |
| $I_{LKG}$ | High-Level leakage current | $V_{PULLUP}$ = 1.8V | | | 1 | µA |
| **LOGIC PINS** | | | | | | |
| $V_{OL}$ | Output low threshold level | IL = 5mA, sink current, $V_{PULLUP}$ =3.3V, /INT pin | | | 0.4 | V |
| $I_{LKG}$ | High-Level leakage current | $V_{PULLUP}$ = 3.3V, /INT pin | | | 1 | µA |

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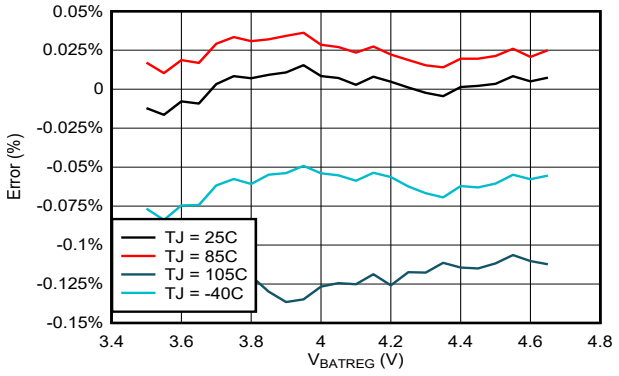
## 7.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| $t_{VIN_OVPZ_DGL}$ | VIN_OVP deglitch, VIN falling | | 30 | | ms |
| $t_{SLEEP_DGL}$ | Deglitch time to enter SLEEP, VIN falling | | 64 | | µs |
| **BATTERY CHARGER** | | | | | |
| $t_{REC_SC}$ | Recovery time, BATOCP during Discharge Mode | | 250 | | ms |
| $t_{RETRY_SC}$ | Retry window for SYS or BAT short circuit recovery(BATOCP) | | 2 | | s |
| $t_{BUVLO}$ | Deglitch time to disconnect the BATFET when VBAT < $V_{BUVLO}$ setting | | 60 | | µs |
| $t_{TS_DUTY_ON}$ | TS turnon-time (battery only mode) | | 4 | | ms |
| $t_{TS_DUTY_OFF}$ | TS turnoff time (battery only mode) | | 196 | | ms |
| **DIGITAL CLOCK, WATCHDOG and PUSHBUTTON** | | | | | |
| $t_{WDOG}$ | I2C interface reset timer, adjustable | 40 | 160 | Disabled | s |
| $t_{I2CRESET}$ | I2C interface inactive reset timer | | 500 | | ms |
| $t_{SHIPWAKE}$ | Wake timer to count for shipmode (WAKE2 DefaultTimer) | | 2 | | s |


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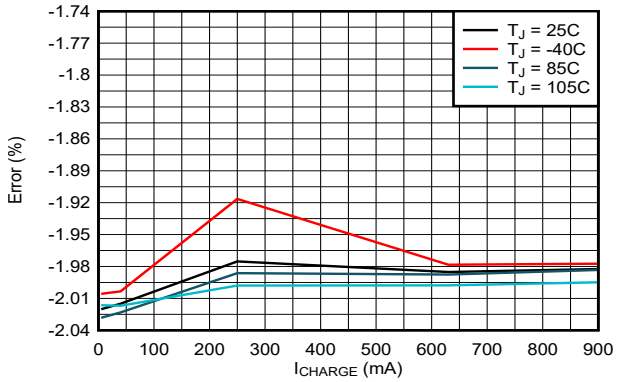
## 7.7 Typical Characteristics

VIN = 5 V, $C_{IN}$ = 2.2 µF, $C_{OUT}$ = 10 µF, $C_{BAT}$ = 1 µF (unless otherwise specified)



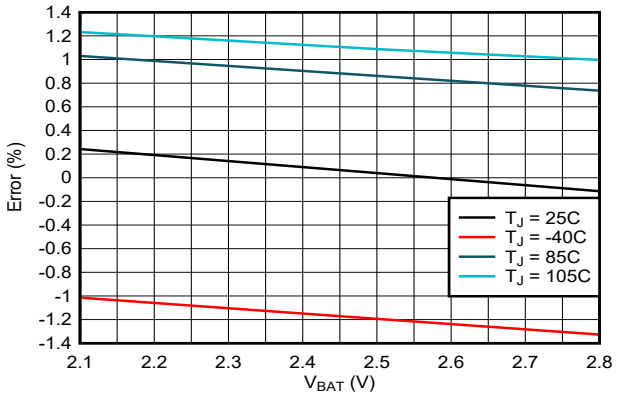

VIN = 5 V

**Figure 7-1. Battery Regulation Voltage Accurary vs. VBATREG Setting**



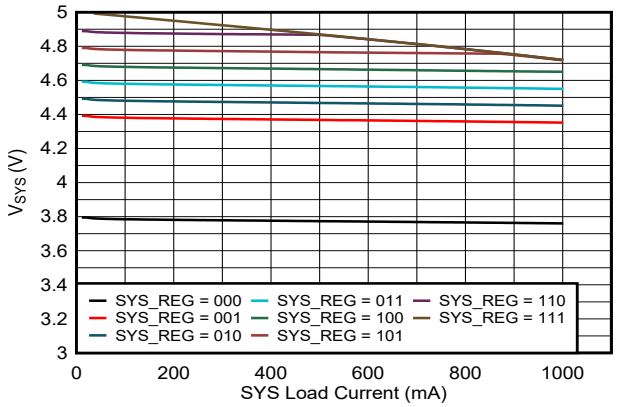

VIN = 5 V VBAT = 3.1 V

**Figure 7-2. Charge Current Accuracy vs. ICHARGE Setting**



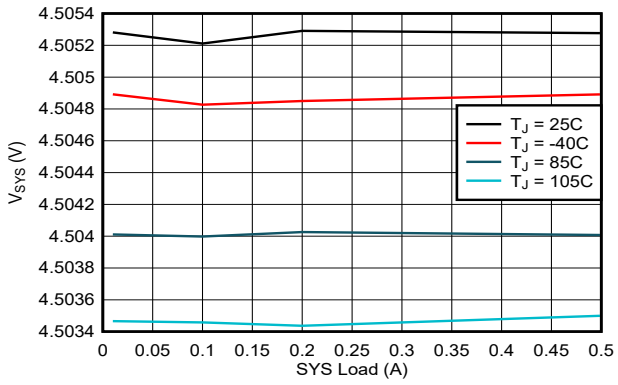

VIN = 5 V ICHG = 100 mA

**Figure 7-3. Precharge Accuracy vs Battery Voltage**




VIN = 5 V VBAT = 0 V

**Figure 7-4. SYS Load Regulation**




VIN = 5 V SYS_REG_CTRL = 010 (4.5 V)

**Figure 7-5. SYS Load Regulation vs. Temperature**

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# 8 Detailed Description

## 8.1 Overview

The BQ25180 integrates a linear charger that allows the battery to be charged with a programmable charge current of up to 1 A. In addition to the charge current, other charging parameters can be programmed through $I^2C$ such as the precharge, termination, battery regulation voltage, and input current limit.

The power path allows the system to be powered from a regulated output, SYS, even when the battery is deeply discharged or charging, by drawing power from IN pin. It also prioritizes the system load in SYS, reducing the charging current, if necessary, in order support the load when input power is limited. If the input supply is removed and the battery voltage level is above $V_{BUVLO}$, SYS will automatically and seamlessly switch to battery power.

Charging is done through the internal battery MOSFET. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, thermal regulation, $V_{DPPM}$, and $V_{INDPM}$. During the charging process, all loops are enabled and the one that is dominant takes control.

The device supports multiple battery chemistries for single-cell applications, through adjustable battery regulation voltage regulation ($V_{BATREG}$) and charge current ($I_{CHG}$) options.

### 8.1.1 Battery Charging Process

When a valid input source is connected ($V_{IN}$ > $V_{UVLO}$ and $V_{BAT}$+$V_{SLEEPZ}$ ≤ $V_{IN}$ < $V_{IN_OVP}$), the state of the CHARGE_DISABLE bit and the TSMR pin determines whether a charge cycle is initiated. When the CHARGE_DISABLE bit is set to disable charging, $V_{HOT}$ < $V_{TS}$ < $V_{COLD}$ and a valid input source is connected, the battery discharge FET is turned off, preventing any charging of the battery. Note that supplement behavior is independent of the CHARGE_DISABLE bit.

The following figure illustrates a typical charge cycle.


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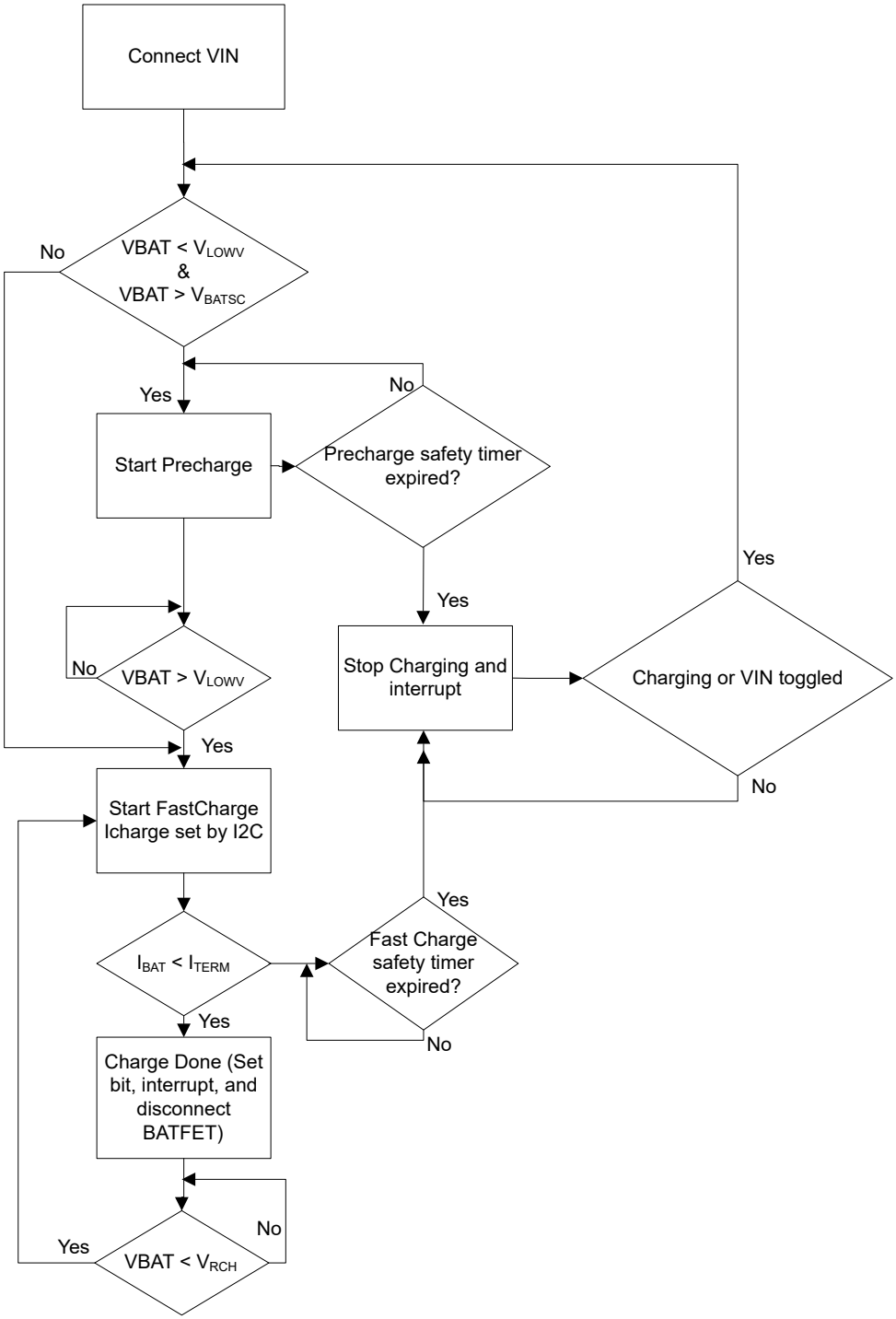



**Figure 8-1. Charger Flow Diagram**

### *8.1.1.1 Trickle Charge*

In order to prevent damage to the battery, the device will charge the battery at a much lower current level (IBATSC) when the battery voltage (VBAT) is below the VBATSC threshold. During trickle charge, the device still counts against the precharge safety timer. Rather trickle charge and precharge are counting against the same duration of 25% of the fast charge timer.

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#### 8.1.1.2 Precharge

When battery voltage is above the $V_{BATSC}$ but lower than $V_{LOWV}$ threshold, the battery is charged with the precharge current level. The precharge current (IPRECHARGE) can be programmed through $I^2C$ and can be adjusted by the host. Once the battery voltage reaches $V_{LOWV}$, the charger will then operate in Fast Charge mode, charging the battery at ICHG.

During precharge, the safety timer is set to 25% of the safety timer value during fast charge. In the case where termination is disabled, precharge current is set to 20% of fast charge current setting.

#### 8.1.1.3 Fast Charge

The charger has two main control loops that control charging when $V_{BAT} > V_{LOWV}$: the Constant Current (CC) and Constant Voltage (CV) loops. When the CC loop is dominant, the battery is charged at the maximum charge current level $I_{CHG}$, unless there is a TS fault condition (JEITA operation), VINDPM is active, thermal regulation or DPPM is active. (See respective sections for details on these modes of operation). Once the battery voltage approaches the battery regulation target, the CV loops becomes more dominant and the charging current starts tapering off. Once the charging current reaches the termination current ($I_{TERM}$) the charge is done, Charge_done status is set. If the $I^2C$ setting of VBATREG is set higher than 4.65 V, the battery regulation voltage is still maintained at 4.65 V. The device will switch to fastcharge mode based on VLOWV setting on the register map.

#### 8.1.1.4 Termination

The device will automatically terminate charging once the charge current reaches ITERM, which is programmable through $I^2C$. After termination the charger will operate in high impedance mode, disabling the BATFET to disconnect the battery. Power is provided to the system (SYS) by IN supply as long as $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT} + V_{SLEEPZ}$ and $V_{IN} < V_{IN_OVP}$.

Termination is only enabled when the charger CV loop is active in fast charge operation. Termination is disabled if the charge current reaches $I_{TERM}$ while the VINDPM, DPPM, or thermal regulation loops are active. The charger will only go into the termination when the current drops to $I_{TERM}$ due to the battery reaching the target voltage and not due to the charge current limitation imposed by the previously mentioned controlled loops.

Post termination, the battery FET is disabled and the voltage on BAT pin is monitored to check if it has dropped to the VRCH threshold. If it does, a new charge cycle is established. The safety timers are reset. During charging or even when charge is done, a higher SYS load will be supported through the supplement operation.


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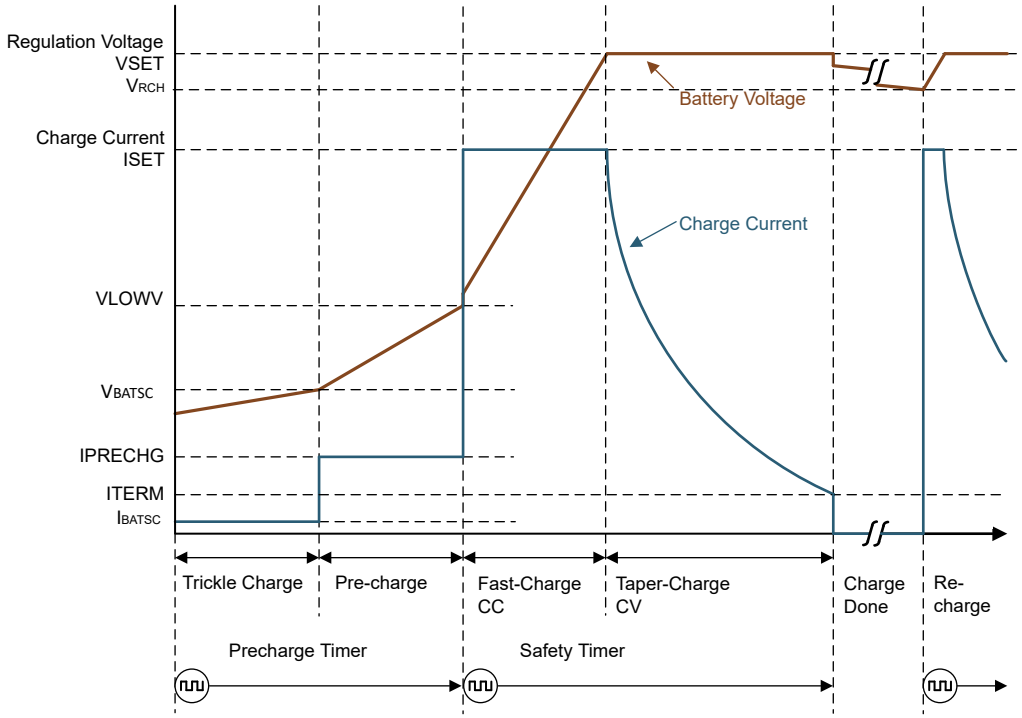



**Figure 8-2. Typical Charging Profile of a Battery**

## 8.2 Functional Block Diagram

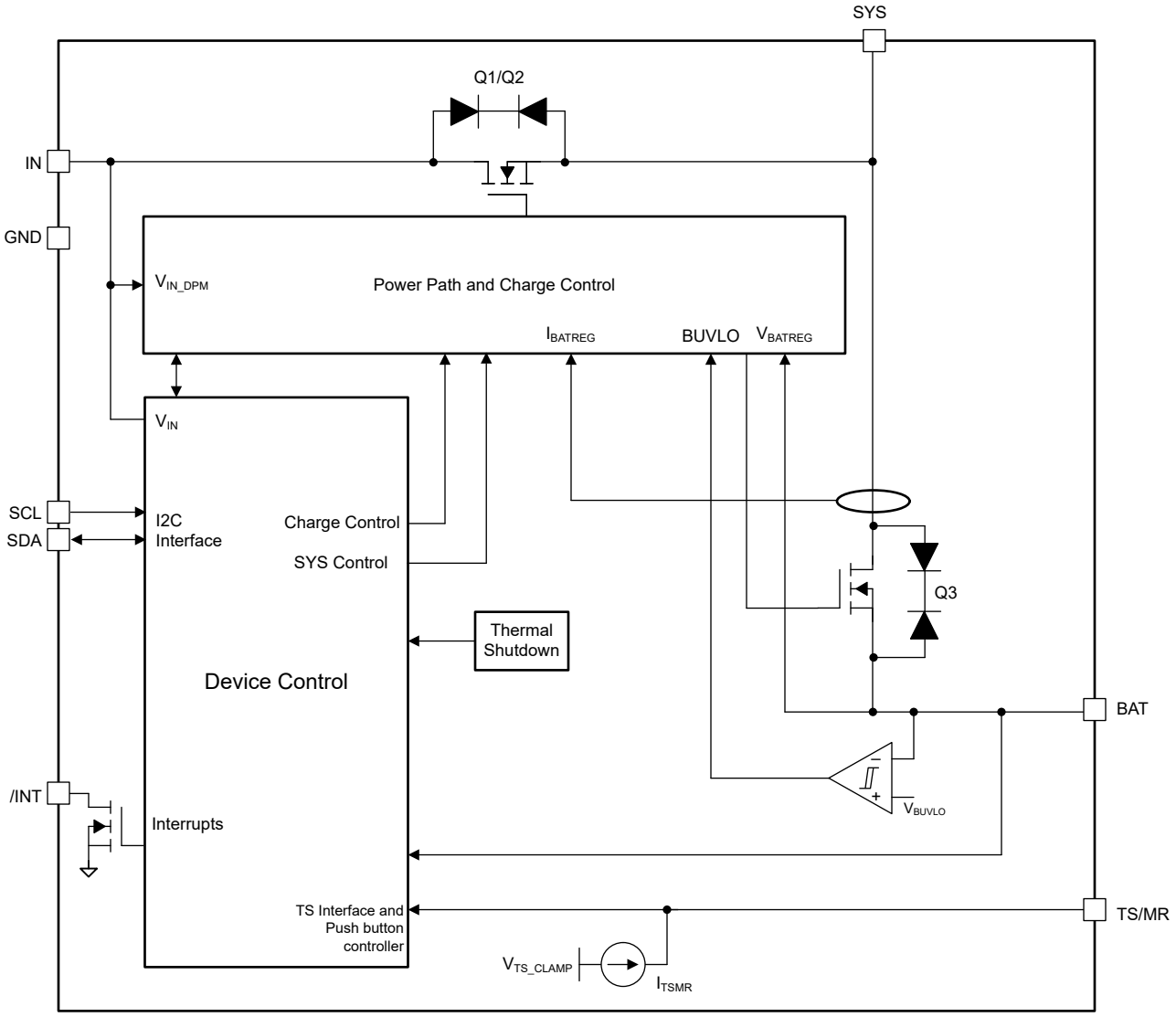



**Figure 8-3. Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Input Voltage Based Dynamic Power Management (VINDPM)

The VINDPM loop prevents the input voltage from collapsing to a point where charging could be interrupted due to adapter voltage crashing below VINDPM value. This is done by reducing the current drawn by the charger enough to keep $V_{IN}$ > VINDPM setting.

During the normal charging process, if the input power source is not able to support the programmed or default charging current and system load, the supply voltage decreases. Once the supply drops to VINDPM, the input DPM current and voltage loops will reduce the input current through the blocking FETs Q1 and Q2 to prevent the further drop of the supply. The VINDPM threshold is programmable through the $I^2C$ register and can be completely disabled. This is set through the VINDPM_0 and VINDPM_1 selection bits. When the device enters this mode, the charge current may be lower than the set value and the VINDPM_ACTIVE_STAT bit is set. If the 2x timer is set through the 2XTMR_EN bit, the safety timer is extended while VINDPM is active. Additionally, termination is disabled when VINDPM is active.


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### 8.3.2 Dynamic Power Path Management Mode (DPPM)

With a valid input source connected, the power path management circuitry monitors the input voltage and current continuously. The current into IN is shared at SYS between charging the battery and powering the system load at SYS. If the sum of the charging and load currents exceeds the preset maximum input current, the input DPM loop reduces input current. If SYS drops below the DPPM voltage threshold, the charging current is reduced by the DPPM loop through the BATFET (Q3). If SYS falls below the supplement mode threshold after BATFET charging current is reduced to zero, the part will enter supplement mode. SYS voltage is maintained above battery voltage when the DPPM loop is in control. Battery termination is disabled when the DPPM loop is active.

The VDPPM threshold is typically 100 mV above VBAT. The VDPPM disable bit (VDPPM_DIS = b1) will allow the charger to operate with lower headroom on VSYS. In VBAT tracking mode where VSYS is VBAT+225 mV, disabling this bit will have no effect.

### 8.3.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at SYS reduces further. When the SYS voltage drops below the battery voltage to $V_{BSUP1}$, the battery supplements the system load. The battery stops supplementing the system load when the voltage on the SYS pin rises within the battery voltage to $V_{BSUP2}$. During supplement mode, the battery supplement current is not regulated, however, the BATOCP protection circuit is active if enabled. Battery termination is disabled while in supplement mode. Battery voltage has to be higher than the battery undervoltage lockout threshold (VBUVLO) in order to supplement the system.

### 8.3.4 SYS Power Control (SYS_MODE bit control)

The device also offers the option to control SYS through the $I^2C$ SYS_MODE bits. These bits can force SYS to be supplied by BAT instead of IN (even if $V_{IN} > V_{BAT} + V_{SLEEP}$), disconnect SYS from either supply, pull SYS down or leave it floating. The table below shows the device behavior based on SYS_MODE setting:

**Table 8-1. Settings**

| SYS_MODE | DESCRIPTION | SYS SUPPLY | SYS PULLDOWN |
|---|---|---|---|
| 00 | Normal Operation | IN or BAT | Off except during HW reset |
| 01 | Force BAT power (IN disconnected) | BAT | Off except during HW reset |
| 10 | SYS Off –Floating | None | Off |
| 11 | SYS Off – Pulled Down | None | On |

#### SYS_MODE = 00

This is the default state/normal operation of the device. SYS will be powered from IN if $V_{IN} > V_{UVLO}$, $V_{IN} >$ VBAT + $V_{SLEEPZ}$, and $V_{IN} < V_{IN_OVP}$. SYS will powered by BAT if these conditions are not met. SYS will only be disconnected from IN or BAT and pulled down when a HW Reset occurs or the device goes into Ship mode.

#### SYS_MODE = 01

When this configuration is set, SYS will be powered by BAT if $V_{BAT} > V_{BUVLO}$ regardless of $V_{IN}$ state. This allows the host to minimize the current draw from the adapter while it is still connected as needed in the system. If SYS_MODE = 01 is set while $V_{BAT} < V_{BUVLO}$, the SYS_MODE = 01 setting will be ignored and the device will go to SYS_MODE = 00. In the same manner, if the adapter ($V_{IN}$) is removed and then connected the device will also switch to SYS_MODE = 00. This prevents the device from needing a POR in order to restore power to the system thereby allowing battery charging. If SYS_MODE = 01 is set during charging, charging will be stopped and the battery will start to provide power to SYS as needed. The behavior is similar to that when the input adapter is disconnected.

#### SYS_MODE = 10

When this configuration is set, SYS will be disconnected and left floating. The device remains on and active. Toggling $V_{IN}$($V_{IN}$ <$V_{INUVLO}$) will reset SYS_MODE to 00.

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**SYS_MODE = 11**

When this configuration is set, SYS will be disconnected and pulled down to ground. Toggling $V_{IN}$ will reset SYS_MODE to 00.

#### *8.3.4.1 SYS Pulldown Control*

The device has an internal pulldown on the SYS pin which is enabled in the following cases:

**Table 8-2. States**

| STATE | NOTES |
|---|---|
| Shipmode | Pulldown on SYS is enabled once the device enters shipmode and after disconnecting the BATFET |
| HW_RESET | Pulldown on SYS is enabled after the BATFET and input blocking FETs are disconnected and retained until the autowake timer expires |
| SYS_MODE = 11 (SYS pulldown mode) | Pulldown on SYS is enabled after the BATFET and input blocking FETs are disconnected and retained until either an $I^2C$ transaction is issued to change SYS_MODE or VIN is toggled. |

### 8.3.5 SYS Regulation

The device includes a SYS voltage regulation loop. By regulating the SYS voltage the device prevents downstream devices connected to SYS from being exposed to voltages as high as $V_{IN_OVP}$. SYS regulation is only active when $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT} + V_{SLEEPZ}$ and $V_{IN} < V_{IN_OVP}$ rather than meeting the VIN_Powergood condition.

The SYS voltage regulation target can be controlled through the SYS_REG_CTRL_2:0 bits in the SYS_REG register to either track the battery, set to a fixed voltage, or enable pass through modes.

In battery tracking mode, the minimum voltage is at the $V_{MINSYS}$ value for a battery < 3.6 V. As battery voltage increases VSYS is regulated to 225 mV above battery. If $V_{IN} < V_{MINSYS}$ and VIN_Powergood is still active, then SYS will be in dropout.

In fixed voltage mode, SYS voltage is regulated to a target set by the host ranging from 4.4 V to 4.9 V. If $V_{IN}$ voltage is less than the SYS target voltage, then the device will be in dropout mode.

In pass through mode, the SYS path is unregulated and the $V_{SYS}$ voltage is equal to $V_{IN}$.

**Table 8-3. SYS Voltage Regulation Settings**

| SYS_REG_CTRL | VSYS TARGET |
|---|---|
| 000 | VBAT + 225 mV (3.8 V minimum) |
| 001 | 4.4 |
| 010 (default) | 4.5 |
| 011 | 4.6 |
| 100 | 4.7 |
| 101 | 4.8 |
| 110 | 4.9 |
| 111 | Pass through |

### 8.3.6 ILIM Control

The input current limit can be controlled through $I^2C$ by selecting the the ILIM bits.

If the ILIM clamp is active, the ILIM_ACTIVE_STAT bit is set.


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MASK_ILIM will prevent an interrupt from being issued but does not override the ILIM behavior itself. The ILIM value can be programmed dynamically through the $I^2C$ by the host. The ILIM settings of 100mA and 500mA are designed to be the maximum value to support standard systems.

### 8.3.7 Protection Mechanisms

#### *8.3.7.1 Input Overvoltage Protection*

Input overvoltage protection protects the device and downstream components connected to SYS, and BAT against damage from overvoltage on the input supply. When VIN > $V_{IN_OVP}$, a VIN overvoltage condition is determined to exist. During the VIN overvoltage condition, the device turns the input FET OFF, battery discharge FET ON, sends a single 128-µs pulse on INT, and the fault bit (VIN_OVP_FAULT_FLAG) is updated over $I^2C$. The VIN_PGOOD_STAT bit also is affected by the VIN overvoltage condition as the VIN powergood condition will fail. Once the VIN overvoltage condition is removed ($V_{IN} \leq V_{IN_OVP}$ - $V_{IN_OV_HYS}$ ), the VIN_OVP_STAT bit is cleared and the device returns to normal operation. Thereafter, a VIN powergood condition is determined if VIN > VBAT + $V_{SLEEPZ}$ and VIN > $V_{IN_UVLO}$.

#### *8.3.7.2 Battery Undervoltage Lockout*

In order to prevent deep discharge of the battery the device integrates a battery undervoltage lockout feature which will disengage the BAT to SYS path when voltage at the battery drops below the programmed BUVLO setting present in the CHARGERCTRL1 register. BUVLO status can also be read when a valid voltage on VIN is present.

#### *8.3.7.3 System Overvoltage Protection*

The system overvoltage protection is to prevent SYS from overshooting to a high voltage due to the input supply. SYS_OVP will momentarily disconnect the blocking FETs and re-engage when the thresholds have dropped to less than the SYS_OVP_FALLING threshold.

The SYS_OVP_RISING threshold is typically 105% of the target SYS voltage and the SYS_OVP_FALLING threshold is 102.5% of the target SYS voltage.

#### *8.3.7.4 System Short Protection*

When a valid adapter is connected to the device, the device turns ON the input blocking FET for 5 ms and it detects the SYS pin to be shorted (voltage on SYS <1.6V). In this scenario, the device will turn OFF the input FET for ~200 µs and turn it back ON for 5 ms for SYS to rise above 1.6V. If after 10 tries, the SYS short still persists, the device will turn OFF SYS until adapter is connected again.

#### *8.3.7.5 Battery Overcurrent Protection*

In order to protect the device from overcurrent and prevent excessive battery discharge current, the device detects if the current on the battery FET exceeds IBAT_OCP. If the BATOCP limit is reached, the battery discharge FET is turned off and the device starts operating in hiccup mode, re-enabling the BATFET $t_{REC_SC}$ (250 ms) after being turned OFF by the overcurrent condition. If the overcurrent condition is triggered upon retry for 4 to 7 consecutive times in a 2-s window, the BATFET shall then remain off until a valid VIN is connected (VIN = VIN_POWERGOOD). If the overcurrent condition and hiccup operation occur while in supplement mode where VIN is already present, VIN must be toggled in order for the BATFET to be enabled and start another detection cycle.

#### *8.3.7.6 Safety Timer and Watchdog Timer*

At the beginning of each charge cycle mode (Precharge or Fast Charge), the device starts the respective mode safety timer. If charging has not terminated before the programmed safety time, $t_{MAXCHG}$ expires or the device does not exit the precharge mode before $t_{PRECHG}$ expires, charging is disabled. The precharge safety time, $t_{PRECHG}$, is 25% of $t_{MAXCHG}$. When a safety timer fault occurs, a single 128-µs pulse is sent on the INT pin and the STAT and FAULT bits of the status registers are updated over $I^2C$.

The charge enable bit or input power must be toggled in order to clear the safety timer fault.

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If the safety timer has expired, the device will produce an interrupt and update the SAFETY_TMR_FAULT_FLAG bit on the register map. The safety timer duration is programmable using the SAFETY_TIMER_1:0 bits. When the safety timer is active, changing the safety timer duration resets the safety timer. The device also contains a 2XTMR_EN bit that doubles the safety timer duration to prevent premature safety timer expiration when the charge current is reduced by a high load on SYS (DPM operation- causing VDPPM to be enabled), VINDPM, thermal regulation, or a NTC (JEITA) condition. When the 2XTMR_EN bit is set, the timer is allowed to run at half speed when any loop is active other than CC or CV. In the event where during CC mode the battery voltage drops to push the charger into precharge mode, (due to a large load on battery, thermal events, and so forth) the safety timer will reset counting through precharge and then resetting the fast charge safety timer. If the device entered battery supplement mode while in precharge, CC or CV mode, while the charger is not disabled, the device will suspend the safety timer until charging can resume again. This prevents the safety timer from resetting when a supplement condition is caused.

In addition to the safety timer, the device contains a watchdog timer that monitors the host through the $I^2C$ interface. The watchdog timer is enabled by default and may be disabled by the host through an $I^2C$ transaction. Once the initial transaction is received, the watchdog timer is started. The watchdog timer is reset by any transaction by the host using the $I^2C$ interface. If the watchdog timer expires without a reset from the $I^2C$ interface, all charger parameters registers (ICHG, IPRECHARGE, ITERM,VLOWV, and so forth) are reset to the default values. The watchdog timer can be set through the WATCHDOG_SEL_1:0 bits either in battery only mode or when an adapter is present.

**Table 8-4. Watchdog Settings**

| WATCHDOG_SEL_1:0 | ACTION |
|---|---|
| 00 | Device will only perform a software reset after 160s of the last $I^2C$ transaction |
| 01 | Device will issue a HW_Reset after 160s of last $I^2C$ transation |
| 10 | Device will issue a HW_Reset after 40s of the last $I^2C$ transaction |
| 11 | Watchdog functionality is completely disabled |

#### *8.3.7.7 Thermal Protection and Thermal Regulation*

During operation, to protect the device from damage due to overheating, the junction temperature of the die, $T_J$, is monitored. When $T_J$ reaches $T_{SHUT_RISING}$, the device stops charging operation and VSYS is shutdown. If in the case where $T_J > T_{SHUT_RISING}$ prior to power being applied to the device (either battery or adapter), the input FET or BATFET will not turn ON, regardless of the TSMR pin. Thereafter if temperature falls below $T_{SHUT_FALLING}$, the device will automatically power up if VIN is present or if in battery only mode.

During the charging process, to prevent overheating in the device, the device monitors the junction temperature of the die and reduces the charging current once $T_J$ reaches the thermal regulation threshold ($T_{REG}$) based on bits set by the THERM_REG setting. If the charge current is reduced to 0, the battery supplies the current needed to supply the SYS output. Thermal regulation can be disabled through $I^2C$.

Ensure that system power dissipation is under the limit of the device. The power dissipated by the device can be calculated using the following equation:

$$P_{DISS} = P_{SYS} + P_{BAT}$$

Where:

$$P_{SYS} = (V_{IN} – V_{SYS}) * I_{IN}$$

$$P_{BAT} = (V_{SYS} – V_{BAT}) * I_{BAT}$$

The die junction temperature, $T_J$, can be estimated based on the expected board performance using the following equation:

$$T_J = T_A + \theta_{JA} * P_{DISS}$$

$\theta_{JA}$ is largely driven by board layout. For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics Application Report*. Under typical conditions, the time spent in this state is very short.


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### 8.3.8 Pushbutton Wake and Reset Input

The pushbutton function implemented through the TSMR pin has three main functions. First, it serves as a means to wake the device from ultra-low power modes like ship mode. Second, it serves as a short button press detector, sending an interrupt to the host when the button driving the TSMR pin has been pressed for Wake1, Wake2, or long press durations. This allows the implementation of different functions in the end application such as menu selection and control. Finally it serves as a means to get the device into ship mode or reset the system by performing a power cycle/ hardware reset (shut down SYS and automatically powering it back on) after detecting a long button press. The timing for the short and long button press duration is programmable through $I^2C$ for added flexibility and allows system designers to customize the end user experience of a specific application. Note that if a specific timer duration is changed through $I^2C$ while that timer is active and has not expired, the new programmed value will be ignored until the timer expires and/or is reset by new push button action. In battery only mode the device will automatically pulse the TSMR current source ON for $t_{TS_DUTY_ON}$ duration and turn it OFF for $t_{TS_DUTY_OFF}$ duration to check if a button is pressed. If a button press is registered, the device will begin counting against Wake1, Wake2 or long press durations. This button press detection routine in battery only mode is run as long as it is enabled by the EN_PUSH bit. When a valid adapter is present, the TSMR current source is always ON to monitor charging.

#### *8.3.8.1 Pushbutton Wake or Short Button Press Functions*

There are two programmable wake or short button press timers, WAKE1 and WAKE2. There are no specific actions taken by the $t_{WAKE1}$ or $t_{WAKE2}$ durations other than issuing an interrupt and updating the wake registers. For a wake from shipmode event when the button press is enabled, the push button has to be low for $t_{shipwake}$ before the device can turn ON the SYS rail.

In the case where a valid $V_{IN}$ ($V_{IN}$ > $V_{UVLO}$) is connected prior to the $t_{shipwake}$ timer expiring, the device will exit shipmode immediately regardless of the TS/MR or wake timer state. Refer to Section 8.5 for more details.

#### *8.3.8.2 Pushbutton Reset or Long Button Press Functions*

Depending on the configuration set on the pushbutton long press action register bits, the device will perform a shipmode entry or hardware reset or completely ignore the long button press action.

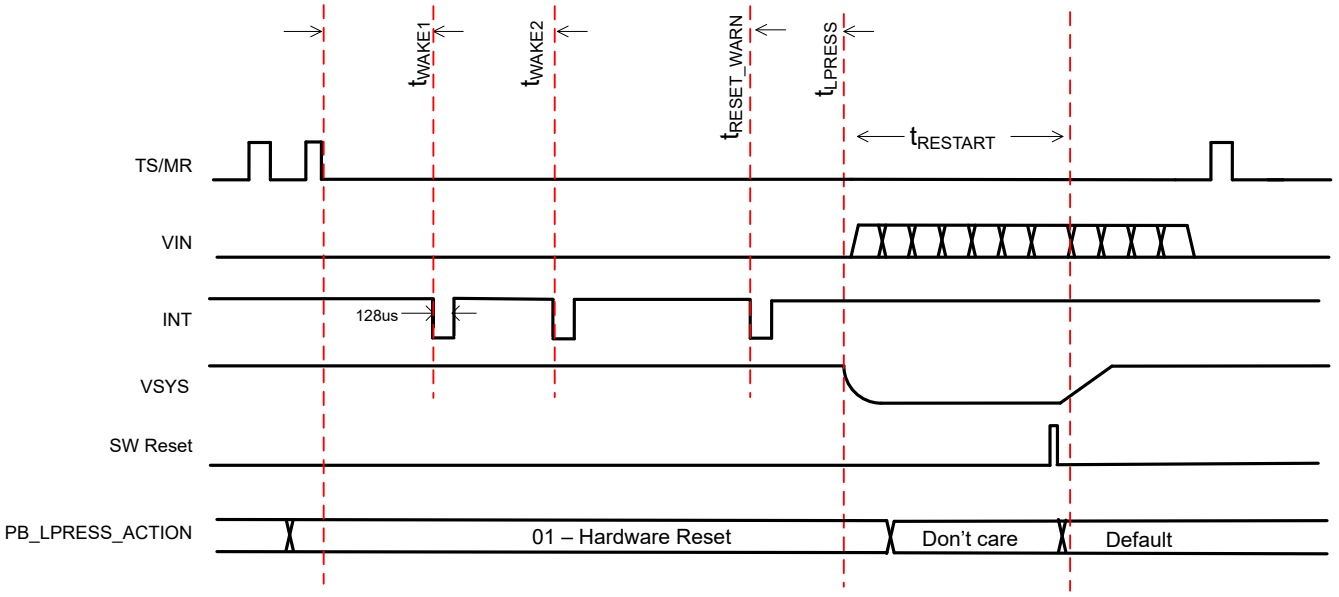



**Figure 8-4. Pushbutton Long Press Reset**

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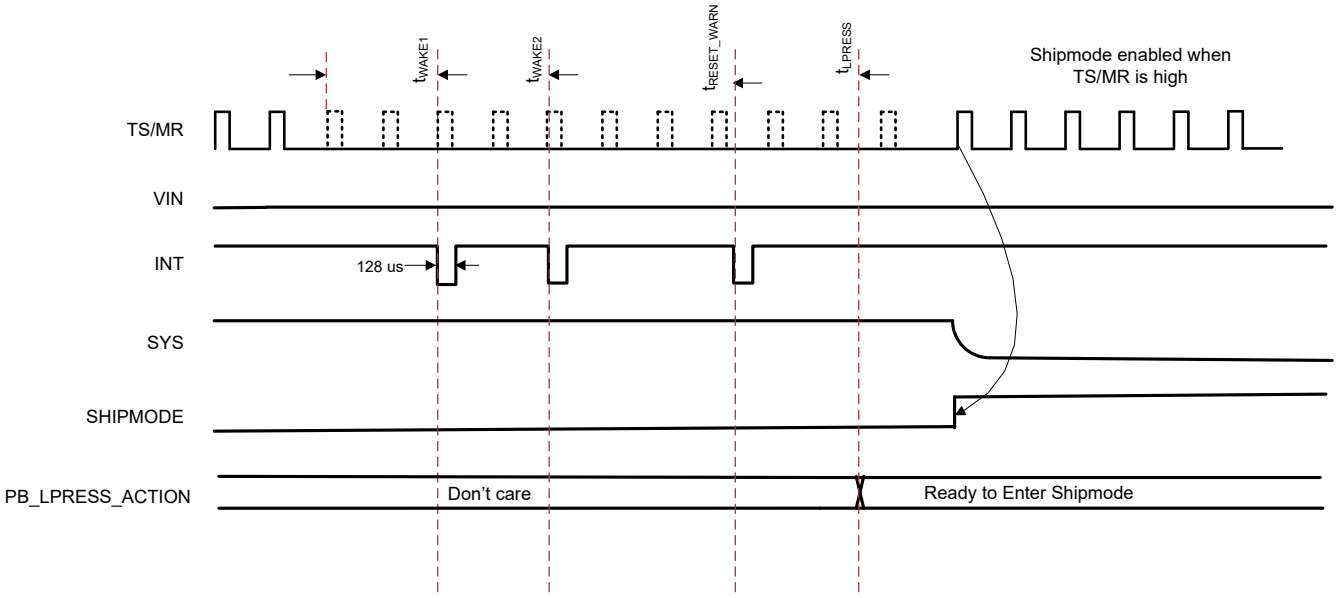



**Figure 8-5. Pushbutton Long Press Shipmode**

### 8.3.9 15-Second Timeout for HW Reset

Based on the I²C register bit WATCHDOG_15S_ENABLE the device can perform a HW reset/power cycle in the same manner a long button press or HW_RESET would. This 15-second watchdog or timeout is gated upon $V_{IN} > V_{VBAT} + V_{SLEEPZ}$ so that the HW reset would only occur if the host does not respond after a charger is connected and VIN_PGOOD_STAT is set.

If the charger is connected and the host responds before the 15-second watchdog expires, the part continues in normal operation and starts the normal 50-second watchdog timer if enabled. The 15-second watchdog may be enabled/disabled through I²C with the WATCHDOG_15S_ENABLE bit.

### 8.3.10 Hardware Reset

The device is capable of a hardware reset to completely powercycle the system. This is partcularly useful when a soft reset on the MCU or host fails to work. Below is a sequence of events during a hadware reset:

1. Turn OFF (if adapter is present) input blocking FET (Q1/Q2)
2. Turn OFF battery FET (Q3)
3. Engage pulldown on SYS
4. Start the Autowake timer
5. Once the Autowake timer expires, disconnect the pulldown on SYS
6. Reset all registers to default
7. Turn ON battery FET and input FET (if applicable)

### 8.3.11 Software Reset

When a software reset is issued either through a watchdog action configurable through the WATCHDOG_SEL bits or register reset configurable through the REG_RST bit, the device will reset all of the registers to the defaults. Any bits loaded through OTP memory are also loaded. If the device was waiting to go to shipmode (all conditions for entering ship are fulfilled except adapter removal), a hardware or software reset will cancel the pending shipmode request. If the shipmode request was written through I²C, the host can cancel the ship entry by clearing the bit before shipmode entry has happened.

### 8.3.12 Interrupt Indicator (/INT) Pin

The device contains an open-drain output that signals its status and is valid only after the device has completed start-up into a valid state. If the part starts into a fault, interrupts will not be sent.


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The /INT pin is normally in high impedance and is pulled low for 128 µs when an interrupt condition occurs. When a fault or status change occurs or any other condition that generates an interrupt, a 128-µs pulse (/INT pin pulled down) is sent on /INT to notify the host.

Interrupts can be masked through $I^2C$. If the interrupt condition occurs while the interrupt is masked an interrupt pulse will not be sent. If the interrupt is unmasked while the fault condition is still present, an interrupt pulse will not be sent until the /INT trigger condition occurs while unmasked. Below are a list of interrupts that can be masked through $I^2C$.

**Table 8-5. Mask Bit**

| MASK BIT | ACTION |
|---|---|
| ILIM_INT_MASK | Do not issue an /INT pulse when ILIM limiting occurs |
| VDPM_INT_MASK | Do not issue an /INT pulse when VINDPM or DDPM is active |
| TS_INT_MASK | Do not issue an /INT pulse when any of the TS events have occured. |
| TREG_INT_MASK | Do not issue an /INT pulse when TREG is actively reducing the current |
| PG_INT_MASK | Do not issue an /INT pulse when VIN meets VIN_PG condition |
| BAT_INT_MASK | Do not issue an /INT pulse when BATOCP or BUVLO event is triggered |
| CHG_STATUS_INT_MASK | Do not send an interrupt anytime there is a charging status change. |

### 8.3.13 External NTC Monitoring (TS)

#### *8.3.13.1 TS Biasing and Function*

The device can be configured to meet JEITA requirements or a simpler HOT/COLD function only. Additionally, the TS charger control function can be disabled through the TS_EN bit. This will only disable the TS charge action but the faults are still reported based on the TS voltage. To satisfy the JEITA requirements, four temperature thresholds are monitored: cold battery threshold, cool battery threshold, warm battery threshold, and hot battery threshold. These temperatures correspond to the VCOLD, VCOOL, VWARM, and VHOT thresholds in the Electrical Characteristics table. Charging and safety timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$. When $V_{COOL} < V_{TS} < V_{COLD}$, the charging current is reduced to the value programmed in the TS_Setting register/bit TS_ICHG_0. When $V_{HOT} < V_{TS} < V_{WARM}$, the battery regulation voltage is reduced by 100 mV or 200 mV based on the value programmed in the TS_VRCG_0 bit within the TS_Setting register.

For devices where the TS function is not needed, tie a 10-kΩ resistor to the TS pin.

There is an active voltage clamp present on this device which will prevent the voltage on the TSMR pin from rising above the VTS_CLAMP threshold. This will particularly be ON when the TSMR pin is floating. The bit TS_OPEN_STAT is set when this clamp is active. This will also be ON regardless of the TS_EN bit. The interrupt is asserted as long as the TS_INT mask is not written.

The bits TS_HOT/TS_COLD, TS_WARM, and TS_COOL will allow these thresholds to be adjusted. The hysteresis will also move along with these thresholds. When the TS_WARM condition occurs, the device will lower the battery target regulation voltage by TS_VRCG but will not modify the VBAT_CTRL register.

The TS_ICHG bit will reduce charging current based on the factor described in the register map when the TSMR pin hits a TS_COOL condition. The TREG function will still be based on this reduced threshold.

The TS_VRCG_0 bit will reduce the charging voltage when the TSMR pin hits the TS_WARM threshold. The factor will be based on the register map.

When the button is detected as pressed (TSMR pin low) during the charging process, charging will be momentarily suspended until the button is high again. When charging is disabled in any of the TS faults, trickle charging is also disabled. In a TS fault where the current is reduced (COOL), the trickle charging current is not altered.

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### 8.3.14 I²C Interface

The device uses an I²C compatible interface to program and read control parameters, status bits, and so forth. I²C ™ is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All of the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The device works as a preipheral and supports the following data transfer modes, as defined in the I²C Bus™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements.

Register contents remain intact as long as $V_{BAT}$ or $V_{IN}$ voltages remain above their respective undervoltage lockout thresholds and the device is not in shutdown mode.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The device only supports 7-bit addressing. The device 7-bit address is 0x6A (8-bit shifted address is 0xD4).

#### *8.3.14.1 F/S Mode Protocol*

The master initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 8-6. All I²C-compatible devices should recognize a start condition.

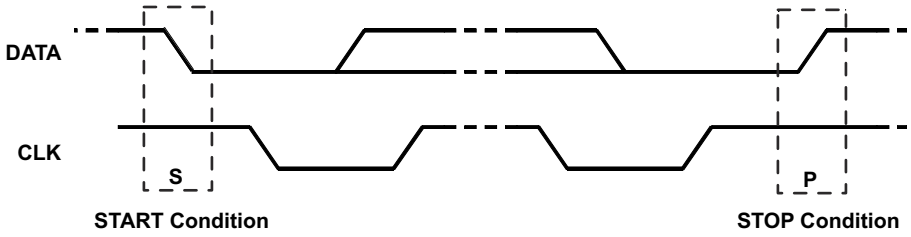



**Figure 8-6. START and STOP Condition**

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 8-7). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 8-8) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

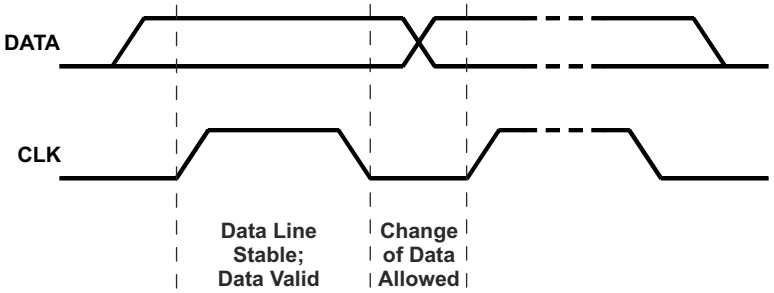



**Figure 8-7. Bit Transfer on the Serial Interface**


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The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 8-6). This releases the bus and stops the communication link with the addressed slave. All $I^2C$ compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave $I^2C$ logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

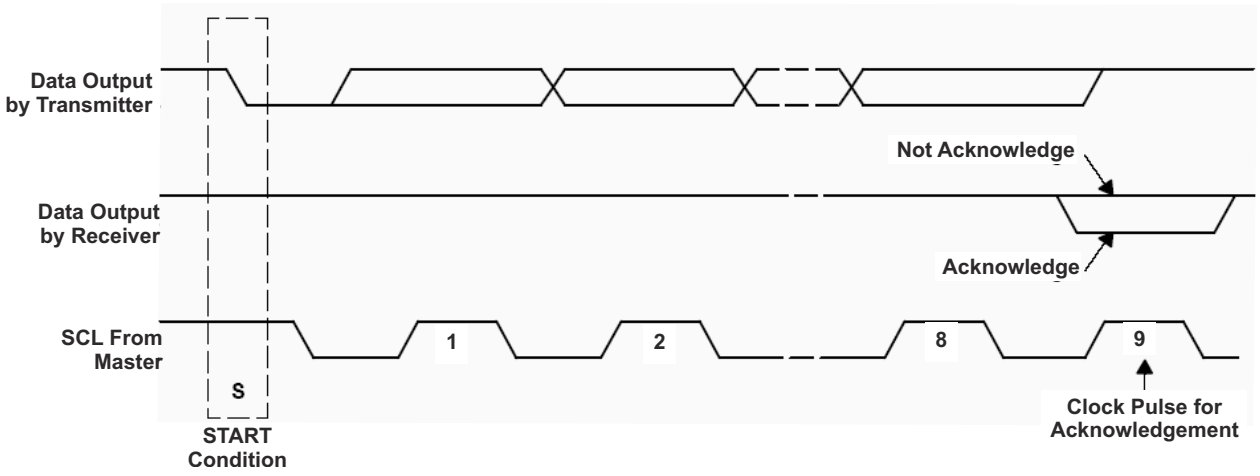



**Figure 8-8. Ackowledge on the $I^2C$ Bus**

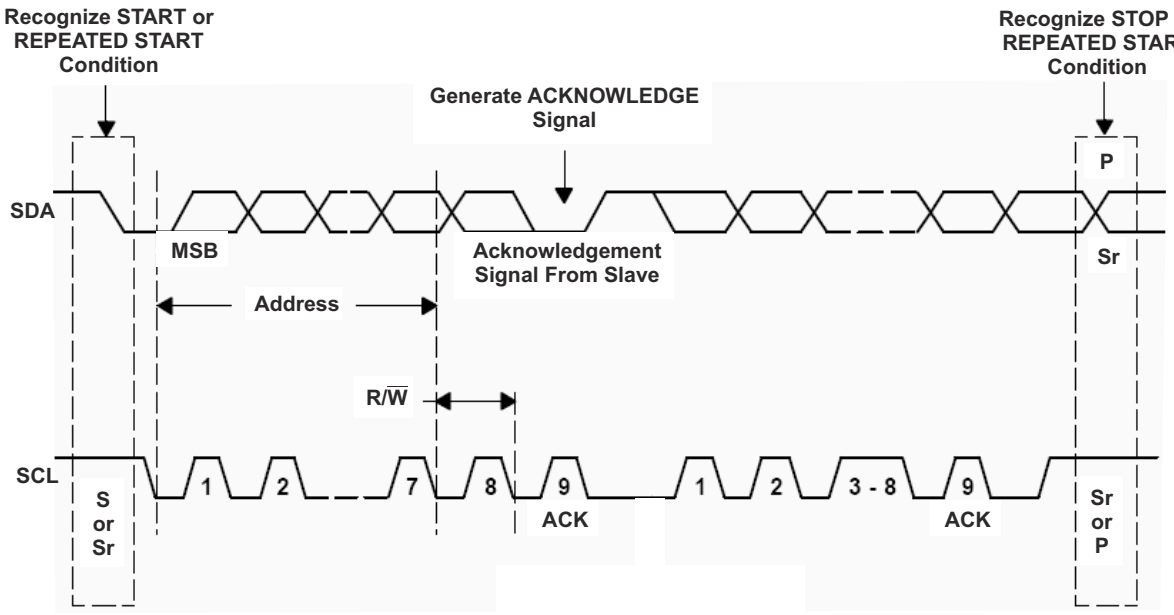



**Figure 8-9. Bus Protocol**

## 8.4 Device Functional Modes

The BQ25180 has four main modes of operation: Battery Mode, Ship Mode, Charge/Adapter Mode when a supply is connected to IN, and Shutdown mode. The table below summarizes the functions that are active for each operation mode.

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**Table 8-6. Function Availability Based on Primary Mode of Operation**

| FUNCTION | CHARGE/ADAPTER MODE | BATTERY MODE | SHIP MODE | SHUTDOWN MODE |
|---|---|---|---|---|
| Input overvoltage | Yes | Yes | No | No |
| Input undervoltage | Yes | Yes | Yes | Yes |
| Battery overcurrent | Yes, if enabled | Yes | Yes, if enabled | No |
| Battery undervoltage | Yes | Yes | No | No |
| Input DPM | Yes, if enabled | No | No | No |
| Dynamic power path management | Yes, if enabled | No | No | No |
| BATFET | Yes | Yes | No | No |
| TS measurement | Yes | No | No | No |
| Battery charging | Yes, if enabled | No | No | No |
| ILIM | Yes (Register Value) | No | No | No |
| Pushbutton input | Yes | Yes, if enabled | Yes | No |
| INT output | Yes | Yes | No | No |
| $I^2C$ | Yes | Yes | No | No |

## 8.5 Register Maps

### 8.5.1 I2C Registers

Table 8-7 lists the memory-mapped registers for the I2C registers. All register offset addresses not listed in Table 8-7 should be considered as reserved locations and the register contents should not be modified.

**Table 8-7. I2C Registers**

| Offset | Acronym | Register Name | Section |
|---|---|---|---|
| 0x0 | STAT0 | Charger Status | Go |
| 0x1 | STAT1 | Charger Status and Faults | Go |
| 0x2 | FLAG0 | Charger Flag Registers | Go |
| 0x3 | VBAT_CTRL | Battery Voltage Control | Go |
| 0x4 | ICHG_CTRL | Fast Charge Current Control | Go |
| 0x5 | CHARGECTRL0 | Charger Control 0 | Go |
| 0x6 | CHARGECTRL1 | Charger Control 1 | Go |
| 0x7 | IC_CTRL | IC Control | Go |
| 0x8 | TMR_ILIM | Timer and Input Current Limit Control | Go |
| 0x9 | SHIP_RST | Shipmode, Reset and Pushbutton Control | Go |
| 0xA | SYS_REG | SYS Regulation Voltage Control | Go |
| 0xB | TS_CONTROL | TS Control | Go |
| 0xC | MASK_ID | MASK and Device ID | Go |

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

**Table 8-8. I2C Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| **Read Type** | | |
| R | R | Read |


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**Table 8-8. I2C Access Type Codes (continued)**

| Access Type | Code | Description |
|---|---|---|
| RC | R<br>C | Read<br>to Clear |
| **Write Type** | | |
| W | W | Write |
| **Reset or Default Value** | | |
| *-n* | | Value after reset or the default value |

#### 8.5.1.1 STAT0 Register (Offset = 0x0) [Reset = X]

STAT0 is shown in Figure 8-10 and described in Table 8-9.

Return to the Summary Table.

**Figure 8-10. STAT0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_OPEN_STAT | CHG_STAT_1:0 | | ILIM_ACTIVE_STAT | VDPPM_ACTIVE_STAT | VINDPM_ACTIVE_STAT | THERMREG_ACTIVE_STAT | VIN_PGOOD_STAT |
| R-X | R-X | | R-X | R-X | R-X | R-X | R-X |

**Table 8-9. STAT0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | TS_OPEN_STAT | R | X | TS Open Status<br>1b0 = TSMR pin is not Open<br>1b1 = TSMR pin is Open |
| 6-5 | CHG_STAT_1:0 | R | X | Charging Status Indicator<br>2b00 = Not Charging while charging is enabled.<br>2b01 = Constant Current Charging (Trickle Charge/ Pre Charge or in Fast Charge Mode)<br>2b10 = Constant Voltage Charging<br>2b11 = Charge Done or charging is disabled by the host. |
| 4 | ILIM_ACTIVE_STAT | R | X | Input Curent Limit Active<br>1b0 = Not Active<br>1b1 = Active |
| 3 | VDPPM_ACTIVE_STAT | R | X | VDPPM Mode Active<br>1b0 = Not Active<br>1b1 = Active |
| 2 | VINDPM_ACTIVE_STAT | R | X | VINDPM Mode Active<br>1b0 = Not Active<br>1b1 = Active |
| 1 | THERMREG_ACTIVE_STAT | R | X | Thermal Regulation Active<br>1b0 = Not Active<br>1b1 = Active |
| 0 | VIN_PGOOD_STAT | R | X | VIN Power Good<br>1b0 = VIN Power Not Good<br>1b1 = VIN Power Good |


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### 8.5.1.2 STAT1 Register (Offset = 0x1) [Reset = X]

STAT1 is shown in Figure 8-11 and described in Table 8-10.

Return to the Summary Table.

**Figure 8-11. STAT1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VIN_OVP_STAT | BUVLO_STAT | RESERVED | TS_STAT_1:0 | | SAFETY_TMR_FAULT_FLAG | WAKE1_FLAG | WAKE2_FLAG |
| R-1b0 | R-X | R-X | R-2b00 | | RC-1b0 | RC-1b0 | RC-1b0 |

**Table 8-10. STAT1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | VIN_OVP_STAT | R | 1b0 | VIN_OVP Fault<br>1b0 = Not Active<br>1b1 = Active |
| 6 | BUVLO_STAT | R | X | Battery UVLO Status<br>1b0 = Not Active<br>1b1 = Active |
| 5 | RESERVED | R | X | Reserved |
| 4-3 | TS_STAT_1:0 | R | 2b00 | TS Status<br>2b00 = Normal<br>2b01 = VTS < VHOT or VTS > VCOLD(charging suspended)<br>2b10 = VCOOL < VTS < VCOLD (Charging current reduced by value set by TS_Registers)<br>2b11 = VWARM > VTS > VHOT (Charging voltage reduced by value set by TS_Registers) |
| 2 | SAFETY_TMR_FAULT_FLAG | RC | 1b0 | Safety Timer Expired Fault Cleared only after CE is toggled.<br>1b0 = Not Active<br>1b1 = Active |
| 1 | WAKE1_FLAG | RC | 1b0 | Wake 1 Timer Flag<br>1b0 = Does not meet Wake 1 Condition<br>1b1 = Met Wake 1 Condition |
| 0 | WAKE2_FLAG | RC | 1b0 | Wake 2 Timer Flag<br>1b0 = Does not meet Wake 2 Condition<br>1b1 = Met Wake2 Condition |

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### 8.5.1.3 FLAG0 Register (Offset = 0x2) [Reset = X]

FLAG0 is shown in Figure 8-12 and described in Table 8-11.

Return to the Summary Table.

**Figure 8-12. FLAG0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_FAULT | ILIM_ACTIVE_FLAG | VDPPM_ACTIVE_FLAG | VINDPM_ACTIVE_FLAG | THERMREG_ACTIVE_FLAG | VIN_OVP_FAULT_FLAG | BUVLO_FAULT_FLAG | BAT_OCP_FAULT |
| RC-X | RC-X | RC-X | RC-X | RC-X | RC-X | RC-X | RC-X |

**Table 8-11. FLAG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | TS_FAULT | RC | X | TS_Fault<br>1b0 = No TS Fault detected<br>1b1 = TS Fault detected |
| 6 | ILIM_ACTIVE_FLAG | RC | X | ILIM Active<br>1b0 = NO ILIM Fault detected<br>1b1 = ILIM Fault detected |
| 5 | VDPPM_ACTIVE_FLAG | RC | X | VDPPM FLAG<br>1b0 = VDPPM fault not detected<br>1b1 = VDPPM fault detected |
| 4 | VINDPM_ACTIVE_FLAG | RC | X | VINDPM FLAG<br>1b0 = VINDPM fault not detected<br>1b1 = VINDPM fault detected |
| 3 | THERMREG_ACTIVE_FLAG | RC | X | Thermal Regulation FLAG<br>1b0 = No thermal regulation detected<br>1b1 = Thermal regulation has occured |
| 2 | VIN_OVP_FAULT_FLAG | RC | X | VIN_OVP FLAG<br>1b0 = VIN_OVP fault not detected<br>1b1 = VIN_OVP fault detected |
| 1 | BUVLO_FAULT_FLAG | RC | X | Battery undervoltage FLAG<br>1b0 = Battery undervoltage fault not detected<br>1b1 = Battery undervoltage fault detected |
| 0 | BAT_OCP_FAULT | RC | X | Battery overcurrent protection<br>1b0 = Battery overcurrent condition not detected<br>1b1 = Battery overcurrent condition detected |


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#### 8.5.1.4 VBAT_CTRL Register (Offset = 0x3) [Reset = 0x46]

VBAT_CTRL is shown in Figure 8-13 and described in Table 8-12.

Return to the Summary Table.

**Figure 8-13. VBAT_CTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | VBATREG_6:0 | | | | | | |
| R/W-1b0 | R/W-7b1000110 | | | | | | |

**Table 8-12. VBAT_CTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 1b0 | Reserved |
| 6-0 | VBATREG_6:0 | R/W | 7b1000110 | Battery Regulation Voltage VBATREG= 3.5V + VBATREG_CODE * 10mV.<br>Maximum programmable voltage = 4.65V |

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### 8.5.1.5 ICHG_CTRL Register (Offset = 0x4) [Reset = 0x05]

ICHG_CTRL is shown in Figure 8-14 and described in Table 8-13.

Return to the Summary Table.

**Figure 8-14. ICHG_CTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CHG_DIS | ICHG_6:0 | | | | | | |
| R/W-1b0 | R/W-7b0000101 | | | | | | |

**Table 8-13. ICHG_CTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CHG_DIS | R/W | 1b0 | Charge Disable<br>1b0 = Battery Charging Enabled<br>1b1 = Battery Charging Disabled |
| 6-0 | ICHG_6:0 | R/W | 7b0000101 | For ICHG <= 35mA = ICHGCODE +5mA For ICHG > 35mA = 40+ ((ICHGCODE-31)*10)mA.<br>Maximum programmable current = 1000mA |


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### 8.5.1.6 CHARGECTRL0 Register (Offset = 0x5) [Reset = 0x2C]

CHARGECTRL0 is shown in Figure 8-15 and described in Table 8-14.

Return to the Summary Table.

**Figure 8-15. CHARGECTRL0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | IPRECHG | ITERM_1:0 | | VINDPM_1:0 | | THERM_REG_1:0 | |
| R/W-1b0 | R/W-1b0 | R/W-2b10 | | R/W-2b11 | | R/W-2b00 | |

**Table 8-14. CHARGECTRL0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 1b0 | Reserved |
| 6 | IPRECHG | R/W | 1b0 | Precharge current = x times of term<br>1b0 = Precharge is 2x Term<br>1b1 = Precharge is Term |
| 5-4 | ITERM_1:0 | R/W | 2b10 | Termination current = % of Icharge<br>2b00 = Disable<br>2b01 = 5% of ICHG<br>2b10 = 10% of ICHG<br>2b11 = 20% of ICHG |
| 3-2 | VINDPM_1:0 | R/W | 2b11 | VINDPM Level Selection<br>2b00 = 4.2 V<br>2b01 = 4.5 V<br>2b10 = 4.7 V<br>2b11 = Disabled |
| 1-0 | THERM_REG_1:0 | R/W | 2b00 | Thermal Regulation Threshold<br>2b00 = 100C<br>2b11 = Disabled |

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### 8.5.1.7 CHARGECTRL1 Register (Offset = 0x6) [Reset = 0x56]

CHARGECTRL1 is shown in Figure 8-16 and described in Table 8-15.

Return to the Summary Table.

**Figure 8-16. CHARGECTRL1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IBAT_OCP_1:0 | | BUVLO_2:0 | | | CHG_STATUS_INT_MASK | ILIM_INT_MASK | VDPM_INT_MASK |
| R/W-2b01 | | R/W-3b010 | | | R/W-1b1 | R/W-1b1 | R/W-1b0 |

**Table 8-15. CHARGECTRL1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | IBAT_OCP_1:0 | R/W | 2b01 | Battery Discharge Current Limit<br>2b00 = 500mA<br>2b01 = 1000mA<br>2b10 = 1500mA<br>2b11 = Disabled |
| 5-3 | BUVLO_2:0 | R/W | 3b010 | Battery Undervoltage LockOut Falling Threshold.<br>3b000 = 3.0V<br>3b001 = 3.0V<br>3b010 = 3.0V<br>3b011 = 2.8V<br>3b100 = 2.6V<br>3b101 = 2.4V<br>3b110 = 2.2V<br>3b111 = 2.0V |
| 2 | CHG_STATUS_INT_MASK | R/W | 1b1 | Mask Charging Status Interrupt<br>1b0 = Enable Charging Status Interrupt anytime there is a charging status change.<br>1b1 = Mask Charging Status Interrupt |
| 1 | ILIM_INT_MASK | R/W | 1b1 | Mask ILIM Fault Interrupt<br>1b0 = Enable ILIM Interrupt<br>1b1 = Mask ILIM Interrupt |
| 0 | VDPM_INT_MASK | R/W | 1b0 | Mask VINDPM and VDPPM Interrupt<br>1b0 = Enable VINDPM and VDPPM Interrupt<br>1b1 = Mask VINDPM and VDPPM Interrupt |


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### 8.5.1.8 IC_CTRL Register (Offset = 0x7) [Reset = 0x84]

IC_CTRL is shown in Figure 8-17 and described in Table 8-16.

Return to the Summary Table.

**Figure 8-17. IC_CTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_EN | VLOWV_SEL | VRCH_0 | 2XTMR_EN | SAFETY_TIMER_1:0 | | WATCHDOG_SEL_1:0 | |
| R/W-1b1 | R/W-1b0 | R/W-1b0 | R/W-1b0 | R/W-2b01 | | R/W-2b00 | |

**Table 8-16. IC_CTRL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | TS_EN | R/W | 1b1 | TS Auto Function<br>1b0 = TS auto function disabled (Only charge control is disabled. TS monitoring is enabled)<br>1b1 = TS auto function enabled |
| 6 | VLOWV_SEL | R/W | 1b0 | Precharge Voltage Threshold (VLOWV)<br>1b0 = 3V<br>1b1 = 2.8V |
| 5 | VRCH_0 | R/W | 1b0 | Recharge Voltage Threshold<br>1b0 = 100mV<br>1b1 = 200 mV |
| 4 | 2XTMR_EN | R/W | 1b0 | Timer Slow<br>1b0 = The timer is not slowed at any time<br>1b1 = The timer is slowed by 2x when in any control other than CC or CV |
| 3-2 | SAFETY_TIMER_1:0 | R/W | 2b01 | Fast Charge Timer<br>2b00 = 3 hour fast charge<br>2b01 = 6 hour fast charge<br>2b10 = 12 hour fast charge<br>2b11 = Disable safety timer |
| 1-0 | WATCHDOG_SEL_1:0 | R/W | 2b00 | Watchdog Selection<br>2b00 = 160s default register values<br>2b01 = 160s HW_RESET<br>2b10 = 40s HW_RESET<br>2b11 = Disable watchdog function |

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### 8.5.1.9 TMR_ILIM Register (Offset = 0x8) [Reset = 0x4D]

TMR_ILIM is shown in Figure 8-18 and described in Table 8-17.

Return to the Summary Table.

**Figure 8-18. TMR_ILIM Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MR_LPRESS_1:0 | | MR_RESET_VIN | AUTOWAKE_1:0 | | ILIM_2:0 | | |
| R/W-2b01 | | R/W-1b0 | R/W-2b01 | | R/W-3b101 | | |

**Table 8-17. TMR_ILIM Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | MR_LPRESS_1:0 | R/W | 2b01 | Push button Long Press duration timer<br>2b00 = 5s<br>2b01 = 10s<br>2b10 = 15s<br>2b11 = 20s |
| 5 | MR_RESET_VIN | R/W | 1b0 | Hardware reset condition<br>1b0 = Reset sent when long press duration is met<br>1b1 = Reset sent when long press duration is met and VIN_Powergood |
| 4-3 | AUTOWAKE_1:0 | R/W | 2b01 | Auto Wake Up Timer Restart<br>2b00 = 0.5s<br>2b01 = 1s<br>2b10 = 2s<br>2b11 = 4s |
| 2-0 | ILIM_2:0 | R/W | 3b101 | Input Current Limit Setting<br>3b000 = 50mA<br>3b001 = 100mA(max.)<br>3b010 = 200mA<br>3b011 = 300mA<br>3b100 = 400mA<br>3b101 = 500mA(max.)<br>3b110 = 700mA<br>3b111 = 1100mA |


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### 8.5.1.10 SHIP_RST Register (Offset = 0x9) [Reset = 0x11]

SHIP_RST is shown in Figure 8-19 and described in Table 8-18.

Return to the Summary Table.

**Figure 8-19. SHIP_RST Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REG_RST | EN_RST_SHIP_1:0 | | PB_LPRESS_ACTION_1:0 | | WAKE1_TMR | WAKE2_TMR | EN_PUSH |
| R/W-1b0 | R/W-2b00 | | R/W-2b10 | | R/W-1b0 | R/W-1b0 | R/W-1b1 |

**Table 8-18. SHIP_RST Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | REG_RST | R/W | 1b0 | Software Reset<br>1b0 = Do nothing<br>1b1 = Software Reset |
| 6-5 | EN_RST_SHIP_1:0 | R/W | 2b00 | Shipmode Enable and Hardware Reset<br>2b00 = Do nothing<br>2b01 = Enable shutdown mode with wake on adapter insert only<br>2b10 = Enable shipmode with wake on button press or adapter insert<br>2b11 = Hardware Reset |
| 4-3 | PB_LPRESS_ACTION_1:0 | R/W | 2b10 | Pushbutton long press action<br>2b00 = Do nothing<br>2b01 = Hardware Reset<br>2b10 = Enable shipmode<br>2b11 = Enable shutdown mode |
| 2 | WAKE1_TMR | R/W | 1b0 | Wake 1 Timer Set<br>1b0 = 300ms<br>1b1 = 1s |
| 1 | WAKE2_TMR | R/W | 1b0 | Wake 2 Timer Set<br>1b0 = 2s<br>1b1 = 3s |
| 0 | EN_PUSH | R/W | 1b1 | Enable Push Button and Reset Function on Battery Only<br>1b0 = Disable<br>1b1 = Enable |

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### 8.5.1.11 SYS_REG Register (Offset = 0xA) [Reset = 0x40]

SYS_REG is shown in Figure 8-20 and described in Table 8-19.

Return to the Summary Table.

**Figure 8-20. SYS_REG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SYS_REG_CTRL_2:0 | | | RESERVED | SYS_MODE_1:0 | | WATCHDOG_15S_ENABLE | VDPPM_DIS |
| R/W-3b010 | | | R/W-1b0 | R/W-2b00 | | R/W-1b0 | R/W-1b0 |

**Table 8-19. SYS_REG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | SYS_REG_CTRL_2:0 | R/W | 3b010 | SYS Regulation Voltgage<br>3b000 = Battery Tracking Mode<br>3b001 = 4.4V<br>3b010 = 4.5V<br>3b011 = 4.6V<br>3b100 = 4.7V<br>3b101 = 4.8V<br>3b110 = 4.9V<br>3b111 = Pass-Through (VSYS is VIN) |
| 4 | RESERVED | R/W | 1b0 | Reserved |
| 3-2 | SYS_MODE_1:0 | R/W | 2b00 | Sets how SYS is powered in any state, except SHIPMODE<br>2b00 = SYS powered from VIN if present or VBAT<br>2b01 = SYS powered from VBAT only, even if VIN present<br>2b10 = SYS disconnected and left floating<br>2b11 = SYS disconnected with pulldown |
| 1 | WATCHDOG_15S_ENABLE | R/W | 1b0 | I2C Watchdog<br>1b0 = Mode Disabled<br>1b1 = Do a HW reset after 15s if no I2C transaction after VIN plugged |
| 0 | VDPPM_DIS | R/W | 1b0 | Disable VDPPM<br>1b0 = Enable VDPPM<br>1b1 = Disable VDPPM |


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### 8.5.1.12 TS_CONTROL Register (Offset = 0xB) [Reset = 0x00]

TS_CONTROL is shown in Figure 8-21 and described in Table 8-20.

Return to the Summary Table.

**Figure 8-21. TS_CONTROL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_HOT | | TS_COLD | | TS_WARM | TS_COOL | TS_ICHG | TS_VRCG |
| R/W-2b00 | | R/W-2b00 | | R/W-1b0 | R/W-1b0 | R/W-1b0 | R/W-1b0 |

**Table 8-20. TS_CONTROL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | TS_HOT | R/W | 2b00 | TS Hot threshold register<br>2b00 = Default 60C<br>2b01 = 65C<br>2b10 = 50C<br>2b11 = 45C |
| 5-4 | TS_COLD | R/W | 2b00 | TS Cold threshold register<br>2b00 = Default 0C<br>2b01 = 3C<br>2b10 = 5C<br>2b11 = -3C |
| 3 | TS_WARM | R/W | 1b0 | TS Warm threshold<br>1b0 = Default 45C<br>1b1 = Disabled |
| 2 | TS_COOL | R/W | 1b0 | TS Cool threshold register<br>1b0 = Default 10C<br>1b1 = Disabled |
| 1 | TS_ICHG | R/W | 1b0 | Fast charge current when decreased by TS function<br>1b0 = 0.5*ICHG<br>1b1 = 0.2*ICHG |
| 0 | TS_VRCG | R/W | 1b0 | Reduced target battery voltage during Warm<br>1b0 = VBATREG -100mV<br>1b1 = VBATREG -200mV |

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### 8.5.1.13 MASK_ID Register (Offset = 0xC) [Reset = 0xC0]

MASK_ID is shown in Figure 8-22 and described in Table 8-21.

Return to the Summary Table.

**Figure 8-22. MASK_ID Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_INT_MASK | TREG_INT_MASK | BAT_INT_MASK | PG_INT_MASK | Device_ID | | | |
| R/W-1b1 | R/W-1b1 | R/W-1b0 | R/W-1b0 | R-4b0000 | | | |

**Table 8-21. MASK_ID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | TS_INT_MASK | R/W | 1b1 | Mask TS<br>1b0 = Enable TS Interrupt<br>1b1 = Mask TS Interrupt |
| 6 | TREG_INT_MASK | R/W | 1b1 | Mask TREG<br>1b0 = Enable TREG Interrupt<br>1b1 = Mask TREG Interrupt |
| 5 | BAT_INT_MASK | R/W | 1b0 | Mask BATOCP and BUVLO<br>1b0 = Enable BOCP and BUVLO Interrupt<br>1b1 = Mask BOCP and BUVLO Interrupt |
| 4 | PG_INT_MASK | R/W | 1b0 | Mask PG and VINOVP<br>1b0 = Enable PG and VINOVP Interrupt<br>1b1 = Mask PG and VINOVP Interrupt |
| 3-0 | Device_ID | R | 4b0000 | Device ID<br>4b0000 = BQ25180 |


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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

A typical application of the BQ25180 consists of the device configured as an $I^2C$ controlled single cell Li-ion battery charger and power path manager or battery applications such as smart watches and wireless headsets. A battery thermistor may be connected to the TS pin to allow the device to monitor the battery temperature and control charging as desired.

The system designer may connect the TS/MR pin input to a push button to send interrupts to the host as a button is pressed or to allow the application end user to reset the system.

## 9.2 Typical Application

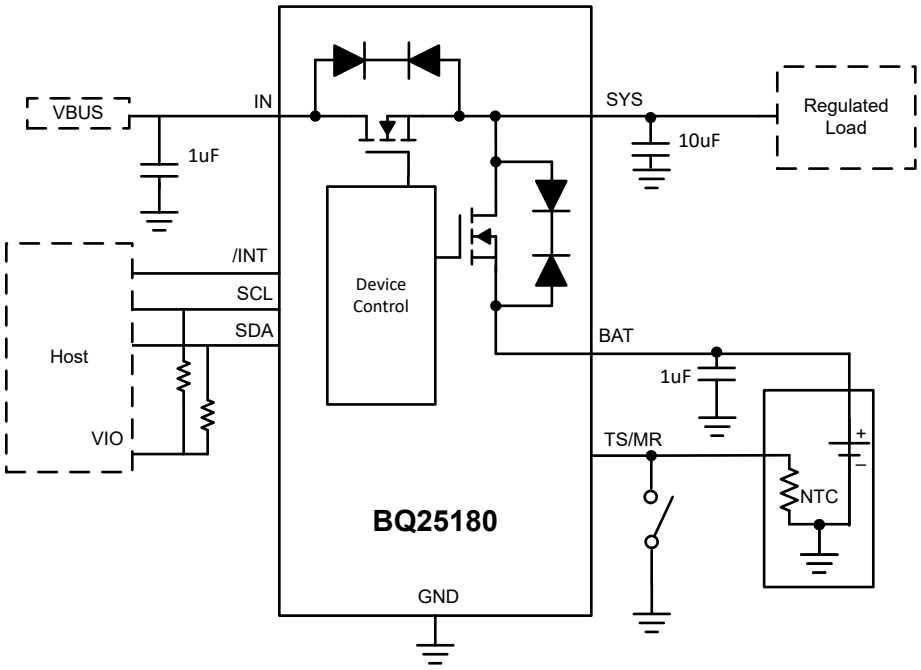



**Figure 9-1. Typical Application**

### 9.2.1 Design Requirements

The design requirements for the following design example are shown in Table 9-1.

**Table 9-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| IN supply voltage | 5 V |
| Battery regulation voltage | 4.2 V |

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Input (IN/SYS) Capacitors

Low ESR ceramic capacitors such as X7R or X5R are preferred for input decoupling capacitors and should be placed as close as possible to the supply and ground pins for the IC. Due to the voltage derating of the capacitors, it is recommended that 25-V rated capacitors are used for the IN and SYS pins which can normally operate at 5 V. After derating the minimum capacitance must be higher than 1 µF.

#### 9.2.2.2 TS

The ground connection for the NTC must be made as close as possible to the GND pin of the device or kelvin connected to it to minimize any error in TS measurement due to IR drops on the ground board lines.

If the system designer does not wish to use the TS function for charging control, a 10-kΩ resistor must be connected from TS to ground.

#### 9.2.2.3 Recommended Passive Components

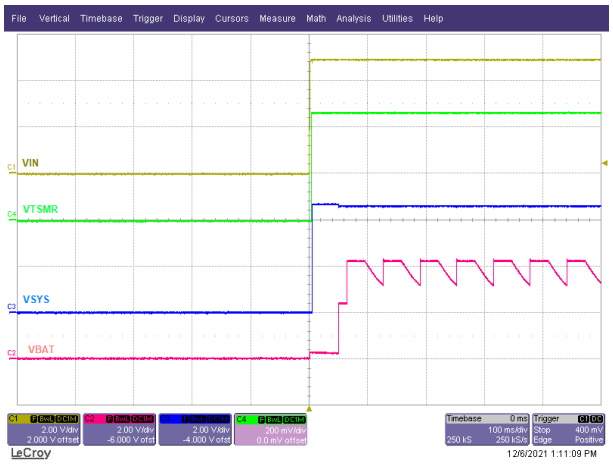
**Table 9-2. Passive Components**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $C_{SYS}$ | Capacitance on SYS pin | 1 | 10 | 100 | µF |
| $C_{BAT}$ | Capacitance on BAT pin | 1 | 1 | - | µF |
| $C_{IN}$ | IN input bypass capacitance | 1 | 1 | 10 | µF |


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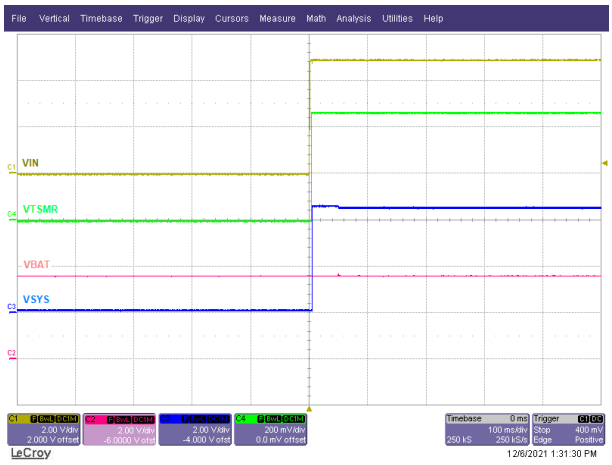
### 9.2.3 Application Curves

$C_{IN}$ = 1 µF, $C_{OUT}$ = 10 µF, $V_{IN}$ = 5 V, $V_{OUT}$ = 3.8 V, $I_{CHG}$ = 10 mA (unless otherwise specified)



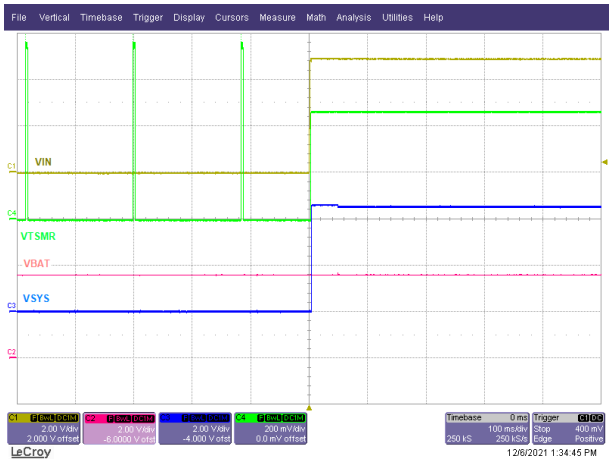

VIN = 5 V VBAT = Floating

**Figure 9-2. Power Up with IN Supply Insertion with No Battery**



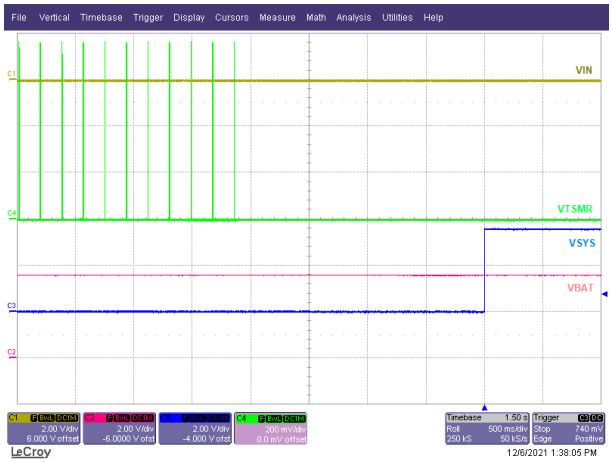

VIN = 5 V VBAT = 3.6 V

**Figure 9-3. Power Up from Shutdown Mode with VIN Supply Insertion**




VIN = 0 V → 5 V VBAT = 3.8 V

**Figure 9-4. Power Up from Shipmode with VIN Insertion**



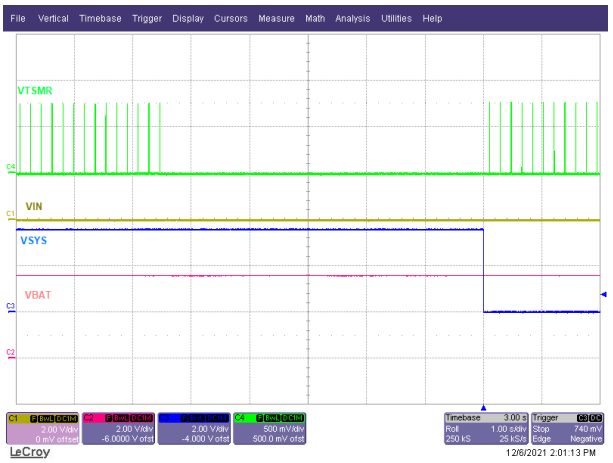

MR_LPRESS = 00 (5s Long Press Timer)

**Figure 9-5. Power Up from Shipmode with /TSMR Button Press**




MR_LPRESS = 00 (5s Long Press Timer)
PB_LPRESS_ACTION = 01 (Hardware Reset)

**Figure 9-6. Hardware Reset with /TSMR Press**




MR_LPRESS = 00 (5s Long Press Timer)
PB_LPRESS_ACTION = 10

**Figure 9-7. Enter Shipmode with Push Button Long Press**



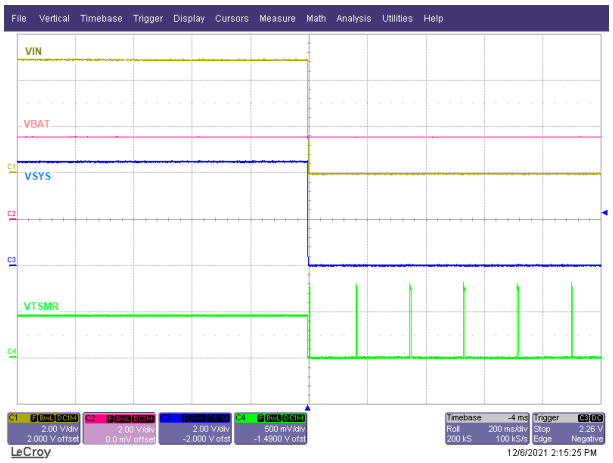

**Figure 9-8. Hardware Reset Through $I^2C$**




EN_RST_SHIP = 01 (enable shutdown with wake on adapter insert only)

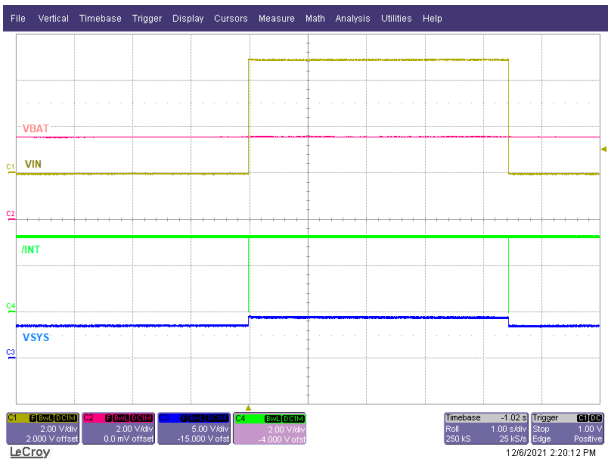
**Figure 9-9. Shutdown Entry on VIN Removal**


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EN_RST_SHIP = 10 (enable shutdown with wake on adapter insert only)

**Figure 9-10. Shipmode Entry on VIN Removal**




$V_{IN}$ = 0 V → 5 V → 0 V

**Figure 9-11. Power Good Interrupt on /INT**

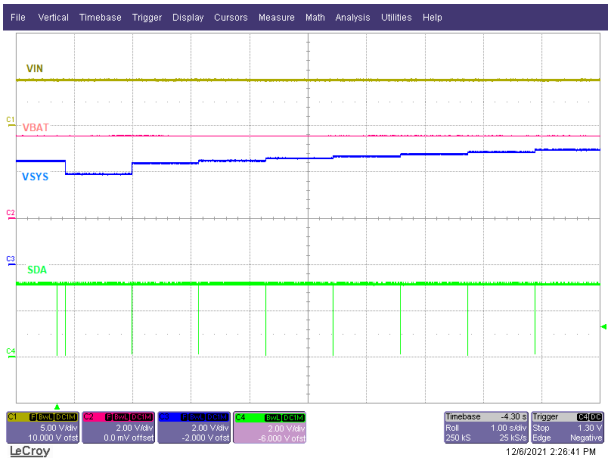



VIN = 0 V

PB_LPRESS_ACTION = 11 (enable shutown mode)

MR_LPRESS = 00 (5 seconds)

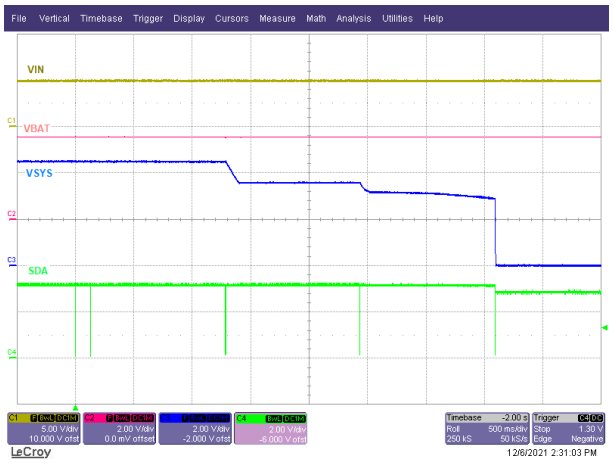
**Figure 9-12. Shutdown Mode Entry with Push Button Long Press**




SYS_REG_CTRL = 000 → 111 in steps

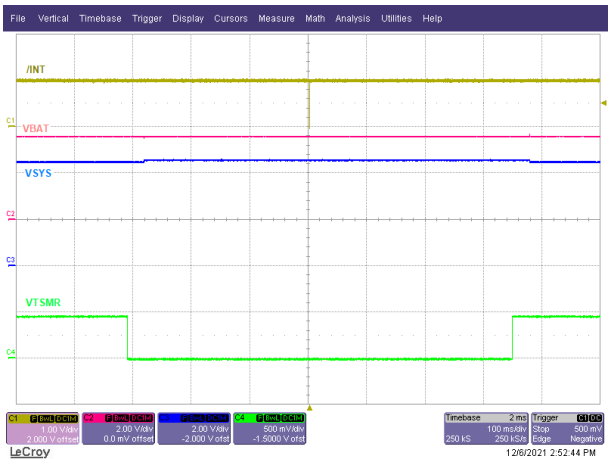
**Figure 9-13. SYS Regulation Sweep**

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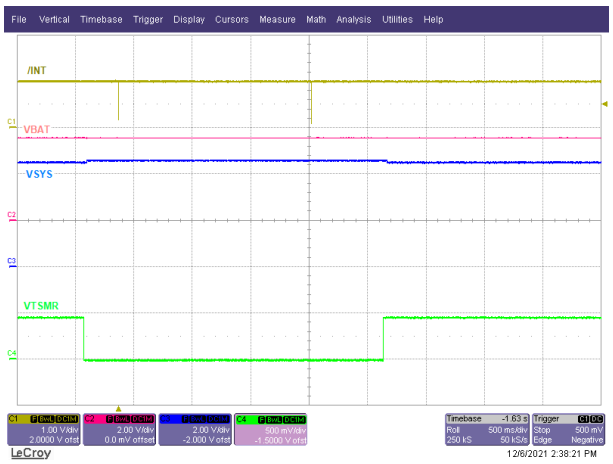

SYS_MODE = 00 → 01 → 10 → 11

**Figure 9-14. SYS Mode Sweep**



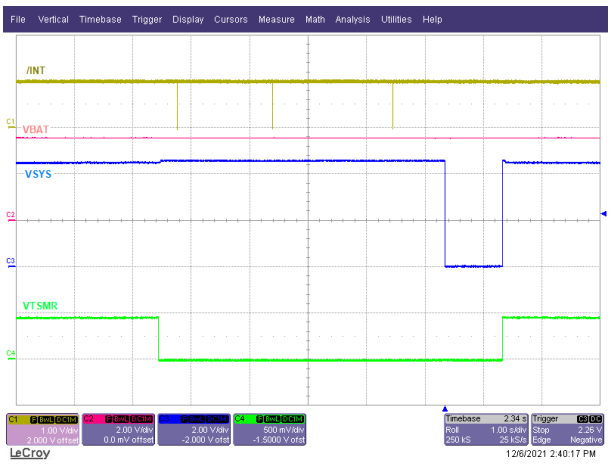

VIN = 5 V

**Figure 9-15. Wake1 Interrupt with VIN Present**




VIN = 5 V

**Figure 9-16. Wake2 Interrupt with VIN Present**



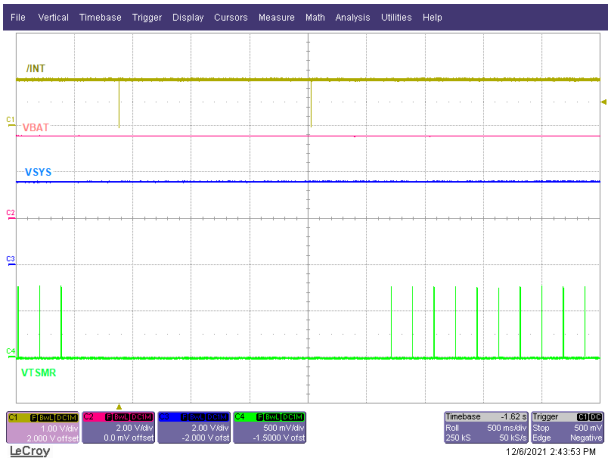

VIN = 5 V
MR_LPRESS = 00 (5 seconds)
PB_LPRESS_ACTION = Hardware Reset

**Figure 9-17. Long Press Interrupt with VIN Present**




VIN = 0 V

**Figure 9-18. Wake1 Interrupt without VIN**




VIN = 5 V

**Figure 9-19. Wake2 Interrupt without VIN Present**


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VIN = 0 V

MR_LPRESS = 00 (5 seconds)

PB_LPRESS_ACTION = 11 (Hardware Reset)

**Figure 9-20. Long Press Interrupt without VIN Present**

## 10 Power Supply Recommendations

The BQ25180 requires the adapter or IN supply to be between 2.7 V and 5.5 V. The battery voltage must be higher than 3.15 V or $V_{BUVLO}$ to ensure proper operation.


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# 11 Layout

## 11.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND, the capacitor from SYS to GND and BAT to GND should be placed as close as possible to the device, with short trace runs to IN, SYS, BAT and GND.Have solid ground plane that is tied to the GND bump
- The pushbutton GND should be connected close to the device as possible.
- The high current charge paths into IN, SYS and BAT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.

## 11.2 Layout Example

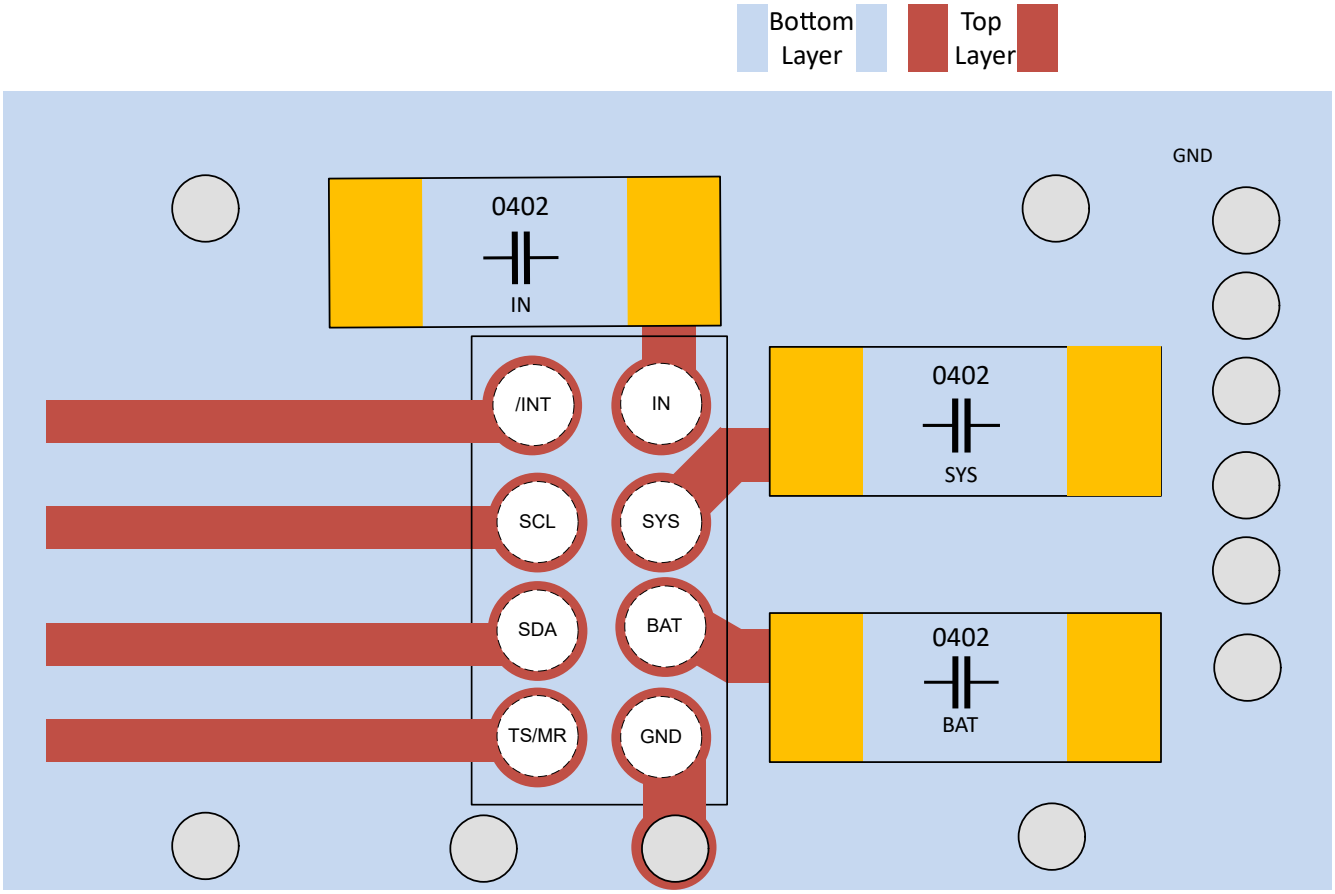



**Figure 11-1. Layout Example**

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |


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## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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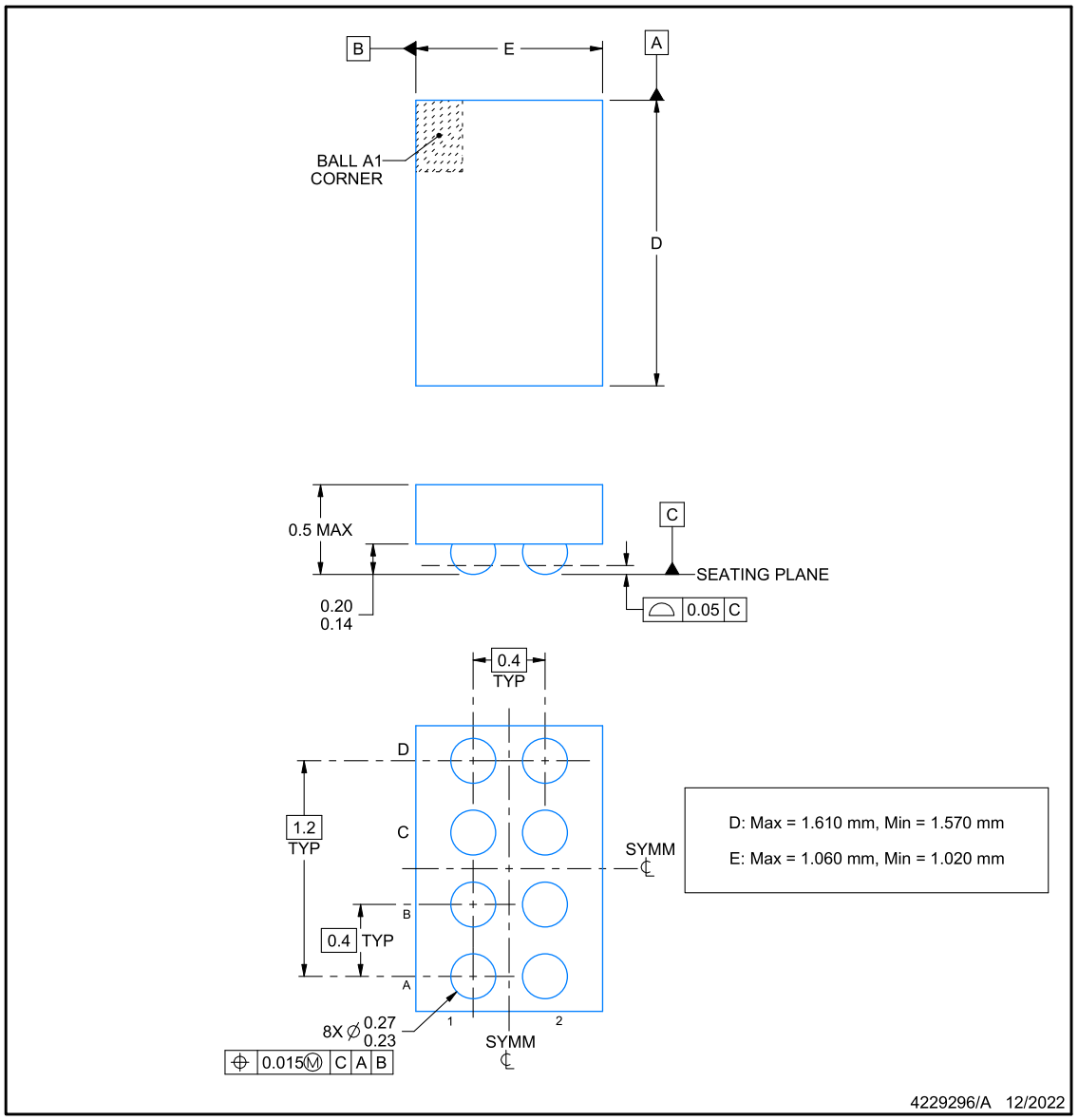


# PACKAGE OUTLINE

## YBG0008-C01

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

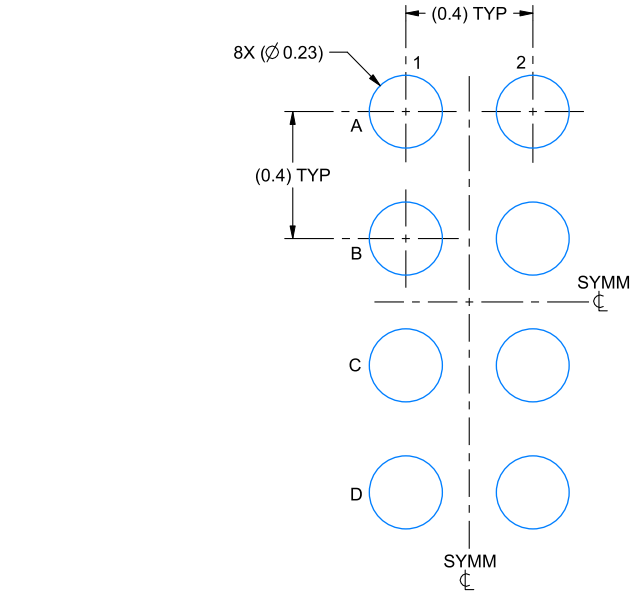

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# EXAMPLE BOARD LAYOUT

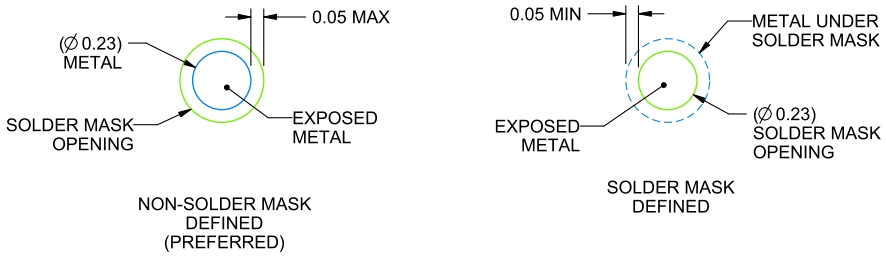
## YBG0008-C01

### DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

4229296/A 12/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



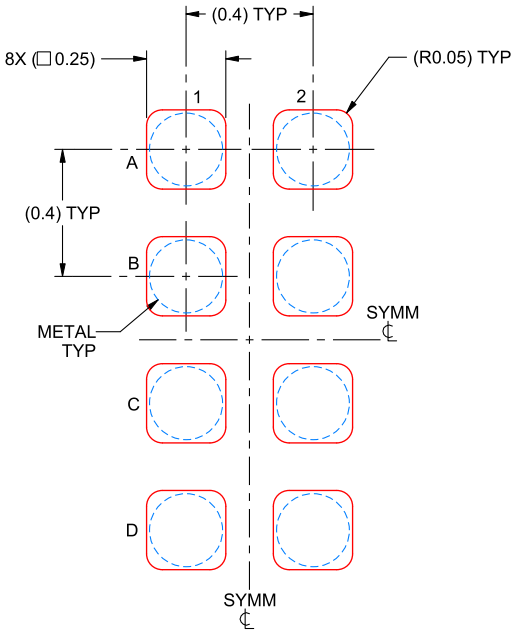
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## EXAMPLE STENCIL DESIGN

### YBG0008-C01

### DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4229296/A 12/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| BQ25180YBGR | Active | Production | DSBGA (YBG) \| 8 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | B180 |
| BQ25180YBGR.A | Active | Production | DSBGA (YBG) \| 8 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | B180 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

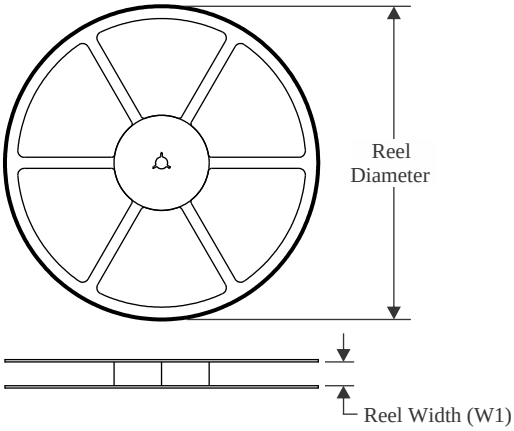
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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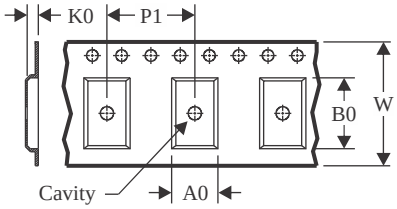
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

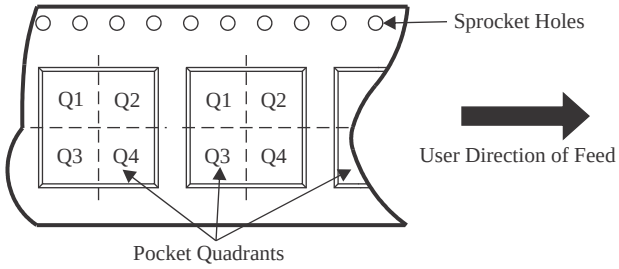



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

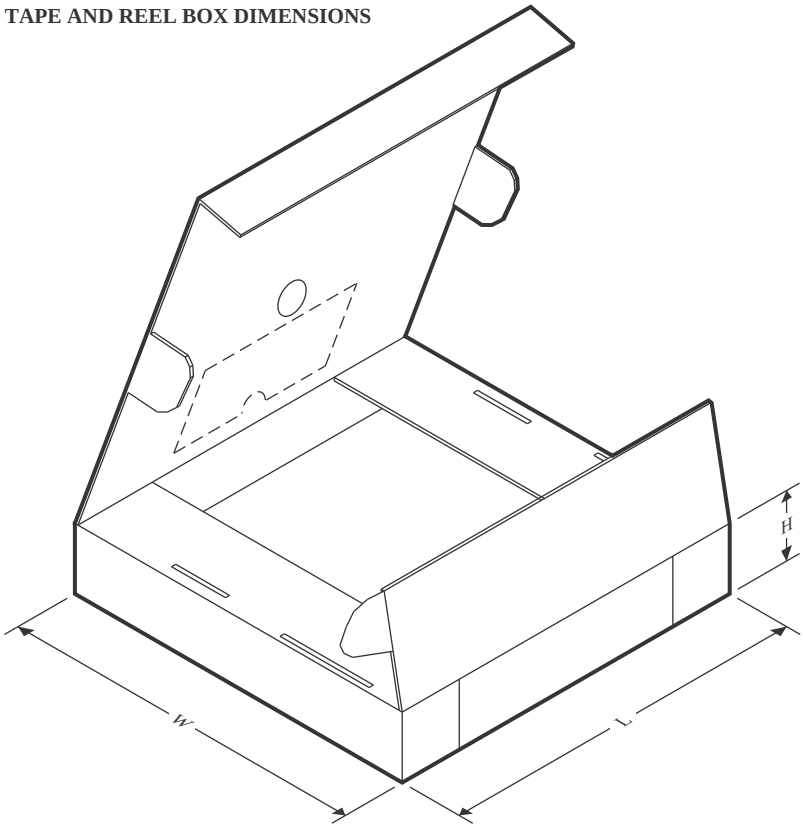
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ25180YBGR | DSBGA | YBG | 8 | 3000 | 180.0 | 8.4 | 1.15 | 1.75 | 0.65 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ25180YBGR | DSBGA | YBG | 8 | 3000 | 182.0 | 182.0 | 20.0 |

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