TEXAS INSTRUMENTS
BQ25173
SLUSDY6 – NOVEMBER 2021

BQ25173: 800-mA Linear Charger for 1- to 4-Cell Supercapacitor

1 Features

- Input voltage up-to 40-V tolerant
- Automatic Sleep mode for low power consumption
  - 350-nA leakage current
  - 2-µA input leakage current when charge disabled
- Supports 1- to 4-cell supercapacitor
- Supports charging supercapacitor from 0 V
- External resistor programmable operation
  - FB pin to adjust supercapacitor regulation voltage
  - ISET to set charge current from 10 mA to 800 mA
- High accuracy
  - ±1% charge voltage accuracy
  - ±10% charge current accuracy
- Charging features
  - $\overline{CE}$ pin for charging function control
  - Open-drain output for status and fault indication
  - Open-drain output for power-good indication
- Integrated fault protection
  - 18-V IN overvoltage protection
  - 1000-mA overcurrent protection
  - 125°C thermal regulation; 150°C thermal shutdown protection
  - OUT short-circuit protection
  - ISET pin short/open protection

2 Applications

- Smart meter
- Barcode scanner
- Portable medical equipment
- Dashboard camera

3 Description

The BQ25173 is an integrated 800-mA linear charger for 1- to 4-cell supercapacitors targeted at space-limited applications. The device has a single power output that charges the supercapacitor. The system load can be placed in parallel with the supercapacitor; the charge current is shared between the system and supercapacitor.

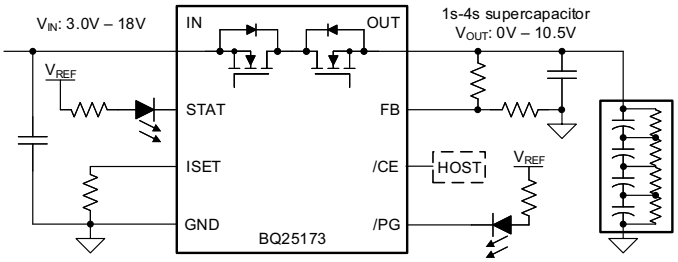
During charging, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold, T_{REG}, is exceeded. This feature allows for fast charging of a fully discharged supercapacitor.

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge function control. The charge voltage and fast-charge current are programmable through external resistors.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
BQ25173	WSON (8)	2.0 mm x 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
November 2021	*	Initial Release

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5 Pin Configuration and Functions

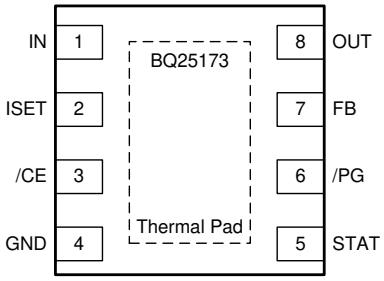

Figure 5-1. DSG (WSON) Package 8-Pin Top View

Table 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
IN	1	P	Input power. Connect to external DC supply. Bypass IN with at least 1-µF capacitor to GND, placed close to the IC.
ISET	2	I	Programs the device fast-charge current, I_{CHG}. External resistor from ISET to GND defines fast-charge current value. Expected range is 30 kΩ (10 mA) to 375 Ω (800 mA). $I_{CHG} = K_{ISET} / R_{ISET}$.
$\overline{CE}$	3	I	Active low charge enable pin. Charging is enabled when the CE pin is LOW. IC remains in Shutdown mode and charging is disabled when the CE pin is HIGH. An internal pulldown resistor (R_{PD_CE}) enables the IC by default if this pin is floating.
GND	4	–	Ground pin.
STAT	5	O	Open-drain charger status indication output. Connect to pullup rail with a 10-kΩ resistor. LOW indicates V_{OUT} has reached 98% of the programmable regulation voltage, V_{REG}. HIGH indicates charge in progress.
$\overline{PG}$	6	O	Open-drain charger power-good output. Connect to pullup rail with a 10-kΩ resistor. $\overline{PG}$ goes LOW when $V_{IN} > V_{IN_LOWV}$ and $V_{OUT} + V_{SLEEPZ} < V_{IN} < V_{IN_OV}$.
$\overline{FB}$	7	I	Programs the supercapacitor regulation voltage, V_{REG}. Use a feedback divider not exceeding 1 MΩ from V_{OUT} to GND to set the regulation voltage. The bottom of the resistor divider network can be connected to $\overline{PG}$ for reduced power consumption when the input is removed (for $V_{REG} \leq$ 5 V).
OUT	8	P	Supercapacitor connection. System load may be connected in parallel with supercapacitor. Bypass OUT with at least 1-µF capacitor to GND, placed close to the IC.
Thermal Pad	—	P	Exposed pad beneath the IC for heat dissipation. Solder thermal pad to the board with vias connecting to solid GND plane.

(1) I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	40	V
Voltage	OUT	–0.3	13	V
Voltage	$\overline{CE}$, FB, ISET, STAT, $\overline{PG}$	–0.3	5.5	V
Output Sink Current	$\overline{PG}$, STAT		5	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the d ality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	3.0		18	V
V_{OUT}	Output voltage	0		10.5	V
I_{OUT}	Output current			0.8	A
T_J	Junction temperature	–40		125	°C
C_{IN}	IN capacitor	1			µF
C_{OUT}	OUT capacitor	1			µF
R_{ISET}	ISET resistor	0.375		30	kΩ

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6.4 Thermal Information

THERMAL METRIC(1)		BQ25173 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC(1))	75.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

3.0V < V_{IN} < 18V and V_{IN} > V_{OUT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_OUT}	Quiescent output current (OUT)	OUT= 4.2V, IN floating or IN = 0V - 5V, Charge Disabled ($\overline{CE}$ high), T_J = 25 °C		0.350	0.6	µA
		OUT= 4.2V, IN floating or IN = 0V - 5V, Charge Disabled ($\overline{CE}$ high), T_J < 105 °C		0.350	0.8	µA
I_{Q_OUT}	Quiescent output current (OUT)	OUT = 8.4V, IN floating or IN = 0V - 14V, Charge Disabled ($\overline{CE}$ high), T_J = 25 °C		0.8	1.2	µA
		OUT = 8.4V, IN floating or IN = 0V - 14V, Charge Disabled ($\overline{CE}$ high), T_J < 105 °C		0.8	1.5	µA
I_{SD_IN}	Shutdown input current (IN) with charge disabled	IN = 5V, Charge Disabled ($\overline{CE}$ high), no capacitor		2	4	µA
		IN = 14V, Charge Disabled ($\overline{CE}$ high), no capacitor		3.5	6	µA
I_{Q_IN}	Quiescent input current (IN)	IN = 5V, OUT = 3.8V, Charge Enabled ($\overline{CE}$ low), ICHG = 0A		0.45	0.6	mA
I_{Q_IN}	Quiescent input current (IN)	IN = 14V, OUT = 7.6V, Charge Enabled ($\overline{CE}$ low), ICHG = 0A		0.45	0.6	mA
INPUT						
V_{IN_OP}	IN operating range		3.0		18	V
V_{IN_LOWV}	IN voltage to start charging	IN rising	3.05	3.09	3.15	V
V_{IN_LOWV}	IN voltage to stop charging	IN falling	2.80	2.95	3.10	V
V_{SLEEPZ}	Exit sleep mode threshold	IN rising, V_{IN} - V_{OUT}, OUT = 4V	95	135	175	mV
V_{SLEEP}	Sleep mode threshold hysteresis	IN falling, V_{IN} - V_{OUT}, OUT = 4V		80		mV
V_{IN_OV}	VIN overvoltage rising threshold	IN rising	18.1	18.4	18.7	V
V_{IN_OVZ}	VIN overvoltage falling threshold	IN falling		18.2		V
CONFIGURATION PINS SHORT/OPEN PROTECTION						
R_{ISET_SHORT}	Highest resistor value considered short	R_{ISET} below this at startup, charger does not initiate charge, power cycle or $\overline{CE}$ toggle to reset			350	Ω
CHARGER						
V_{FB_REF}	Feedback reference voltage			0.8		V
$V_{FB_REF_ACC}$	Feedback reference voltage accuracy	Tj = -40°C to 125°C	-1		1	%
I_{CHG_RANGE}	Typical charge current regulation range	V_{OUT} > V_{BAT_LOWV}	10		800	mA
K_{ISET}	Charge current setting factor, I_{CHG} = K_{ISET} / R_{ISET}	10mA < ICHG < 800mA	270	300	330	AΩ
I_{CHG_ACC}	Charge current accuracy	R_{ISET} = 375Ω, OUT = 3.8V or 7.6V	720	800	880	mA
		R_{ISET} = 600Ω, OUT = 3.8V or 7.6V	450	500	550	mA
		R_{ISET} = 3.0kΩ, OUT = 3.8V or 7.6V	90	100	110	mA
		R_{ISET} = 30kΩ, OUT = 3.8V or 7.6V	9	10	11	mA
V_{CHG}	Supercapacitor charged threshold	OUT rising, as percentage of FB regulation target		98		%
R_{ON}	Charging path FET on-resistance	IOUT = 400mA, T_J = 25°C		845	1000	mΩ
		IOUT = 400mA, T_J = -40 - 125°C		845	1450	mΩ
CHARGER PROTECTION						
I_{OUT_OCP}	Output current limit threshold	IOUT rising	0.9	1	1.1	A

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6.5 Electrical Characteristics (continued)

3.0V < V_{IN} < 18V and V_{IN} > V_{OUT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE REGULATION AND TEMPERATURE SHUTDOWN						
T_{REG}	Typical junction temperature regulation			125		°C
T_{SHUT}	Thermal shutdown rising threshold	Temperature increasing		150		°C
	Thermal shutdown falling threshold	Temperature decreasing		135		°C
LOGIC INPUT PIN (/CE)						
V_{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
R_{PD_CE}	$\overline{CE}$ pin internal pulldown resistor		3.3			MΩ
LOGIC OUTPUT PIN (STAT, $\overline{PG}$)						
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{OUT_BIAS}	High-level leakage current	Pull up rail 3.3V			1	µA

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
CHARGER					
$t_{OUT_OCP_DGL}$	Deglitch time for I_{OUT_OCP}, IOUT rising		100		µs

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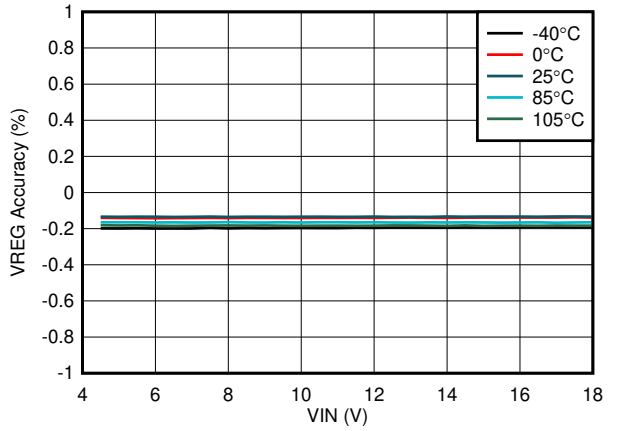
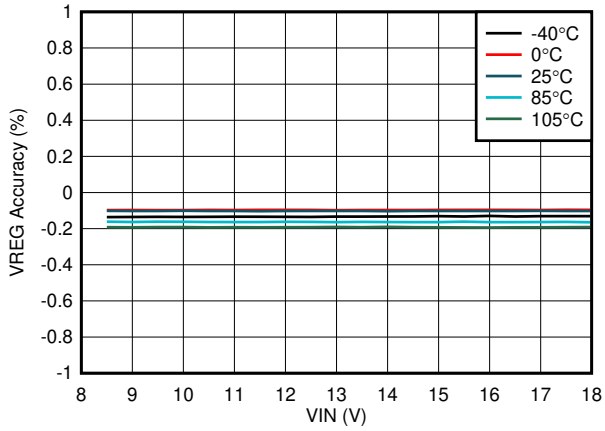
6.7 Typical Characteristics

C_{IN} = 1 µF, C_{OUT} = 1 µF



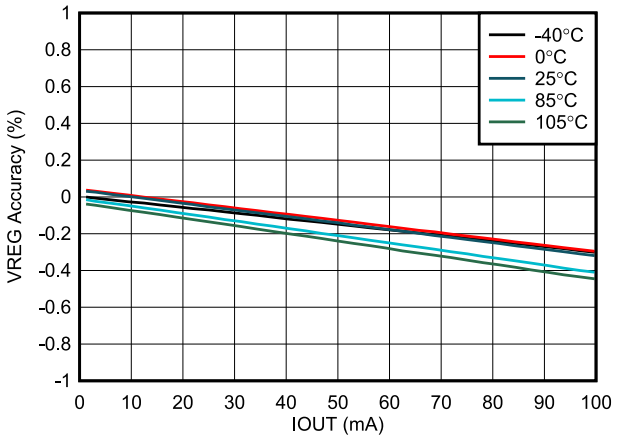
I_{OUT} = 10 mA V_{OUT} = 4.2 V

Figure 6-1. Line Regulation



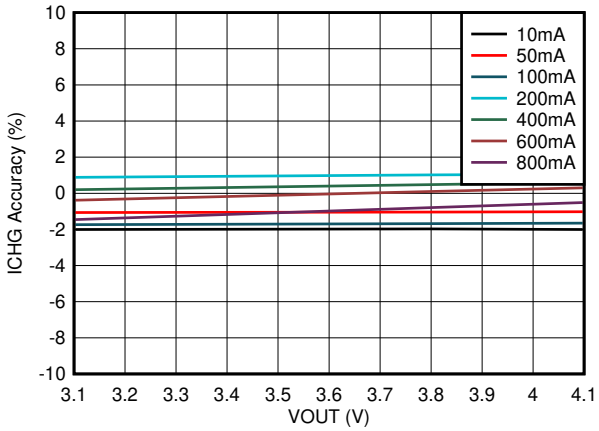
I_{OUT} = 10 mA V_{OUT} = 8.4 V

Figure 6-2. Line Regulation



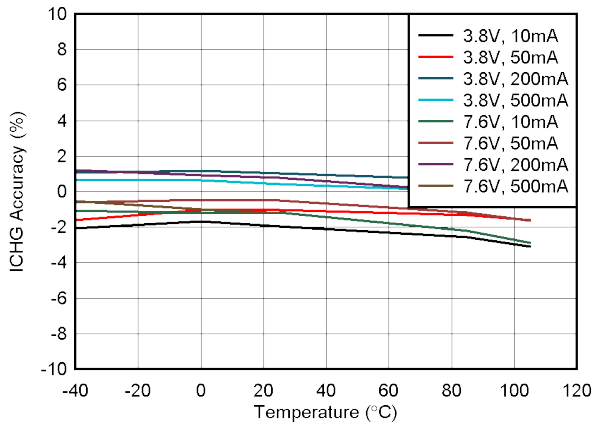
V_{IN} = 5 V V_{OUT} = 4.2 V

Figure 6-3. Load Regulation



V_{IN} = 5 V Temp. = 25ºC

Figure 6-4. ICHG Accuracy vs. V_{OUT}



V_{IN} = 5 V and 12 V V_{OUT} = 3.8 V and 7.6 V

Figure 6-5. ICHG Accuracy vs. Temperature

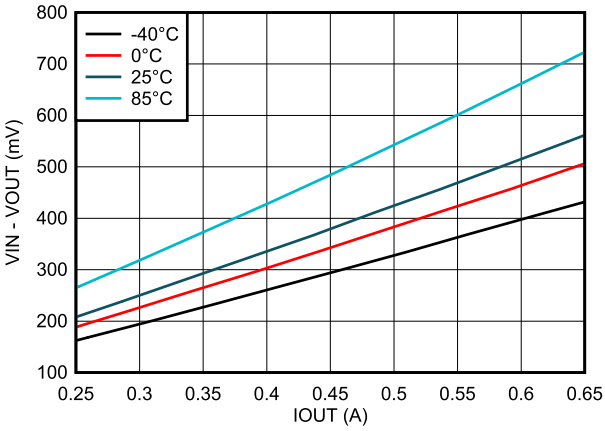


Figure 6-6. Dropout Voltage vs. Output Current

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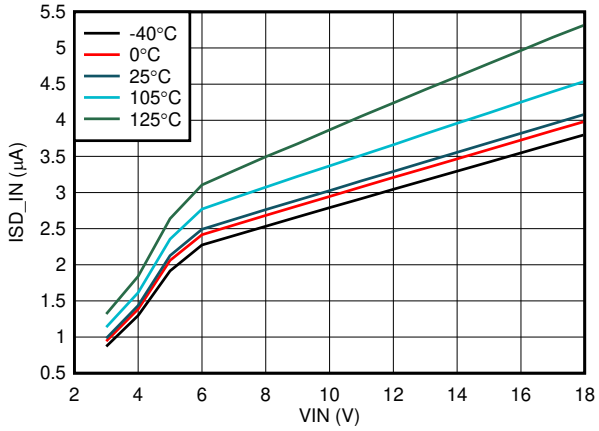
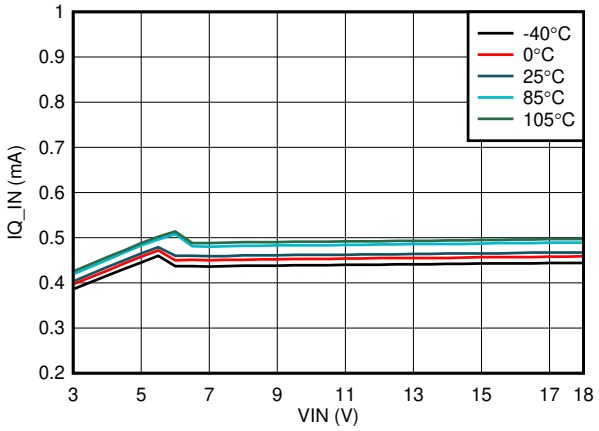
6.7 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 1 µF



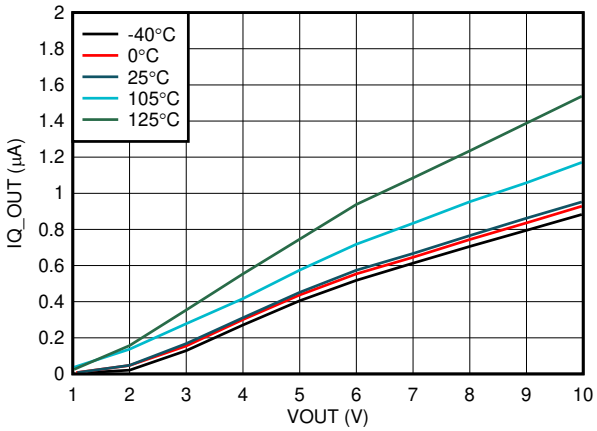
$\overline{CE}$ Pin = HIGH V_{OUT} = 0 V

Figure 6-7. Input Shutdown Current vs. Input Voltage



$\overline{CE}$ Pin = LOW ICHG = 0 A

Figure 6-8. Input Quiescent Current vs. Input Voltage



V_{IN} = 0 V

Figure 6-9. Output Quiescent Current vs. Output Voltage

7 Detailed Description

7.1 Overview

The device has a single power output that charges the supercapacitor. The system load can be placed in parallel with the supercapacitor; the charge current is shared between the system and supercapacitor.

The charger is designed for a single path from the input to the output to charge the supercapacitor. Upon application of a valid input power source, the ISET pin is checked for short/open circuit.

The device attempts to charge the supercapacitor at the fast-charge current setting from fully discharged (0 V) up to the programmable regulation voltage, V_{REG}. Power dissipation in the IC is greatest in fast charge with a lower supercapacitor voltage. If the IC temperature reaches T_{REG}, the IC enters thermal regulation and reduces the charge current as needed to keep the temperature from rising any further. The fast-charge current is programmed using the ISET pin. Figure 7-1 shows the typical supercapacitor charging profile with thermal regulation. At lower fast-charge settings, the junction temperature of the IC is less than T_{REG} and thermal regulation is not entered.

Once the supercapacitor has charged to the regulation voltage, the voltage loop takes control and holds the voltage at the regulation voltage as the current tapers down to zero. There is no current termination threshold as seen in Li-ion chargers.

Further details are described in Section 7.3.

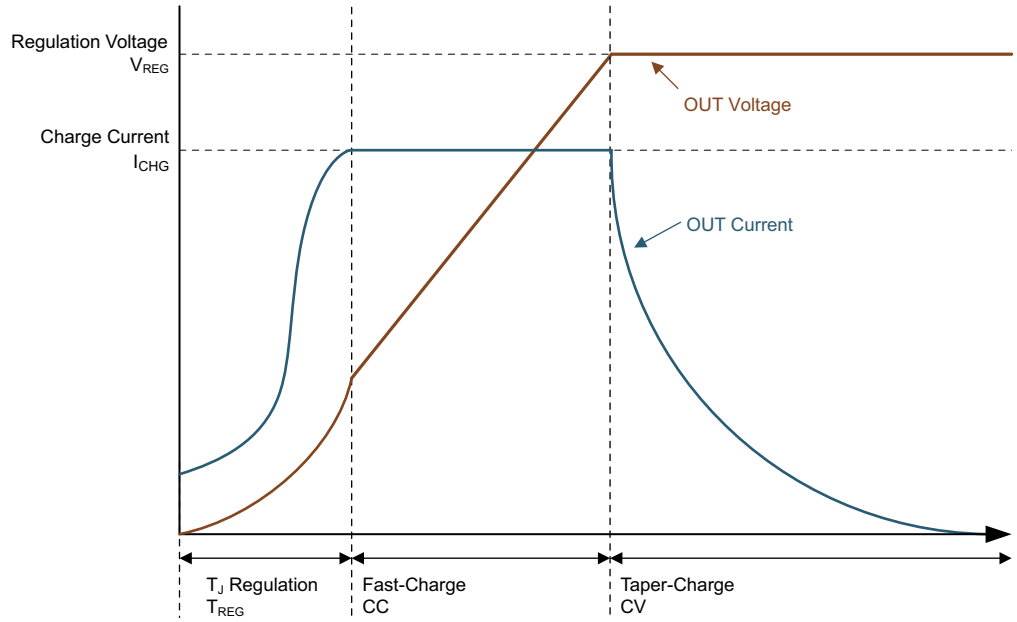


Figure 7-1. Supercapacitor Charging Profile with Thermal Regulation

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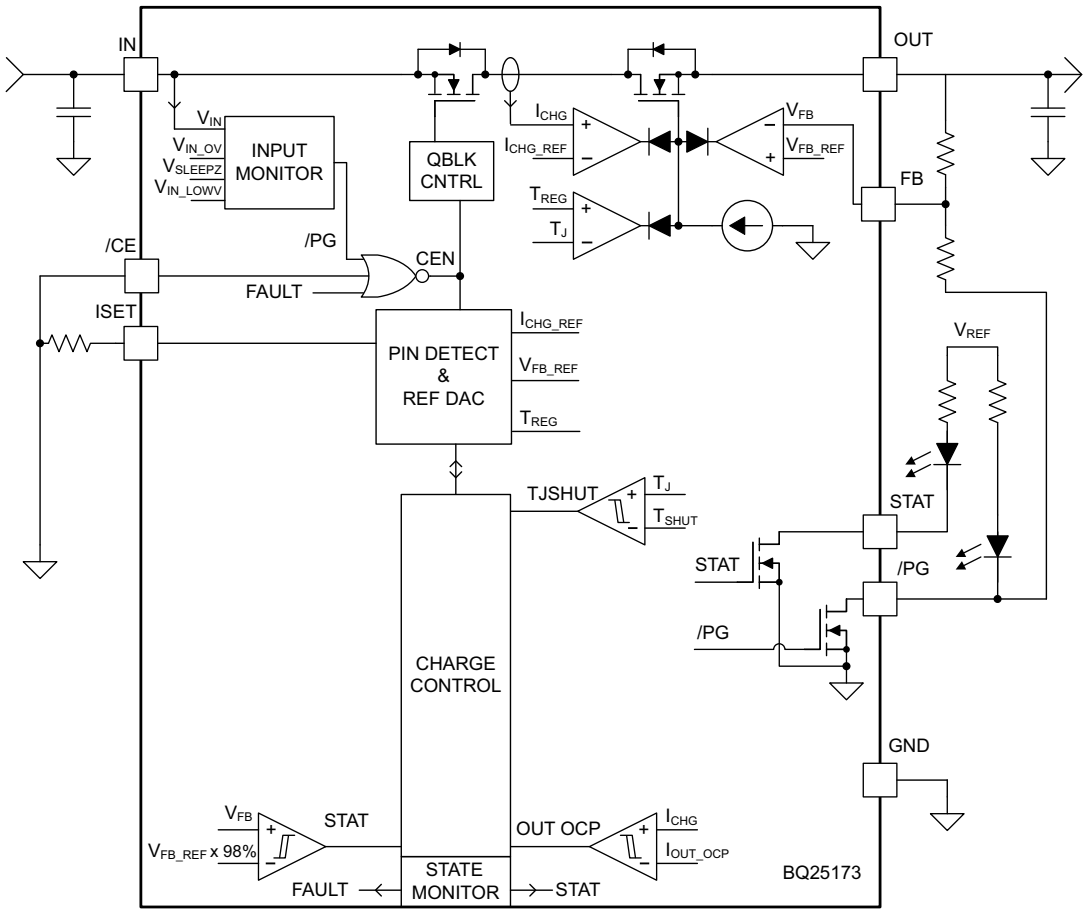
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Power Up from Input Source

When an input source is plugged in and charge is enabled, the device checks the input source voltage to turn on all of the bias circuits. The device detects and sets the charge current limits before the linear regulator is started. The power-up sequence from the input source is listed below:

1. ISET pin detection
2. Charger power up

7.3.1.1 ISET Pin Detection

After a valid VIN is plugged in and the $\overline{CE}$ pin is pulled LOW, the device checks the resistor on the ISET pin for a short circuit ($R_{ISET} < R_{ISET_SHORT}$). If a short condition is detected, the charger remains in the FAULT state until the input or $\overline{CE}$ pin is toggled. If the ISET pin is open circuit, the charger proceeds through pin detection and starts the charger with no charge current. This pin is monitored during charging and changes in R_{ISET} while the charger is operating immediately translates to changes in charge current.

An external pulldown resistor (±1% or better recommended to minimize charge current error) from the ISET pin to GND sets the charge current as:

$$I_{CHG} = \frac{K_{ISET}}{R_{ISET}} \quad (1)$$

where:

- I_{CHG} is the desired fast-charge current
- K_{ISET} is the gain factor found in the electrical specifications
- R_{ISET} is the pulldown resistor from the ISET pin to GND

For charge currents below 50 mA, an extra RC circuit is recommended on the ISET pin to achieve a more stable current signal. For greater accuracy at lower currents, part of the current-sensing FET is disabled to give better resolution.

7.3.2 Supercapacitor Regulation Voltage

The device allows for the supercapacitor regulation voltage, V_{REG}, to be programmed with a resistor divider between the OUT and FB pins:

$$V_{REG} = V_{FB_REF} \times \frac{R_{FBT} + R_{FBB}}{R_{FBB}} \quad (2)$$

Where V_{FB_REF} is listed in the electrical characteristcs table. The resistors can be seen in Figure 7-2. The total resistance (R_{FBT} + R_{FBB}) should not exceed 1 MΩ.

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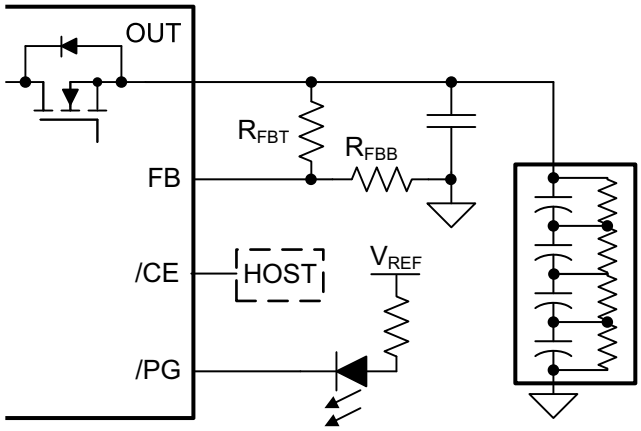

Figure 7-2. BQ25173 Feedback Divider

7.3.3 Supercapacitor Charging Profile

The device charges a supercapacitor in two phases: constant current and constant voltage. Power dissipation in the IC is greatest in fast charge with a lower supercapacitor voltage. If the IC temperature reaches T_{REG}, the IC enters thermal regulation and reduces the charge current as needed to keep the temperature from rising any further. As the supercapacitor approaches the regulation voltage, the current tapers down to 0 mA. There is no current termination threshold as seen in Li-Ion chargers.

7.3.4 Status Outputs ($\overline{PG}$, STAT)

7.3.4.1 Power Good Indicator ($\overline{PG}$ Pin)

This open-drain pin pulls LOW to indicate a good input source when:

1. VIN above V_{IN_LOWV}
2. VIN above V_{OUT} + V_{SLEEPZ} (not in SLEEP)
3. VIN below V_{IN_OV}

The $\overline{PG}$ pin can be used as the GND connection for the bottom resistor in the feedback divider to prevent divider leakage current from the supercapacitor when the charger is disabled. This is only recommended when $V_{REG} \leq$ 5 V (1-2s supercapacitors) as the absolute maximum rating on $\overline{PG}$ is 5.5 V. An example circuit can be seen in Figure 8-1.

7.3.4.2 Charging Status Indicator (STAT)

The device indicates the charging state on the open-drain STAT pin. This pin can drive an LED.

Table 7-1. STAT Pin State

CHARGING STATE	STAT PIN STATE
V_{FB} < 98% of V_{FB_REF}	High
V_{FB} > 98% of V_{FB_REF}	Low
Fault (VIN OVP, OUT OCP, or ISET pin short)	Blink at 1 Hz

7.3.5 Protection Features

The device closely monitors input and output voltage, as well as internal FET current and temperature for safe linear regulator operation.

7.3.5.1 Input Overvoltage Protection (VIN OVP)

If the voltage at the IN pin exceeds V_{IN_OV}, the device enters STANDBY mode. Once the IN voltage recovers to normal level, charging resumes.

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7.3.5.2 Output Overcurrent Protection (OUT OCP)

During normal operation, the OUT current should be regulated to the ISET programmed value. However, if a short circuit occurs on the ISET pin, the OUT current may rise to an unintended level. If current at the OUT pin exceeds I_{OUT_OCP}, the device turns off after a deglitch, $t_{OUT_OCP_DGL}$, and the device remains latched off. An input supply or $\overline{CE}$ pin toggle is required to restart operation.

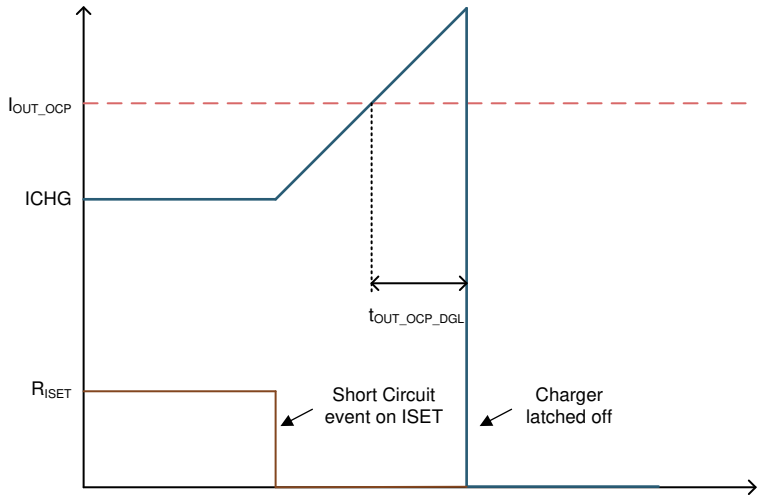

Figure 7-3. Overcurrent Protection

7.3.5.3 Thermal Regulation and Thermal Shutdown (T_{REG} and T_{SHUT})

The device monitors its internal junction temperature (T_J) to avoid overheating and to limit the IC surface temperature. When the internal junction temperature exceeds the thermal regulation limit, the device automatically reduces the charge current to maintain the junction temperature at the thermal regulation limit (T_{REG}). During thermal regulation, the actual charging current is usually below the programmed value on the ISET pin.

Additionally, device thermal shutdown turns off the linear regulator when the IC junction temperature exceeds the T_{SHUT} threshold. The charger resumes operation when the IC die temperature decreases below the T_{SHUT} falling threshold.

7.4 Device Functional Modes

7.4.1 Shutdown or Undervoltage Lockout (UVLO)

The device is in the shutdown state if the IN pin voltage is less than V_{IN_LOWV}. The internal circuitry is powered down, all the pins are high impedance, and the device draws from the input supply. Once the IN voltage rises above the V_{IN_LOW} threshold, the IC will enter Sleep Mode or Active Mode depending on the OUT pin voltage.

7.4.2 Sleep Mode

The device is in Sleep Mode when $V_{IN_LOWV} < V_{IN} < V_{OUT} + V_{SLEEPZ}$. The device waits for the input voltage to rise above $V_{OUT} + V_{SLEEPZ}$ to start operation.

7.4.3 Active Mode

The device is powered up and charges the supercapacitor when the $\overline{CE}$ pin is LOW and the IN voltage ramps above both V_{IN_LOWV}, and $V_{OUT} + V_{SLEEPZ}$. The device draws I_{Q_IN} from the supply to bias the internal circuitry. For details on the device power-up sequence, refer to Section 7.3.1.

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7.4.3.1 Standby Mode

The device is in Standby Mode if a valid input supply is present and a recoverable fault is detected. The internal circuitry is partially biased, and the device continues to monitor for the recoverable fault to be removed.

7.4.4 Fault Mode

The fault conditions are categorized into recoverable and nonrecoverable as follows:

- Recoverable, from which the device should automatically recover once the fault condition is removed:
  - VIN OVP
- Nonrecoverable, requiring pin or input supply toggle to resume operation:
  - OUT OCP
  - ISET pin short detected

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A typical application consists of the device configured as a standalone charger for a 1- to 4-cell supercapacitor. The regulation voltage, V_{REG}, is configured using a resistor divider between the OUT and FB pins. The charge current is configured using a pulldown resistor on the ISET pin. Pulling the $\overline{CE}$ pin above V_{IH} disables the charging function. Charger and input supply status are reported with the STAT and PG pins.

8.2 Typical Applications

8.2.1 1s Supercapacitor Charger Design Example

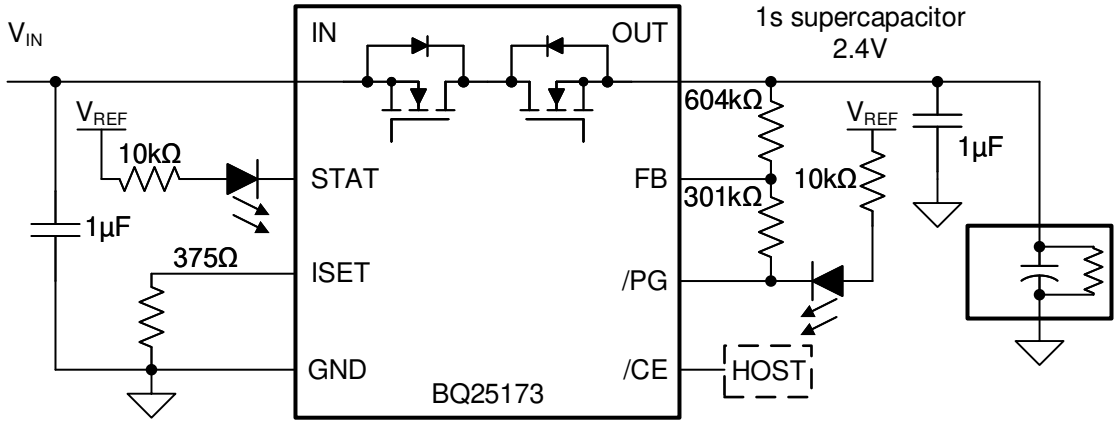

Figure 8-1. BQ25173 1s Supercapacitor Application Diagram

8.2.1.1 Design Requirements

- Supply voltage is 5 V to 18 V
- Fast charge current: I_{CHG} = 800 mA
- Regulation voltage: V_{REG} = 2.4 V
- $\overline{CE}$ is an open-drain control pin
- $\overline{PG}$ pin is used as the GND connection in the feedback divider to minimize supercapacitor current leakage

8.2.1.2 Detailed Design Procedure

- With R_{FBT} = 604 kΩ, calculate R_{FBB} so V_{REG} = 2.4 V using Equation 2
- R_{ISET} = [K_{ISET} / I_{CHG}] from electrical characteristics table.
  - K_{ISET} = 300 AΩ
  - R_{ISET} = [300 AΩ/0.8 A] = 375 Ω

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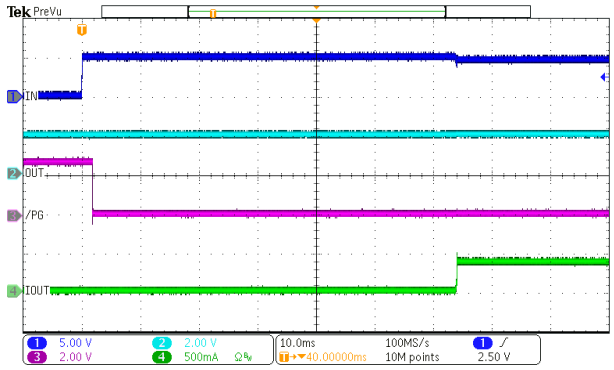
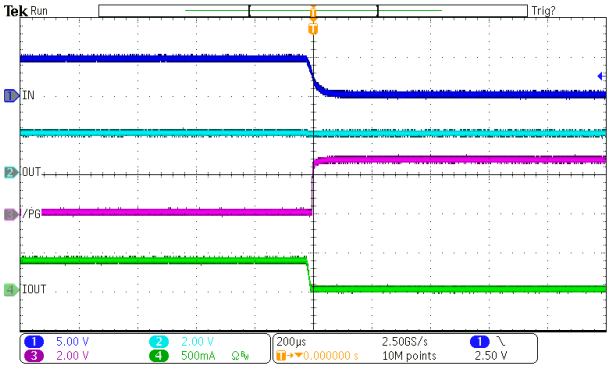
8.2.1.3 Application Curves

C_{IN} = 1 µF, C_{OUT} = 1 µF, C_{SC} = 25 F, V_{IN} = 5 V (unless otherwise specified)



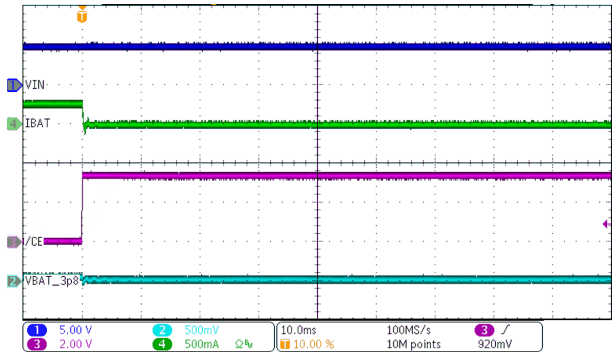
I_{CHG} = 400 mA

Figure 8-2. Power Up with Supercapacitor



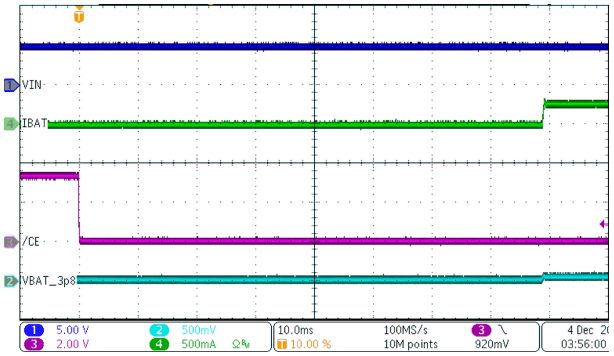
I_{CHG} = 400 mA

Figure 8-3. Power Down with Supercapacitor



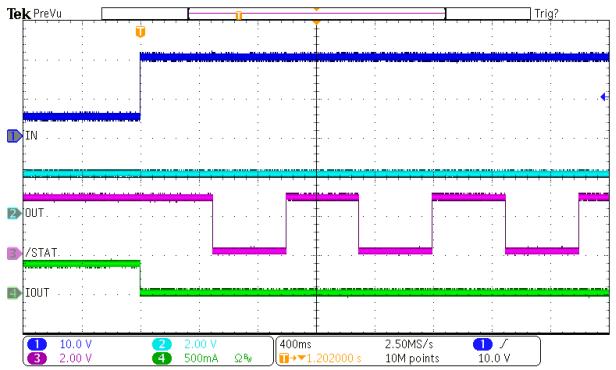
/CE pulled high I_{CHG} = 250 mA

Figure 8-4. Charge Disable



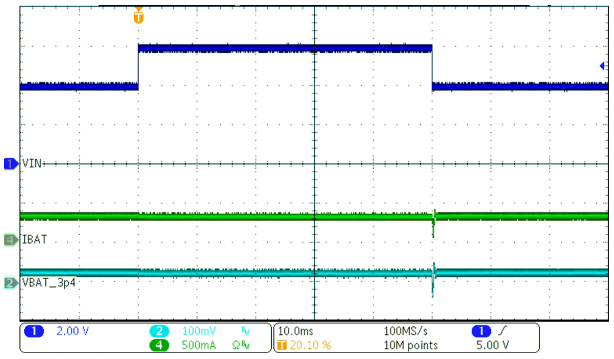
/CE pulled low I_{CHG} = 400 mA

Figure 8-5. Charge Enable



VIN = 5 V → 20 V I_{CHG} = 400 mA

Figure 8-6. IN OVP Response



V_{IN} = 4 V → 6 V V_{OUT} = 3.5 V I_{CHG} = 250 mA

Figure 8-7. IN Transient Response

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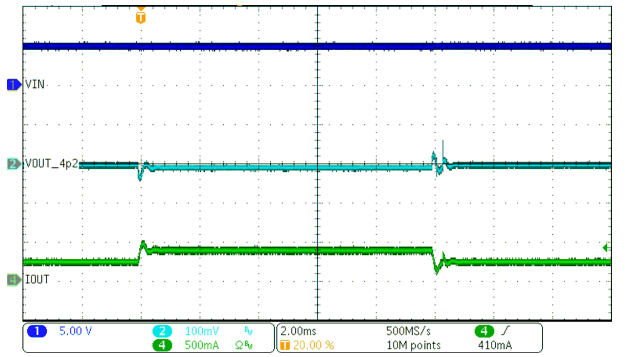
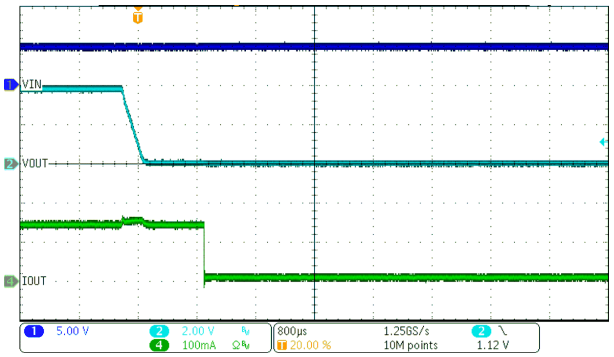


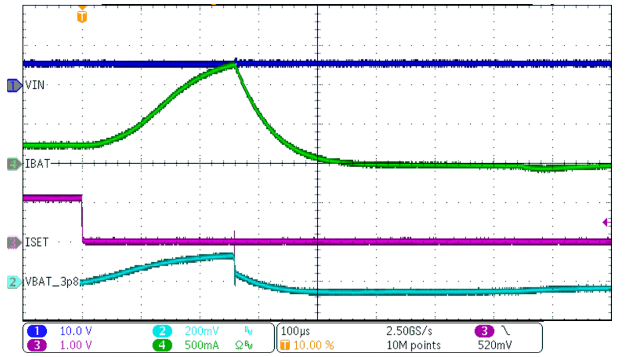
V_{OUT} = 4.2 V I_{SYS} = 0 mA → 500 mA → 0 mA I_{CHG} = 250 mA

Figure 8-8. OUT Transient Response



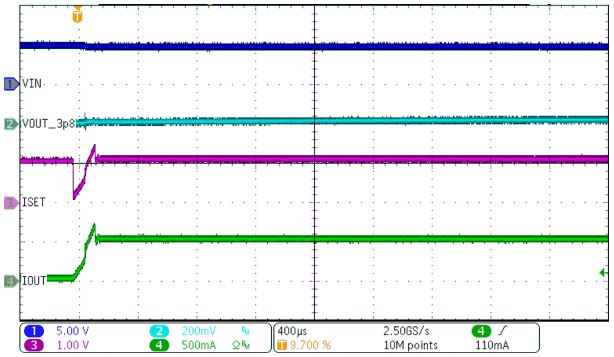
V_{OUT} = 4.0 V → 0 V I_{CHG} = 250 mA

Figure 8-9. OUT Short-Circuit Response



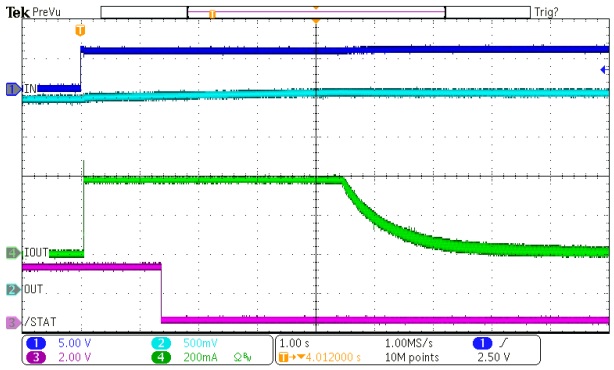
I_{SET} = 1.2 kΩ → 0 Ω

Figure 8-10. ISET Short-Circuit Response



ISET = 50 mA → 500 mA

Figure 8-11. ISET Change Response



V_{REG} = 2.5 V I_{CHG} = 400 mA

Figure 8-12. Charge Complete

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8.2.2 4s Supercapacitor Charger Design Example

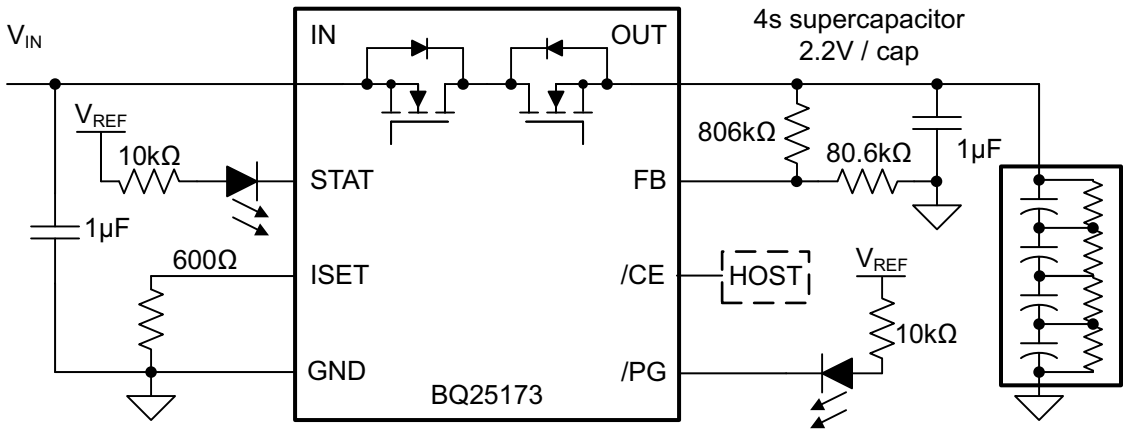

Figure 8-13. BQ25173 4s Supercapacitor Application Diagram

8.2.2.1 Design Requirements

The design requirements include the following:

- Supply voltage is 9 V to 18 V
- Fast charge current: I_{CHG} = 500 mA
- Regulation voltage: V_{REG} = 8.8 V
- $\overline{CE}$ is a control pin, pull high to disable the charger

8.2.2.2 Application Curves

For application curves, refer to Section 8.2.1.3.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0 V and 18 V (up to 40 V tolerant) and current capability of at least the maximum designed charge current. If located more than a few inches from the IN and GND pins, a larger capacitor is recommended.

10 Layout

10.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND and the output filter capacitor from OUT to GND should be placed as close as possible to the device, with short trace runs to both IN, OUT, and GND.

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the supercapacitor. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high-current charge paths into the IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.

10.2 Layout Example

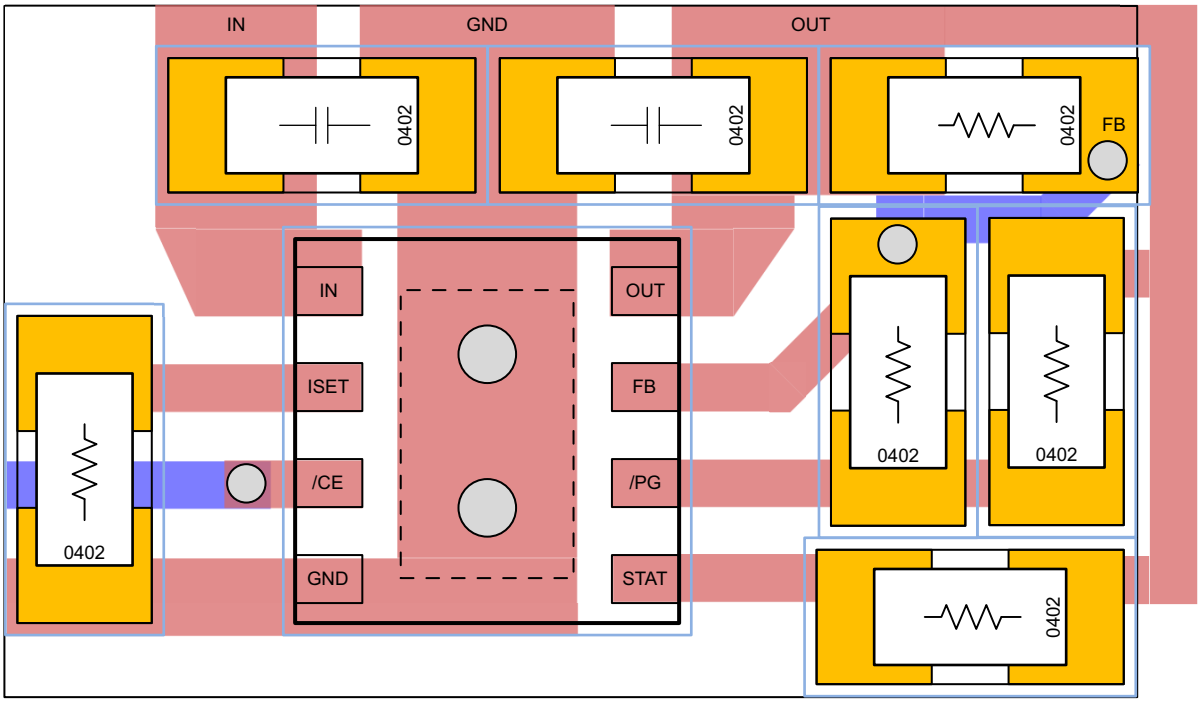

Figure 10-1. BQ25173 Board Layout Example

10.3 Thermal Package

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = (T_J - T) / P \quad (3)$$

Where:

T_J = chip junction temperature
T = ambient temperature
P = device power dissipation

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Factors that can influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of supercapacitors, maximum power dissipation is typically seen at the beginning of the charge cycle when the voltage is at its lowest.

Device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. P can be calculated from the following equation during charging:

$$P = [V_{(IN)} – V_{(OUT)}] \times I_{(OUT)} \quad (4)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for nontypical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

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11 Device and Documentation Support

11.1 Device Support

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To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25173DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B173
BQ25173DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B173

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF BQ25173 :

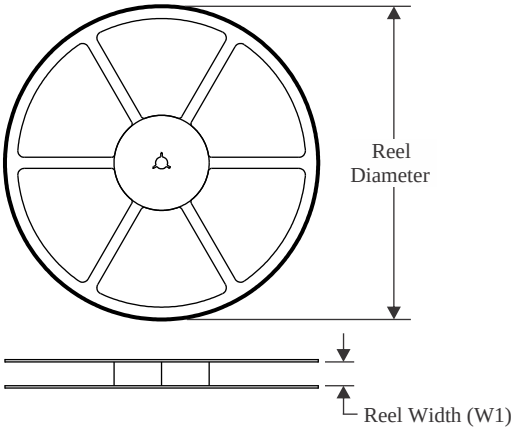
- Automotive : BQ25173-Q1

NOTE: Qualified Version Definitions:

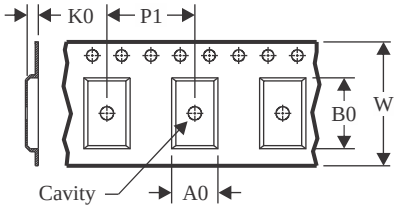
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

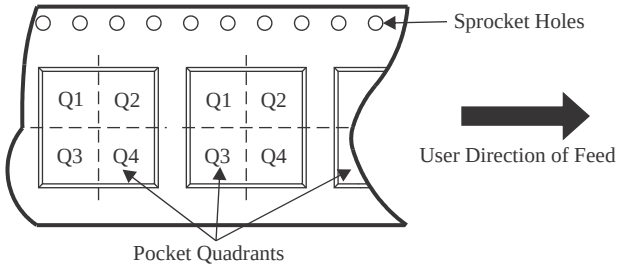


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

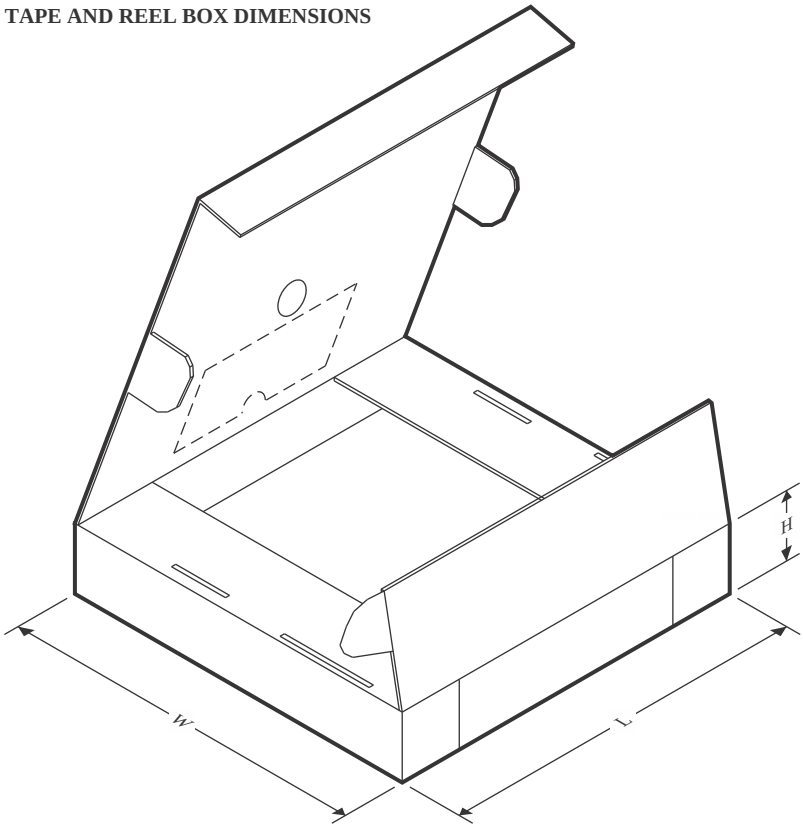
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25173DSGR	WSON	DSG	8	3000	178.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25173DSGR	WSON	DSG	8	3000	208.0	191.0	35.0

GENERIC PACKAGE VIEW

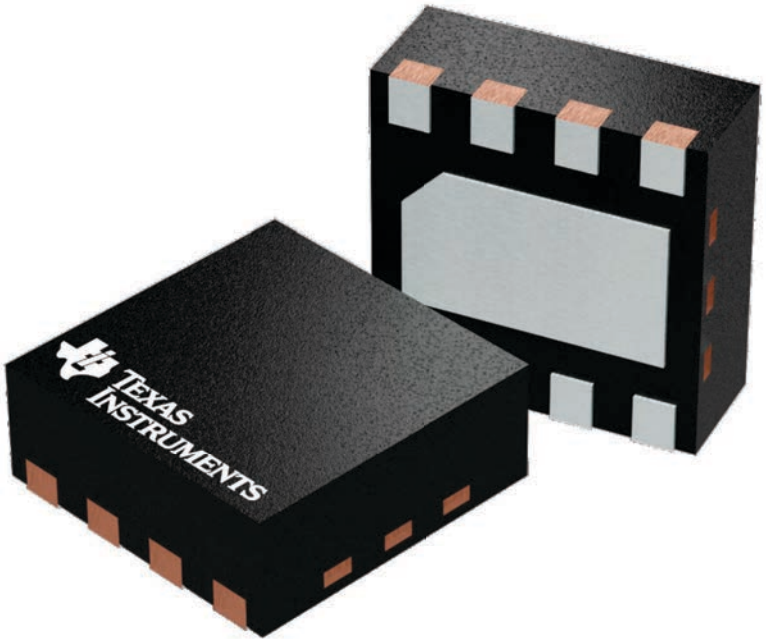
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



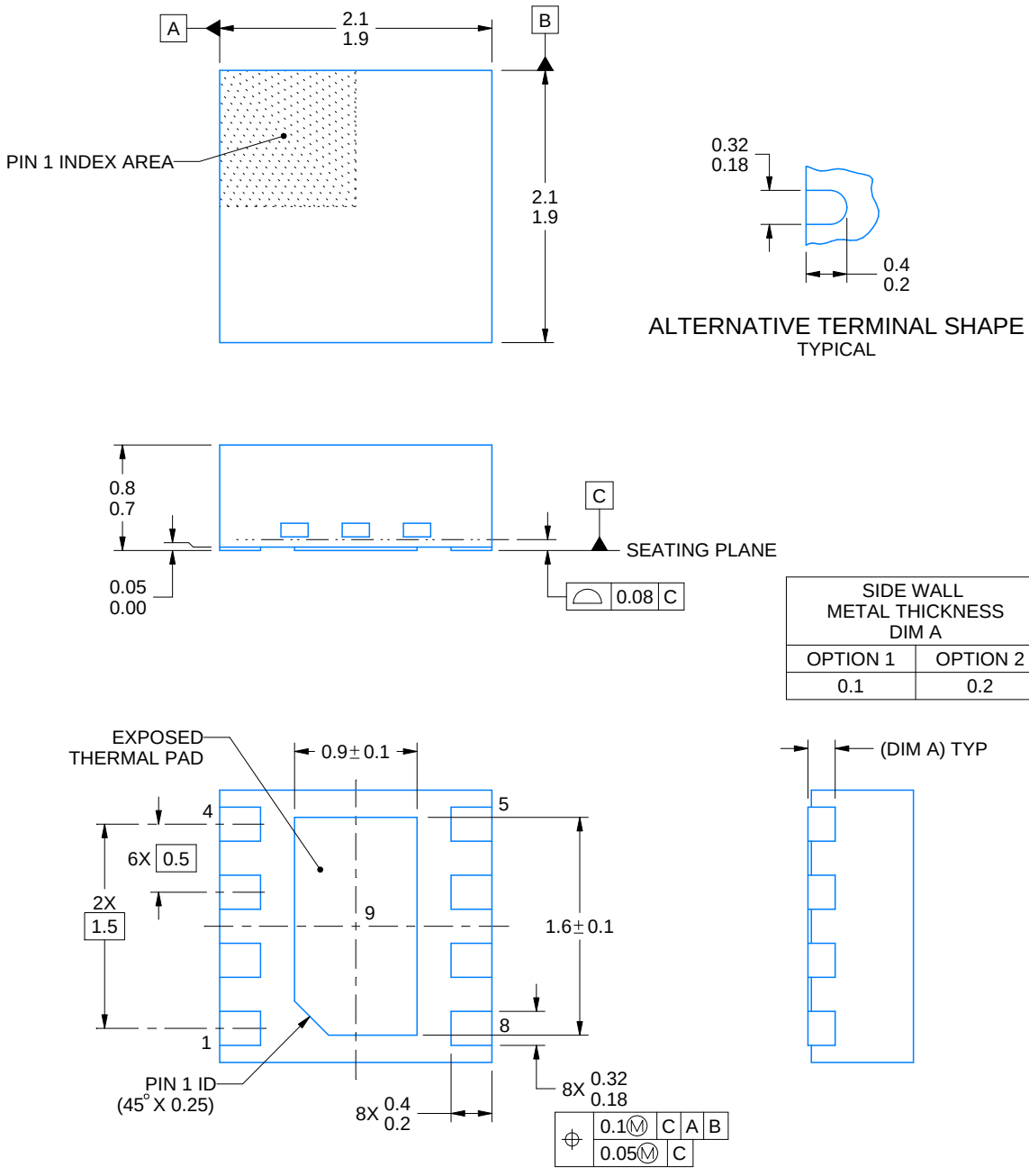
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

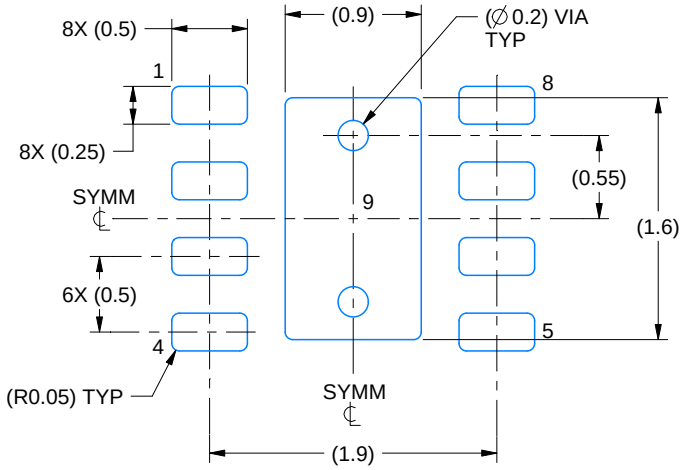
PLASTIC SMALL OUTLINE - NO LEAD



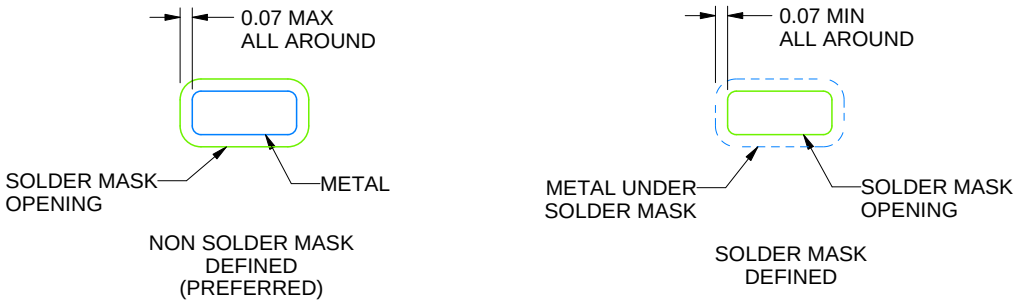
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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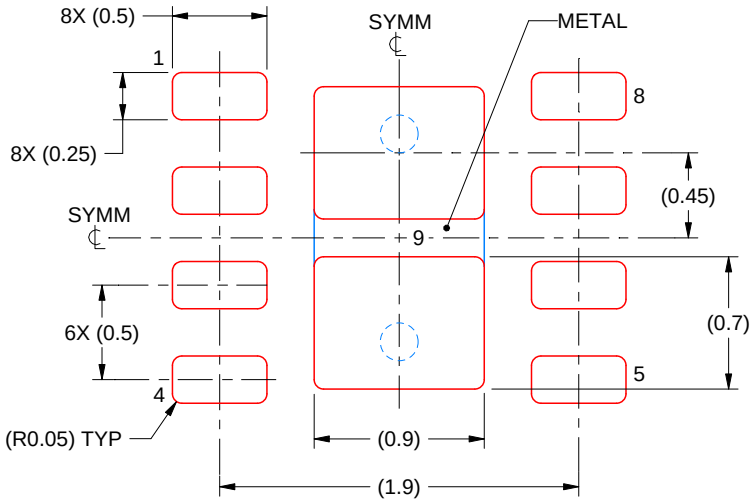
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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