BQ24810 SMBus 1- to 4-Cell Buck Battery Charge Controller With Peak Power, Hybrid Power Boost and Battery Only Boost Modes

1 Features

- Hybrid Power Boost Mode to power up system from adapter and battery together
  - Ultra-fast transient response of 100µs to enter Hybrid Power Boost Mode
  - Ultra-fast ICHG recovery within 60µs after exiting Hybrid Power Boost Mode
- Battery Only Boost Mode to support larger system transients and extend battery run time
- Peak power two-level input current limit to maximize the power from adapter and minimize battery discharge
- Charge 1- to 4-cell battery pack from 4.5V to 24V adapter
- High accuracy power and current monitoring for CPU throttling
  - Comprehensive $\overline{\text{PROCHOT}}$ profile
  - ± 2% Current monitor accuracy
  - ± 5% System Power Monitor Accuracy (PMON)
- Automatic NMOS power source selection from adapter or battery
  - ACFET fast turn on in 100µs when exiting learn mode from battery removal
- Programmable input current, charge voltage, charge and discharge current limit
  - ±0.4% Charge voltage (16mV/step)
  - ±2% Input current (64mA/step)
  - ±2% Charge current (64mA/step)
  - ±2% Discharge current (512mA/step)
- High integration
  - Battery LEARN function
  - Battery present monitor
  - Boost Mode indicator
  - Loop compensation
  - BTST Diode
- Enhanced safety features for overvoltage protection, overcurrent protection, battery, inductor, and MOSFET short-circuit protection
- Switching frequency: 300kHz, 400kHz, 600kHz, and 800kHz
- Realtime system control on ILIM pin to limit charge and discharge current
- 0.65mA Adapter standby quiescent current for Energy Star
- Input current limit (IINDPM) up to 21.12A/10.56A with 5mΩ/10mΩ sense resistor
- V_{SYSMIN} regulation up to 16.128V+2.3V during battery only boost mode

2 Applications

- Standard notebook PC and tablet (multimedia) PC
- Industrial and medical and healthcare equipment
- Personal electronics and portable electronics
- System with battery backup unit (BBU)

3 Description

The BQ24810 device is a high-efficiency, synchronous buck multi-chemistry battery charger supporting 1-, 2-, 3-, or 4-series Li+ cells, or other battery chemistries up to 19.2V.

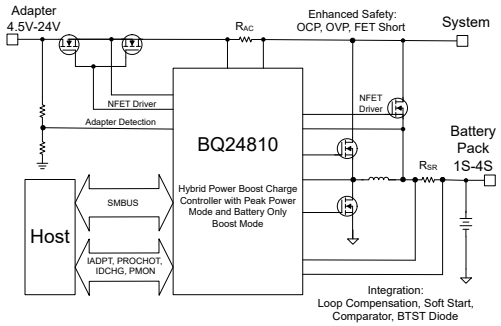
Through SMBus, a host microcontroller programs charge current, charge voltage, input current limit and discharge current limit with high regulation accuracies. Additionally, the BQ24810 supports a two level input current limit (Peak Power mode) to fully utilize the adapter capabilities and reduce battery discharge. The BQ24810 provides adapter current (IADP), battery discharge current (IDCHG), and system power (PMON) signals to the host microcontroller and outputs the $\overline{\text{PROCHOT}}$ signal to throttle back CPU speed when needed.

The BQ24810 supports hybrid power boost mode to boost the battery voltage to supplement the adapter when system power demand is temporarily higher than the adapter is able to provide. When the adapter is not present, the BQ24810 supports battery only boost mode to boost the battery voltage above the minimum system operating voltage, providing more headroom to support system transients.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
BQ24810	RUY (WQFN 28)	4.00mm × 4.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

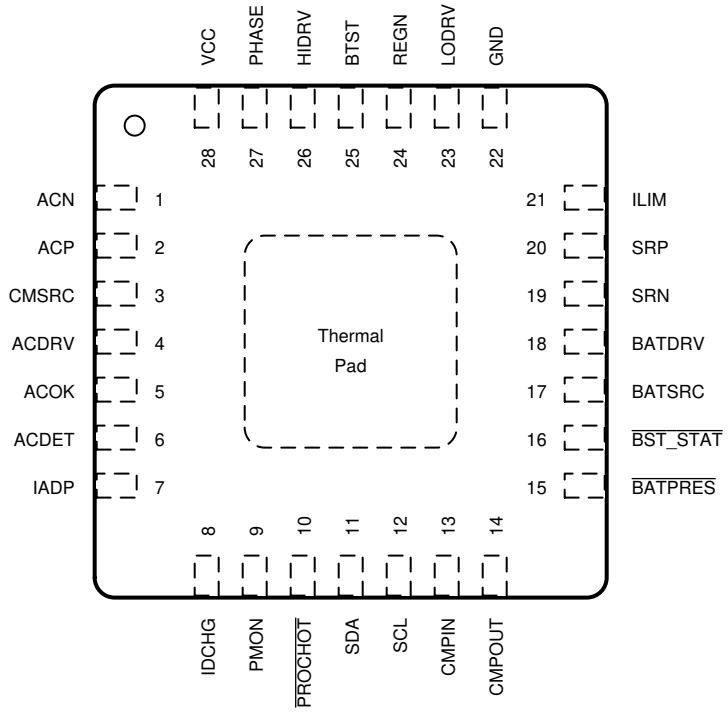


Figure 4-1. RUY Package 28-Pin WQFN Top View

Table 4-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
ACN	1	Input current sense resistor negative input. Place an optional 0.1-µF ceramic capacitor from ACN to GND for common-mode filtering. Place a 0.1-µF ceramic capacitor from ACN to ACP to provide differential mode filtering.
ACP	2	Input current sense resistor positive input. Place a 0.1-µF ceramic capacitor from ACP to GND for common-mode filtering. Place a 0.1-µF ceramic capacitor from ACN to ACP to provide differential-mode filtering.
CMSRC	3	ACDRV charge pump source input. Place a 4-kΩ resistor from CMSRC to the common source of ACFET (Q1) and RBFET (Q2) to limit the inrush current on CMSRC pin.
ACDRV(BQ 24810)	4	Charge pump output to drive both adapter input N-channel MOSFET (ACFET) and reverse blocking N-channel MOSFET (RBFET). ACDRV voltage is 6 V above CMSRC when ACOK is HIGH. ACDRV voltage is equal to CMSRC pin when ACOK is low. Place a 4-kΩ resistor from ACDRV to the gate of ACFET and RBFET limits the inrush current on ACDRV pin.
ACOK	5	Active HIGH AC adapter detection open drain output. It is pulled HIGH to external pull-up supply rail by external pull-up resistor when a valid adapter is present (ACDET above 2.4 V, VCC above UVLO but below ACOV and VCC above BAT). If any of the above conditions is not valid, ACOK is pulled LOW by internal MOSFET. Connect a 10-kΩ pull-up resistor from ACOK to the pull-up supply rail.
ACDET	6	Adapter detection input. Program adapter valid input threshold by connecting a resistor divider from adapter input to ACDET pin to GND pin. When ACDET pin is above 0.6 V and VCC is above UVLO, REGN LDO is present, ACOK comparator, input current buffer (IADP), discharge current buffer (IDCHG), independent comparator, and power monitor buffer (PMON) can be enabled with SMBus. When ACDET is above 2.4 V, and VCC is above SRN but below ACOV, ACOK goes HIGH. Total resistance from Adapter to ACDET to GND varies from 100 kΩ to 1 MΩ.
IADP	7	Buffered adapter current output. V_{IADP} = 20 or 40 × (V_{ACP} – V_{ACN}) The ratio of 20x and 40x is selectable with SMBus. Place 100-pF (or less) ceramic decoupling capacitor from IADP pin to GND. This pin can be floating if this output is not in use.
IDCHG	8	Buffered discharge current. V_{IDCHG} = 8 or 16 × (V_{SRN} – V_{SRP}) The ratio of 8x or 16x is selectable with SMBus. Place 100-pF (or less) ceramic decoupling capacitor from IDSCHG pin to GND. This pin can be floating if this output is not in use.

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Table 4-1. Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
PMON	9	Buffered system power output. The output current is proportional to the total power from the adapter and battery together. The ratio is selectable through SMBus. Place a resistor from PMON pin to GND to generate PMON voltage. Place a 100-pF (or less) ceramic decoupling capacitor from PMON pin to GND. The pin voltage is clamped to a maximum of 3.3 V.
$\overline{\text{PROCHOT}}$	10	Active low, open-drain output of the processor hot indicator. The charger IC monitors events like adapter current, battery discharge current. After any event in the $\overline{\text{PROCHOT}}$ profile is triggered, signal is asserted low. Connect a 500-Ω pull-up resistor from $\overline{\text{PROCHOT}}$ pin to the CPU V_{tt} supply rail (commonly 1.05 V.)
SDA	11	SMBus open-drain data I/O. Connect to SMBus data line from the host controller or smart battery. SMBus communication starts when VCC is above UVLO. Connect a 10-kΩ pull-up resistor according to SMBus specifications.
SCL	12	SMBus open-drain clock input. Connect to SMBus clock line from the host controller or smart battery. SMBus communication starts when VCC is above UVLO. Connect a 10-kΩ pull-up resistor according to SMBus specifications.
CMPIN	13	Input of independent comparator. Internal reference, output polarity and deglitch time are selectable by SMBus. Place a resistor between CMPIN and CMPOUT to program hysteresis when the polarity is HIGH. If comparator is not in use, CMPIN is tied to ground, and CMPOUT is left floating.
CMPOUT	14	Open-drain output of independent comparator. Place 10-kΩ pull-up resistor from CMPOUT to pull-up supply rail. Comparator reference, output polarity and deglitch time are selectable by SMBus. The comparator is active when REGN is available. If comparator is not in use, CMPIN is tied to ground, and CMPOUT is left floating.
$\overline{\text{BATPRES}}$	15	Active low battery present input signal. Low indicates battery present, high indicates battery absent. The device exits the LEARN function and turns on ACFET/RBFET if $\overline{\text{BATPRES}}$ pin is pulled HIGH. Note that ACFET/RBFET is not driven on until BATFET has been turned off in order to protect against adapter to battery short. Upon $\overline{\text{BATPRES}}$ from LOW to HIGH, battery charging and hybrid power boost mode are disabled. The host can enable charging and hybrid power boost mode by write to REG0x14() and REG0x15() when $\overline{\text{BATPRES}}$ is HIGH.
$\overline{\text{BST_STAT}}$	16	Active low, open-drain output for hybrid power boost mode indication. It is pulled low when the IC is operating in either hybrid boost mode or battery only boost mode. Otherwise, it is pulled HIGH. Connect a 10-kΩ pull-up resistor from $\overline{\text{BST_STAT}}$ pin to the pull-up supply rail.
BATSRC	17	Connect to the source of N-channel BATFET. BATDRV voltage is 6 V above BATSRC to turn on BATFET. Place a 10-Ω resistor from BATSRC to the source of BATFET to limit the inrush current on BATSRC pin.
BATDRV	18	Charge pump output to drive N-channel MOSFET between battery and system (BATFET). BATDRV voltage is 6 V above BATSRC to turn on BATFET and power system from battery. BATDRV is shorted to BATSRC to turn off BATFET. Place a 4-kΩ resistor from BATDRV to the gate of BATFET to limit the inrush current on BATDRV pin.
SRN	19	Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN pin with a 0.1-µF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-µF ceramic capacitor from SRP to SRN to provide differential mode filtering. Place a 10-Ω resistor at the SRN pin to protect against reverse-polarity battery insertion.
SRP	20	Charge current sense resistor positive input. Connect SRP pin with a 0.1-µF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-µF ceramic capacitor from SRP to SRN to provide differential mode filtering. Place a 10-Ω resistor at the SRP pin to protect against reverse-polarity battery insertion.
ILIM	21	Charge current and discharge current limit. $V_{ILIM} = 20 \times (V_{SRP} - V_{SRN})$ for charge current and $V_{ILIM} = 5 \times (V_{SRN} - V_{SRP})$ for discharge current. Program ILIM voltage by connecting a resistor divider from system reference 3.3-V rail to ILIM pin to GND pin. The lower of ILIM voltage and 0x14() (for charge) or 0x39 (for discharge) reference sets actual regulation limit. Charging and Hybrid Boost are disabled if ILIM is pulled below 90 mV.
GND	22	IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through pad underneath IC.
LODRV	23	Low-side power MOSFET driver output. Connect to low-side N-channel MOSFET gate.
REGN	24	6-V linear regulator output supplied from VCC. The LDO is active when ACDET above 0.6 V, VCC above UVLO. Connect a ≥ 2.2-µF 0603 ceramic capacitor from REGN to GND. The diode between REGN and BTST is integrated.
BTST	25	High-side power MOSFET driver power supply. Connect a 47-nF capacitor from BTST to PHASE. The diode between REGN and BTST is integrated inside the IC.
HIDRV	26	High-side power MOSFET driver output. Connect to the high side N-channel MOSFET gate.
PHASE	27	High-side power MOSFET driver source. Connect to the source of the high-side N-channel MOSFET.

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Table 4-1. Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
VCC	28	Input supply to power the IC. Use 10-Ω resistor and 1-μF capacitor to ground as a low pass filter to limit inrush current. A diode OR is connected to VCC. It powers te charger IC from input adapter or system rail if battery only boost mode is supported. The diode OR instead powers the charger IC from adapter or battery rail if battery only boost mode is not supported. Refer to Section 7 for examples with and without battery only boost support.
Thermal Pad	–	Exposed pad beneath the IC. Analog ground and power ground star-connected only at the thermal pad plane. Always solder the thermal pad to the board and have vias on the thermal pad plane connecting to analog ground and power ground planes. It also serves as a thermal pad to dissipate heat.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	SRN, SRP, ACN, ACP, CMSRC, VCC, BATSRC	–0.3	30	V
	PHASE	–2	30	V
	ACDET, SDA, SCL , LODRV, REGN, IADP, IDCHG, PMON, ILIM, ACOK, CMPIN, CMPOUT, $\overline{\text{BATPRES}}$, $\overline{\text{BST_STAT}}$	–0.3	7	V
	$\overline{\text{PROCHOT}}$	–0.3	5.7	V
	BTST, HIDRV, ACDRV, BATDRV	–0.3	36	V
Differential Voltage	BTST-PHASE, HIDRV-PHASE, ACDRV-CMSRC, BATDRV-BATSRC	–0.3	7	V
	ACP-ACN, SRP-SRN	–0.5	0.5	V
Transient Voltage	LODRV (2% duty cycle)	–4	7	V
	HIDRV (2% duty cycle)	–4	36	V
	PHASE (2% duty cycle)	–4	30	V
	REGN (5 ms)	–0.3	9	V
Output Sink Current	ACOK, $\overline{\text{BST_STAT}}$, $\overline{\text{PROCHOT}}$		6	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	SRN, SRP, ACN, ACP, CMSRC, VCC, BATSRC	0		24	V
	PHASE	–2		24	V
	ACDET, SDA, SCL , LODRV, REGN, IADP, IDCHG, PMON, ILIM, ACOK, CMPIN, CMPOUT, $\overline{\text{BATPRES}}$, $\overline{\text{BST_STAT}}$	0		6.5	V
	/PROCHOT	–0.3		5	V
	BTST, HIDRV, ACDRV, BATDRV	0		30	V
Differential Voltage	ACP-ACN, SRP-SRN	–0.4		0.4	V
Output Sink Current	ACOK, $\overline{\text{BST_STAT}}$, $\overline{\text{PROCHOT}}$			6	mA
T_J	Junction temperature	–40		125	°C

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Storage temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC[1]		BQ24810 RUY (WQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Current with battery only (T_J=0-85C), (SRP, SRN, BATSRC, PHASE, VCC, ACP, ACN)	V_{BAT} = 16.8V, VCC disconnected to battery, REG0x12[15]=1			5	µA
		V_{BAT} = 16.8V, VCC connected to battery, REG0x12[15]=1		25	44	µA
		V_{BAT} = 16.8V, VCC connect to battery, BATFET on, REG0x12[15]=0, REGN on, Comparator and /PROCHOT enabled, PMON and boost mode disabled		700	800	µA
		V_{BAT} = 16.8V, VCC connect to battery, BATFET on, REG0x12[15]=0, REGN on, Comparator, /PROCHOT and PMON enabled, boost mode disabled		1100	1200	µA
		V_{BAT} = 13.5V, VCC connect to battery, BATFET on, REG0x12[15]=0, REGN on, Comparator, /PROCHOT, PMON and boost mode enabled, but not switching.		1.8		mA
I_{Q_VBUS}	Quiescent input current (VBUS)	V_{VCC_ULVO}<V_{VCC}<V_{ACOVP}, V_{ACDET}> 2.4V, charge disabled		0.65	0.80	mA
		V_{VCC_ULVO}<V_{VCC}<V_{ACOVP}, V_{ACDET} >2.4V, charge enabled, no switching		1.60	3.00	mA
		V_{VCC_ULVO}<V_{VCC}<V_{ACOVP}, V_{ACDET} >2.4V, charge enabled, switching, MOSFET Qg 4nC		10		mA
REGN LDO						
V_{REGN_REG}	REGN Regulator Voltage	V_{VCC} =10V, V_{ACDET}>V_{wakeup_RISE}	5.7	6.0	6.3	V

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5.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{REGN_LIM}	REGN Current Limit	V_{REGN} = 4.0V, V_{VCC} > $V_{UVLO,}$ in charging mode	80	100		mA
		V_{REGN} = 4.0V, V_{VCC} > $V_{UVLO,}$ Not in charging mode	13			mA
$V_{REGN_DROPOUT}$	REGN Output Voltage Dropout	V_{VCC} = 5V, I_{LOAD}=20mA	4.4	4.6	4.75	V
I_{REGN_TSHUT}	REGN Output under thermal shutdown	V_{REGN}=5V	13	23		mA
C_{REGN}	REGN Output Capacitor	I_{LOAD} = 100uA to 50mA		2		µF
VCC / VBAT SUPPLY						
V_{VBUS_OP}	VBUS operating range		4.5		24	V
$V_{VCC_UVLOZ_RISE}$	Input Undervoltage Rising Threshold	V_{VCC} rising	2.4	2.6	2.8	V
$V_{VCC_UVLOZ_FALL}$	Input Undervoltage Falling Threshold	V_{VCC} falling	2.2	2.4	2.6	V
$V_{VCC_UVLOZ_HYS}$	Input Undervoltage Falling Hysteresis	V_{VCC} falling		200		mV
V_{SLEEP_FALL}	Sleep Falling Threshold to turnoff ACFET	VCC ramps down to SRN	–40	25	100	mV
V_{SLEEP_RISE}	Sleep Rising Threshold to turnon ACFET	VCC ramps up above SRN	280	400	520	mV
V_{WAKEUP_RISE}	WAKEUP Detect Rising Threshold	V_{VCC}>V_{VCC_UVLOZ}, ACDET ramps up		0.57	0.80	V
V_{WAKEUP_FALL}	WAKEUP Detect Falling Threshold	V_{VCC}>V_{VCC_UVLOZ}, ACDET ramps down	0.3	0.51		V
V_{ACOK_RISE}	ACOK Rising Threshold	V_{VCC}>V_{VCC_UVLOZ}, ACDET ramps up	2.375	2.4	2.43	V
V_{ACOK_FALL}	ACOK Falling Threshold	V_{VCC}>V_{VCC_UVLOZ}, ACDET ramps down	2.3	2.345	2.40	V
V_{ACOV_RISE}	VCC Overvoltage Rising Threshold	VCC ramps up	24	26	28	V
V_{ACOV_FALL}	VCC Overvoltage Falling Threshold	VCC ramps down	22	25	27	V
V_{ACNSRN_FALL}	ACN to BAT Falling Threshold to turn on BATFET	ACN ramps down towards SRN	120	200	280	mV
V_{ACNSRN_RISE}	ACN to BAT Rising Threshold to turn off BATFET	ACN ramps above SRN	220	290	360	mV
$V_{BATDEPL_FALL}$	Battery Depletion Falling Threshold, as percentage of voltage regulation limit. Exit boost mode and learn mode.	REG0x3B[15:14]=00	56	60	64	%
		REG0x3B[15:14]=01	60	65	68	%
		REG0x3B[15:14]=10	64	68	72	%
		REG0x3B[15:14]=11	68	72	78	%
$V_{BATDEPL_RISE}$	Battery Depletion Rising Hysteresis	REG0x3B[15:14]=00	285	370	500	mV
		REG0x3B[15:14]=01	300	390	530	mV
		REG0x3B[15:14]=10	320	420	565	mV
		REG0x3B[15:14]=11	340	445	600	mV
$V_{BATLOWV_FALL}$	Battery LOWV Falling Threshold	SRN ramps down	2.3	2.5	2.8	V
$V_{BATLOWV_RISE}$	Battery LOWV Rising Threshold	SRN ramps up		2.7		V
$I_{BATLOWV}$	Battery LOWV charge current limit	R_{SR} = 10 mΩ		500		mA
ACFET/RBFET and BATFET DRIVERS						
I_{ACFET}	ACDRV Charge Pump Current Limit(BQ24810)	V_{ACDRV}-V_{CMSRC}=4.5V	32.5	60		µA
V_{DRV_ACFET}	Gate Drive Voltage on ACFET with no load (BQ24810)	V_{ACDRV}-V_{CMSRC} when V_{VCC}>V_{UVLO}	5.7	6.1	6.5	V
R_{ACDRV_OFF}	ACDRV Turnoff Resistance(BQ24810)		9.0	9.7	10.4	kΩ
I_{BATFET}	BATDRV Charge Pump Current Limit	V_{BATDRV}-V_{BATSRC}=5V	40	60		µA

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5.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DRV_BATFET}	Gate Drive Voltage on BATFET	V_{BATDRV}-V_{BATSRC} when V_{SRN}>V_{BAT_UVLO}	5.5	6.1	6.8	V
R_{BATDRV_OFF}	BATDRV Turnoff Resistance		5	6.2	7.4	kΩ
R_{BATDRV_LOAD}	Minimum Load between gate and source		500			kΩ
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		1.024		19.2	V
V_{REG_STEP}	Typical charge voltage step			16		mV
V_{REG_ACC}	Charge voltage accuracy	ChargeVoltage() = 0x41A0		16.800		V
		-10C-85C	–0.4		0.4	%
		-40C-125C	–0.5		0.5	%
		ChargeVoltage() = 0x3130		12.592		V
		-10C-85C	–0.4		0.4	%
		-40C-125C	–0.5		0.5	%
		ChargeVoltage() = 0x20D0		8.400		V
		-10C-85C	–0.4		0.4	%
		-40C-125C	–0.6		0.6	%
		ChargeVoltage() = 0x1060		4.192		V
		-10C-85C	–0.5		0.8	%
		-40C-125C	–0.7		0.8	%
I_{CHG_RANGE}	Typical charge current regulation range	R_{SR} = 10 mΩ	0		8128	mA
I_{CHG_STEP}	Typical charge current regulation step	R_{SR} = 10 mΩ		64		mA
I_{CHG_ACC}	Charge Current Regulation Accuracy (SRN>2V, R_{SR} = 10 mΩ , -40°C-85°C)	ChargeCurrent() = 0x1000		4096		mA
			–2		2	%
		ChargeCurrent() = 0x0800		2048		mA
			–3		3	%
		ChargeCurrent() = 0x0400		1024		mA
			-5		5	%
		ChargeCurrent() = 0x0200		512		mA
			–10		10	%
		ChargeCurrent() = 0x0100		256		mA
		ChargeVoltage() = 0x20D0, 0x3031, 0x41A0	–16		16	%
		ChargeVoltage() = 0x1060	–20		20	%
		ChargeCurrent() = 0x00C0		192		mA
			–20		20	%
		ChargeCurrent() = 0x0080		128		mA
			–30		30	%
$I_{LEAK_SRP-SRN}$	SRP and SRN Leakage Mismatch		–8		8	µA
INPUT CURRENT REGULATION						
I_{LIM1_RANGE}	Typical input current regulation range	R_{AC} = 10 mΩ	0		10560	mA
I_{LIM1_STEP}	Typical Input Current Regulation Step	R_{AC} = 10 mΩ		64		mA

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5.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM1_ACC}	Input Current Regulation Accuracy (0-85℃)	R_{AC} = 10 mΩ, InputCurrent() = 0x1000		4096		mA
			–2		2	%
		R_{AC} = 10 mΩ, InputCurrent() = 0x0800		2048		mA
			–3		3	%
		R_{AC} = 10 mΩ, InputCurrent() = 0x0400		1024		mA
			–5		5	%
$I_{LEAK_ACP-ACN}$	ACP and ACN Leakage Mismatch		–5		5	µA
PEAK POWER MODE						
T_{OVLD}	Peak Power Overload Period	REG0x38[15:14]= 00	0.59		1.00	mS
		REG0x38[15:14]= 01	1.3		2.0	mS
		REG0x38[15:14]= 10	3.1		5.0	mS
		REG0x38[15:14]= 11	7.0		10.1	mS
T_{MAX}	Peak Power Cycle Period	REG0x38[9:8]= 00	17.0	20	23.4	mS
		REG0x38[9:8]= 01	34	40	46	mS
		REG0x38[9:8]= 10	68	80	92	mS
		REG0x38[9:8]= 11	935	1100	1265	mS
I_{LIM2_ACC}	Peak Current Limit Accuracy	InputCurrent() = 0x1000, REG0x3C[14:11]=1001		6144		mA
			97		101	%
		InputCurrent() = 0x0800, REG0x3C[14:11]=1001		3072		mA
			96		102	%
		InputCurrent() = 0x0400, REG0x3C[14:11]=1001		1536		mA
			98		109	%
		InputCurrent() = 0x0200, REG0x3C[14:11]=1001		768		mA
			94	107	114	%
BATTERY DISCHARGE CURRENT REGULATION (HYBRID POWER BOOST MODE)						
V_{IDCHG_RNG}	DIscharge Current Regulation Range	R_{SR} = 10 mΩ	0		32256	mA
I_{IDCHG_STEP}	Discahrge Current Regulation Step	R_{SR} = 10 mΩ		512		mA
I_{DCHG_ACC}	Discharge Current Regulation Accuracy(-40℃-85℃)	DischargeCurrent() = 0x2000		8192		mA
			–2		2	%
		DischargeCurrent() = 0x1000		4096		mA
			–3		3	%
		DischargeCurrent() = 0x0800		2048		mA
			–5		5	%
		DischargeCurrent() = 0x0400		1024		mA
			–8		8	%
		DischargeCurrent() = 0x0200		512		mA
			–10		10	%
BATTERY ONLY BOOST MODE						
V_{SYSMIN_RNG}	Minimum System Voltage Range (System Voltage Regulation is 1.5 or 2.3V higher)		5.632		16.128	V
V_{SYSMIN_STEP}	Typical System Voltage Regulation Step			256		mV

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5.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SYSMIN_ACC}	System Voltage Regulation Accuracy	VSYSMIN() = 0x2600		9.728		V
			–2.2		2.8	%
		VSYSMIN() = 0x1980		6.656		V
			–2.2		2.8	%
V_{SYSMIN_ENTER}	System Voltage Falling Threshold to enter Battery Boost	As percentage of VSYSMIN		100		%
CURRENT SENSE AMPLIFIER						
V_{IADP}	IADP Output Voltage Range		0		3.3	V
I_{IADP}	IADP Output Current				1	mA
A_{IADP}	IADP Sense Amplifier Gain	V_{IADP} / (V_{ACP}- V_{ACN}), REG0x12[4]=0		20		V/V
V_{IADP_ACC}	Current Sense Amplifier Gain Accuracy	V_{ACP}-V_{ACN} = 40mV	–2		2	%
		V_{ACP}-V_{ACN} = 20mV	–4		4	%
		V_{ACP}-V_{ACN} = 10mV	–7		7	%
		V_{ACP}-V_{ACN} = 5mV	–20		20	%
		V_{ACP}-V_{ACN} = 2.5mV	–30		30	%
		V_{ACP}-V_{ACN} = 1.5mV	–40		40	%
V_{IADP_CLAMP}	IADP Clamp Voltage		3		3.3	V
C_{IADP}	IADP Output Load Capacitance	With 0 to 1mA load			100	pF
V_{IDCHG}	IDCHG Output Voltage Range		0		3.3	V
I_{IDCHG}	IDCHG Output Current		0		1	mA
A_{IDCHG}	Current Sense Amplifier Gain	V_{IDCHG} / (V_{SRN}-V_{SRP}), REG0x12[3]=1		16		V/V
V_{IDCHG_ACC}	Current Sense Output Accuracy	V_{SRN}-V_{SRP} = 40mV	–5		5	%
		V_{SRN}-V_{SRP} = 20mV	–9		9	%
		V_{SRN}-V_{SRP} = 10mV	–17		17	%
		V_{SRN}-V_{SRP} = 5mV	–34		34	%
V_{IDCHG_CLAMP}	IDCHG Clamp Voltage		3		3.3	V
C_{IDCHG}	IDCHG Output Load Capacitance	With 0 to 1mA load			100	pF
V_{PMON}	PMON Output Voltage Range		0		3.3	V
I_{PMON}	PMON Output Current		0		100	µA
A_{PMON}	PMON System Gain	I_{PMON} / (P_{IN}+ P_{BAT}), REG0x3B[9]=1		1		µA/W
V_{PMON_ACC}	PMON Gain Accuracy (REG0x3B[9]=1)	Adapter Only with System Power = 19.5V/45W	–4		4	%
		Adapter Only with System Power = 12V/24W	–6		6	%
		Adapter Only with System Power = 5V/9W	–10		10	%
		Battery Only with System Power 11V/44W	–4.5		4.5	%
		Battery Only with System Power 7.4V/ 29.8W	–7		7	%
		Battery Only with System Power 3.7V/ 14.4W	–10		10	%
V_{PMON_CLAMP}	PMON Clamp Voltage		3		3.3	V
INPUT OVER-CURRENT PROTECTION						
V_{ACOC}	Rising Threshold w.r.t. ILIM2 current limit	REG0x37[9]=1	190	200	215	%

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5.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ACOC_CLAMP}	ACOC Threshold Clamp Low Value	V_{ACP}-V_{ACN}	50			mV
V_{ACOC_CLAMP}	ACOC Threshold Clamp High Value	V_{ACP}-V_{ACN}			190	mV
BATTERY OVER-VOLTAGE PROTECTION						
V_{BAT_OVP}	Overvoltage Rising Threshold as percentage of V_{BAT_REG}	SRN ramps up	103	104	105	%
	Overvoltage Falling Threshold as percentage of V_{BAT_REG}	SRN ramps down	101	102	103	%
I_{BAT_OVP}	Discharge Resistor on SRP	V_{SRN}>6V		6		mA
		V_{SRN}=4.5V		2		mA
CONVERTER PROTECTION						
V_{OCP_LIMIT}	Cycle by cycle Over-Current Limit, measured voltage between SRP and SRN.	ChargeCurrent()=0x0xxxH	54	60	66	mV
		ChargeCurrent()=0x1000H-0x17C0H	80	90	100	mV
		ChargeCurrent()=0x1800H-0x1FC0H	110	120	130	mV
V_{UCP_FALL}	Cycle by cycle Under-Current Falling Threshold	SRP ramps down towards SRN	1.0	5	9.00	mV
$V_{LL_FALL_BUCK}$	Light Load Falling Threshold in Buck Mode	SRP ramps down towards SRN		1.25		mV
$V_{LL_RISE_BUCK}$	Light Load Rising Threshold in Buck Mode	SRP ramps above SRN		2.5		mV
$V_{LL_FALL_BOOST}$	Light Load Falling Threshold in Boost Mode	SRN ramps down towards SRP		2.5		mV
$V_{LL_RISE_BOOST}$	Light Load Rising Threshold in Boost Mode	SRN ramps above SRP		5.0		mV
INDUCTOR SHORT, MOSFET SHORT PROTECTION						
$V_{IFAULT_HI_RISE}$	ACN to PH Rising Threshold	REG0x37[7] = 0	450	750	1200	mV
$V_{IFAULT_LO_RISE}$	PH to GND Rising Threshold	REG0x37[6] = 1	165	250	340	mV
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	REG0x12[9:8] = 00	510	600	690	KHz
		REG0x12[9:8] = 01	680	800	920	KHz
		REG0x12[9:8] = 10	255	300	345	KHz
		REG0x12[9:8] = 11	340	400	460	KHz
$R_{DS_HI_ON}$	High-side Driver (HSD) Turnon Resistance	V_{BTST} – V_{PH} = 5.5 V		1.72		Ω
$R_{DS_HI_OFF}$	High-side Driver Turnoff Resistance	V_{BTST} – V_{PH} = 5.5 V		0.59		Ω
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold	V_{BTST} – V_{PH} when LSFET refresh pulse is requested, VBUS = 5V	3.85	4.3	4.7	V
$R_{DS_LO_ON}$	Low-side Driver (LSD) Turnon Resistance			4.5		Ω
$R_{DS_LO_OFF}$	Low-side Driver Turnoff Resistance			0.51		Ω
I_{STEP}	Soft-start Step Size			64		mA
t_{STEP}	Soft-start Step Time			400		us
THERMAL SHUTDOWN						
T_{SHUT_RISE}	Thermal Shutdown Rising threshold	Temperature Increasing		155		°C
T_{SHUT_FALL}	Thermal Shutdown Falling threshold	Temperature Decreasing		135		°C
PROCHOT COMPARATORS						

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5.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ICRIT}	ICRIT comparator threshold	REG0x3C[14:11]=1001, as percentage of input current limit 4096mA	161	165	168	%
V_{INOM}	INOM Comparator Threshold	as percentage of input current limit 4096mA, 0x3F()=0x1000, 0x3C [0] = 0	107	110	112	%
		as percentage of input current limit 4096mA, 0x3F()=0x1000, 0x3C [0] = 1	104	106	108	%
V_{IDCHG}	IDCHG comparator threshold	REG0x3D[15:11]=10000, as voltage between SRN and SRP	160	163.84	167	mV
		REG0x3D[15:11]=00100, as voltage between SRN and SRP	38	40.96	44	mV
V_{VBATT}	VBATT Comparator Threshold (-40℃-85℃)	REG0x3C[7:6]=00	5.71	5.75	5.95	V
		REG0x3C[7:6]=01	5.88	6.00	6.12	V
		REG0x3C[7:6]=10	6.22	6.25	6.46	V
		REG0x3C[7:6]=11	6.48	6.50	6.72	V
MISC COMPARATORS						
V_{CMP_OS}	Independent comparator Input Offset		–4		4	mV
V_{CMP_CM}	Independent comparator Input Common-mode		0		6.5	V
V_{CMP_REF}	Independent comparator Reference Voltage (CMPIN falling)	REG0x3B[7]=0	2.27	2.3	2.32	V
		REG0x3B[7]=1	1.17	1.2	1.22	V
$V_{CMP_RISE_HYST}$	Independent comparator Reference Hysteresis	REG0x3B[6]=0		100		mV
V_{ILIM_FALL}	ILIM as Converter Enable Falling Threshold	V_{ILIM} falling	60	75	90	mV
V_{ILIM_RISE}	ILIM as Converter Enable Rising Threshold	V_{ILIM} rising	90	105	120	mV
ANALOG AND DIGITAL I/O						
I_{AIN_LEAK}	Input bias current	V = 7V	–1		1	µA
V_{IN_LO}	Input high threshold (SDA, SCL)	SDA and SCL pins			0.8	V
V_{IN_HI}	Input low threshold (SDA, SCL)	SDA and SCL pins	2.1			V
I_{DIN_LEAK}	Input bias current (SDA, SCL)	V = 7V, SDA and SCL pins	–1		1	µA
V_{OUT_LO}	Output Saturation Voltage (ACOK, SDA, CMPOUT, /BST_STAT)	5 mA drain current			500	mV
I_{OUT_LEAK}	Leakage Current (ACOK, SDA, CMPOUT, /BST_STAT)	V = 7V	–1		1	uA
$V_{OUT_LO_PH}$	Output Saturation Voltage (/PROCHOT)	17mA drain current			300	mV
$I_{OUT_LEAK_PH}$	Leakage Current (/PROCHOT)	V = 5.5V	–1		1	uA

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
COMPARATOR DEGLITCH					
$t_{ACOK_RISE_DEG}$	ACOK rising deglitch to turnon ACFET, REG0x37[12]=0	100	150	200	ms
	ACOK rising deglitch to turnon ACFET, REG0x37[12]=1	0.9	1.3	1.7	s
$t_{ACOK_FALL_DEG}$	ACOK falling deglitch to turnoff ACFET			3	µs
t_{ACOC_DEG}	Deglitch time to latch off ACFET	4.5	6	7.5	ms

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5.6 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
$t_{BATDEPL_FALL_DEG}$	Battery depletion falling threshold to turnoff BATFET and turnon ACFET in Learn mode.		2		µs
PWM DRIVER TIMING					
$t_{DEADTIME_RISE}$	Driver dead time from low-side to high-side		20		ns
$t_{DEADTIME_FALL}$	Driver deadtime from high-side to low-side		20		ns
SMBus TIMING CHARACTERISTICS					
t_R	SCL/SDA rise time			300	ns
t_F	SCL/SDA fall time			300	ns
$t_{W(H)}$	SCL pulse width high	0.6			µs
$t_{W(L)}$	SCL pulse width low	1.3			µs
$t_{SU(STA)}$	Setup time for START condition	0.6			µs
$t_{H(STA)}$	Start condition hold time after which first clock pulse is generated	0.6			µs
$t_{SU(DAT)}$	Data setup time	100			ns
$t_{H(DAT)}$	Data hold time	0			ns
$t_{SU(STOP)}$	Set up time for STOP condition	0.6			µs
$t_{(BUF)}$	Bus free time between START and STOP conditions	1.3			µs
$F_{S(CL)}$	Clock frequency	10		400	kHz
HOST COMMUNICATION FAILURE					
$t_{TIMEOUT}$	SMBus bus release timeout(1)	25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal	10			ms
t_{WDI}	Watchdog timeout period, REG0x12[14:13]=01	4	5	6	s
	Watchdog timeout period, REG0x12[14:13]=10	70	88	105	s
	Watchdog timeout period, REG0x12[14:13]=11	140	175	210	s

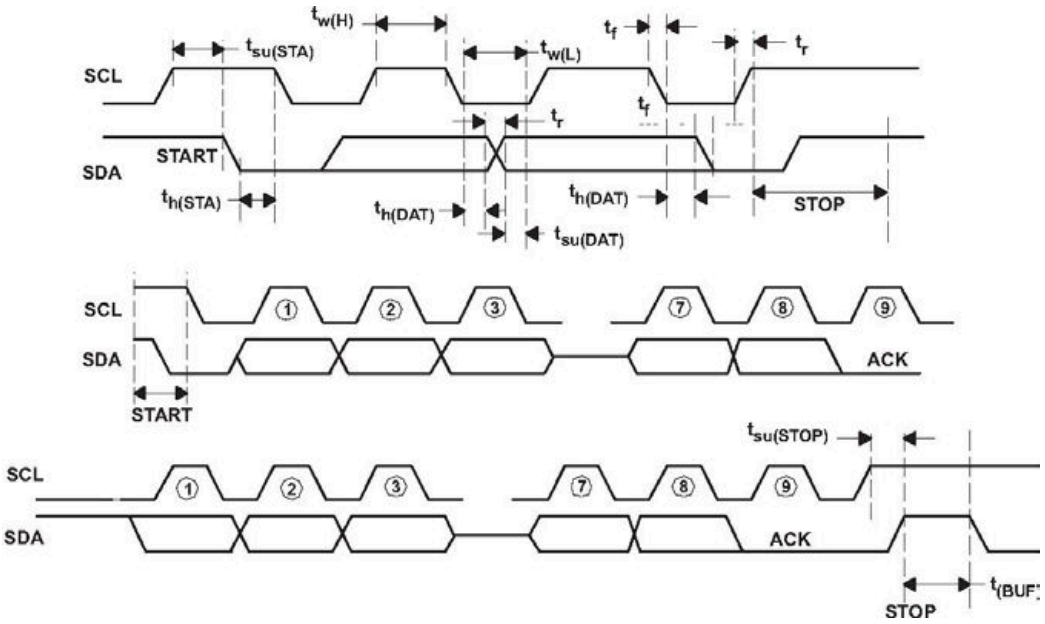


Figure 5-1. SMBus Communication Timing Waveforms

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5.7 Typical Characteristics

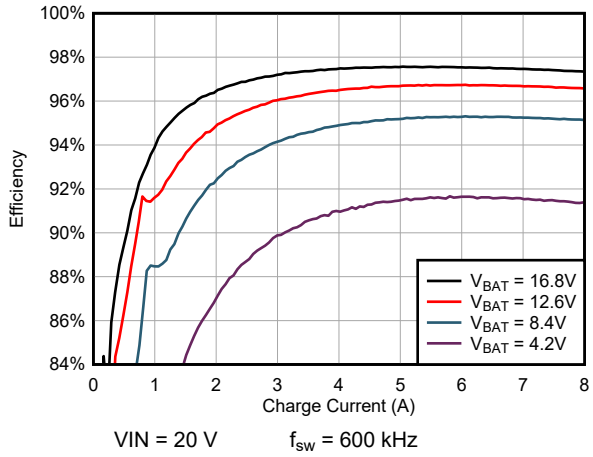


Figure 5-2. Efficiency During Charging

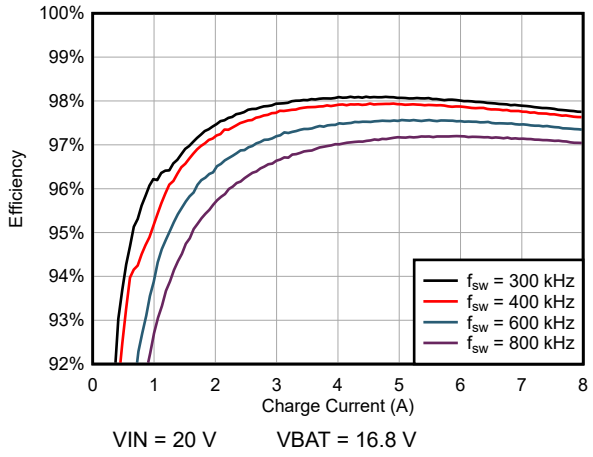


Figure 5-3. Efficiency During Charging

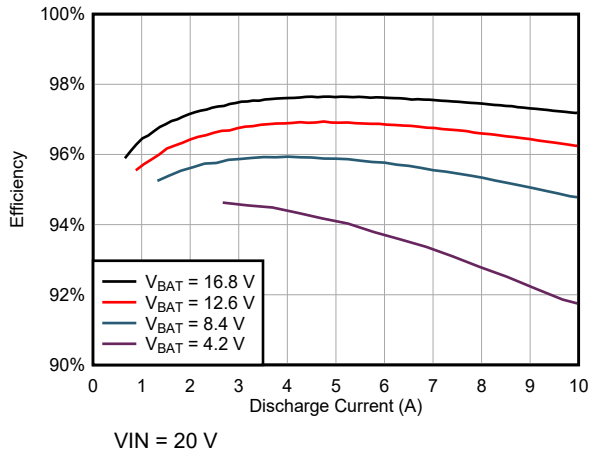


Figure 5-4. Efficiency During Hybrid Boost

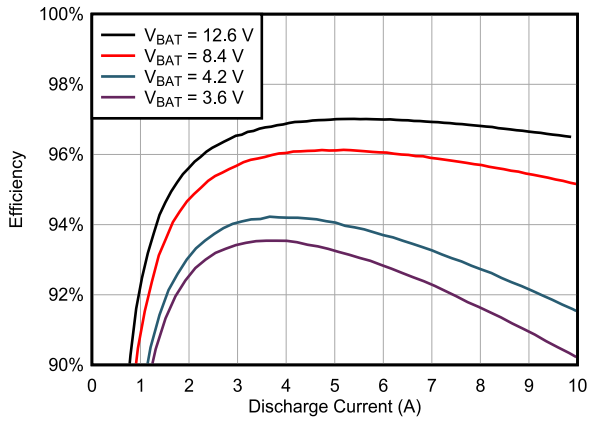


Figure 5-5. Efficiency During Battery Only Boost

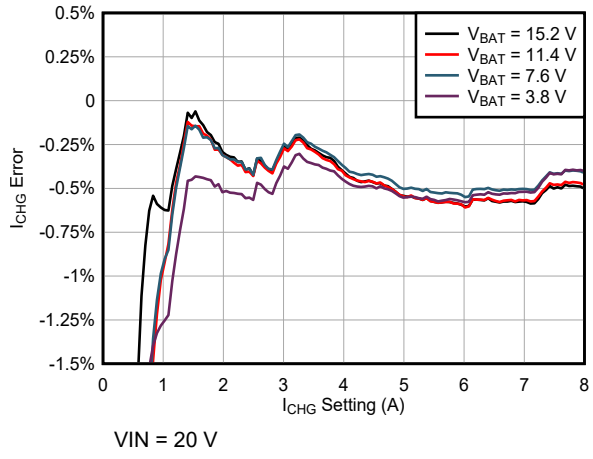


Figure 5-6. Charge Current Accuracy

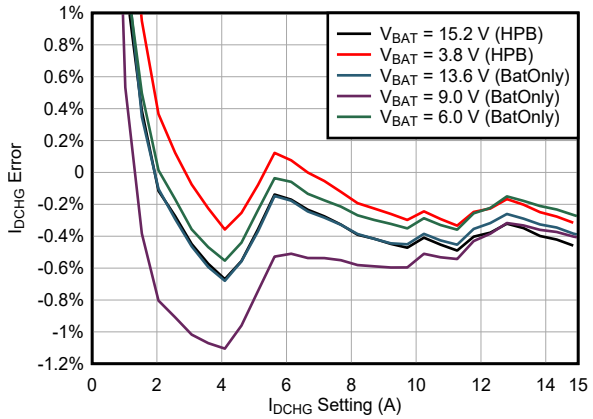
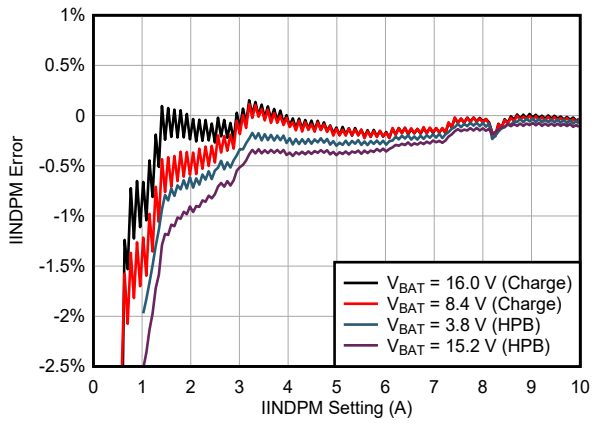


Figure 5-7. Discharge Current Accuracy

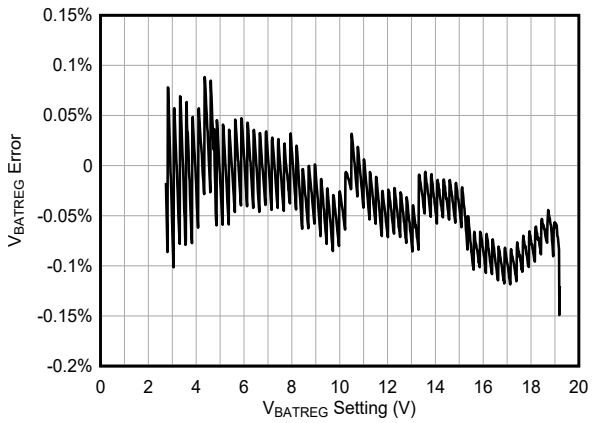
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5.7 Typical Characteristics (continued)



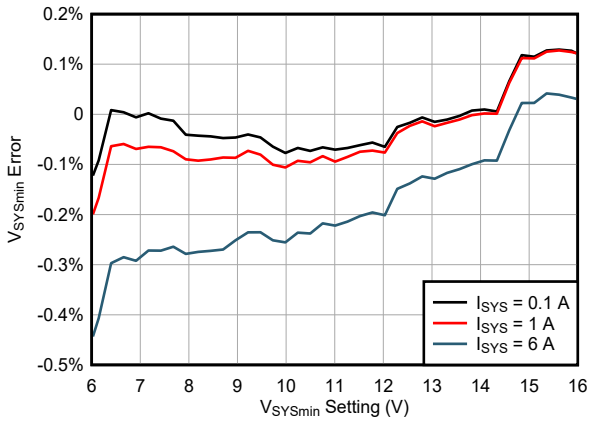
VIN = 20 V

Figure 5-8. Input Current Limit (ILIM1) Accuracy



VIN = 20 V

Figure 5-9. Charge Voltage Accuracy



VIN = 20 V $V_{SYS} = V_{SYSMIN}$ + VBOOST VBOOST = 2.3 V

Figure 5-10. Minimum System Voltage (VSYSMIN) Accuracy

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6 Detailed Description

6.1 Overview

The BQ24810 is a 1-4 cell buck battery charge controller with power selection for space-constrained, multi-chemistry portable applications such as notebook and detachable ultrabook. It supports wide input range of input sources from 4.5 V to 24 V, and 1-4 cell battery for a versatile solution. As a buck charger, it requires an adapter voltage greater than the maximum battery voltage.

The BQ24810 supports automatic system power source selection with separate drivers for n-channel MOSFETS on the adapter side and battery side.

The BQ24810 features Dynamic Power Management (DPM) to limit the input power and avoid AC adapter over-loading. During battery charging, as the system power increases, the charging current will reduce to maintain total input current below adapter rating. If system power demand temporarily exceeds the adapter rating, the BQ24810 supports hybrid power boost mode (previously called "turbo boost mode") to boost the battery voltage through the switching regulator in order to provide supplement current.

Most adapters have the ability to maintain a current level above their nominal rating for a milliseconds or even tens of milliseconds. The BQ24810 has two level input current DPM, also known as Peak Power mode, to allow the user to extend the input current DPM to support a higher input current for a programmable overload time, then allow the adapter to recover by fixing the input current limit at the nominal rating. This allows full utilization of the adapter capabilities to reduce battery discharge.

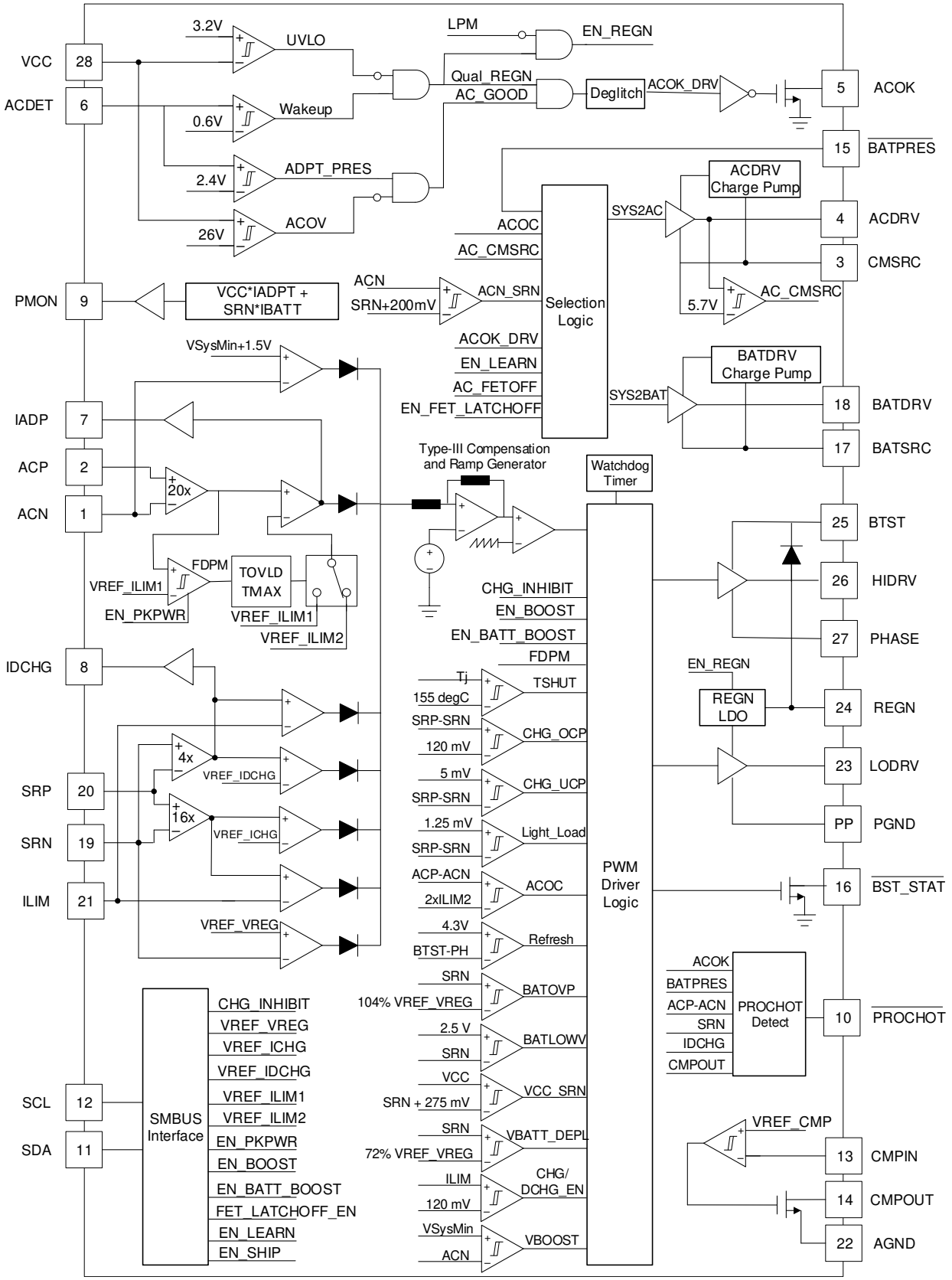
When powering the system directly from the battery without an adapter, the battery voltage may fall below the level required to maintain the system. BQ24810 provides the battery only boost mode to boost the system voltage above the battery voltage, allowing the system to utilize the remaining battery power for extended battery life.

The BQ24810 closely monitors system power (PMON), input current (IADP) and battery discharge current (IDCHG) with highly accurate current sense amplifiers. If current is too high, adapter or battery is removed, a $\overline{\text{PROCHOT}}$ signal is asserted to CPU so that the CPU optimizes its performance to the power available to the system.

The SMBus controls input current, charge current and charge voltage registers with high resolution, high accuracy regulation limits. It also sets the $\overline{\text{PROCHOT}}$ timing and threshold profile to meet system requirements.

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6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Device Power Up

The BQ24810 gets power from adapter or battery. A diode-OR is placed to power VCC from adapter or system rail if battery only boost is supported. This configuration will power up the IC from a battery attach without adapter present via the body diode of the BATFET. If battery only boost is not supported, a diode-OR is placed to power VCC from adapter or directly from battery. After VCC is above its UVLO threshold, the device wakes up from power-on-reset (POR) and starts communication. Refer to Section 7 for examples with and without battery only boost support.

6.3.1.1 Battery Only

When VCC voltage is above UVLO, BQ24810 powers up to turn on BATFET and starts SMBus communication. By default, the BQ24810 stays in low power mode (REG0x12[15] = 1) with lowest quiescent current. When REG0x12[15] is set to 0, the device enters performance mode. User can enable IDCHG buffer, PMON, $\overline{\text{PROCHOT}}$, battery only boost mode or comparator through SMBus. REGN LDO is enabled (except when only IDCHG buffer) for accurate reference during PMON, $\overline{\text{PROCHOT}}$, battery only boost mode and comparator operations.

6.3.1.2 Adapter Detect and ACOK Output

An external resistor divider attenuates the adapter voltage before it goes to ACDET. If the battery boost mode is not used, the adapter detect threshold must be programmed to a value greater than the maximum battery voltage, but lower than the minimum allowed adapter voltage. If the battery only boost mode is used, the adapter detect threshold must instead be programmed to a value that is higher than the system regulation voltage programmed in REG0x38[5] and REG0x3E. When ACDET is above 0.6 V, all bias circuits are enabled.

The open drain ACOK output is pulled to external rail under the following conditions:

- $V_{UVLO} < V_{VCC} < V_{ACOV}$
- $V_{ACDET} > 2.4$ V
- $V_{VCC} – V_{SRN} > V_{SLEEP}$

ACOK HIGH indicates adapter is detected, or adapter present. The REG0x37[11] tracks the status of ACOK pin. ACOK deglitch time is 150 ms at the first time adapter plug-in if REG0x37[12] has not been overwritten since power-on reset. Once the register has been written to, and for all connections after the first connection, the value set by REG0x37[12] (150 ms or 1.3 sec) is used. Since the POR default of this register is 1.3 sec, if it is not overwritten, the first adapter plugin will have an ACOK deglitch time of 150 ms and all subsequent plugins will have an ACOK deglitch time of 1.3 sec.

6.3.1.2.1 Adapter Overvoltage (ACOV)

When the VCC pin voltage is higher than 26 V, it is considered adapter over voltage. ACOK is pulled low, and charging is disabled. ACFET/RBFET are turned off to disconnect the high voltage adapter from the system during ACOV. BATFET is turned on if turn-on conditions are valid.

When VCC voltage falls below 25 V, it is considered a valid adapter voltage. ACOK is pulled high by an external pull-up resistor. BATFET is turned off and ACFET and RBFET are turned on to power the system from the adapter.

6.3.1.3 REGN LDO

REGN LDO functions as an internal reference. When the adapter is present (ACDET pin is above 0.6 V), the REGN LDO is always enabled. When the adapter is removed (ACDET pin is less than 0.6 V), and low power mode is enabled (REG12[15] = 1), the REGN LDO is disabled regardless of other register bits setting. When the adapter is removed and low power mode is disabled (REG0x12[15] = 0), REGN LDO is enabled when any of the below functions is enabled:

- Power monitor function PMON
- Processor hot function $\overline{\text{PROCHOT}}$
- Independent comparator

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6.3.2 System Power Selection

The BQ24810 device automatically switches adapter or battery power to system. An automatic break-before-make logic prevents shoot-through currents when the selectors switch. The system is powered across the body diode of the BATFET during the brief period between the first selector turning off and the second turning on.

The ACDRV drives a pair of common-source (CMSRC) N-channel power MOSFETs (ACFET and RBFET) between the adapter and ACP. The ACFET separates adapter from system and battery, and limits inrush current when the adapter is plugged in by controlling the ACFET turn-on time. Additionally, it protects the adapter when the system or battery is shorted. The RBFET provides negative input voltage protection and battery discharge protection when adapter is shorted to ground, and minimizes system power dissipation with its low $R_{DS(on)}$ compared to a Schottky diode.

When the voltage measured at the ACDET pin is less than 2.4 V, it is determined that a valid adapter is not present. Under this condition, ACDRV is pulled to CMSRC to keep ACFET and RBFET off, isolating the adapter input from the system rail. BATDRV stays at V_{BATSRC} + 6 V to connect battery to system if all of the following conditions are valid:

- $V_{VCC} > V_{UVLO}$
- $V_{ACN} < V_{SRN}$ + 200 mV
- ACFET/RBFET off

When the voltage measured at the ACDET pin is greater than 2.4 V, a valid adapter is determined to be present. Under this condition, the ACDRV is driven above CMSRC to turn ACFET and RBFET on, and the system power source switches from battery to adapter if all of the following conditions are valid:

- ACOK high with all conditions in Section 6.3.1.2 valid.
- Not in LEARN mode
- In LEARN mode and V_{SRN} < battery depletion threshold

The gate drive voltage on ACFET and RBFET is V_{CMSRC} + 6 V. If the ACFET/RBFET have been turned on for 20 ms, and the voltage across gate and source is still less than 5.7 V, ACFET and RBFET are turned off. After 1.3 sec delay, it resumes turning on ACFET and RBFET. If such a failure is detected seven times within 90 seconds, ACFET/RBFET are latched off and an adapter removal is required to force ACDET < 0.6 V to remove the latch. After the latch is reset, ACFET/RBFET can be turned on again.

To turn off ACFET/RBFET, one of the following conditions must be valid:

- In LEARN mode and V_{SRN} is above battery depletion threshold;
- ACOK low

To limit the adapter inrush current during ACFET turn-on, the Cgs and Cgd external capacitor of ACFET must be carefully selected following the guidelines below:

- Minimize total capacitance on system
- Cgs should be 40× or higher than Cgd to avoid ACFET false turn on during adapter hot plug-in
- Fully turn on ACFET within 20 ms, otherwise, charger IC will consider turn-on failure
- Check with MOSFET vendor on peak current rating
- Place 4-kΩ resistor in series with ACDRV, CMSRC, and BATDRV pin to limit inrush current

6.3.3 Current and Power Monitor

6.3.3.1 High Accuracy Current Sense Amplifier (IADP and IDCHG)

As an industry standard, a high-accuracy current sense amplifiers (CSA) are used to monitor the input current (IADP) and the discharge current (IDCHG). IADP voltage is 20X or 40X the differential voltage across ACP and ACN. IDCHG voltage is 8X or 16X the differential voltage across SRN and SRP. After VCC is above UVLO and ACDET is above 0.6 V, IADP output becomes valid. To lower the voltage on current monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

- V_{IADP} = 20 or 40 × (V_{ACP} – V_{ACN}) IADP gain is set in REG0x12[4] with default 20x.
- V_{IDCHG} = 8 or 16 × (V_{SRN} – V_{SRP}) IDCHG gain is set in REG0x12[3] with default 16x.

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A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay. The CSA output voltage is clamped at 3.3 V. To lower the voltage on current monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

6.3.3.2 High Accuracy Power Sense Amplifier (PMON)

The BQ24810 device monitors the power used by the system by adding the power discharged from the battery to the power pulled from the adapter. The PMON pin is a current source with output current proportional to system power. The PMON output current is calculated in Equation 1. A_{PMON} is the ratio of PMON pin output current to system power. It can be set in REG0x3B[9] with default 1 µA/W (REG0x3B[9] = 1) for 10-mΩ R_{AC} and R_{SR} sense resistors. This gain scales with the value of the sense resistors used so that 20-mΩ R_{AC} and R_{SR} instead have a gain of 2 µA/W with the same setting (REG0x3B[9] = 1).

$$I_{PMON} = A_{PMON} (V_{IN} \times I_{IN} + V_{BAT} \times I_{BAT}) \text{ ; } I_{BAT} > 0 \text{ during discharge; } I_{BAT} < 0 \text{ during charge} \quad (1)$$

The BQ24810 device allows an input sense resistor that is 2x or 1/2x of charge sense resistor by setting REG0x3B[13:12] to 01 or 10, respectively. With REG0x3B[13:12] set to 01, the current measurement across R_{SR} is internally doubled so that a 20-mΩ R_{AC} and 10-mΩ R_{SR} will have the same output at the PMON pin as a 20-mΩ R_{AC} and 20-mΩ R_{SR} will have with REG0x3B[13:12] set to 00. With REG0x3B[13:12] set to 10, the current measurement across R_{AC} is doubled instead. A_{PMON} as a function of R_{AC}, R_{SR}, REG0x3B[9] and REG0x3B[13:12] is summarized in Table 6-1. The REG0x3B[13:12] sense ratio must be set as shown in the table for each R_{AC} and R_{SR} combination. The REG0x3B[9] PMON gain may be set to either 0 or 1. The resultant A_{PMON} for each setting is shown.

Table 6-1. PMON Output Current Gain by Setting

R_{AC}	R_{SR}	REG0x3B[13:12] R_{AC} and R_{SR} Ratio	REG0x3B[9] PMON Gain	A_{PMON}
2.5 mΩ	5 mΩ	10 = R_{AC} and R_{SR} 1:2	0 = 0.25 µA/W for 10 mΩ	0.125 µA/W
2.5 mΩ	5 mΩ	10 = R_{AC} and R_{SR} 1:2	1 = 1 µA/W for 10 mΩ	0.5 µA/W
5 mΩ	5 mΩ	00 = R_{AC} and R_{SR} 1:1	0 = 0.25 µA/W for 10 mΩ	0.125 µA/W
5 mΩ	5 mΩ	00 = R_{AC} and R_{SR} 1:1	1 = 1 µA/W for 10 mΩ	0.5 µA/W
10 mΩ	5 mΩ	01 = R_{AC} and R_{SR} 2:1	0 = 0.25 µA/W for 10 mΩ	0.25 µA/W
10 mΩ	5 mΩ	01 = R_{AC} and R_{SR} 2:1	1 = 1 µA/W for 10 mΩ	1 µA/W
5 mΩ	10 mΩ	10 = R_{AC} and R_{SR} 1:2	0 = 0.25 µA/W for 10 mΩ	0.25 µA/W
5 mΩ	10 mΩ	10 = R_{AC} and R_{SR} 1:2	1 = 1 µA/W for 10 mΩ	1 µA/W
10 mΩ	10 mΩ	00 = R_{AC} and R_{SR} 1:1	0 = 0.25 µA/W for 10 mΩ	0.25 µA/W
10 mΩ	10 mΩ	00 = R_{AC} and R_{SR} 1:1	1 = 1 µA/W for 10 mΩ	1 µA/W
20 mΩ	10 mΩ	01 = R_{AC} and R_{SR} 2:1	0 = 0.25 µA/W for 10 mΩ	0.5 µA/W
20 mΩ	10 mΩ	01 = R_{AC} and R_{SR} 2:1	1 = 1 µA/W for 10 mΩ	2 µA/W
10 mΩ	20 mΩ	10 = R_{AC} and R_{SR} 1:2	0 = 0.25 µA/W for 10 mΩ	0.5 µA/W
10 mΩ	20 mΩ	10 = R_{AC} and R_{SR} 1:2	1 = 1 µA/W for 10 mΩ	2 µA/W
20 mΩ	20 mΩ	00 = R_{AC} and R_{SR} 1:1	0 = 0.25 µA/W for 10 mΩ	0.5 µA/W
20 mΩ	20 mΩ	00 = R_{AC} and R_{SR} 1:1	1 = 1 µA/W for 10 mΩ	2 µA/W

A resistor is connected on the PMON pin to convert output current to output voltage with desired scaling. A maximum 100-pF capacitor to GND is recommended as close as possible to the PMON pin for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay. The PMON output voltage is clamped to 3.3 V.

6.3.4 Processor Hot Indication for CPU Throttling

When CPU is running turbo mode, the peak power may exceed total available power from adapter and battery. The BQ24810 provides the $\overline{\text{PROCHOT}}$ output to signal the CPU that an overload condition has occurred. When

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adapter or battery discharge current exceeds the allowed threshold or system voltage drops, this indicates an overload condition has occurred. Likewise, adapter or battery removal may result in insufficient power for the CPU. The processor hot function in the BQ24810 monitors these events, and optionally asserts the $\overline{\text{PROCHOT}}$ signal when they occur.

The $\overline{\text{PROCHOT}}$ triggering events are:

- ICRIT: adapter peak current (110% of I_{LIM2}), internal maximum upper limit is 200mV across ACP/ACN voltage.
- INOM: adapter average current (110% of I_{LIM1})
- IDCHG: battery discharge current
- VBATT: battery voltage on SRP
- ACOK: upon adapter removal (ACOK pin HIGH to LOW)
- $\overline{\text{BATPRES}}$: upon battery removal ($\overline{\text{BATPRES}}$ pin LOW to HIGH)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)
- Adapter insertion while battery only boost is active (triggers ICRIT event if enabled.)

The threshold of ICRIT, IDCHG or VBATT, and the deglitch time of ICRIT, INOM, IDCHG or CMPOUT are programmable through SMBus. Each triggering event can be individually enabled in REG0x3D[6:0]. The ICRIT threshold is 110% of the I_{LIM2} value as set in REG0x3C[14:11]. When I_{LIM2} is set to a low value, and particularly when the ICRIT deglitch is set to one of the faster values of 10 or 100 uS, the ICRIT $\overline{\text{PROCHOT}}$may trip upon adapter insertion due to inrush current. The exact values which may cause this depend on the amount of capacitance on the system rail and the voltage difference between the adapter and battery. Larger capacitance will lead to larger inrush current, as will larger voltage difference between the adapter and battery. This is most likely to be a concern if the I_{LIM2} value is set to 512 mA or less.

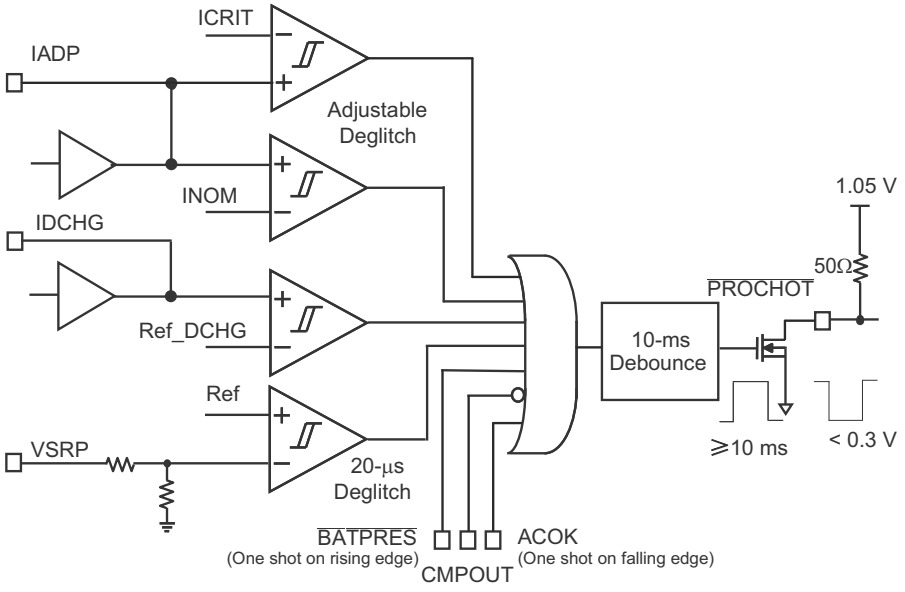


Figure 6-1. $\overline{\text{PROCHOT}}$ Profile

When any event in $\overline{\text{PROCHOT}}$ profile is triggered, $\overline{\text{PROCHOT}}$ is asserted low for minimum 10 ms (default REG0x3C[4:3]=10). At the end of the 10 ms, if the $\overline{\text{PROCHOT}}$ event is still active, the pulse gets extended.

If multiple $\overline{\text{PROCHOT}}$ events occur while the $\overline{\text{PROCHOT}}$ signal remains asserted low, all of the triggering events are saved in status register REG0x3A[6:0]. If the $\overline{\text{PROCHOT}}$ signal deasserts and then is reasserted, the status register will be cleared upon the new high to low transition of the $\overline{\text{PROCHOT}}$ signal so that only the newly detected event is read. Whenever the host reads REG0x3A, this will also clear all of the flagged events from that register after they are read.

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6.3.5 Input Current Dynamic Power Management

The BQ24810 employs dynamic power management to reduce charging current to maintain a maximum adapter current I_{LIM1}, set in REG0x3F(). If the system current requirement exceeds I_{LIM1}, the charger will enter peak power mode (if enabled) as described in Section 6.3.6. If peak power mode is not enabled, the charger will instead enter hybrid boost (if enabled and all required conditions are met) as described in Section 6.4.2. If neither peak power mode nor hybrid boost is entered, the adapter current may exceed I_{LIM1}, potentially generating an INOM or ICRIT $\overline{\text{PROCHOT}}$ or ACOC event.

The BQ24810 features improved precision in both I_{LIM1} and the FDPM_RISE threshold used to enter hybrid boost mode. REG0x3F() allows setting I_{LIM1} in increments of 64 mA.

Typically there are mainly two kinds of adapters which BQ24810 can support, however they do requests configuration in an opposite direction based on their own characteristics. In order to achieve the best performance of both of them, BQ24810 reserve flexibility to adjust charger turbo boost mode entry and charger current ramp up process accordingly. These are summarized in Table 6-2.

The BQ24810 has several user registers that can speed up the hybrid power boost mode and charging entry/exit times. These key registers can have effects on the adapter input current, battery discharge current, and the battery charge current transients. These are summarized in Table 6-3, where tradeoffs can be made between minimizing overshoot of adapter or battery currents, and transition speeds for HPB and ICHG mode.

Table 6-2. Recommended Hybrid Power Boost Mode and Charge Current Ramp Up Setting for Different Input Sources

ADAPTER TYPE	DEDICATED BARREL ADAPTER	THIRD PARTY PD ADAPTER
Characteristic	Robust and capable to handle 500us 1.5ms current overshoot. Key requests: • Quick ICHG recovery after system load removal • Maximize adapter output power • Conservative to enter turbo boost	Sensitive and precise current limit and possible to crash due to overcurrent. Key requests: • Minimize charger input current overshoot • Fast to enter turbo boost mode
Typical IINDPM setting under 10mΩ RAC	3.25A~10A	2A~5A
Typical IINDPM setting under 5mΩ RAC	5A~20A	2A~5A
FDPM_RISE (REG0x36[4:2])	higher threshold setting like 107%/111%	lower threshold setting like 104%
FDPM_FALL(REG0x36[1:0])	Threshold to exit turbo boost mode: Suggest to use 96% (11b)/95%(10b)	lower threshold setting like 93%/90%
FDPM_DEG(REG0x37[5:3])	Longer setting like 380us/750us/1.5ms to maximum power from adapter	Shorter setting like 10us/20us/50us to speed up turbo boost mode entry and minimize input current overshoot
EN_ICHG_PRESET(REG0x36[15])	1b to speed up ICHG ramp up after exit turbo	1b to speed up ICHG ramp up after exit turbo
SEL_MORE_PRESET(REG0x36[13:12])	• 00b for ICHG<10A • 01b for 10A< ICHG	• 00b for ICHG<10A • 01b for 10A< ICHG
EN_CHARGE_FAST_TRANS(REG0x36[10])	1b to speed up charge current ramp up	0b to minimize ovecurrent at input
EN_TURBO_FAST_TRANS(REG0x36[11])	0b to maximize power from adapter	1b to minimize ovecurrent at input
MORE_TURBO_PRESET(REG0x3B[2])	0b to help reduce IIN undershoot and IBAT discharge overshoot during Turbo	1b to help reduce IIN overshoot and may increase IBAT discharge overshoot during Turbo
FAST_CHG_TURBO_TRANS(REG0x37[0])	0b to help reduce IIN undershoot and IBAT discharge overshoot during Turbo	1b to help reduce IIN overshoot and may increase IBAT discharge overshoot during Turbo

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Table 6-3. Key User Registers Impact on Turbo Boost + Charging Performance Summary

REGISTER NAMES	ADAPTER INPUT CURRENT	BATTERY DISCHARGE CURRENT	BATTERY CHARING CURRENT
FDPM_DEG(REG0x37[5:3])	Longer options help maximize output power from barrel adatper and shorter options help minimize input current overshoot for PD adapters	Longer options help reduce battery discharge current and extend battery life. Shorter options help increase battery discharge current to avoid crash input source	NA
EN_ICHG_PRESET(REG0x36[15])	NA	NA	Enable to speed up ICHG recover speed significantly after charger exit turbo boost
SEL_MORE_PRESET(REG0x36[13:12])	More preset value could slightly reduce IIN overshoot time and also increase undershoot value	More preset value could slightly increase battery discharge current overshoot	Working together with EN_ICHG_PRESET, when it is enabled more preset value to help speed up ICHG recover speed after exiting turbo boost
EN_CHARGE_FAST_TRANS(REG0x36[10])	NA	NA	Enable to speed up ICHG recovery speed
EN_TURBO_FAST_TRANS(REG0x36[11])	Enable(1b) to reduce IIN overshoot duration and slightly increase IIN undershoot as side effect	Enable(1b) to increase battery discharge current overshoot	NA
MORE_TURBO_PRESET(REG0x3B[2])	1b to add more preset value for turbo boost ramp which slightly reduce IIN overshoot time and also increase undershoot value	1b to add more preset value for turbo boost ramp can can increase IBAT discharge overshoot	NA
FAST_CHG_TURBO_TRANS(REG0x37[0])	Enable(1b) to reduce IIN overshoot	Enable(1b) to increase battery dicharge current overshoot	NA
TURBO_SPEED(REG0x36[9:8])	Higher codes with stronger compensation to reduce IIN overshoot time and increase IIN undershoot	Higher codes with stronger compensation to increase battery discharge overshoot	NA

6.3.5.1 Setting Input Current Limit

System current normally fluctuates as portions of the system are powered-up or put to sleep. With the input current limit, the current draw from the AC wall adapter is limited to a set level to avoid overloading the adapter.

The total input current, from a wall adapter or other DC source, is the sum of the system current and current required to charge the battery. When the input current exceeds the set input current limit, the BQ24810 device decreases the charge current to provide priority to the system load. As the system current rises, the available charge current drops to 0. If the system load increases further after charging current has been reduced to 0, the charger goes into hybrid power boost mode and adds battery power to support the system load, maintaining the input current limit.

During DPM regulation, the total input current is the sum of the device supply current I_{BIAS}, the charger input current, and the system load current I_{LOAD}, and can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \left[\frac{I_{BATTERY} \cdot V_{BATTERY}}{V_{IN} \cdot \eta} \right] + I_{BIAS} \quad (2)$$

In the above equation, η is the efficiency the switching regulator and $I_{BATTERY}$ is the battery charging or discharging current (positive for charging and negative for discharging). In charging mode, the charger converter is in buck configuration. In hybrid power boost mode, the charger converter is in boost configuration.

To set the input current limit, write a 16-bit InputCurrent() command (REG0x3F) using the data format listed in Table 6-19. When using a 10-mΩ sense resistor, the BQ24810 device provides an input-current limit range of 64 mA to 8.128 A, with 64-mA resolution. Upon POR, default input current limit is 4096 mA on 10-mΩ current sensing resistor (R_{AC}). Additionally, when 0 mA or a value above 8.128A is written, the write is considered invalid and is not written to the register.

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The ACP and ACN pins are used to sense R_{AC} with default value of 10 mΩ. However, resistors of other values can also be used. The actual current is scaled by the ratio of 10 mΩ and R_{AC}. For example, the input current setting code of 4096mA on 10 mΩ becomes 2048mA if sense resistor is 20 mΩ. For a larger sense resistor, larger sense voltage is given, and higher regulation accuracy, but at the expense of higher conduction loss and a more narrow current range. For a smaller sense resistor (5 mΩ, 4 mΩ..etc), smaller sense voltage is given, and lower regulation accuracy, but at the benefits of lower conduction loss and a wider current regulation range can be achieved.

6.3.6 Two-Level Adapter Current Limit (Peak Power Mode)

An adapter can usually supply current higher than its DC rating for a few milliseconds to tens of milliseconds. The BQ24810 employs two-level input current limit, or peak power mode, to fully utilize the adapter overloading capability and minimize battery discharge. Peak power mode is enabled in REG0x38[13]. The DC current limit, or I_{LIM1}, is the same as adapter DC current DPM, set in REG0x3F(). The overloading current, or I_{LIM2}, is set in REG0x3C[14:11], as a percentage of I_{LIM1}.The maximum I_{LIM2} regulation is clamped at around 109mV across ACP-ACN voltage due to IC internal implementation. This is 10.9A under 10 mΩ and if higher ILIM2 is needed then smaller RAC have to be used.

With peak power mode enabled, adapter current greater than I_{LIM1} will not immediately trigger hybrid boost supplement mode. Instead, if the adapter current remains above the I_{LIM1} (scaled by FDPM_RISE percentage) threshold for 50 uS, peak power mode is entered and the adapter DPM limit is raised to I_{LIM2} for a period of T_{OVLD} as set in 0x38H [15:14]. During this period, hybrid boost may still be entered if it is enabled and adapter current exceeds I_{LIM2} (scaled by FDPM_RISE percentage) for a period of FDPM_DEG as set in REG0x37[4:3]. At the end of the T_{OVLD} period, the BQ24810 enters a recovery period where the DPM limit is set to I_{LIM1} for $T_{MAX} – T_{OVLD}$. So the longest adapter current overshoot should be FDPM_DEG+T_{OVLD} above ILIM1. T_{MAX} is set in REG0x38[15:14]. Once the full T_{MAX} (overload and recovery periods) has expired, the peak power mode exits, also forcing an exit from hybrid boost mode if it is active. Upon this exit, the BQ24810 will immediately re-enter a new peak power mode cycle if adapter current remains above the I_{LIM1} (scaled by FDPM_RISE percentage) for the 50 uS qualifying period.

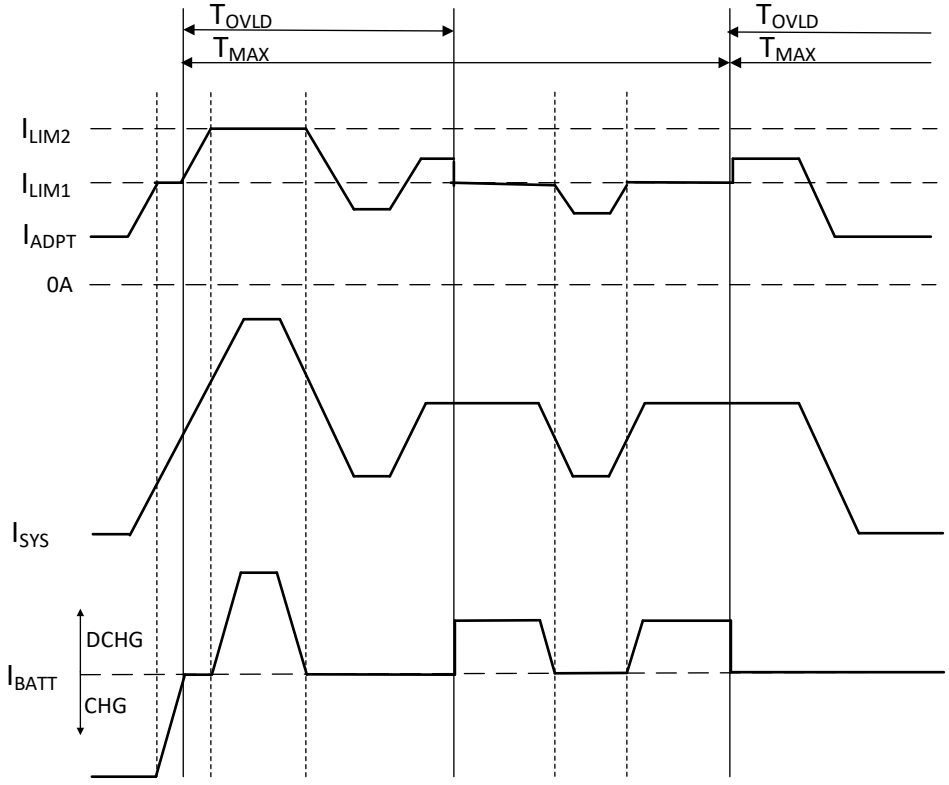


Figure 6-2. Two-Level Adapter Current Limit Timing Diagram, REG0x37[8] = 0

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Charging may optionally be disabled (REG0x37[8]=0) during T_{MAX} in order to reduce adapter current during overload condition. If REG0x37[8] is instead set to 1, and if all other conditions for charging are met, including the charge inhibit bit (REG0x12[0]) being set to 0, then charging will resume during T_{MAX} if the adapter current falls below the active current limit, which is I_{LIM2} during T_{OVLD} and I_{LIM1} during the subsequent relaxation period.

During the peak power mode overload period (T_{OVLD}), the INOM event will not trigger $\overline{\text{PROCHOT}}$, even if the event is enabled and adapter current exceeds the INOM threshold. The ICRIT event remains active during this time. During the recovery period (T_{MAX} - T_{OVLD}), both the INOM and ICRIT events are active if enabled.

The peak power mode timing parameters (T_{OVLD} and T_{MAX}) are not allowed to be changed while peak power mode is enabled. Any write to either 0x38H [15:14] (T_{OVLD}) or 0x38H [9:8] (T_{MAX}) or EN_3L while the peak power mode is enabled (0x38 [13] = 1) will be ignored. In order to change these parameters, the user must first disable peak power mode by writing 0x38 [13] = 0, then update T_{OVLD} and/or T_{MAX}, and then re-enable the peak power mode by writing 0x38 [13] = 1.

6.3.7 EMI Switching Frequency Adjust

The charger switching frequency can be adjusted between 300 kHz, 400 kHz, 600 kHz or 800 kHz to solve EMI issues through SMBus command REG0x12[9:8]. Lower switching frequencies provide greater efficiency and lower EMI. Using a higher switching frequency reduces ripple, allowing smaller inductor and capacitor values.

6.3.8 Device Protections Features

6.3.8.1 Charger Timeout

The BQ24810 device includes a watchdog timer to suspend charging, hybrid power boost mode or battery only boost mode if the charger does not receive a write ChargeVoltage() or write ChargeCurrent() command within 175 s (adjustable through REG0x12[14:13] command).

If a watchdog timeout occurs, all register values remain unchanged, but the converter is suspended. A write to ChargeVoltage(), or ChargeCurrent(), or change of REG0x12[14:13] resets watchdog timer and resumes converter for charging, hybrid power boost mode or battery only boost mode. The watchdog timer can be disabled, or set to 5, 88, or 175 s through SMBus command REG0x12[14:13].

6.3.8.2 Input Overcurrent Protection (ACOC)

If no battery is present, hybrid boost mode has been disabled, or if the hybrid boost discharge current limit (IDCHG) is regulated then the BQ24810 device cannot maintain the input current level once the charge current has been reduced to 0. When the input current exceeds 1.25x or 2x of I_{LIM2} set point for the 6-ms deglitch time, ACFET/RBFET is latched off and an adapter removal is required to force ACDET < 0.6 V to remove the latch. After the latch is removed, ACFET/RBFET can be turned on again.

The ACOC function threshold can be set to 1.25x or 2x of ILIM2 current with ACOC_VTH (REG0x37[9]) or disabled through SMBus command EN_ACOC (REG0x37[10]). There is boundary clamp V_{ACOC_CLAMP} for ACOC thresholds, the upper clamp is 190mV and lower clamp is 50mV across ACP and ACN pin voltage.

6.3.8.3 Charge Overcurrent Protection (CHG_OCP)

The BQ24810 device has cycle-by-cycle peak overcurrent protection. It monitors the voltage across SRP and SRN, and prevents the current from exceeding the threshold based on the charge current set point. The high-side gate drive turns off for the rest of the cycle when over current is detected, and resumes when the next cycle starts.

The charge OCP threshold is automatically set to 6, 9, and 12 A on a 10-mΩ current sensing resistor based on charge current register value. This prevents the threshold from being too high, which is not safe, or too low, which can be triggered in typical operation. Select proper inductance to prevent OCP triggering in typical operation due to high inductor current ripple.

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6.3.8.4 Battery Overvoltage Protection (BATOVP)

In battery charging, the BQ24810 device does not allow the high-side and low-side MOSFET to turn-on when the battery voltage at SRN exceeds 104% of the regulation voltage set point. If BATOVP lasts over 16 ms, the charger is completely disabled until the battery voltage at SRN falls below 102% of the regulation voltage set point. This allows a quick response to an overvoltage condition – such as when the load is removed or the battery is disconnected. A 6-mA current sink from SRP to GND is only on during BATOVP and allows discharging the stored output inductor energy that is transferred to the output capacitors.

In battery boost mode (either battery only boost or hybrid power boost), the BQ24810 device keeps running boost operation when BATOVP is detected, and no 6-mA sink is applied to SRP during these boost modes.

6.3.8.5 Battery Short

When battery voltage on SRN falls below 2.5 V, the converter resets for 1 ms and resumes charge if all the enable conditions in the Enable and Disable Charging section are satisfied. This prevents overshoot current in the inductor, which can saturate the inductor and may damage the MOSFET. The charge current is limited to 0.5 A on 10-mΩ current sensing resistor when BATLOWV condition persists and LSFET keeps off. The LSFET turns on only for a refreshing pulse to charge BTST capacitor.

6.3.8.6 Thermal Shutdown Protection (TSHUT)

The WQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As an added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shutdown, the REGN LDO current limit is reduced to 14 mA. Once the temperature falls below 135°C, charge can be resumed with soft start. During TSHUT, the ACFET/RBFET stays on to power the system rail.

6.3.8.7 Inductor Short, MOSFET Short Protection

The BQ24810 device has a unique short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across RDS(on) of the switching MOSFETs. In case of a MOSFET short or inductor short circuit, the overcurrent condition is sensed by the comparator, the HSFET or LSFET is turned off for the remainder of the switching cycle, and a counter is incremented. The high-side and low-side MOSFETs each have an independent comparator and counter. After either counter reaches seven, the charger is latched off and ACFET and RBFET are turned off to disconnect the adapter from the system. BATFET is turned on to connect the battery pack to the system. The short circuit counters are reset each time that the power stage is enabled, but once either counter reaches seven, the charger is latched off. To reset the charger from latch-off status, the IC VCC pin must be pulled below UVLO or the ACDET pin must be pulled below 0.6 V. The low-side MOSFET Vds monitor circuit is enabled by REG0x37[7], and the threshold is 250 mV measured between the PHASE and GND pins. The high-side MOSFET Vds monitor circuit is enabled by REG0x37[6], and the threshold is 750 mV measured between the ACP and PHASE pins, including both the RAC sense resistor and the HSFET. During hybrid boost and battery only boost functions, the low-side MOSFET short circuit protection threshold is used for cycle-by-cycle current limiting, but the charger does not latch off.

Due to the blanking time of the MOSFET short protection, which blanks out the switching noise from when the MOSFET first turns on, the cycle-by-cycle charge overcurrent protection may detect high current and turn off MOSFET before the MOSFET short protection is triggered. In such a case, the charger's MOSFET short protection may not be activated, so that the counter does not count to seven and then latch off. Instead the charger may continuously keep switching with very narrow duty cycle to limit the cycle-by-cycle current peak value. However, the charger should still be safe and does not cause failure because the duty cycle is limited to a very short time and the MOSFET should still be inside the safety operation area. During a soft start period, it may take a long time instead of just seven switching cycles to detect short circuit due to the same reason of the blanking time.

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6.4 Device Functional Modes

6.4.1 Battery Charging in Buck Mode

The step-down switching controller is designed to charge a series stack of batteries. The battery charging cycle has two phases - constant current (CC) and constant voltage (CV). During the constant current phase, the charger regulates the charging current to the limit in REG0x14(). Once the voltage on SRN reaches the limit in REG0x15, the charger enters CV mode to regulate the battery voltage. The following conditions must be valid to start charge:

- Charge is enabled through SMBus (REG0x12[0], default is 0, charge enabled)
- ILIM pin voltage is higher than $V_{ILIM(RISE)}$ (120 mV nominal)
- All ChargeCurrent(), ChargeVoltage() and InputCurrent() registers have valid value programmed
- ACOK is valid (see Device Power Up for details)
- ACFET and RBFET turn on without latchoff failure (see System Power Selection for details)
- V_{SRN} does not exceed BATOVP threshold
- IC temperature does not exceed TSHUT threshold
- Not in ACOC condition (see Device Protections Features for details)

One of the following conditions stops on-going charging:

- Charge is inhibited through SMBus(REG0x12[0] = 1)
- ILIM pin voltage is lower than $V_{ILIM(FALL)}$ (75 mV nominal)
- ChargeCurrent(), ChargeVoltage() or InputCurrent() is set to 0 or out of range
- ACOK is pulled low (see Device Power Up for details)
- ACFET turns off
- V_{SRN} exceeds BATOVP threshold
- TSHUT IC temperature threshold is reached
- ACOC is detected (see Device Protections Features for details)
- Short circuit is detected (see Inductor Short, MOSFET Short Protection for details)
- Watchdog timer expires if watchdog timer is enabled (see Charger Timeout for details)

6.4.1.1 Setting the Charge Current

To set the charge current, write a 16-bit ChargeCurrent() command (REG0x14) using the data format listed in Table 6-15. With 10-mΩ sense resistor, the BQ24810 device provides a charge current range of 128 mA to 8.128 A, with 64-mA step resolution. Upon POR, charge current is 0 A. Any conditions for ACOK low except ACOV resets the ChargeCurrent() to 0. Sending ChargeCurrent() 0 mA terminates charge. To provide secondary protection, the BQ24810 has an ILIM pin with which the user can program the maximum allowed charge current. Internal charge current limit is the lower one between the voltage set by ChargeCurrent(), and the voltage on ILIM pin. To disable this function, the user can pull ILIM above 2 V, which is the maximum charge current regulation limit. Setting REG0x38[7] to 0 will also disable the ILIM pin charge current limiting so that only the REG0x14 value is used. When ILIM is below 60 mV, battery charging is disabled. The preferred charge current limit can be derived from the below equation:

$$I_{CHG} = \frac{V_{ILIM}}{20 \times R_{SR}} \quad (3)$$

The SRP and SRN pins are used to sense R_{SR} with default value of 10 mΩ. However, resistors of other values can also be used. The actual current is scaled by the ratio of 10 mΩ and R_{SR}. For example, the charge current setting code of 4096mA on 10 mΩ becomes 2048mA if sense resistor is 20 mΩ. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss. If current sensing resistor value is too high, it may trigger an overcurrent protection threshold because the current ripple voltage is too high. In such a case, either a higher inductance value or a lower current sensing resistor value should be used to limit the current ripple voltage level. A current sensing resistor value no more than 20 mΩ is suggested.

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6.4.1.2 Setting the Charge Voltage

To set the output charge regulation voltage, write a 16-bit ChargeVoltage() command (REG0x15) using the data format listed in Table 6-16. The BQ24810 device provides charge voltage range from 1.024 to 19.200 V, with 16-mV step resolution. Upon POR, charge voltage limit is 0 V. Sending ChargeVoltage() 0 mV disables battery charging.

The SRN pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible. Place a decoupling capacitor (0.1 µF recommended) as close to IC as possible to decouple high frequency noise.

6.4.1.3 Automatic Internal Soft-Start Charger Current

Every time the charge is enabled, the charger automatically applies soft-start on charge current to avoid any overshoot or stress on the output capacitors or the power converter. The charge current starts at 128 mA, and the step size is 64 mA in CCM mode for a 10-mΩ current sensing resistor. Each step lasts around 400 µs in CCM mode, till it reaches the programmed charge current limit. No external components are needed for this function.

During DCM mode, the soft start up current step size is larger and each step lasts for longer time period due to the intrinsic slow response of DCM mode.

6.4.2 Hybrid Power Boost Mode

The BQ24810 device supports the hybrid power boost mode to boost battery voltage to adapter level and supplement adapter power when system power demand is temporarily higher than adapter maximum level. Ultra fast 100 µs response time (requires REG0x37[4:3] = 10b) keeps the adapter from crashing. After device powers up, the REG0x37[2] is 0 to disable hybrid power boost mode. To enable hybrid power boost mode, host writes 1 to REG0x37[2]. The $\overline{\text{BST_STAT}}$ pin and REG0x37[1] indicate if the device is in hybrid power boost mode when 0x37[11] = 1.

To support hybrid power boost mode, input current must be set higher than 1024 mA for 10-mΩ input current sensing resistor including 1024mA. There is internal minimum clamp 960mA internal to prevent charger enter turbo boost mode if IINDPM is programmed 960mA or lower. The threshold to enter hybrid power boost mode (FDPM_RISE in REG0x37[5]) is set as percentage to the input current limit. When peak power is not enabled, the input current limit is always I_{LIM1}, set in REG0x3F(). For discussion of hybrid boost behavior when peak power is enabled, refer to Section 6.3.6. When input current is higher than FDPM_RISE of input current limit, the BQ24810 converter changes from buck charging converter to hybrid power boost converter. During hybrid power boost mode the adapter current is regulated at input current limit level so that adapter will not crash. If the watchdog timer is enabled (REG0x12[14:13]) and it expires, it will halt the hybrid boost mode converter. Writing to REG0x12[14:13], REG0x14 or REG0x15 will restart the watchdog timer and allow hybrid boost mode to be reentered.

One of the following conditions stops on-going hybrid power boost mode:

- Adapter current falls below FDPM_FALL (REG0x37[0]) threshold for FDPM_FALL_DEG (REG0x37[14]) of time
- Adapter current falls below 750 mA for 30 uS
- Adapter current falls below input current limit (100% of IINDPM) for greater than 6ms of time.
- Hybrid power boost mode is disabled (REG0x37[2] = 0)
- Adapter is removed
- Battery voltage is below depletion threshold in REG0x3B[15:14]
- ACFET turns off
- TSHUT IC temperature threshold is reached
- Short circuit is detected (see Inductor Short, MOSFET Short Protection for details)
- Watchdog timer expires if watchdog timer is enabled (see Charger Timeout for details)

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6.4.3 Battery Only Boost Mode

When the system is powered from the battery with no adapter attached, a large system load will drop the system voltage significantly due to the battery's impedance. In order to provide the ability to handle large transients over the full operating range of the battery, the BQ24810 provides battery only boost mode. This mode uses the switching converter to boost the battery voltage to a regulated system output, providing additional headroom for system transients.

Unlike the hybrid power boost mode, which is expected to enter and exit frequently as supplemental current is required, battery only boost mode is entered once and maintained until either the adapter is plugged in, the battery reaches the BAT_DEPL_VTH (REG0x3B[15:14]) battery depletion threshold, or the mode is manually exited with the EN_BATT_BOOST (REG0x38[6]) bit. Entry into the mode may either be handled automatically, using the V_{SYSMIN} threshold as set in VSysMin() (REG0x3E) register, or manually using the EN_BATT_BOOST bit. In order to use automatic entry, EN_BATT_BOOST is set to 1 while system voltage is above V_{SYSMIN}. When the system voltage falls below V_{SYSMIN}, the converter will enter battery only boost mode, regulating the system voltage to either 1.5V or 2.3V above V_{SYSMIN} as set by the VBOOST (REG0x38[5]) bit.

All of the following conditions must be met in order to enter battery only boost mode:

- Battery only boost mode is enabled (REG0x38[6] = 1)
- Battery low power mode is disabled (REG0x12[15] = 0)
- System voltage (V_{ACN}) is below V_{SYSMIN}
- ACOK is LOW
- Battery voltage (V_{SRN}) is above depletion threshold in REG0x3B[15:14]

The time required to transition from direct-battery to regulated boost output is dependent on system conditions and generally requires between 1-5 msec. During this time, the battery via the body diode of the battery MOSFET holds up the system rail, resulting in a temporary voltage drop between the battery and system according to the forward voltage of the body diode. The VSysMin() entry should be set to a high enough threshold that the battery can support the transition under the worst case loading condition. A method for calculating this threshold is provided in Equation 4

$$VSysMin() = V_{OP_MIN} + (I_{SYS_MAX} \times R_{BATT}) + V_{BATFET_FD} \quad (4)$$

V_{OP_MIN} is the minimum operational voltage that will support the system. R_{BATT} includes both the internal impedance of the battery as well as any resistance in the power path between the battery and the system. V_{BATFET_FD} is the forward voltage drop of the BATFET body diode.

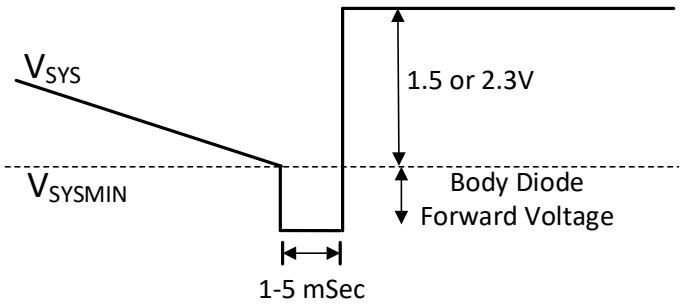


Figure 6-3. Entry Into Battery Only Boost Mode

For systems where finer control is desired, entry into battery-only boost mode may be executed manually. For manual control, an external microcontroller is used to monitor the battery charge using a battery gas gauge IC or other method, and this information is used to determine the optimal point for entry into battery only boost mode. In order to manually enter battery only boost, V_{SYSMIN} must be set below the current system voltage and then the REG0x38[6] enable bit set to 1. V_{SYSMIN} may be adjusted after battery only boost is active in order to adjust the system regulation voltage. There is a delay of approximately 50 mSec (typical) between completion of the SMBUS command to enable battery only boost and entry into the mode.

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One of the following conditions stops on-going battery only boost mode:

- Battery only boost mode is disabled (REG0x38[6] = 0)
- Battery low power mode is enabled (REG0x12[15] = 1)
- Adapter plugs in and ACOK goes HIGH
- Battery voltage (V_{SRN}) is below depletion threshold in REG0x3B[15:14]
- Battery voltage (V_{SRN}) rises to within 200 mV of system regulation voltage (measured at V_{ACN})
- TSHUT IC temperature threshold is reached
- Short circuit is detected (see Inductor Short, MOSFET Short Protection for details)
- Watchdog timer expires if watchdog timer is enabled (see Charger Timeout for details)

In battery-only boost mode, the BQ24810 will regulate system voltage to either (V_{SYSMIN} + 1.5V) or (V_{SYSMIN} + 2.3 V) as set in REG0x38[5]. In order to properly transition during adapter insertion and removal, it is required that the minimum ACOK falling threshold for ACDET (2.30 V scaled by ACDET resistor divider) is above this regulation point. Once the device is in boost mode, status bit REG0x37[1] is set to 1 and $\overline{\text{BST_STAT}}$ pin goes LOW.

If the adapter is inserted while battery only boost mode is active, the system voltage will transition from the battery only boost regulation voltage to the adapter voltage, maintaining battery only boost mode for a deglitch time of AC_PLUG_EXIT_DEG (25ms/3ms/2ms/1ms), set in REG0x36[6:5]. Additionally, the ICRIT $\overline{\text{PROCHOT}}$ signal, if enabled, is automatically asserted, even if the adapter current never exceeds the ICRIT threshold. This may be used to preemptively slow the CPU during the transition.

6.4.3.1 Setting AC_PLUG_EXIT_DEG in Battery Only Boost Mode

To set the AC_PLUG_EXIT_DEG (deglitch time to exit battery only boost after the adapter is plugged in), write a 2-bit command to REG0x36[6:5] using the data format listed in Section 6.6.6. The BQ24810 device provides 4 options of deglitch time, 25ms/3ms(default)/2ms/1ms (00b/01b/10b/11b). When the deglitch time is set to a longer duration, the V_{SYSMIN} is more likely to stay above the programmed voltage, as the ACFET is turned on. The overlap time of enabling ACFET and battery only boost mode may cause the adapter to force the battery pack to a higher voltage. Setting a lower deglitch time will decrease the duration of the battery pack raising in voltage when initially plugged in. If the deglitch is too small, there is a chance the V_{SYSMIN} may dip below the set voltage before the ACFET is fully turned on. A 3ms deglitch is recommended for the TI EVM in *BQ24810 EVM User's Guide*, considering the ACFET and gate drive RC time constant.

6.4.3.2 Setting Minimum System Voltage in Battery Only Boost Mode

To set the V_{SYSMIN} minimum system voltage during battery only boost mode, write a 16-bit VSysMin() command (REG0x3E) using the data format listed in Table 6-18. The BQ24810 device provides minimum system voltage range from 5.632-16.128 V (0x1600 - 0x3F00), with 256-mV step resolution. Upon POR, minimum system voltage limit is 8.96 V (0x2300). The regulation voltage during battery only boost mode is either 1.5V or 2.3V above V_{SYSMIN} as set in REG0x38[5].

The ACN pin is used to sense the system voltage for converter regulation. Place a decoupling capacitor (0.1 µF recommended) as close to IC as possible to decouple high frequency noise.

6.4.4 Battery Discharge Current Regulation in Hybrid Boost Mode and Battery Only Boost Mode

To keep the discharge current below battery OCP rating during hybrid boost mode or battery only boost mode, the BQ24810 device supports discharge current regulation. After device powers up, the REG0x37[15] is 0 to disable discharge current regulation. To enable discharge current regulation, host writes 1 to REG0x37[15]. REG0x37[15]=1 enables battery discharge current regulation during the hybrid power boost mode and battery only boost mode if the conditions to start either boost mode are valid.

Once the battery discharge current is limited, the input current goes up to meet the system current requirement. The user can assert $\overline{\text{PROCHOT}}$ to detect input current increase (ICRIT or INOM), and request CPU throttling to lower the system power.

To set the discharging current limit, write a 16-bit DischargeCurrent() command (REG0x39) using the data format listed in Table 6-17. When using a 10-mΩ sense resistor, the BQ24810 device provides a discharge current limit

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range of 512 mA to 32.256 A, with 512-mA resolution. Upon POR, default discharge current limit is 6.144 A on 10-mΩ current sensing resistor (R_{SR}).

To provide secondary protection during battery discharge, the BQ24810 has an ILIM pin with which the user can program the maximum discharge current. Typically, the user sets the limit below battery pack over current protection (OCP) threshold for maximum battery discharge capacity. Refer to battery specification for OCP information. Internal discharge current limit is the lower one between the voltage set by DischargeCurrent(), and the voltage on ILIM pin. To disable this function, the user can pull ILIM pin above 1.6V, which is the maximum discharge current regulation limit. Setting REG0x38[7] to 0 will also disable the ILIM pin discharge current limiting so that only the REG0x39 value is used. When ILIM is below 60mV, hybrid boost and battery only boost are disabled. The set discharge current limit can be derived from Equation 5.

$$I_{DCHG} = \frac{V_{ILIM}}{5 \times R_{SR}} \quad (5)$$

The SRP and SRN pins are used to sense R_{SR} with default value of 10 mΩ. However, resistors of other values can also be used. The actual current is scaled by the ratio of 10 mΩ and R_{SR}. For example, the discharge current setting code of 4096mA on 10 mΩ becomes 2048mA if sense resistor is 20 mΩ. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss. If current sensing resistor value is too high, it may trigger an overcurrent protection threshold because the current ripple voltage is too high. In such a case, either a higher inductance value or a lower current sensing resistor value should be used to limit the current ripple voltage level. A current sensing resistor value no more than 20 mΩ is suggested.

When operating in battery only boost mode, the battery is the only power source in the system. Limiting the battery discharge current will cause system voltage to drop if the system load is greater than the amount that may be supplied by the battery with the discharge limit set. When boosting the battery to a higher voltage, the battery discharge current will be larger than the system current according to the ratio of system to battery voltage. It is common for the battery current to be double that of the system current. The discharge limit should be set to the largest current that the battery and switching components can support without damage and should be used only as a protection against high-current damage as might occur from a short circuit. Limiting current in battery boost mode will cause the system voltage to fall below the regulation set point.

6.4.5 Battery LEARN Cycle

A battery LEARN cycle can be activated through the REG0x12[5]. When LEARN is enabled, the system draws power from the battery instead of the adapter by turning off ACFET/RBFET and turning on BATFET. The LEARN function allows the battery to discharge in order to calibrate the battery gas gauge over a complete discharge and charge cycle. The controller automatically exits the LEARN cycle when the battery voltage is below the battery depletion threshold as set in REG0x3B[15:14]. The system switches back to adapter input by turning off BATFET and turning on ACFET/RBFET. After the LEARN cycle, REG0x12[5] is automatically reset to 0.

When adapter is removed during LEARN mode, the charger exits LEARN mode by setting REG0x12[5] to 0. The battery FET keeps powering the system without any glitches. Later when adapter plugs in again, host has to set REG0x12[5] to 1 to enable LEARN mode again.

When the battery is removed during LEARN mode, $\overline{\text{BATPRES}}$ rises from low to high and the device exits LEARN mode. ACFET/RBFET quickly turns on in 100 µs to prevent the system from crashing. The turn-on triggered by $\overline{\text{BATPRES}}$ is faster than that triggered by battery depletion comparator.

6.4.6 Converter Operational Modes

6.4.6.1 Continuous Conduction Mode (CCM)

With sufficient charge current, the inductor current does not cross 0, which is defined as CCM. The controller compares SRP-SRN (CC charging) or SRN (CV charging) to a reference value as set in ChargeCurrent() REG0x14 and ChargeVoltage() REG0x15. This error is integrated in the error amplifier and the error amplifier

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output (EAO) is compared to a ramp voltage. As long as EAO voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds EAO voltage, HSFET turns off and low-side MOSFET (LSFET) turns on. At the end of the cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM, the inductor current always flows and creates a fixed two-pole system. Having the LSFET turn-on keeps the power dissipation low and allows safe charging at high currents.

6.4.6.2 Discontinuous Conduction Mode (DCM)

During the HSFET off time when LSFET is on, the inductor current decreases. If the current goes to 0, the converter enters DCM. Each cycle, if the voltage across SRP-SRN falls below 5 mV (0.5 A on 10 mΩ R_{SR} flowing into the battery for charging or out of the battery for hybrid boost), the undercurrent comparator (UCP) turns off LSFET (if charging) or HSFET (if hybrid boosting) to block negative inductor current.

During DCM the loop response automatically changes. It changes to a single-pole system and the pole is proportional to the load current.

6.4.6.3 Non-Sync Mode and Light Load Comparator

When charging, if the average charge current falls below 125 mA (on 10-mΩ sense resistor) the light load comparator keeps LSFET off to block reverse current in the inductor. When average current rises above 250 mA, the LSFET turns on again. Similarly, in boost mode, when the discharge current is below 250 mA (on 10-mΩ sense resistor), the light load comparator keeps HSFET off. When average current rises above 500 mA, the HSFET turns on again.

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6.5 Programming

6.5.1 SMBus Interface

The BQ24810 device operates as a slave, receiving control inputs from the embedded controller host through the SMBus interface. This devices uses a simplified subset of the commands documented in *System Management Bus Specification V1.1*, which can be downloaded from www.smbus.org. The BQ248110 may use the SMBus read-word and write-word protocols (shown in Table 6-4 and Table 6-5) to receive commands from a smart battery. The BQ24810 device performs only as a SMBus slave device with address 0x12. Note that this SMBUS address is written in 8-bit format, which is the 7-bit SMBus address with a "0" bit appended to represent the R/W bit. The corresponding 7-bit address is 0x09. The BQ24810 does not initiate communication on the bus. The BQ24810 has two identification registers, a 16-bit device ID register (0xFF) and a 16-bit manufacturer ID register (0xFE). The BQ24810 has manufacturer ID of 0x40 and device ID of 0x08.

SMBus communication starts when VCC is above UVLO.

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors (10 kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the master signals a start condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a stop condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figure 6-4 and Figure 6-5 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the start and stop conditions. The SDA state changes only while SCL is low, except for the start and stop conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the device because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The BQ24810 supports the charger commands listed in Table 6-4.

6.5.1.1 SMBus Write-Word and Read-Word Protocols

Table 6-4. Write-Word Format

S (1) (3)	SLAVE ADDRESS(1)	W (1) (6)	ACK (2) (5)	COMMAND BYTE(1)	ACK (2) (5)	LOW DATA BYTE(1)	ACK (2) (5)	HIGH DATA BYTE(1)	ACK (2) (5)	P (1) (4)
	7 bits	1b	1b	8 bits	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

(1) Master to slave
(2) Slave to master (shaded gray)
(3) S = Start condition or repeated start condition
(4) P = Stop condition
(5) ACK = Acknowledge (logic-low)
(6) W = Write bit (logic-low)

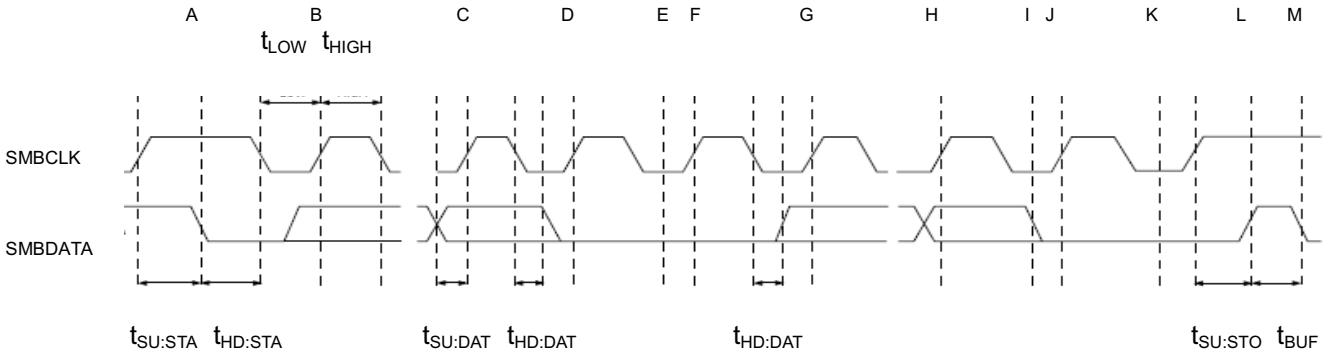
Table 6-5. Read-Word Format

S(1) (3)	SLAVE ADDRESS(1)	W (1) (7)	ACK (2) (5)	COMMAND BYTE(1)	ACK (2) (5)	S(1) (3)	SLAVE ADDRESS(1)	R(1) (8)	ACK (2) (5)	LOW DATA BYTE(2)	ACK (1) (5)	HIGH DATA BYTE(2)	NACK (1) (6)	P (1) (4)
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

(1) Master to slave
(2) Slave to master (shaded gray)
(3) S = Start condition or repeated start condition
(4) P = Stop condition
(5) ACK = Acknowledge (logic-low)
(6) NACK = Not acknowledge (logic-high)
(7) W = Write bit (logic-low)
(8) R = Read bit (logic-high)

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6.5.1.2 Timing Diagrams



A = Start condition

B = MSB of address clocked into slave

C = LSB of address clocked into slave

D = R/W bit clocked into slave

E = Slave pulls SMBDATA line low

F = ACKNOWLEDGE bit clocked into master

G = MSB of data clocked into slave

H = LSB of data clocked into slave

I = Slave pulls SMBDATA line low

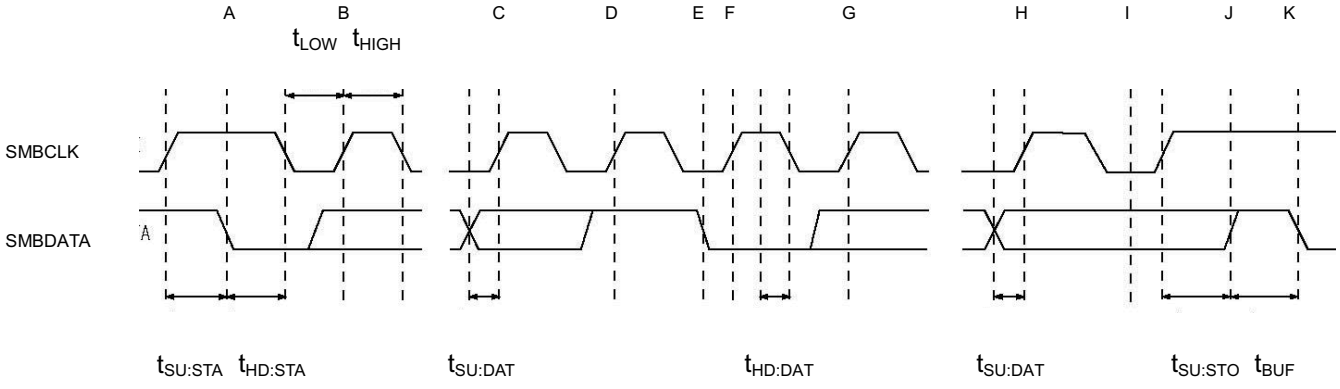
J = Acknowledge clocked into master

K = Acknowledge clock pulse

L = Stop condition, data executed by slave

M = New start condition

Figure 6-4. SMBus Write Timing



A = START CONDITION

E = SLAVE PULLS SMBDATA LINE LOW

I = ACKNOWLEDGE CLOCK PULSE

A = Start condition

B = MSB of address clocked into slave

C = LSB of address clocked into slave

D = R/W bit clocked into slave

E = Slave pulls SMBDATA line low

F = ACKNOWLEDGE bit clocked into master

G = MSB of data clocked into master

H = LSB of data clocked into master

I = Acknowledge clock pulse

J = Stop condition

K = New start condition

Figure 6-5. SMBus Read Timing

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6.6 Register Maps

6.6.1 Battery-Charger Commands

The BQ24810 supports fourteen battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 6-6. ManufacturerID() and DeviceID() can be used to identify the BQ24810. The ManufacturerID() command always returns 0x0040 and the DeviceID() command always returns 0x0008.

Table 6-6. Battery Charger Command Summary

REGISTER ADDRESS	REGISTER NAME	READ OR WRITE	DESCRIPTION	POR STATE
0x12	ChargeOption0() Table 6-7	Read or Write	Charge Options Control 0	0xE108
0x3B	ChargeOption1() Table 6-8	Read or Write	Charge Options Control 1	0xC220
0x38	ChargeOption2()Table 6-9	Read or Write	Charge Options Control 2	0x0384
0x37	ChargeOption3()Table 6-10	Read or Write	Charge Options Control 3	0x1A58
0x36	ChargeOption4()Table 6-11	Read or Write	Charge Options Control 4	0x0091
0x3C	ProchotOption0()Table 6-12	Read or Write	$\overline{\text{PROCHOT}}$ Options Control 0	0x4A54
0x3D	ProchotOption1() Table 6-13	Read or Write	$\overline{\text{PROCHOT}}$ Options Control 1	0x8120
0x3A	ProchotStatus() Table 6-14	Read Only	$\overline{\text{PROCHOT}}$ status	0x0000
0x14	ChargeCurrent() Table 6-15	Read or Write	7-bit Charge Current Setting	0x0000
0x15	ChargeVoltage() Table 6-16	Read or Write	11-bit Charge Voltage Setting	0x0000
0x39	DischargeCurrent() Table 6-17	Read or Write	6-bit Discharge Current Setting	0x1800, or 6144mA
0x3E	VsysMin() Table 6-18	Read or Write	7-bit Minimum System Voltage Setting	0x2300, or 8960 mV
0x3F	InputCurrent() Table 6-19	Read or Write	7-bit Input Current Setting	0x1000, or 4096mA
0xFE	ManufacturerID()	Read Only	Manufacturer ID	0x0040
0xFF	DeviceID()	Read Only	Device ID (BQ24810)	0x0008

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6.6.2 Setting Charger Options

6.6.2.1 ChargeOption0 Register

Figure 6-6. ChargeOption0 Register (0x12)

15	14	13	12	11	10	9	8
EN_LWPWR	WDTMR_ADJ		Reserved			PWM_FREQ	
R/W	R/W		R			R/W	
7	6	5	4	3	2	1	0
Reserved		EN_LEARN	IADP_GAIN	IDCHG_GAIN	Reserved		CHRG_INHIBIT
R		R/W	R/W	R/W	R		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-7. ChargeOption0 Register (0x12)

BIT	BIT NAME	DESCRIPTION
[15]	Low Power Mode Enable (EN_LWPWR)	0: IC in performance mode with battery only. The $\overline{\text{PROCHOT}}$, current/power monitor buffer, battery only boost mode, and independent comparator follow register setting. 1: IC in low power mode with battery only. IC is in the lowest quiescent current when this bit is 1. $\overline{\text{PROCHOT}}$, discharge current monitor buffer, power monitor buffer, battery only boostmode and independent comparator are disabled. (default at POR)
[14:13]	WATCHDOG Timer Adjust (WDTMR_ADJ)	Set maximum delay between consecutive SMBus write charge voltage or charge current command. If IC does not receive write on REG0x14() or REG0x15() within the watchdog time period, the charger converter stops to disable charge and boost mode operations. After expiration, the timer will resume upon the write of REG0x14() or REG0x15(). The charge or boost operations will resume if all the other conditions are valid. 00: Disable watchdog timer 01: Enabled, 5 sec 10: Enabled, 88 sec 11: Enable watchdog timer (175 s) (default at POR)
[12:10]	Reserved	0 - Reserved
[9:8]	Switching Frequency (PWM_FREQ)	Converter switching frequency. 00: 600 kHz 01: 800 kHz (default at POR) 10: 300 kHz 11: 400 kHz
[7:6]	Reserved	0 - Reserved
[5]	LEARN Mode Enable (EN_LEARN)	Battery LEARN mode enable. In LEARN mode, ACFET and RBFET turn off and BATFET turns on. When $\overline{\text{BATPRES}}$ is HIGH, IC exits LEARN mode and this bit is set back to 0. When the battery is depleted, the charger cannot enable LEARN mode 0: Disable LEARN mode (default at POR) 1: Enable LEARN mode
[4]	IADP Amplifier Gain for Primary Input (IADP_GAIN)	Ratio of IADP pin voltage over the voltage across ACP and ACN. 0: 20X (default at POR) 1: 40X
[3]	IDCHG Amplifier Gain (IDCHG_GAIN)	Ratio of IDCHG pin voltage over the voltage across SRN and SRP. 0: 8x with discharge current range 0-32A for 10 mΩ RSR. 1: 16x with discharge current range 0-16A for 10 mΩ RSR (default at POR)
[2:1]	Reserved	0 - Reserved
[0]	Charge Inhibit (CHRG_INHIBIT)	Charge inhibit. When this bit is 0, battery charging is enabled with valid value in REG0x14() and REG0x15() 0: Enable charge (default at POR) 1: Inhibit charge

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6.6.3 ChargeOption1 Register

Figure 6-7. ChargeOption1 Register (0x3B)

15	14	13	12	11	10	9	8
BAT_DEPL_VTH		RSNS_RATIO		EN_IDCHG	EN_PMON	PMON_RATIO	Reserved
R/W		R/W		R/W	R/W	R/W	R
7	6	5	4	3	2	1	0
CMP_REF	CMP_POL	CMP_DEG		EN_FET_LATCHOFF	MORE_TURBO_PRESET	EN_SHIP_DCHG	EN_DYNAMIC_CHARGE_OCP
R/W	R/W	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-8. ChargeOption1 Register (0x3B)

BIT	BIT NAME	DESCRIPTION
[15:14]	Battery Depletion Threshold (BAT_DEPL_VTH)	Battery over-discharge threshold. During LEARN cycle, when battery voltage is below the depletion threshold, the IC exits LEARN mode. During boost mode, when battery voltage is below the depletion threshold, the IC exits boost mode. 00: Falling threshold = 60% of ChargeVoltage() register setting 01: Falling threshold = 64% of ChargeVoltage() register setting 10: Falling threshold = 68% of ChargeVoltage() register setting 11: Falling threshold = 72% of ChargeVoltage() register setting (default at POR)
[13:12]	R_{AC} and R_{SR} Ratio (RSNS_RATIO)	Adjust the PMON calculation for different input sense resistor R_{AC} and charge sense resistor R_{SR} ratio. Reference Table 6-1 for further detail.. 00: R_{AC} and R_{SR} 1:1 (default at POR) 01: R_{AC} and R_{SR} 2:1 10: R_{AC} and R_{SR} 1:2 11: Reserved
[11]	IDCHG Buffer Enable (EN_IDCHG)	IDCHG pin output enable. 0: Disable IDCHG output to minimize Iq (default at POR) 1: Enable IDCHG output
[10]	PMON Buffer Enable (EN_PMON)	PMON pin output enable. 0: Disable PMON output to minimize Iq (default at POR) 1: Enable PMON output
[9]	PMON Gain (PMON_RATIO)	Ratio of PMON output current vs total input and battery power. Reference Table 6-1 for further detail. 0: 0.25 µA/W for 10 mΩ sense resistors 1: 1 µA/W for 10 mΩ sense resistors (default at POR)
[8]	Reserved	0 - Reserved
[7]	Independent Comparator Reference (CMP_REF)	Independent comparator internal reference. 0: 2.3 V (default at POR) 1: 1.2 V
[6]	Independent Comparator Polarity (CMP_POL)	Independent comparator output polarity. With comparator polarity bit set as 1, the hysteresis is set by placing a resistor from CMPIN to CMPOUT. With comparator polarity bit set as 0, the hysteresis is internally set as 100mV. 0: When CMPIN is above internal threshold, CMPOUT is LOW (default at POR) 1: When CMPIN is above internal threshold, CMPOUT is HIGH
[5:4]	Independent Comparator Deglitch Time (CMP_DEG)	Independent comparator deglitch time, applied on the edge where CMPOUT goes LOW. No deglitch time is applied on the rising edge of CMPOUT. If the value in REG0x3B[7:3] is changed by host, deglitch time will get reset. 00: Independent comparator is disabled 01: Independent comparator is enabled with output deglitch time 1 µs Note: 1 µs deglitch should not be used when low-power mode bit is enabled. 10: Independent comparator is enabled with output deglitch time 2 ms (default at POR) 11: Independent comparator is enabled with output deglitch time 5 sec
[3]	Power Path Latch-off Enable (EN_FET_LATCHOFF)	When independent comparator is triggered, both ACFET/RBFET turn off. The latch off is cleared by either POR or write this bit to zero. This function is available with CMP_DEG setting of 2 ms (10) or 5 sec (11). 0: When independent comparator is triggered, no power path latch off (default at POR) 1: When independent comparator is triggered, power path latches off.
[2]	MORE_TURBO_PRESET	Add more preset for turbo boost mode entry which could help reduce IIN overshoot but at same time slightly increase IIN undershoot and IBAT discharge overshoot as trade off: 0: Disable 1: Enable (default at POR)
[1]	Discharge SRN for Shipping Mode (EN_SHIP_DCHG)	Discharge SRN pin for 200 ms with minimum 5-mA current. 0: Disable discharge mode (default at POR) 1: Enable discharge mode

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Table 6-8. ChargeOption1 Register (0x3B) (continued)

BIT	BIT NAME	DESCRIPTION
[0]	EN_DYNAMIC_CHARGE_OCP	Enable short time(80ys) CHG_OCP threshold lift when ramp up charge current after exiting turbo, this is used to avoid ICHG chatter at beginning part of ICHG recover: 0: Disable (default at POR) 1: Enable

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6.6.4 ChargeOption2 Register

Figure 6-8. ChargeOption2 Register (0x38)

15	14	13	12	11	10	9	8
PKPWR_TOVLD		EN_PKPWR		Reserved		PKPWR_TMAX	
R/W		R/W		R		R/W	
7	6	5	4	3	2	1	0
EN_EXTILIM	EN_BATT_BOOST	VBOOST	Reserved				
R/W	R/W	R/W	R				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-9. ChargeOption2 Register (0x38)

BIT	BIT NAME	DESCRIPTION
[15:14]	Peak Power Mode Over-load Time (PKPWR_TOVLD)	Input source maximum over-load time T_{OVLD} in peak power mode. 00: 1 ms (default @ POR) 01: 2 ms 10: 5 ms 11: 10 ms
[13]	Peak Power Mode Enable (EN_PKPWR)	Peak power mode enable. 0: Disable peak power mode (default @ POR) 1: Enable peak power mode
[12:10]	Reserved	0 - Reserved
[9:8]	Peak Power Mode Cycle Time (PKPWR_TMAX)	Peak power mode cycle time T_{MAX}. Relax time is T_{MAX} - T_{OVLD}. 00: 20 ms (default @ POR) 01: 40 ms 10: 80 ms 11: 1 sec
[7]	External Current Limit Enable (EN_EXTILIM)	External ILIM pin enable to set the charge and discharge current. 0: Charge/discharge current limit is set by REG0x14() and 0x39(). 1: Charge/discharge current limit is set by the lower value of ILIM pin and registers. (default at POR)
[6]	Battery Only Boost Mode Enable (EN_BATT_BOOST)	Battery only boost mode enable. When charger exits battery boost due to higher battery voltage or fault, this enable bit does not automatically go to zero. 0: Disable battery only boost mode (default at POR) 1: Enable battery only boost mode.
[5]	System Regulation Voltage in Battery Only Boost Mode (VBOOST)	System regulation voltage in battery only boost mode. 0: 1.5V + VsysMin() (default at POR) 1: 2.3V + VSysMin()
[4:0]	Reserved	0 - Reserved

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6.6.5 ChargeOption3 Register

Figure 6-9. ChargeOption3 Register (0x37)

15	14	13	12	11	10	9	8
EN_IDCHG_REG	FDPM_FALL_DEG	ACDRV_OFF	ACOK_DEG	ACOK_STAT	EN_ACOC	ACOC_VTH	PKPWR_ENCHRG
R/W	R/W	R/W	R/W	R	R/W	R/W	R
7	6	5	4	3	2	1	0
IFAULT_HI	IFAULT_LO	FDPM_DEG			EN_HYBRID_BOOST	BOOST_STAT	FAST_CHG_TURBO_TRANS
R/W	R/W	R/W			R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-10. ChargeOption3 Register (0x37)

BIT	BIT NAME	DESCRIPTION
[15]	Discharge Current Regulation Enable (EN_IDCHG_REG)	Battery discharge current regulation enable. 0: Disable discharge current regulation (default at POR) 1: Enable discharge current regulation
[14]	FDPM_FALL_DEG	Turbo boost mode exit deglitch time when IIN falls below FDPM_FALL threshold but still >0.75A(IINDPM>2A) or >0.38A(IINDPM<2A). 0: 320us. (default at POR) 1: 640us.
[13]	ACDRV Disable (ACDRV_OFF)	Force ACFET/RBFET to turn off, even with good adapter present. 0: ACFET/RBFET control based on "System Power Selection". (default at POR) 1: Turn off ACFET/RBFET.
[12]	ACOK Deglitch Time for Primary Input (ACOK_DEG)	Adjust ACOK rising edge deglitch time. After POR, the first time adapter plugs in, deglitch time is always 150 ms if this register has not been written by the host. Starting from the 2nd time adapter plugs in, the deglitch time follows the bit setting. 0: ACOK rising edge deglitch time 150ms 1: ACOK rising edge deglitch time 1.3 sec (default at POR)
[11]	Adapter Present Indicator (ACOK_STAT)	Input present indication bit. This bit is set to 1 when ACOK pin goes HIGH. Refer to for conditions to transition ACOK. 0: AC adapter is not present 1: AC adapter is present
[10]	ACOC Enable (EN_ACOC)	ACOC protection threshold by monitoring ACP_ACN voltage. 0: Disable ACOC (default at POR) 1: Enable ACOC
[9]	ACOC Limit (ACOC_VTH)	ACOC protection threshold by monitoring ACP_ACN voltage. 0: 125% of ILIM2 1: 200% of ILIM2 (default at POR)
[8]	PKPWR_ENCHRG	Allow battery charging during peak power T_{MAX} cycle. 0: Battery charging is NOT allowed during T_{MAX}. The adapter only supports system load. This reduces the chance of overloading the adapter. (default at POR) 1: Battery charging is allowed during T_{MAX}. The adapter current capability of ILIM1 and ILIM2 is fully utilized.
[7]	HSFET VDS Threshold (IFAULT_HI)	MOSFET/inductor short protection by monitoring ACN to PHASE voltage 0: Disable (default at POR) 1: 750 mV
[6]	LSFET VDS Threshold (IFAULT_LO)	MOSFET/inductor short protection by monitoring PHASE to GND voltage (LSFET drain-source voltage.) Also provides cycle-by-cycle current limit protection during hybrid boost and battery only boost functions. 0: Disable 1: 250 mV (default at POR)
[5:3]	Fast DPM Deglitch Time (FDPM_DEG)	Response time from system current exceeding Fast DPM Threshold to battery discharge in boost mode. 000: Response time 10 µs 001: Response time 20 µs 010: Response time 50 µs 011: Response time 100 µs (default at POR) 100: Response time 185 µs 101: Response time 380 µs 110: Response time 750 µs 111: Response time 1.5 ms
[2]	Hybrid Power Boost Mode Enable(EN_HYBRID_BOOST)	Hybrid power boost mode enable bit. When $\overline{\text{BATPRES}}$ goes from LOW to HIGH (battery removal), this bit will be reset to zero to disable boost mode. When the charger exits hybrid power boost due to smaller load or fault, this enable bit doesn't automatically go to zero. 0: Disable hybrid power boost mode (default at POR) 1: Enable hybrid power boost mode

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Table 6-10. ChargeOption3 Register (0x37) (continued)

BIT	BIT NAME	DESCRIPTION
[1]	Boost Mode Indication (BOOST_STAT)	Active-high boost mode indicator. This bit is read only. 0: Charger is not in hybrid power boost mode or battery only boost mode (default at POR) 1: Charger is in hybrid power boost mode or battery only boost mode (Note that the $\overline{\text{BST_STAT}}$ pin is active-low and is low when the BOOST_STAT register bit is set to 1.)
[0]	FAST_CHG_TURBO_TRANS	Minimize the converter shut off time when transfer from charign direction to reverse turbo boost operation 0: Disable (default at POR) 1: Enable

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6.6.6 ChargeOption4 Register

Figure 6-10. ChargeOption4 Register (0x36)

15	14	13	12	11	10	9	8
EN_ICHG_PRESET	3L_TIME	SEL_MORE_PRESET		EN_TURBO_FAST_TRANS	EN_CHARGE_FAST_TRANS	TURBO_SPEED	
R/W	R/W	R/W		R/W	R/W	R/W	
7	6	5	4	3	2	1	0
GDRV_STR_EN	AC_PLUG_EXIT_DEG		FDPDM_RISE			FPDM_FALL	
R/W	R/W		R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-11. ChargeOption4 Register (0x36)

BIT	BIT NAME	DESCRIPTION
[15]	EN_ICHG_PRESET	Disable SEL_MORE_PRESET bits functions and its additional FDPM deglitch for minimizing IINDPM overshoot. 0: Disable 1: Enable (default at POR)
[14]	3L_TIME	Three level adapter current limit feature time duration adjustment for 3L unlimited input current. Not recommend to change this on the fly when peak power mode is active. 0: 1ms (default at POR) 1: 3ms
[13:12]	SEL_MORE_PRESET	ICHG current regulation internal amplifier preset output value adjustment. 00: 0mV (default at POR)(Additional 160us deglitch time for FDPM enter add on FDPM_DEG) 01: 15mV(Additional 160us deglitch time for FDPM enter add on FDPM_DEG) 10: 30mV(Additional 640us deglitch time for FDPM enter add on FDPM_DEG) 11: 40mV(Additional 640us deglitch time for FDPM enter add on FDPM_DEG)
[11]	EN_TURBO_FAST_TRANS	Enable the ultra fast temporary turbo boost mode entry feature. This also activates the minimum turbo boost blank time (BOOST_EXIT_BLK) which prevents exiting turbo boost within 320us after FDPM_DEG. Setting to 0b decreases the minimum turbo boost time to either 30us (if adapter current stays below 750mA) or FDPM_FALL_DEG (if adapter current stays below FDPM_FALL but above 750mA). 0: Disable 1: Enable (default at POR)
[10]	EN_CHARGE_FAST_TRANS	Enable the ultra fast temporary ICHG fast recovery feature. 0: Disable 1: Enable (default at POR)
[9:8]	TURBO_SPEED	Turbo Boost mode startup RHP zero compensation adjustment. 00: Original speed no change (default at POR) 01: 15% speed increase 10: Reserved (similar to code 01b) 11: Reserved (similar to code 01b)
[7]	GDRV_STR_EN	Enable BUCK charger HS and LS gate drive strength. When enabled, it is recommended to include an RC low pass filter on ACP/ACN to improve IINDPM/PMON/IADP accuracy. 0: Disable 1: Enable (default at POR)
[6:5]	AC_PLUG_EXIT_DEG	Deglitch time from AC pluged in to charger exit battery only boost mode. 00: 25 ms 01: 3 ms(default at POR) 10: 2 ms 11: 1 ms
[4:2]	Hybrid Power Boost Mode Entry Threshold (FDPM_RISE)	Fast DPM comparator threshold to enter hybrid power boost mode. The threshold is set as percentage to the input current limit. When peak power is not enabled, the input current limit is ILIM1, set in REG0x3F(). When the device is in T_{OVLD} of peak power mode cycle, input current limit is ILIM2, and the threshold is 107% of ILIM2. For the rest of peak power mode cycle, input current limit is ILIM1. 000: Reserved 001: 104% 010: 105% 011: 106% 100: 107% (default at POR) 101: 111% 110: Reserved 111: Reserved

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Table 6-11. ChargeOption4 Register (0x36) (continued)

BIT	BIT NAME	DESCRIPTION
[1:0]	Hybrid Power Boost Mode Exit Threshold (FDPM_FALL)	Fast DPM comparator threshold to exit hybrid power boost mode. 00: 90% 01: 93% (default at POR) 10: 95% 11: 96%

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6.6.7 ProchotOption0 Register

Figure 6-11. ProchotOption0 Register (0x3C)

15	14	13	12	11	10	9	8
EN_3L	ILIM2_VTH[3:0]				ICRIT_DEG		Reserved
R/W	R/W				R/W		R
7	6	5	4	3	2	1	0
VBATT_VTH[1:0]		EN_PROCHOT_EXT	PROCHOT_WIDTH[1:0]		PROCHOT_CLEAR	INOM_DEG	INOM_VTH
R/W		R/W	R/W		R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-12. ProchotOption0 Register (0x3C)

BIT	BIT NAME	DESCRIPTION
[15]	EN_3L	Enable three level input current regulation 0: Disable three-level adapter current limit. (default at POR) 1: Enable three-level adapter current limit.
[14:11]	Peak Adapter Current Limit (ILIM2_VTH)	ILIM2 threshold as percentage of DPM in REG0x3F(). At 250% setting, when IDPM is over 3.648A, clamp ILIM2 to 230% of IDPM. The current is measured on the R_{AC} between ACP and ACN. ICRIT is set as 110% of I_{LIM2}. 0001 - 1001: 110% - 150%, step 5% 1001: 150%, 1010: 160%, 1011: 170%, 1100: 180%, 1101: 200%, 1110: 220%; 1111: 250% Default 150% (1001)
[10:9]	ICRIT Deglitch Time (ICRIT_DEG)	Typical ICRIT deglitch time. 00: 10 µs 01: 100 µs (default at POR) 10: 400 µs 11: 800 µs
[8]	Reserved	0 - Reserved
[7:6]	Battery Voltage Threshold (VBATT_VTH)	Battery voltage threshold to trigger $\overline{\text{PROCHOT}}$. Measure on SRN with fixed 20-µs deglitch time. Trigger when SRN voltage is below the threshold. If REG0x15() is programmed below VBATT threshold, it is recommended to not enable VBATT in $\overline{\text{PROCHOT}}$ profile. 00: 5.75 V 01: 6.00 V (default at POR) 10: 6.25 V 11: 6.50 V
[5]	$\overline{\text{PROCHOT}}$ Pulse Extension Enable (EN_PROCHOT_EXT)	When pulse extension is enabled, keep $\overline{\text{PROCHOT}}$ pin voltage low until host write 0x3C[2] = 0. 0: Disable pulse extension (default at POR) 1: Enable pulse extension
[4:3]	$\overline{\text{PROCHOT}}$ Pulse Width (PROCHOT_WIDTH[1:0])	Minimum $\overline{\text{PROCHOT}}$ pulse width when REG0x3C[5]=0 00: 100 µs 01: 1 ms 10: 10 ms (default at POR) 11: 5 ms
[2]	$\overline{\text{PROCHOT}}$ Pulse Clear (PROCHOT_CLEAR)	Clear $\overline{\text{PROCHOT}}$ pulse when (0x3C[5] = 1). 0: Clear $\overline{\text{PROCHOT}}$ pulse and drive $\overline{\text{PROCHOT}}$ pin HIGH 1: Idle (default at POR)
[1]	INOM Deglitch Time (INOM_DEG)	Maximum INOM deglitch time. INOM threshold is 110% of DPM in REG0x3F(). Measure current between ACP and ACN. Trigger when the current is above this threshold. 0: 1 ms (max) (default at POR) 1: 15 ms (max)
[0]	INOM Threshold (INOM_VTH)	INOM current threshold as percentage of DPM in REG0x3F(). 0: 110% (default at POR) 1: 106%

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6.6.8 ProchotOption1 Register

Figure 6-12. ProchotOption1 Register (0x3D)

15	14	13	12	11	10	9	8
IDCHG_VTH						IDCHG_DEG	
R/W						R/W	
7	6	5	4	3	2	1	0
Reserved	PROCHOT_PROFILE						
R	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-13. ProchotOption1 Register (0x3D)

BIT	BIT NAME	DESCRIPTION
[15:10]	IDCHG Threshold (IDCHG_VTH)	6 bit, range, range 0 A to 32256 mA, step 512 mA. Measure current between SRN and SRP. Trigger when the discharge current is above the threshold. Default: 16384 mA (100000)
[9:8]	IDCHG Deglitch Time (IDCHG_DEG)	Typical IDCHG deglitch time. 00: 1.6 ms 01: 100 µs (default at POR) 10: 6 ms 11: 12 ms
[7]	Reserved	0 - Reserved
[6:0]	$\overline{\text{PROCHOT}}$ Profile Enable (PROCHOT_PROFILE)	When adapter is present, the $\overline{\text{PROCHOT}}$ function is enabled by the below bits. When adapter is removed, ICRIT, INOM, $\overline{\text{BATPRES}}$, and ACOK functions are automatically disabled in the $\overline{\text{PROCHOT}}$ profile. Comparator, IDCHG, and VBATT function settings are preserved. When all the bits are 0, $\overline{\text{PROCHOT}}$ function is disabled. Bit 6: Independent comparator, 0: disable (default at POR); 1: enable Bit 5: ICRIT, 0: disable; 1: enable (default at POR) Bit 4: INOM, 0: disable (default at POR); 1: enable Bit 3: IDCHG, 0: disable (default at POR); 1: enable Bit 2: VBATT, 0: disable (default at POR); 1: enable Bit 1: $\overline{\text{BATPRES}}$, 0: disable (default at POR) ; 1: enable (one-shot rising edge triggered) Bit 0: ACOK, 0: disable (default at POR) ; 1: enable (one-shot falling edge triggered)

6.6.9 ProchotStatus Register

Figure 6-13. ProchotStatus Register (0x3A)

15	14	13	12	11	10	9	8
Reserved							
R							
7	6	5	4	3	2	1	0
Reserved	PROCHOT_STAT[6:0]						
R	R						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-14. ProchotStatus Register (0x3A)

BIT	BIT NAME	DESCRIPTION
[15:7]	Reserved	0 - Reserved
[6:0]	$\overline{\text{PROCHOT}}$ status (PROCHOT_STAT)	The status of all events triggered during the same $\overline{\text{PROCHOT}}$ pulse are set to 1. The register resets when either of below two conditions occurs. • Host first read after $\overline{\text{PROCHOT}}$ goes high • $\overline{\text{PROCHOT}}$ goes low to start another pulse. Bit 6: Independent comparator, 0: Not triggered; 1: Triggered Bit 5: ICRIT, 0: Not triggered; 1: Triggered Bit 4: INOM, 0: Not triggered; 1: Triggered Bit 3: IDCHG, 0: Not triggered; 1: Triggered Bit 2: VBATT, 0: Not triggered; 1: Triggered Bit 1: $\overline{\text{BATPRES}}$, 0: Not triggered ; 1: Triggered Bit 0: ACOK, 0: Not triggered ; 1: Triggered

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6.6.10 Charge Current Register

Figure 6-14. Charge Current Register (0x14)

15	14	13	12	11	10	9	8
Reserved			DACICHG[6:2]				
R			R/W				
7	6	5	4	3	2	1	0
DACICHG[1:0]		Reserved					
R/W		R					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-15. Charge Current Register (0x14), Using 10-mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
15		Not used; 1 = invalid write
14		Not used; 1 = invalid write
13		Not used; 1 = invalid write
12	Charge Current, DACICHG 6	0 = Adds 0 mA of charger current 1 = Adds 4096 mA of charger current
11	Charge Current, DACICHG 5	0 = Adds 0 mA of charger current 1 = Adds 2048 mA of charger current
10	Charge Current, DACICHG 4	0 = Adds 0 mA of charger current 1 = Adds 1024 mA of charger current
9	Charge Current, DACICHG 3	0 = Adds 0 mA of charger current 1 = Adds 512 mA of charger current
8	Charge Current, DACICHG 2	0 = Adds 0 mA of charger current 1 = Adds 256 mA of charger current
7	Charge Current, DACICHG 1	0 = Adds 0 mA of charger current 1 = Adds 128 mA of charger current
6	Charge Current, DACICHG 0	0 = Adds 0 mA of charger current 1 = Adds 64 mA of charger current
5		Not used; value ignored
4		Not used; value ignored
3		Not used; value ignored
2		Not used; value ignored
1		Not used; value ignored
0		Not used; value ignored

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6.6.11 Charge Voltage Register

Figure 6-15. Charge Voltage Register (0x15)

15	14	13	12	11	10	9	8
Reserved	DACV[10:4]						
R	R/W						
7	6	5	4	3	2	1	0
DACV[3:0]				Reserved			
R/W				R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-16. Charge Voltage Register (0x15)

BIT	BIT NAME	DESCRIPTION
15		Not used; 1 = invalid write
14	Charge voltage, DACV 10	0 = Adds 0 mV of charger voltage 1 = Adds 16384 mV of charger voltage
13	Charge voltage, DACV 9	0 = Adds 0 mV of charger voltage 1 = Adds 8192 mV of charger voltage
12	Charge voltage, DACV 8	0 = Adds 0 mV of charger voltage 1 = Adds 4096 mV of charger voltage
11	Charge voltage, DACV 7	0 = Adds 0 mV of charger voltage 1 = Adds 2048 mV of charger voltage
10	Charge voltage, DACV 6	0 = Adds 0 mV of charger voltage 1 = Adds 1024 mV of charger voltage
9	Charge voltage, DACV 5	0 = Adds 0 mV of charger voltage 1 = Adds 512 mV of charger voltage
8	Charge voltage, DACV 4	0 = Adds 0 mV of charger voltage 1 = Adds 256 mV of charger voltage
7	Charge voltage, DACV 3	0 = Adds 0 mV of charger voltage 1 = Adds 128 mV of charger voltage
6	Charge voltage, DACV 2	0 = Adds 0 mV of charger voltage 1 = Adds 64 mV of charger voltage
5	Charge voltage, DACV 1	0 = Adds 0 mV of charger voltage 1 = Adds 32 mV of charger voltage
4	Charge voltage, DACV 0	0 = Adds 0 mV of charger voltage 1 = Adds 16 mV of charger voltage
3		Not used; value ignored
2		Not used; value ignored
1		Not used; value ignored
0		Not used; value ignored

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6.6.12 Discharge Current Register

Figure 6-16. Discharge Current Register (0x39)

15	14	13	12	11	10	9	8
Reserved		DACIDCHG					Reserved
R		R/W					R
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-17. Discharge Current Register (0x39), Using 10-mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
15		Not used; 1 = invalid write
14	Discharge current, DACIDCHG 5	0 = Adds 0 mA of discharge current 1 = Adds 16384 mA of discharge current
13	Discharge current, DACIDCHG 4	0 = Adds 0 mA of discharge current 1 = Adds 8192 mA of discharge current
12	Discharge current, DACIDCHG 3	0 = Adds 0 mA of discharge current 1 = Adds 4096 mA of discharge current
11	Discharge current, DACIDCHG 2	0 = Adds 0 mA of discharge current 1 = Adds 2048 mA of discharge current
10	Discharge current, DACIDCHG 1	0 = Adds 0 mA of discharge current 1 = Adds 1024 mA of discharge current
9	Discharge current, DACIDCHG 0	0 = Adds 0 mA of discharge current 1 = Adds 512 mA of discharge current
8		Not used; value ignored
7		Not used; value ignored
6		Not used; value ignored
5		Not used; value ignored
4		Not used; value ignored
3		Not used; value ignored
2		Not used; value ignored
1		Not used; value ignored
0		Not used; value ignored

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6.6.13 Minimum System Voltage Register

Figure 6-17. Minimum System Voltage Register (0x3E)

15	14	13	12	11	10	9	8
Reserved		DACVS					
R		R/W					
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-18. Minimum System Voltage Register (0x3E)

BIT	BIT NAME	DESCRIPTION
15		Not used; 1 = invalid write
14		Not used; 1 = invalid write
13	Minimum system voltage, DACVS5	0 = Adds 0 mV of minimum system voltage 1 = Adds 8192 mV of minimum system voltage
12	Minimum system voltage, DACVS4	0 = Adds 0 mV of minimum system voltage 1 = Adds 4096 mV of minimum system voltage
11	Minimum system voltage, DACVS3	0 = Adds 0 mV of minimum system voltage 1 = Adds 2048 mV of minimum system voltage
10	Minimum system voltage, DACVS2	0 = Adds 0 mV of minimum system voltage 1 = Adds 1024 mV of minimum system voltage
9	Minimum system voltage, DACVS1	0 = Adds 0 mV of minimum system voltage 1 = Adds 512 mV of minimum system voltage
8	Minimum system voltage, DACVS0	0 = Adds 0 mV of minimum system voltage 1 = Adds 256 mV of minimum system voltage
7		Not used; value ignored
6		Not used; value ignored
5		Not used; value ignored
4		Not used; value ignored
3		Not used; value ignored
2		Not used; value ignored
1		Not used; value ignored
0		Not used; value ignored

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6.6.14 Input Current Register

Figure 6-18. Input Current Register (0x3F)

15	14	13	12	11	10	9	8
Reserved		DACIIN[7:2]					
R		R/W					
7	6	5	4	3	2	1	0
DACIIN[1:0]		Reserved					
R/W		R					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Using 10-mΩ Sense Resistor Maximum clamp at 10.560A, when use 5-mΩ Sense Resistor Maximum clamp at 21.12A.

Table 6-19. Input Current Register (0x3F), Using 10-mΩ Sense Resistor Maximum Clamp at 10.560A

BIT	BIT NAME	DESCRIPTION
15		Not used; 1 = invalid write
14		Not used; 1 = invalid write
13	Input current, DACIIN 7	0 = Adds 0 mA of input current 1 = Adds 8192 mA of input current
12	Input current, DACIIN 6	0 = Adds 0 mA of input current 1 = Adds 4096 mA of input current
11	Input current, DACIIN 5	0 = Adds 0 mA of input current 1 = Adds 2048 mA of input current
10	Input current, DACIIN 4	0 = Adds 0 mA of input current 1 = Adds 1024 mA of input current
9	Input current, DACIIN 3	0 = Adds 0 mA of input current 1 = Adds 512 mA of input current
8	Input current, DACIIN 2	0 = Adds 0 mA of input current 1 = Adds 256 mA of input current
7	Input current, DACIIN 1	0 = Adds 0 mA of input current 1 = Adds 128 mA of input current
6	Input current, DACIIN 0	0 = Adds 0 mA of input current 1 = Adds 64 mA of input current
5		Not used; value ignored
4		Not used; value ignored
3		Not used; value ignored
2		Not used; value ignored
1		Not used; value ignored
0		Not used; value ignored

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6.6.15 Register Exceptions

Certain system events, such as adapter or battery removal, introduce a response within the register set, such as to reset one or more fields to their POR value. Table Table 6-20 provides a list of register fields and their response to such system events.

Table 6-20. Register Exceptions

REGISTER FIELD	FIELD NAME	ACDET < 2.4V	$\overline{\text{BATPRES}}$ High	BATDEPL	EN_PKPWR= 1	UNDERVALUE	OVERVALUE
0x12H [5]	LEARN_EN	POR Value, Write Ignored	POR Value, Write Ignored	POR Value, Write Ignored			
0x38H [6]	EN_BATT_BOOST			POR Value if Boost Active			
0x37H [2]	EN_HYBRID_BOOST		POR Value				
0x38H [15:14]	PKPWR_TOVLD				Write ignored		
0x38H [9:8]	PKPWR_TMAX				Write ignored		
0x14H	ICHG	POR Value	POR Value			64 mA treated as 0	Write ignored
0x15H	VCHG		POR Value			Write ignored	Write ignored
0x39H	IDCHG					Write ignored	Write ignored
0x3EH	VSysMin					Write ignored	Write ignored
0x3FH	IDPM					Write ignored	Write ignored

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The BQ24810EVM evaluation module (EVM) is a complete charger module for evaluating the BQ24810. The application curves were taken using the BQ24810EVM. Refer to the *BQ24810 EVM User's Guide* for EVM information.

7.2 Typical Applications

Two typical applications are provided in this section. The first is a battery charging system that supports Battery-only Boost, see Figure 7-1. The second is a battery charging system that does not support battery-only boost, see Figure 7-22. For details on the operation of battery-only boost mode, refer to Section 6.4.3.

7.2.1 Typical System Schematic

Applications that use the battery-only boost function require that VCC be powered by a diode selector between the adapter input and the system rail as shown with the D1 and D2 components in Figure 7-1. It is important that VCC be powered from the system rail instead of directly from the battery in systems that support battery-only boost mode. During heavy load conditions while operating in battery-only boost mode, the current draw from the battery may cause the voltage as measured at the SRN pin to drop below the level required to support the switching regulator. By powering VCC instead from the system rail, it provides a sufficient voltage to the converter in this condition. Note that, in this configuration, initial power-up of the device from battery insert without an adapter incurs a voltage drop across the body diode of the Q3 switch in addition to the voltage drop across the D2 Schottky diode. For a partially-charged 1-S lithium-ion battery, this additional voltage drop across the Q3 backgate diode may drop the voltage at VCC below the under-voltage lockout. For this reason, this configuration should not be used with a 1-S lithium-ion battery.

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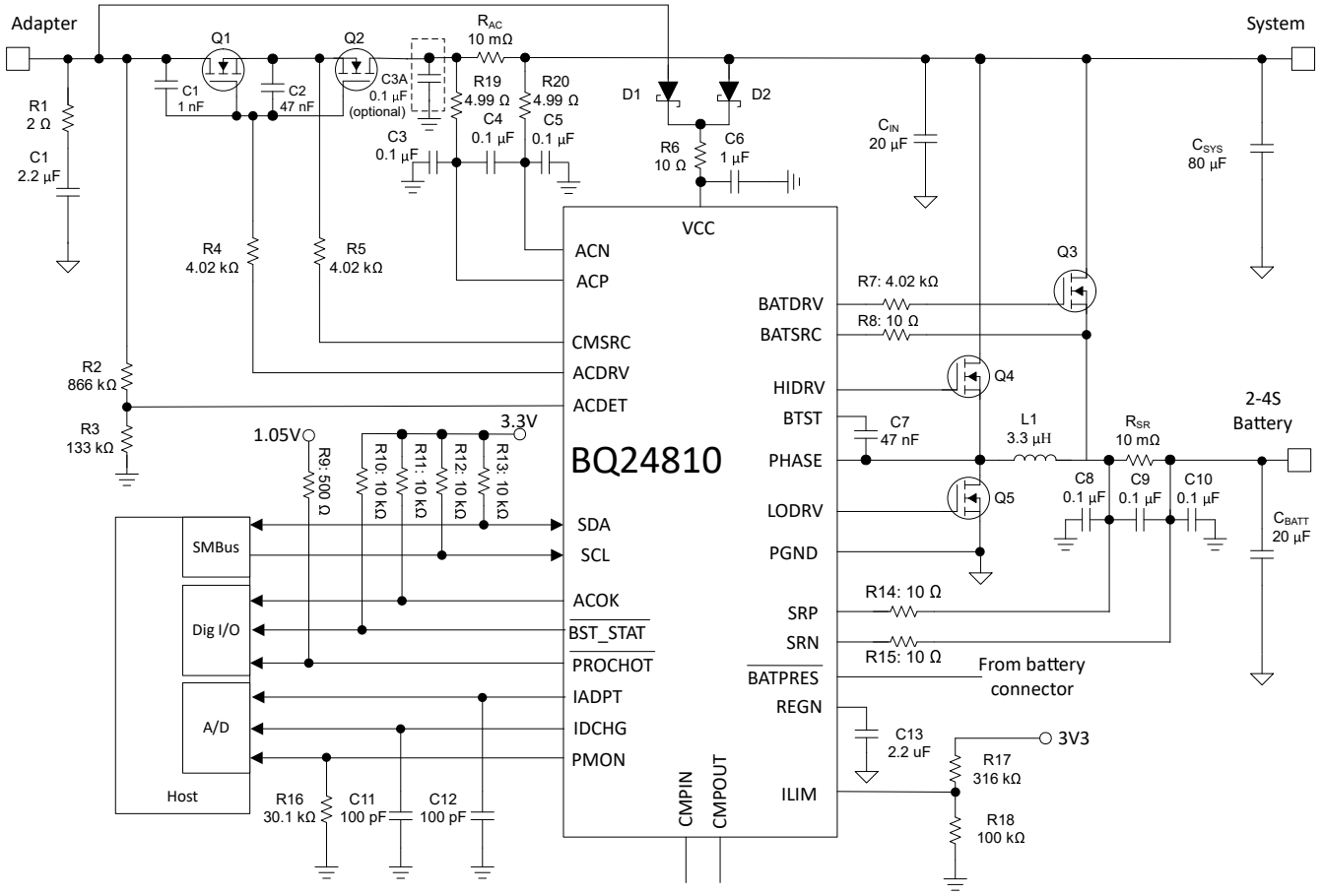


Figure 7-1. Typical System Schematic

7.2.1.1 Design Requirements

Table 7-1. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage(2)	17.7 V < Adapter Voltage < 24 V
Input Current Limit(2)	3.2 A for 65-W adapter
Battery Charge Voltage(1)	12592 mV for 3-s battery
Battery Charge Current(1)	4096 mA for 3-s battery
Battery Discharge Current(1)	10240 mA for 3-s battery supporting battery only boost mode

(1) Refer to battery specification for settings.
(2) Refer to adapter specification for settings for Input Voltage and Input Current Limit.

7.2.1.2 Detailed Design Procedure

The parameters are configurable using the evaluation software.

The simplified application circuits (see Figure 7-1 and Figure 7-22) show the minimum capacitance requirements for each pin. Inductor, capacitor, and MOSFET selection and are explained in the rest of this section. Refer to the *BQ24810 EVM User's Guide* for the full application schematic.

7.2.1.2.1 Adapter Current Sense Filter

To improve common-mode and differential-mode noise rejection for the adapter current sensing across the R_{AC} sense resistor, 0.1 µF C3, C4 and C5 capacitors are placed at ACP and ACN. For 2S lithium-ion battery

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applications, an additional 0.1 µF capacitor may be placed at C3A location in parallel with C3 for improved filtering. The C3A capacitor is not recommended for 3S or 4S battery applications.

7.2.1.2.2 Negative Output Voltage Protection

Reversely inserting the battery pack into the charger output during production or hard shorts on battery to ground will generate negative voltage on SRP, SRN, and BATSRC pins. IC internal electrostatic-discharge (ESD) diodes from GND pin to SRP or SRN pins and two anti-parallel (AP) diodes between SRP and SRN pins can be forward biased and negative current can pass through the ESD diodes and AP diodes when output has negative voltage, potentially damaging the IC. Small resistors for SRP, SRN and BATSRC (R12-R14) limit the negative current into these pins. The suggested resistor value is 10 Ω for the SRP, SRN, and BATSRC pins.

7.2.1.2.3 Reverse Input Voltage Protection

Q6, R12, and R13 in Figure 7-2 give system and IC protection from reversed adapter voltage. In normal operation, Q6 is turned off by negative Vgs. When adapter voltage is reversed, Q6 Vgs is positive. As a result, Q6 turns on to short gate and source of Q2 so that Q2 is off. Q2 body diode blocks negative voltage to system. However, CMSRC and ACDRV pins need R3 and R4 to limit the current due to the ESD diode of these pins when turned on. Q6 must have low Vgs threshold voltage and low Qgs gate charge so that it turns on before Q2. R3 and R4 must have sufficient power rating for the power dissipation when the ESD diode is on. If Q1 is replaced by Schottky diode for reverse adapter voltage protection, Q2, R3 and R4 are not needed.

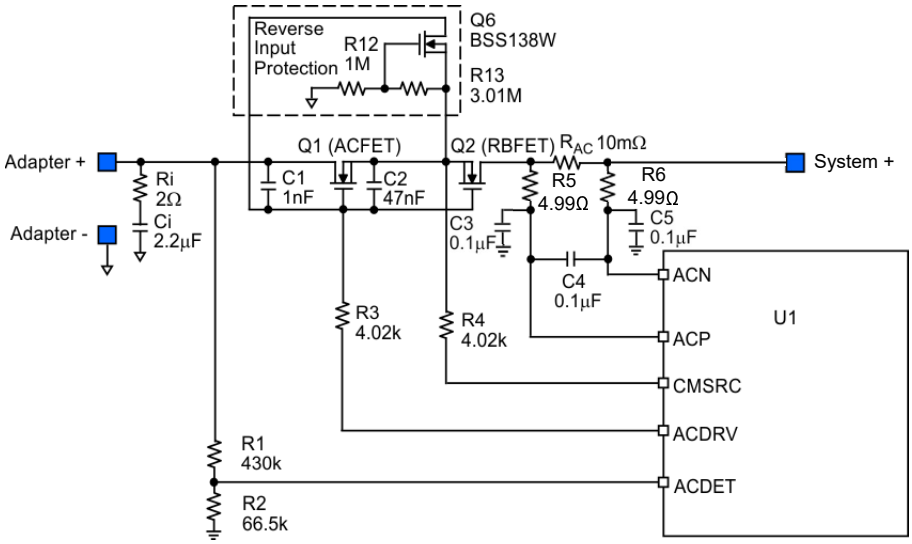


Figure 7-2. Reverse Input Voltage Protection Circuit

7.2.1.2.4 Reduce Battery Quiescent Current

When the adapter is not present, if VCC is powered with voltage higher than UVLO directly or indirectly (such as through a LDO or switching converter) from battery, the internal BATFET charge pump gives the BATFET pin 6-V higher voltage than the SRN pin to drive the n-channel BATFET. As a result, the battery has higher quiescent current. This is only necessary when the battery powers the system due to a high system current that goes through the MOSFET channel instead of the body diode to reduce conduction loss and extend the battery working life. When the system is totally shutdown, it is not necessary to let the internal BATFET charge pump work. The host controller can turn off the switches in the battery pack to disconnect the battery from the system. Some packs may wake up again if the voltage on SRN pin stays above pack UVLO too long. By setting ChargeOption1() bit[1] to 1, host can enable current source inside charger IC to discharge the SRN pin quickly. As a result, the system is discharged down to zero to minimize the quiescent current.

7.2.1.2.5 C_{IN} Capacitance

C_{IN} provides input capacitance when the converter is operating in forward buck charging mode. This should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is

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half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 6:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (6)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed as close as possible to the drain of the high side switching MOSFET (HIFET). The voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for 19- V to 20-V input voltage. 10- to 20-µF capacitance is suggested for typical of 3- to 4-A charging current.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

7.2.1.2.6 L_1 Inductor Selection

The BQ24810 has four selectable fixed switching frequencies. Higher switching frequency allows the use of smaller inductor and capacitor values but decreases efficiency and increases EMI. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (7)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (f_S) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (8)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9V to 12.6V for 3-cell battery pack. For 20-V adapter voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12-V to 16.8-V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design. Refer to the Section 7.2.1.2.8 section for recommended inductor value by charging current and switching frequency.

7.2.1.2.7 C_{BATT} Capacitance

C_{BATT} is the output capacitor for buck charging mode and should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (9)$$

The BQ24810 has internal loop compensator. To get good loop stability, the resonant frequency of the inductor and C_{BATT} should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25V X7R or X5R for capacitor. Refer to the Section 7.2.1.2.8 section for recommended C_{BATT} capacitor value by charge current and switching frequency. Place the capacitors after charging current sensing resistor to get the best charge current regulation accuracy.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead

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to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

7.2.1.2.8 Buck Charging Internal Compensation

The synchronous buck PWM converter uses a fixed frequency voltage control scheme and internal type III compensation network. The LC output filter gives a characteristic resonant frequency:

$$f_O \approx \frac{1}{2\pi\sqrt{LC}} \quad (10)$$

The resonant frequency, f_o, is used to determine the compensation to ensure there is sufficient phase margin for the target bandwidth. The LC output filter should be selected to give a resonant frequency of 10- to 20-kHz nominal for the best performance. Suggested component values for different ChargeCurrent() REG0x14 settings are shown in Table 7-2 to Table 7-3 for the available switching frequencies of 300 - 800 kHz. Note that these tables are generated based on the charging configuration, so the Output Capacitor is the capacitance at the battery connection, close to the SRN node of the battery charging sense resistor. The procedure for generating these tables is to first select the inductor value to have a ripple current that is in the range of 20 - 40% of the target charge current. Once the inductor value has been calculated, the output capacitance is chosen to have an output stage resonant frequency between 10- to 20-kHz.

Table 7-2. Suggested Component Values by Charge Current for 600-kHz and 800-kHz (Default) Switching Frequencies

CHARGE CURRENT	2A	3A	4A	6A	8A
L_1 (µH)	6.8 or 8.2	5.6 or 6.8	3.3 or 4.7	3.3	2.2
C_{BATT} (µF) (Effective after derating)	20	20	20	30	40

Table 7-3. Suggested Component Values by Charge Current for 300-kHz and 400-kHz Switching Frequencies

CHARGE CURRENT	3A	4A	5A	6A	8A
L_1 (µH)	10	6.8 or 8.2	6.8	5.6	4.7
C_{BATT} (µF) (Effective after derating)	15	20	20	20	20

Ceramic capacitors show a DC-bias effect. This effect reduces the effective capacitance when a DC-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a DC bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value to get the required value at the operating point.

7.2.1.2.9 C_{SYS} Capacitance

C_{SYS} capacitance combines with C_{IN} to provide output capacitance when BQ24810 is operating in battery only boost mode and provides bulk capacitance in all modes to support fast load transients on SYS. The distinction between C_{IN} and C_{SYS} is that C_{IN} is ceramic capacitor only and must be placed very close to the high side switching MOSFET Q4. C_{SYS} may be a mixture of ceramic and tantalum capacitors and does not have as tight of a placement requirement.

If battery only boost mode is supported, the sum of (C_{SYS} + C_{IN}) is chosen according to the internal compensation requirement of the Section 7.2.1.2.8 section.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data

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sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

7.2.1.2.10 Battery Only Boost Internal Compensation

The synchronous boost PWM converter uses a fixed frequency voltage control scheme and internal type III compensation network. The LC output filter has a characteristic resonant frequency:

$$f_O \approx \frac{1}{2\pi\sqrt{LC}} \cdot \frac{V_{IN}}{V_o} \tag{11}$$

The resonant frequency, f_o, is used to determine the compensation to ensure there is sufficient phase margin for the target bandwidth. The LC output filter should be selected to give a resonant frequency of 3.5- to 6.0-kHz nominal for the best performance. Suggested output capacitance versus inductor is shown in Table 7-4. The designer should first determine the inductor value using the tables provided in Section 6.4.6, then use Table 7-4 to determine the appropriate battery only boost output capacitance using that inductor value. These tables are generated based on the battery-only boost configuration, so the output capacitance is measured at the system node, which is the sum of C_{IN} and C_{SYS} as shown on Figure 7-1. The minimum capacitance value is calculated using boost ratio (V_{SYS} / V_{BATT} = V_O / V_{IN}) of 1.5 and a resonant frequency of 6.0 kHz. Also, a minimum output capacitance of 60 µF is recommended regardless of resonant frequency to support the transient response. Table 7-4 shows the minimum suggested value. Additional C_{SYS} may be added for improved transient response.

Table 7-4. Suggested Minimum Component Value for Battery-Only Boost Operation

L_1 (µH)	2.2	3.3	4.7	5.6	6.8	8.2
C_{IN} (µF) (Effective after derating)	20	20	20	20	20	20
Minimum C_{SYS}(µF) (Effective after derating)	120	80	50	40	40	40

7.2.1.2.11 Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred for 19- to 20-V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD};\ FOM_{bottom} = R_{DS(on)} \times Q_G \tag{12}$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ($R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (f_S), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times f_s \tag{13}$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

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$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \tag{14}$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \tag{15}$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}) and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \tag{16}$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^{2} \times R_{DS(on)} \tag{17}$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F), non-synchronous mode charging current ($I_{NONSYNC}$), and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \tag{18}$$

The maximum charging current in non-synchronous mode can be up to 0.25 A for a 10-mΩ charging current sensing resistor or 0.5 A if battery voltage is below 2.5 V. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

7.2.1.2.12 Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on VCC pin.

There are several methods to damping or limit the over voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However these two solutions may not have low cost or small size.

A cost effective and small size solution is shown in Figure 7-3. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for VCC pin. C2 is VCC pin decoupling capacitor and it should be place to VCC pin as close as possible. C2 value should be less than C1 value so R1 can dominate the equivalent ESR value to get enough damping effect. R2 is used to limit inrush current of D1 to prevent D1 getting damage when adapter hot plug-in. R2 and C2 should have 10us time constant to limit the dv/dt on VCC pin to reduce inrush current when adapter hot plug in. R1 has high inrush current. R1 package must be sized enough to handle inrush current power loss according to resistor manufacturer's data sheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

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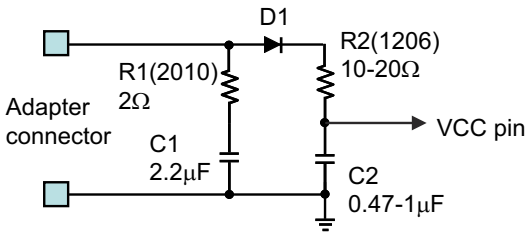
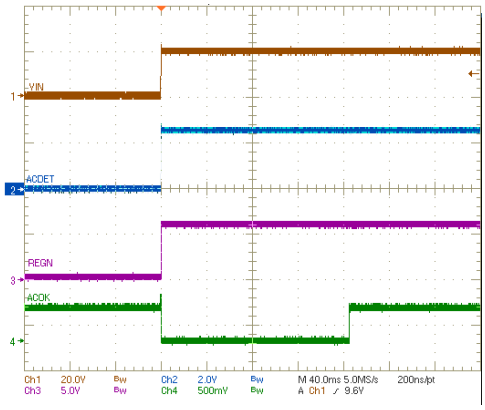


Figure 7-3. Input Filter

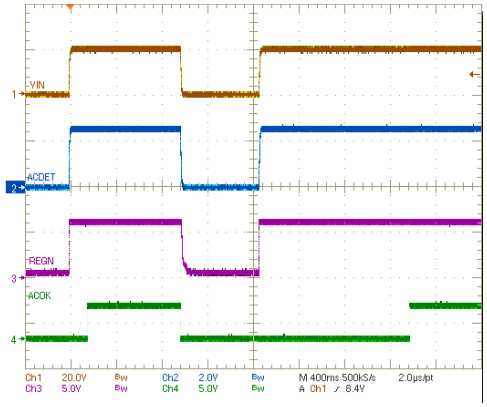
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7.2.1.3 Application Curves



No Battery

Figure 7-4. VCC, ACDET, REGN, and ACOK During Power Up



V_{BAT} = 11V

Figure 7-5. Power On ACOK Delay at 1st and 2nd Adapter Plug-in

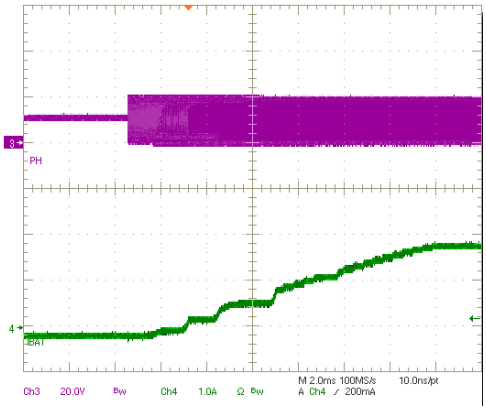


Figure 7-6. Charge Enable With Soft Start

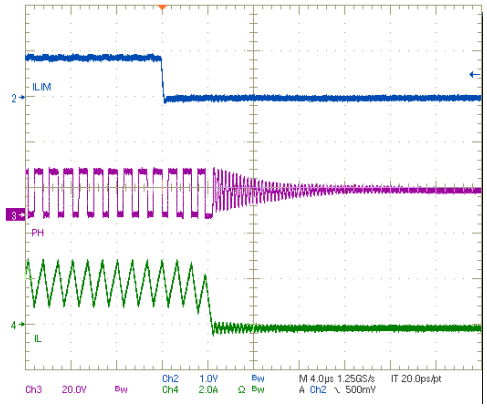
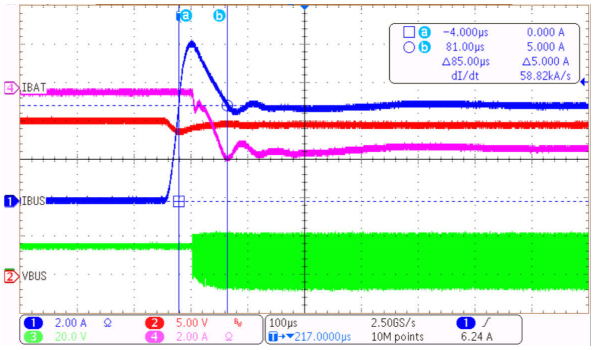


Figure 7-7. Charge Disabled by ILIM



V_{IN} = 19.5V I_{DPM} = 5056mA V_{BAT} = 14.8V
I_{SYS} = 0A - 7A FDPM_RISE=104% FDPM_DEG=10µs
TURBO_SPEED=10b

Figure 7-8. Hybrid Power Boost Mode Enabled

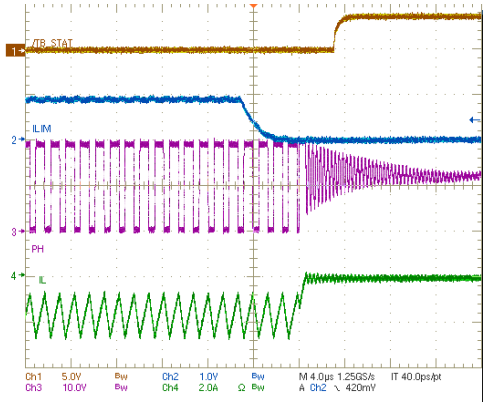


Figure 7-9. Hybrid Power Boost Mode Disabled by ILIM

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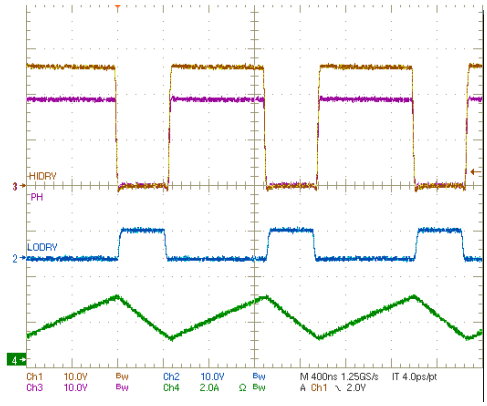


Figure 7-10. Converter in Continuous Conduction Mode (CCM) During Charging

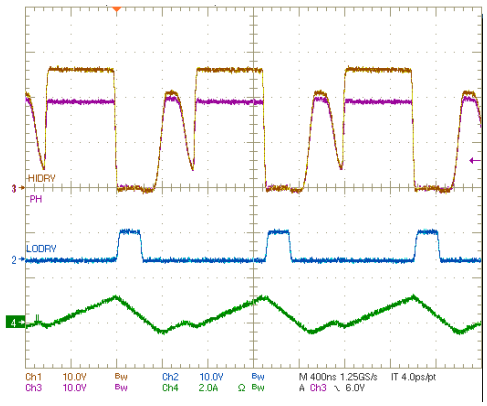


Figure 7-11. Converter in Discontinuous Conduction Mode (DCM) During Charging

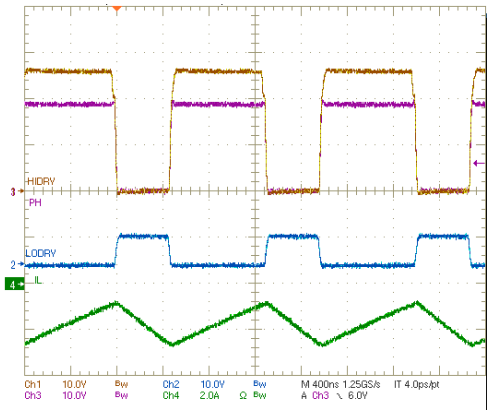
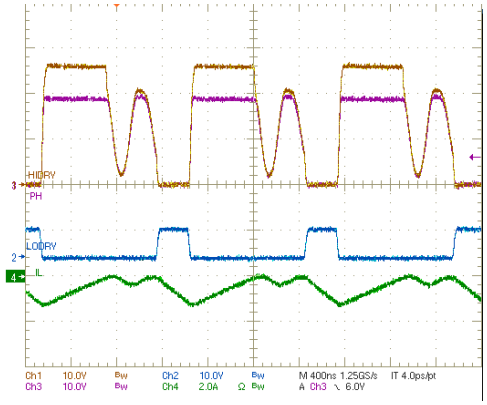
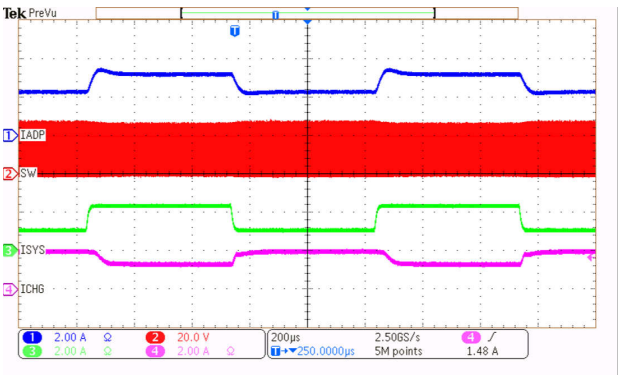


Figure 7-12. Converter in Continuous Conduction Mode During Hybrid Power Boost Mode



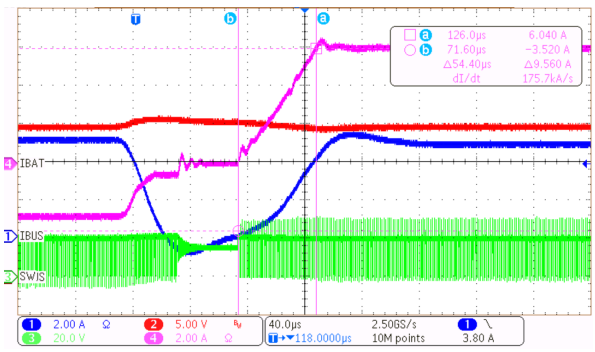
I_{DPM} = 4096mA I_{CHG} = 2432mA VBAT = 11V

Figure 7-13. Converter in Discontinuous Conduction Mode During Hybrid Power Boost Mode



V_{IN} = 19.5V I_{DPM} = 3072mA V_{BAT} = 11V
I_{CHG} = 2048mA I_{SYS} = 1A - 2.2A

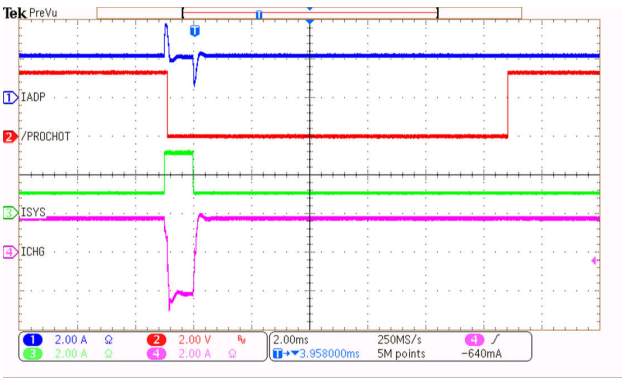
Figure 7-14. Input Current Regulation During System Load Transient



V_{IN} = 19.5V I_{DPM} = 5A V_{BAT} = 14.8V
I_{SYS} = 0A - 8A I_{CHG} = 6A SEL_MORE_PRESET=11
EN_ICHG_PRESET=1 EN_CHG_FAST_TRANS=1

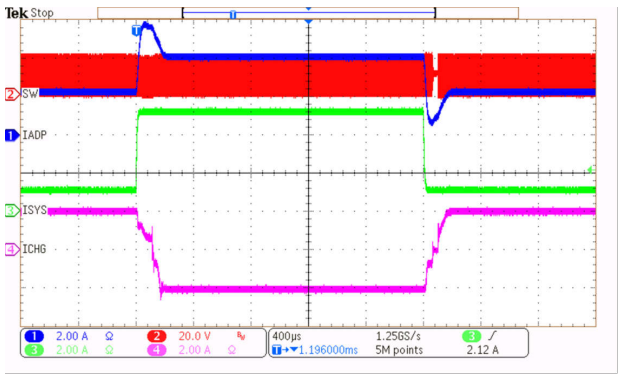
Figure 7-15. Hybrid Power Boost Mode With Charge Enable

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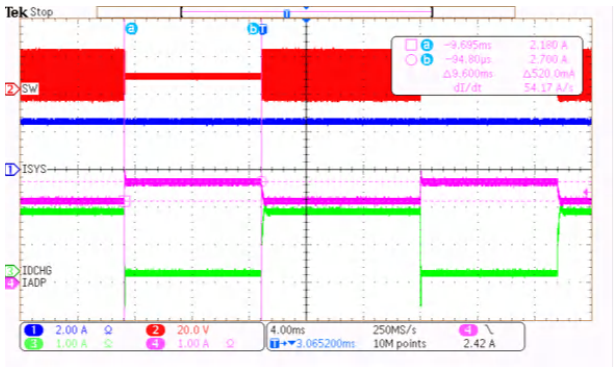
V_{IN} = 19.5V I_{DPM} = 2048mA I_{CHG} = 2048mA
V_{BAT} = 11V I_{CRIT} 120% x I_{DPM} I_{SYS} = 1A - 3A
$\overline{\text{PROCHOT}}$ pulsewidth 0x3C[4:3] = 10 (10ms)

Figure 7-16. Hybrid Power Boost Mode with Charge Enable, $\overline{\text{PROCHOT}}$ Asserted



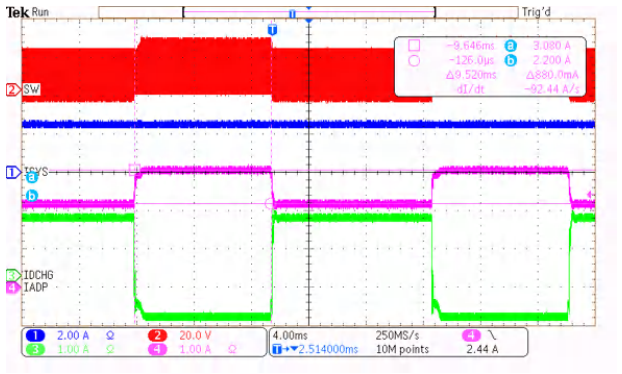
V_{IN} = 19.5V I_{DPM} = 2560mA V_{BAT} = 11V
I_{CHG} = 2048mA I_{DCHG} = 2048mA I_{SYS} = 1A - 5A

Figure 7-17. Hybrid Power Boost Mode With Discharge Current Regulation



V_{IN} = 19.5V V_{BAT} = 7.2V I_{SYS} = 2.5A
I_{LIM1} = 2048 mA I_{LIM2} = 3072 mA T_{OVLD} = 10ms
T_{MAX} = 20ms

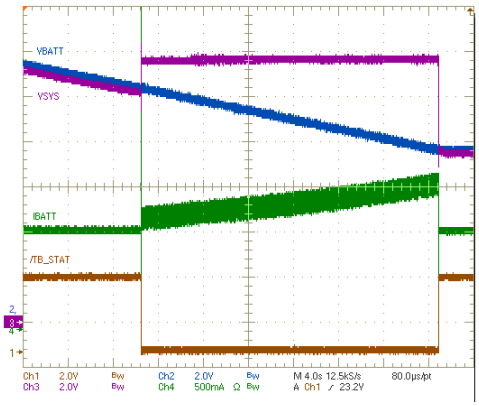
Figure 7-18. Peak Power Mode with PKPWR_ENCHRG=0



V_{IN} = 19.5V V_{BAT} = 7.2V I_{SYS} = 2.5A
I_{LIM1} = 2048mA I_{LIM2} = 3072mA T_{OVLD} = 10ms
T_{MAX} = 20ms

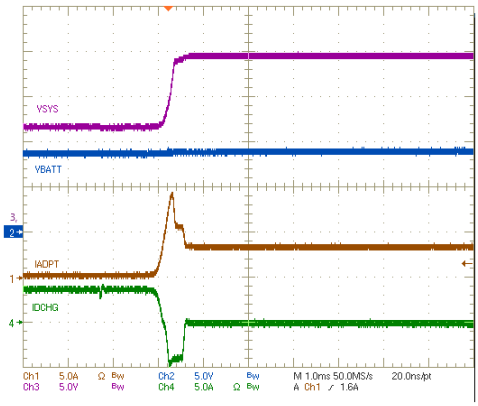
Figure 7-19. Peak Power Mode with PKPWR_ENCHRG=1

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V_{BATT} = 12V to 6V V_{SYSMIN} = 10.24V VBOOST = 2.3V
I_{SYS} = 1A

Figure 7-20. Battery Only Boost Entry and Exit by Battery Voltage



V_{BATT} = 9.0V V_{SYSMIN} = 10.24V VBOOST = 2.3V
I_{SYS} = 3.0A V_{ADPT} = 20V

Figure 7-21. Battery Only Boost Exit by Adapter Plug In

7.2.2 Migration from Previous Devices (Does Not Support Battery Only Boost)

The system schematic shown in Figure 7-22 is compatible with the previous generation BQ24780S. The BQ24810 may be used in this system configuration; however, this system configuration does not support the battery only boost mode. The requirements for systems that do not operate in battery only boost are slightly relaxed. Firstly, less capacitance is required at C_{SYS}. Secondly, the VCC diode selector (D1 and D2) may be configured to select between the adapter input and battery input. Because this provides a path directly from the battery to VCC across a single Schottky diode, this configuration may be used in a 1-S lithium-ion battery system in addition to 2-S, 3-S and 4-S lithium-ion battery systems.

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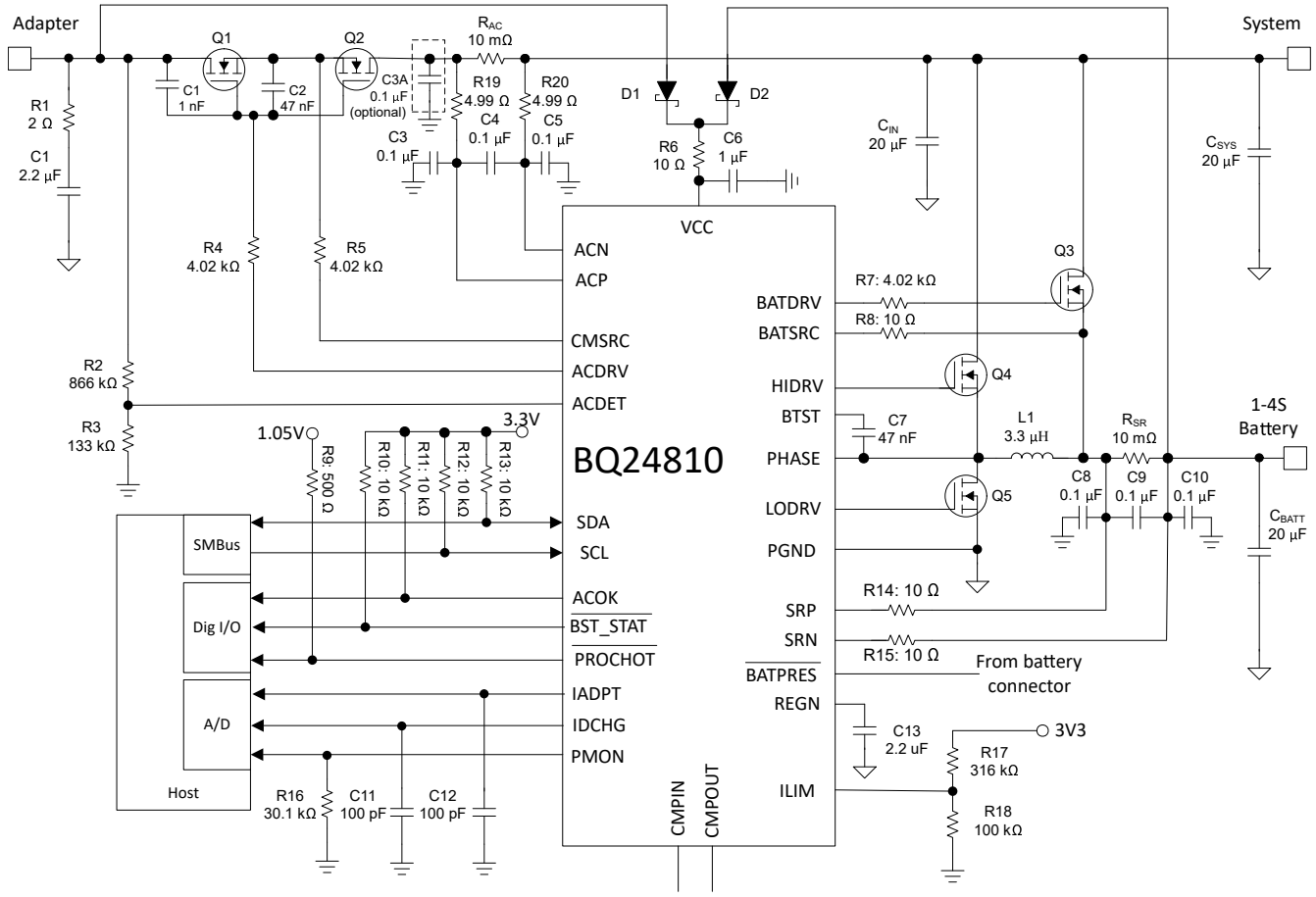


Figure 7-22. Typical System Schematic for Migrating From BQ24780S (Does not support battery only boost)

7.2.2.1 Design Requirements

Table 7-5. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage(1)	17.7 V < Adapter Voltage < 24 V
Input Current Limit(1)	3.2 A for 65-W adapter
Battery Charge Voltage(2)	12592 mV for 3-s battery
Battery Charge Current(2)	4096 mA for 3-s battery
Battery Discharge Current(2)	6144 mA for 3-s battery

(1) Refer to battery specification for settings.
(2) Refer to adapter specification for settings for Input Voltage and Input Current Limit.

7.2.2.2 Detailed Design Procedure

Refer to Section 7.2.1.2 for the detailed design procedures for all components except C_{SYS}.

7.2.2.2.1 C_{SYS} Capacitance

C_{SYS} capacitance combines with C_{IN} to provide bulk capacitance in all modes to support fast load transients on SYS. The distinction between C_{IN} and C_{SYS} is that C_{IN} is ceramic capacitor only and must be placed very close to the high side switching MOSFET Q4. C_{SYS} may be a mixture of ceramic and tantalum capacitors and does not have as tight of a placement requirement.

When battery only boost mode is not supported the value of C_{SYS} should be chosen according to the decoupling requirements of the system load. A minimum of 20-µF is recommended in addition to the capacitance supplied at C_{IN}.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

7.2.2.3 Application Curves

Refer to Section 7.2.1.3 for the application curves.

7.3 Power Supply Recommendations

When adapter is attached, and ACOK goes HIGH, the system is connected to adapter through ACFET/RBFET. An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. If battery only boost mode is not used, the adapter detect threshold must be set to a value greater than the maximum battery voltage, but lower than the minimum allowed adapter voltage. If battery only boost mode is used, the adapter detect threshold must instead be set to a value greater than the battery boost regulation voltage as determined by REG0x3E and REG0x38[5].

When adapter is removed, the system is connected to battery through BATFET. Typically the battery depletion threshold should be greater than the minimum system voltage so that the battery capacity can be fully utilized for maximum battery life.

7.4 Layout

7.4.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 7-23) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout of PCB according to this specific order is essential.

1. Place input capacitor as close as possible to switching MOSFET’s supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET’s gate pins and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
3. Place inductor input pin to switching MOSFET’s output pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 7-24 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC
5. Place output capacitor next to the sensing resistor output and ground
6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling
8. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case if possible).
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible

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10. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
11. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the WQFN information, See *Quad Flatpack No-Lead Logic Packages Application Report* and *QFN and SON PCB Attachment Application Report*.

7.4.2 Layout Examples

7.4.2.1 Layout Consideration of Current Path

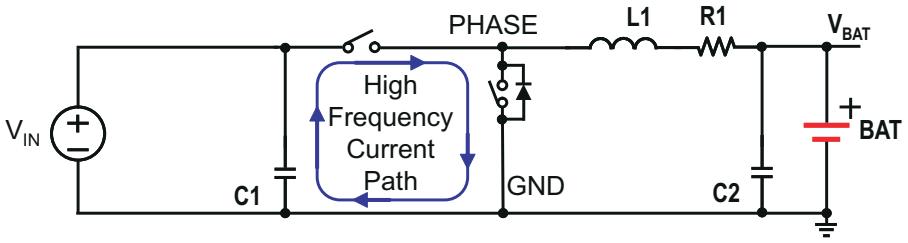


Figure 7-23. High Frequency Current Path

7.4.2.2 Layout Consideration of Short Circuit Protection

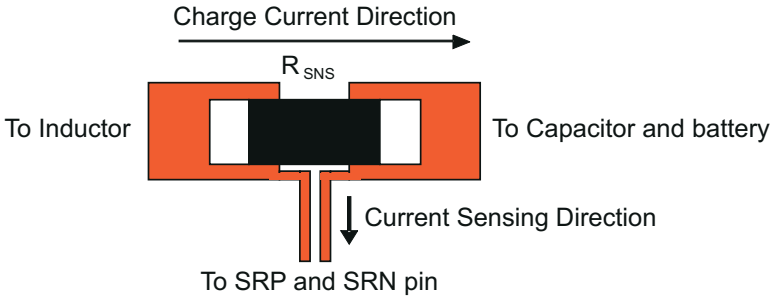


Figure 7-24. Sensing Resistor PCB Layout

7.4.2.3 Layout Consideration for Short Circuit Protection

The BQ24810 has a unique short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across $R_{DS(on)}$ of the MOSFETs after a certain amount of blanking time. For a MOSFET short or inductor short circuit, the over current condition is sensed by two comparators, and two counters are triggered. After seven occurrences of a short circuit event, the charger will be latched off. To reset the charger from latch-off status, remove and then reconnect the adapter. Figure 7-25 shows the BQ24810 short circuit protection block diagram.

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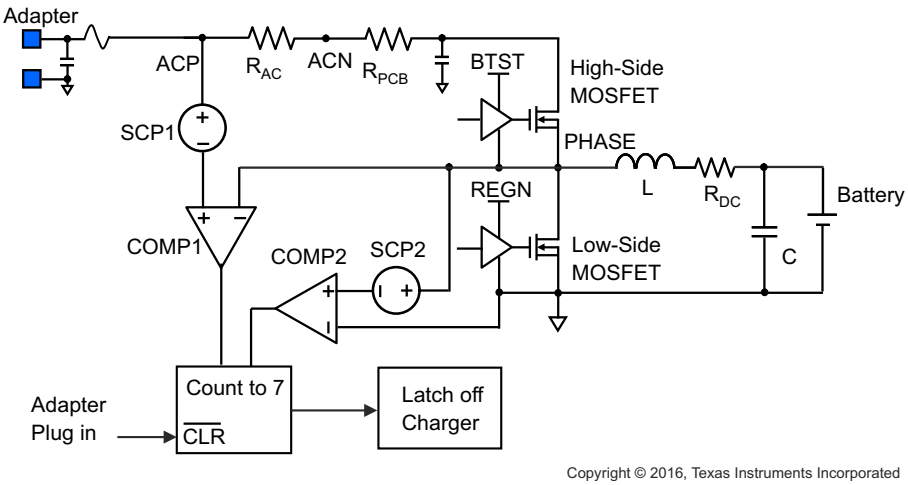
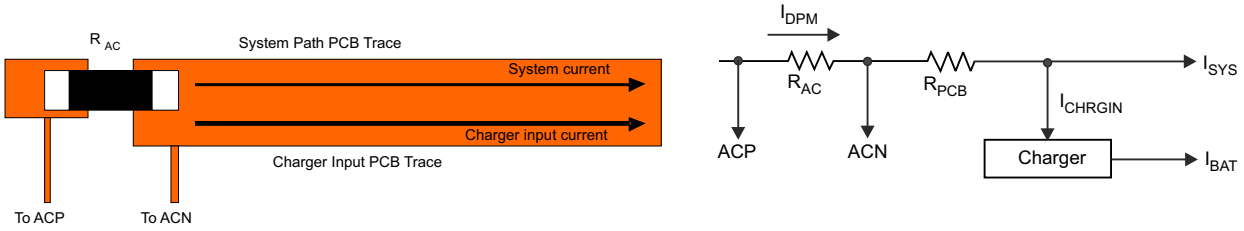


Figure 7-25. Block Diagram of BQ24810 Short Circuit Protection

In normal operation, the low side MOSFET current is from source to drain which generates a negative voltage drop when it turns on, as a result the over current comparator can not be triggered. When the high side switch short circuit or inductor short circuit happens, the large current of low side MOSFET is from drain to source and can trigger low side switch over current comparator. The BQ24810 senses the low side switch voltage drop through the PHASE pin and GND pin.

The high-side FET short is detected by monitoring the voltage drop between ACP and PHASE. As a result, it not only monitors the high side switch voltage drop, but also the adapter sensing resistor voltage drop and PCB trace voltage drop from ACN pin of R_{AC} to charger high side switch drain. Usually, there is a long trance between input sensing resistor and charger converting input, a careful layout will minimize the trace effect.

To prevent unintentional charger shut down in normal operation, MOSFET $R_{DS(on)}$ selection and PCB layout is very important. Figure 7-26 shows a improvement PCB layout example and its equivalent circuit. In this layout, the system current path and charger input current path is not separated, as a result, the system current causes voltage drop in the PCB copper and is sensed by the IC. The worst layout is when a system current pull point is after charger input; as a result all system current voltage drops are counted into over current protection comparator. The worst case for IC is when the total system current and charger input current sum equals the DPM current. When the system pulls more current, the charger IC tries to regulate the R_{AC} current as a constant current by reducing the charging current.

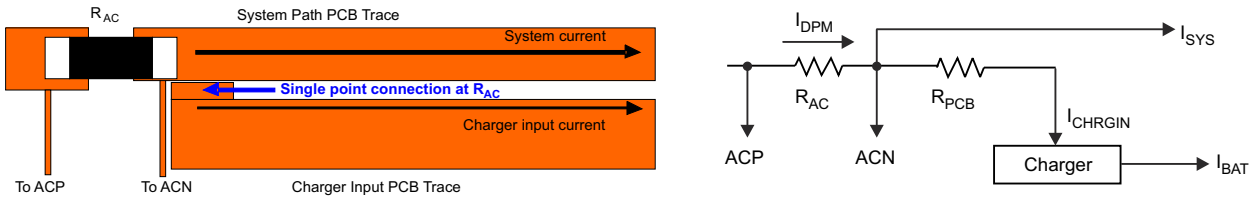


(a) PCB Layout **(b) Equivalent Circuit**

Figure 7-26. PCB Layout Example

Figure 7-27 shows the optimized PCB layout example. The system current path and charge input current path is separated, as a result the IC only senses charger input current caused PCB voltage drop and minimized the possibility of unintentional charger shut down in normal operation. This also makes PCB layout easier for high system current application.

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(a) PCB Layout (b) Equivalent Circuit

Figure 7-27. Optimized PCB Layout Example

The total voltage drop sensed by IC can be express as the following equation.

$$V_{top} = R_{AC} \times I_{DPM} + R_{PCB} \times (I_{CHRGIN} + (I_{DPM} - I_{CHRGIN}) \times k) + R_{DS(on)} \times I_{PEAK} \quad (19)$$

where the R_{AC} is the AC adapter current sensing resistance, I_{DPM} is the DPM current set point, R_{PCB} is the PCB trace equivalent resistance, I_{CHRGIN} is the charger input current, k is the PCB factor, $R_{DS(on)}$ is the high side MOSFET turn on resistance and I_{PEAK} is the peak current of inductor. Here the PCB factor k equals 0 means the best layout shown in Figure 7-27 where the PCB trace only goes through charger input current while k equals 1 means the worst layout shown in Figure 7-26 where the PCB trace goes through all the DPM current. The total voltage drop must below the high side short circuit protection threshold to prevent unintentional charger shut down in normal operation.

The low side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[7] disables LSFET protection when set to 0 and enables the protectoin with a threshold of 250 mV when set to 1. The high side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[8] disables HSFET protection when set to 0 and enables the protection with a threshold of 750 mV when set to 1. For a fixed PCB layout, host should set proper short circuit protection threshold level to prevent unintentional charger shut down in normal operation.

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following: *BQ24810 EVM User's Guide*

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24810RUYR	Active	Production	WQFN (RUY) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24810

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

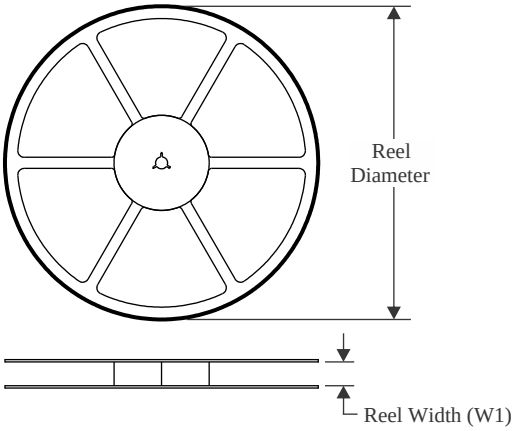
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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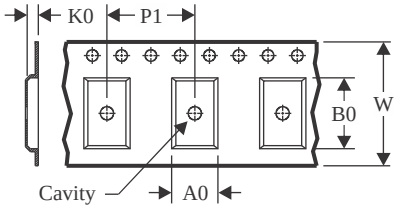
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

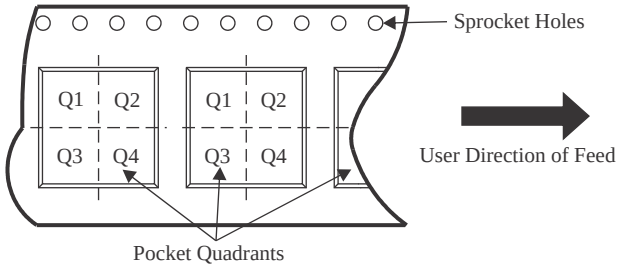


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

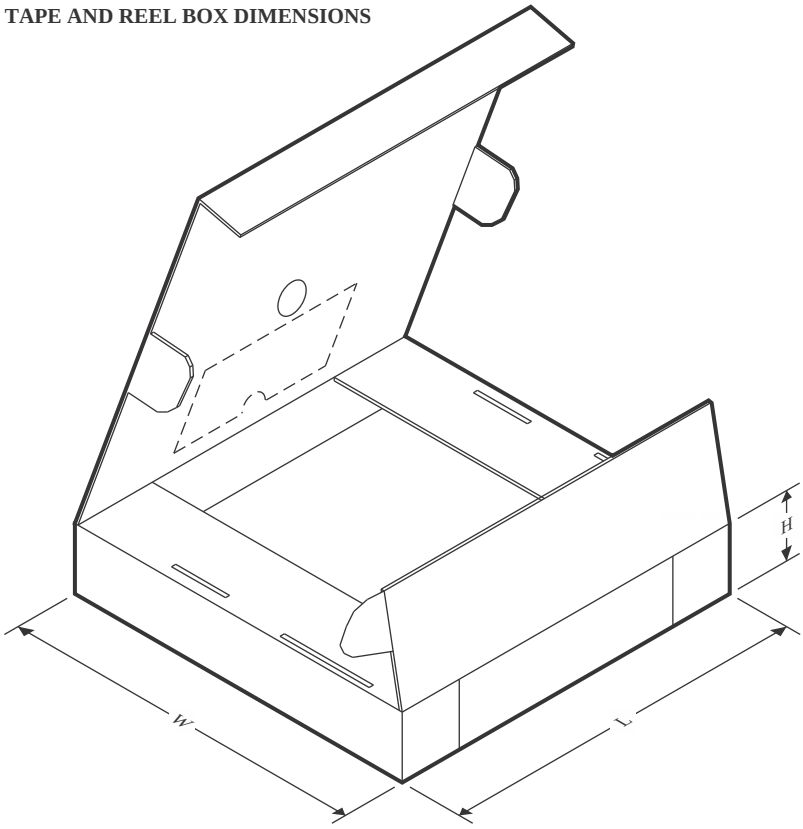
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24810RUYR	WQFN	RUY	28	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

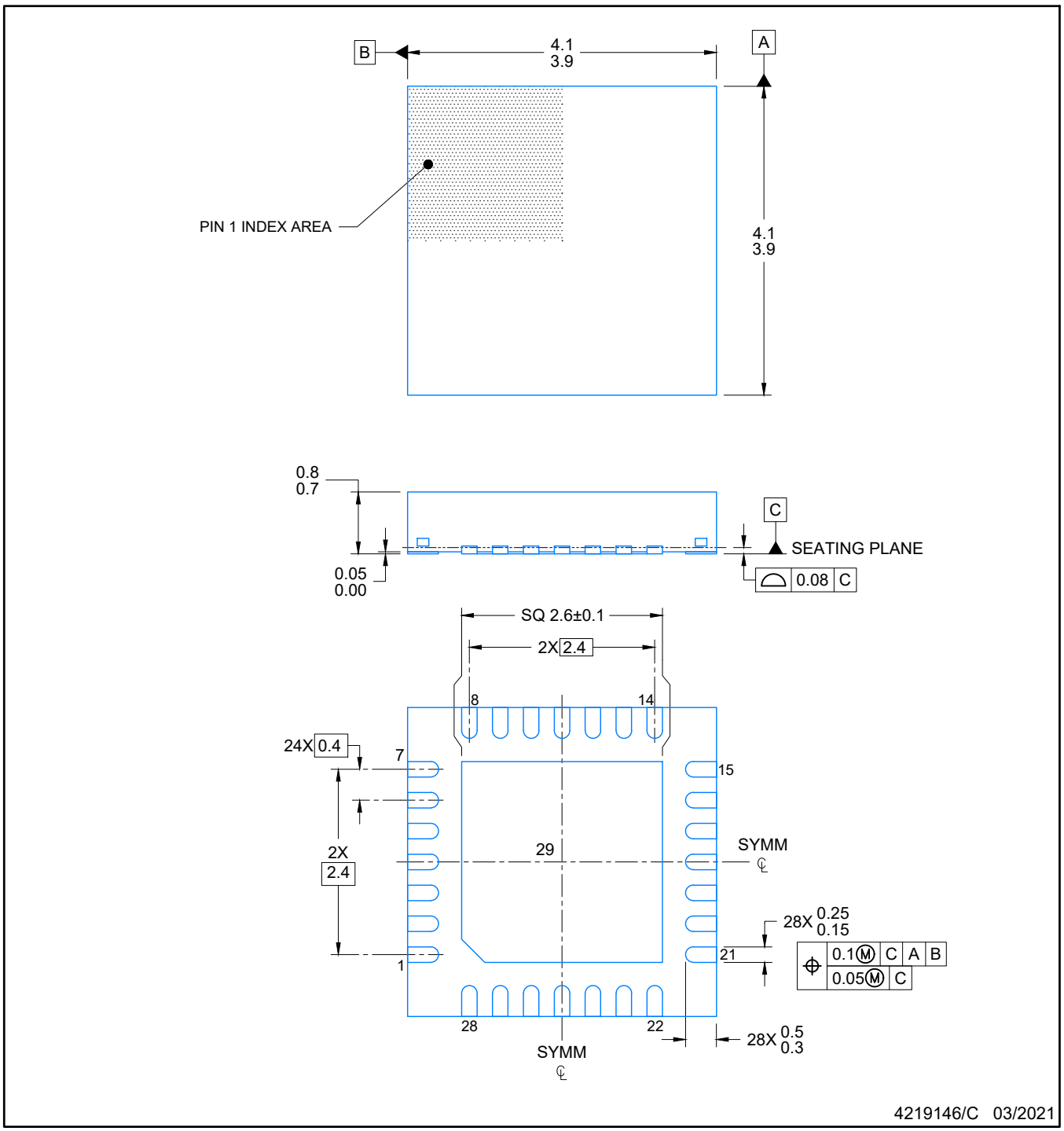
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24810RUYR	WQFN	RUY	28	3000	353.0	353.0	32.0

PACKAGE OUTLINE

RUY0028A

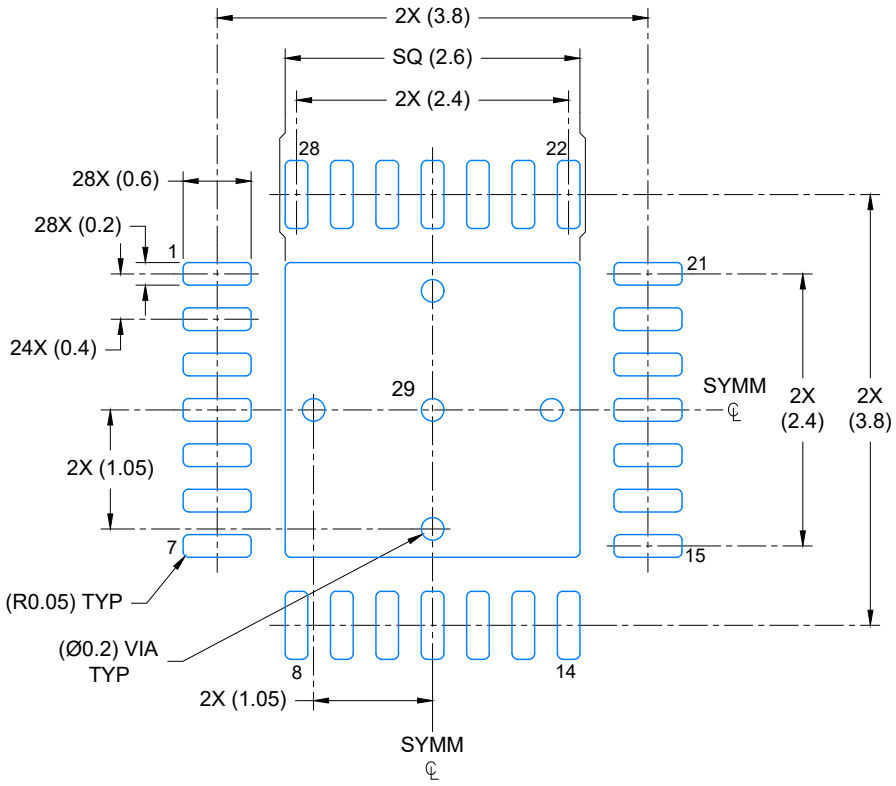
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

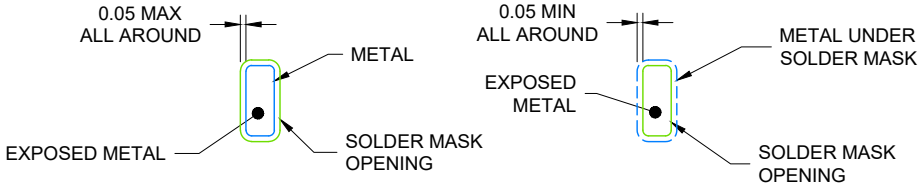


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

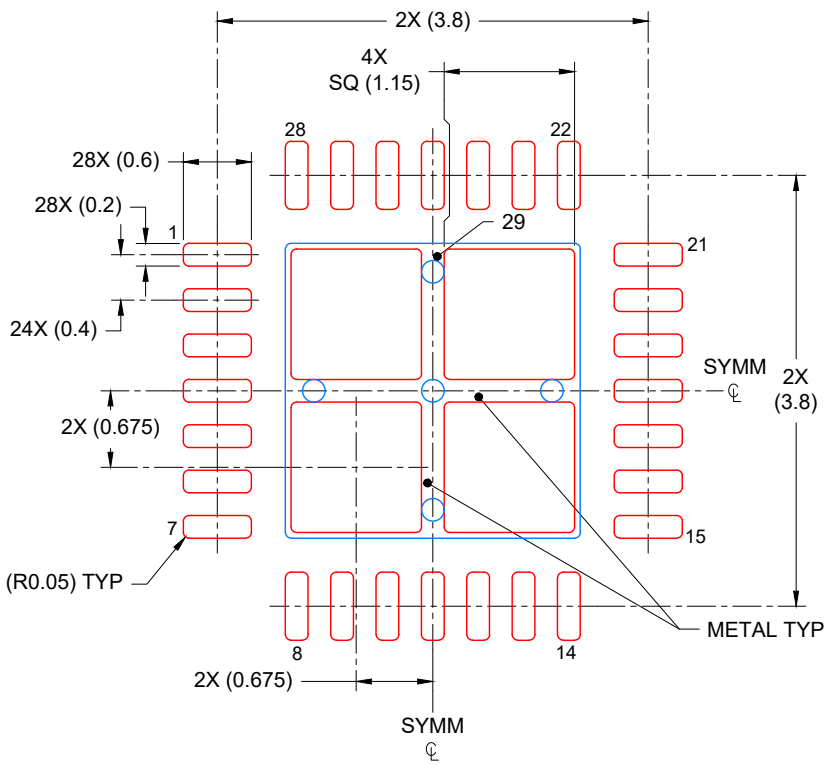
SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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