

SINGLE-CELL Li-ION CHARGE MANAGEMENT IC WITH TIMER-ENABLE FOR PDAs AND INTERNET APPLIANCES

FEATURES

- **Highly Integrated Solution With FET Pass Transistor and Reverse-Blocking Schottky and Thermal Protection**
- **Timer-Enable Function That Allows Host to Disable Charge Timer and Termination When Charge Current Is Shared With a Load or When Battery Is Absent**
- **Integrated Voltage and Current Regulation With Programmable Charge Current**
- **High-Accuracy Voltage Regulation (±1%)**
- **Ideal for Low-Dropout Linear Charger Designs for Single-Cell Li-Ion Packs With Coke or Graphite Anodes**
- **Up to 1.2-A Continuous Charge Current**
- **Safety-Charge Timer During Preconditioning and Fast Charge**
- **Integrated Cell Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage of Charge**
- **Optional Temperature or Input-Power Monitoring Before and During Charge**
- **Various Charge-Status Output Options for Driving Single, Double, or Bicolor LEDs or Host-Processor Interface**
- **Charge Termination by Minimum Current and Time**
- **Low-Power Sleep Mode**
- **Packaging: 5 mm × 5 mm MLP (bq24007)or 20-Lead TSSOP PowerPAD™**

APPLICATIONS

- **PDAs**
- **Internet Appliances**
- **MP3 Players**
- **Digital Cameras**

DESCRIPTION

The bq2400x series ICs are advanced Li-Ion linear charge management devices for highly integrated and space-limited applications. They combine high-accuracy current and voltage regulation; FET pass-transistor and reverse-blocking Schottky; battery conditioning, temperature, or input-power monitoring; charge termination; charge-status indication; and charge timer in a small package.

The bq24007 and bq24008 provide the timer-enable function, allowing the host to disable the charge timer when charge current is shared with a load or when the battery is absent. This feature is ideal for applications such as cellular phones, PDAs, and internet appliances.

The bq2400x measures battery temperature using an external thermistor. For safety reasons, the bq2400x inhibits charge until the battery temperature is within the user-defined thresholds. Alternatively, the user can monitor the input voltage to qualify charge. The bq2400x series then charge the battery in three phases: preconditioning, constant current, and constant voltage. If the battery voltage is below the internal low-voltage threshold, the bq2400x uses low-current precharge to condition the battery. A preconditioning timer provides additional safety. Following pre-conditioning, the bq2400x applies a constant-charge current to the battery. An external sense-resistor sets the magnitude of the current. The constant-current phase is maintained until the battery reaches the charge-regulation voltage. The bq2400x then transitions to the constant voltage phase. The user can configure the device for cells with either coke or graphite anodes. The accuracy of the voltage regulation is better than ±1% over the operating junction temperature and supply voltage range.

Charge is terminated by maximum time or minimum taper current detection

The bq2400x automatically restarts the charge if the battery voltage falls below an internal recharge threshold.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002 − 2004, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGE		CHARGE STATUS CONFIGURATION
	20-LEAD HTTSOP PowerPAD™ (PWP)(1)	20-LEAD 5 mm × 5 mm MLP (RGW)(2)	
−40°C to 125°C	bq24007PWP	bq24007RGW	Single LED
	bq24008PWP	Not available	Single bicolor LED

(1) The PWP package is available taped and reeled. Add R suffix to device type (e.g. bq24007PWPR) to order. Quantities 2500 devices per reel.
(2) The RGW package is available taped and reeled. Add R suffix to device type (e.g. bq24007RGWR) to order. Quantities 3000 devices per reel.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JA}	Θ_{JC}	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$
PWP(1)	30.88°C/W	1.19°C/W	3.238 W	0.0324W/°C
RGW(2)	31.41°C/W	1.25°C/W	3.183 W	0.0318W/°C

(1) This data is based on using the JEDEC high-K board and topside traces, top and bottom thermal pad (6,5 × 3,4 mm), internal 1 oz power and ground planes, 8 thermal via underneath the die connecting to ground plane.
(2) This data is based on using the JEDEC high-K board and topside traces, top and bottom thermal pad (3,25 × 3,25 mm), internal 1 oz power and ground planes, 9 thermal via underneath the die connecting to ground plane.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	bq24007 bq24008
Supply voltage (V_{CC} with respect to GND)	13.5 V
Input voltage (IN, ISNS, $\overline{\text{TMR EN}}$, APG/THERM/CR/STAT1/STAT2, VSENSE, TMR SEL, VSEL) (all with respect to GND)	13.5 V
Output current (OUT pins)	2 A
Output sink/source current (STAT1 and STAT2)	10 mA
Operating free-air temperature range, T_A	−40°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Junction temperature range, T_J	−40°C to 125°C
Lead temperature (Soldering, 10 s)	300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.5	10	V
Input voltage, VIN	4.5	10	V
Continuous output current		1.2	A
Operating junction temperature range, T_J	−40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature supply and input voltages, and V_I (V_{CC}) ≥ V_I (IN) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} current	V_{CC} > V_{CC_UVLO}			1	mA
Standby current (sum of currents into OUT and VSENSE pins)	V_{CC} < V_{CC_UVLO}, $V_{O(OUT)}$ = 4.3 V, VSENSE = 4.3 V		2	4	μA

VOLTAGE REGULATION, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Output voltage	VSEL = V_{SS}, 0 < I_O ≤ 1.2 A	4.059	4.10	4.141	V
	VSEL = V_{CC}, 0 < I_O ≤ 1.2 A	4.158	4.20	4.242	V
Load regulation	1 mA ≤ I_O ≤ 1.2 A, $V_{I(IN)}$= 5 V, V_{CC} =5 V, T_J = 25°C		1		mV
Line regulation	$V_{O(OUT)}$+V_{DO}+$V_{ilim(MAX)}$ < $V_{I(VCC)}$ < 10 V, T_J = 25°C		0.01		%/V
Dropout voltage = VI(IN)-$V_{O(OUT)}$	I_O = 1.0 A, 4.9 V <$V_{I(Vcc)}$< 10 V			0.7	V
	I_O = 1.2 A, $V_{O(OUT)}$+V_{DO}+$V_{(ilim)}$MAX <$V_{I(VCC)}$< 10 V			0.8	V

CURRENT REGULATION, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Current regulation threshold	VSENSE < $V_{O(VSEL-LOW/HIGH)}$	0.095	0.1	0.105	V
Delay time	VSENSE pulsed above VVLOWV to I_O = 10% of regulated value(1)			1	ms
Rise time	I_O increasing from 10% to 90% of regulated value. $R_{(SNS)}$ ≥ 0.2 Ω, (1)	0.1		1	ms

(1) Specified by design, not production tested.

CURRENT SENSE RESISTOR, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
External current sense resistor range ($R_{(SNS)}$)	100 mA ≤ ilim ≤ 1.2 A	0.083		1	Ω

PRECHARGE CURRENT REGULATION, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Precharge current regulation	V_{SENSE}<V_{LOWV}, 0.083 ≤ $R_{(SNS)}$ ≤ 1.0 Ω	40	60	80	mA

V_{CC} UVLO COMPARATOR, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Start threshold		4.35	4.43	4.50	V
Stop threshold		4.25	4.33	4.40	V
Hysteresis		50			mV

APG/THERM COMPARATOR, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Upper trip threshold		1.480	1.498	1.515	V
Lower trip threshold		0.545	0.558	0.570	V
Input bias current				1	μA

LOWV COMPARATOR, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Start threshold		2.80	2.90	3.00	V
Stop threshold		3.00	3.10	3.20	V
Hysteresis		100			mV

ELECTRICAL CHARACTERISTICS CONTINUED

over recommended operating junction temperature supply and input voltages, and V_I (V_{CC}) ≥ V_I (IN) (unless otherwise noted)

HIGHV (RECHARGE) COMPARATOR, 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		3.80	3.90	4.00	V

OVERV COMPARATOR, 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		4.35	4.45	4.55	V
Stop threshold		4.25	4.30	4.35	V
Hysteresis		50			mV

TAPERDET COMPARATOR, 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Trip threshold		12	18.5	25	mV

$\overline{\text{TMR EN}}$ LOGIC INPUT, 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	kΩ

VSEL LOGIC INPUT, 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	kΩ

TMR SEL INPUT 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.7			V
Low-level input voltage				0.6	V
Input bias current	$V_{I(TMR\ SEL)}$ ≤ 5V			15	µA

STAT1, STAT2 (bq24008), 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output (low) saturation voltage	I_O = 10 mA			1.5	V
Output (low) saturation voltage	I_O = 4 mA			0.6	V
Output (high) saturation voltage	I_O = −10 mA	V_{CC}−1.5			V
Output (high) saturation voltage	I_O = −4 mA	V_{CC}−0.5			V
Output turn on/off time	I_O = ± 10 mA, C = 100 p(1)			100	µs

(1) Specified by design, not production tested.

POWER-ON RESET (POR), 0°C ≤ T_J ≤ 125°C					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POR delay	See Note 1	1.2		3	ms
POR falling-edge deglitch	See Note 1	25		75	µs

(1) Specified by design, not production tested.

ELECTRICAL CHARACTERISTICS CONTINUED

over recommended operating junction temperature supply and input voltages, and V_I (V_{CC}) ≥ V_I (IN) (unless otherwise noted)

APG/THERM DELAY, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
APG/THERM falling-edge deglitch	See Note 1	25		75	µs

(1) Specified by design, not production tested.

TIMERS, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
User-selectable timer accuracy	T_A = 25°C	−15%		15%	
		−20%		20%	
Precharge and taper timer			22.5		minute

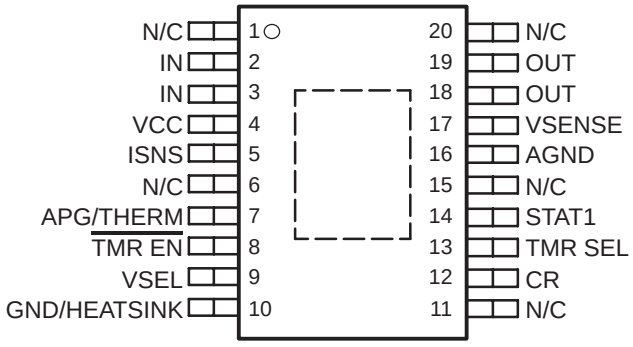
THERMAL SHUTDOWN, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Thermal trip	See Note 1		165		°C
Thermal hysteresis	See Note 1		10		°C

(1) Specified by design, not production tested.

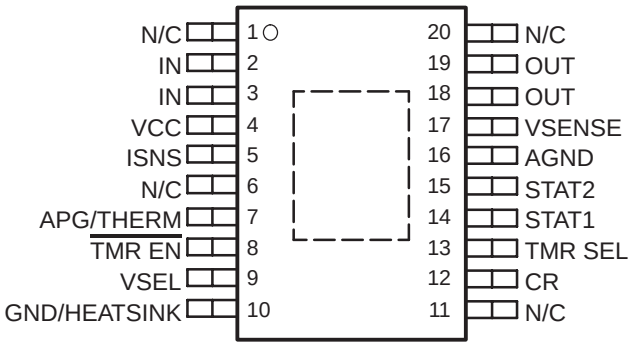
CR PIN, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Output voltage	0 < $I_{O(CR)}$ < 100 µA, $C_{(CR)}$ = 0.22 µF	2.81	2.85	2.88	V

PIN ASSIGNMENTS

bq24007
PWP PACKAGE
(TOP VIEW)

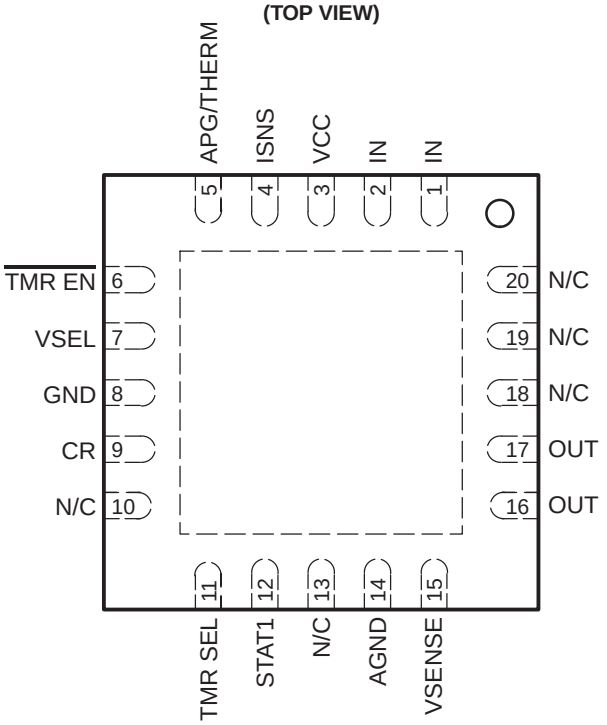


bq24008
PWP PACKAGE
(TOP VIEW)



N/C − Do not connect

bq24007
RGW PACKAGE
(TOP VIEW)

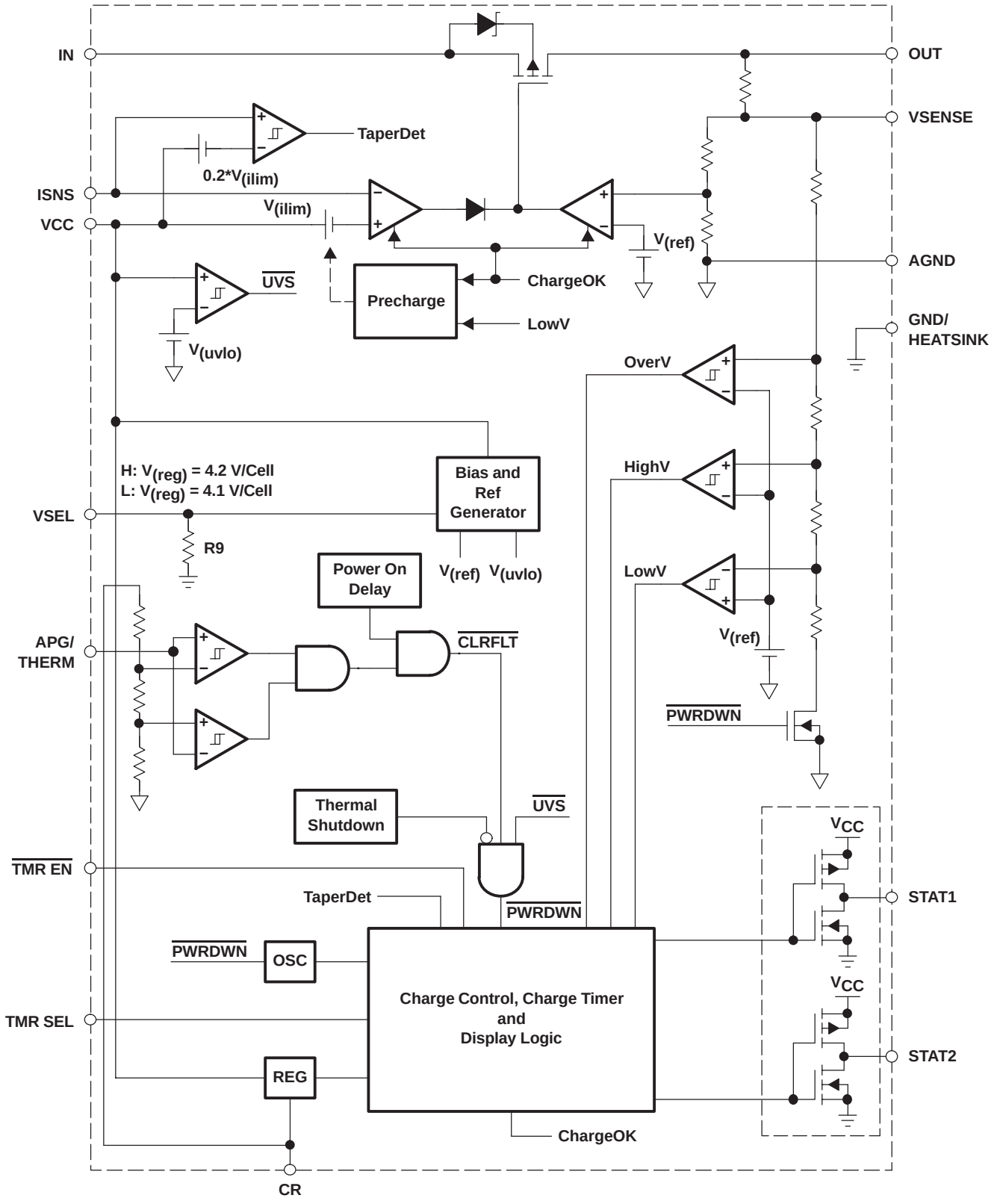


N/C − Do Not Connect

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PWP	RGW		
AGND	16	14		Ground pin; connect close to the negative battery terminal.
APG/THERM	7	5	I	Adapter power good input/thermistor sense input
CR	12	9	I	Internal regulator bypass capacitor
$\overline{\text{TMR EN}}$	8	6	I	Charge-enable input. Active-high enable input with internal pulldown. Low-current stand-by mode active when EN is low.
GND/HEATSINK	10	8		Ground pin; connect to PowerPAD heat-sink layout pattern.
IN	2, 3	1, 2	I	Input voltage. This input provides the charging voltage for the battery.
ISNS	5	4	I	Current sense input
N/C	1, 6, 11, 15, 20	10, 13, 18−20		No connect. These pins must be left floating. Pin 15 is N/C on bq24007PWP only. Pin 13 is N/C on bq24007RGW only.
OUT	18, 19	16, 17	O	Charge current output
STAT1	14	12	O	Status display output 1
STAT2	15	−	O	Status display output 2 (for bq24008 only)
TMR SEL	13	11	I	Charge timer selection input
VCC	4	3	I	Supply voltage
VSEL	9	7	I	4.1-V or 4.2-V charge regulation selection input
VSENSE	17	15	I	Battery voltage sense input

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

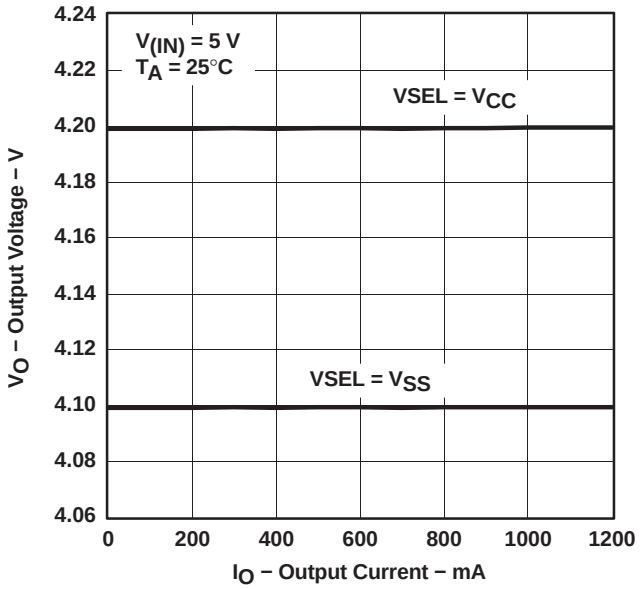


Figure 1

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

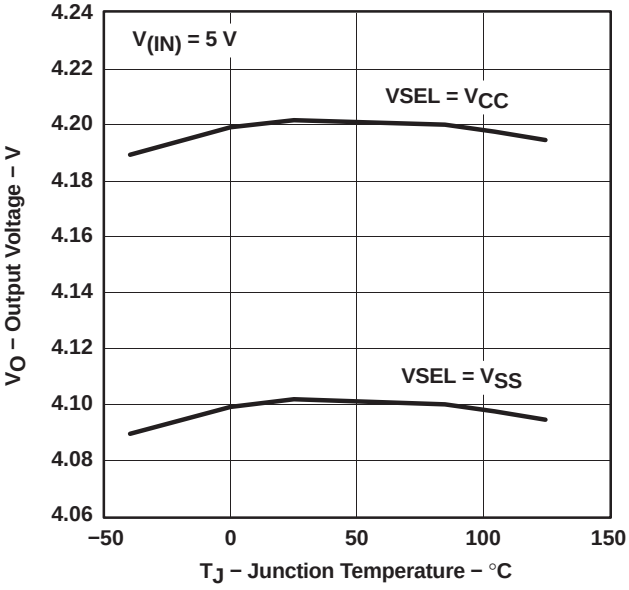


Figure 2

OUTPUT VOLTAGE vs INPUT VOLTAGE

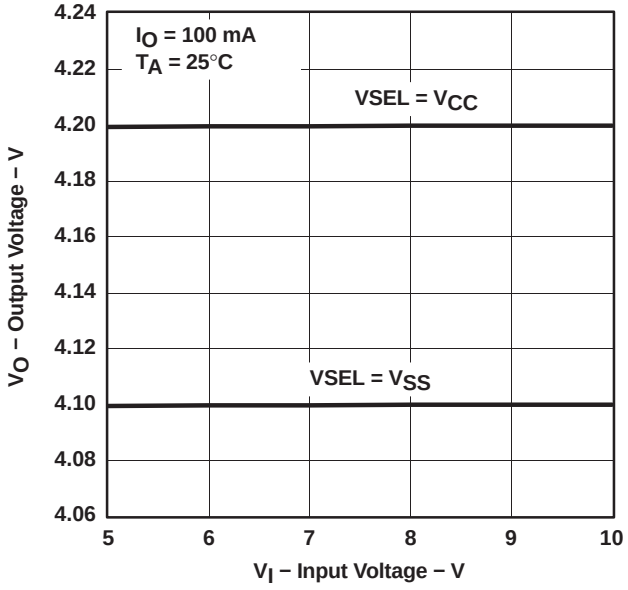


Figure 3

CURRENT SENSE VOLTAGE vs INPUT VOLTAGE

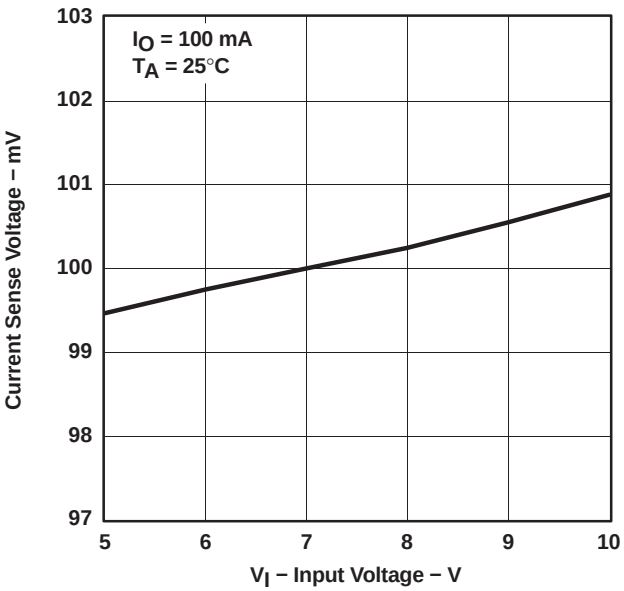


Figure 4

TYPICAL CHARACTERISTICS

CURRENT SENSE VOLTAGE vs JUNCTION TEMPERATURE

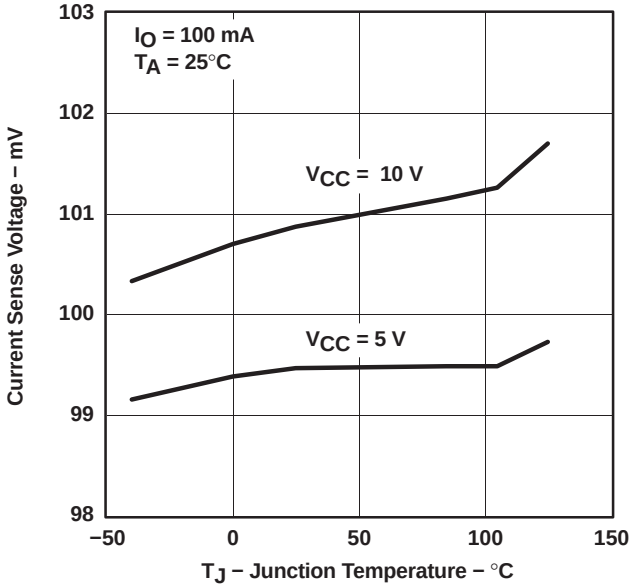


Figure 5

QUIESCENT CURRENT vs INPUT VOLTAGE

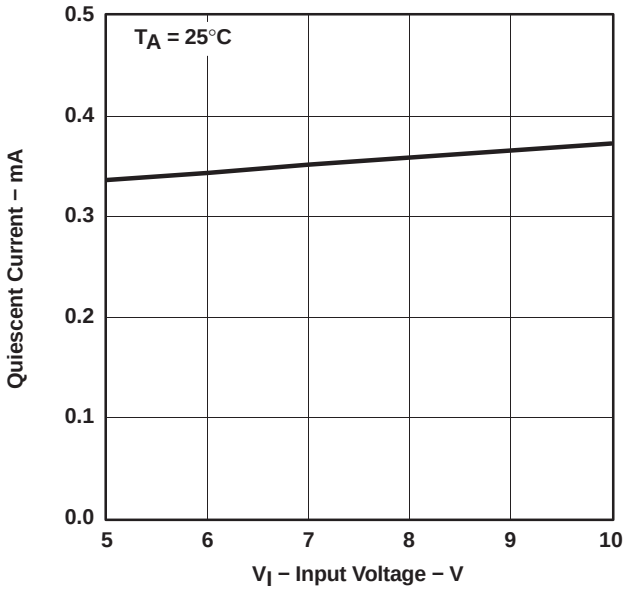


Figure 6

DROPOUT VOLTAGE vs INPUT VOLTAGE

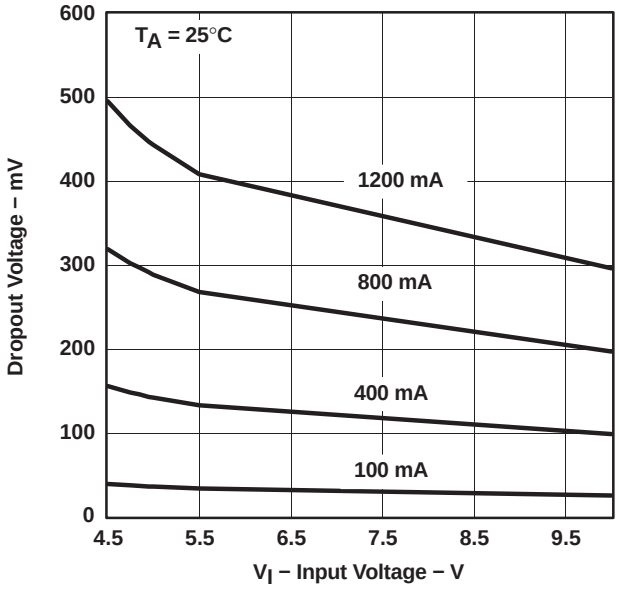


Figure 7

TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE vs OUTPUT CURRENT

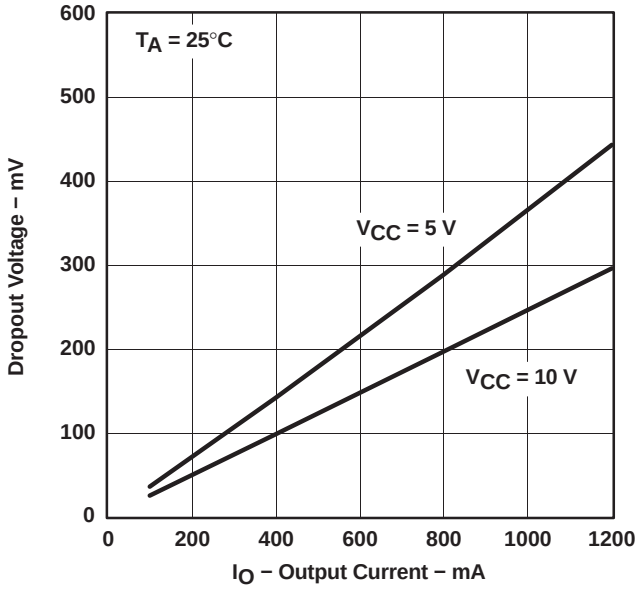


Figure 8

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

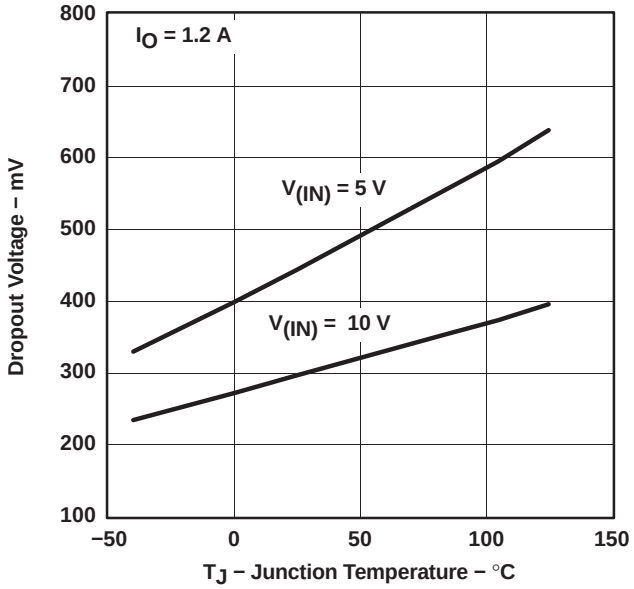


Figure 9

REVERSE CURRENT vs JUNCTION TEMPERATURE

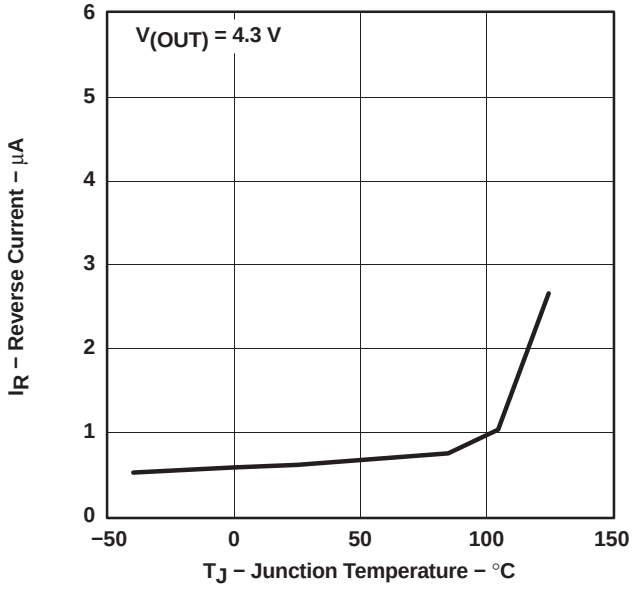


Figure 10

REVERSE CURRENT LEAKAGE vs VOLTAGE ON OUT PIN

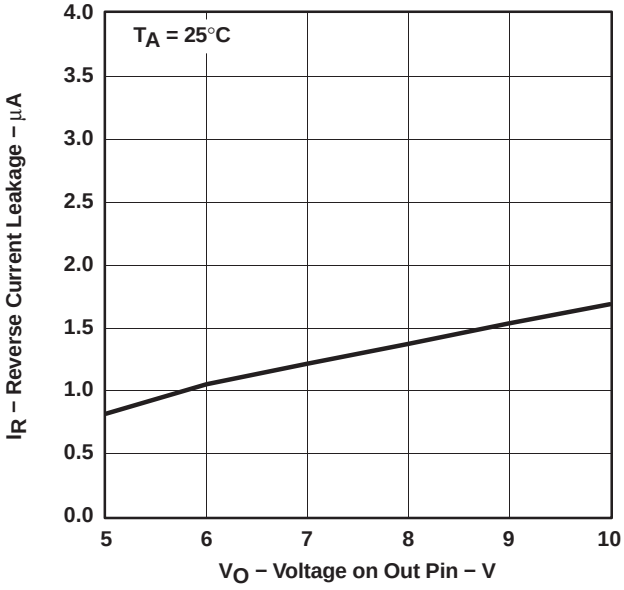


Figure 11

APPLICATION INFORMATION

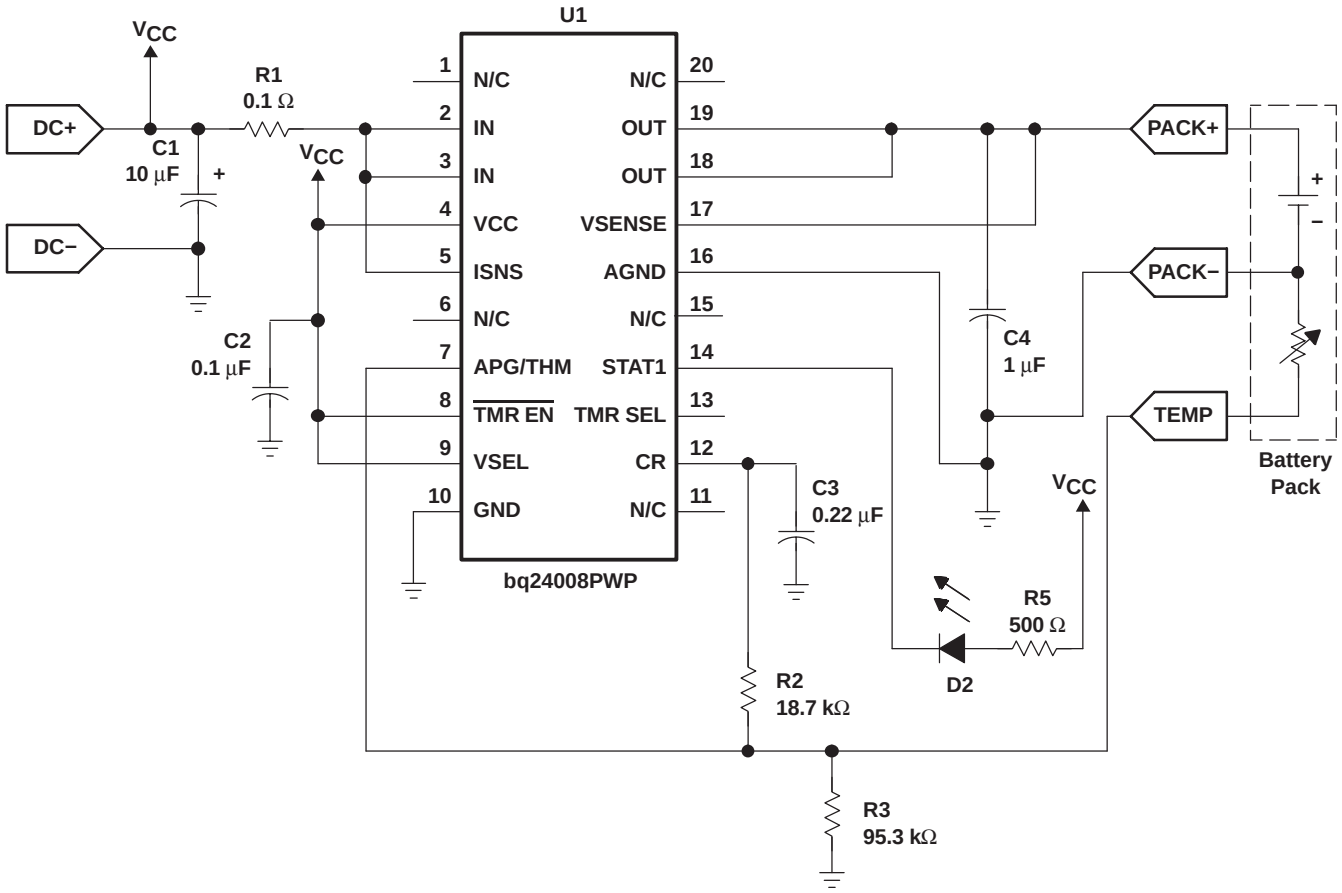


Figure 12. Single-Cell Li-Ion/Li-Pol Charger With Safety Timer Disabled

- If the TMR SEL pin is left floating (3 HR time), a 10-pF capacitor should be installed between TMR SEL and CR.
- If a micro process is monitoring the STAT pins, it may be necessary to add some hysteresis into the feedback to prevent the STAT pins from cycling while crossing the taper detect threshold (usually less than one half second). See SLUU083 EVM or SLUU113 EVM for additional resistors used for the STAT pins.

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The bq2400x supports a precision current- and voltage-regulated Li-Ion charging system suitable for cells with either coke or graphite anodes. See Figure 13 for a typical charge profile and Figures 14 and 15 for an operational flowchart.

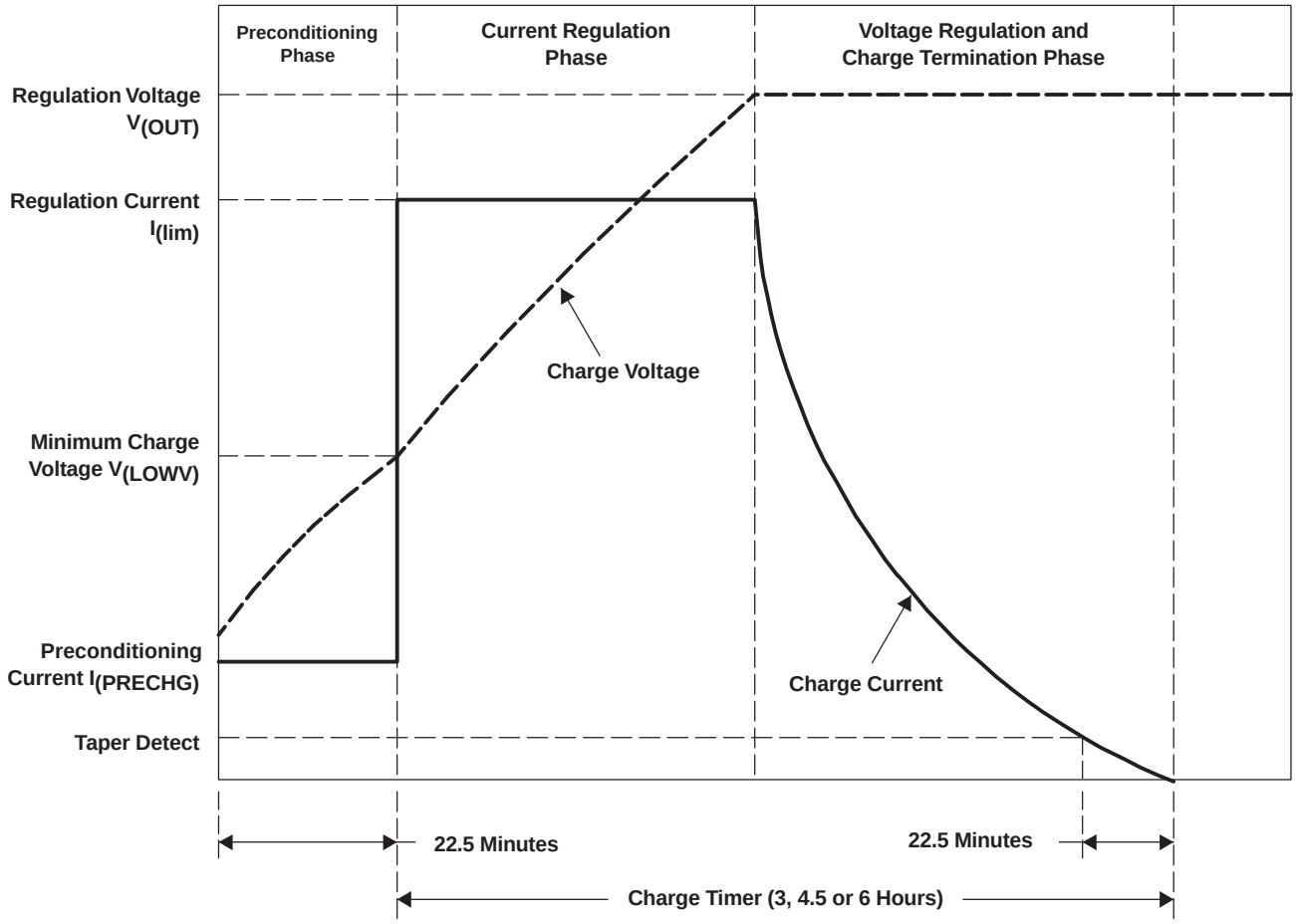


Figure 13. Typical Charge Profile

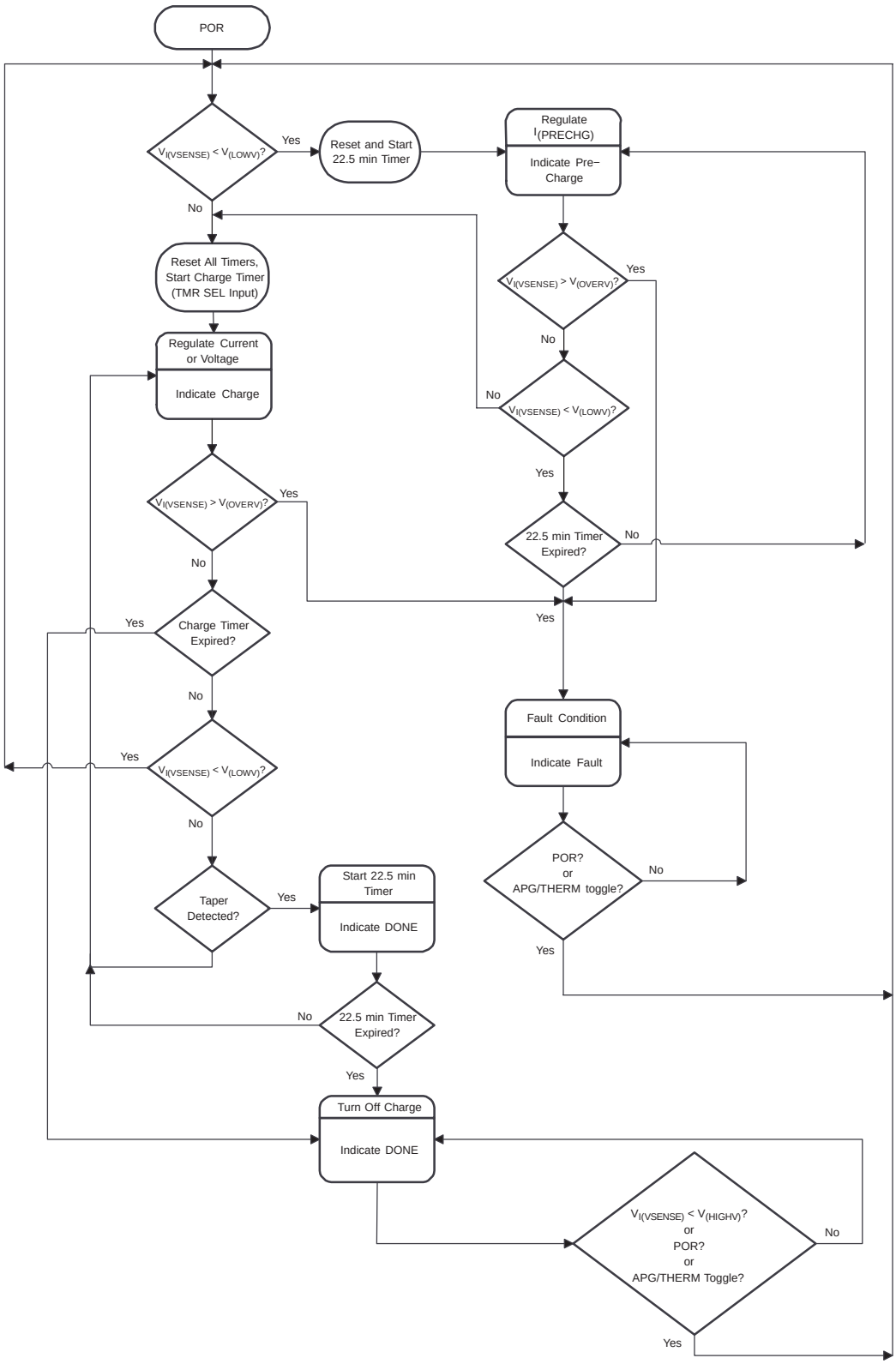


Figure 14. Operational Flow Chart With the Charge Termination Timers Enabled ($\overline{\text{TMR EN}}$ = 0)

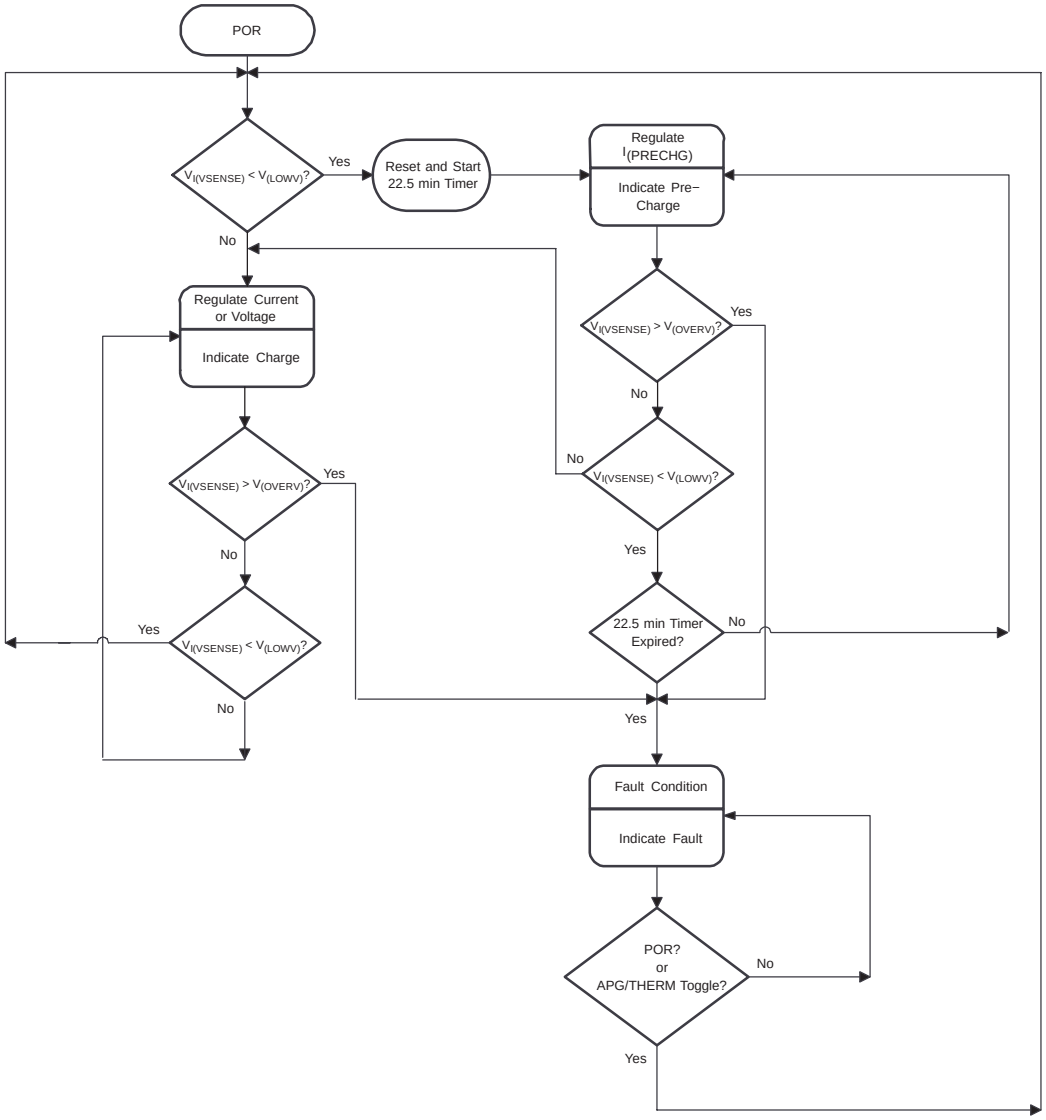


Figure 15. Operational Flow Chart With the Charge Timers Disabled ($\overline{\text{TMR EN}}$ = 1)

Charge Qualification and Preconditioning

The bq2400x starts a charge cycle when power is applied while a battery is present. Charge qualification is based on battery voltage and the APG/THERM input.

As shown in the block diagram, the internal LowV comparator output prevents fast-charging a deeply depleted battery. When set, charging current is provided by a dedicated precharge current source. The precharge timer limits the precharge duration. The precharge current also minimizes heat dissipation in the pass element during the initial stage of charge.

The APG/THERM input can also be configured to monitor either the adapter power or the battery temperature using a thermistor. The bq2400x suspends charge if this input is outside the limits set by the user. Please refer to the APG/THERM input section for additional details.

Timer Enable Function

The logic $\overline{\text{TRM EN}}$ enables or disables the charge safety timer. A low-level signal on this pin enables the timer (charge and taper). A high-level input disables the timers and allows the charger to operate continuously. No charge termination is provided when this input is high. Note that the preconditioning timer remains active regardless of the status of this input.

The $\overline{\text{TRM EN}}$ input can be changed any time during the charge cycle. A low-to-high transition on this pin resets the timers.

APG/THERM Input

The bq400x continuously monitors temperature or system input voltage by measuring the voltage between the APG/THERM (adapter power good/thermistor) and GND. For temperature, a negative- or a positive- temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage. (See Figure 16.) The bq2400x compares this voltage against its internal V_{TP1} and V_{TP2} thresholds to determine if charging is allowed. (See Figure 17.)

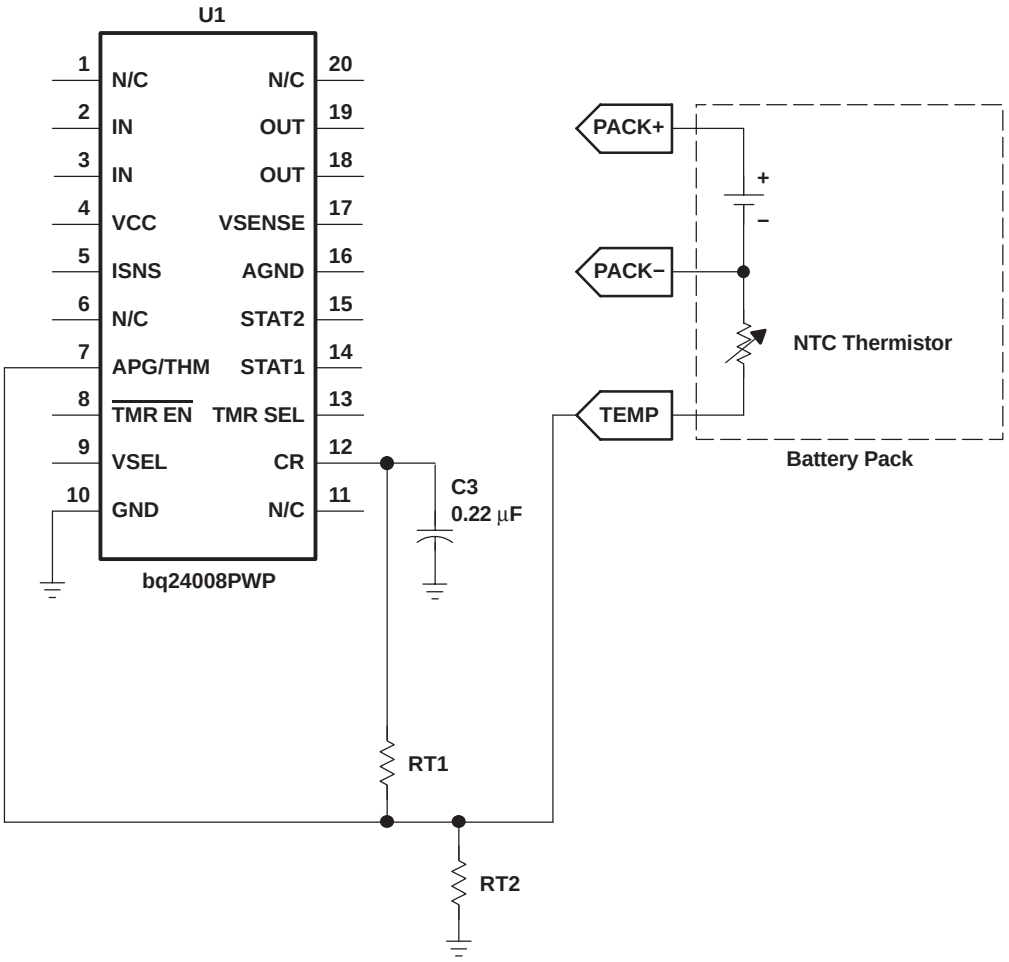


Figure 16. Temperature Sensing Circuit

If the charger designs incorporate a thermistor, the resistor divider RT1 and RT2 is calculated by using the following two equations.

First, calculate RT2.

$$RT2 = \frac{V_B R_H R_C \left[\frac{1}{V_C} - \frac{1}{V_H}\right]}{R_H \left(\frac{V_B}{V_H} - 1\right) - R_C \left(\frac{V_B}{V_C} - 1\right)}$$

then use the resistor value to find RT1.

$$RT1 = \frac{\frac{V_B}{V_C} - 1}{\frac{1}{RT2} + \frac{1}{R_C}}$$

Where:

$V_B = V_{CR}$ (bias voltage)

R_H = Resistance of the thermistor at the desired hot trip threshold

R_C = Resistance of the thermistor at the desired cold trip threshold

V_H = VP2 or the lower APG trip threshold

V_C = VP2 or the upper APG trip threshold

RT1 = Top resistor in the divider string

RT2 = Bottom resistor in the divider string

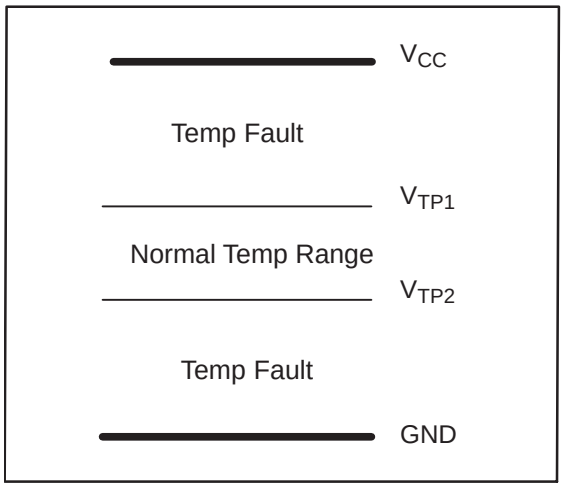


Figure 17. Temperature Threshold

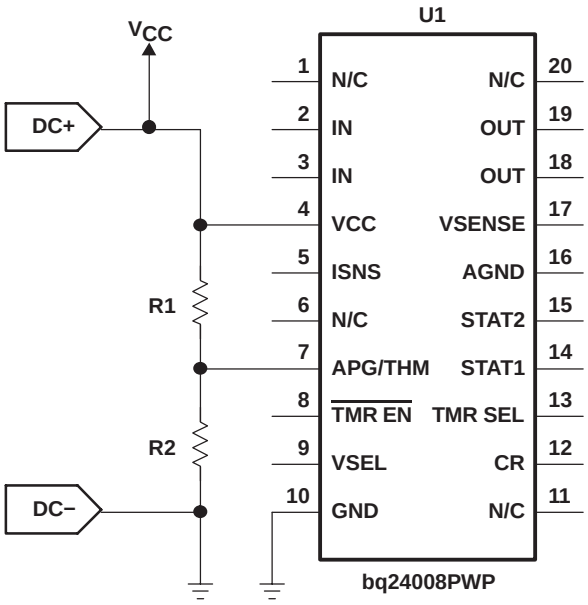


Figure 18. APG Sensing Circuit

Values of resistors R1 and R2 can be calculated using the following equation:

$$V_{(APG)} = V_{CC} \frac{R2}{(R1 + R2)}$$

where $V_{(APG)}$ is the voltage at the APG/THM pin.

Current Regulation

The bq2400x provides current regulation while the battery-pack voltage is less than the regulation voltage. The current regulation loop effectively amplifies the error between a reference signal, Vilim, and the drop across the external sense resistor, R_{SNS}.

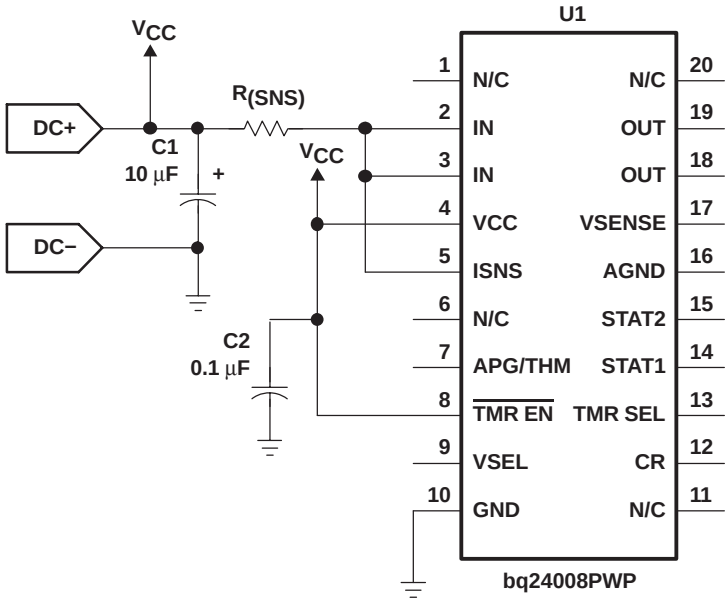


Figure 19. Current Sensing Circuit

Charge current feedback, applied through pin ISNS, maintains regulation around a threshold of Vilim. The following formula calculates the value of the sense resistor:

$$R_{(SNS)} = \frac{V_{(ilim)}}{I_{(REG)}}$$

where I_{REG} is the desired charging current.

Voltage Monitoring and Regulation

Voltage regulation feedback is through pin VSENSE. This input is tied directly to the positive side of the battery pack. The bq2400x supports cells with either coke (4.1 V) or graphite (4.2 V) anode. Pin VSEL selects the charge regulation voltage.

VSEL State (see Note)	CHARGE REGULATION VOLTAGE
Low	4.1 V
High	4.2 V

NOTE: VSEL should not be left floating.

Charge Termination

The bq2400x continues with the charge cycle until termination by one of the two possible termination conditions:

Maximum Charge Time: The bq2400x sets the maximum charge time through pin TMRSEL. The TMR SEL pin allows the user to select between three different total charge-time timers (3, 4, 5, or 6 hours). The charge timer is initiated after the preconditioning phase of the charge and is reset at the beginning of a new charge cycle. Note that in the case of a fault condition, such as an out-of-range signal on the APG/THERM input or a thermal shutdown, the bq2400x suspends the timer. Charge timers are active only when $\overline{\text{TMR EN}}$ input is low.

TMRSEL STATE	CHARGE TIME
Floating(1)	3 hours
Low	6 hours
High	4.5 hours

(1) To improve noise immunity, it is recommended that a minimum of 10 pF capacitor be tied to Vss on a floating pin.

Minimum Current: The bq2400x monitors the charging current during the voltage regulation phase. The bq2400x initiates a 22-minute timer once the current falls below the taperdet trip threshold. Fast charge is terminated once the 22-minute timer expires.

Charge Status Display

The two available options allow the user to configure the charge status display for single LED (bq24007) or a bicolor LED (bq24008). The output stage is totem pole for the bq24007 and bq24008. The following tables summarize the operation of the three options:

Table 1. bq24007 (Single LED)

CHARGE STATE	STAT1
Precharge	ON (LOW)
Fast charge	ON (LOW)
FAULT	Flashing (1 Hz, 50% duty cycle)
Done (>90%)	OFF (HIGH)
Sleep-mode	OFF (HIGH)
APG/Therm invalid	OFF (HIGH)
Thermal shutdown	OFF (HIGH)
Battery absent	OFF (HIGH)

Table 2. bq24008 (Single Bicolor LED)

CHARGE STATE	LED1 (RED)	LED2 (GREEN)	APPARENT COLOR
Precharge	ON (LOW)	OFF (HIGH)	RED
Fast charge	ON (LOW)	OFF (HIGH)	RED
FAULT	ON (LOW)	ON (LOW)	YELLOW
Done (>90%)	OFF (HIGH)	ON (LOW)	GREEN
Sleep-mode	OFF (HIGH)	OFF (HIGH)	OFF
APG/Therm invalid	OFF (HIGH)	OFF (HIGH)	OFF
Thermal shutdown	OFF (HIGH)	OFF (HIGH)	OFF
Battery absent	OFF (HIGH)	OFF (HIGH)(1)	OFF(1)

(1) If thermistor is used, then the green LED is off.

Thermal Shutdown

The bq2400x monitors the junction temperature T_J of the DIE and suspends charging if T_J exceeds 165°C. Charging resumes when T_J falls below 155°C.

DETAILED DESCRIPTION

POWER FET

The integrated transistor is a P-channel MOSFET. The power FET features a reverse-blocking Schottky diode, which prevents current flow from OUT to IN.

An internal thermal-sense circuit shuts off the power FET when the junction temperature rises to approximately 165°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 10°C, the power FET turns back on. The power FET continues to cycle off and on until the fault is removed.

CURRENT SENSE

The bq2400x regulates current by sensing, on the ISNS pin, the voltage drop developed across an external sense resistor. The sense resistor must be placed between the supply voltage (Vcc) and the input of the IC (IN pins).

VOLTAGE SENSE

To achieve maximum voltage regulation accuracy, the bq2400x uses the feedback on the VSENSE pin. Externally, this pin should be connected as close to the battery cell terminals as possible. For additional safety, a 10-kΩ internal pullup resistor is connected between the VSENSE and OUT pins.

TIMER ENABLE

The logic $\overline{\text{TMR EN}}$ enables or disables the charge safety timer. A low-level signal on this pin enables the timers. A high-level input disables the timers and allows the charge to operate continuously. No charge termination is provided when this input is high. Note that the preconditioning timer remains active regardless of the status of this input.

THERMAL INFORMATION

THERMALLY ENHANCED TSSOP-20

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad (see Figure 20) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

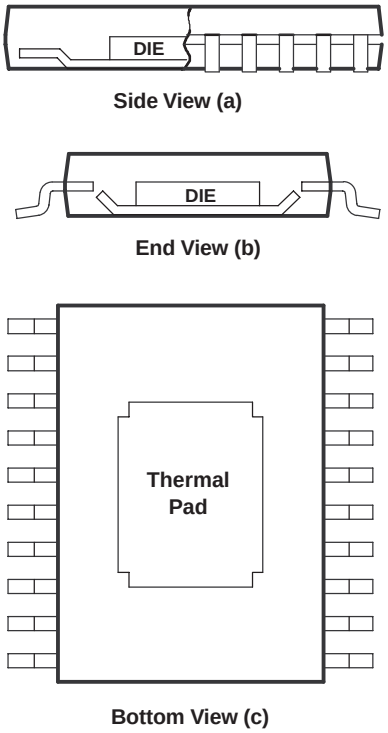


Figure 20. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air. (Reference Figure 22(a), 8 cm^2 of copper heat sink and natural convection.) Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly. (See Figure 22(b) and 22(c).) The line drawn at 0.3 cm^2 in Figures 21 and 22 indicates performance at the minimum recommended heat-sink size.

THERMAL INFORMATION

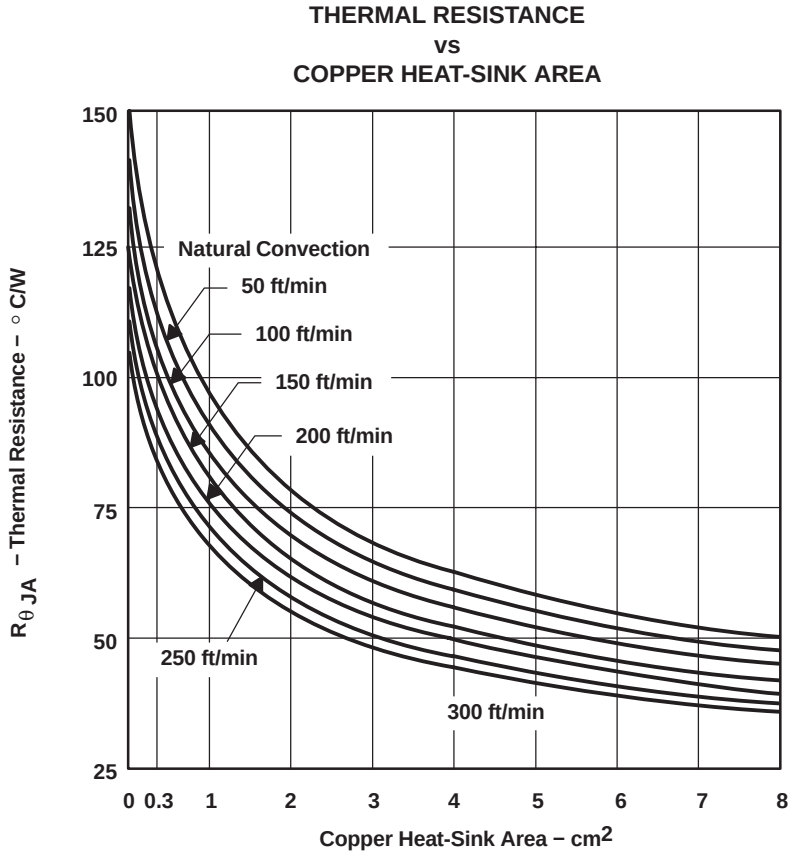


Figure 21

THERMAL INFORMATION

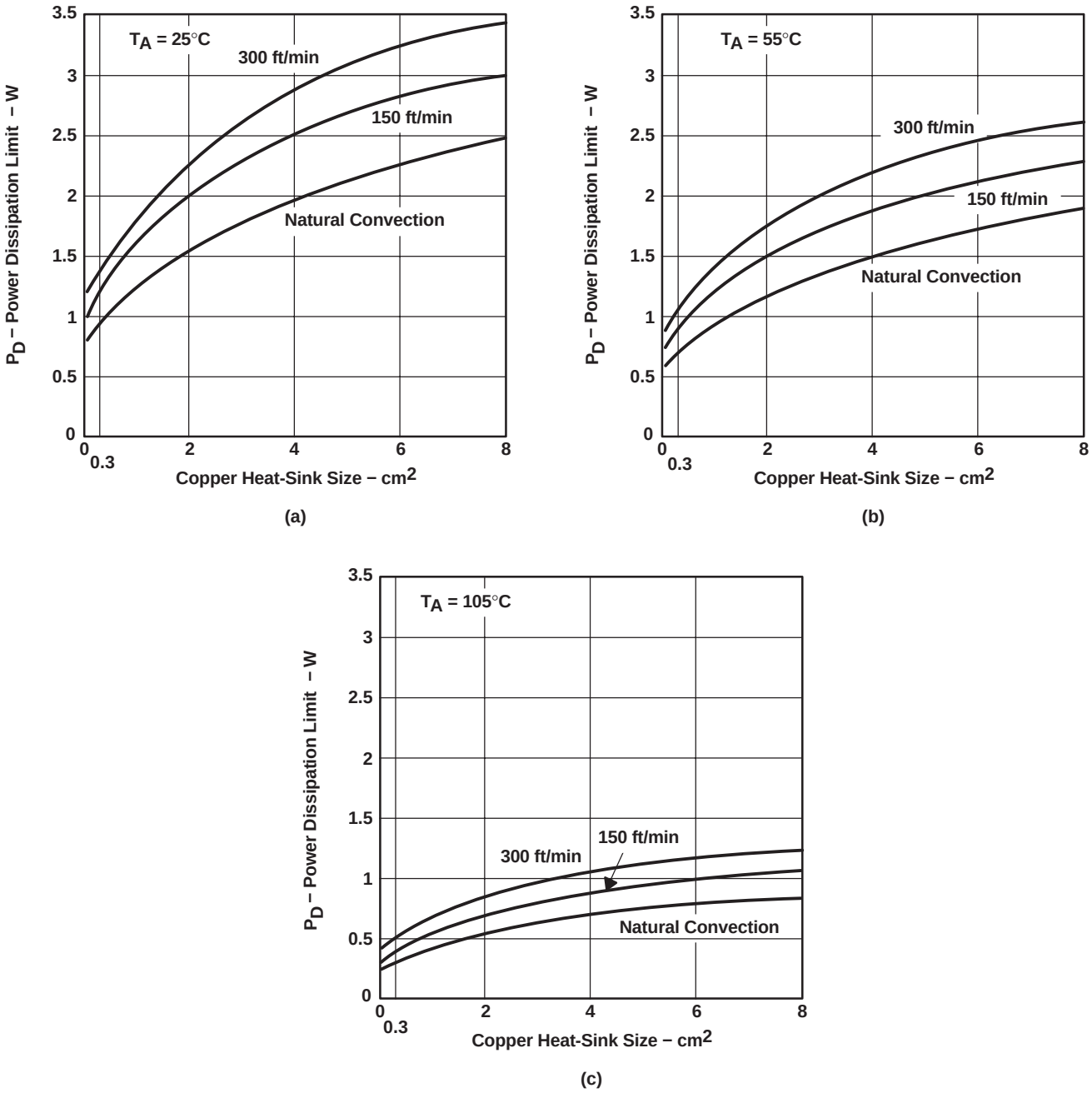


Figure 22. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24008PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24008
BQ24008PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24008
BQ24008PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24008
BQ24008PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24008

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

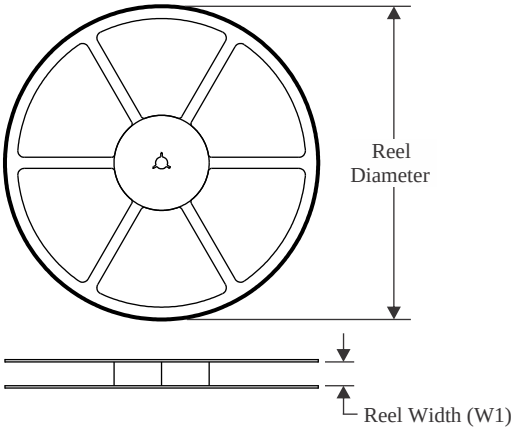
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

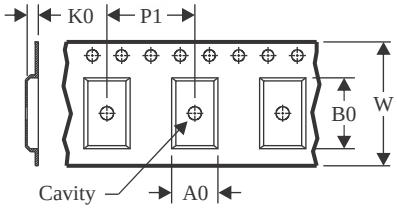
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

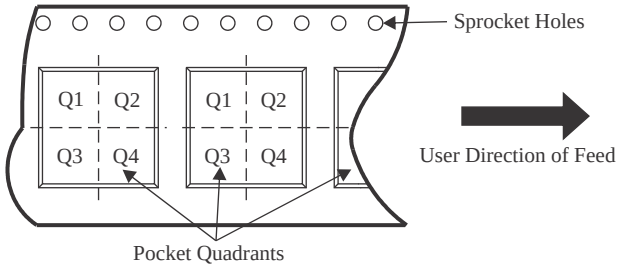


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

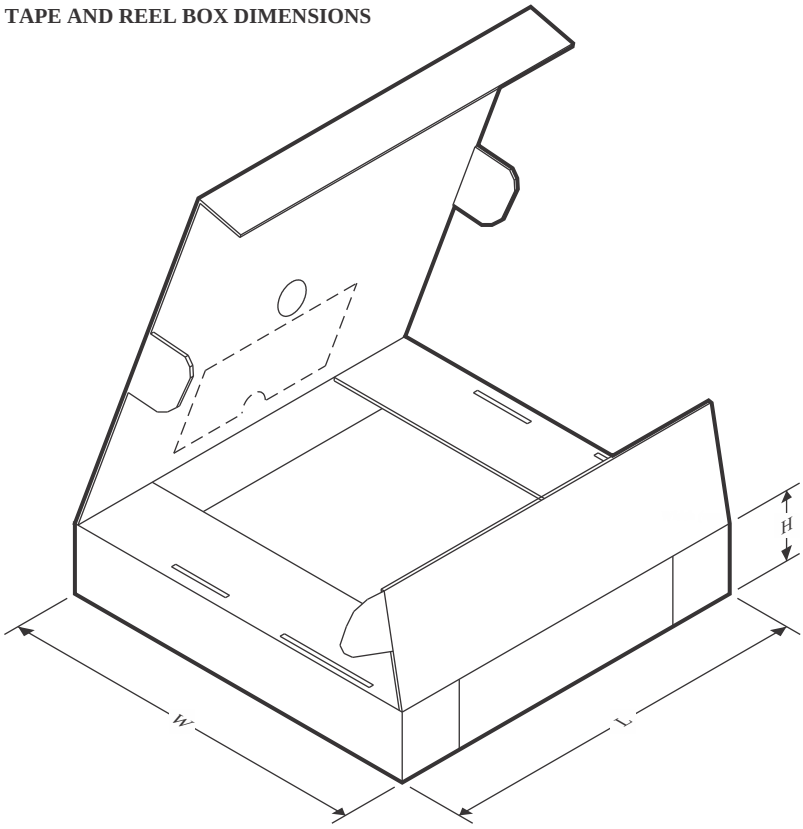
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24008PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

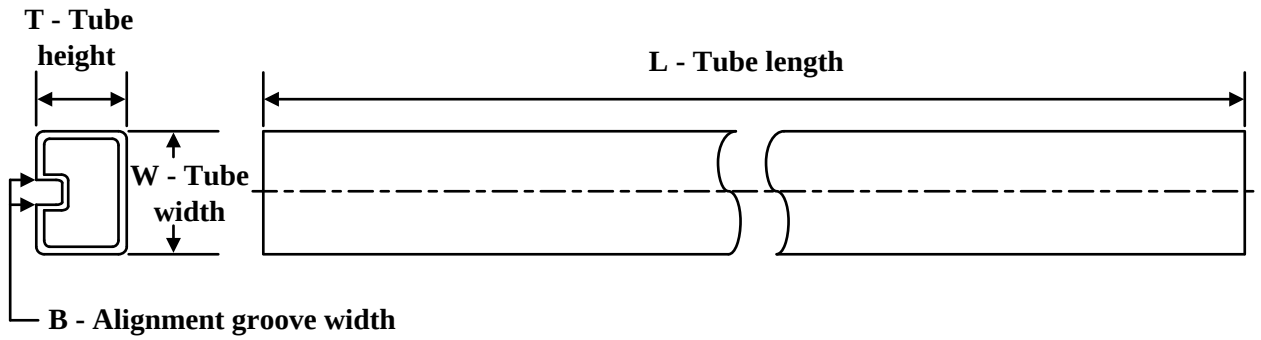
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24008PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ24008PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
BQ24008PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

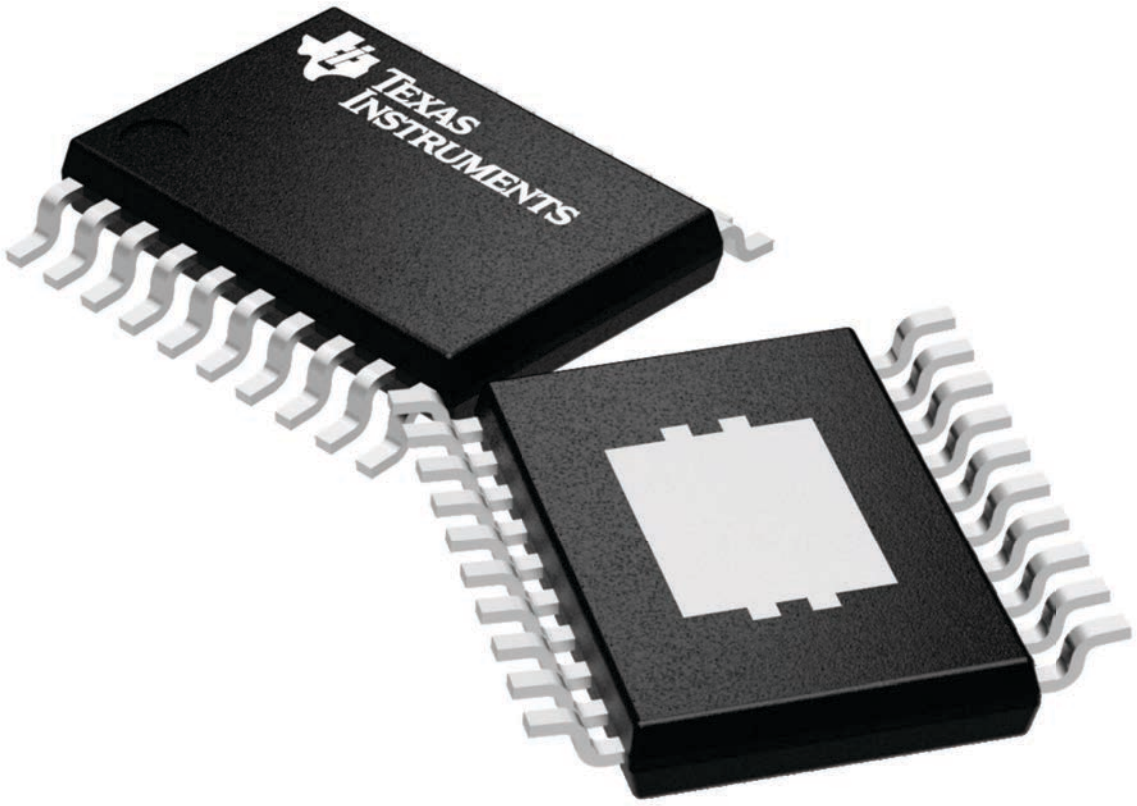
PWP 20

HTSSOP - 1.2 mm max height

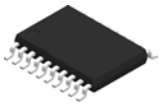
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

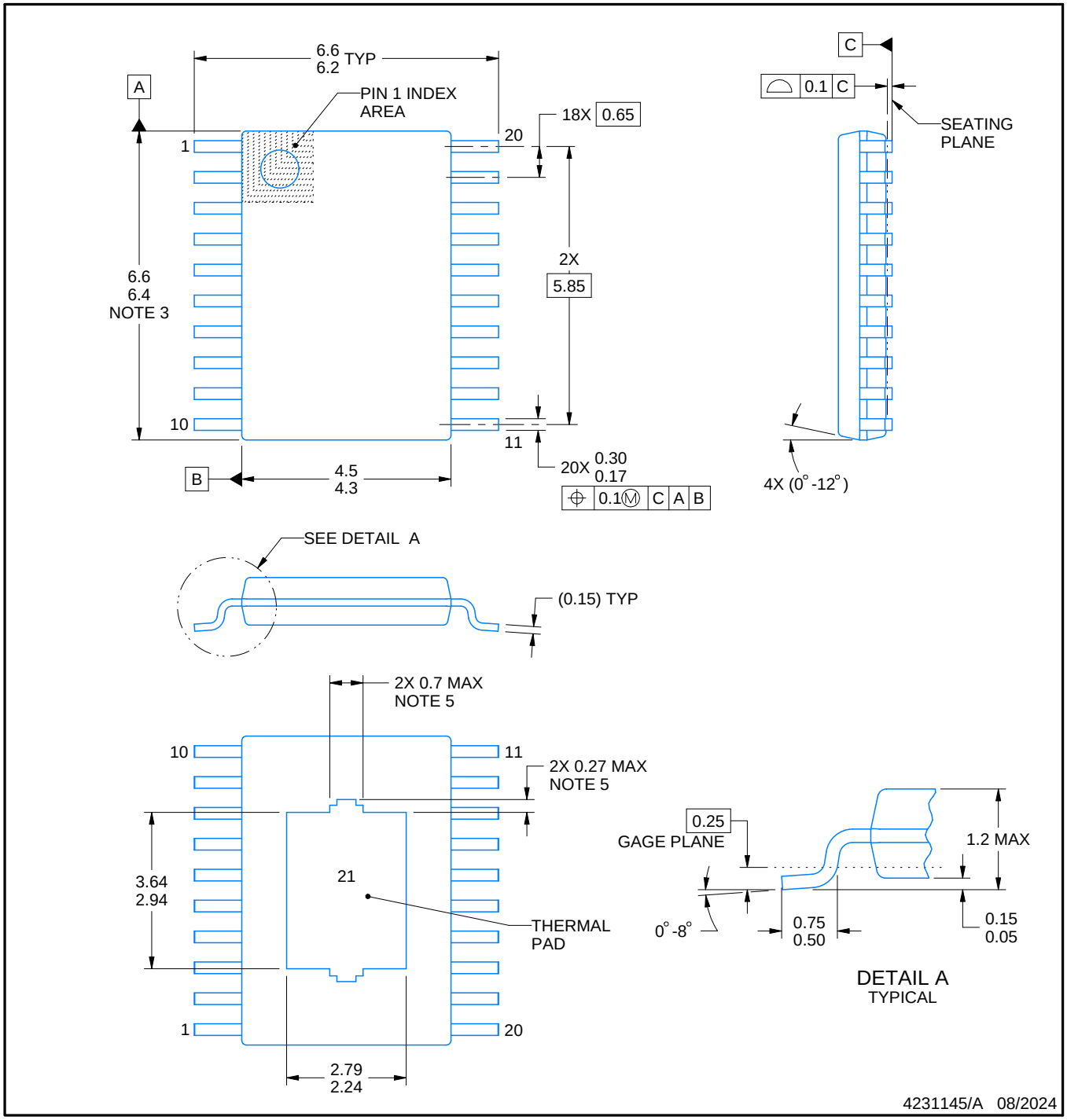


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

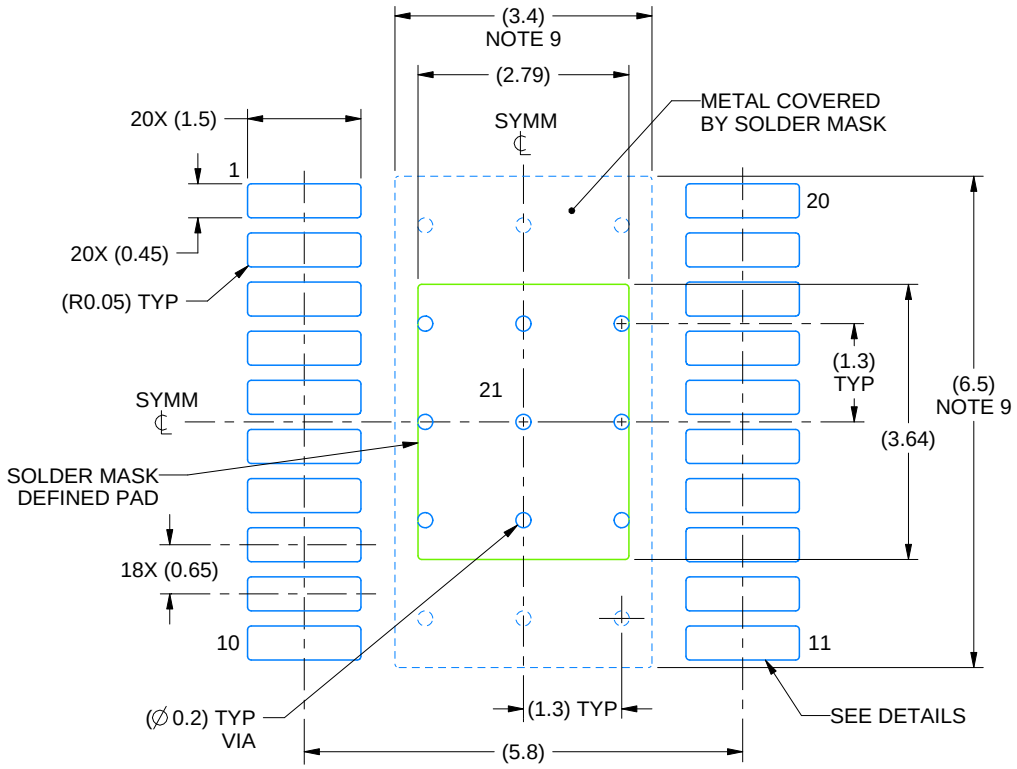
SMALL OUTLINE PACKAGE



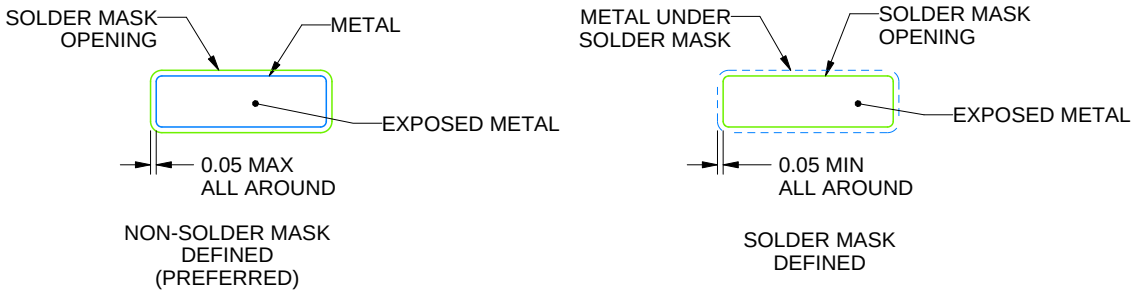
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

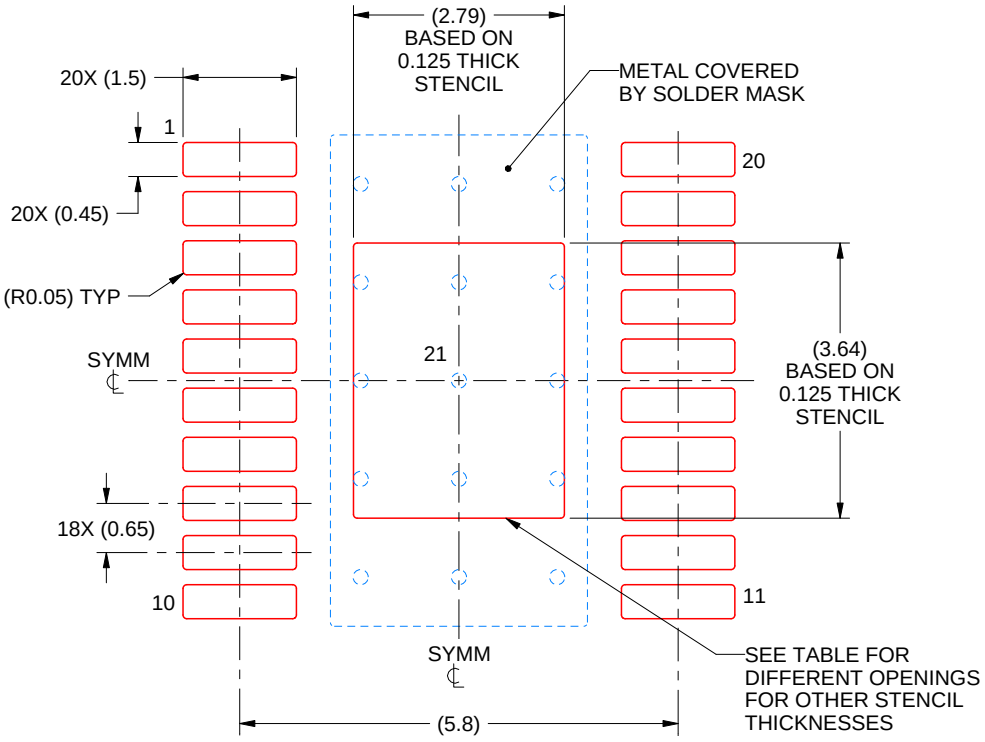


SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025

ENTEGRECİ

Bu belge www.entegreci.com üzerinden sunulmaktadır.

Elektronik komponent tedarikinde Entegreci

Entegreci, Eskişehir merkezli, Türkiye geneline satış yapan bir elektronik komponent mağazasıdır. Entegreler (IC), mikrodenetleyiciler, transistörler, diyotlar, pasif elemanlar, konnektörler, modüller ve geliştirme kartları tek adetten seri üretim adetlerine kadar satılır. Ürün sayfalarında güncel stok durumunu, fiyatı ve datasheet bağlantısını bulabilirsiniz.

Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

www.entegreci.com

Ürün kategorileri

Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

Üreticileri görün

Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

Teklif isteyin

www.entegreci.com | **destek@entegreci.com** | **0850 305 90 34**

Entegreci is an online electronic components store based in Türkiye. Search by manufacturer part number to see stock, prices and datasheets for integrated circuits, microcontrollers, transistors, passive components and connectors, or request a quote for parts that are not listed.

Bu sayfa Entegreci tarafından eklenmiştir. Belgenin önceki sayfaları asıl yayıncısına aittir ve içeriği değiştirilmemiştir; en güncel sürüm için belgenin yayıncısına başvurun.