BQ2057, BQ2057x Advanced Linear Charge Management ICs for Single- and Two-Cell Lithium-Ion and Lithium-Polymer

1 Features

- Ideal for single (4.1 V or 4.2 V) and dual-cell (8.2 V or 8.4 V) Li-ion or Li-pol packs
- Requires small number of external components
- 0.3-V dropout voltage for minimizing heat dissipation
- Better than ±1% voltage regulation accuracy with preset voltages
- AutoCompM dynamic compensation of battery pack's internal impedance to reduce charge time
- Optional cell-temperature monitoring before and during charge
- Integrated voltage and current regulation with programmable charge-current and high- or low-side current sensing
- Integrated cell conditioning for reviving deeply discharged cells and minimizing heat dissipation during initial stage of charge
- Charge status output for single or dual led or host processor interface
- Automatic battery-recharge feature
- Charge termination by minimum current
- Automatic low-power sleep mode when V_{CC} is removed
- EVMs available for quick evaluation
- Packaging: 8-pin SOIC, 8-pin TSSOP, 8-pin MSOP

2 Applications

- Emergency Call Systems, Telematics control unit
- Aftermarket Telematics
- Gaming and Computer Accessories
- Portable Medical Equipment
- EPOS Card Reader

3 Description

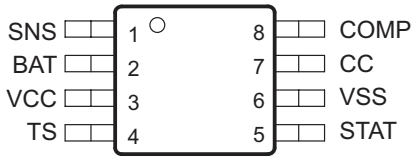
The BQ2057 series advanced lithium-ion (Li-ion) and lithium-polymer (Li-pol) linear charge-management ICs are designed for cost-sensitive and compact portable electronics. They combine high-accuracy current and voltage regulation, battery conditioning, temperature monitoring, charge termination, charge-status indication, and AutoComp™ charge-rate compensation in a single 8-pin IC. MSOP, TSSOP, and SOIC package options are offered to fit a wide range of end applications.

The BQ2057 continuously measures battery temperature using an external thermistor. For safety, the BQ2057 inhibits charge until the battery temperature is within user-defined thresholds. The BQ2057 then charges the battery in three phases: conditioning, constant current, and constant voltage. If the battery voltage is below the low-voltage threshold, $V_{(min)}$, the BQ2057 precharges using a low current to condition the battery. The conditioning charge rate is approximately 10% of the regulation current. The conditioning current also minimizes heat dissipation in the external pass-element during the initial stage of the charge. After conditioning, the BQ2057 applies a constant current to the battery. An external sense-resistor sets the current. The sense-resistor can be on either the high or low side of the battery without additional components. The constant-current phase continues until the battery reaches the charge-regulation voltage.

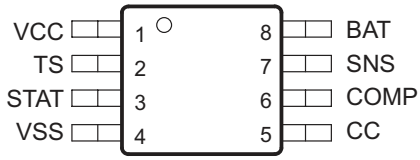
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
BQ2057C, BQ2057W	SOIC (8)	4.90 mm × 3.91 mm
BQ2057, BQ2057C, BQ2057T,BQ2057W	TSSOP (8)	3.00 mm × 4.40 mm
BQ2057, BQ2057C	MSOP (8)(2)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) Note the difference in pinout for this device.



BQ2057xSN or BQ2057xTS SOIC (SN) or TSSOP (TS) Package Top View



BQ2057xDGK MSOP DGK Package Top View

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2002) to Revision G (December 2022)	Page
• Added ESD Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
• Updated Device Comparison Table	4
• Added thermal information	5
• Added typical characteristics curves	8
• Added figure to Section 10.2	22
• Added design requirements	22
• Added application curves	23
• Added Layout Guidelines subsections	25
• Added layout example	26

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5 Description (continued)

The BQ2057 then begins the constant-voltage phase. The accuracy of the voltage regulation is better than ±1% over the operating-temperature and supply-voltage ranges. For single and dual cells, the BQ2057 is offered in four fixed-voltage versions: 4.1 V, 4.2 V, 8.2 V, and 8.4 V. Charge stops when the current tapers to the charge termination threshold, $I_{(TERM)}$. The BQ2057 automatically restarts the charge if the battery voltage falls below the $V_{(RCH)}$ threshold.

The designer also may use the AutoComp feature to reduce charging time. This proprietary technique allows safe and dynamic compensation for the internal impedance of the battery pack during charge.

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6 Device Comparison Table

T_A	PACKAGE			
	CHARGE REGULATION VOLTAGE	SOIC (SN)	TSSOP (TS)	MSOP(1) (DGK)
−20°C to 70°C	4.1 V	BQ2057SN	BQ2057TS	BQ2057DGK
	4.2 V	BQ2057CSN	BQ2057CTS	BQ2057CDGK
	8.2 V	BQ2057TSN	BQ2057TTS	Not available
	8.4 V	BQ2057WSN	BQ2057WTS	

(1) Note the difference in pinout for this package.

7 Pin Configuration and Functions

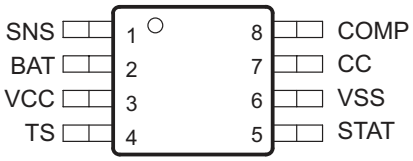

Figure 7-1. BQ2057xSN or BQ2057xTS SOIC (SN) or TSSOP (TS) Package Top View

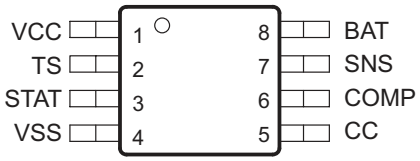

Figure 7-2. BQ2057xDGK MSOP DGK Package Top View

Table 7-1. Pin Functions-

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOIC (SN) and TSSOP (TS)	MSOP (DGK)		
BAT	2	8	I	Voltage sense input
CC	7	5	O	Charge control output
COMP	8	6	I	Charge-rate compensation input (AutoComp)
SNS	1	7	I	Current sense input
STAT	5	3	O	Charge status output
TS	4	2	I	Temperature sense input
VCC	3	1	I	Supply voltage
VSS	6	4	-	Ground

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltage (V_{CC} with respect to GND)	−0.3	18	V
	Input voltage, SNS, BAT, TS, COMP (all with respect to GND)	−0.3	V_{CC}+0.3	V
	Sink current (STAT pin) not to exceed P_D		20	mA
	Source current (STAT pin) not to exceed P_D		10	mA
	Output current (CC pin) not to exceed P_D		40	mA
P_D	Total power dissipation (at 25°C)		300	mW
T_A	Operating free-air temperature range	–20	70	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5		15	V
T_A	Operating free-air temperature range	–20		70	°C

8.4 Thermal Information

THERMAL METRIC(1)		BQ2057xSN or BQ2057xTS SOIC (SN) or TSSOP (TS) PACKAGE 8 PINS	BQ2057xDGK MSOP DGK PACKAGE 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.1	121.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.5	58.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.6	65.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87.4	65.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(VCC)}$	V_{CC} Current	$V_{CC} > V_{CC(min)}$, Excluding external loads		2	4	mA
$I_{(VCCS)}$	V_{CC} Sleep current	For BQ2057 and BQ2957C, $V_{(BAT)} \geq V(min)$, V(BAT) – VCC ≥ 0.8 V		3	6	µA
		For BQ2057T and BQ2957W, V(BAT) ≥ $V_{(min)}$, $V_{(BAT)} - V_{CC} \geq 0.8$ V			10	
$I_{IB(BAT)}$	Input bias current on BAT pin	$V_{(BAT)} = V_{(REG)}$			1	µA
$I_{IB(SNS)}$	Input bias current on SNS pin	$V_{(SNS)}$ = 5 V			5	µA
$I_{IB(TS)}$	Input bias current on TS pin	$V_{(TS)}$ = 5 V			5	µA
$I_{IB(COMP)}$	Input bias current on COMP pin	$V_{(COMP)}$ = 5 V			5	µA
BATTERY VOLTAGE REGULATION						
$V_{O(REG)}$	Output voltage	BQ2057, See (1) (2) (3)	4.059	4.10	4.141	V
		BQ2057C, See (1) (2) (3)	4.158	4.20	4.242	
		BQ2057T, See (1) (2) (3)	8.119	8.20	8.282	
		BQ2057W, See (1) (2) (3)	8.317	8.40	8.484	
CURRENT REGULATION						
$V_{(SNS)}$	Current regulation threshold	BQ2057 and BQ2057C, High-side current sensing configuration	95.4	105	115.5	mV
		BQ2057T and BQ2057W, High-side current sensing configuration	103.6	125	137.5	
		BQ2057 and BQ2057C, Low-side current sensing configuration	100	110	121	
		BQ2057T and BQ2057W, Low-side current sensing configuration	108.1	130	143	
CHARGE TERMINATION DETECTION						
$I_{(TERM)}$	Charge termination current detect threshold	Voltage at pin SNS, relative to V_{CC} for high-side sensing, and to V_{SS} for low-side sensing, 0°C ≤ T_A ≤ 50°C	−30	−14	−4	mV
TEMPERATURE COMPARATOR						
$V_{(TS1)}$	Lower temperature threshold	TS pin voltage	29.1	30	30.9	%VCC
$V_{(TS2)}$	Upper temperature threshold		58.3	60	61.8	
PRECHARGE COMPARATOR						
$V_{(min)}$	Precharge threshold	BQ2057	2.94	3	3.06	V
		BQ2057C	3.04	3.1	3.16	
		BQ2057T	5.9	6.1	6.22	
		BQ2057W	6.18	6.3	6.43	
PRECHARGE CURRENT REGULATION						
$I_{(PRECHG)}$	Precharge current regulation	Voltage at pin SNS, relative to V_{CC} for high-side sensing, and to V_{SS} for low-side sensing, 0°C ≤ T_A ≤ 50°C		13		mV
		Voltage at pin SNS, relative to VCC for high-side sensing, 0°C ≤ T_A ≤ 50°C, V_{CC} = 5 V	3	13	22	mV
V_{RCH} COMPARATOR (Battery Recharge Threshold)						
$V_{(RCH)}$	Recharge threshold	BQ2057 and BQ2057C	$V_{O(REG)}$− 98 mV	$V_{O(REG)}$− 100 mV	$V_{O(REG)}$− 102 mV	V
		BQ2057T and BQ2057W	$V_{O(REG)}$− 196 mV	$V_{O(REG)}$− 200 mV	$V_{O(REG)}$− 204 mV	V
CHARGE-RATE COMPENSATION (AutoComp)						
$G_{(COMP)}$	AutoComp gain	$V_{(BAT)}$+0.3 V≤ $V_{CC} \leq V_{CC(max)}$, BQ2057, BQ2057C, BQ2057T, BQ2057W	1.87	2.2	2.53	V/V
		$V_{(BAT)}$+0.3 V ≤ $V_{CC} \leq V_{CC(max)}$, BQ2057T and BQ2057W in low-side sensing configuration	2.09	2.4	2.76	
STAT PIN						

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8.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL(STAT)}$	Output (low) voltage	I_{OL} = 10 mA			0.7	V
$V_{OH(STAT)}$	Output (high) voltage	I_{OH} = 5 mA	V_{CC}–0.5			
CC PIN						
$V_{OL(CC)}$	Output low voltage	$I_{O(CC)}$ = 5 mA (sink)			1.5	V
$I_{O(CC)}$	Sink current	Not to exceed power rating specification (P_D)	5		40	mA

(1) For high-side current sensing configuration.
(2) For low-side current sensing configuration, the tolerance is ±1% for T_A = 25°C and ±1.2% for −20°C ≥ T_A ≥ 70°C.
(3) $V_{(BAT)}$+0.3 V ≤ V_{CC} ≤ $V_{CC(max)}$

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8.6 Typical Characteristics

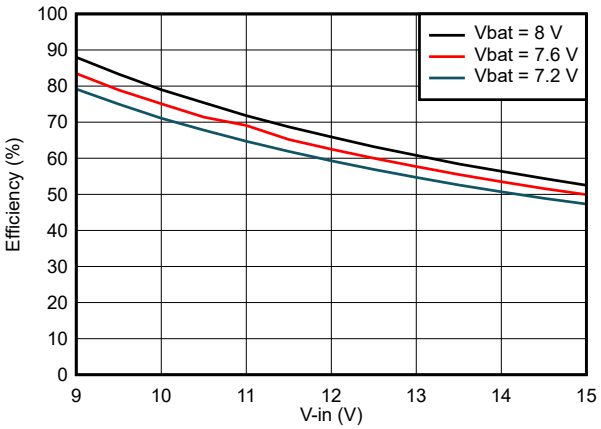

Figure 8-1.

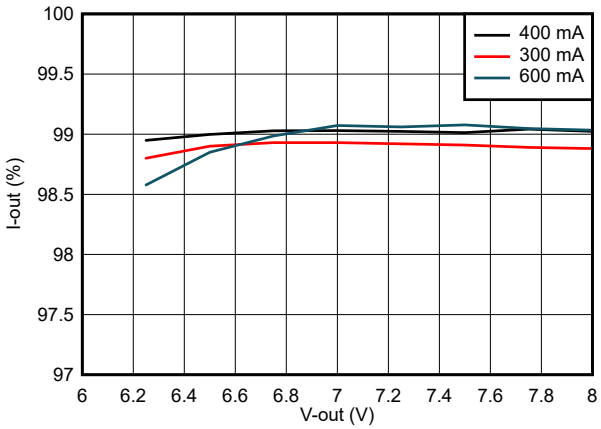

Figure 8-2.

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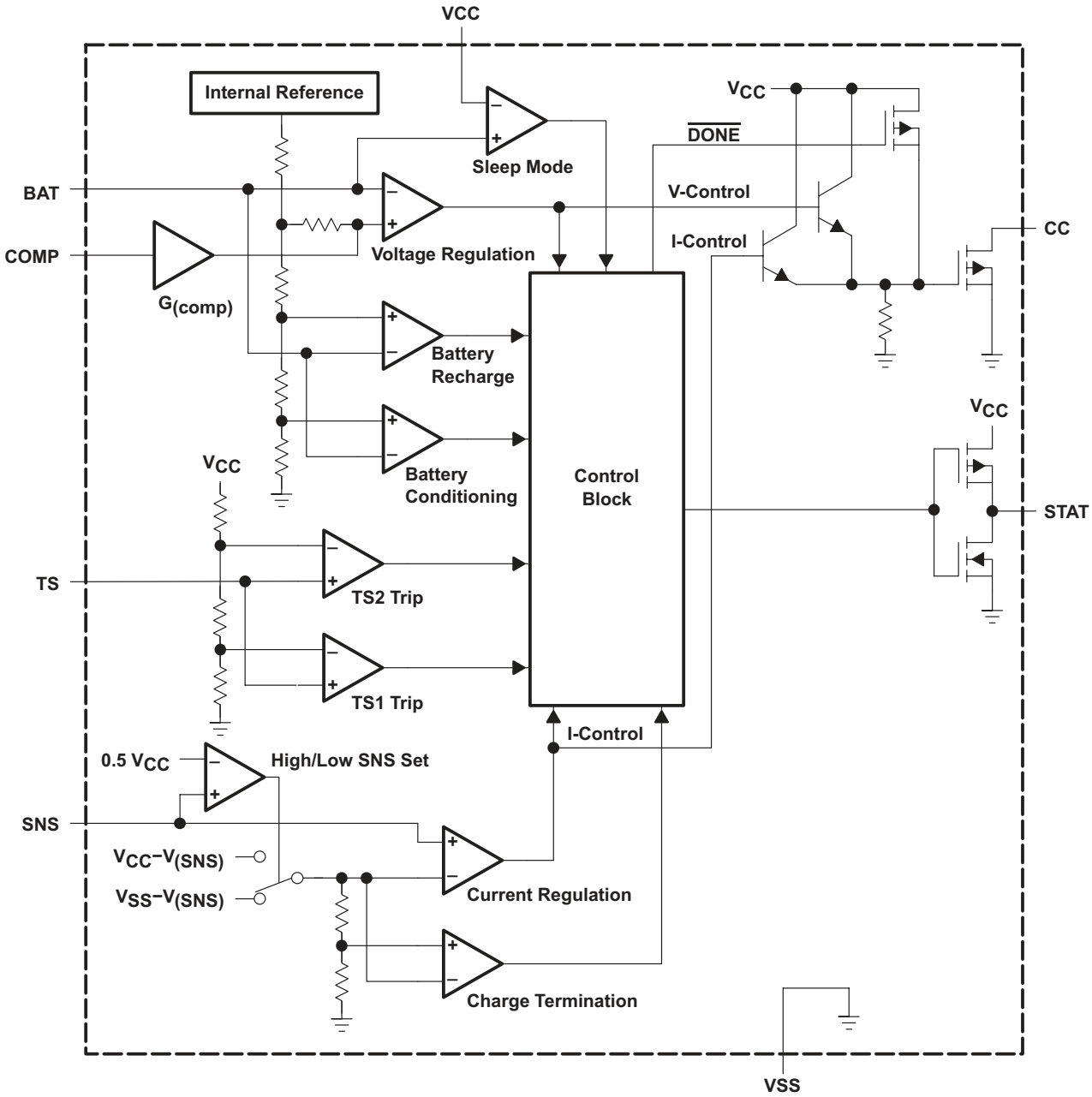
9 Detailed Description

9.1 Overview

Descriptions of the devices are presented in the following sections.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Current-Sense Input

Battery current is sensed via the voltage developed on this pin by an external sense resistor. The external resistor can be placed on either the high or low side of the battery. (See schematics for details.)

9.3.2 Battery-Voltage Input

Voltage sense-input tied directly to the positive side of the battery.

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9.3.3 Temperature Sense Input

Input for an external battery-temperature monitoring circuit. Connecting this input to VCC/2 disables this feature.

9.3.4 Charge-status Output

Three-state indication of charge in progress, charge complete, and temperature fault or sleep mode.

9.3.5 Charge-Control Output

Source-follower output that drives an external pass-transistor (PNP or P-channel MOSFET) for current and voltage regulation.

9.3.6 Charge-Rate Compensation Input

Sets the charge-rate compensation level. The voltage-regulation output may be programmed to vary as a function of the charge current delivered to the battery.

9.3.7 Supply Voltage Input

Power supply input and current reference for high-side sensing configuration.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Functional Description

The BQ2057 is an advanced linear charge controller for single or two-cell Li-Ion or Li-Pol applications. Figure 10-1 shows the schematic of charger using a PNP pass transistor. Figure 10-2 is an operational state diagram, and Figure 10-3 is a typical charge profile. Figure 10-4 shows the schematic of a charger using P-channel MOSFET.

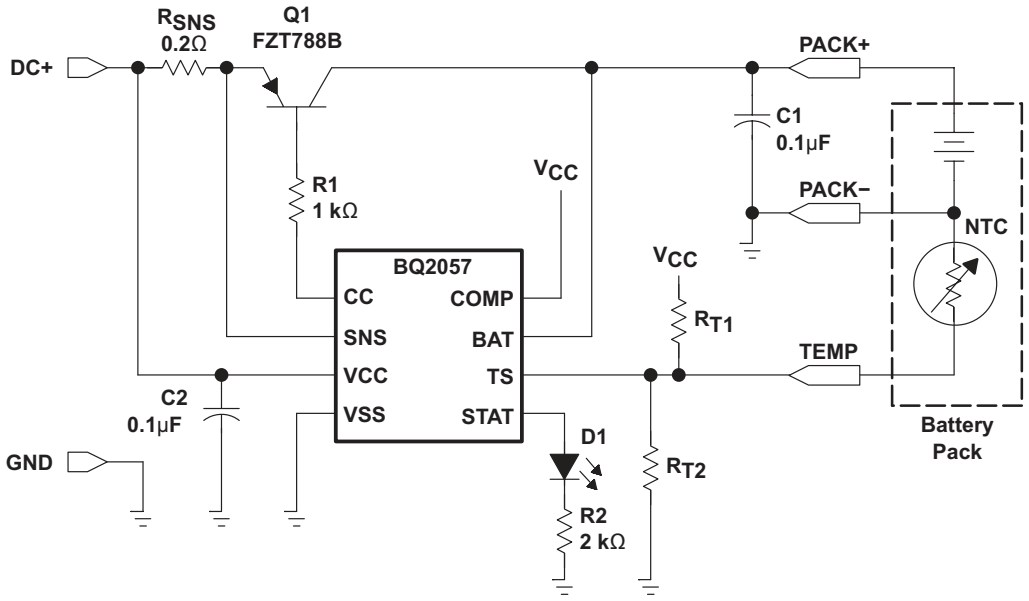

Figure 10-1. Low Dropout Single- or Two-Cell Li-Ion/Li-Pol Charger

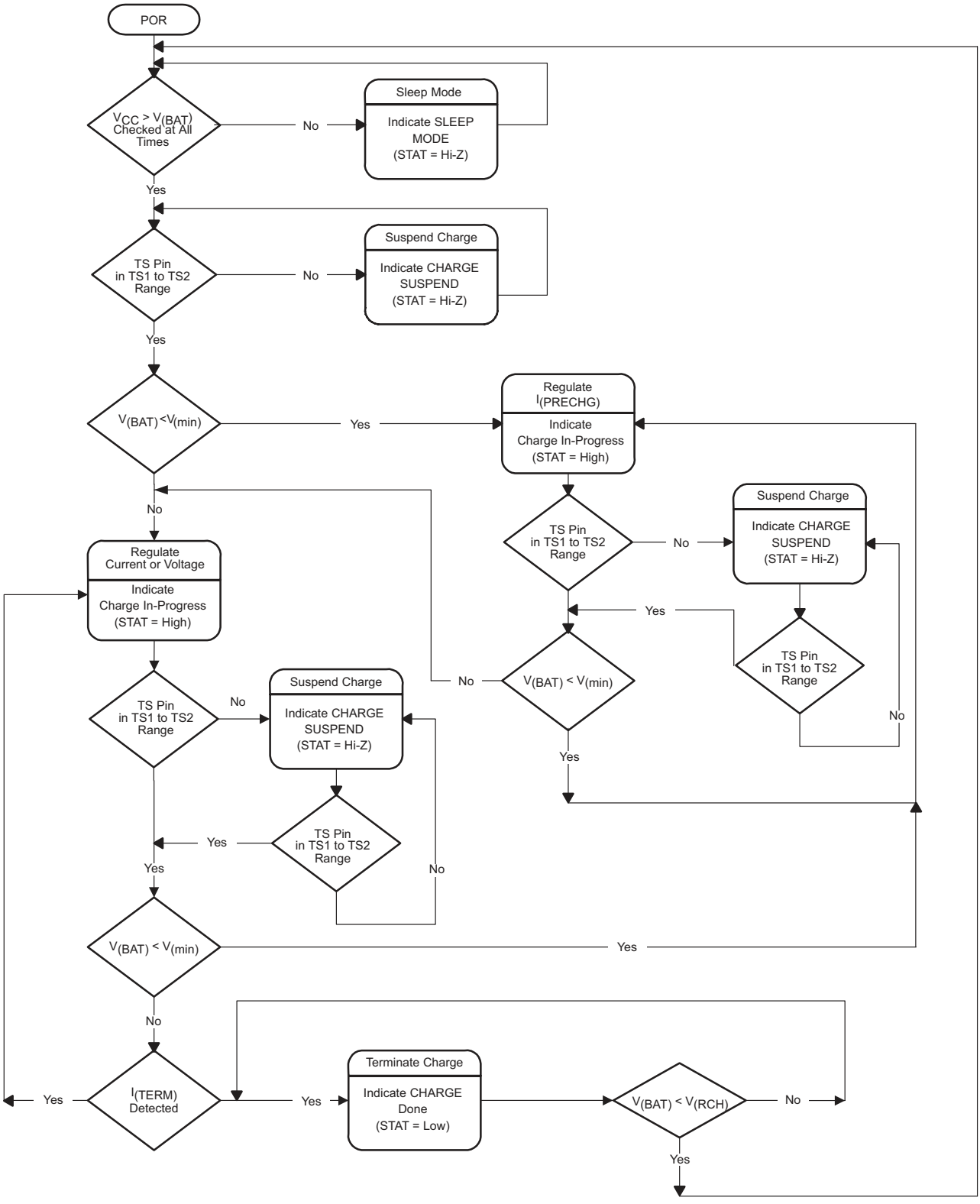

Figure 10-2. Operation Flowchart

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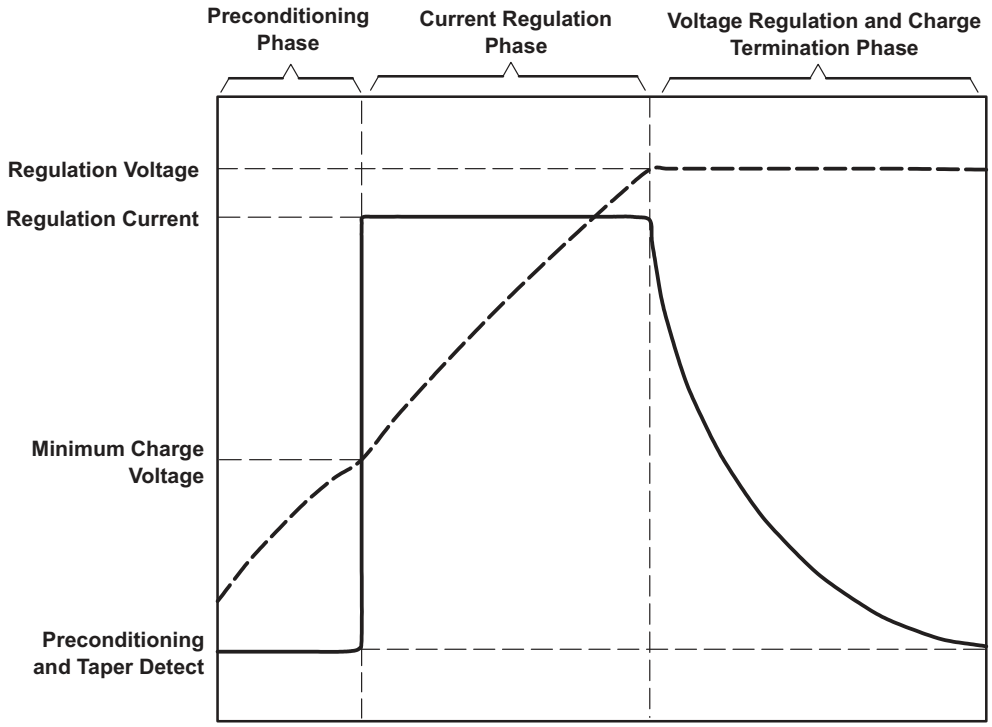

Figure 10-3. Typical Charge Profile

10.1.2 Qualification and Precharge

When power is applied, the BQ2057 starts a charge-cycle if a battery is already present or when a battery is inserted. Charge qualification is based on battery temperature and voltage. The BQ2057 suspends charge if the battery temperature is outside the $V_{(TS1)}$ to $V_{(TS2)}$ range and suspends charge until the battery temperature is within the allowed range. The BQ2057 also checks the battery voltage. If the battery voltage is below the precharge threshold $V_{(min)}$, the BQ2057 uses precharge to condition the battery. The conditioning charge rate $I_{(PRECHG)}$ is set at approximately 10% of the regulation current. The conditioning current also minimizes heat dissipation in the external pass-element during the initial stage of charge. See Figure 10-3 for a typical charge-profile.

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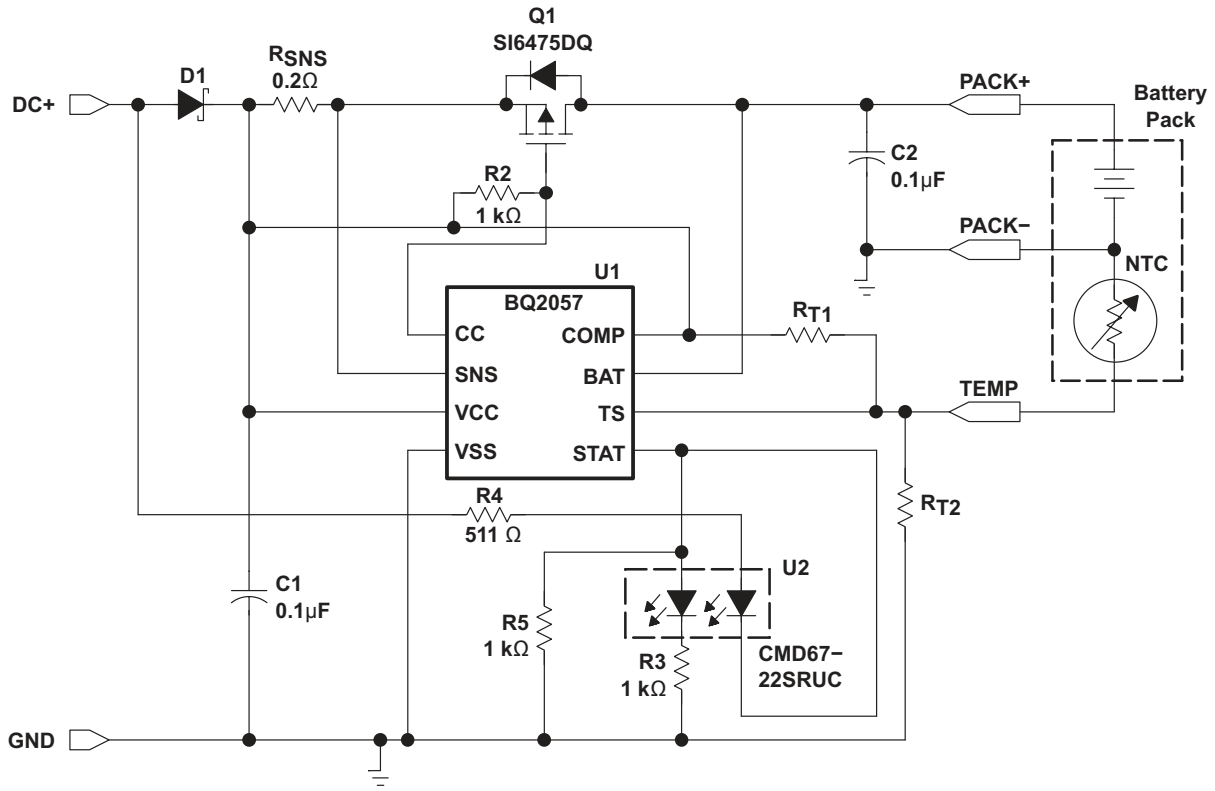

Figure 10-4. 0.5-A Charger Using P-Channel MOSFET

10.1.3 Current Regulation Phase

The BQ2057 regulates current while the battery-pack voltage is less than the regulation voltage, $V_{O(REG)}$. The BQ2057 monitors charge current at the SNS input by the voltage drop across a sense-resistor, R_{SNS}, in series with the battery pack. In high-side current sensing configuration (see Figure 10-5), R_{SNS} is between the VCC and SNS pins, and in low-side sensing (see Figure 10-6) the R_{SNS} is between VSS (battery negative) and SNS (charger ground) pins. Charge-current feedback, applied through pin SNS, maintains a voltage of $V_{(SNS)}$ across the current sense resistor. Equation 1 calculates the value of the sense resistor:

$$R_{SNS} = \frac{V_{(SNS)}}{I_{O(REG)}} \quad (1)$$

Where $I_{O(REG)}$ is the desired charging current.

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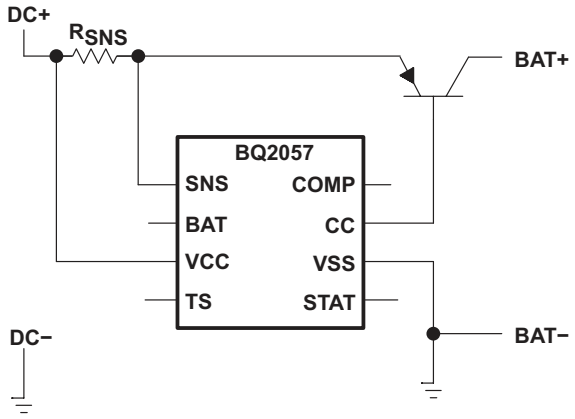

Figure 10-5. High-Side Current Sensing

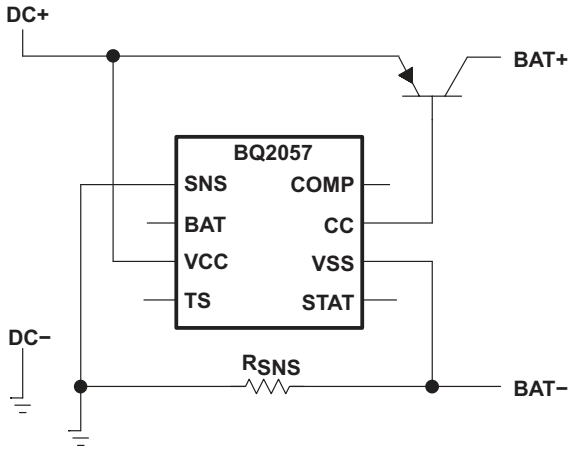

Figure 10-6. Low-Side Current Sensing

10.1.4 Voltage Regulation Phase

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The BQ2057 monitors the battery-pack voltage between the BAT and VSS pins. The BQ2057 is offered in four fixed-voltage versions: 4.1 V, 4.2 V, 8.2 V, and 8.4 V.

Other regulation voltages can be achieved by adding a voltage divider between the positive and negative terminals of the battery pack and using BQ2057T or BQ2057W. The voltage divider presents scaled battery-pack voltage to BAT input. (See Figure 10-7 and Figure 10-8.) The resistor values RB1 and RB2 for the voltage divider are calculated by the following equation:

$$\frac{R_{B1}}{R_{B2}} = \left(N \times \frac{V_{(CELL)}}{V_{O(REG)}} \right) - 1 \quad (2)$$

Where:

N = Number of cells in series
$V_{(CELL)}$ = Desired regulation voltage per cell

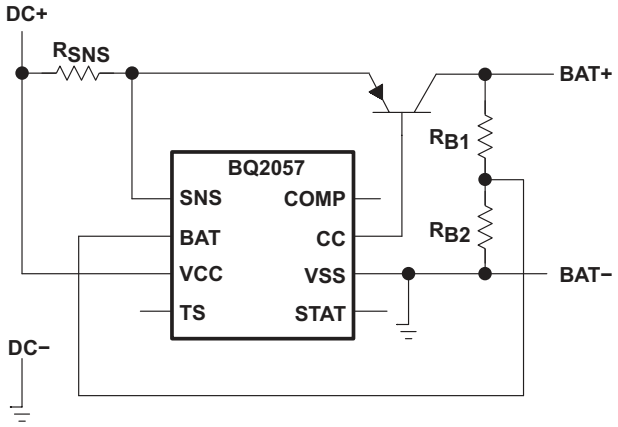

Figure 10-7. Optional Voltage Divider for Nonstandard Regulation Voltage, (High-Side Current Sensing)

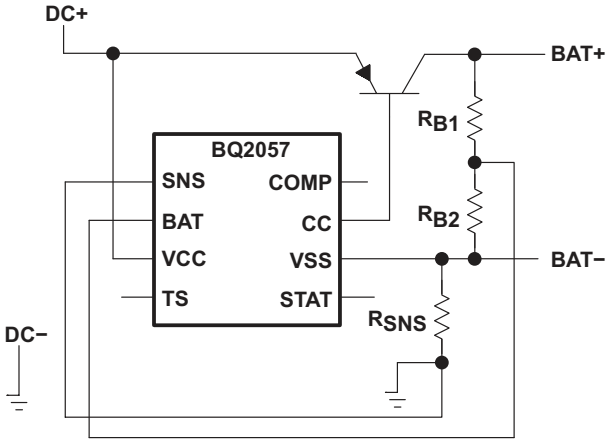

Figure 10-8. Optional Voltage Divider for Nonstandard Regulation Voltage, (Low-Side Current Sensing)

10.1.5 Charge Termination and Recharge

The BQ2057 monitors the charging current during the voltage-regulation phase. The BQ2057 declares a done condition and terminates charge when the current tapers off to the charge termination threshold, $I_{(TERM)}$. A new charge cycle begins when the battery voltage falls below the $V_{(RCH)}$ threshold.

10.1.6 Battery Temperature Monitoring

The BQ2057 continuously monitors temperature by measuring the voltage between the TS and VSS pins. A negative- or a positive-temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage. (See Figure 10-9.) The BQ2057 compares this voltage against its internal V(TS1) and V(TS2) thresholds to determine if charging is allowed. (See Figure 10-10.) The temperature sensing circuit is immune to any fluctuation in V_{CC}, since both the external voltage divider and the internal thresholds ($V_{(TS1)}$ and $V_{(TS2)}$) are referenced to VCC.

The resistor values of $R_{(T1)}$ and $R_{(T2)}$ are calculated by the following equations:

For NTC Thermistors

$$R_{T1} = \frac{5 \times R_{TH} \times R_{TC}}{3 \times (R_{TC} - R_{TH})} \quad (3)$$

$$R_{T1} = \frac{5 \times R_{TH} \times R_{TC}}{3 \times (R_{TC} - R_{TH})} \quad (4)$$

For PTC Thermistors

$$R_{T1} = \frac{5 \times R_{TH} \times R_{TC}}{3 \times (R_{TH} - R_{TC})} \quad (5)$$

$$R_{T2} = \frac{5 \times R_{TH} \times R_{TC}}{\left[(2 \times R_{TH}) - (7 \times R_{TC})\right]} \quad (6)$$

Where $R_{(TC)}$ is the cold temperature resistance and $R_{(TH)}$ is the hot temperature resistance of thermistor, as specified by the thermistor manufacturer.

R_{T1} or R_{T2} can be omitted If only one temperature (hot or cold) setting is required. Applying a voltage between the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to pin TS disables the temperature-sensing feature.

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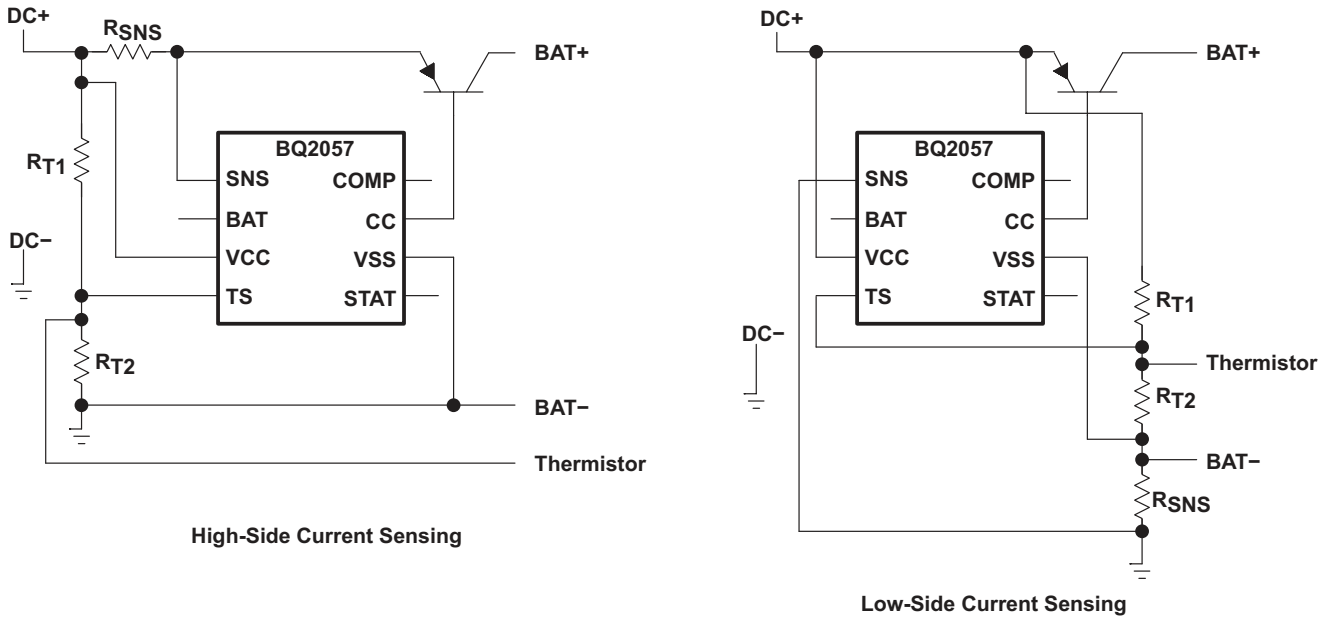

Figure 10-9. Temperature Sensing Circuits

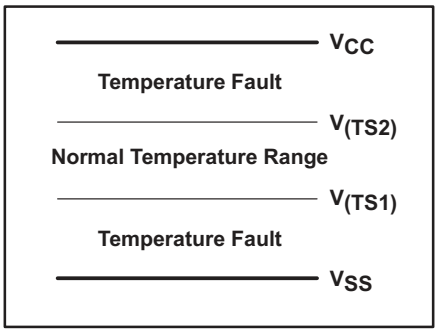

Figure 10-10. BQ2057 TS Input Thresholds

10.1.7 Charge Inhibit Function

The TS pin can be used as charge-inhibit input. The user can inhibit charge by connecting the TS pin to VCC or VSS (or any level outside the V(TS1) to V(TS2) thresholds). Applying a voltage between the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to pin TS returns the charger to normal operation.

10.1.8 Charge Status Indication

The BQ2057 reports the status of the charger on the 3-state STAT pin. The following table summarized the operation of the STAT pin.

CONDITION	STAT PIN
Battery conditioning and charging	High
Charge complete (Done)	Low
Temperature fault or sleep mode	Hi-Z

The STAT pin can be used to drive a single LED (Figure 10-1), dual-chip LEDs (Figure 4) or for interface to a host or system processor (Figure 10-11). When interfacing the BQ2057 to a processor, the user can use an output port, as shown in Figure 10-11, to recognize the Hi-Z state of the STAT pin. In this configuration, the user needs to read the input pin, toggle the output port and read the STAT pin again. In a Hi-Z condition, the input port always matches the signal level on the output port.

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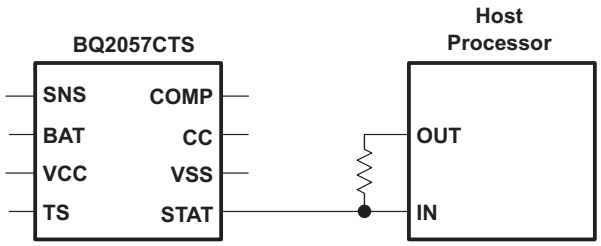

Figure 10-11. Interfacing the BQ2057 to a Host Processor

10.1.9 Low-power Sleep Mode

The BQ2057 enters the sleep mode if the VCC falls below the voltage at the BAT input. This feature prevents draining the battery pack during the absence of VCC.

10.1.10 Selecting an External Pass-Transistor

The BQ2057 is designed to work with both PNP transistor and P-channel MOSFET. The device should be chosen to handle the required power dissipation, given the circuit parameters, PCB layout and heat sink configuration. The following examples illustrate the design process for either device:

PNP transistor: Selection steps for a PNP bipolar transistor: Example: V_I = 4.5 V, $I_{(REG)}$ = 1 A, 4.2-V single-cell Li-Ion (bq2057C). V_I is the input voltage to the charger and $I_{(REG)}$ is the desired charge current (see Figure 10-1).

1. Determine the maximum power dissipation, P_D, in the transistor. The worst case power dissipation happens when the cell voltage, $V_{(BAT)}$, is at its lowest (typically 3 V at the beginning of current regulation phase) and VI is at its maximum.
   Where V_{CS} is the voltage drop across the current sense resistor.

$$P_D = \left(V_I - V_{CS} - V_{(BAT)}\right) \times IREG$$
$$P_D = \left(4.5 - 0.1 - 3\right) \times 1\,A$$
$$P_D = 1.4\ W \quad (7)$$

2. Determine the package size needed in order to keep the junction temperature below the manufacturer's recommended value, $T_{(J)max}$. Calculate the total theta, θ(°C/W), needed.

$$\theta_{JC} = \frac{\left(T_{(J)max} - T_{A(max)}\right)}{P_D}$$
$$\theta_{JC} = \frac{\left(150 - 40\right)}{1.4}$$
$$\theta_{JC} = 78°C / W \quad (8)$$

   Now choose a device package with a theta at least 10% below this value to account for additional thetas other than the device. A SOT223 package, for instance, has typically a theta of 60°C/W.
3. Select a collector-emitter voltage, $V_{(CE)}$, rating greater than the maximum input voltage. A 15-V device will be adequate in this example.
4. Select a device that has at least 50% higher drain current I_C rating than the desired charge current $I_{(REG)}$.
5. Using Equation 9, calculate the minimum beta (β or h_{FE}) needed:

$$\beta_{min} = \frac{I_{CMAX}}{1_B}$$
$$\beta_{min} = \frac{1}{0.035}$$
$$\beta_{min} = 28 \quad (9)$$

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where $I_{max(C)}$ is the maximum collector current (in this case same as $I_{(REG)}$), and I_B is the base current (chosen to be 35 mA in this example).

Note

The beta of a transistor drops off by a factor of 3 over temperature and also drops off with load. Therefore, note the beta of device at $I_{(REG)}$ and the minimum ambient temperature when choosing the device. This beta should be larger than the minimum required beta.

Now choose a PNP transistor that is rated for $V_{(CE)}$ ≥15 V, θ_{JC} ≤ 78°C/W, I_C ≥ 1.5 A, β_{min} ≥ 28 and that is in a SOT223 package.

P-channel MOSFET: Selection steps for a P-channel MOSFET: Example: V_I = 5.5 V, $I_{(REG)}$ = 500 mA, 4.2-V single-cell Li-Ion (BQ2057C). V_I is the input voltage to the charger and $I_{(REG)}$ is the desired charge current. (See Figure 10-4.)

1. Determine the maximum power dissipation, P_D, in the transistor.
   The worst case power dissipation happens when the cell voltage, $V_{(BAT)}$, is at its lowest (typically 3 V at the beginning of current regulation phase) and V_I is at its maximum.
   Where V_D is the forward voltage drop across the reverse-blocking diode (if one is used), and V_{CS} is the voltage drop across the current sense resistor.

$$P_D = \left(V_I - V_D - V_{(CS)} - V_{(BAT)}\right) \times I_{(REG)}$$
$$P_D = \left(5.5 - 0.4 - 0.1 - 3\right) \times 0.5\ A$$
$$P_D = 1\ W \quad (10)$$

2. Determine the package size needed in order to keep the junction temperature below the manufacturer's recommended value, T_{JMAX}. Calculate the total theta, θ(°C/W), needed.

$$\theta_{JC} = \frac{\left(T_{max(J)} - T_{A(max)}\right)}{P_D}$$
$$\theta_{JC} = \frac{(150 - 40)}{1}$$
$$\theta_{JC} = 110°C / W \quad (11)$$

   Now choose a device package with a theta at least 10% below this value to account for additional thetas other than the device. A TSSOP-8 package, for instance, has typically a theta of 70°C/W.
3. Select a drain-source voltage, $V_{(DS)}$, rating greater than the maximum input voltage. A 12-V device will be adequate in this example.
4. Select a device that has at least 50% higher drain current (I_D) rating than the desired charge current $I_{(REG)}$.
5. Verify that the available drive is large enough to supply the desired charge current.

$$V_{(GS)} = \left(V_D + V_{(CS)} + V_{OL(CC)}\right) - V_I$$
$$V_{(GS)} = \left(0.4 + 0.1 + 1.5\right) - 5.5$$
$$V_{(GS)} = -3.5 \quad (12)$$

   Where $V_{(GS)}$ is the gate-to-source voltage, V_D is the forward voltage drop across the reverse-blocking diode (if one is used), and V_{CS} is the voltage drop across the current sense resistor, and $V_{OL(CC)}$ is the CC pin output low voltage specification for the BQ2057.

   Select a MOSFET with gate threshold voltage, $V_{(GSth)}$, rating less than the calculated $V_{(GS)}$.

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Now choose a P-channel MOSFET transistor that is rated for V_{DS} ≤ −15 V, θ_{JC} ≤ 110°C/W, I_D ≥ 1 A, $V_{(GSth)}$ ≥ −3.5 V and in a TSSOP package.

10.1.11 Selecting Input Capacitor

In most applications, all that is needed is a high-frequency decoupling capacitor. A 0.1-µF ceramic, placed in proximity to VCC and VSS pins, works well. The BQ2057 works with both regulated and unregulated external dc supplies. If a nonregulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance must be added to the input of the charger.

10.1.12 Selecting Output Capacitor

The BQ2057 does not require any output capacitor for loop stability. The user can add output capacitance in order to control the output voltage when a battery is not present. The charger quickly charges the output capacitor to the regulation voltage, but the output voltage decays slowly, because of the low leakage current on the BAT pin, down to the recharge threshold. Addition of a 0.1-µF ceramic capacitor, for instance, results in a 100-mV(pp) ripple waveform, with an approximate frequency of 25 Hz. Higher capacitor values can be used if a lower frequency is desired.

10.1.13 Automatic Charge-rate Compensation

To reduce charging time, the BQ2057 uses the proprietary AutoComp technique to compensate safely for internal impedance of the battery pack. The AutoComp feature is disabled by connecting the COMP pin to VCC in high-side current-sensing configuration, and to VSS in low-side current-sensing configuration. The COMP pin must not be left floating.

Figure 10-12 outlines the major components of a single-cell Li-Ion battery pack. The Li-Ion battery pack consists of a cell, protection circuit, fuse, connector, current sense-resistors, and some wiring. Each of these components contains some resistance. Total impedance of the battery pack is the sum of the minimum resistances of all battery-pack components. Using the minimum resistance values reduces the odds for overcompensating. Overcompensating may activate the safety circuit of the battery pack.

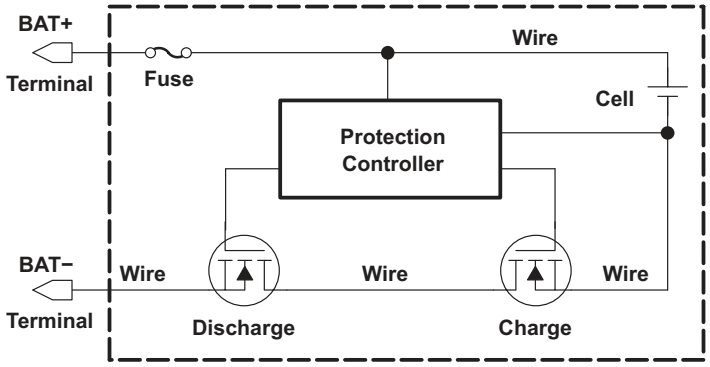

Figure 10-12. Typical Components of a Single-Cell Li-Ion Pack

Compensation is achieved through input pin COMP (Figure 10-13). A portion of the current-sense voltage, presented through this pin, is scaled by a factor of G(COMP) and summed with the regulation threshold, VO(REG). This process increases the output voltage to compensate for the battery pack's internal impedance and for undesired voltage drops in the circuit.

AutoComp setup requires the following information:

- Total impedance of battery pack ($Z_{(PACK)}$)
- Maximum charging current ($I_{(REG)}$)

The voltage drop across the internal impedance of battery pack, $V_{(Z)}$, can then be calculated using Equation 13:

$$V_{(Z)} = Z_{(PACK)} \times I_{(REG)} \quad (13)$$

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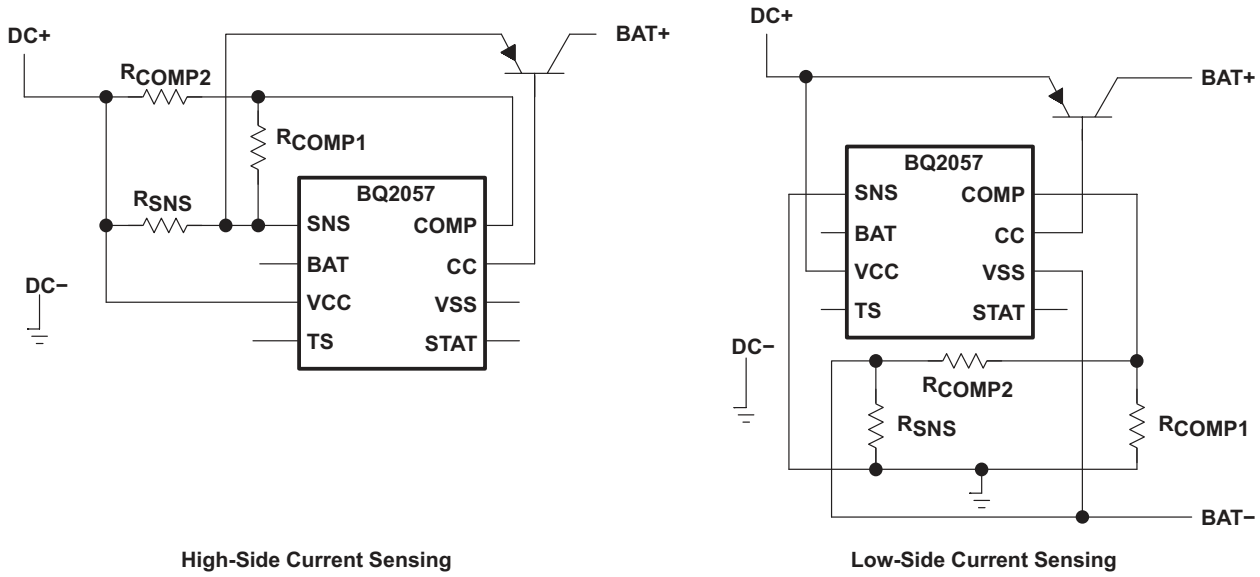
The required compensation is then calculated using Equation 14:

$$V_{(COMP)} = \frac{V_{(Z)}}{G_{(COMP)}}$$
$$V_{(PACK)} = V_{O(REG)} + \left(G_{(COMP)} \times V_{(COMP)}\right) \quad (14)$$

Where $V_{(COMP)}$ is the voltage on COMP pin. This voltage is referenced to VCC in high-side current sensing configuration and to VSS for low-side sensing. $V_{(PACK)}$ is the voltage across the battery pack.

The values of $R_{(COMP1)}$ and $R_{(COMP2)}$ can be calculated using Equation 15:

$$\frac{V_{(COMP)}}{V_{(SNS)}} = \frac{R_{COMP2}}{R_{COMP1} + R_{COMP2}} \quad (15)$$



High-Side Current Sensing

Low-Side Current Sensing

Figure 10-13. AutoComp Circuits

The following example illustrates these calculations:

Assume $Z_{(PACK)}$ = 100 mΩ, $I_{(REG)}$ = 500 mA, high-side current sensing BQ2057C

$$V_{(Z)} = Z_{(PACK)} \times I_{(REG)}$$
$$V_{(Z)} = 0.1 \times 0.5$$
$$V_{(Z)} = 50 \text{ mV} \quad (16)$$

$$V_{(COMP)} = \frac{V_{(Z)}}{G_{(COMP)}}$$
$$V_{(COMP)} = \frac{0.05}{2.2}$$
$$V_{(COMP)} = 22.7 \text{ mV}$$
$$\text{Let } R_{COMP2} = 10 \text{ k}\Omega \quad (17)$$

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$$R_{COMP1} = \frac{R_{COMP2} \times \left(V_{(SNS)} - V_{(COMP)}\right)}{V_{(COMP)}}$$

$$R_{COMP1} = 10k \times \frac{\left(105\ mV - 22.7\ mV\right)}{22.7\ mV}$$

$$R_{COMP1} = 36.25\ k\Omega \quad (18)$$

Use the closest standard value (36.0 kΩ) for R_{COMP1}.

10.2 Typical Application

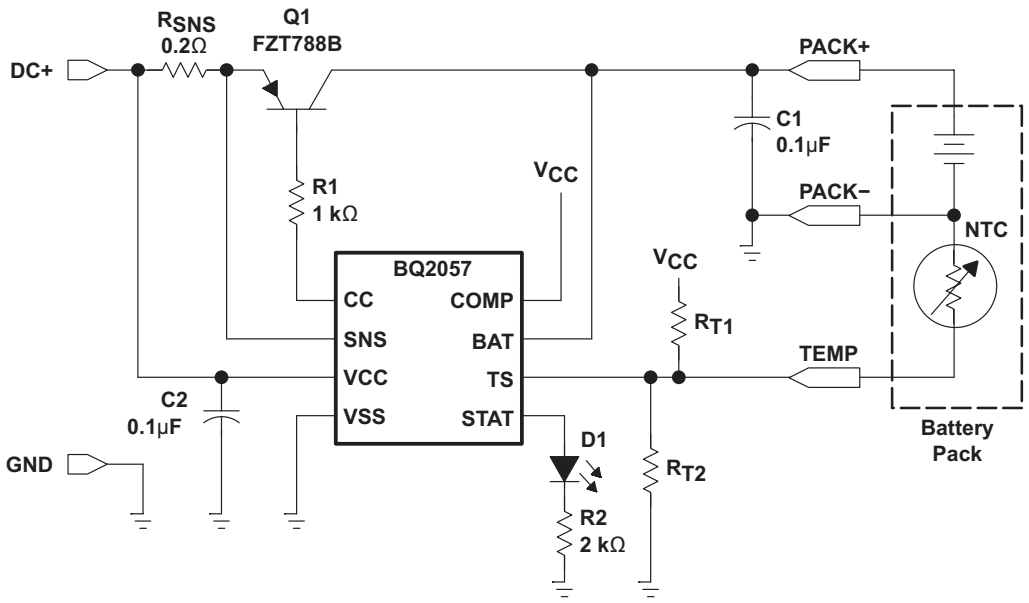

Figure 10-14. Low Dropout Single- or Two-Cell Li-Ion/Li-Pol Charger

10.2.1 Design Requirements

The design requirements include the following:

- Supply voltage = 12 V
- Dual cell Li-ion 8.2 V
- Fast charge current = 600 mA
  - High-side current sense
- Termination current = 10% (default)
- Precharge current = 10% (default)
- TS – Battery temperature sense = 10 kΩ (103AT, NTC)
  - 0°C cold and 60°C hot

10.2.2 Detailed Design Procedure

The detailed design procedure is listed below:

- Single cell Li-ion, 8.2 V - BQ2057T
- Pass transistor
  - For PNP BJT, see section 10.1.10 PNP transistor
  - For P-Type MOSFET, see section 10.1.10 P-channel MOSFET
- Fast charge current, see equation 1
  - Rsns = Vsns / Iout - 125 mV/600mA = 0.2 Ω
- Termination Current default to 10% of fast charge current

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- Pre-Charge Current default to 10% of fast charge current.
- TS – apply Equations 3 and 4 to calculate RT1 and RT2
  - RT1 = 5600 Ω (5.62 kΩ), RT2 = 12326 Ω (12.4 kΩ)

10.2.3 Application Curves

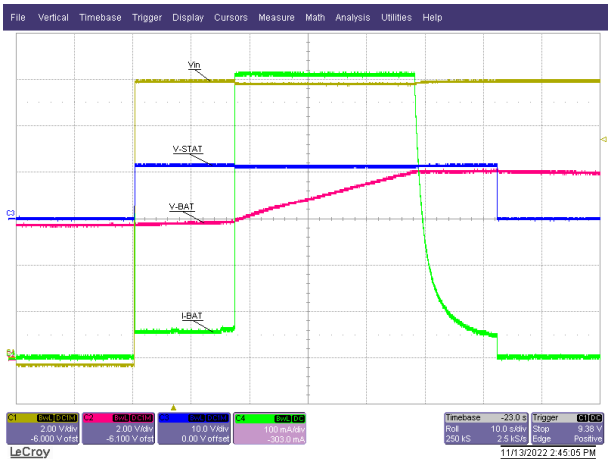

Figure 10-15. Charge Profile with Battery Simulator

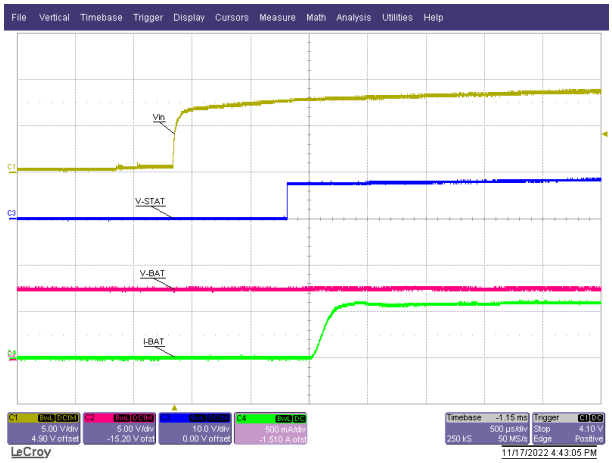

Figure 10-16. Charge Profile with Battery Simulator - STAT

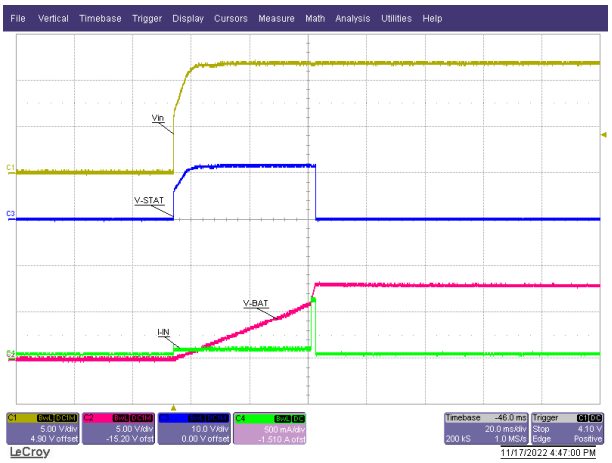

Figure 10-17. Power On - No Battery

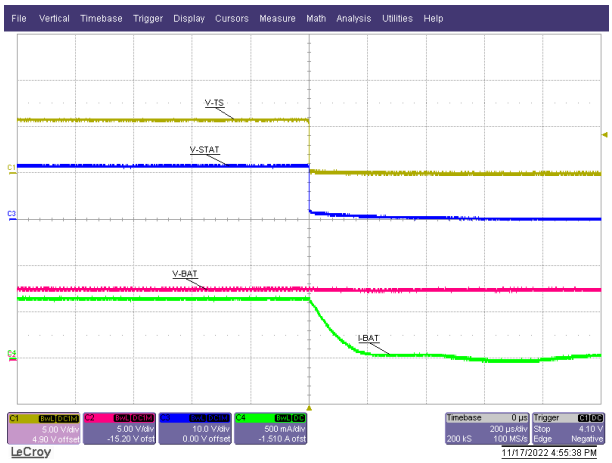

Figure 10-18. Shutdown - TS Pin Low

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11 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 15 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the device, VCC and GND terminals, a larger capacitor is recommended.

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12 Layout

12.1 Layout Guidelines

12.1.1 Power FET

The external pass PNP transistor or P-channel MOSFET will have high thermal rise, good heat sinking will be required.

12.1.2 Current Sense

The BQ2057 regulates current by sensing, on the SNS pin, the voltage drop developed across an external sense resistor. The sense resistor must be placed between the supply voltage (Vcc) and the input of the IC (IN pins).

12.1.3 Voltage Sense

To achieve maximum voltage regulation accuracy, the BQ2057 uses the feedback on the BAT pin. Externally, this pin should be connected as close to the battery cell terminals as possible. For additional safety, a 10-kΩ internal pullup resistor is connected between the VSENSE and OUT pins.

12.1.4 Enable (TS)

The TS pin can be used as charge-inhibit. Pulling up to VCC or pulling down to VSS places the device in a low-power standby mode.

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12.2 Layout Example

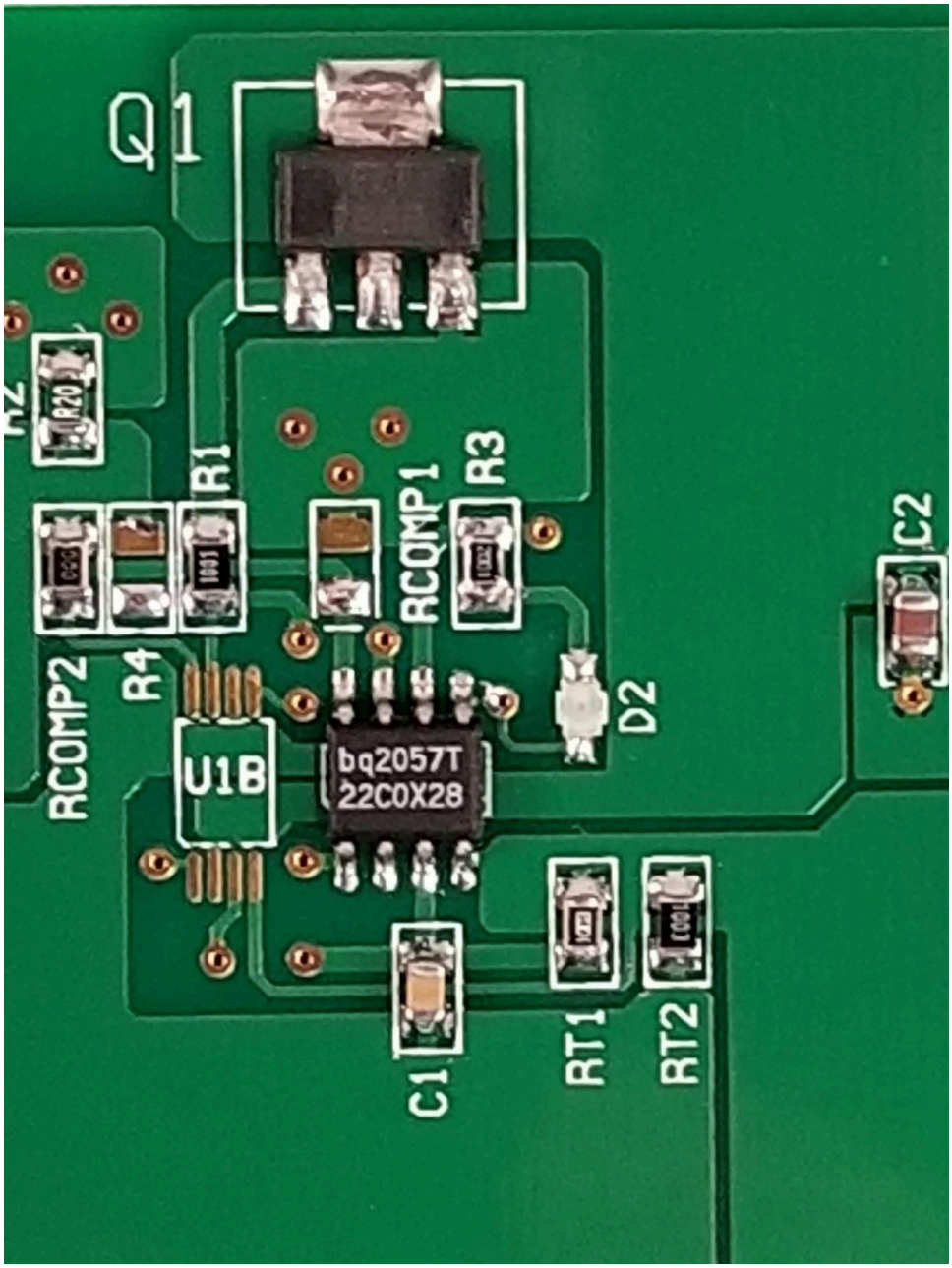

Figure 12-1. Layout Example

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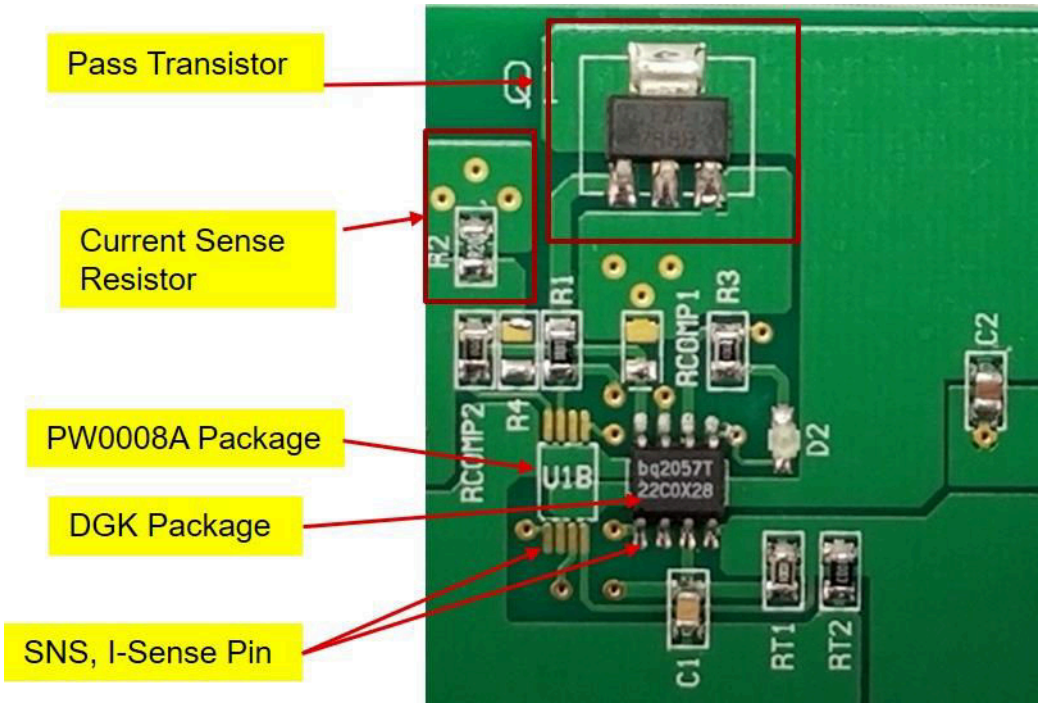

Figure 12-2. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2057CDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 70	2057C
BQ2057CDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 70	2057C
BQ2057CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 70	2057C
BQ2057CDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 70	2057C
BQ2057CSN	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2057C
BQ2057CSN.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2057C
BQ2057CSNTR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2057C
BQ2057CSNTR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2057C
BQ2057CTS	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2057C
BQ2057CTS.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2057C
BQ2057CTSTR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2057C
BQ2057CTSTR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2057C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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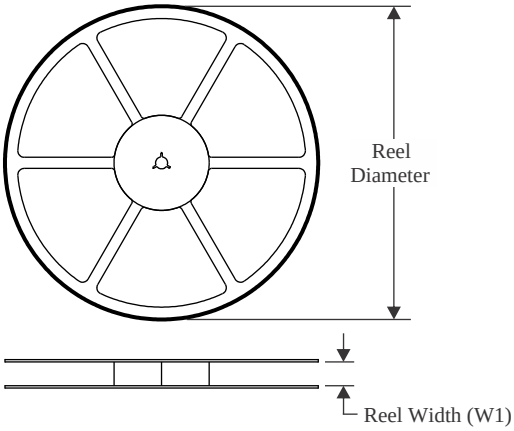
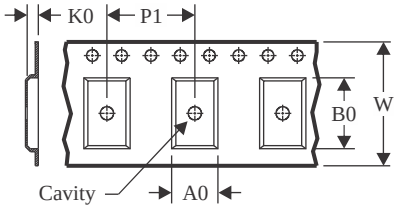
TAPE AND REEL INFORMATION

REEL DIMENSIONS

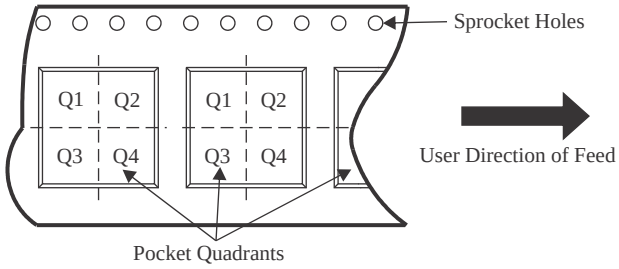


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

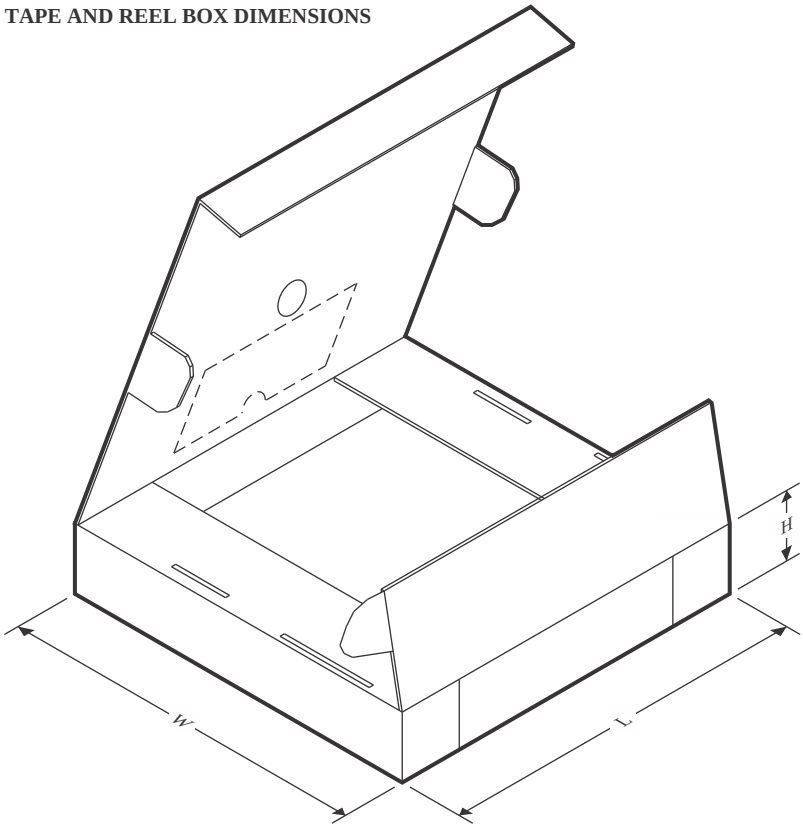
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2057CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ2057CSNTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
BQ2057CTSTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

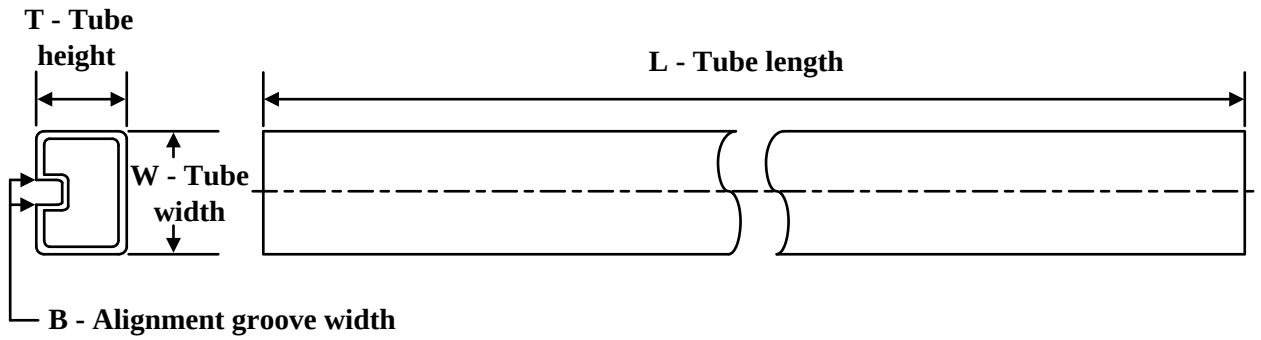
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2057CDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
BQ2057CSNTR	SOIC	D	8	2500	353.0	353.0	32.0
BQ2057CTSTR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

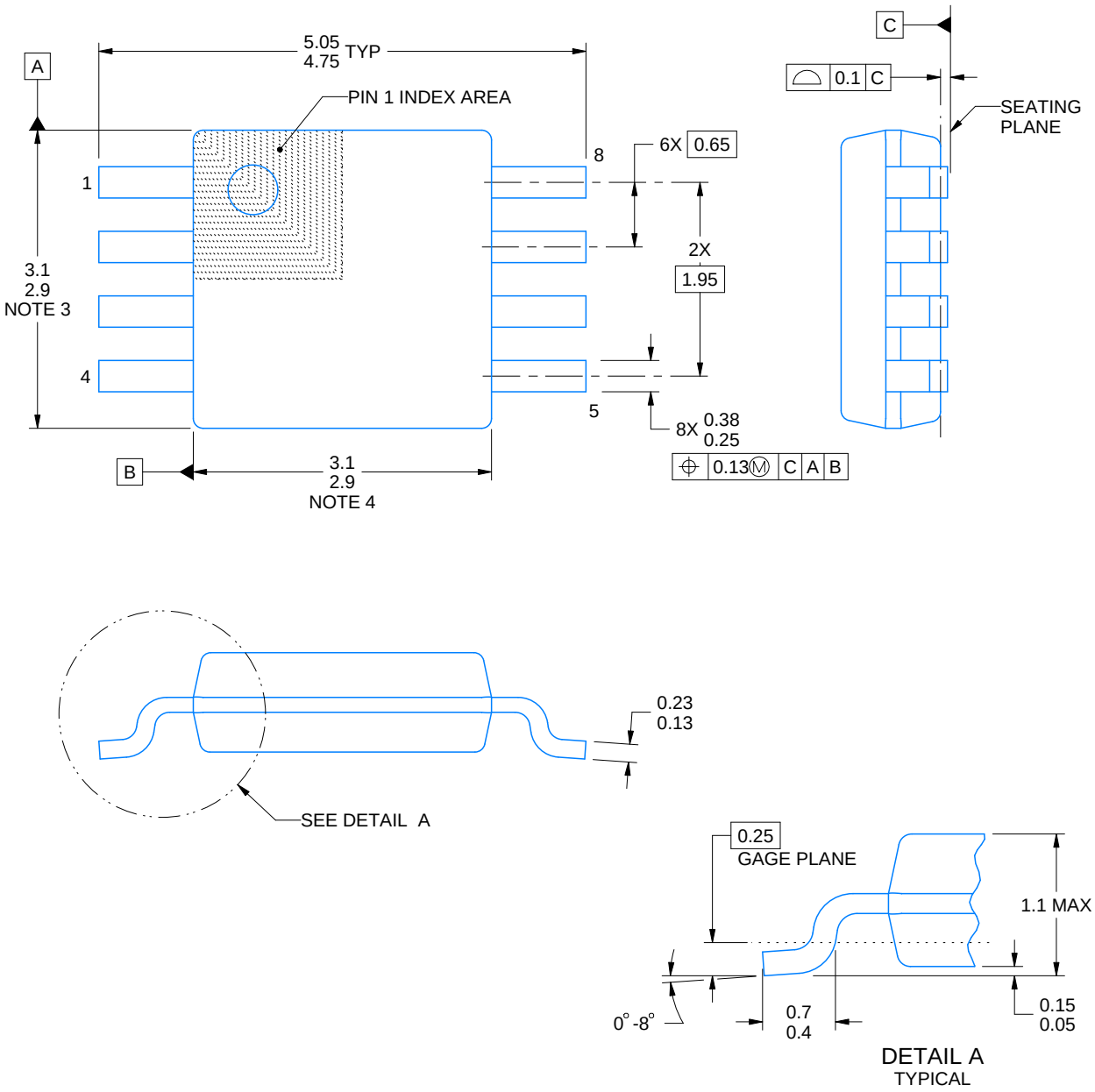
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ2057CDGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
BQ2057CDGK.A	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
BQ2057CSN	D	SOIC	8	75	506.6	8	3940	4.32
BQ2057CSN.A	D	SOIC	8	75	506.6	8	3940	4.32
BQ2057CTS	PW	TSSOP	8	150	508	8.5	3250	2.8
BQ2057CTS.A	PW	TSSOP	8	150	508	8.5	3250	2.8

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

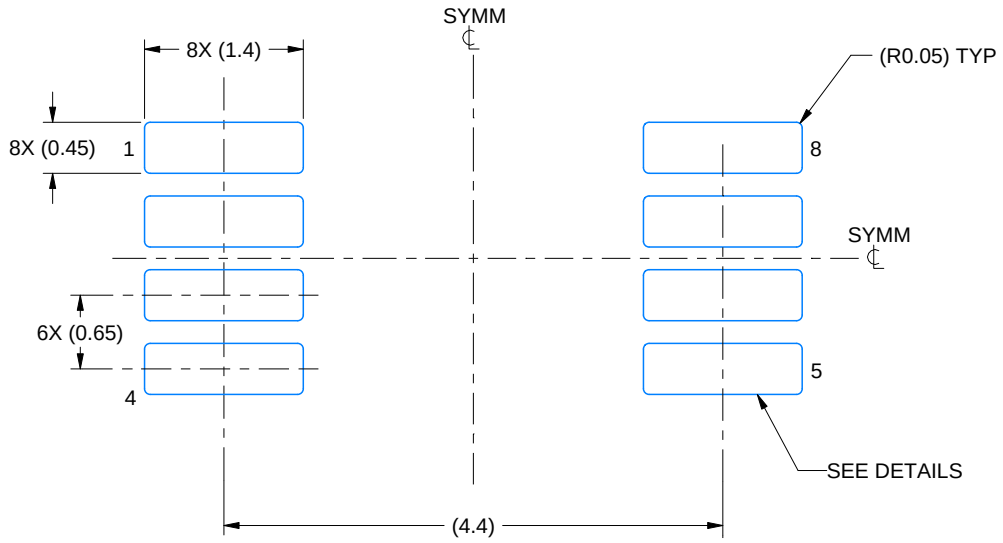
SMALL OUTLINE PACKAGE



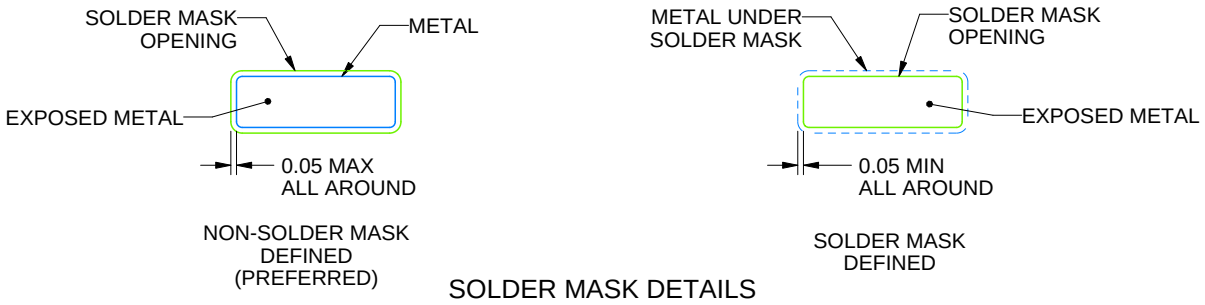
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

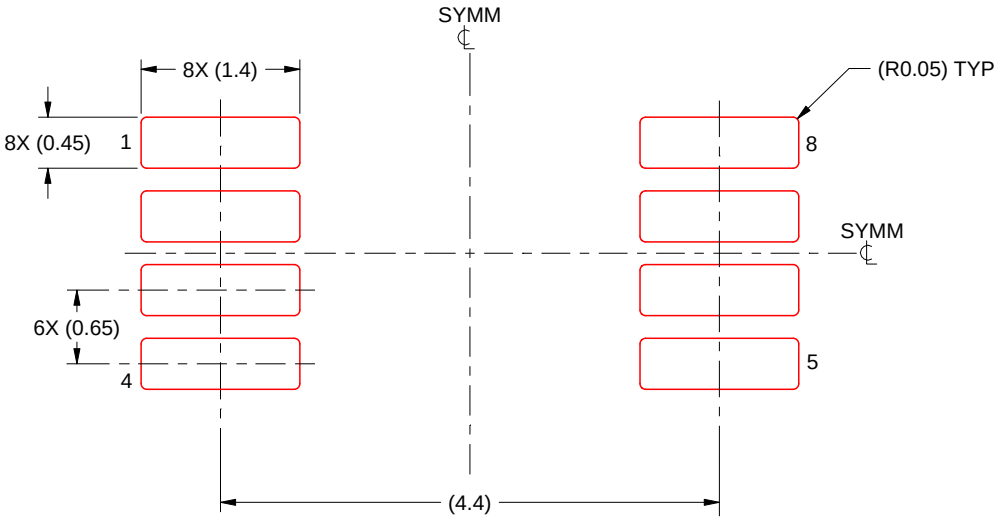


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

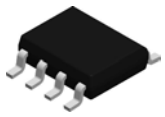


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

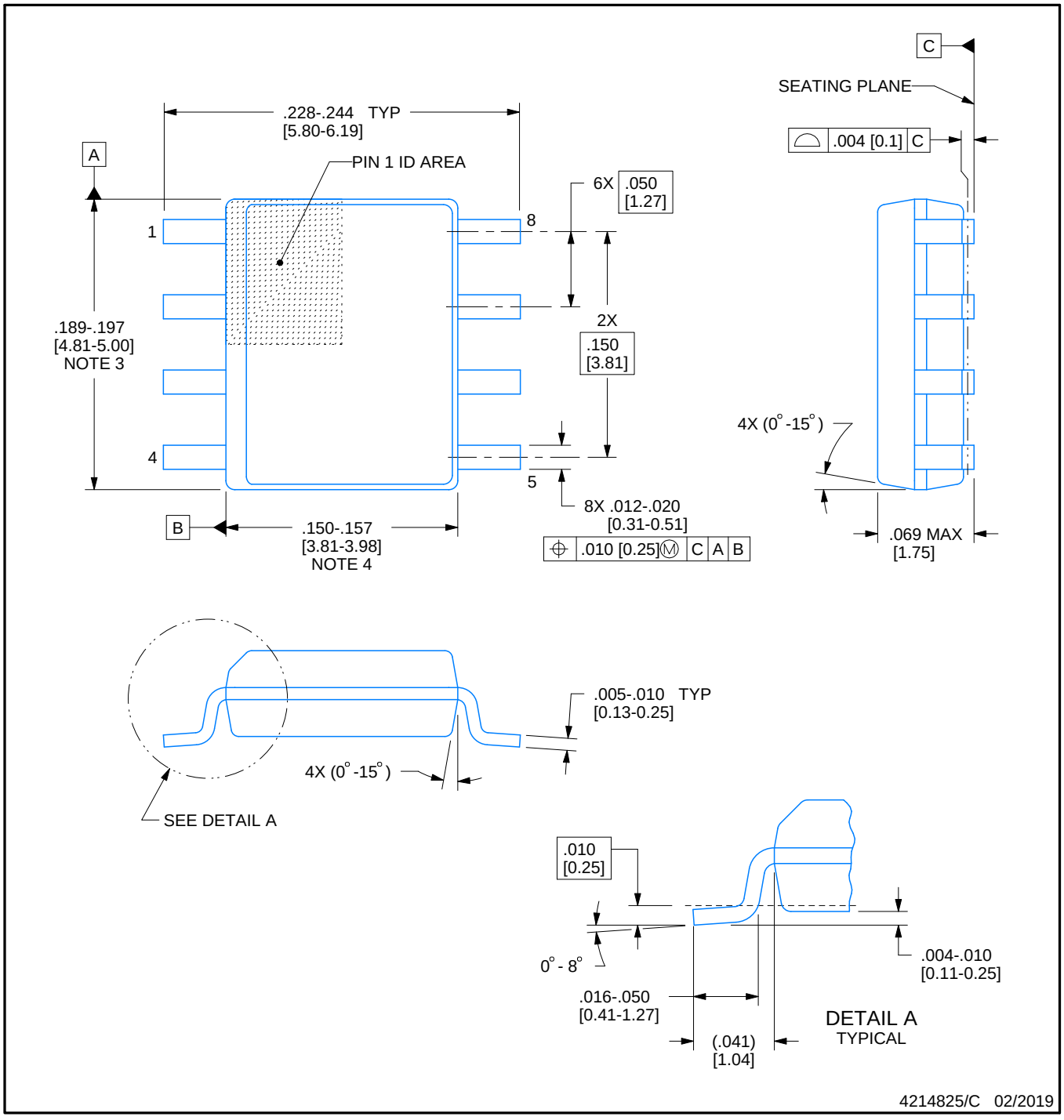


PACKAGE OUTLINE

D0008A

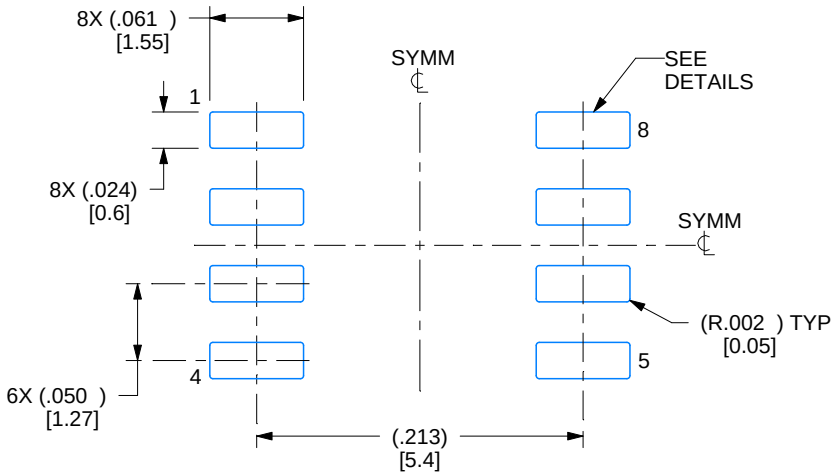
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

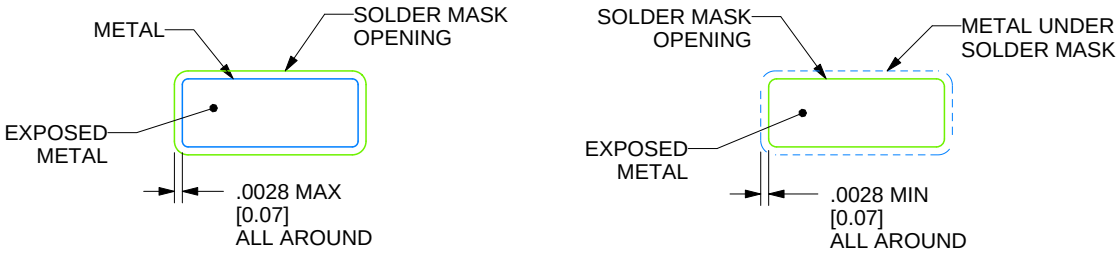


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

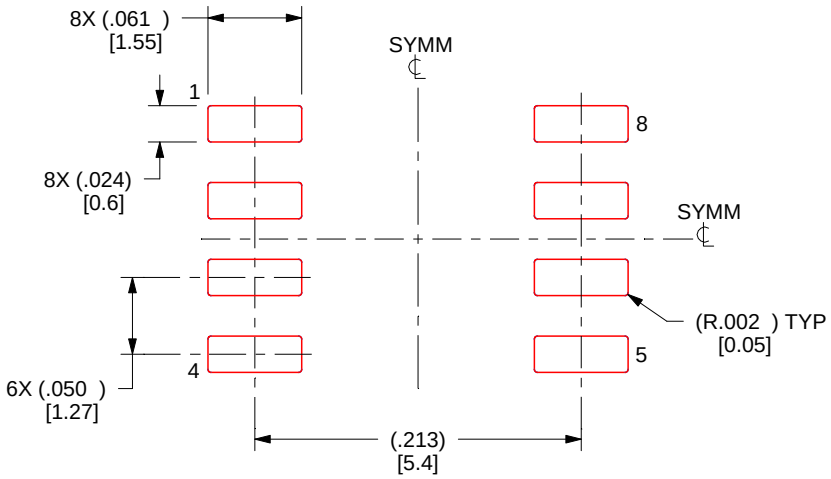
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

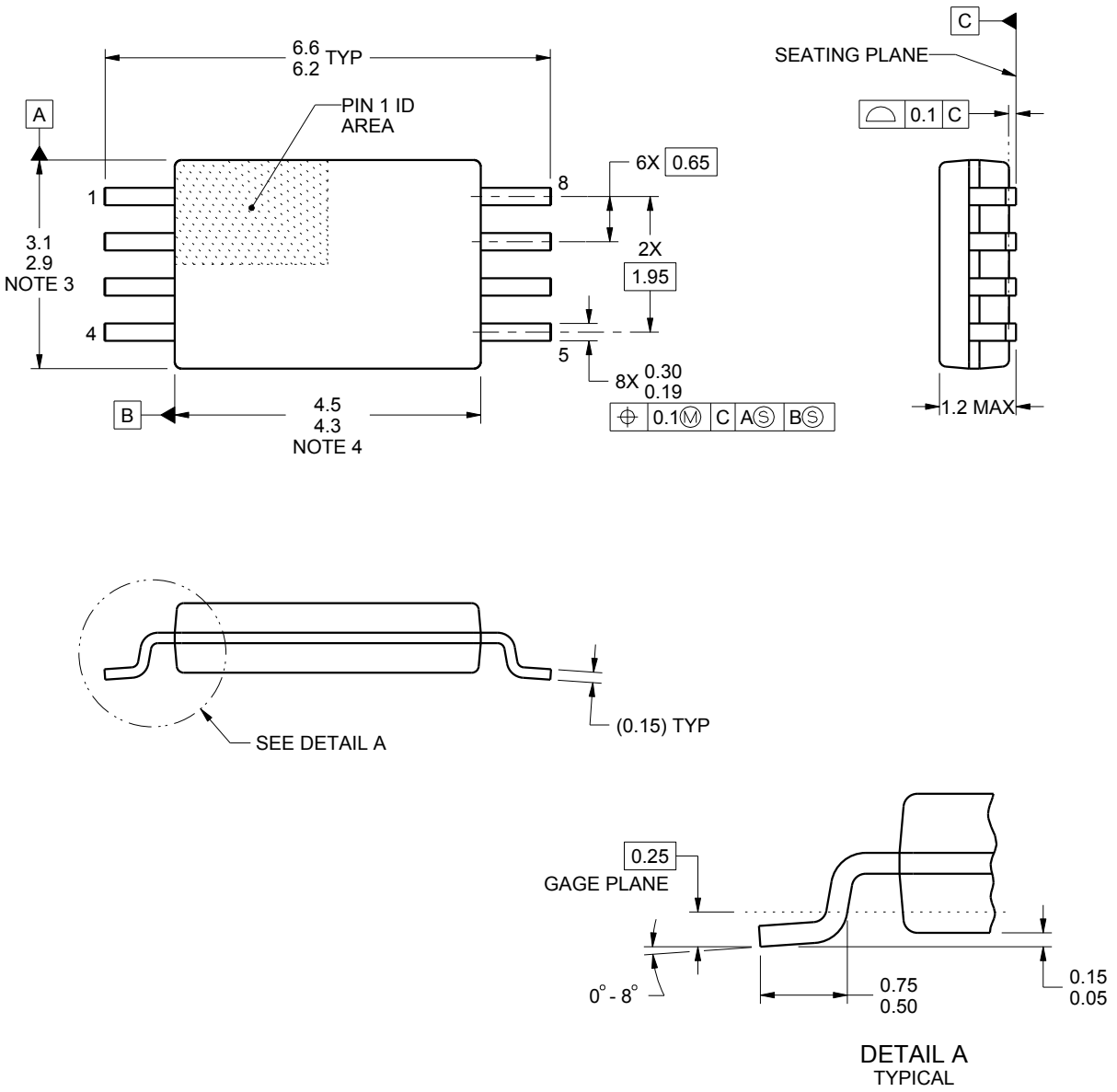
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

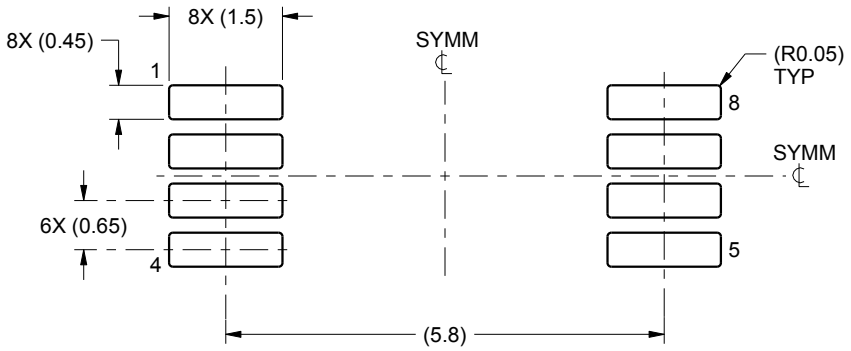
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

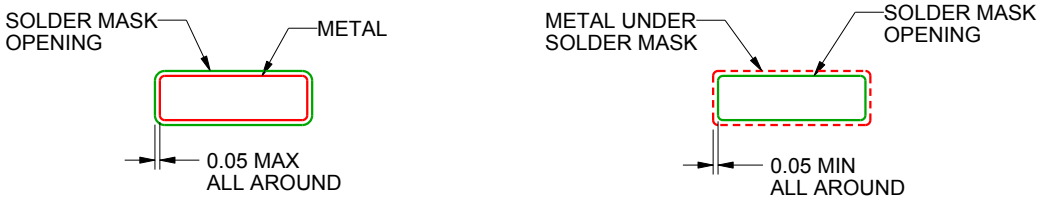


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

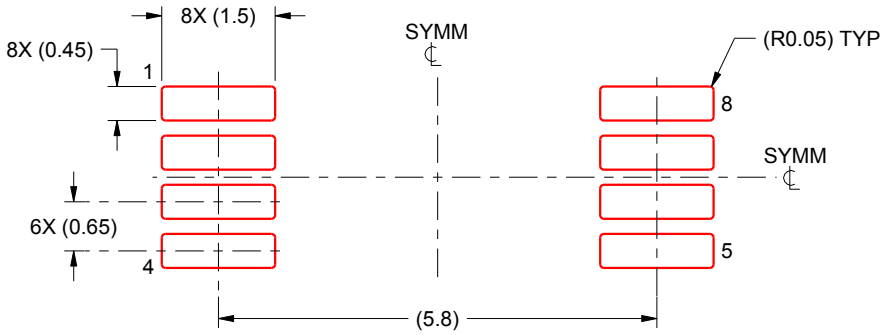


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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