Application Note AN-95
InnoSwitch3-PD Family

Design Guide

Introduction

The InnoSwitch™3-PD series family of ICs dramatically simplifies the development and manufacturing of fully programmable, USB-PD compliant, highly efficient power supplies, particularly those in compact enclosures.

InnoSwitch3-PD combines a high-voltage power switch (MOSFET or PowiGaN™), along both primary-side and secondary-side controllers that incorporate a USB Type-C and USB Power Delivery management, all in one device. The architecture incorporates a proprietary inductive coupling feedback mechanism – FluxLink™ to transmit switching requests to the primary-side controller.

The InnoSwitch3-PD primary-side controller employs a quasi-resonant (QR) flyback control-scheme that uses both variable frequency and variable current limit to regulate power delivery to the secondary-side. The power supply is able to operate in continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CRM), providing seamless transitions between states. The primary-side controller consists of a current limit controller with leading-edge blanking, frequency jitter oscillator, audible noise reduction engine for light load operation, current limit selection circuitry, a 5 V regulator on the PRIMARY BYPASS pin, primary-sensed output overvoltage protection feature that is realised by connecting a series resistor and Zener diode from the filtered bias winding voltage to the PRIMARY BYPASS pin, lossless input line voltage sensing and integrated over-temperature protection. A receiver circuit is also included which is magnetically coupled to the secondary controller.

The InnoSwitch3-PD secondary controller consists of a transmitter circuit that is magnetically coupled to the primary-side receiver via FluxLink, synchronous rectifier FET driver, VBUS series-switch driver and load discharge, QR mode control, oscillator and timing regulator on the SECONDARY BYPASS pin, a 3.6 V regulator on the µVCC pin, a USB Type-C and PD controller, and a host of integrated protection features.

Basic Circuit Configuration

Figure 1 shows the schematic for a 45 W flyback power supply for USB PD applications. Different output power levels may require different component values and a differently configured input stage to optimize EMI and surge protection, but the general circuit is similar.

Scope

This application note is intended to assist in designing an isolated AC-DC flyback power supply or charger using the InnoSwitch3-PD device. It provides guidelines for selecting key components and the information necessary to complete a suitable transformer design. To simplify the task, this application note refers directly to the InnoSwitch3-PD PIXls designer spreadsheet that is part of the PI Expert™ design software suite (available online https://www.power.com/design-support/pi-expert)

InnoSwitch3-PD Firmware

InnoSwitch3-PD parts that are marked with standard Feature Codes have been pre-loaded with appropriate firmware to support typical USB PD requirements. The firmware defines the USB PD Source Capabilities (Fixed Supply PDOs and PPS APDOs) supported by the device and configures the protection features.

Refer to the InnoSwitch3-PD data sheet for a complete list of available Feature Codes and firmware configurations for each InnoSwitch3-PD device. For applications that require custom USB PD source capabilities or a specific firmware configuration, please contact Power Integrations to discuss requirements.

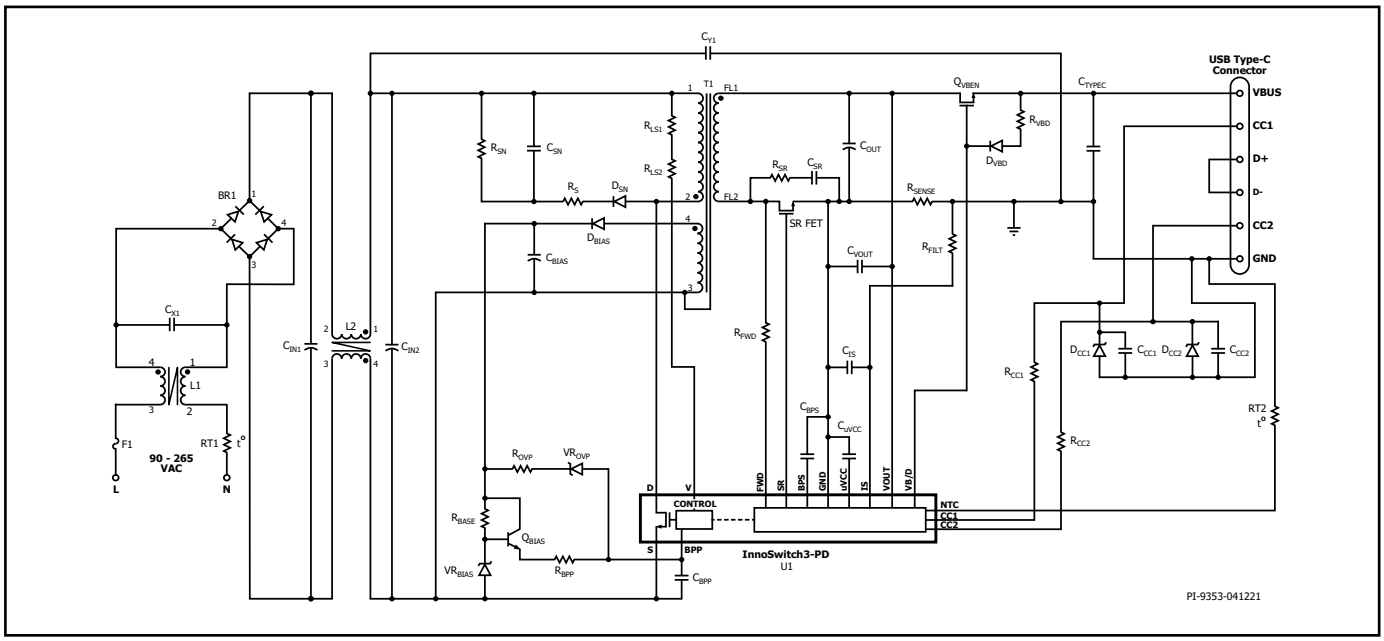


Figure 1. Typical 45 W USB Power Delivery Flyback Power Supply using InnoSwitch3-PD.

This Product is Covered by Patents and/or Pending Patent Applications.

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach, and can use the following information to quickly create the transformer and select the components for a first prototype. For this, only the information described below needs to be entered into the PIXls spreadsheet, other parameters will be automatically selected. References to spreadsheet line numbers are provided in square brackets, e.g. [L3] corresponds to line 3 in thespreadsheet.

1. Enter AC input voltage range and line frequency, VAC_MIN [L3], VAC_MAX [L4], LINEFREQ [L6]
2. Enter input capacitance, CAP_INPUT [L7]
   - For applications without hold-up-time requirement, 2 µF / W is recommended for universal (85 – 265 VAC) or low-line-only designs (110 / 115 VAC). 1 µF / W is recommended for high-line-only designs (230 VAC).
   - For applications with hold-up time requirements, a higher capacitance value will be needed. Calculate the minimum input capacitance based on output power, estimate efficiency, and determining hold-up voltage. Refer to equations in Appendix A.
   - If this cell is left blank, then the capacitance is automatically calculated without a hold-up time requirement and a target VMIN of 70 V (universal or low-line-only input) or 150 V (high-line-only input) for an optimal input filter capacitance value.
3. Enter highest output voltage required (including PPS APDOs), to SETPOINT1 VOUT1 [L10]
4. Enter continuous output current, IOUT1 [L11]
5. Enter efficiency estimate, EFFICIENCY [L13] as a decimal
   - Use 0.88 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC) and 0.90 for a single 230 VAC (185-265 VAC) design. Adjust the number accordingly after measuring the efficiency of the first prototype-board at maximum load and VACMIN
6. Enter loss factor, Z_factor [L14]
   - Typically, 0.5 for set-points <3 A, and up to 0.65 for 5 A set-points
7. Select set-point type, TYPE (PDO or APDO) [L15]
8. Repeat Steps 3 to 7 (VOUT to TYPE) for the succeeding SET-POINTs based on the USB PD Source for Capabilities of the design (PDOs and PPS APDOs). Enter the SET-POINTs with voltages in descending voltage order. This means SET-POINT1 voltage must be greater than SET-POINT2 voltage, and SET-POINT2 voltage must be greater than SET-POINT3 voltage
9. Enter desired Cable Drop Compensation (CDC) for PDOs, VOLTAGE_CDC [L81]
   - "0" for no Cable Drop Compensation or "0.300" for 300 mV CDC
10. Select power supply enclosure, ENCLOSURE (Adapter/Open Frame) [L86]
11. Select current limit mode, ILIMIT_MODE [L87]
    - Two current limit configurations are available, STANDARD or INCREASED
12. Select InnoSwitch3-PD device from drop-down list [L89] according to output power, input voltage and application
13. Enter desired maximum switching frequency at full load, FSWITCHING_MAX [L103]
14. Enter desired reflected output voltage, VOR [L104]
15. Choose core type (if desired), CORE [L133] from drop down menu
    - Suggested core size will be selected automatically if none is entered
    - For custom core, choose CUSTOM CORE [L133], and enter core parameters from [L134] to [L142]
16. Enter secondary number of turns [L158]

If any warnings are generated, make changes to the design by following the instructions provided in the right-most column of the spreadsheet.

- Build transformer as suggested in "Transformer Construction" tab
- Select key components
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were initially used (e.g. efficiency, VMIN). Note that the initial efficiency estimate is very conservative.

Product[4,5]	230 VAC ± 15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
INN3865C/3875C	25 W	30 W	22 W	25 W
INN3866C/3876C	35 W	40 W	27 W	36 W
INN3877C	40 W	45 W	36 W	40 W
INN3867C	45 W	50 W	40 W	45 W
INN3868C	55 W	65 W	50 W	55 W
INN3878C	70 W	75 W	55 W	65 W
INN3879C	80 W	85 W	65 W	75 W
INN3870C	90 W	100 W	75 W	85 W
INN3896C	25 W	35 W	20 W	30 W

Table 1. Output Power Table of InnoSwitch3-PD.

Notes:
1. Maximum output power is dependent on the design, with maximum IC package temperature kept <125 °C.
2. Minimum continuous power in a typical non-ventilated enclosed adapter measured at 40 °C ambient.
3. Minimum peak power capability.
4. C Package: InSOP-24D.
5. INN386xC – 650 V MOSFET, INN387xC – 725 V MOSFET, INN3878C, INN3879C and INN3870C – 750 V PowiGaN switch, INN3896C – 900 V MOSFET.

Step-by-Step Design Procedure

This design procedure uses the PIXIs design software (available as a free download from the Power Integrations website), which automatically performs the key calculations for an InnoSwitch3-PD flyback power supply design. PIXIs allows designers to simplify what would otherwise be the highly iterative design process. Look-up tables and empirical design guidelines are provided where appropriate to help simplify the design task.

Iterate the design to eliminate warnings. Any estimated circuit parameters that lie outside the recommended range of values can be corrected by following the guidance given in the right hand column. Once all warnings have been cleared, the output transformer design parameters can be used to create a prototype transformer.

Step 1 – Application Variables

Input Specifications

Enter: VIN_MIN, VIN _MAX, LINEFREQ, CAP_INPUT

Minimum and Maximum Input Voltage, V_MIN, V_MAX (VAC)
Determine the input voltage range from Table 2 for a particular regional requirement.

Line Frequency, LINEFREQ (Hz)
50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate overall design margin. For absolute worst-case or when required by the product specification reduce these numbers by 6% (47 Hz or 56 Hz).

Total Input Capacitance, CAP_INPUT (µF)
Enter total input capacitance using Table 3 for guidance. The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, VMIN > 70 V.

1	ACDC_InnoSwitch3-PD_Flyback_022421; Rev.0.4; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-PD Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX	265		265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE	50		50	Hz	AC line voltage frequency
7	CAP_INPUT	81.0		81.0	uF	Input capacitance

Figure 2. Application Variable Section of InnoSwitch3-PD Design Spreadsheet with Gray Override Cells.

Region	Nominal Input Voltage (VAC)	Minimum Input Voltage (VAC)	Maximum Input Voltage (VAC)	Nominal Line Frequency (Hz)
Japan	100	85	132	50 / 60
United States, Canada	120	90	132	60
Australia, China, European Union Countries, India, Korea, Malaysia, Russia	230	185	265	50
Indonesia, Thailand, Vietnam	220	185	265	50
Rest of Europe, Asia, Africa, Americas and rest of the world	115, 120, 127	90	155	50 / 60
	220, 230	185	265	50 / 60
	240	185	265	50

Visit: https://www.iec.ch/world-plugs

Table 2. Worldwide Nominal Input Line Voltages and Line Frequencies.

AC Input Voltage (VAC)	Total Input Capacitance per Watt of Output Power (µF/W)	
	Full Wave Rectification	
	Open Frame or Charger / Adapter without hold-up time requirement	Adapter with hold-up time requirement[1]
85 – 265 (Universal)	2	>2
100 / 115 (Low-Line only)	2	>2
230 (High-Line only)	1	>1

Note 1: Calculated minimum input capacitance to meet hold-up time requirement. Simple calculation is presented in Appendix A.

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

Output Set-Points

Enter: VOUT, IOUT, EFFICIENCY, Z-FACTOR, TYPE, CDC
A USB PD power supply typically supports multiple set-points. InnoSwitch3-PD can provide both Fixed Supply Power Data Object (PDO) and Programmable Power Supply Augmented Power Data Object (PPS APDO), based on the firmware uploaded into the IC. Table 4 shows some examples of USB PD Source Capabilities for different PD Power (PDP) Ratings in an InnoSwitch3-PD design. Please refer to USB Power Delivery Specifications documents for the required and optional source capabilities for a given PDP rating (https://www.usb.org/document-library/usb-power-delivery).

Once all of the USB PD Source Capabilities have been defined, multiple set points must be created in PIXIs by entering VOUT, IOUT, EFFICIENCY, Z-FACTOR, and TYPE to cover all the desired source capabilities.

Nominal SET-POINT Voltage, VOUT (V)

Each of the set points should be entered in PI XIs including their corresponding load current. As noted previously, the SET-POINTs should be entered in descending order of voltage. For USB PD power supplies that support PPS, the highest voltage set point will generally be the maximum voltage limit for the PPS APDO.

For example, a 45 W power adapter with source capabilities in Table 4 is to be designed. The highest output voltage is 21 V, and this should be entered as SET-POINT1 as shown in Figure 3. The complete list of set-points that must be entered is: 21 V, 20 V, 16 V, 15 V, 11 V, 9 V, 5 V, and 3.3 V.

Power Supply Output Current, IOUT (A)
This is the maximum continuous load current of the power supply for each set point. For PDO and PPS APDOs that are not power limited (PPS Power Limited bit set to 0), the IOUT of the set-point is simply the maximum current of the PDO or APDO.

For PPS APDOs that are power limited, whenever the USB PD Sink sends a valid Output Voltage and Current Limit request that exceeds the PDP rating, the power supply will reduce its current limit such that the PDP rating is not exceeded, therefore, for power-limited APDOs, IOUT should be entered using the equation below, rounded down to the nearest 50 mA.

$$I_{OUT} = \frac{PDP}{V_{OUT}}$$

Using the same 45 W design example described earlier, SETPOINT5 corresponds to 11 V which is PPS APDO, 45 W power-limited. The IOUT for SETPOINT5 should be entered as 4.050 A.

Also note that when the design supports multiple PPS APDOs, the 3.3 V set-point should be created using the maximum current capability. Again for the 45 W design example, this will correspond to SETPOINT8 having 3.3 V and 5 A as VOUT and IOUT. There is no need to create new set-points for 3.3 V / 3 A or 3.3 V / 2.25 A.

PD Power (PDP) Rating	USB PD Source Capabilities	Source Type
27 W	5 V / 3 A	Fixed Supply PDO
	9 V / 3 A	Fixed Supply PDO
	3.3 V – 11 V / 3 A	Programmable Power Supply APDO (27 W Power-Limited)
45 W	5 V / 5 A	Fixed Supply PDO
	9 V / 5 A	Fixed Supply PDO
	15 V / 3 A	Fixed Supply PDO
	20 V / 2.25 A	Fixed Supply PDO
	3.3 V – 11 V / 5 A	Programmable Power Supply APDO (45 W Power-Limited)
	3.3 V – 16 V / 3 A	Programmable Power Supply APDO
	3.3 V – 21 V / 2.25 A	Programmable Power Supply APDO
60 W	5 V / 3 A	Fixed Supply PDO
	9 V / 3 A	Fixed Supply PDO
	15 V / 3 A	Fixed Supply PDO
	20 V / 3 A	Fixed Supply PDO
	3.3 V – 21 V / 3 A	Programmable Power Supply APDO
100 W	5 V / 5 A	Fixed Supply PDO
	9 V / 5 A	Fixed Supply PDO
	15 V / 5 A	Fixed Supply PDO
	20 V / 5 A	Fixed Supply PDO
	3.3 V – 21 V / 5 A	Programmable Power Supply APDO

Table 4. Sample USB PD Source Capabilities (including optional PPS APDOs) at Different PDP Ratings.

9	**SET-POINT 1**					
10	VOUT1	**21.00**		21.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	**2.250**		2.250	A	Output current 1
12	POUT1			47.25	W	Output power 1
13	EFFICIENCY1	**0.90**		0.90		Converter efficiency for output 1
14	Z_FACTOR1	**0.50**		0.50		Z-factor for output 1
15	TYPE	**APDO**		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
16						
17	**SET-POINT 2**					
18	VOUT2	**20.00**		20.14	V	Output voltage 2
19	IOUT2	**2.250**		2.250	A	Output current 2
20	POUT2			45.30	W	Output power 2
21	EFFICIENCY2	**0.90**		0.90		Converter efficiency for output 2
22	Z_FACTOR2	**0.50**		0.50		Z-factor for output 2
23	TYPE	**PDO**		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
24						
25	**SET-POINT 3**					
26	VOUT3	**16.00**		16.00	V	Output voltage 3
27	IOUT3	**3.000**		3.000	A	Output current 3
28	POUT3			48.00	W	Output power 3
29	EFFICIENCY3	**0.90**		0.90		Converter efficiency for output 3
30	Z_FACTOR3	**0.50**		0.50		Z-factor for output 3
31	TYPE	**APDO**		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
32						
33	**SET-POINT 4**					
34	VOUT4	**15.00**		15.18	V	Output voltage 4
35	IOUT4	**3.000**		3.000	A	Output current 4
36	POUT4			45.54	W	Output power 4
37	EFFICIENCY4	**0.90**		0.90		Converter efficiency for output 4
38	Z_FACTOR4	**0.50**		0.50		Z-factor for output 4
39	TYPE	**PDO**		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
40						
41	**SET-POINT 5**					
42	VOUT5	**11.00**		11.00	V	Output voltage 5
43	IOUT5	**4.050**		4.050	A	Output current 5
44	POUT5			44.55	W	Output power 5
45	EFFICIENCY5	**0.90**		0.90		Converter efficiency for output 5
46	Z_FACTOR5	**0.50**		0.50		Z-factor for output 5
47	TYPE	**APDO**		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)

Figure 3. Set-points 1 to 5 of a 45 W InnoSwitch3-PD Design. All Remaining Set-points (9 V, 5 V, and 3.3 V) must be Completely Filled in the Spreadsheet.

Output Power, POUT (W)
This is calculated for each set point value and will be automatically adjusted based on cable drop compensation selected.

Power Supply Efficiency, EFFICIENCY (η)
Enter the estimated efficiency of the complete power supply measured from the input and output terminals under peak load conditions and worst-case line (generally lowest input voltage). Table 5 can be used as a reference for initial values. Once a prototype has been constructed, the measured efficiency should be entered. Further transformer iteration(s) can be performed if required.

Power Supply Loss Allocation Factor, Z_FACTOR
This factor describes the apportioning of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, etc.) are not processed by the power stage (transferred through the transformer) and therefore although they reduce efficiency the transformer design is not effected.

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

Since the secondary losses are generally dominated by secondary-current related losses (such as RMS current through SRFET, average current through SR FET body diode, current ripple through output capacitor ESR), it follows that Z-factor generally increases with load current and not necessarily with output power.

At the first phase of designing an InnoSwitch3-PD power supply when no prototype has been built, a Z-factor estimate of 0.5 is recommended for set-points with IOUT of 3 A and below, and a Z-factor up to 0.65 can be used for set-points with IOUT of 5 A. If there is a need to optimize calculations, a power loss budget measured from the prototype can be used to determine the actual secondary losses and the Z-factor can be iterated in the spreadsheet.

Set-point Type, TYPE
Select whether the corresponding set-point is a PDO (Fixed Power Data Object) or APDO (Augmented Power Data Object).

Cable Drop Compensation, VOLTAGE_CDC (V)
Select the appropriate cable drop compensation depending on the choice of cable for the design. CDC is only applied to PDOs, and the amount of output voltage compensation linearly increases from 0 V to the CDC value as the load current increases from 0 to full-scale current of the power supply.

Enter a CDC value in PIXls that matches the CDC setting programmed into the InnoSwitch3-PD IC. For example, a 300 mV CDC setting in the InnoSwtich3-PD IC would correspond to the "0.300" entered into the spreadsheet.

PD Power (PDP) Rating	Set-Points			Efficiency Estimate	
	VOUT (V)	IOUT (A)	Type	Typical Low-Line Range / Universal Range (85 VAC Minimum)	Typical High-Line Range (185 VAC Minimum)
27 W	11	2.45	APDO	0.88	0.90
	9	3	PDO	0.88	0.90
	5	3	PDO	0.88	0.89
	3.3	3	APDO	0.86	0.86
45 W	21	2.25	APDO	0.91	0.92
	20	2.25	PDO	0.91	0.92
	16	3	APDO	0.91	0.92
	15	3	PDO	0.91	0.92
	11	4.1	APDO	0.90	0.91
	9	5	PDO	0.90	0.91
	5	5	PDO	0.89	0.90
	3.3	5	APDO	0.87	0.88
60 W	21	3	APDO	0.90	0.93
	20	3	PDO	0.90	0.93
	15	3	PDO	0.90	0.93
	9	3	PDO	0.90	0.92
	5	3	PDO	0.90	0.91
	3.3	3	APDO	0.87	0.88
100 W	21	5	APDO	0.91	0.93
	20	5	PDO	0.91	0.93
	15	5	PDO	0.91	0.93
	9	5	PDO	0.90	0.92
	5	5	PDO	0.90	0.92
	3.3	5	APDO	0.88	0.89

Table 5. Initial Efficiency Estimate with Output Measured on the PCB and with Synchronous Rectification for Set-points from Different PDP Ratings.

Note:
For adapter power supplies that require more than 75 W input during normal operation, power factor connection is typically applied. This may effect the input voltage to the flyback controller and the efficient estimate.

Step 2 – Primary Controller Selection

Enter: ENCLOSURE, ILIMIT_MODE, VDRAIN_BREAKDOWN, DEVICE_GENERIC

85	PRIMARY CONTROLLER SELECTION					
86	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
87	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
88	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
89	DEVICE_GENERIC	INN38X9		INN38X9		Device selection
90	DEVICE_CODE			INN3879C		Device code
91	PDEVICE_MAX			65	W	Device maximum power capability
92	RDSON_25DEG			0.44	Ω	Primary switch on-time resistance at 25°C
93	RDSON_100DEG			0.62	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			1.980	A	Primary switch minimum current limit
95	ILIMIT_TYP			2.130	A	Primary switch typical current limit
96	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.39	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			600.81	V	Peak drain voltage on the primary switch during turn-off

Figure 4. Primary Controller Selection of InnoSwitch3-PD Design Spreadsheet with Current Limit Mode Selection.

Enclosure
Power device selection will also be dependent on the application environment. For an open frame application where the operating ambient temperature is lower than in an enclosed adapter, PIXIs will suggest a smaller device for the same output power.

Generic Device Code, DEVICE_GENERIC
The default option is automatically selected based on input voltage range, maximum output power and application (i.e. adapter or open frame).

For manual selection of device size, refer to the InnoSwitch3-PD power table in the data sheet and select a device based on the output power. Then compare the continuous power to adapter column numbers in the power table, (if the power supply is of fully enclosed type), or compare to the open-frame column (if the power supply is an open-frame design). If the continuous power exceeds the value given in the power table (Table 1), then the next larger device should be selected. Similarly, if the continuous power is close to the maximum adapter power given in the power table, it may be necessary to switch to a larger device based on the measured thermal performance of the prototype.

Device Current Limit Mode, ILIMIT_MODE
For designs where thermals are not as challenging (such as open frame applications) ILIMIT MODE allows the choice of an INCREASED current limit, this will set the peak current of the device equivalent to the next bigger device's standard current limit and allow higher output power. By default, ILIMIT is set to STANDARD.

On-Time Drain Voltage, VDRAIN_ON_PRSW (V)
This parameter is calculated based on RDSON_100DEG and primary RMS current.

Drain Peak Voltage, VDRAIN_OFF_PRSW (V)
This parameter is the assumed Drain voltage seen by the device during off-time. The calculation assumes 10% minimum margin from the breakdown voltage rating of the internal MOSFET and gives a warning if this is exceeded.

VDRAIN < (VIN_MAX * 1.414) + VOR + VLKPRI – (BVDSS × 10%).

VLK_{PRI} is the voltage induced by the leakage inductance of the transformer when the FET turns off.

Other electrical parameters are displayed based from the data sheet, **RDSON_100DEG, ILIMIT_MIN, ILIMIT_TYP, ILIMIT_MAX, VDRAIN_BREAKDOWN.**

Step 3 – Worst-Case Electrical Parameters

Enter: FSWITCHING_MAX, VOR and LPRIMARY_TOL

102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	**75089**		75089	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
104	VOR	**157.5**		157.5	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			82.47	V	Valley of the rectified minimum input AC voltage at full load
106	KP			0.641		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			CCM		Mode of operation
108	DUTYCYCLE			0.640		Primary switch duty cycle
109	TIME_ON			11.31	us	Primary switch on-time
110	TIME_OFF			5.37	us	Primary switch off-time
111	LPRIMARY_MIN			403.8	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			425.0	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			446.3	uH	Maximum primary magnetizing inductance
115						
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.614	A	Primary switch average current
118	IPEAK_PRIMARY			2.116	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.682	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			2.109	A	Primary switch ripple current
121	IRMS_PRIMARY			0.931	A	Primary switch RMS current
122						
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			15.868	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			5.113	A	Secondary winding pedestal current
126	IRMS_SECONDARY			7.596	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			5.719	A	Output capacitor ripple current

Figure 5. Worst-Case Electrical Parameters Section of InnoSwitch3-PD Design Spreadsheet.

Switching Frequency, FSWITCHING_MAX (Hz)

This parameter is the target maximum operating switching frequency of the design (all set points evaluated at full load, minimum rectified AC input voltage). The maximum switching frequency of InnoSwitch3-PD in normal operation is 100 kHz, and the typical overload detection frequency is 110 kHz. In normal operating conditions, the switching frequency at full load should not be close to the overload detection frequency. Similarly, the maximum operating switching frequency should be chosen to be in the higher audible range.

The target maximum switching frequency range is 25 to 95 kHz, but it should be noted that the average frequency, accounting for primary inductance and peak current tolerances must not result in an average frequency of higher than 110 kHz as this will trigger auto-restart due to overload. While increasing switching frequency to reduce transformer size is preferable, Table 6 provides the suggested frequency based on the size of the internal high-voltage FET, and represents the best compromise to balance overall device losses (i.e. conduction and switching losses).

InnoSwitch3-PD Family	Maximum Switching Frequency
INN3865C / INN3875C	80 kHz
INN3866C / INN3876C	75 kHz
INN3877C	70 kHz
INN3867C / INN3868C	65 kHz
PowiGaN device INN3878C	70 kHz
PowiGaN device INN3879C	65 kHz
PowiGaN device INN3870C	60 kHz
INN3896C	70 kHz

Table 6. Suggested Maximum Switching Frequency.

Reflected Output Voltage, VOR (V)

This parameter is the secondary winding voltage seen during the diode / Synchronous Rectifier MOSFET (SR FET) conduction-time reflected back to the primary through the turns ratio of the transformer. Table 7 provides suggested values for VOR. VOR can be adjusted to achieve a design that does not violate design rules for the transformer and SR FET while simultaneously achieving sufficiently low Drain-Source voltage on the primary side MOSFET. VOR can be adjusted as necessary to ensure that no warnings in the spreadsheet are triggered. For design optimization purposes, the following factors should be considered:

- Higher VOR allows increased power delivery at VMIN, which minimizes the value of the input capacitor and maximizes power delivery from a given design.
- Higher VOR reduces the voltage stress on the output diodes and SR FETs, which in some cases may allow a lower voltage rating and not for higher efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases peak and RMS current on the secondary-side which may increase secondary side copper, diode and SR FET losses thereby reducing efficiency.

It should be noted that there are exceptions to this guidance especially for very high output currents where the VOR should be reduced to obtain highest efficiency. Higher output voltages (above 15 V) should employ a higher VOR to maintain acceptable peak inverse voltage (PIV) across the output SR FET.

Optimal selection of the VOR value depends on the specific application and is based on a compromise between the factors mentioned above. Refer to Table 7 for suggested values of VOR based on the maximum supported output voltage of the design.

When Application Variables and Primary Controller Selection have been finalized, FSWITCHING_MAX and VOR, are the parameters that primarily determine the target primary inductance in the spreadsheet.

Maximum Output Voltage	Suggested Range for VOR	
	INN386XC (650 V Switch)	INN387XC (725 / 750 V Switch)
5 V	45 – 60 V	45 – 70 V
9 V	80 – 90 V	80 – 100 V
12 V	100 – 120 V	90 – 120 V
15 V	100 – 120 V	100 – 135 V
20 V	100 – 120 V	120 – 150 V
21 V	100 – 120 V	125 – 160 V

Table 7. Suggested Values for VOR.

Mode of Operation, KP

KP is a measure of how discontinuous or continuous the mode of switching is. K_P below 1 indicates a CCM operation while K_P above 1 indicates DCM operation.

For CCM ($K_P \leq 1$), K_P is the ratio of ripple to peak primary current as illustrated in Figure 6.

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

For DCM ($K_P \geq 1$), K_P is the ratio of primary MOSFET off-time to the SR FET conduction time as shown in Figure 7.

$$K_P \equiv K_{DP} = \frac{(1 - D) \times T}{t} = \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

Each set-point in the design will correspond to a certain K_P value. Some set-points may result in CCM operation while others could be in DCM. The K_P shown in the worst-case electrical parameters section of PIXIs corresponds to the most CCM operation (smallest K_P value) of the design.

The value of K_P should be in the range of $0.5 < K_P < 6.0$. Having a worst-case KP below 0.5 will result in a design that is too continuous and the power supply will be in CCM for most of its operating output range. Under these conditions, the benefit of higher efficiency in DCM or critical mode (CRM) will not be fully utilized. Experience has shown that a K_P value between 0.6 and 1.0 results in high efficiency across all output and load conditions.

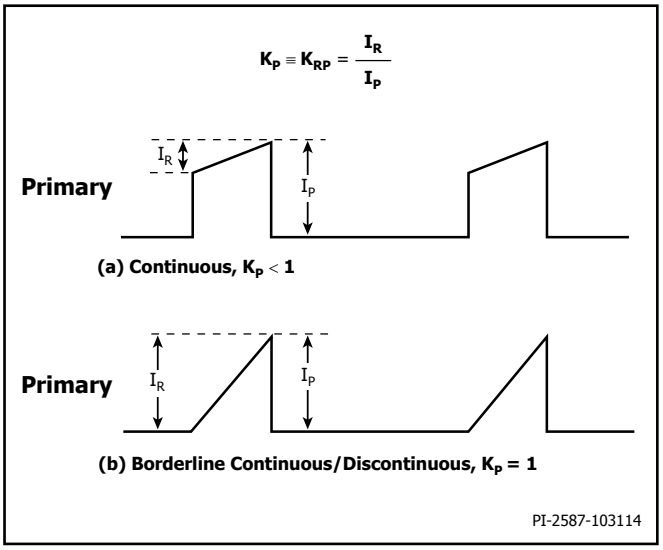


Figure 6. Continuous Mode Current Waveform, $K_P \leq 1$.

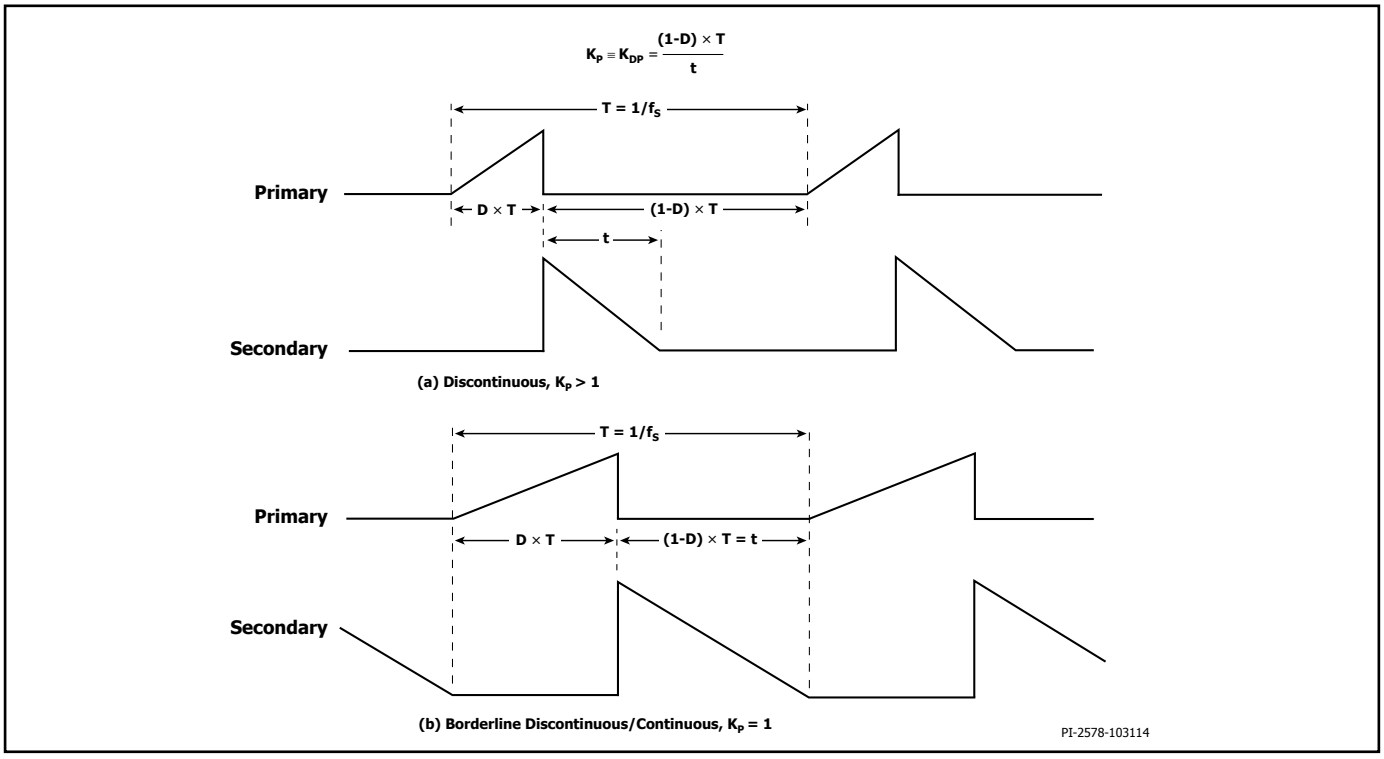


Figure 7. Discontinuous Mode Current Waveform, $K_P \geq 1$.

Typical Primary Inductance, LPRIMARY_TYP (μH)
This is the typical transformer primary inductance target.

Primary Inductance Tolerance, LPRIMARY_TOL (%)
This parameter is the assumed primary inductance tolerance. A value of 7% is used by default, however if specific information is provided from the transformer vendor, then this may be entered in the grey override cell. A value of 7% helps to reduce unit-to-unit variation and is easy to meet for most magnetics vendors. A value of 3% will help improve production tolerance further but will be more challenging to vendors.

The other important electrical parameters are automatically calculated by the spreadsheet. These can be used to appropriately select the other components in the circuit, such as input fuse, EMI filter, bridge rectifier, output rectifier (SR FET) and output capacitors, as described in Figure 1.

Primary Current
IPEAK_PRIMARY – Peak primary current
IPEDESTAL_PRIMARY – Primary MOSFET current pedestal in CCM
IAVG_PRIMARY – Primary MOSFET average current
IRIPPLE_PRIMARY – Primary MOSFET ripple current
IRMS_PRIMARY – Primary MOSFET RMS current

Secondary Current
IPEAK_SECONDARY – Peak secondary current
IPEDESTAL_SECONDARY – Secondary winding current pedestal
IRMS_SECONDARY – Secondary winding RMS current

Minimum Rectified Input Voltage, VMIN
Valley of the rectified minimum AC input voltage at full power is calculated based on input capacitance (CAP_INPUT).

Step 4 – Transformer Construction Parameters

Enter: CORE, AE, LE, AL, VE, BOBBIN, AW, BW, MARGIN
Choose Core and Bobbin based on maximum output power.

131	**TRANSFORMER CONSTRUCTION PARAMETERS**					
132	**CORE SELECTION**					
133	CORE	ATQ23.7/14.6	Info	ATQ23.7/14.6		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
134	CORE NAME			ATQ23.7/14.6		Core code
135	AE			103.0	mm^2	Core cross sectional area
136	LE			38.2	mm	Core magnetic path length
137	AL			7200	nH	Ungapped core effective inductance per turns squared
138	VE			3935	mm^3	Core volume
139	BOBBIN NAME			TBI-238-10051.17XX		Bobbin name
140	AW			22.1	mm^2	Bobbin window area
141	BW			6.60	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
143						
144	**PRIMARY WINDING**					
145	NPRIMARY			30		Primary winding number of turns
146	BPEAK			3369	Gauss	Peak flux density
147	BMAX			3017	Gauss	Maximum flux density
148	BAC			1502	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			472	nH	Typical gapped core effective inductance per turns squared
150	LG			0.256	mm	Core gap length
151	LAYERS_PRIMARY			2		Primary winding number of layers
152	AWG_PRIMARY			27		Primary wire gauge
153	OD_PRIMARY_INSULATED			0.418	mm	Primary wire insulated outer diameter
154	OD_PRIMARY_BARE			0.361	mm	Primary wire bare outer diameter
155	CMA_PRIMARY			216.5	Cmils/A	Primary winding wire CMA
156						
157	**SECONDARY WINDING**					
158	NSECONDARY	4		4		Secondary winding number of turns
159	AWG_SECONDARY			18		Secondary wire gauge
160	OD_SECONDARY_INSULATED			1.328	mm	Secondary wire insulated outer diameter
161	OD_SECONDARY_BARE			1.024	mm	Secondary wire bare outer diameter
162	CMA_SECONDARY			213.8	Cmils/A	Secondary winding wire CMA
163						
164	**BIAS WINDING**					
165	NBIAS			8		Bias winding number of turns

Figure 8. Transformer Core and Construction Variables Section of InnoSwitch3-PD PIXLs Spreadsheet.

Core Type, CORE
By default, if the core-type cell is left empty, the spreadsheet will select the smallest commonly available core suitable for the continuous (average) output power specified. Different core types and sizes from the drop-down list are available to choose from. If a user-preferred core is not available, the grey override cells (AE, LE, AL, VE, AW & BW) can be used to enter the core and bobbin parameters directly from the manufacturer's data sheet. A list of commonly available cores is shown in Table 8.

Safety Margin, MARGIN (mm)
For designs that require safety isolation between primary and secondary but are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically for universal (85 – 265 VAC) input designs a total margin of 6.2 mm is required, and a value of 3.1 mm should be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical; however, if a total margin of 6.2 mm is required then 3.1 mm would still be entered even if the physical margin was only present on one side of the bobbin. For designs using triple insulated wire it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Typically, several bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what margin is required.

Margin reduces the available area for the windings, so a margined types of construction may not be suitable for small core sizes. If after entering the margin, more than 3 primary layers are required, it is suggested that either a larger core be selected or that the design is switched to a zero-margin approach using triple insulated wire.

Primary Turns, NPRIMARY
This is the number of turns for the main winding of the transformer calculated based on VOR and Secondary Turns.

Peak Flux Density, BPEAK (Gauss)
A maximum value of 3800 Gauss is recommended to limit the peak flux density at maximum current limit and 132 kHz operation. Under an output-shorted condition the output voltage is low and little reset of the transformer occurs during the FET off-time. This allows the transformer flux density to "staircase" beyond the normal operating level. A value of 3800 Gauss at the maximum current limit of the selected device together with the built-in protection features of InnoSwitch3-PD provides sufficient margin to prevent core saturation under output short-circuit conditions.

Output Power at 75 kHz	Core and Bobbin Table								
	Core						Bobbin		
	Core	Code	AE (mm^2)	LE (mm)	AL (nH/T^2)	VE (mm^3)	Code	AW (mm^2)	BW (mm)
0 W – 10 W	EE10	PC47EE10-Z	12.1	26.1	850	300	B-EE10-H	12.21	6.60
0 W – 10 W	EE13	PC47EE13-Z	17.1	30.2	1130	517	B-EE13-H	18.43	7.60
0 W – 10 W	EE16	PC47EE16-Z	19.2	35.0	1140	795	B-EE16-H	14.76	8.50
0 W – 10 W	EE19	PC47EE19-Z	23.0	39.4	1250	954	B-EE19-H	29.04	8.80
10 W – 20 W	EE22	PC47EE22-Z	41.0	39.4	1610	1620	B-EE22-H	19.44	8.45
10 W – 20 W	EE25	PC47EE25-Z	41.0	47.0	2140	1962	B-EE25-H	62.40	11.60
20 W – 50 W	EE30	PC47EE30-Z	111.0	58.0	4690	6290	B-EE30-H		13.20
0 W – 10 W	RM5	PC95RM05Z	24.8	23.2	2000	574	B-RM05-V		4.90
10 W – 20 W	RM6	PC95RM06Z	37.0	29.2	2150	1090	B-RM06-V		6.20
20 W – 30 W	RM8	PC95RM08Z	64.0	38.0	5290	2430	B-RM08-V	30.00	8.80
30 W – 50 W	RM10	PC95RM10Z	96.6	44.6	4050	4310	B-RM10-V		10.00
45 W – 65 W	EQ25	EQ25-3C96	100	41.4	4400	4145	EQ25-15.5 A-4P-TH-J-12	34.83	8.1
50 W – 70 W	PQ26/20	PC95PQ26/20Z-12	119	46.3	7470	5490	BPQ26/20-1112CPFR	30.7	9.2

Table 8. Commonly Available Cores and Power Levels at Which These Cores Can be used for Typical Designs.

Maximum Flux Density, BMAX (Gauss)
The low frequency operation resulting from a light load condition can generate frequency components in the audible range within the transformer, especially if a long core is used. To limit audible noise, the transformer should be designed such that the maximum core flux density is below 3000 Gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing will largely eliminate audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

AC Flux Density, BAC (Gauss)
The BAC value can be used for calculating core loss.

Primary Layers, LAYERS_PRIMARY
By default, if the override cell is empty, a value of 3 is assumed. Primary layers should be in the range of $1 \leq L \leq 3$, and in general they should meet the current capacity guideline of 200 – 500 circular mils/ ampere for designs without forced air cooling. Primary winding wire gauge AWG_PRIMARY is calculated in cell [L152]. Values above 3 layers are possible but the increased leakage inductance and physical fit of the windings should be considered. A split primary construction may be helpful for designs where clamp dissipation leakage inductance is too high. In this case half of the primary winding is placed on either side of the secondary (and bias) windings in a sandwich arrangement.

Primary Winding Wire Gauge, AWG_PRIMARY (AWG)
By default, if the override cell is empty, double insulated wire is assumed and a standard wire diameter is chosen. The grey override cells can be used to enter the wire gauge, or if the wire used is different from the standard double insulated type.

Secondary Turns, NSECONDARY
By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the peak operating flux density BPEAK is kept below the recommended maximum of 3800 Gauss (380 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired.

Bias Turns, NBIAS
Determined based on VBIAS set voltage or secondary turns. This parameter is calculated based on the PDO with minimum VOUT (typically 5 V PDO) to obtain the target VBIAS in line [L180].

The other transformer parameters that are automatically calculated by the spreadsheet include:

OD_PRIMARY_INSULATED (mm), Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE (mm), Outer diameter without insulation
CMA_PRIMARY (Cmil/A), Winding CMA
OD_SECONDARY_INSULATED (mm), Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE (mm), Outer diameter without insulation
CMA_ SECONDARY (Cmil/A), Winding CMA

Step 5 – Primary and Secondary Components Selection

Enter: BROWN-IN REQUIRED, VBIAS, VF_BIAS, SRFET

169	**PRIMARY COMPONENTS SELECTION**					
170	**LINE UNDERVOLTAGE**					
171	BROWN-IN REQURED	**68.00**		68.00	V	Required line brown-in threshold
172	RLS			3.56	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
173	BROWN-IN ACTUAL			67.67	V	Actual brown-in threshold using standard resistors
174	BROWN-OUT ACTUAL			59.62	V	Actual brown-out threshold using standard resistors
175						
176	**LINE OVERVOLTAGE**					
177	OVERVOLTAGE_LINE			297.50	V	Actual AC RMS line over-voltage threshold
178						
179	**BIAS WINDING**					
180	VBIAS	**9.00**		9.00	V	Rectified bias voltage at the lowest output set-point
181	VF_BIAS			0.70	V	Bias winding diode forward drop
182	VREVERSE_BIASDIODE			158.32	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS			22	uF	Bias winding rectification capacitor
184	CBPP			4.70	uF	BPP pin capacitor
185						
186						
187						
188	**SECONDARY COMPONENTS SELECTION**					
189	**RECTIFIER**					
190	VDRAIN_OFF_SRFET			70.77	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	**AONS62922**		AONS62922		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V

Figure 9. Primary and Secondary Components Section of InnoSwitch3-PD PIXIs Spreadsheet.

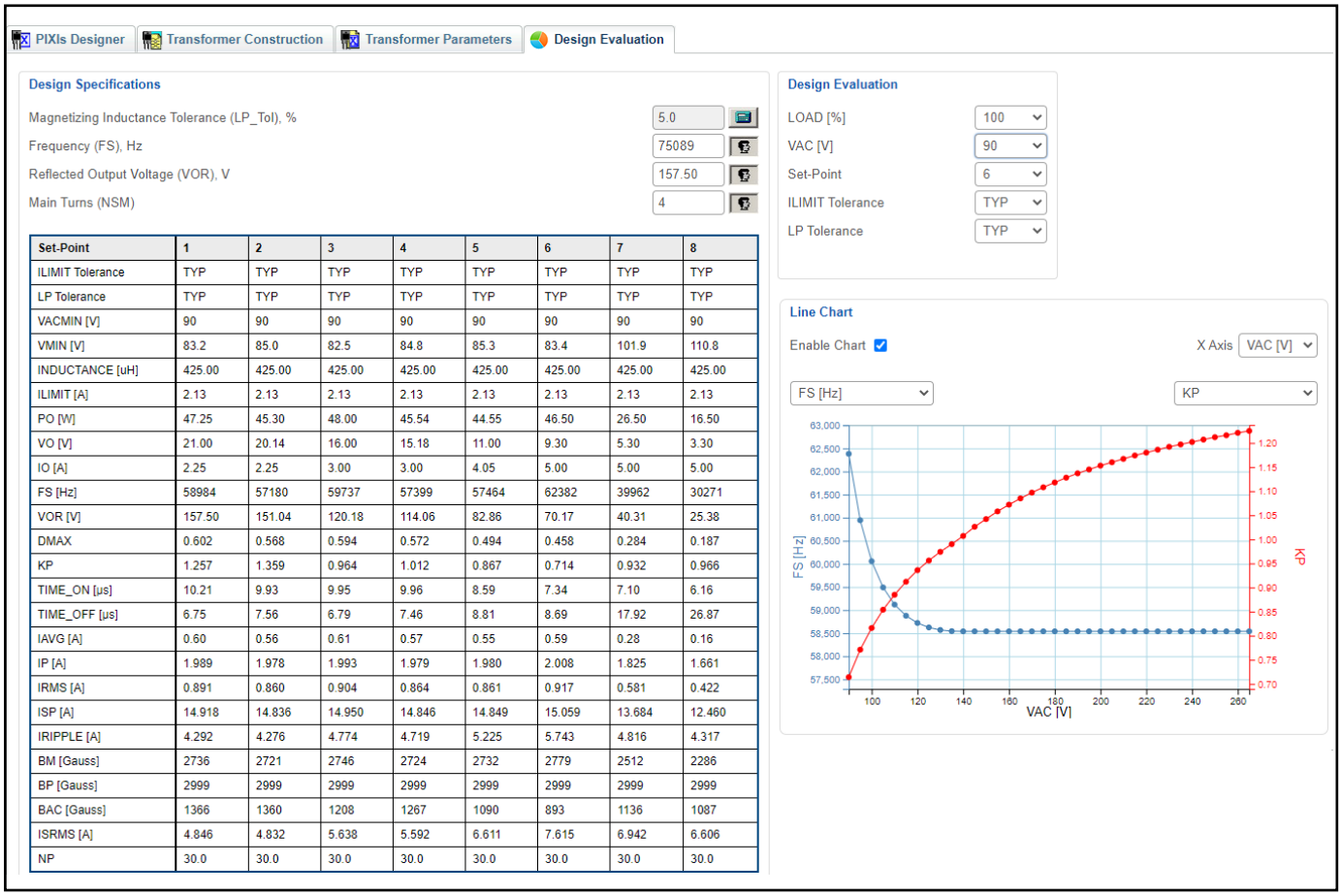
Required Line Undervoltage Brown-in, BROWN-IN REQUIRED
This is the input AC voltage at which the power supply will turn on (once the brown-in threshold (IUV+) is exceeded). The typical value is 20% below minimum AC input voltage (VIN_MIN). The brown-in voltage can be changed to a specific voltage required in cell [L171].

Line Undervoltage / Overvoltage Sense Resistor, RLS
PIXIs will calculate the resistance value based on the brown-in voltage. Shown as RLS1 + RLS2 on Figure 1, they are typically connected after the bridge rectifier. Typical total value for RLS1 + RLS2 is 3.8 MΩ. RLS is approximately equal to $V_{BROWN-IN}$ × 1.414 / IUV+.

Bias Diode Forward Drop, VF_BIAS
A default value of 0.7 V is used though this can be changed to match the type of diode used for rectifying the bias winding.

Synchronous Rectifier MOSFET, SRFET
A selection of synchronous rectifier MOSFETs (SRFET) are provided in the drop-down menu. Based on the SR FET chosen, the breakdown voltage, VBREAKDOWN_SRFET (V), and on-time drain resistance, RDSON_SRFET (mΩ) will be displayed in the spreadsheet.

Step 6 – Design Evaluation



Set-Point	1	2	3	4	5	6	7	8
ILIMIT Tolerance	TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP
LP Tolerance	TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP
VACMIN [V]	90	90	90	90	90	90	90	90
VMIN [V]	83.2	85.0	82.5	84.8	85.3	83.4	101.9	110.8
INDUCTANCE [uH]	425.00	425.00	425.00	425.00	425.00	425.00	425.00	425.00
ILIMIT [A]	2.13	2.13	2.13	2.13	2.13	2.13	2.13	2.13
PO [W]	47.25	45.30	48.00	45.54	44.55	46.50	26.50	16.50
VO [V]	21.00	20.14	16.00	15.18	11.00	9.30	5.30	3.30
IO [A]	2.25	2.25	3.00	3.00	4.05	5.00	5.00	5.00
FS [Hz]	58984	57180	59737	57399	57464	62382	39962	30271
VOR [V]	157.50	151.04	120.18	114.06	82.86	70.17	40.31	25.38
DMAX	0.602	0.568	0.594	0.572	0.494	0.458	0.284	0.187
KP	1.257	1.359	0.964	1.012	0.867	0.714	0.932	0.966
TIME_ON [µs]	10.21	9.93	9.95	9.96	8.59	7.34	7.10	6.16
TIME_OFF [µs]	6.75	7.56	6.79	7.46	8.81	8.69	17.92	26.87
IAVG [A]	0.60	0.56	0.61	0.57	0.55	0.59	0.28	0.16
IP [A]	1.989	1.978	1.993	1.979	1.980	2.008	1.825	1.661
IRMS [A]	0.891	0.860	0.904	0.864	0.861	0.917	0.581	0.422
ISP [A]	14.918	14.836	14.950	14.846	14.849	15.059	13.684	12.460
IRIPPLE [A]	4.292	4.276	4.774	4.719	5.225	5.743	4.816	4.317
BM [Gauss]	2736	2721	2746	2724	2732	2779	2512	2286
BP [Gauss]	2999	2999	2999	2999	2999	2999	2999	2999
BAC [Gauss]	1366	1360	1208	1267	1090	893	1136	1087
ISRMS [A]	4.846	4.832	5.638	5.592	6.611	7.615	6.942	6.606
NP	30.0	30.0	30.0	30.0	30.0	30.0	30.0	30.0

Figure 10. Set-point Analysis Section of InnoSwitch3-PD Design Spreadsheet.

The Design Evaluation tab of the InnoSwitch3-PD PIXIs provides calculated results for multiple parameters when the power supply is operating at different set-points and tolerance conditions.

To use this feature, the Design Evaluation parameters LOAD [%], VAC [V], Set-Point, ILIMIT Tolerance, and LP Tolerance can be configured to the desired value, available from their respective drop-down lists. When any of these parameters is changed, PIXIs automatically calculates the corresponding parameters for all set-points and results are displayed on the table on the left side.

The Line Chart section also displays the trend of two result parameters (selected with drop-down lists) versus either VAC [V] or Load [%]. The data points on the Line Chart corresponds to the selected conditions in the Design Evaluation parameters, only for the selected set-point.

All information in the Design Evaluation tab allows the designer to have an insight on how the power supply will operate even before the first hardware prototype has been created. The results are based on calculations and approximations, so actual results may vary. The power supply designed using the InnoSwitch3-PD PIXIs should be tested to verify actual parameter values.

Critical External Components Selection

The schematic in Figure 11 shows the key external components for a practical 45 W single output InnoSwitch3-PD design.

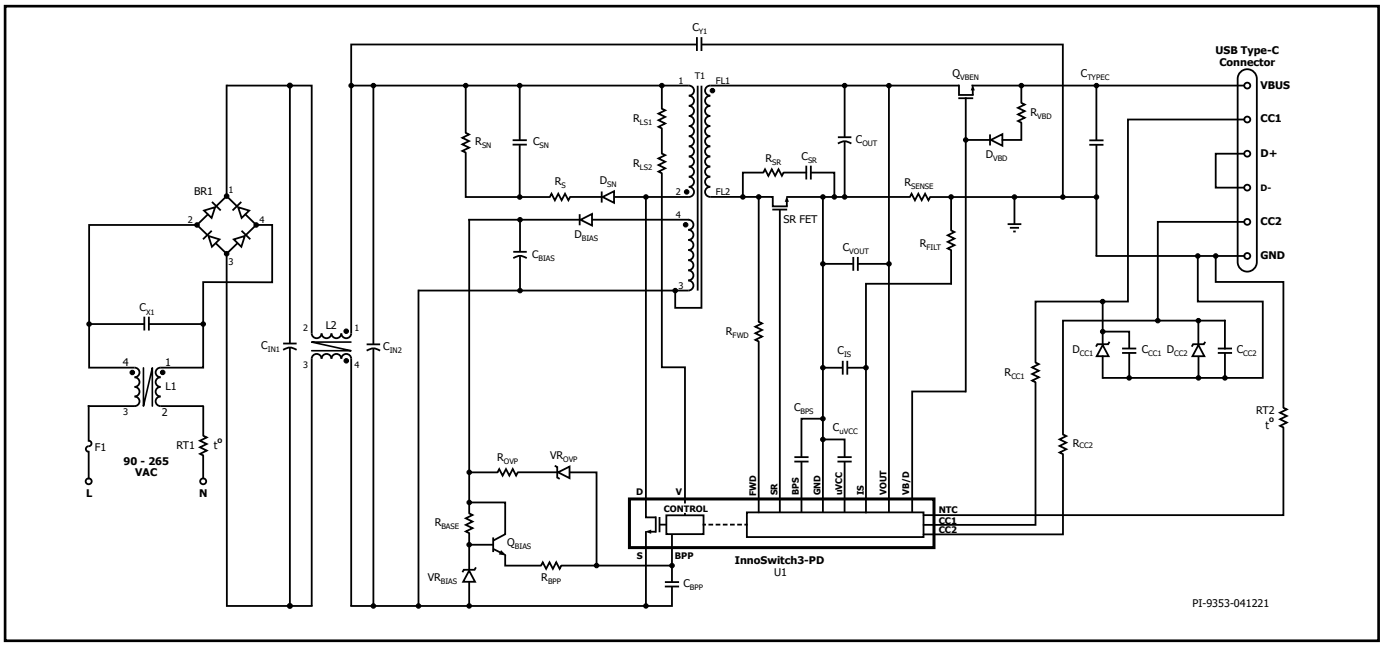


Figure 11. Typical 45 W USB Power Delivery Flyback Power Supply using InnoSwitch3-PD.

PRIMARY BYPASS Pin Capacitor (CBPP)

This capacitor works as a supply decoupling capacitor for the internal primary-side controller and determines current limit for the internal power switch. A 0.47 µF or 4.7 µF capacitor selects either standard or increased current limit, respectively. Although electrolytic capacitors can be used, surface mount multi-layer ceramic capacitors are often preferred for use with double sided boards as they enable the capacitor to be placed close to the IC. A surface mount multi-layer ceramic X7R capacitor rated for 25 V is recommended.

To ensure correct current limit, it is recommended that only 0.47 µF or 4.7 µF capacitors be used. In addition, the BPP capacitor tolerance should be equal or better than indicated below, taking into account the ambient temperature range of the target application. The minimum and maximum acceptable capacitor tolerance values are set by IC characterization (Table 9).

Nominal PRIMARY BYPASS Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	+100%

Table 9. BYPASS Pin Capacitor Tolerance Values.

Primary Clamp Network Across Primary Winding (D_{SN}, R_S, R_{SN}, and C_{SN})

An R2CD clamp is the most commonly used clamp in low-power supplies. For higher power designs, a Zener clamp or the R2CD + Zener clamp can be used to increase efficiency. It is advisable to limit the peak drain voltage to 90% of BV_{DSS} under worst-case conditions (maximum input voltage, maximum overload power or output short-circuit).

In Figure 11, the clamp diode, D_{SN} must be a standard recovery glass-passivated type or a fast recovery diode with a reverse recovery time of less than 500 ns. The use of standard recovery glass passivated diodes allows recovery of some of the clamp energy in each switching cycle and helps improve average efficiency. The diode conducts momentarily each time the FET inside the InnoSwitch3-PD turns off and energy from the leakage reactance is transferred to the clamp capacitor C_{SN}. Resistor R_S, which is in the series path, offers damping, preventing excessive ringing due to resonance between the leakage reactance and the clamp capacitor C_{SN}. Resistor R_{SN} bleeds-off energy stored inside the capacitor C_{SN}. Capacitor C_{SN}, and resistors R_S and R_{SN} must therefore be optimized for each design.

As a general rule it is advisable to minimize the value of capacitor C_{SN} and maximize the value of resistor R_{SN}, while still meeting the 90% BV_{DSS} limit at highest input voltage and full load. The value of R_S should be large enough to damp the ringing in the required time, but not too large such that the drain voltage exceeds 90% of BV_{DSS}.

A ceramic capacitor that uses a dielectric such as Z5U when used in clamp circuit for C_{SN} may generate audible noise, so a polyester film type is a better alternative. Another option is to use ceramic capacitors specifically designed to have low acoustic noise. It is generally preferable to use an SMD ceramic capacitor for C_{SN} to maintain a compact loop for the primary clamp circuit and have a small overall form factor, but it must be confirmed that audible noise requirements for the design are also achieved.

As a guide the following equations can be used to calculate R2CD component values:

$$R_{SN} = \left[\frac{V_C^2}{\frac{1}{2} L_{IK} \times I_{PK}^2 \times \frac{V_C \times F_{SW}}{V_C - V_{OR}}} \right]$$

$$C_{SN} = \frac{V_C}{R_{SN} \times F_{SW} \times dV_{CSN}}$$

$$R_S = \left(\frac{L_{IK}}{C_{SN}}\right)^{\frac{1}{2}}$$

The primary clamp circuit component values can then be tuned once the hardware prototype has been built to meet primary switch peak drain voltage, EMI, and efficiency performance requirements.

Where;

V_C: Voltage across clamp circuit
I_{PK}: Peak switching current
F_{SW}: Switching frequency
L_{IK}: Leakage inductance
V_{OR}: Reflected output voltage
dV_{CSN}: Maximum ripple voltage across clamp capacitor (10%).

Common Primary Clamp Configurations

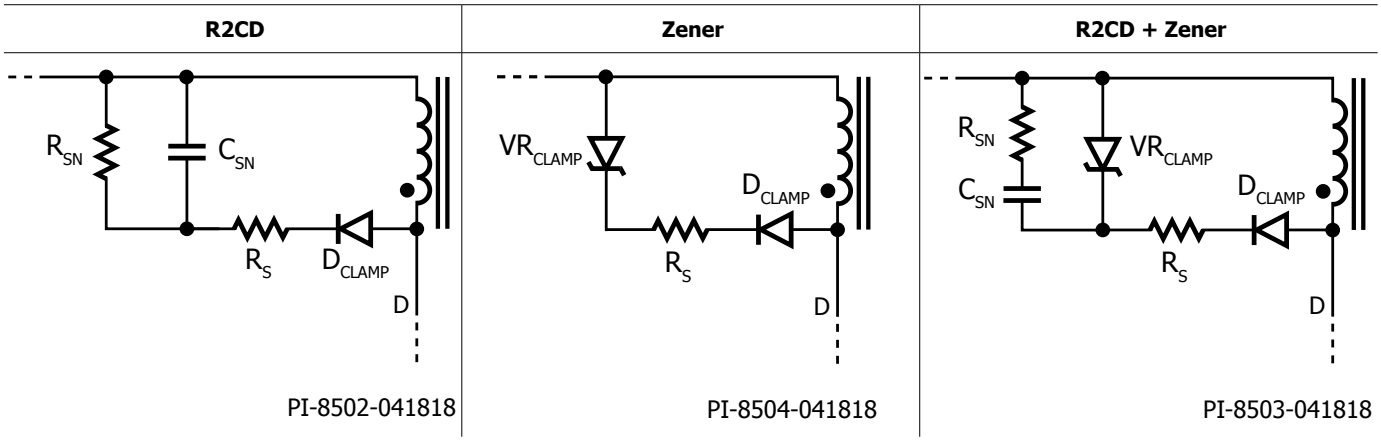


Figure 12. Recommended Primary Clamp Components.

Primary Clamp Circuit

Benefits	R2CD	Zener	R2CD + Zener
Component Cost	Low	Medium	High
No-Load Input Power	High	Low	Medium
Light-Load Efficiency	Low	High	Medium
EMI Suppression	High	Low	Medium

Table 10. Benefits of Primary Clamp Circuits.

External Bias Supply Components (D_{BIAS}, C_{BIAS}, R_{BPP}, R_{BASE}, Q_{BIAS}, VR_{BIAS})

InnoSwitch3-PD can operate even if the IC primary-side is not externally powered. The primary controller has a high voltage internal regulator that can draw current from the Drain pin to charge the BYPASS pin (BPP) capacitor to VBPP whenever the power MOSFET is off. When the power MOSFET is on, the device operates from the energy stored in the BPP capacitor. However, to achieve best-in-class no-load input power and efficiency performance, it is recommended that an external bias circuit which injects sufficient current into BPP such that the high voltage internal regulator does not need to turn on after start-up is used. The no-load consumption can be reduced to less than 20 mW in a 45 W output design when the InnoSwitch3-PD is powered externally through an optimized bias circuit and other design guidelines for minimum no-load input power in this document are followed.

The bias circuit consists of the transformer bias winding (N_{BIAS}), bias diode (D_{BIAS}), bias supply filter capacitor (C_{BIAS}), and a BPP current-limiting element using either a single resistor (R_{BIAS}) or a linear regulator circuit (Q_{LIN}, VZ_{LIN}, R_{ZLIN}, R_{LIN}, R_{BIAS}) as shown in Figures 13 and 14.

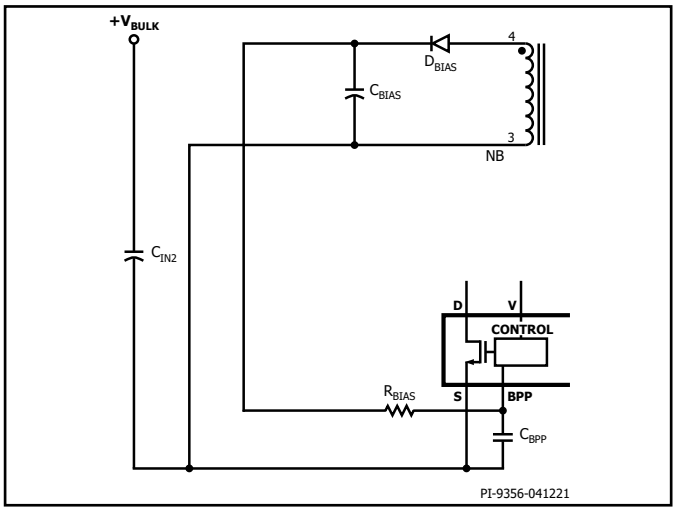


Figure 13. External Bias Circuit using Single Resistor.

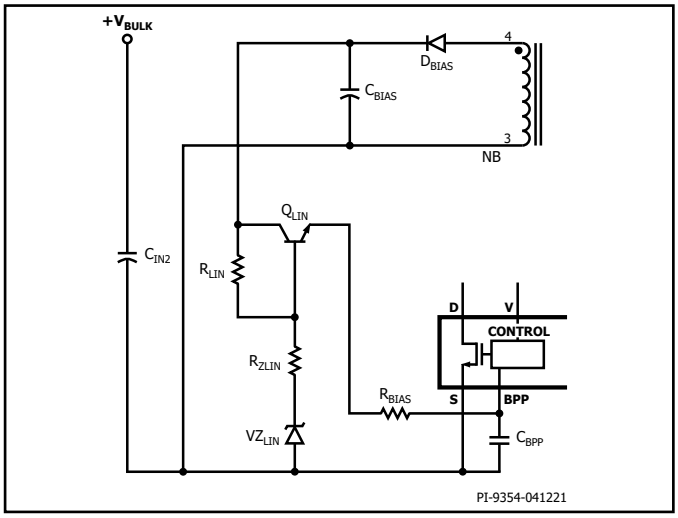


Figure 14. External Bias Circuit using Linear Regulator with Positive Slope (slope controlled by R_{ZLIN}).

For both configurations, the two main design goals are to:

- Supply enough current into BPP at no-load (I_{BPP} > 425 µA) and during normal operation (IBPP will depend on operating switching frequency) such that the high voltage internal regulator does not need to turn on.
- Ensure that the current injected into the BPP pin during normal operation does not exceed the BYPASS shutdown threshold current (I_{SD}), which will trigger a latch-off.

The transformer bias winding turns (N_{BIAS}) and bias filter capacitor (C_{BIAS}) must be chosen such that the bias voltage V_{BIAS} (voltage across C_{BIAS}) is about 8 V at the no-load condition. A 22 µF, low ESR electrolytic aluminum capacitor for C_{BIAS} and a 2:1 turns ratio of N_{BIAS} to $N_{SECONDARY}$ are recommended as starting point. Experience has shown that this combination will result in V_{BIAS} close to 8 V at no-load condition without a Type-C cable and a PD Sink at the output.

A lower value for C_{BIAS} will increase the voltage ripple of V_{BIAS} at no-load, making it difficult to meet the BPP current requirement of the primary controller (at least 425 µA). The use of a ceramic surface mount capacitor for C_{BIAS} is also generally not recommended as they can cause audible noise due to piezoelectric effect in their mechanical structure. Also consider that a ceramic capacitor's effective capacitance decreases as the DC bias voltage increases.

The voltage rating of C_{BIAS} will be determined by V_{BIAS} at maximum V_{OUT}, full load. This value will differ based on the type of bias diode rectifier D_{BIAS} due to the poor voltage regulation of V_{BIAS}. A standard recovery diode for D_{BIAS} has a relatively flat V_{BIAS} regulation as compared to fast or ultra-fast recovery diode which has an increasing V_{BIAS} versus increasing load current characteristic. The lower worst-case V_{BIAS} using a standard recovery D_{BIAS} may help in compact designs since a smaller size of the electrolytic capacitor for C_{BIAS} may be used.

The reverse-recovery current of a standard recovery diode may help dampen ringing during switching transients and improve EMI performance. On the other hand, a fast or ultrafast recovery diode may help to slightly improve efficiency due to lower recovery losses. Select the diode type for D_{BIAS} which best suits the design application.

After selecting N_{BIAS}, C_{BIAS}, and D_{BIAS}, use Table 11 as a guide for selecting the recommended bias circuit configuration based on design specification. Both circuits will be designed to minimize no-load input power. However, as the operating V_{OUT} is increased, V_{BIAS} also increases and the single resistor bias circuit suffers from wasted power in the bias circuit because the supplied BPP current is much higher than what the primary controller needs. If V_{BIAS} becomes high enough, the BPP shutdown current threshold may even be exceeded which will latch-off the power supply. This behavior worsens with a fast recovery D_{BIAS} due to a higher V_{BIAS} vs. output load characteristic. Therefore, single resistor bias is only recommended for low voltage USB PD designs and with a standard recovery D_{BIAS} as the rectifier.

A linear regulator circuit has the advantage of controlling the supplied BPP current to a value just slightly higher that the amount the primary controller requires – even for 21 V output operation. For best efficiency, the linear regulator bias circuit must be used even for low power USB PD designs with only 9 V and 5 V outputs.

	Single Resistor Bias Current	Linear Regulator Bias Current
No-Load Power	(same)	
Average and 10% Load Efficiency	✓	✓✓
Design simplicity, component count	✓✓	✓
Highest V_{OUT} of InnoSwitch3-PD design	Limited to 11 V output for standard recovery D_{BIAS}. Not recommended with fast recovery D_{BIAS}	Up to 21 V

Table 11. Overview of Single Resistor and Linear Regulator Bias Circuits.

The external BPP current that the primary controller requires must first be calculated in order to select the remaining component values of the bias circuit. This value is determined by the operating switching frequency as shown in the following equation.

$$I_{BPP(REQ)} = I_{S1} + (I_{S2} - I_{S1})\left(\frac{F_{SW}}{132\ kHz}\right)$$

Where
I_{BPP_REQ}: Required BPP supply current at F_{SW}
F_{SW}: Operating switching frequency (kHz)
I_{S1}: BPP supply current at no switching (refer to data sheet)
I_{S2}: BPP supply current at 132 kHz (refer to data sheet)

Calculate the required BPP current at no-load and for all set-points at full load. Use the data sheet maximum values of I_{S1} and I_{S2}. For the no-load condition when switching frequency is extremely low, the required BPP current can be approximated as I_{S1} (425 µA).

The Design Evaluation tab of the spreadsheet can be used to obtain the corresponding worst-case switching frequency for each set-point at full load. Ensure that the lowest VAC input, minimum ILIMIT, and minimum LPRIMARY are selected to get the worst-case switching frequency of the set-points.

The single resistor bias circuit is used, R_{BIAS} is chosen to minimize power consumption at no-load as shown in the equation below.

Hardware prototype measurement of V_{BIAS} at no-load is preferred. This must be taken without the Type-C cable and PD Sink at the output as this is the true no-load condition. Whenever sufficient current is supplied to the BPP, the pin voltage will be internally clamped to V_{SHUNT} (5.36 V typical) and the high voltage internal regulator will not need to turn on. Otherwise, the pin voltage will be equal to VBPP (4.90 V typical). These two voltage levels can be used as an indicator of whether or not the internal regulator is drawing current from the DRAIN pin to keep the primary controller operational.

$$R_{BIAS} = \frac{V_{BIAS(No\text{-}Load)} - V_{SHUNT}}{450\ \mu A}$$

With a single resistor bias circuit, there is no other way to limit the supplied BPP current as the output voltage and V_{BIAS} increases, because the R_{BIAS} is optimized for no-load performance. Verify that the supplied BPP current at maximum VOUT and full load is less than the ISD threshold with enough margin to prevent latch-off during normal operation.

If a linear regulator bias circuit is used, R_{BIAS} is also chosen to minimize no-load power consumption and can be estimated using the equation below.

$$R_{BIAS} = \frac{V_{BIAS(No\text{-}Load)} - 0.6\ V - V_{SHUNT}}{450\ \mu A}$$

At no-load, the Zener VZ_{LIN} is expected to be off and resistor R_{LIN} provides the base current needed by transistor Q_{LIN} to supply 450 µA into the BPP pin. Q_{LIN} can be a general purpose low-cost NPN transistor with voltage rating higher than the worst-case V_{BIAS}. The value of R_{LIN} must be high enough to have a low dissipation at maximum V_{BIAS} but must also support the transistor base current needed to generate 450 µA of emitter current at the no-load condition. R_{LIN} can be set to 100 kΩ as a starting value.

The values of VZ_{LIN} and R_{ZLIN} will depend on the slope characteristic of required BPP current for all set-points at full-load. Figure 15 illustrates two possible cases. For a 45 W / 5 A USB PD design, there could be multiple set-points corresponding to almost 45 W output (9 V / 5 A to 21 V / 2.25 A). Since BPP current requirement is directly proportional to switching frequency, all 45 W set-points would result in approximately constant BPP current requirement from 9 V to 21 V set-points. However, in a 60 W / 3 A USB PD design, the output power generally increases with the set-point voltage. This results in a linearly increasing BPP current requirement.

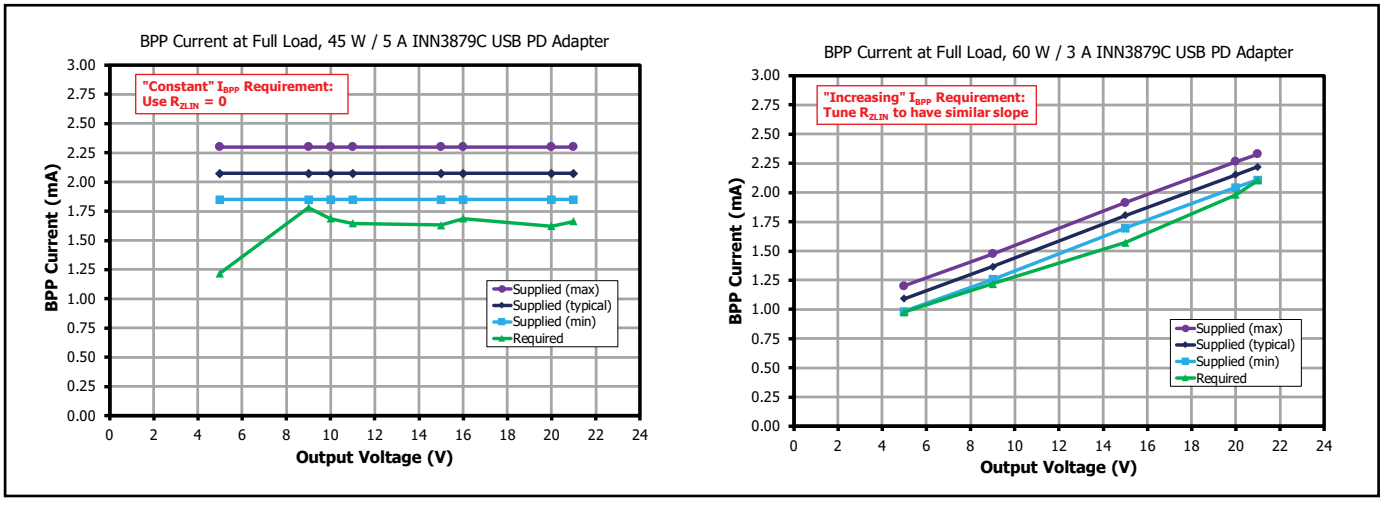


Figure 15. Effect of RZLIN of Linear Regulator Bias Circuit to the Supplied BPP Current.

For USB PD designs with constant BPP current requirement, RZ_{LIN} must be set to 0 so that the supplied BPP current is also constant. VZ_{LIN} must be chosen such that the highest BPP current requirement ($I_{BPP_REQ(MAX)}$) of the design is satisfied even at the lower end of the Zener voltage tolerance. Use the equation below to select V_{ZLIN} (±5% voltage tolerance can be used).

$$VZ_{LIN} = \frac{I_{BPP_REQ(MAX)} \times R_{BIAS} + 0.6\ V + V_{SHUNT}}{0.95}$$

$$R_{ZLIN} = 0$$

For USB PD designs with increasing BPP current requirement, use the equations below for the initial values of VZ_{LIN} and R_{ZLIN}.

$$VZ_{LIN} = \frac{I_{BPP_REQ(5\ V)} \times R_{BIAS} + 0.6\ V + V_{SHUNT}}{0.95}$$

$$R_{ZLIN} = \left(\frac{I_{BPP_REQ(MAX)} \times R_{BIAS} + 0.6\ V + V_{SHUNT} - 0.95 \times VZ_{LIN}}{V_{BIAS(MAX)} - I_{BPP_REQ(MAX)} \times R_{BIAS} - 0.6\ V - V_{SHUNT}} \right) \times R_{LIN}$$

Where

$I_{BPP_REQ(5V)}$: Required BPP supply current at 5 V set-point
$V_{BIAS(MAX)}$: Maximum voltage across CBIAS, typically at maximum VOUT, full load
V_{SHUNT}: BPP internal clamp voltage (5.36 V typical) when current is provided into BPP

Verify the hardware performance particularly the supplied BPP current at no-load condition without the Type-C cable and PD Sink at the output. A BPP current below 425 µA at no-load should never be used as this might result in the high voltage internal tap turning on, increasing no-load consumption. Iterate the bias circuit design until the no-load consumption and efficiency requirements have been achieved.

Primary-Sensed Overvoltage Protection (VR_{OVP}, R_{OVP})

Primary-side output overvoltage protection provided by the InnoSwitch3-PD IC uses an internal latch-off that is triggered by a threshold current of ISD flowing into the PRIMARY BYPASS pin. For the bypass capacitor to be effective as a high frequency filter, the capacitor (C_{BPP}) should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

Primary-sensed output OVP can be realized by connecting a series resistor (R_{OVP}) and a Zener diode (VZ_{OVP}) from the rectified and filtered bias winding voltage supply (C_{BIAS}) to the PRIMARY BYPASS pin as shown in Figure 16. The voltage across C_{BIAS} may be higher than expected depending on the bias diode D_{BIAS} recovery type (fast and ultra-fast recovery diodes result in higher V_{BIAS} than standard recovery diodes), coupling of the bias winding with the output winding, and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. Ideally this measurement should be made at the lowest input voltage, with full output load and highest output voltage. This measured voltage should be used to select the components required to provide primary sensed OVP.

It is recommended that the Zener diode VZ_{OVP} be selected with a clamping voltage approximately 6 V lower than the rectified voltage of the bias winding at which OVP is expected to be triggered. Finally, series resistor R_{OVP} can be set to a small value such as 47 Ω, which can cause a current higher than I_{SD} to be injected into the PRIMARY BYPASS pin during an output overvoltage event.

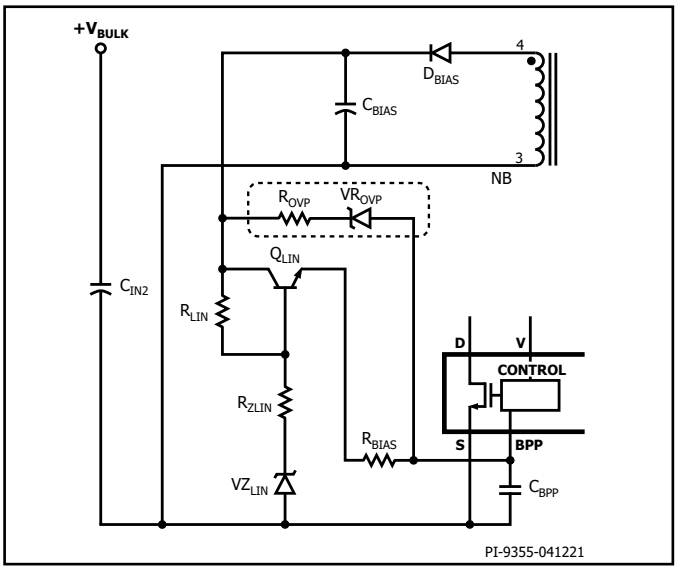


Figure 16. Primary-Sensed Output OVP using Zener Diode and Series Resistor from C_{BIAS} to PRIMARY BYPASS Pin.

SECONDARY BYPASS Pin Capacitor (C_{BPS})

This capacitor works as a supply decoupling capacitor for the secondary-side controller. A surface mount, 2.2 µF, 25 V, multi-layer ceramic capacitor is recommended for satisfactory operation of the IC. The SECONDARY BYPASS Pin voltage needs to reach 4.4 V before the output voltage reaches its target voltage. A significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 µF will cause unpredictable operation. The capacitor must be located adjacent to the IC pins. The 25 V rating is necessary to guarantee sufficient capacitance in operation (the capacitance of ceramic capacitors drops with applied voltage). 10 V rated capacitors are not recommended for this reason. For best results capacitors with X7R or X5R dielectrics should be used.

Output Synchronous Rectifier MOSFET (SR FET)

InnoSwitch3-PD features a built-in synchronous rectifier (SR) driver that enables the use of low-cost low voltage MOSFETs for synchronous rectification and increases system efficiency. Since the SR driver is referenced to the output GND, the SR FET is placed in the return line. GND is the typical threshold that ensures the SR FET will turn off ($V_{SR(TH)}$) at the end of the flyback conduction time. There is a slight delay between the commencement of the flyback cycle and the turn on of the SR FET in order to avoid current shoot through. During SR FET conduction the energy stored in the inductor is transferred to the load, the current will continue to drop until the voltage across the $R_{DS(ON)}$ of the SR FET drops to 0 V. At this point the SYNCHRONOUS RECTIFIER pin will pull the gate low to instantaneously turn off the SR FET. Minimal current will flow through the SR FET body diode during the remainder of the flyback time (see Figure 17). Putting a Schottky diode across the SR FET may increase efficiency by 0.1% – 0.2% depending on the design and SR FET used. In continuous conduction mode (CCM), the SR FET is turned off when a feedback pulse is sent to the primary to demand a switching cycle.

The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. An SR FET with a high threshold voltage is therefore not suitable. SR FETs with a gate voltage threshold voltage range ($V_{GS(TH)}$) of 1.5 V to 2.5 V are recommended.

Since the termination of the ON-time of the SR FET is based on when the Drain-Source voltage of the FET reaches 0 V during the conduction cycle, using an SR MOSFET with ultra-low $R_{DS(ON)}$ (< 5 mΩ) may result to early termination of the SR FET drive signal. This will cause secondary current to instead conduct through the body diode of the SR FET, which has a higher voltage drop compared to the SR FET's $R_{DS(ON)}$ and may therefore cause a slight reduction in system efficiency (see Figure 18).

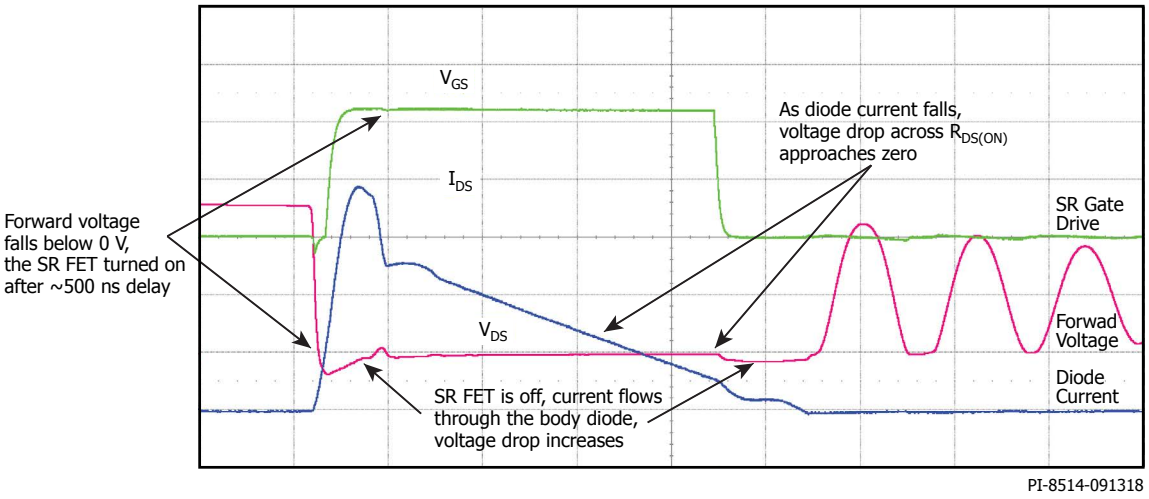


Figure 17. SR FET Turn-ON and Turn-OFF events during DCM Operation.

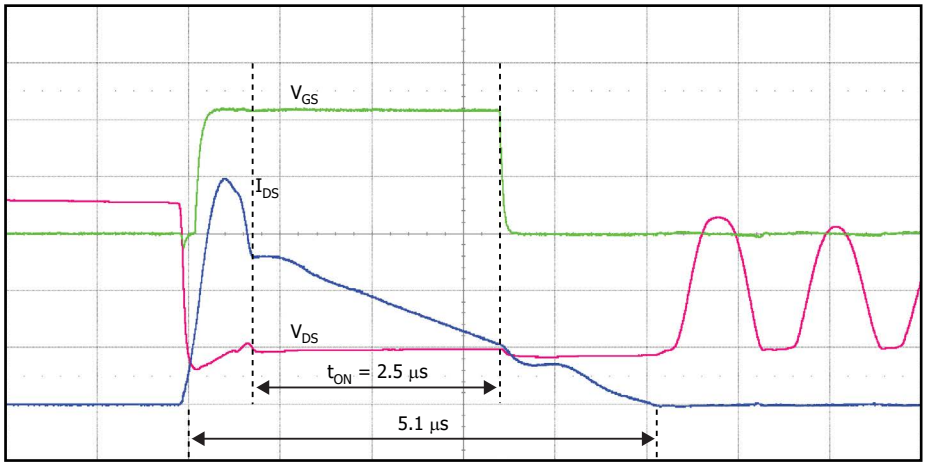


Figure 18. Effect of $R_{DS(ON)}$ on SR FET Conduction Time.

The recommended optimum SR FET Drain-to-Source on-resistance ($R_{DS(ON)}$) is approximately.

$$R_{DS(ON)} \approx \frac{0.16 \times V_O}{I_P \times VOR}$$

Some SR FETs, suitable for synchronous rectification and which meet the criteria described in this section is shown in Table 12.

The voltage rating of the SR FET should be at least 1.3 times the expected peak inverse voltage (PIV). The spreadsheet estimates the SR FET PIV by adding two voltages: voltages: (1) DC output voltage, and (2) the applied maximum input DC bus voltage multiplied by the primary-to-secondary turns ratio of the transformer. This value is displayed as VDRAIN_OFF_SRFET [L190]. To get the total PIV, the value in [L190] should be added to the peak of the parasitic ringing voltage on the secondary seen during SR FET turn-off. The parasitic ring voltage and the total SR FET PIV should still be measured to confirm that there is sufficient margin for the BV_{DSS} of the SR FET and the antiparallel diode (if used).

The SR FET provides significant efficiency improvement without a cost penalty due to the low cost of low voltage MOSFETs. It is possible to use a Schottky or fast-recovery diode for output rectification, by shorting gate drive SYNCHRONOUS RECTIFIER pin to secondary ground. This may be preferred for high-voltage output.

The DC current rating of MOSFET needs to be >2 times higher than the average output current. Depending on the temperature rise and the duration of a peak load condition, it may be necessary to increase the SR FET current rating and heat dissipation area once the prototype has been built.

At the instance of voltage reversal across the primary winding due to primary FET turn-on, the interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform. This ringing can be suppressed using a RC snubber connected across the SR FET. A snubber resistor of 10 Ω to 47 Ω may be used (higher resistance values will lead to a noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

Part	PIV	I_{DRAIN}	$V_{GS(TH)}$ Max	$V_{GS(TH)}$ Min	C_{ISS}	C_{RSS}	C_{RSS}/C_{ISS}	RG	$R_{DS(ON)}$	T_{RR}	Package	Manufacturer
	(V)	(A)	(V)	(V)	(pF)	(pF)	(%)	(Ω)	(Ω)	(ns)		
AO4260	60	18	2.4	1.3	4940	32	0.65	0.9	6.3	22	8-SOIC (0.154", 3.90 mm Width)	Alpha & Omega
AO4264	60	12	2.5	1.4	2007	12.5	0.62	1.2	13.5	15	8-SOIC (0.154", 3.90 mm Width)	Alpha & Omega
AON6244	60	85	2.5	1.5	3838	14.5	0.38	1	6.2	17	8-PowerSMD, Flat Leads	Alpha & Omega
AON6266	60	30	2.5	1.5	1340	10	0.75	1.5	19	17	8-PowerSMD, Flat Leads	Alpha & Omega
AON7246	60	34.5	2.5	1.5	1340	10	0.75	1.5	19	15	8-PowerVDFN	Alpha & Omega
AO4294	100	11.5	2.4	1.4	2420	11	0.45	0.6	15.5	25	8-SOIC (0.154", 3.90 mm Width)	Alpha & Omega
AON7292	100	23	2.6	1.6	1170	8	0.68	0.7	32	24	8-WDFN Exposed Pad	Alpha & Omega
AO4292	100	8	2.7	1.6	1190	7	0.59	3	33	20	SOIC-8	Alpha & Omega
AO4294	100	11.5	2.4	1.4	2420	11	0.45	3	15.5	25	SOIC-8	Alpha & Omega
AO4296	100	13.5	2.3	1.3	3130	12.5	0.4	3	10.6	28	SOIC-8	Alpha & Omega
AOD294A	100	55	2.5	1.5	2305	11.5	0.5	3	15.5	30	TO-252	Alpha & Omega
AOD296A	100	70	2.3	1.3	3130	12.5	0.4	3	10.6	30	TO-252	Alpha & Omega
AOD2910	100	31	2.7	1.6	1190	7	0.59	3	33	30	TO-252	Alpha & Omega
AOD2916	100	25	2.7	1.6	870	3.5	0.4	3	43.5	20	TO-252	Alpha & Omega
AON6220	100	48	2.3	1.3	4525	22.5	0.5	1.1	7.4	32	DFN5X6	Alpha & Omega
AOD2544	150	23	2.7	1.7	675	4	0.59	2.9	66	37	TO-252 DPAK	Alpha & Omega
AON7254	150	17	2.7	1.7	675	4	0.59	2.9	66	37	8-WDFN Exposed Pad	Alpha & Omega

Table 12. List of MOSFETs Suitable for Synchronous Rectification.

When the primary MOSFET turns on, a fast-rising voltage is transferred to the secondary via the transformer and appears across the drain-source of the SR FET. This high dv/dt combined with high ratio of C_{GD} to C_{ISS} MOSFET capacitances will induce a gate-source voltage on the SR FET. If the induced gate voltage exceeds the minimum gate threshold voltage, $V_{GS(TH)}$, then it will turn-on the SR FET causing cross-conduction possibly leading to catastrophic failure. The recommended C_{GD} (C_{RSS}), is less than 35 pF, and the ratio of C_{RSS} to C_{ISS} to be less than 0.02.

Another important parameter in the selection of SR FET is the reverse recovery time (T_{RR}) of its body diode. The reverse recovery characteristics of the SR FET's body-diode can influence the level of voltage stress on the drain when the primary FET switches on. As shown in Figure 19, the SR FET with a slow body diode (> 40 ns T_{RR}) has twice the voltage stress compared to the one with a fast body diode. The recommended maximum reverse recovery time (T_{RR}) of the body diode is less than 40 ns.

FORWARD Pin Resistor (R_{FWD})

The FORWARD pin is connected to the Drain terminal of the synchronous rectifier MOSFET (SR FET). This pin is used to sense the drain voltage of the SR FET and allows precise turn-on and turn-off control. This pin is also used to charge the BPS (SECONDARY BYPASS pin) capacitor when the output voltage is lower than the BPS voltage.

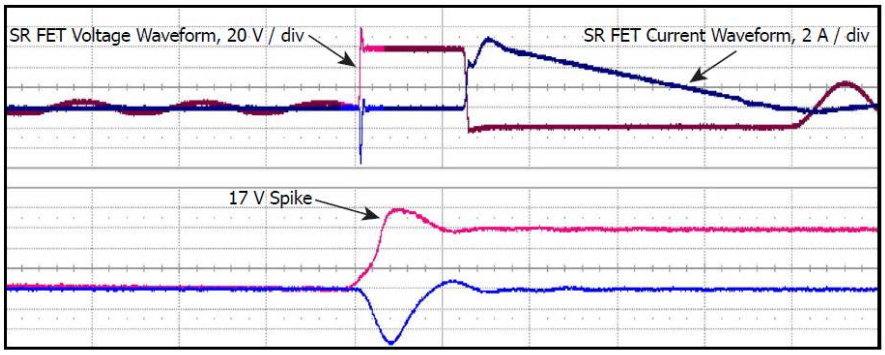
A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current and works for wide range of output voltages. A higher or lower resistor value should not be used as it can affect device operation and effect synchronous rectification timing.

Care should be taken to ensure that the voltage on the FORWARD pin never exceeds its absolute maximum voltage specified in the device data sheet. Since the FORWARD pin monitors the drain voltage of the SR FET, the peak voltage experienced by the FORWARD pin is also the drain-source voltage of the SR FET during turn-off, including the voltage spike. A snubber circuit across the SR FET must be chosen to meet both SR FET drain-source breakdown voltage and the FORWARD pin absolute maximum voltage with enough margin.

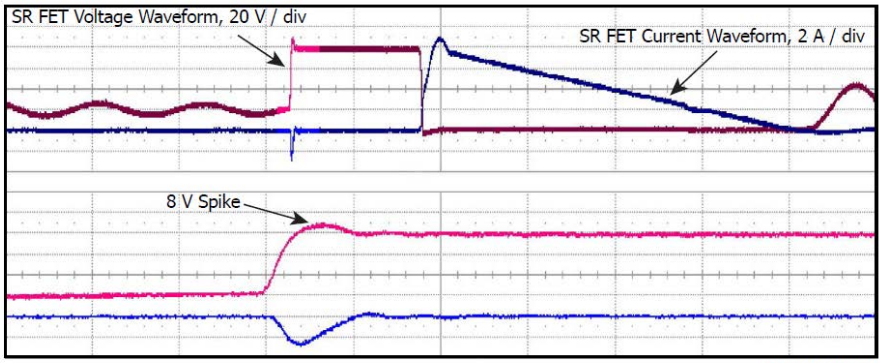
Output Filter Capacitance (COUT)

The current ripple rating of the output capacitor(s) should be greater than the calculated value in the spreadsheet, IRIPPLE_CAP_OUTPUT. If a suitable capacitor cannot be found, then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ripple ratings. Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This is to ensure that the capacitor is not oversized.

The use of aluminum-polymer solid capacitors has gained considerable popularity due to their compact size, stable temperature characteristics; extremely low ESR and high RMS ripple current rating. These capacitors enable the design of ultra-compact chargers and adapters. Typically, 200 µF to 300 µF of aluminum-polymer capacitance per ampere of output current is adequate.



SR FET with slow body diode, showing high-voltage spike, 17 V.



SR FET with fast body diode, significantly low voltage spike, 8 V.

Figure 19. Effect of Body Diode Reverse Recovery Time on VDS.

The other factor that influences choice of the capacitance is allowable output ripple. Ensure that only capacitors with a voltage rating higher than the highest output voltage plus suitable margin are used.

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR. The voltage rating of the capacitor should be at least 1.2 times the output voltage (VOUT).

Output Current Sense Resistor and IS pin filter (R_{SENSE}, R_{FILT}, C_{IS})

The current sense resistor R_{SENSE} is a very small value resistor (typically 9 mΩ or 6 mΩ) used to measure the load current. For constant current (CC) output operation, the voltage across R_{SENSE} is connected to a low-pass filter formed by R_{FILT} and C_{IS}, wherein the capacitor CIS should be directly connected as close as possible to the IS and secondary GND pins of the IC. Because R_{SENSE} has a very small value, the termination and copper traces may change the value as seen by the IS and GND pins. Therefore, it is important to use kelvin-connection from the termination pads of R_{SENSE} to the low-pass filter R_{FILT} and C_{IS}.

The voltage across IS and GND pins (voltage across R_{SENSE} after the low-pass filter) is compared to an internal current limit voltage threshold which is configured by the InnoSwitch3-PD IC up to approximately 32 mV maximum ($I_{SV(TH)}$). Therefore, the maximum available constant current limit or the full-scale constant current of an InnoSwitch3-PD power supply is determined by R_{SENSE} and is given by the equation below.

$$I_{FULLSCALE} = \frac{I_{SV(TH)}}{R_{SENSE}}$$

The full-scale current must always be higher than the maximum rated output current of the power supply. Similarly, at the maximum output current condition, the voltage across IS and GND pins must be close to 32 mV to fully utilize the dynamic range of current sensing.

R_{FLIT} and C_{IS} form a low pass filter to reduce noise at IS and GND pins. Recommended values are 10 Ω 1% for R_{FILT} and 4.7 µF, X7R ceramic capacitor with at least 10 V rating for C_{FILT}. R_{SENSE}, R_{FILT}, and C_{FILT} must be placed close to IS and GND pins with short traces in order to have an accurate constant current limit and to prevent ground impedance noise instability.

Use Table 13 as reference for the recommended R_{SENSE}, R_{FILT}, and C_{FILT} values based on the maximum output current of the power supply.

Maximum Rated I_{OUT}	R_{SENSE}	R_{FILT}	C_{IS}	Full-scale Current (approx)
≤ 3 A	9 mΩ, 1%, ≥ 0.125 W	10 Ω, 1%	4.7 µF, X7R	3.56 A
5 A	6 mΩ, 1%, 0.5 W			5.33 A

Table 13. Recommended R_{SENSE}, R_{FILT}, and C_{IS} Values and Corresponding Full-scale Current.

Accurate current sensing is achieved through a combination of the correct firmware (identified by the device Feature Code in the product data sheet), using its corresponding R_{SENSE} value (9 mΩ for 3 A design, or 6 mΩ for 5 A design), and following the recommended PCB layout presented in the later part of this document (Layout Example). For PCB layouts wherein a significant trace resistance is present resulting into higher effective resistance seen by the IS and GND pins, there could be a shift in output constant current limit accuracy. R_{SENSE} can be adjusted to a different value from Table 12 to compensate for the offset.

VBUS Series Switch and Load Discharge Circuit (Q_{VBEN}, D_{VBD}, R_{VBD})

This VBUS series switch is enabled or disabled by the VB/D pin of the InnoSwitch3-PD IC through firmware. A low-cost, n-channel MOSFET with at least 30 V rating and sufficient continuous drain current rating can be used. A low $R_{DS(ON)}$ (< 10 mΩ) is also preferred to reduce conduction losses. VB/D pin gate drive is typically 4.5 V with respect to VOUT so a gate voltage threshold voltage range ($V_{GS(TH)}$) of 1.5 V to 2.5 V are recommended.

The InnoSwitch3-PD can also discharge the VBUS output voltage by bringing the VB/D pin to ground. The discharge circuit is a series diode + resistor tied from the VBUS output to the VB/D pin shown in the typical application schematic. A low-cost, general purpose diode and a 100 Ω resistor are recommended. This diode and resistor must be placed as close as possible to the bus switch gate-source pins.

VOUT pin Decoupling Capacitor (C_{VOUT})

The VOUT pin should be decoupled to the GND pin with at least 2.2 µF ceramic capacitor.

uVCC pin Decoupling Capacitor (C_{uVCC})

The uVCC pin should be decoupled to the GND pin with at least 2.2 µF ceramic capacitor. No external load should be connected on uVCC.

CC1/CC2 Protection Circuit (R_{CC1}, R_{CC2}, C_{CC1}, C_{CC2}, D_{CC1}, D_{CC2})

To achieve ESD robustness for CC1 and CC2 pins, an RC and Zener network must be used in the design. Zener diodes D_{CC1} and D_{CC2} must be placed as close as possible to the Type-C connector CC pins and output return. Zener voltage must be chosen such that it can withstand a VOUT to CC1/CC2 short circuit fault that could be caused by a frayed cable. For designs that support 20 or 21 V output, a 24 V 200 mW Zener is sufficient.

A 22 Ω resistor and 560 pF capacitor are recommended for each CC line. Higher values must be avoided to maintain the switching slew rate of CC1 and CC2 during USB PD communication.

Key Applications Design Considerations

Output Power Table

The output power table in the data sheet (Table 1) represents the maximum practical continuous output power that can be obtained under the following conditions:

- The minimum DC input voltage (after the bridge rectifier) is 90 V or higher for 85 VAC input, 220 V or higher for 230 VAC input (or 115 VAC with a voltage-doubler). Input capacitor voltage should be sized to meet these criteria for AC input designs.
- Efficiency assumptions depend on power level. Smallest device power level assumes efficiency >84% increasing to >89% for the largest device and are quite conservative.
- Transformer primary inductance tolerance of ±10%.
- Reflected output voltage (VOR) is set to maintain K_P = 0.8 at minimum input voltage for universal line and K_P = 1 for high-line designs.
- Maximum conduction loss for adapters is limited to 0.6 W, 0.8 W for open frame designs.
- Increased current limit is selected for open frame power designs and standard current limit for adapter designs.
- The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 110 °C.
- Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters is assured.
- To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.5 is used. This prevents the initial current limit (I_{INT}) from being exceeded at FET turn-ON.
- It is unique feature in InnoSwitch3-PD that a designer can set the maximum steady-state operating switching frequency between 25 kHz to 95 kHz depending on the transformer design. One of the ways to effectively lower device temperature is to design the transformer to operate at low switching frequency, a good starting point is 60 kHz for larger device such as size 8, but for smaller device such size 5, 80 kHz is appropriate.

Recommendations for Circuit Board Layout

Single-Point Grounding

Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. Create a separate trace to connect the bias capacitor ground to the input filter capacitor negative terminal (see Figure 20).

Bypass Capacitors

The PRIMARY BYPASS (C_{BPP}), SECONDARY BYPASS (C_{BPS}), Current Sense Filter (C_{IS}), V_{OUT} filter (C_{VOUT}), and µVCC ($C_{µVCC}$) decoupling capacitors must be located directly adjacent to the PRIMARY BYPASS-SOURCE, SECONDARY BYPASS-GROUND, IS, VOUT, and uVCC pins, respectively. Connections should be routed via short traces.

Signal Components

External components Line Sensing resistors (R_{LS1}, R_{LS2}), BPP resistor (R_{BIAS}) and bias linear regulator components (if present), output current sense resistor and filter (R_{SENSE}, R_{FILT}), and FORWARD resistor (R_{FWD}), which are used for monitoring feedback information must be placed as close as possible to the IC pin with short traces. R_{SENSE} must be kelvin-connected to the low-pass filter formed by R_{FILT} and C_{IS}, and C_{IS} must be directly adjacent to IS and GND pins for accurate current sensing.

Critical Loop Area

Circuit loops where high dv/dt or di/dt occurs should be kept as small as possible. The area of the primary loop that connects the input filter capacitor, transformer primary and Drain-Source pins of the IC should be kept as small as possible. Similarly, the area of the secondary loop formed by the secondary winding, output capacitors, and SR FET should be kept as small as possible.

No loop area should be placed inside another loop (see Figure 21). This will minimize cross-talk between circuits.

Primary Clamp Circuit

A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop between the clamp components, the transformer and the IC. When using an RCD or R2CD clamp, although C_{SN} and R_{SN} are in parallel, C_{SN} must be placed closer to the primary winding than R_{SN}.

Y Capacitor

The placement of the Y capacitor should be directly from the primary input filter capacitor positive terminal to the output positive or return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the IC.

Output SR MOSFET

For best performance, the area of the loop connecting the secondary winding, the output SR FET, and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the terminals of the SR FET for heat sinking. The distance between SR FET source and InnoSwitch3-PD GND pin needs to be short to prevent negative current flowing through the primary FET.

ESD Immunity

Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD or hi-pot isolation requirements. The spark gap is best placed between output return and/or positive terminals and one of the AC inputs (after the fuse). In this configuration a 6.4 mm (dependent on customer requirement) spark gap is more than sufficient to meet the creepage and clearance requirements of most applicable safety standards. See layout example Figure 21.

A spark gap across the common-mode-choke or inductor helps provide low impedance path for a high energy discharge due to ESD or a common-mode surge.

Drain Node

The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin, and the trace width and length in this circuit should be minimized.

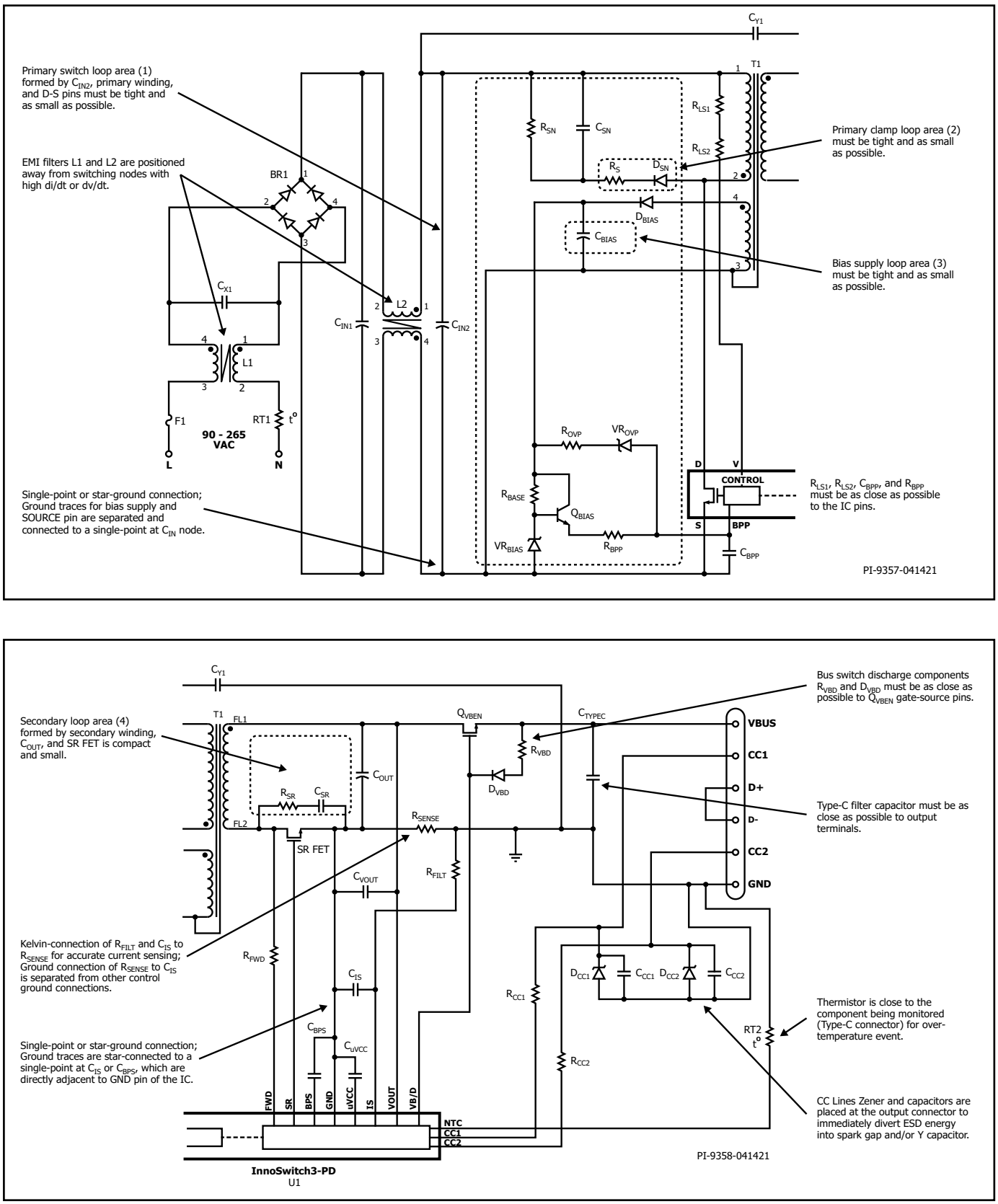
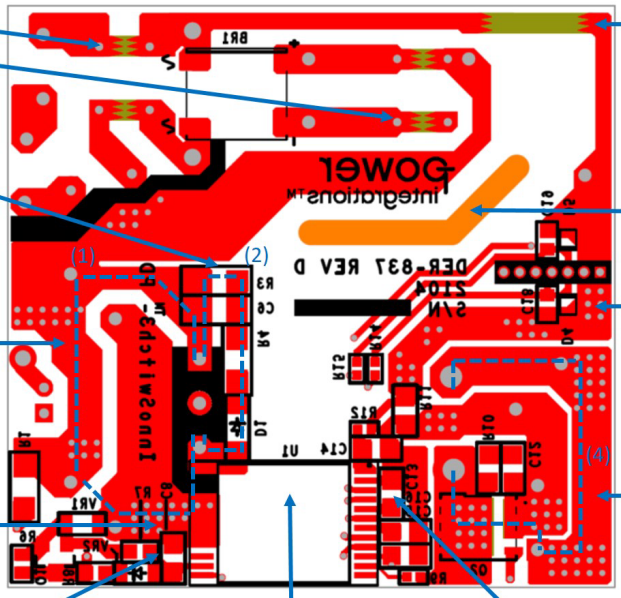


Figure 20. PRIMARY and SECONDARY Sides – Typical Schematic of InnoSwitch3-PD Showing Critical Loops Areas, Critical Component Traces and Single-Point or Star Grounding.

Layout Example



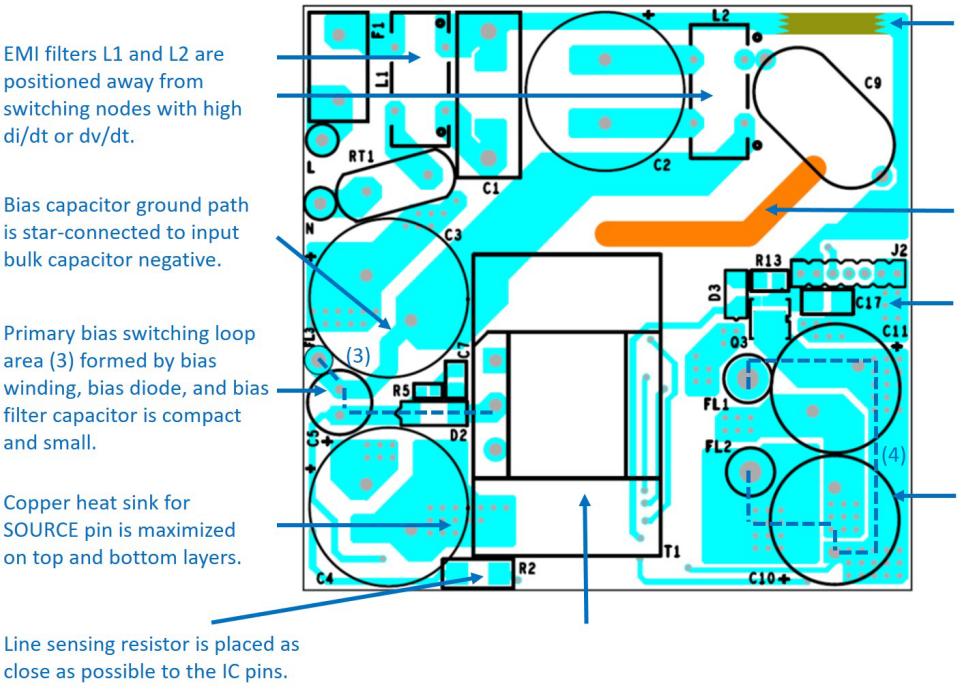


Figure 21. BOTTOM and TOP Sides – Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placements and Spark Gap Location.

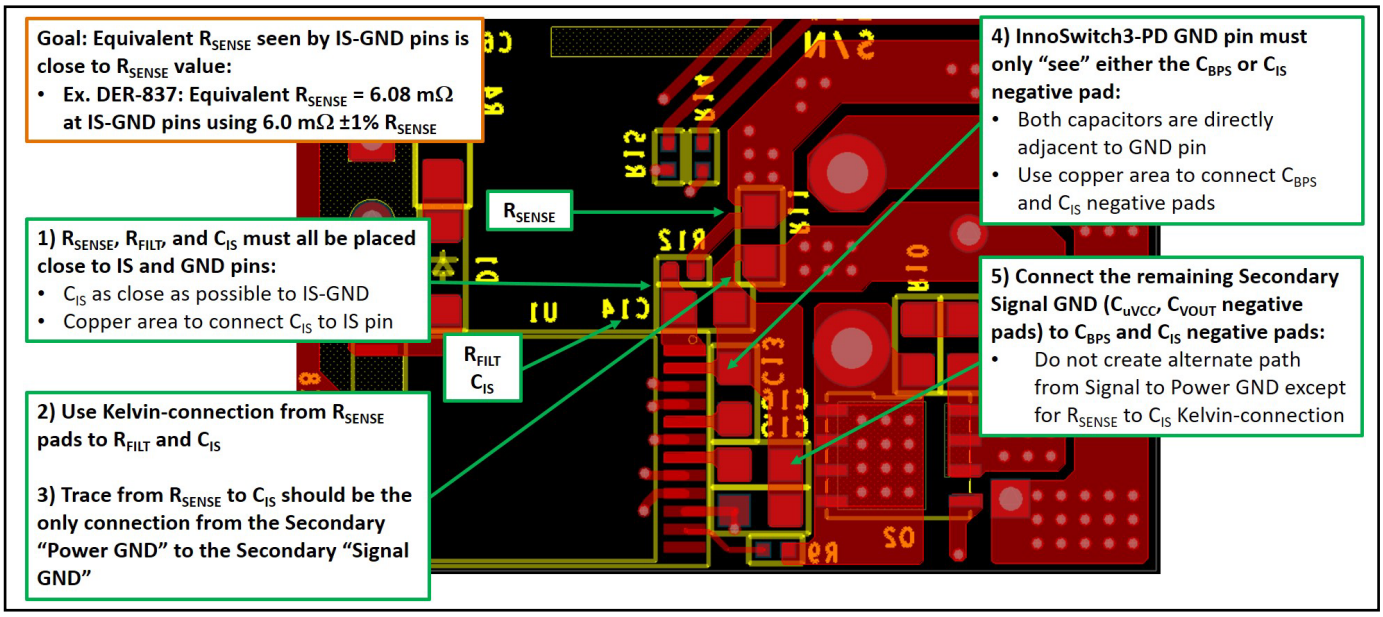


Figure 22. PCB Layout Guide for R_{SENSE}, R_{FILT}, and C_{IS} to Achieve Accurate Current Sensing.

Design Considerations When Using PowiGaN Devices (INN3x78C, INN3x79C and INN3x70C)

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 23.

VOR is the reflected output voltage across the primary winding when the secondary is conducting. VBUS is the DC voltage connected to one end of the transformer primary winding.

In addition to VBUS+VOR, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch.

VCLM in Figure 23 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of VBUS, VOR and VCLM.

VOR and the clamp voltage VCLM should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

To make full use of QR capability and ensure flattest efficiency over line/load, set reflected output voltage (VOR) to maintain KP = 0.8 at minimum input voltage for universal input and KP ≥ 1 for high-line only conditions.

Consider the following for design optimization:

17. Higher VOR allows increased power delivery at VMIN, which minimizes the value of the input capacitor and maximizes power delivery from a given PowiGaN INN3878C, INN3879C and INN3870C device.
18. Higher VOR reduces the voltage stress on the output diodes and SR FETs.
19. Higher VOR increases leakage inductance which reduces power
20. Higher VOR increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents the VOR should be reduced to get highest efficiency. For output voltages above 15 V, VOR should be maintained higher to maintain an acceptable PIV across the output synchronous rectifier.

VOR choice will affect the operating efficiency and should be selected carefully. Table below shows the typical range of VOR for optimal performance:

Maximum Output Voltage	Suggested Range for VOR
	INN387xC (725 V / 750 V Switch)
5 V	45 – 70 V
9 V	80 – 100 V
12 V	90 – 120 V
15 V	100 – 135 V
20 V	120 – 150 V
21 V	125 – 160 V

Table 14. Suggested VOR for PowiGaN Devices.

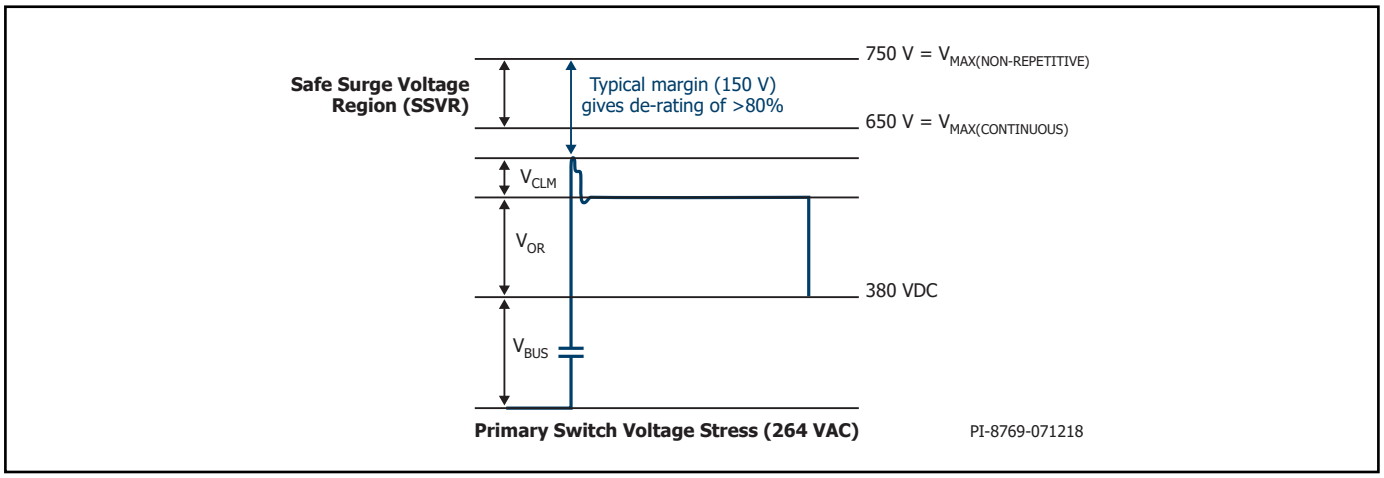


Figure 23. Peak Drain Voltage for 264 VAC Input Voltage.

Effect of Surge Voltage on $R_{DS(ON)}$ of the Device (INN3x78C, INN3x79C and INN3x70C)

R_{DSON} of the device increases when subjected to repetitive surge over 650 V on the drain, however the device R_{DSON} recovers to nominal value over time.

Figure 24 shows the effect of repetitive surge on $R_{DS(ON)}$ of the device, whereas:

T1	T2	R_{DSON} Increase
100 s	20 hr	5%

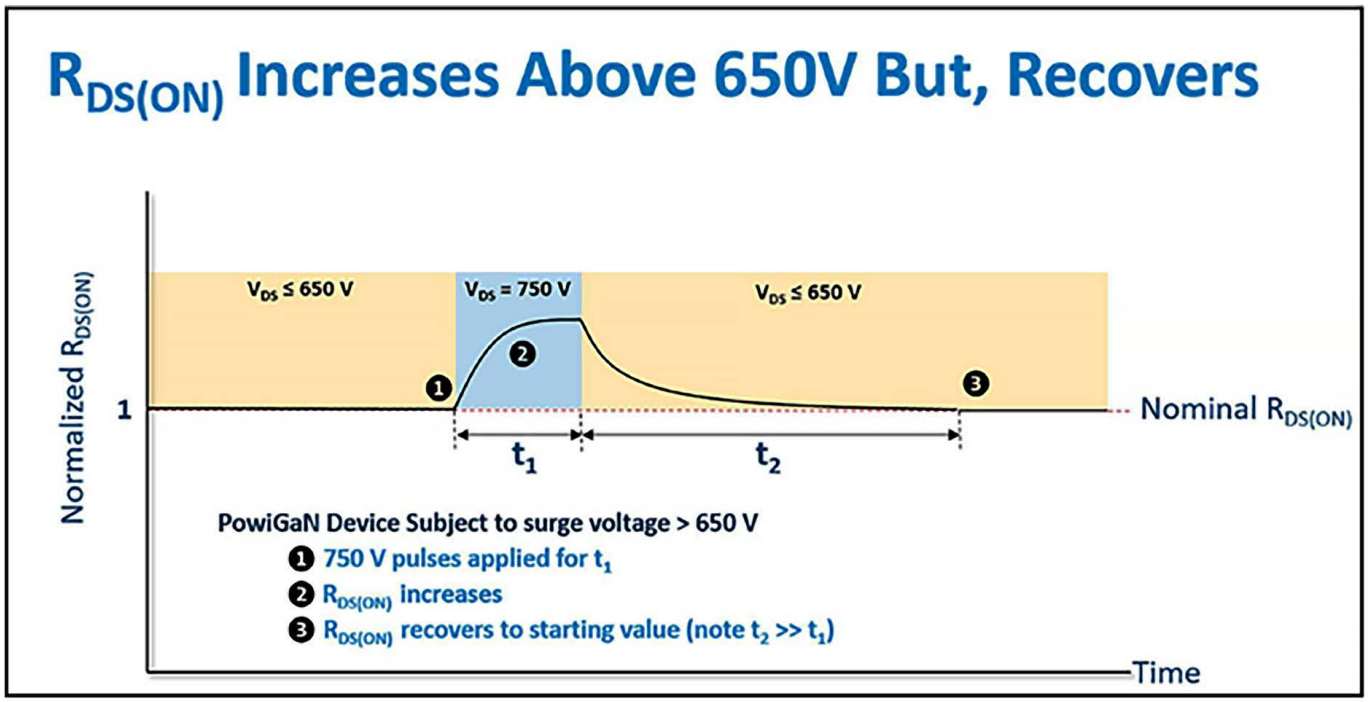


Figure 24. Effect of Surge Voltage on R_{DSON} of the Device.

Recommended Position of InSOP-24D Package with Respect to Transformer

The PCB underneath the transformer and InSOP-24D must be rigid. If a large size transformer core is used on the board with thin PCB, (<1.5 mm), it is recommended that the transformer be away from the InSOP package.

Cutting a slot in the PCB that runs near to or underneath the InSOP package is generally not recommended as this weakens the PCB. In the case of a long PCB, it is recommended that mechanical support or post be placed in the middle of the board or near the InSOP package.

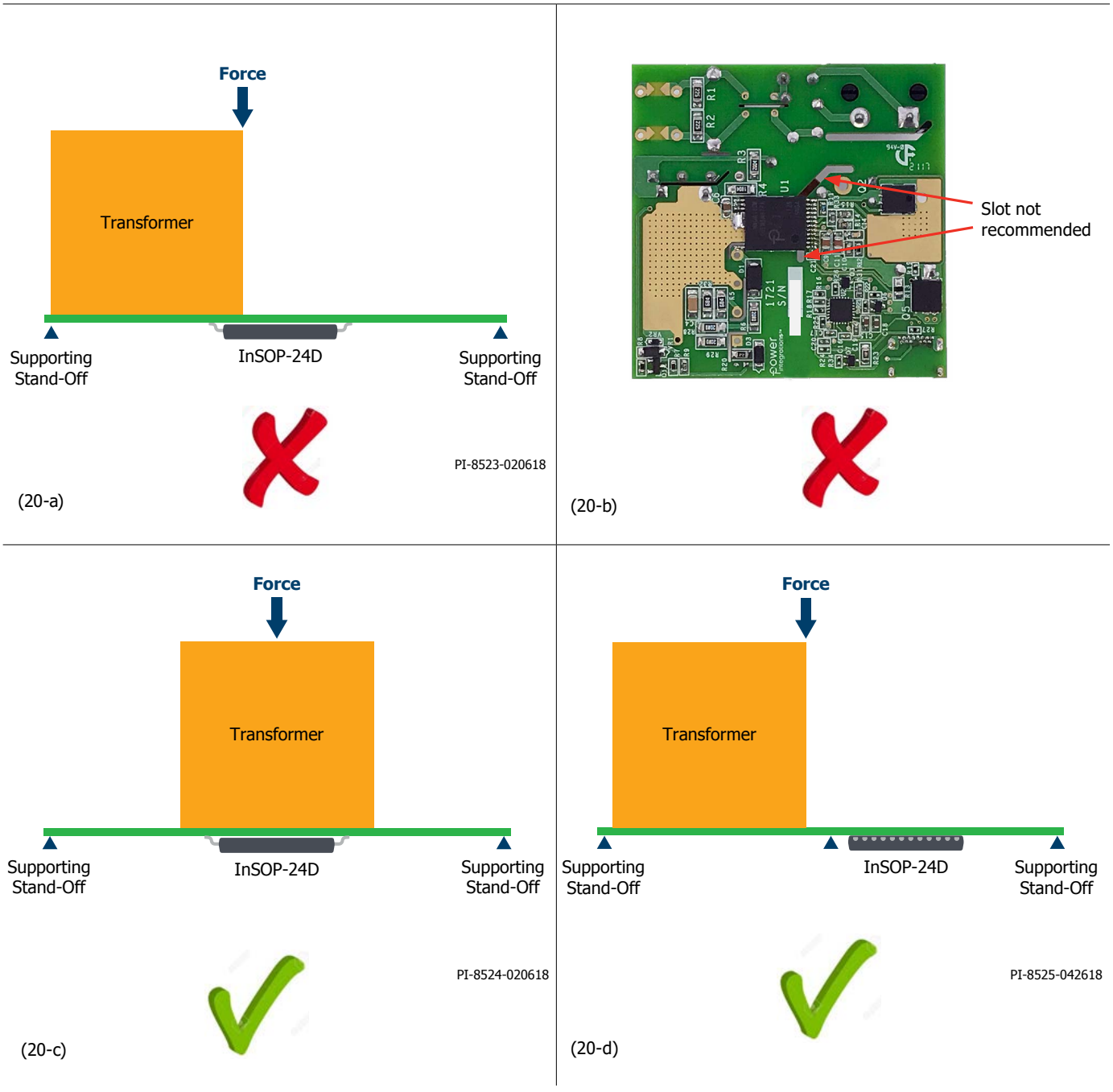


Figure 25. Recommended Position of InSOP-24D Package Shown with Check Mark.

Recommendations to Reduce No-load Consumption

The InnoSwitch3-PD IC will start in self-powered mode, drawing energy from the BYPASS pin capacitor that is charged from an internal current source. A bias winding is required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3-PD IC has started switching. A bias winding supply to the PRIMARY BYPASS pin enables power supplies to have low no-load power consumption. Refer to Critical External Components Selection section of this document for guidance on how to design the external bias supply circuit.

Proper selection of EMI filter X capacitor at the AC input can also improve no-load consumption. X capacitor is generally needed to reduce differential noise and meet conducted EMI requirements. However, the power dissipation of these X capacitors (few mW) typically increases with capacitance value. Also, for the same capacitance value, the capacitors from different manufacturers have different power dissipation. For example, 330 nF capacitors from two different manufacturers can have 2.80 mW and 6.85 mW dissipation at 230 VAC. It is recommended to verify the power loss of the X capacitor to be used and the possible alternate parts.

Some safety standards also require X-capacitors above 100 nF to be discharged within certain timing specifications. If the power supply can meet EMI specifications with 100 nF X capacitor, then a bleeder circuit may not be required. However, if a discharge circuit to the X capacitor is required for safety requirements, the CAPZero™ Family devices from Power Integrations should be used. This minimizes the additional power dissipation to be less than 5 mW @ 230 VAC.

Other areas that may help reduce no-load consumption further are;
1. Low value of primary clamp capacitor, C_{SN}.
2. Schottky or ultrafast diode for bias supply rectifier, D_{BIAS}.
3. Low ESR capacitor for bias supply filter capacitor, C_{BIAS}.
4. Low value SR FET RC snubber capacitor, C_{SR}.
5. Tape between primary winding layers, and multi-layer tapes between primary and secondary windings to reduce inter winding capacitance.

Recommendations for Reducing EMI

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area (see Figure 21).
2. A small capacitor parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor (2 – 47 Ω) in series with the bias winding helps reduce radiated EMI.
4. A small resistor and ceramic capacitor (< 22 pF) in series across primary winding and/or across secondary winding (< 100 pF) may help reduce conducted and/or radiated EMI. However, if value is large, then no-load consumption will increase.
5. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common-mode noise. However, the same performance can be achieved by use of shield windings in the transformer. Shield windings can also be used in conjunction with common mode filter inductors at the input to reduce conducted and radiated EMI.
6. Adjusting SR MOSFET RC snubber component values can help reduce high frequency radiated and conducted EMI.
7. A resistor across the differential inductors reduces their Q factor which can reduce EMI above 10 MHz. However low frequency EMI below 5 MHz may increase slightly.
8. A 1 µF ceramic capacitor connected at the output of the power supply may help to reduce radiated EMI.
9. A slow diode (i.e. 250 ns < t_{RR} < 500 ns) as the bias rectifier (D_{BIAS}) is generally good for reducing conducted EMI > 20 MHz and radiated EMI > 30 MHz.

Recommendations for Increased ESD Immunity

1. Sufficient clearance should be maintained (> 8 mm) between the primary-side and secondary-side circuits (especially underneath InSOP package and transformer). It is not recommended to place spark gap near or across InSOP package.
2. Use two spark gaps connected to secondary terminals (output return and positive) and one of the AC inputs after the fuse (see Figure 21). In this configuration at least 6.8 mm gap is often sufficient to meet creepage and clearance requirements of applicable safety standards.
3. Use a spark gap across common-mode choke or inductor to provide a low impedance path for any high energy discharge build up due to ESD or common mode surge.
4. Use a Y capacitor connected from either positive or negative output terminals to the input bulk capacitor's positive terminal or to the AC input after the fuse.
5. Ensure that the spark gap and Y capacitors do not share the same power traces.
6. Employ good layout practices and follow the PCB layout recommendations in the application note.
7. Apply multi-layer tape between bias and secondary windings, and also between secondary and primary windings.
8. To improve ESD robustness of CC1 and CC2 lines, 22 Ω, 5% resistors are required in series with the pins and the Type C connector. 24 V, 200 mW Zener diodes and 560 pF, 50 V ceramic capacitors are required to be connected between pins and the Type-C connector return after the 22 Ω resistor (Figure 21).

Thermal Management Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore, the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without causing EMI problems. Similarly, for the output SR MOSFET, maximize the PCB area connected to the pins on the package through which heat is dissipated.

Sufficient copper area should be provided on the board to keep the IC temperature safely below absolute maximum limits. It is recommended that the copper area to which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load, lowest rated input AC supply voltage and at highest rated temperature. Further de-rating can be applied as required.

Heat Spreader

For stringent thermal requirements, position the IC adjacent to the transformer as shown in Figure 25-d. This will reduce heat transfer to the IC from the transformer. For enclosed high power applications such as laptop adaptor or similar applications with high ambient environment, using the PCB as a heat sink may not be enough for the IC to operate within specified operating temperature, therefore a metal heat spreader may be necessary to keep the IC cool. Unless a ceramic material is used for the heat sink, care must be taken to maximize the safety limit.

A heat spreader is formed by combination of a heat spreader material (Copper or Aluminum), a 0.4 mm mylar pad (for reinforced isolation) and a thermally conductive pad for better heat transfer between the IC and the spreader.

Figure 26 shows the basic idea how to implement the attachment of a heat spreader to an InSOP-24D package while maintaining creepage between primary-side and secondary-side pins of InnoSwitch3-PD IC.

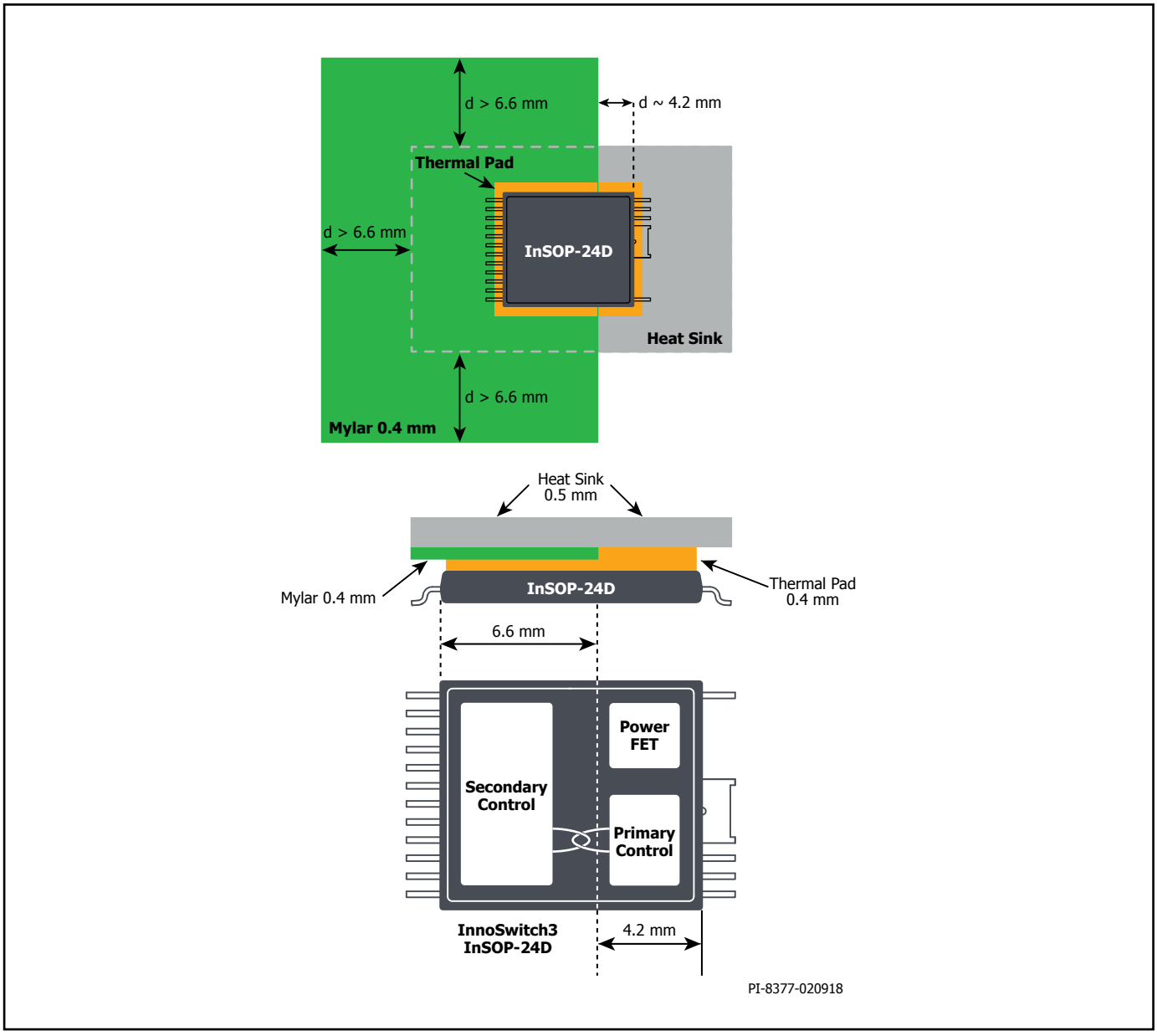


Figure 26. Simplified Diagram of Heat Spreader Attachment to an InSOP-24D Package.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch3-PD designs should be verified on-the-bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

Maximum Drain Voltage
Verify that VDS of InnoSwitch3-PD and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.

Maximum Drain Current
At maximum ambient temperature, maximum input voltage, maximum output voltage and peak output (overload) power, review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum drain current for the primary MOSFET should be below the specified absolute maximum ratings.

Thermal Check
At specified maximum output power, minimum input voltage and maximum ambient temperature. Verify that temperature specification limits for InnoSwitch3-PD IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of MOSFET $R_{DS(ON)}$. At low-line, maximum power, a maximum InnoSwitch3-PD SOURCE pin temperature of 110 °C is recommended to allow for $R_{DS(ON)}$ variation.

Application Example

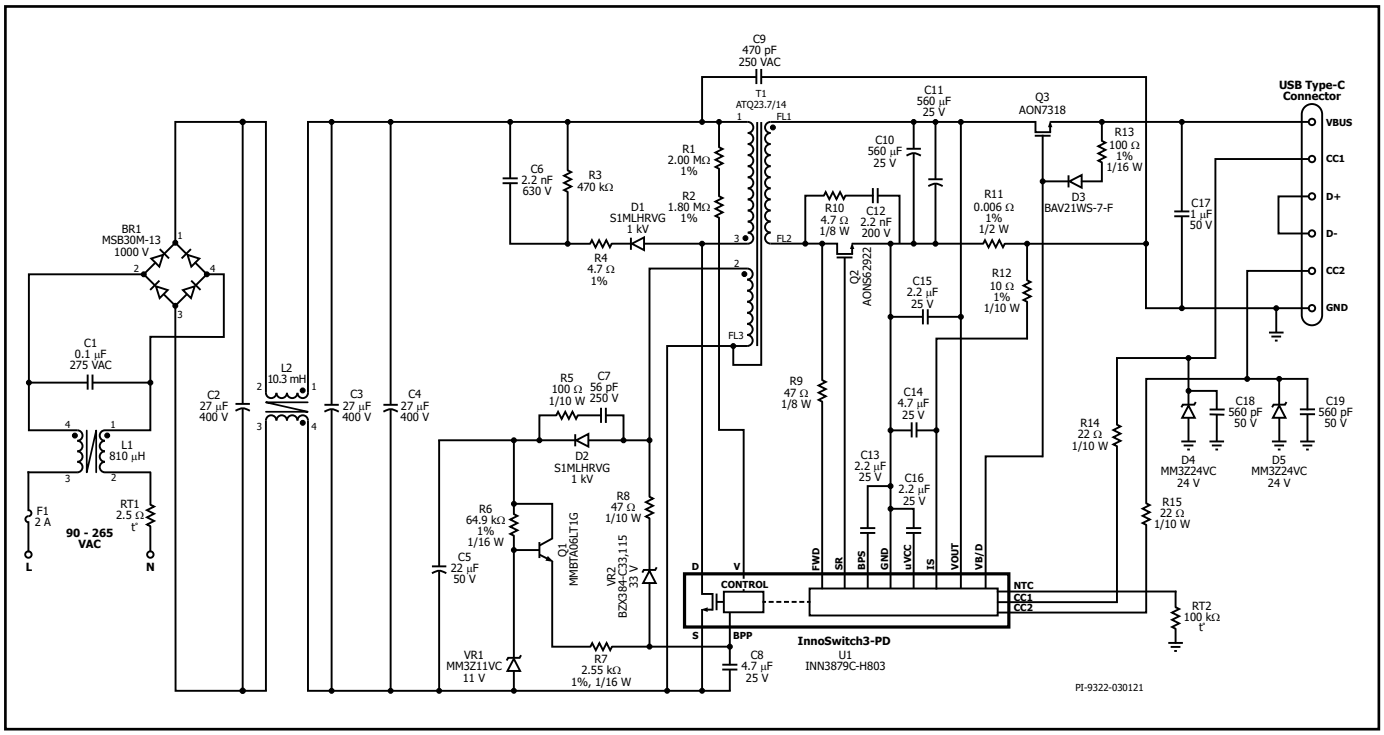


Figure 27. Schematic of DER-837 45 W 5 A USB PD 3.0 Power Supply using INN3879C-H803.

A High Efficiency, 45 W 5 A Universal Input USB PD Power Supply (InnoSwitch3-PD)

The circuit in Figure 27 uses INN3879C-H803 device for a 45 W, 5 A USB PD 3.0 power supply with the following Source Capabilities:

- PDO1: 5 V / 5 A (Fixed Supply)
- PDO2: 9 V / 5 A (Fixed Supply)
- PDO3: 15 V / 3 A (Fixed Supply)
- PDO4: 20 V / 2.25 A (Fixed Supply)
- PDO5: 3.3 V – 11 V / 5 A (PPS, 45 W power-limited)
- PDO6: 3.3 V – 16 V / 3 A (PPS)
- PDO7: 3.3 V – 21 V / 2.25 A (PPS)

This power supply delivers higher than 90% average efficiency from 90 VAC to 265 VAC input for all supported 45 W Fixed Supply PDOs (9 V / 5 A, 15 V / 3 A, and 20 V / 2.25 A) using INN3879C.

Fuse F1 isolates the circuit and provides protection from component failure. NTC thermistor RT1 limits the inrush current when the input AC supply is connected. Common mode chokes L1 and L2, with capacitors C9 and C1 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage to have a full wave rectified DC, which is filtered by the bulk capacitors C2, C3, and C4.

Resistors R1 and R2 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage. A low-cost R2CD clamp formed by diode D1, resistors R3, and R4, and capacitor C6 limits the peak drain-source voltage of InnoSwitch3-PD U1 at the instant the switch inside U1 turns off.

During normal operation, the primary side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. A linear regulator comprising resistor R6, R7, BJT Q1 and Zener diode VR1 ensures sufficient current flows through R7 into the BPP pin of the InnoSwitch3-PD IC such that the internal current source of U1 is not required to charge C8 to minimize power consumption during no-load condition and at normal operation. The RC network consisting of resistor R5 and capacitor C7 offers damping of the high frequency ringing in the voltage across diode D2 to reduce radiated EMI. Zener diode VR2 and resistor R8 provide primary sensed output overvoltage protection.

The secondary-side of the InnoSwitch3-PD IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q2 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R10 and C12. SR FET Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R9 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13 connected to the BPS pin of InnoSwitch3-PD IC provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R11. The current measurement is filtered with resistor R12 and capacitor C14, and then monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the integrated secondary and USB PD controllers of InnoSwitch3-PD IC up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-PD IC uses variable frequency and variable primary switch peak current limit control schemes to maintain a fixed output current.

For constant current (CC) operation, when the output voltage falls, the secondary side controller inside InnoSwitch3-PD IC will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C13 via resistor R9 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-PD IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the integrated secondary and USB PD controllers of the InnoSwitch3-PD IC and output voltage regulation is achieved by variable frequency and variable primary switch peak current limit control schemes. Capacitor C15 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-channel MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. MOSFET Q3 is controlled by the VB/D pin on the InnoSwitch3-PD IC. Resistor R13 and diode D3 are connected across the Source and Gate terminals of the Q3 to provide a discharge path for the bus voltage when the Q3 is turned off. Capacitor C17 is used at the output for ESD protection and output voltage ripple reduction.

The USB Power Delivery (USB PD) controller is integrated within the InnoSwitch3-PD IC. Capacitor C16 connected to µVCC pin serves as a decoupling capacitor to the internal regulator which provides power to the USB PD controller. USB PD protocol is communicated other either CC1 or CC2 line depending on the orientation in which the Type-C plug is connected. Capacitors C18 and C19, resistors R14 and R15, and Zener diodes D4, and D5 provide protection from ESD to pins CC1 and CC2.

Troubleshooting Matrix

Problem Symptoms	Possible Causes of the Problem	Solutions to the Problem
Input fuse blows at start-up	Components in power stage are incorrectly assembled or damaged	1. Verify polarities of the components used (e.g. bridge rectifier polarity). 2. Verify interconnections between components.
	InnoSwitch3-PD drain terminals are shorted to the source terminal on the circuit board.	1. Check for solder bridging and short-circuits on PCB. 2. Verify if IC is damaged.
	Insufficient fuse current rating	1. Verify fuse rating using PIXLs. 2. Replace fuse with sufficient current rating and I^2t.
No voltage across BPP capacitor or drain-source pins of InnoSwitch3-PD	No AC input voltage at bridge rectifier input terminals or no DC voltage across input bulk capacitor after the bridge rectifier	1. Check voltage at the input of the bridge rectifier. 2. Check components and connections in the EMI filter stage including thermistor.
	Input fuse is open	Verify that input fuse is functional.
Power supply does not startup	InnoSwitch3-PD pins are incorrectly connected on the circuit board	Confirm that none of the pins are open or are accidently connected to the adjacent pin on the circuit board.
	Output capacitor polarity is reversed	Verify polarity of the capacitor.
	V pin current is less than IUV-	Verify the values of the line sensing resistors and their connections.
Power supply undergoes auto-restart upon start-up	VOUT pin of InnoSwitch3-PD is open	Confirm that VOUT pin is connected to the positive terminal of the output capacitor.
	Overshoot of output voltage at startup	Probe output voltage to confirm that output voltage does not exceed output OV threshold of 6.2 V on start-up. Confirm that the recommended values of BPP and BPS capacitors are used, or increase output capacitance, or redesign transformer to decrease overshoot.
	Overload condition	Verify that the load being applied is not greater than the output current rating.
No output voltage at Type-C connector although voltage is present across output capacitor before the bus switch	No sink attached	Verify that a PD sink is attached through a working Type-C cable. A 5.1 kΩ resistor can be temporarily connected from any CC pin to output ground to simulate a PD sink.
	InnoSwitch3-PD with non-standard Feature Code is being used.	Verify the IC has been programmed successfully. After start-up, confirm that the voltage across CC pins and GND pins is about 3.6 V when the Type-C cable is disconnected.

Table 15. Basic Troubleshooting Guide for InnoSwitch3-PD Power Supply Designs.

Failure Mode Analysis

Described below is the device level failure mode analysis including the system effects of an open circuit for each pin as well as adjacent pin-to-pin short. In each case a safe failure is expected.

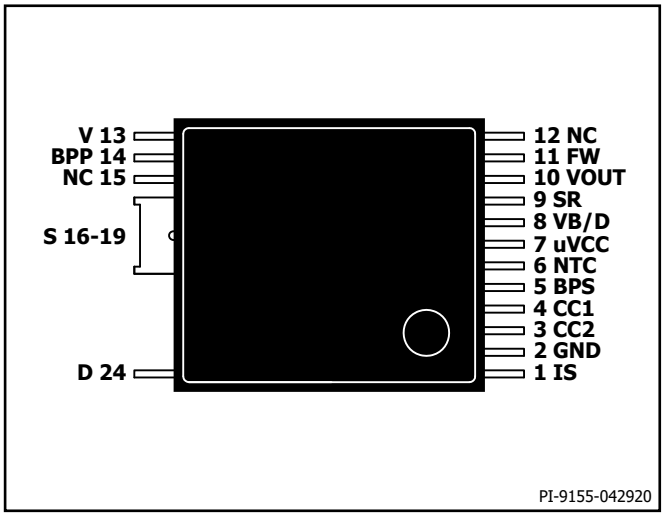


Figure 28. InnoSwitch3-PD Pin Configuration.

Fault Type: Pin Open	Observed Behavior	
	Fault applied Before Power-up	Fault applied After Power-up
IS	Power supply will Auto-Restart. No output voltage after the bus switch (VBUS_OUT).	Power supply will Auto-Restart. No output voltage after the bus switch (VBUS_OUT).
GND	VBUS_IN will regulate at 5 V but with high ripple. No output voltage after the bus switch (VBUS_OUT). Potential IC damage at prolonged operation due to high IC power consumption.	At light load, VBUS_OUT will regulate but with high output ripple. At heavy load, Auto-Restart will trigger and bus switch will remain open. Risk of damage to the IC at prolonged operation due to high IC power consumption.
VCONN Line	Power supply will operate normally except for VCONN-related functions. VCONN will not be supplied to Type-C cable.	Power supply will operate normally except for VCONN-related functions. VCONN will not be supplied to Type-C cable.
CC Line	Power supply will start-up normally except for CC-related functions. Connection of a Type-C cable or USB PD Sink will not be detected. VBUS_IN will regulate at 5 V and bus switch will remain open.	VBUS_IN will transition to 5 V and bus switch will open. CC-related functions will be unusable.
BPS	Latch-off will trigger if primary-sensed output OVP circuit is present.	Power supply will Auto-Restart. Then it will latch-off will trigger if primary-sensed output OVP circuit is present.
NTC	Power supply will operate normally except for NTC-related functions.	Power supply will operate normally except for NTC-related functions.
uVCC	Power supply will operate normally except for all USB PD controller-related functions. VBUS_IN will regulate at 5 V and bus switch will remain open.	VBUS_IN will transition to 5 V and bus switch will open. USB PD controller-related functions will be unusable.
VB/D	VBUS_IN will regulate at 5 V and bus switch will remain open.	A low voltage may appear at VBUS_OUT, indicating the bus switch is only partially on. Risk of damage to the bus switch when high load current is drawn.

SR	Power supply will Auto-Restart.	High dissipation of SR FET due to secondary current passing through SR FET body diode.
VOUT	VBUS_IN will increase beyond 5 V during start-up. Latch-off will trigger if primary-sensed output OVP circuit is present.	VBUS_IN will increase beyond target regulation voltage. Latch-off will trigger if primary-sensed output OVP circuit is present.
FWD	VBUS_IN will increase beyond 5 V during start-up. Latch-off will trigger if primary-sensed output OVP circuit is present.	Power supply will Auto-Restart.
V	Primary FET will not switch due to Line UV condition.	Primary FET will stop switching due to Line UV condition.
BPP	Primary FET will not switch. Continuous BPP oscillation from 3.1 to 6.2 V.	Power supply will Latch-off. Continuous BPP oscillation from 3.1 to 6.2 V.
S	BPP voltage will rise beyond typical voltage and BPP will be internally damaged.	BPP voltage will rise beyond typical voltage and BPP will be internally damaged.
D	Primary FET will not switch.	Primary FET will stop switching.

Note: CC1/CC2 pins will function as either VCONN or CC Line depending on Type-C cable orientation.

Table 16. Failure Mode Analysis for Pin Open Fault.

Fault Type: Pin-to-Pin Short	Observed Behavior	
	Fault applied Before Power-up	Fault applied After Power-up
IS & GND	No output constant current regulation.	No output constant current regulation.
GND & CC2 (GND & CC Line)	Power supply will start-up normally except for CC-related functions. Connection of a Type-C cable or USB PD Sink will not be detected. VBUS_IN will remain at 5 V and bus switch will remain open.	In Fixed PDO: normal operation In PPS APDO: Hard Reset will trigger due to PPS communication timeout. Bus switch will turn off and remain open.
GND & CC2 (GND & VCONN)	Power supply will operate normally except for VCONN-related functions. VCONN will not be supplied to Type-C cable.	Power supply will operate normally except for VCONN-related functions. VCONN will not be supplied to Type-C cable.
CC2 & CC1	VBUS_IN will remain at 5 V and bus switch will remain open.	VBUS_IN will transition to 5 V and bus switch will open.
CC1 & BPS (CC Line & BPS)	Power supply will start-up normally except for CC-related functions. Connection of a Type-C cable or USB PD Sink will not be detected. VBUS_IN will remain at 5 V and bus switch will remain open.	VBUS_IN will transition to 5 V and bus switch will open.
CC1 & BPS (VCONN & BPS)	Power supply will start-up normally. VCONN voltage will be pulled-up to BPS voltage.	Power supply will operate normally. VCONN voltage will be pulled-up to BPS voltage.
BPS & NTC	Power supply will Auto-Restart every 1.6 seconds. VBUS_IN will remain at 5 V and bus switch will remain open.	Power supply will operate normally.
NTC & uVCC	Power supply will operate normally except for NTC-related functions.	Power supply will operate normally except for NTC-related functions.
uVCC & VB/D	A low voltage may appear at VBUS_OUT, indicating the bus switch is only partially on.	A low voltage may appear at VBUS_OUT, indicating the bus switch is only partially on.
VB/D & SR	Narrow pulses observed in VBUS_OUT with peak voltage less than 3 V.	Risk of damage to the IC.
SR & VOUT	Power supply will Auto-Restart every 2 seconds.	Risk of damage to the IC due to high voltage imposed on SR pin.
VOUT & FWD	VBUS_IN will increase beyond 5 V during start-up. Latch-off will trigger if primary-sensed output OVP circuit is present.	Risk of damage to the IC due to high voltage imposed on VOUT pin.
FWD & NC12	Potential damage to the resistor between SR drain and FWD pin. VBUS_IN might increase beyond 5 V during start-up. Latch-off might trigger if primary-sensed output OVP circuit is present.	Potential damage to the resistor between SR drain and FWD pin. Latch-off might trigger if primary-sensed output OVP circuit is present.
V & BPP	Primary FET will not switch.	Power supply will latch-off.
BPP & NC15	Power supply will start-up normally.	Power supply will operate normally.
NC15 & S	Power supply will start-up normally.	Power supply will operate normally.
S & D	Fuse at AC input will blow.	Fuse at AC input will blow.

Table 17. Failure Mode Analysis for Adjacent Pin-to-Pin Short Fault.

Appendix A

Input Capacitance Selection to Meet Hold-up Time Requirement

Hold-up time is the period wherein the power supply is able to maintain a regulated output even after an interruption or removal of AC input has occurred. It is typically measured starting from the instance the AC input is interrupted until the power supply output voltage drops to 90% of its normal operating value.

When the AC input is removed, an InnoSwitch3-PD power supply can still maintain output regulation until the input brown-out protection is triggered. This protection is integrated within the IC, wherein if the power supply is already operational, the fault is triggered when the current into the V pin drops below the I_{UV-} threshold. The current into V pin can be configured by choosing the total resistance connected from the V pin into either the AC side of the bridge rectifier or the DC side which is the input bulk capacitor positive node. At least two resistors in series will be used to withstand the voltage stress and meet safety requirements for each component.

For designs with hold-up time requirement, it is recommended to connect the V pin resistors to the input bulk capacitor instead of the AC side of the bridge rectifier. The V pin total resistance should be chosen based on the desired line overvoltage and undervoltage protection thresholds of the power supply. The resulting input bulk capacitor voltage threshold for brown-out protection can be estimated as:

$$V_{BULK(BROWNOUT)} = (I_{UV-}) (R_{LS})$$

Where;

$V_{BULK(BROWNOUT)}$: Input bulk capacitor brown-out voltage threshold. If bulk capacitor voltage drops below this value, brown-out protection will be triggered.

I_{UV-}: UV/OV pin brown-out threshold (data sheet parameter).

R_{LS}: Total resistance for line sensing (resistance from V pin to input bulk capacitor).

Knowing the input bulk capacitor voltage threshold for brown-out protection, the required input capacitance value to meet hold-up time requirement is calculated as:

$$C_{BULK} \geq \frac{2(P_{OUT})(T_{HOLD})}{(\eta[(V_{BULK})^2 - (V_{BULK(BROWNOUT)})^2]}$$

Where;

C_{BULK}: Minimum input bulk capacitance required to meet hold-up time.

P_{OUT}: Maximum rated output power of the design.

T_{HOLD}: Hold-up time requirement.

η: Efficiency estimate at when operating at P_{OUT}.

V_{BULK}: Minimum input bulk capacitor voltage when operating at P_{OUT}.

$V_{BULK(BROWNOUT)}$: Input bulk capacitor brown-out voltage threshold.

Revision	Notes	Date
A	Initial release.	09/21

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