# ZXMN20B28KTC-VB Datasheet

## N-Channel 200 V (D-S) MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 200 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.85 |
| $Q_g$ (Max.) (nC) | 13 | |
| $Q_{gs}$ (nC) | 3.0 | |
| $Q_{gd}$ (nC) | 7.9 | |
| Configuration | Single | |

### FEATURES

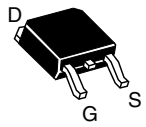
- Trench Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 % $R_g$ Tested
- Compliant to RoHS Directive 2002/95/EC

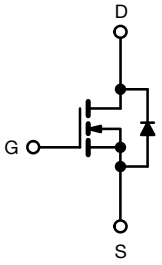
RoHS COMPLIANT

### APPLICATIONS

- Primary Side Switch

**DPAK (TO-252)**




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | 200 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 5.0 | A |
| | | $T_C$ = 100 °C | | 4.0 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 20 | |
| Linear Derating Factor | | | | 0.33 | W/°C |
| Linear Derating Factor (PCB Mount) [e] | | | | 0.020 | |
| Single Pulse Avalanche Energy [b] | | | $E_{AS}$ | 161 | mJ |
| Repetitive Avalanche Current [a] | | | $I_{AR}$ | 4.8 | A |
| Repetitive Avalanche Energy [a] | | | $E_{AR}$ | 4.2 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 42 | W |
| Maximum Power Dissipation (PCB mount) [e] | $T_A$ = 25 °C | | | 2.5 | |
| Peak Diode Recovery dV/dt [c] | | | dV/dt | 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering Recommendations (Peak temperature) [d] | for 10 s | | | 260 | |

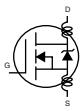
**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 14 mH, $R_g$ = 25 Ω, $I_{AS}$ = 4.8 A (see fig. 12).
c. $I_{SD} \leq$ 5.2 A, dI/dt ≤ 95 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | - | 110 | °C/W |
| Maximum Junction-to-Ambient (PCB mount) [a] | $R_{thJA}$ | - | - | 50 | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | - | 3.0 | |

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 200 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.29 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V | - | - | 25 | µA |
| | | $V_{DS}$ = 160 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 2.9 A [b] | - | 0.85 | - | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 2.9 A [b] | 1.7 | - | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | - | 185 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 100 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 30 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V, $I_D$ = 4.8 A, $V_{DS}$ = 160 V, see fig. 6 and 13 [b] | - | - | 13.0 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | - | 3.0 | |
| Gate-Drain Charge | $Q_{gd}$ | | - | - | 7.9 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 100 V, $I_D$ = 4.8 A, $R_G$ = 18 Ω, $R_D$ = 20 Ω, see fig. 10 [b] | - | 7.2 | - | ns |
| Rise Time | $t_r$ | | - | 22 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 19 | - | |
| Fall Time | $t_f$ | | - | 13 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact  | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 4.8 | A |
| Pulsed Diode Forward Current [a] | $I_{SM}$ | | - | - | 19 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 4.8 A, $V_{GS}$ = 0 V [b] | - | - | 1.8 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 4.8 A, dI/dt = 100 A/µs [b] | - | 150 | 300 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 0.91 | 1.8 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

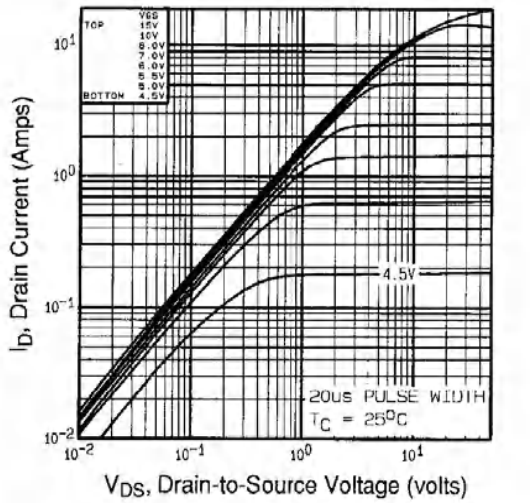



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

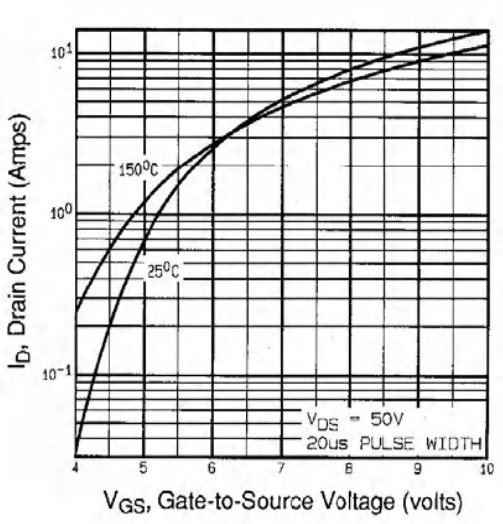



**Fig. 3 - Typical Transfer Characteristics**

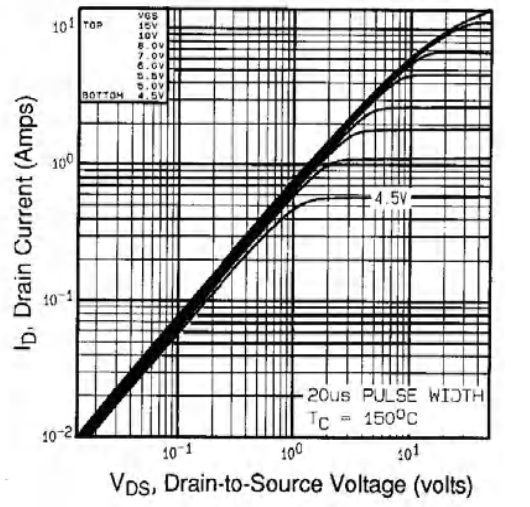



**Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C**

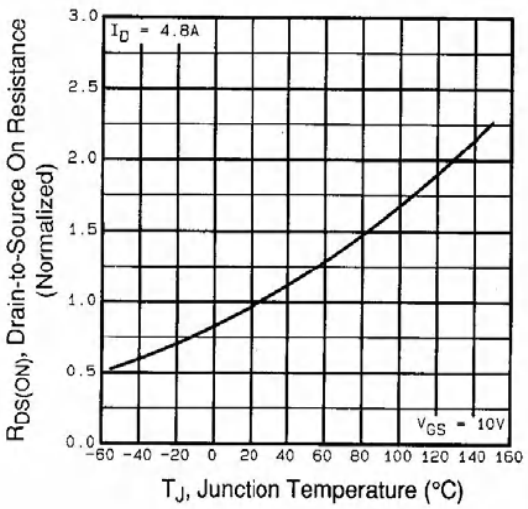



**Fig. 4 - Normalized On-Resistance vs. Temperature**

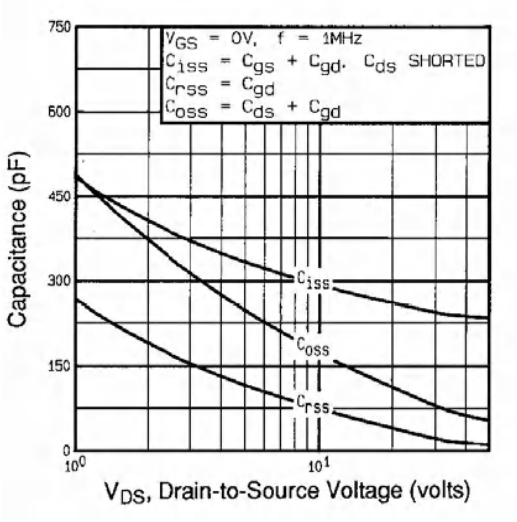



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

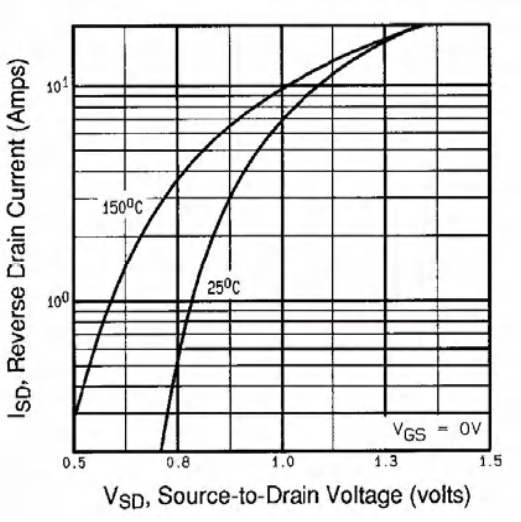



Fig. 7 - Typical Source-Drain Diode Forward Voltage

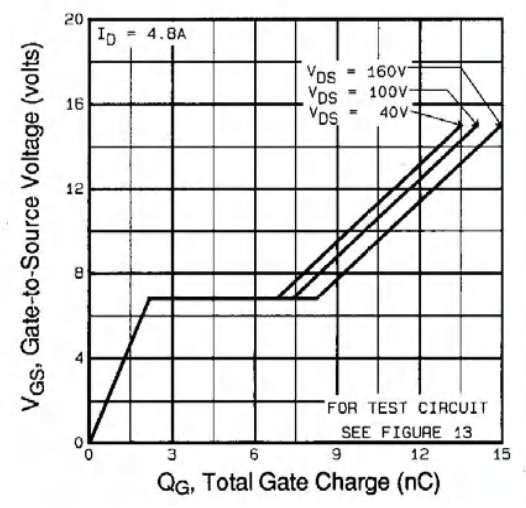



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

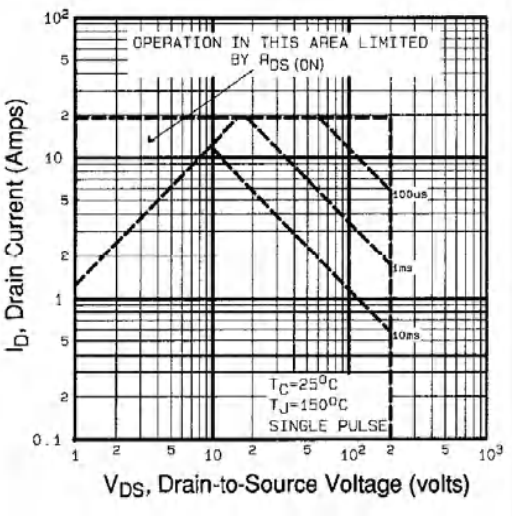



Fig. 8 - Maximum Safe Operating Area

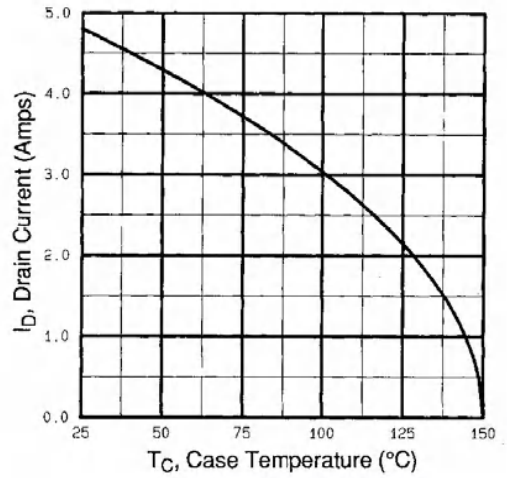



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

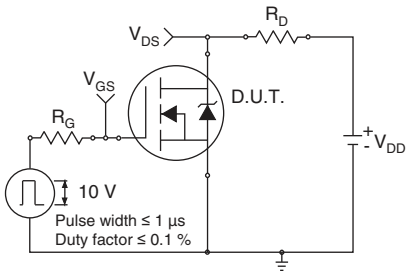



**Fig. 10a - Switching Time Test Circuit**

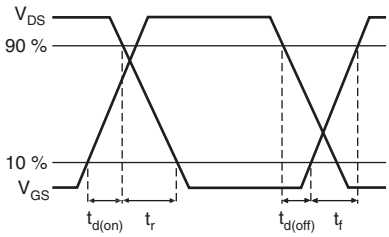



**Fig. 10b - Switching Time Waveforms**

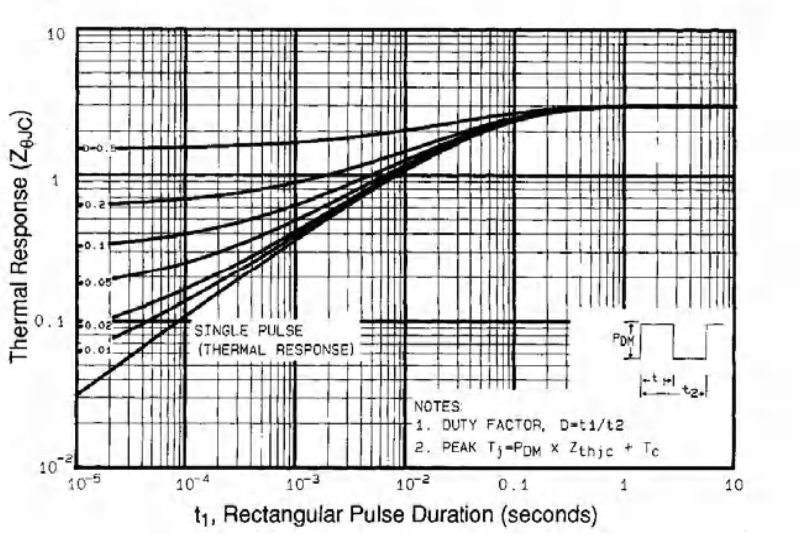



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

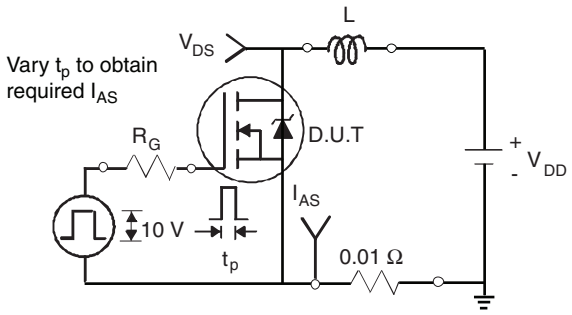



**Fig. 12a - Unclamped Inductive Test Circuit**

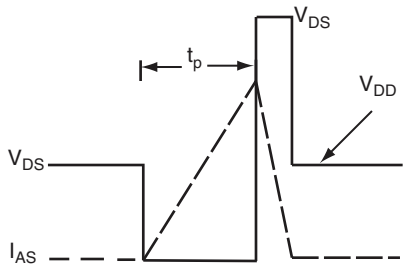



**Fig. 12b - Unclamped Inductive Waveforms**

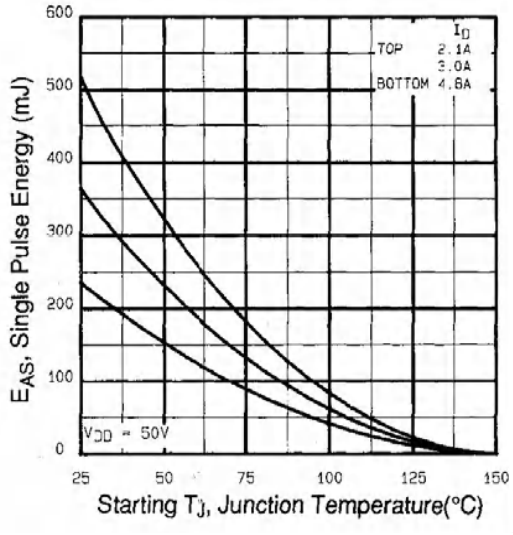



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

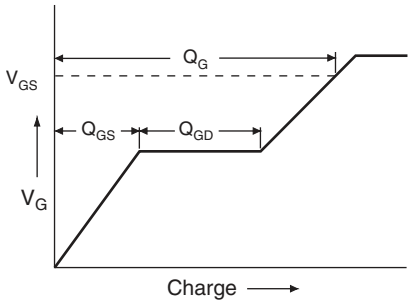



**Fig. 13a - Basic Gate Charge Waveform**

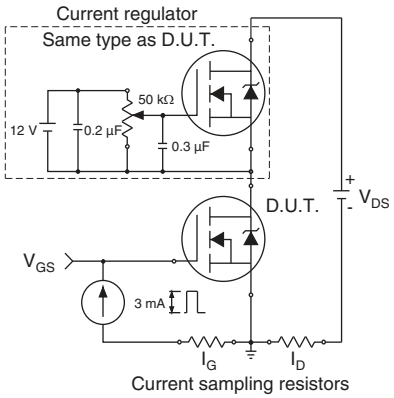
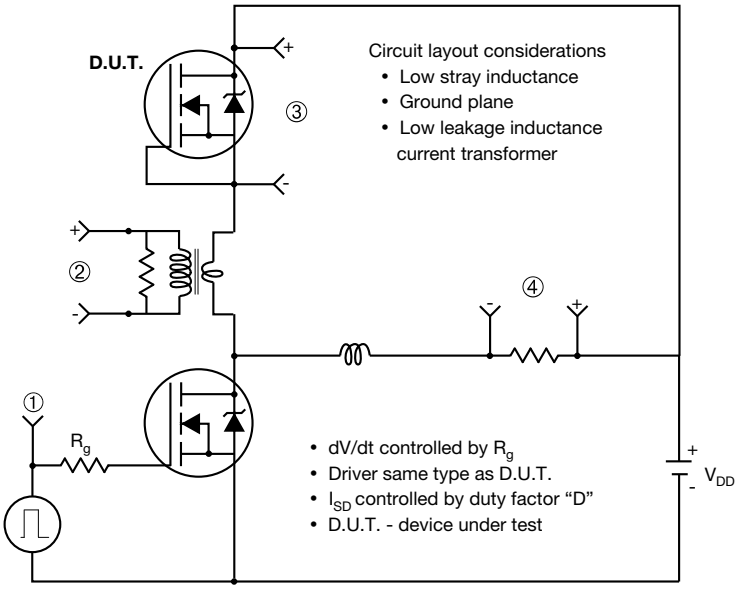
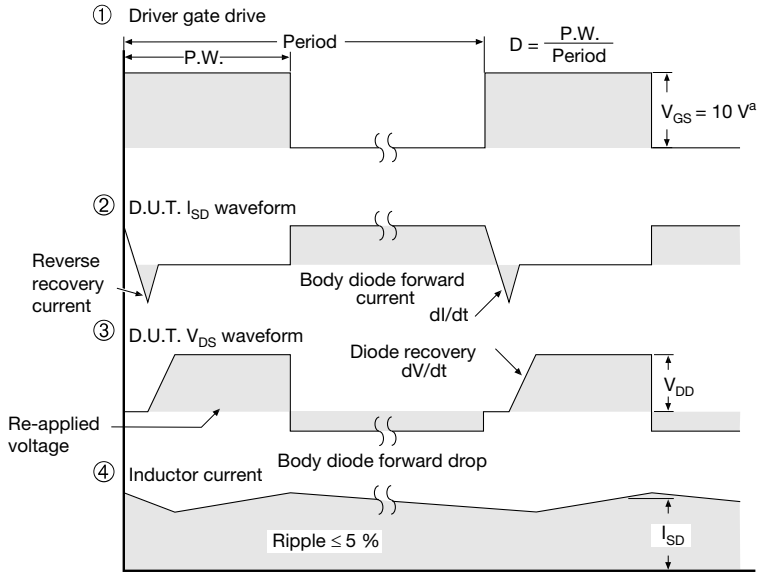



**Fig. 13b - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**



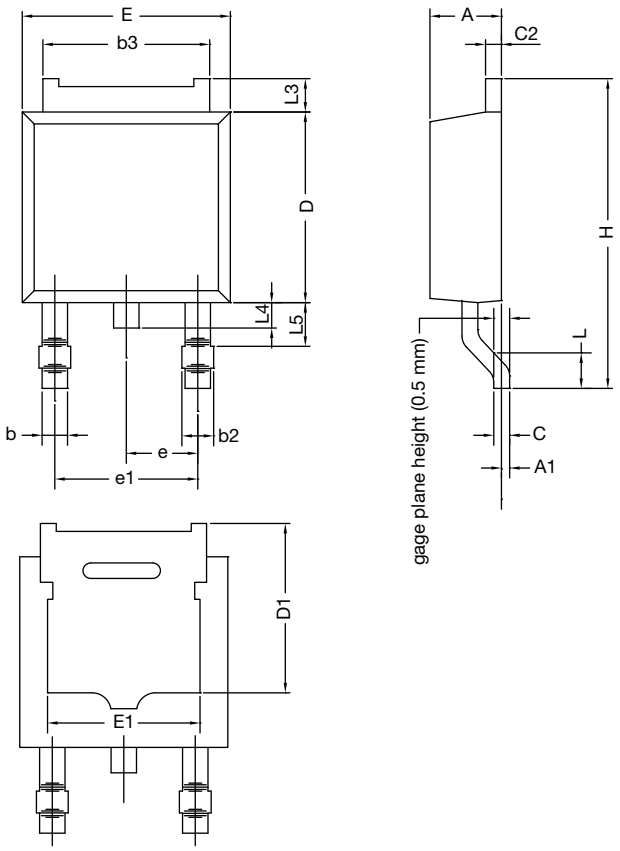




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

# TO-252AA Case Outline

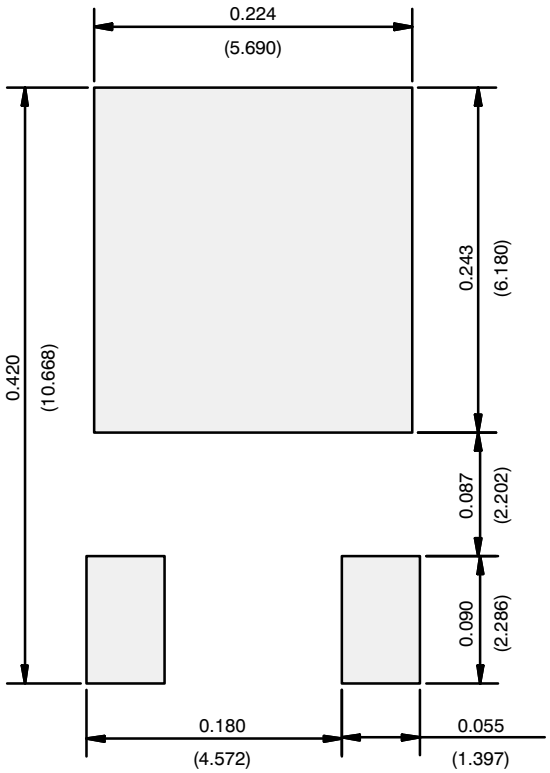



| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 2.18 | 2.38 | 0.086 | 0.094 |
| A1 | - | 0.127 | - | 0.005 |
| b | 0.64 | 0.88 | 0.025 | 0.035 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 |
| b3 | 4.95 | 5.46 | 0.195 | 0.215 |
| C | 0.46 | 0.61 | 0.018 | 0.024 |
| C2 | 0.46 | 0.89 | 0.018 | 0.035 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 4.10 | - | 0.161 | - |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | - | 0.170 | - |
| H | 9.40 | 10.41 | 0.370 | 0.410 |
| e | 2.28 BSC | | 0.090 BSC | |
| e1 | 4.56 BSC | | 0.180 BSC | |
| L | 1.40 | 1.78 | 0.055 | 0.070 |
| L3 | 0.89 | 1.27 | 0.035 | 0.050 |
| L4 | - | 1.02 | - | 0.040 |
| L5 | 1.01 | 1.52 | 0.040 | 0.060 |
| ECN: T16-0236-Rev. P, 16-May-16<br>DWG: 5347 | | | | |

**Notes**

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)




Recommended Minimum Pads
Dimensions in Inches/(mm)

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**Üreticileri görün**

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