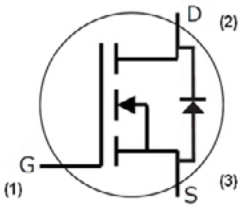
C3M0065090D

Silicon Carbide Power MOSFET C3M™ MOSFET Technology
N-Channel Enhancement Mode

Features

- C3M SiC MOSFET technology
- High blocking voltage with low On-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant





RoHS

Halogen-Free

Part Number	Package	Marking
C3M0065090D	TO 247-3	C3M0065090D

Typical Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch Mode Power Supplies

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			900	V	T_C = 25°C	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	Note 1
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/15			Static	Note 2
DC Continuous Drain Current	I_D			36	A	V_{GS} = 15 V, T_C = 25 °C, T_J ≤150 °C	Fig. 19
				23		V_{GS} = 15 V, T_C = 100 °C, T_J ≤150 °C	
Pulsed Drain Current	I_{DM}			90		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Avalanche energy, Single Pulse	E_{AS}			110	mJ	I_D = 22A, V_{DD} = 50V	
Power Dissipation	P_D			125	W	T_C = 25 °C, T_J = 150°C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +150	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

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Electrical Characteristics (T_C = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	900	—	—	V	V_{GS} = 0 V, I_D = 100 µA	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.1	3.5	V	V_{DS} = V_{GS}, I_D = 5 mA	Fig. 11
		—	1.6	—		V_{DS} = V_{GS}, I_D = 5 mA, T_J = 150℃	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	100	µA	V_{DS} = 900 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	65	78	mΩ	V_{GS} = 15 V, I_D = 20 A	Fig. 4, 5, 6
		—	90	—		V_{GS} = 15 V, I_D = 20 A, T_J = 150°C	
Transconductance	g_{fs}	—	16	—	S	V_{DS} = 20 V, I_{DS} = 20 A	Fig. 7
			13			V_{DS} = 20 V, I_{DS} = 20 A, T_J = 150°C	
Input Capacitance	C_{iss}	—	760	—	pF	V_{GS} = 0 V, V_{DS} = 600 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Output Capacitance	C_{oss}	—	66	—			
Reverse Transfer Capacitance	C_{rss}	—	5	—			
Output Capacitance Stored Energy	E_{oss}	—	16	—	µJ		Fig. 16
Turn-On Switching Energy (Body Diode FWD)	E_{on}	—	250	—		V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 20 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH, T_J = 150°C	Fig. 26 Note 3
Turn Off Switching Energy (Body Diode FWD)	E_{off}	—	48	—			
Turn-On Delay Time	$t_{d(on)}$	—	36	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 20 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27
Rise Time	t_r	—	10	—			
Turn-Off Delay Time	$t_{d(off)}$	—	14	—			
Fall Time	t_f	—	9	—			
Internal Gate Resistance	$R_{G(int)}$	—	3.5	—	Ω	f = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}	—	9	—	nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 20 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	12	—			
Total Gate Charge	Q_g	—	33	—			

Reverse Diode Characteristics (T_C = 25℃ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	4.4	—	V	V_{GS} = -4 V, I_{SD} = 10 A	Fig. 8, 9, 10
		4.0	—		V_{GS} = -4 V, I_{SD} = 10 A, T_J = 150°C	
Continuous Diode Forward Current	I_S	—	23.5	A	V_{GS} = -4 V	
Diode Pulse Current	I_{SM}	—	90		V_{GS} = -4 V, pulse width t_P limited by $T_{j\,max}$	
Reverse Recovery Time	t_{rr}	28	—	nS	V_{GS} = -4 V, I_{SD} = 20 A, V_R = 400 V dif/dt = 1245 A/µs, T_J = 150°C	
Reverse Recovery Charge	Q_{rr}	185	—	nC		
Peak Reverse Recovery Current	I_{rrm}	10	—	A		

Thermal Characteristics

Parameter	Symbol	Max	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.0	°C/W	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

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Typical Performance

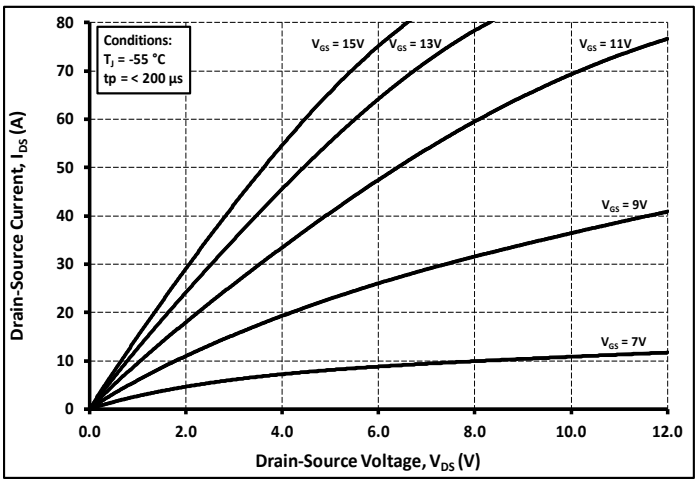


Figure 1. Output Characteristics T_J = -55°C

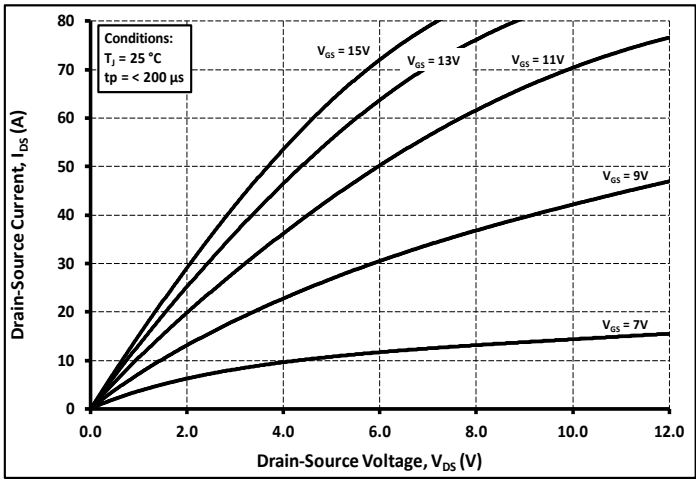


Figure 2. Output Characteristics T_J = 25°C

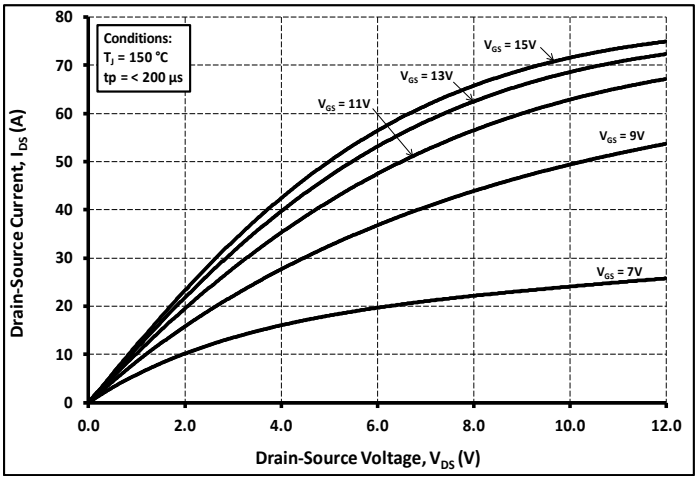


Figure 3. Output Characteristics T_J = 150°C

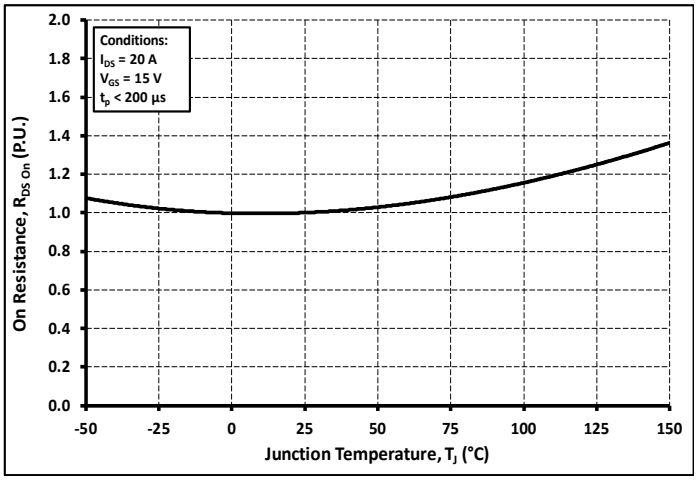


Figure 4. Normalized On-Resistance vs. Temperature

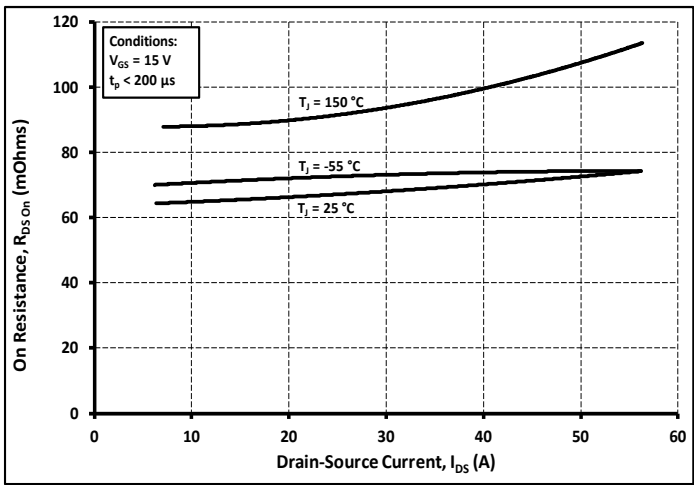


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

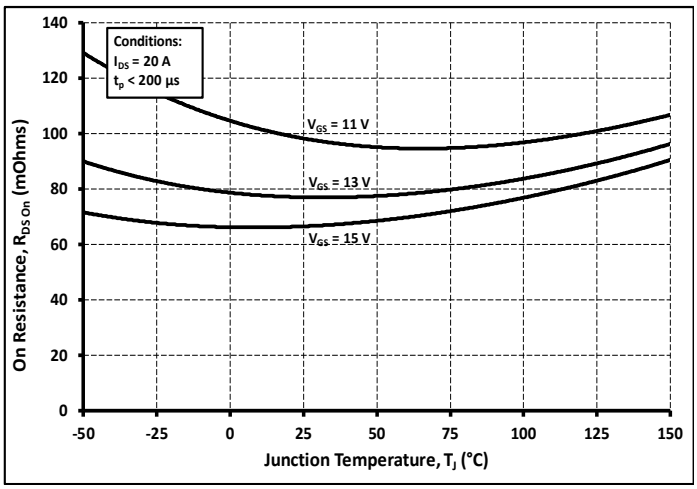


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

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Typical Performance

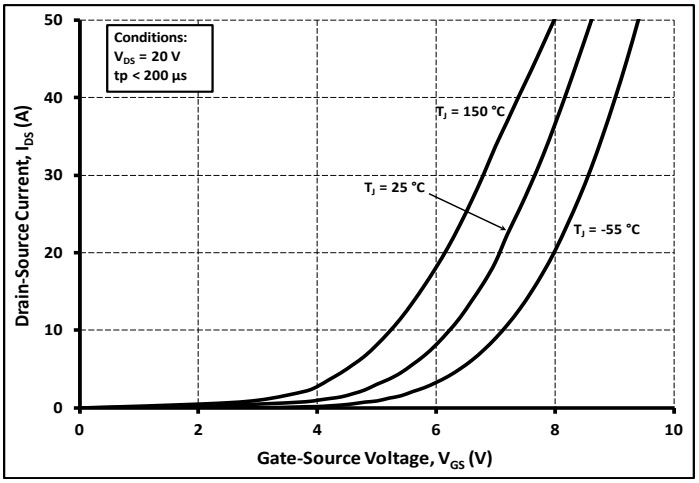


Figure 7. Transfer Characteristic for Various Junction Temperatures

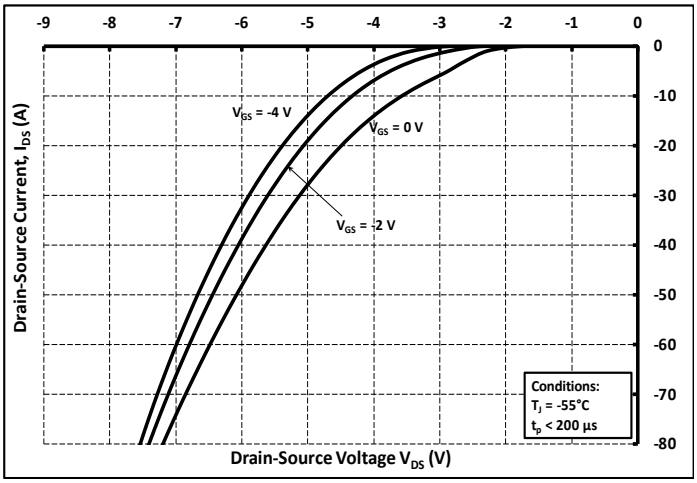


Figure 8. Body Diode Characteristic at -55°C

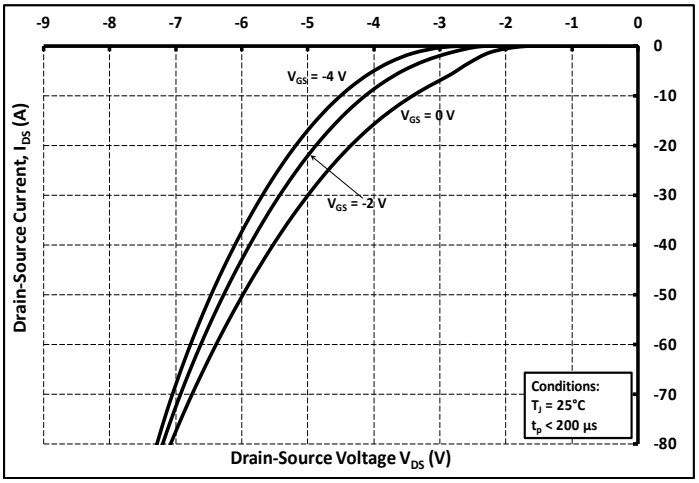


Figure 9. Body Diode Characteristic at 25°C

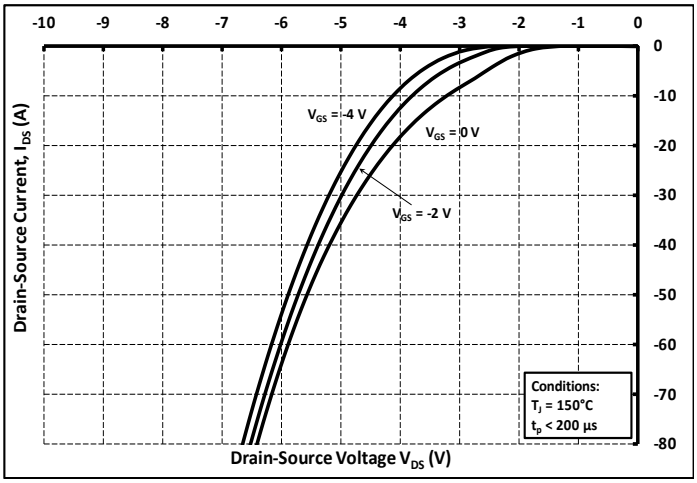


Figure 10. Body Diode Characteristic at 150°C

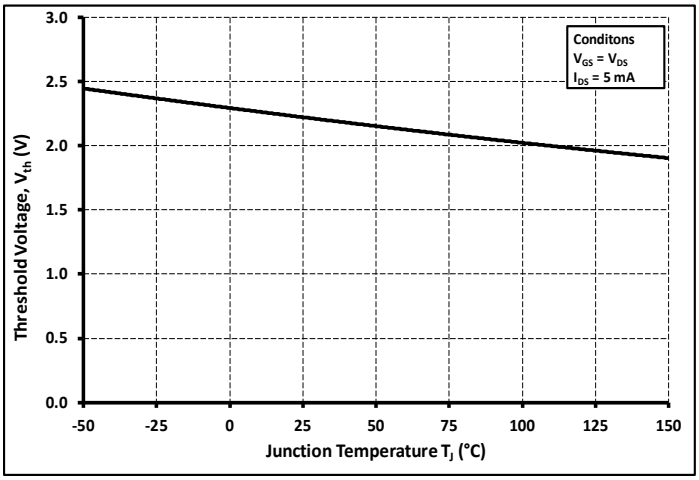


Figure 11. Threshold Voltage vs. Temperature

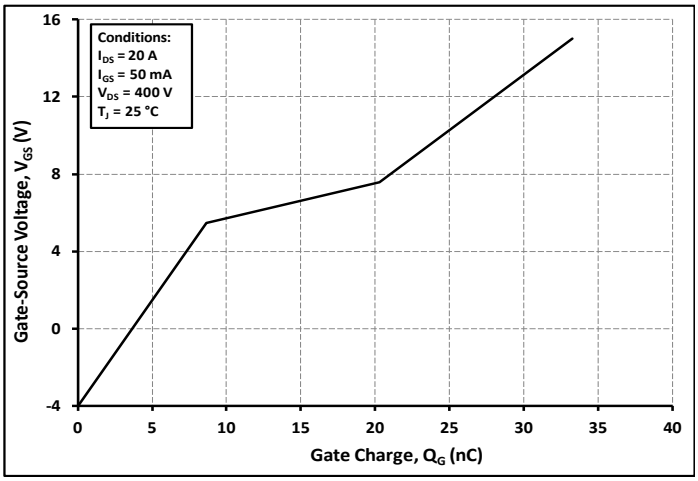


Figure 12. Gate Charge Characteristics

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Typical Performance

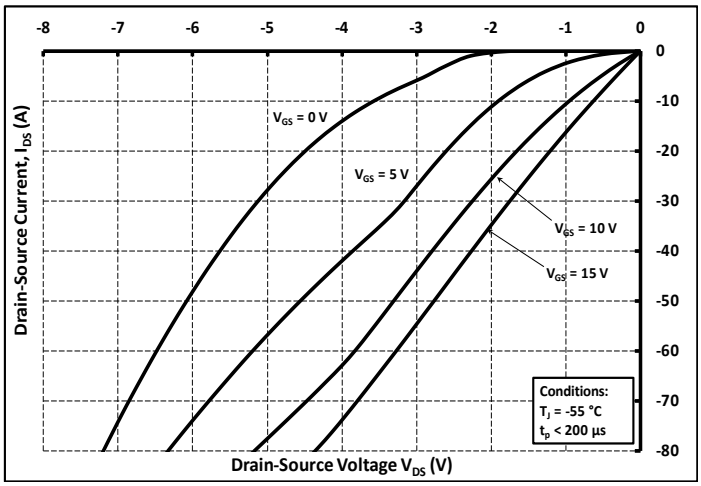


Figure 13. 3rd Quadrant Characteristic at -55°C

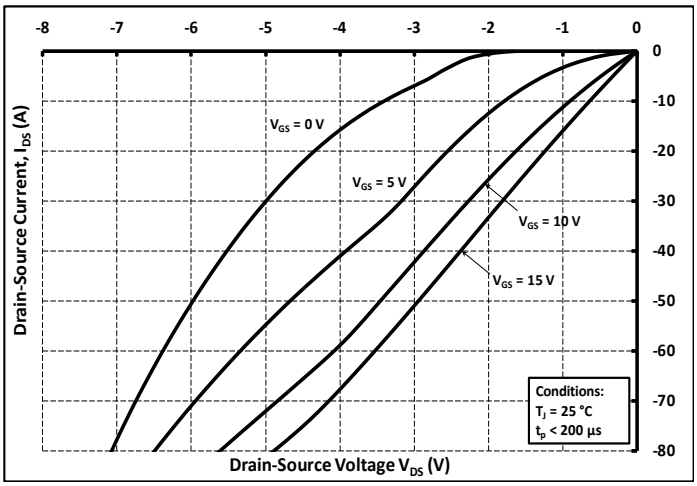


Figure 14. 3rd Quadrant Characteristic at 25°C

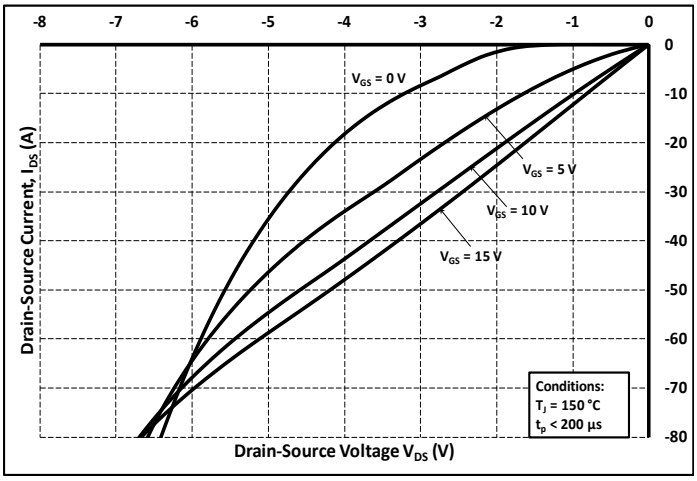


Figure 15. 3rd Quadrant Characteristic at 150°C

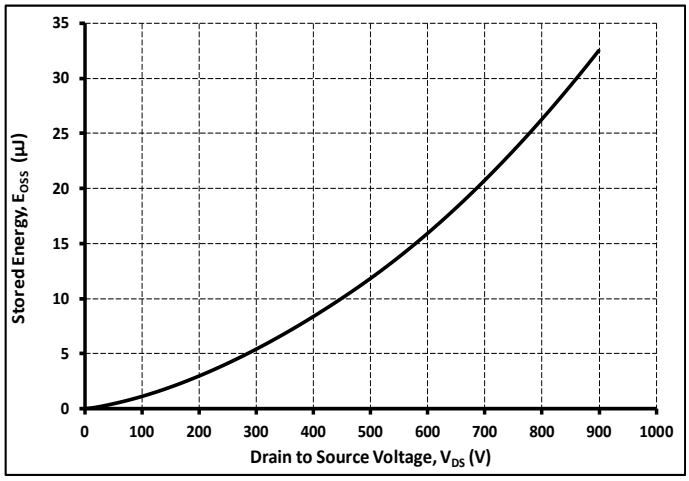


Figure 16. Output Capacitor Stored Energy

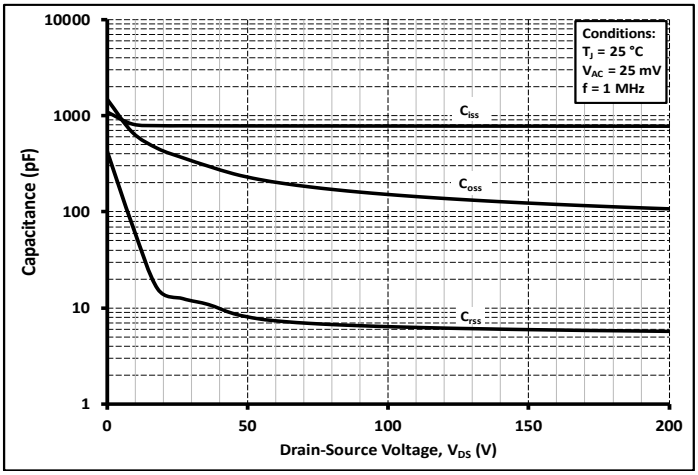


Figure 17. Capacitances vs Drain-Source Voltage (0 - 200 V)

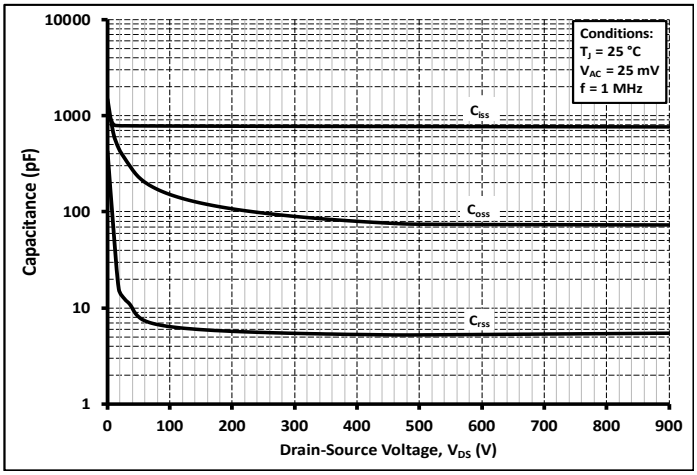


Figure 18. Capacitances vs Drain-Source Voltage (0 - 900 V)

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Typical Performance

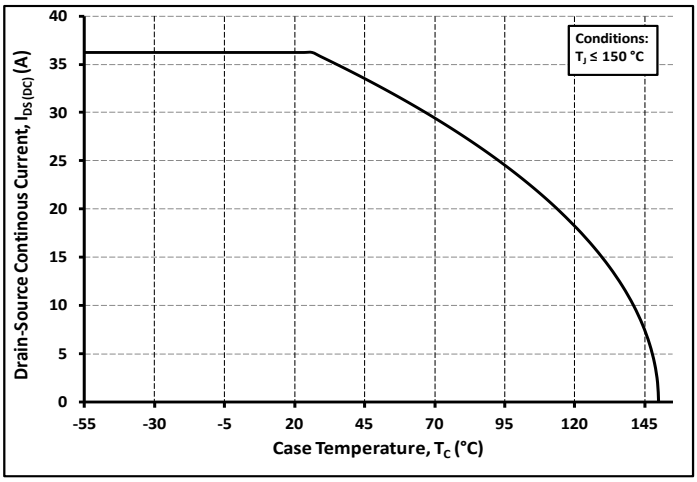


Figure 19. Continuous Drain Current Derating vs. Case Temperature

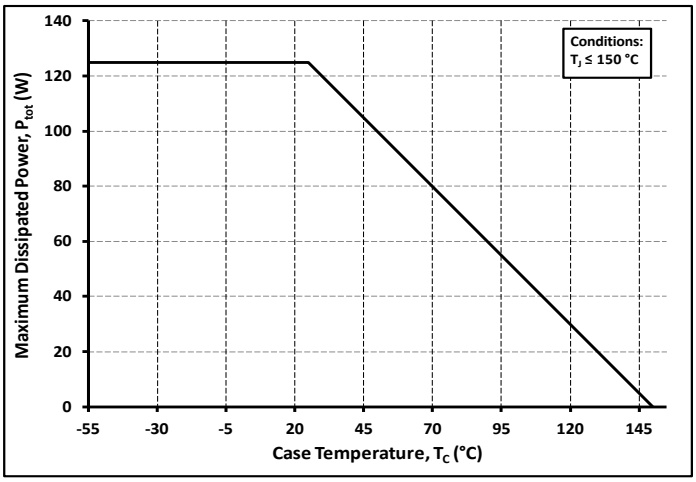


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

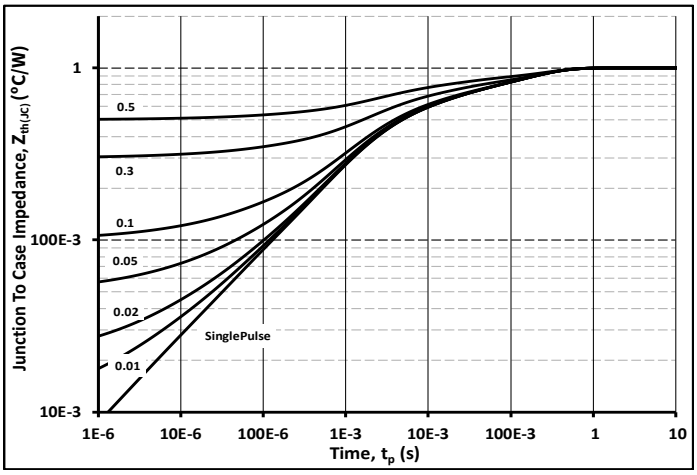


Figure 21. Transient Thermal Impedance (Junction - Case)

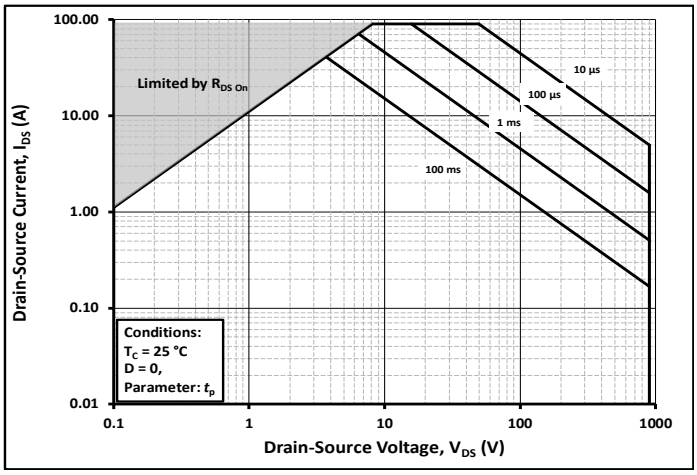


Figure 22. Safe Operating Area

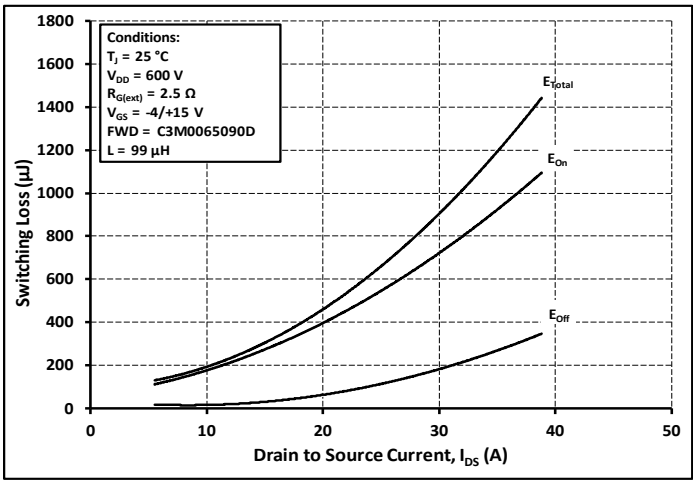


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600 V)

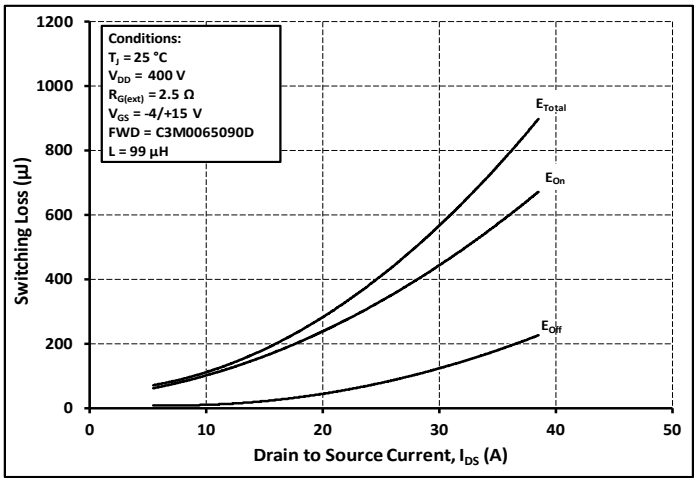


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400 V)

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Typical Performance

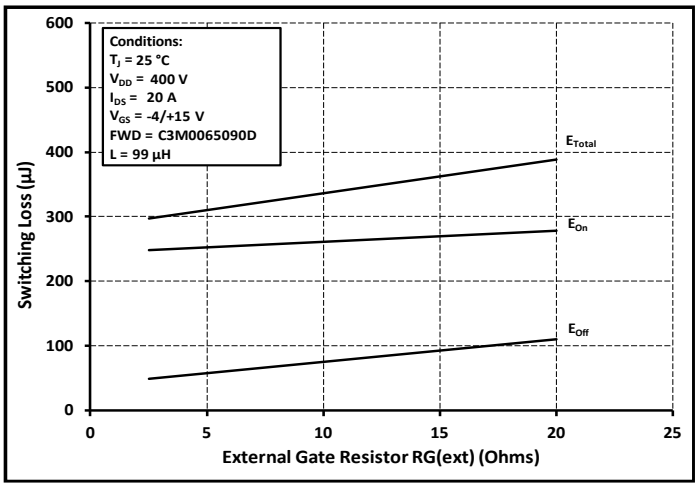


Figure 25. Clamped Inductive Switching Energy vs $R_{G(ext)}$

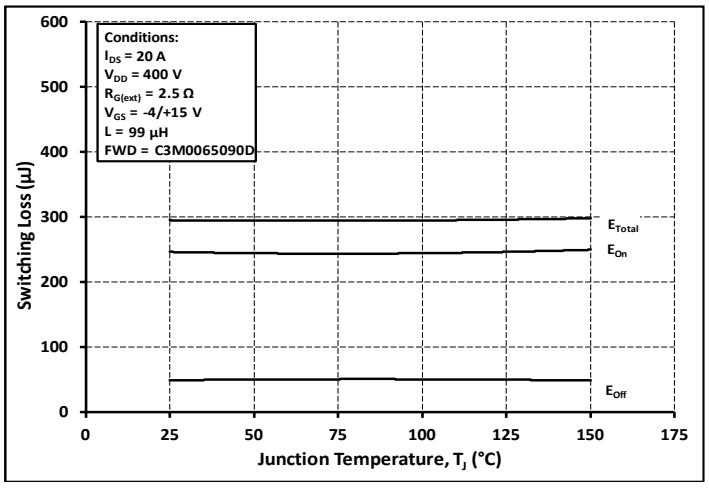


Figure 26. Clamped Inductive Switching Energy vs Temperature

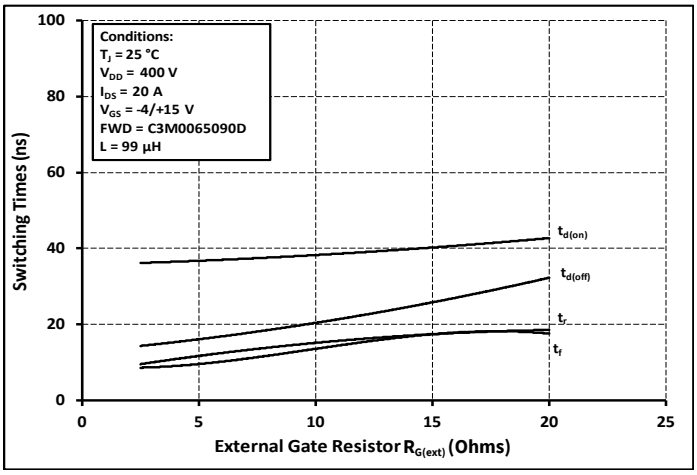


Figure 27. Switching Times vs. $R_{G(ext)}$

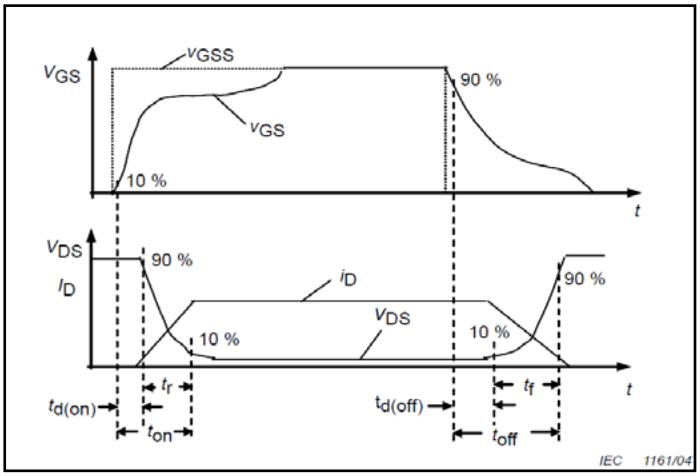


Figure 28. Switching Times Definition

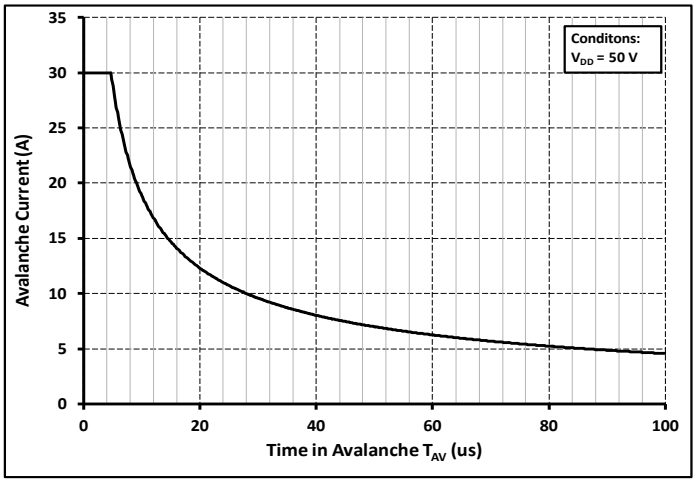


Figure 29. Single Avalanche SOA curve

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Test Circuit Schematic

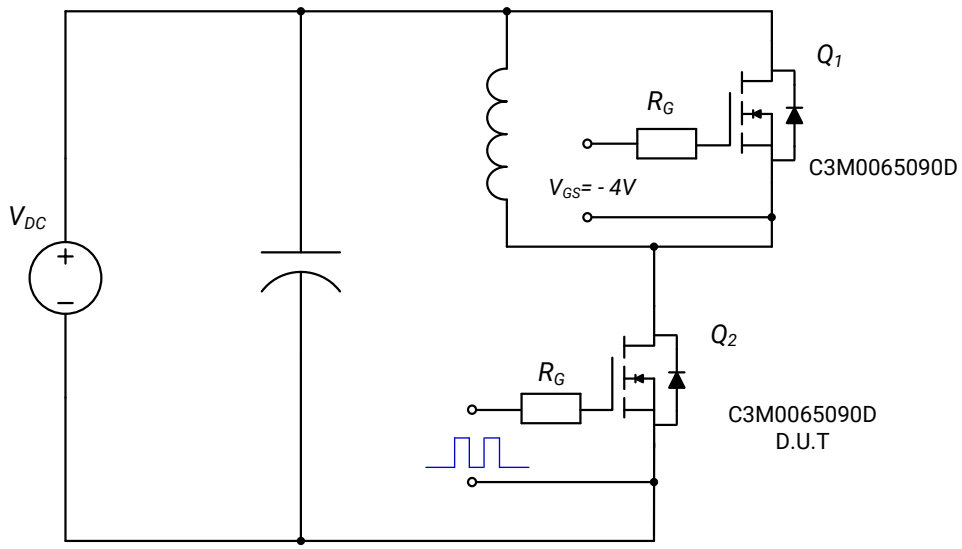
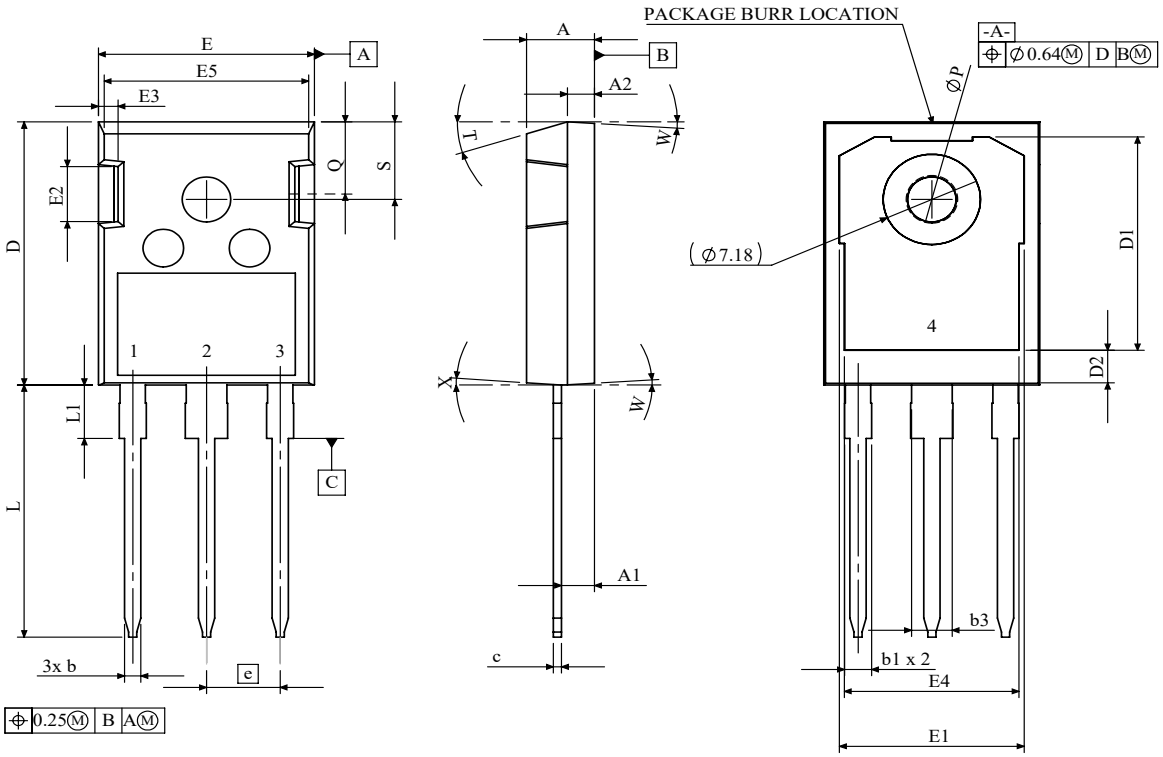


Figure 30. Clamped Inductive Switching Waveform Test Circuit

Note:
Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

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Package Dimensions – Package TO-247-3



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.27	2.52
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.74
D	20.75	21.05
D1	16	17.4
D2	2.86	3.26
E	15.75	16.13
E1	13.5	14.55
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
E5	14.65	15.05
e	5.44 BSC	
L	19.73	20.48
L1	3.97	4.69
ØP	3.18	4.06
Q	5.42	5.96
S	5.85	6.49
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

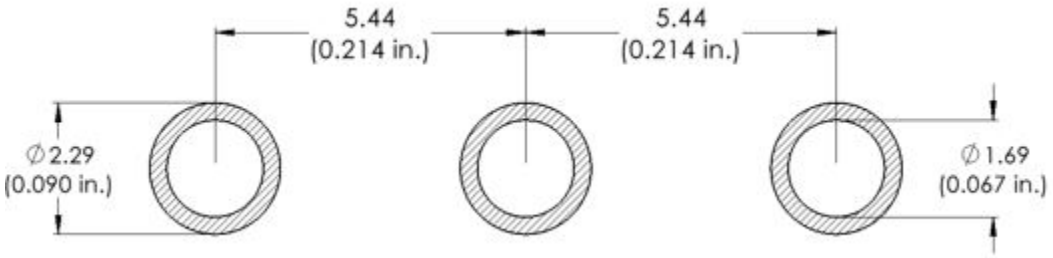
TITLE: PACKAGE OUTLINE DRAWING: TO-247-3L(MOSFET)

Date: 3/4/24 | REVISION NO. 02 | A4

PRD 05964 | SCALE:1:1 | SHEET 1 OF 1

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Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
D	June-2019	N/A
5	November-2023	Not Released
6	January-2024	Updated Wolfspeed branding, package drawing, package image, and solder pad layout, added Revision History Table, Table 1 layout revised
7	May-2024	Fig 25 extrapolation corrected, dynamic data updated
8	September - 2024	Legal Disclaimer, POD, Diode Pulse Current Symbol
9	September - 2026	Updated product marking

Related Links

- SPICE Models
- SiC MOSFET Isolated Gate Driver reference design
- SiC MOSFET Evaluation Board

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